

High-Performance, Multi-Mode Step-Down Controller

Features

- Single 3.3V or 5V Supply
- Supports Load Currents up to 40A
- Programmable Valley Current/Voltage Mode PWM Architecture
- 3.3V Logic PWM Output Compatible with Power Stage Modules and DrMOS Modules
- Single Tri-State PWM Output
- Programmable Switching Frequency: 200 kHz to 2 MHz
- Differential Remote Sensing for Output Voltage and Inductor Current
- 0.6V Reference Voltage with Total $\pm 1\%$ Accuracy for Output
- Adjustable Soft-Start/Soft-Stop and Pre-Biased Safe Startup
- Supports Light Load and Outside Audio Modes
- Programmable Slope Compensation and Loop Compensation
- Enable Input, Power Good (PG) Output for Sequencing
- Programmable OCP, Output OVP, Thermal OTP, and Dedicated FAULTb Pin for System Safe Startup/Stop
- Internal Thermal Shutdown and UVLO
- -40°C to $+125^{\circ}\text{C}$ Junction Temperature Range
- Available in 20-Lead 3 mm x 3 mm WQFN Package

Applications

- Servers and Work Stations
- Routers, Switches, Networking/Telecom Infrastructure
- Printers, Scanners, Graphics and Video Cards
- High Current, High Performance POLs

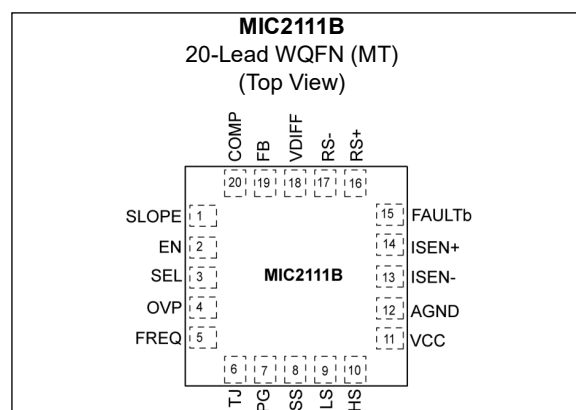
General Description

The MIC2111B is a programmable-frequency, valley current/voltage mode PWM controller that provides the control and protection features necessary for power devices and drivers that use current sensing across the inductor. The MIC2111B can provide single tri-state PWM logic signal to work with either power stage modules or discrete driver and MOSFETs. The device has precision enable and power good (PG) functions for sequencing of multiple power supplies. In addition, the solution is compatible with intelligent power stages in a high current, step-down DC/DC converter.

To optimize system size and system efficiency, the MIC2111B frequency can be programmed from 200 kHz to 2 MHz. The device operates in power saving mode at light loads by reducing frequency. Optional outside audio range operation is possible when the power stage is configured in light load mode. The solution uses differential current sensing for better current limit accuracy and a dedicated differential amplifier for remote output sensing for accurate output voltage control. The MIC2111B has a high gain transconductance amplifier for loop compensation. External slope compensation can be added through a resistor to avoid sub-harmonic oscillations. Other features include programmable OCP, output OVP, and thermal OTP protections. The MIC2111B offers Microchip's proprietary bi-directional, single wire fault communication for total system protection.

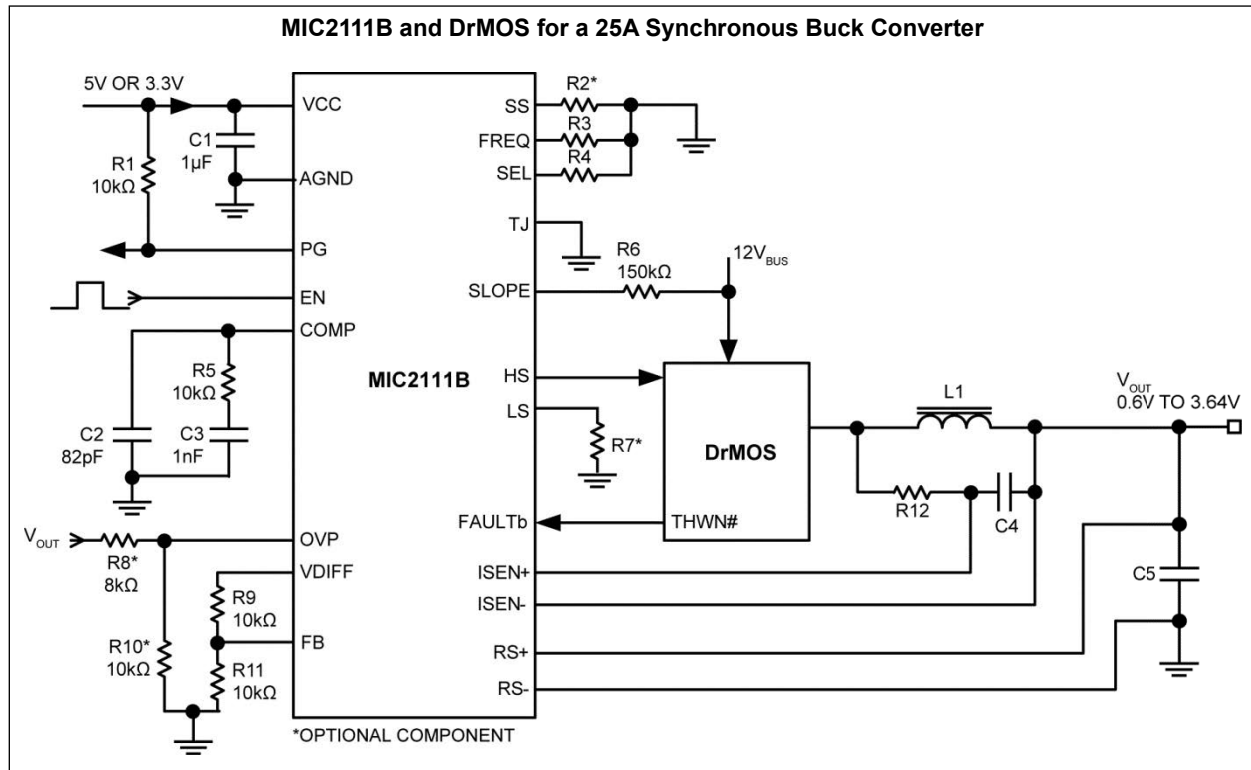
The MIC2111B is available in a 20-lead 3 mm x 3 mm WQFN package and has a junction temperature range of -40°C to $+125^{\circ}\text{C}$.

Package Type

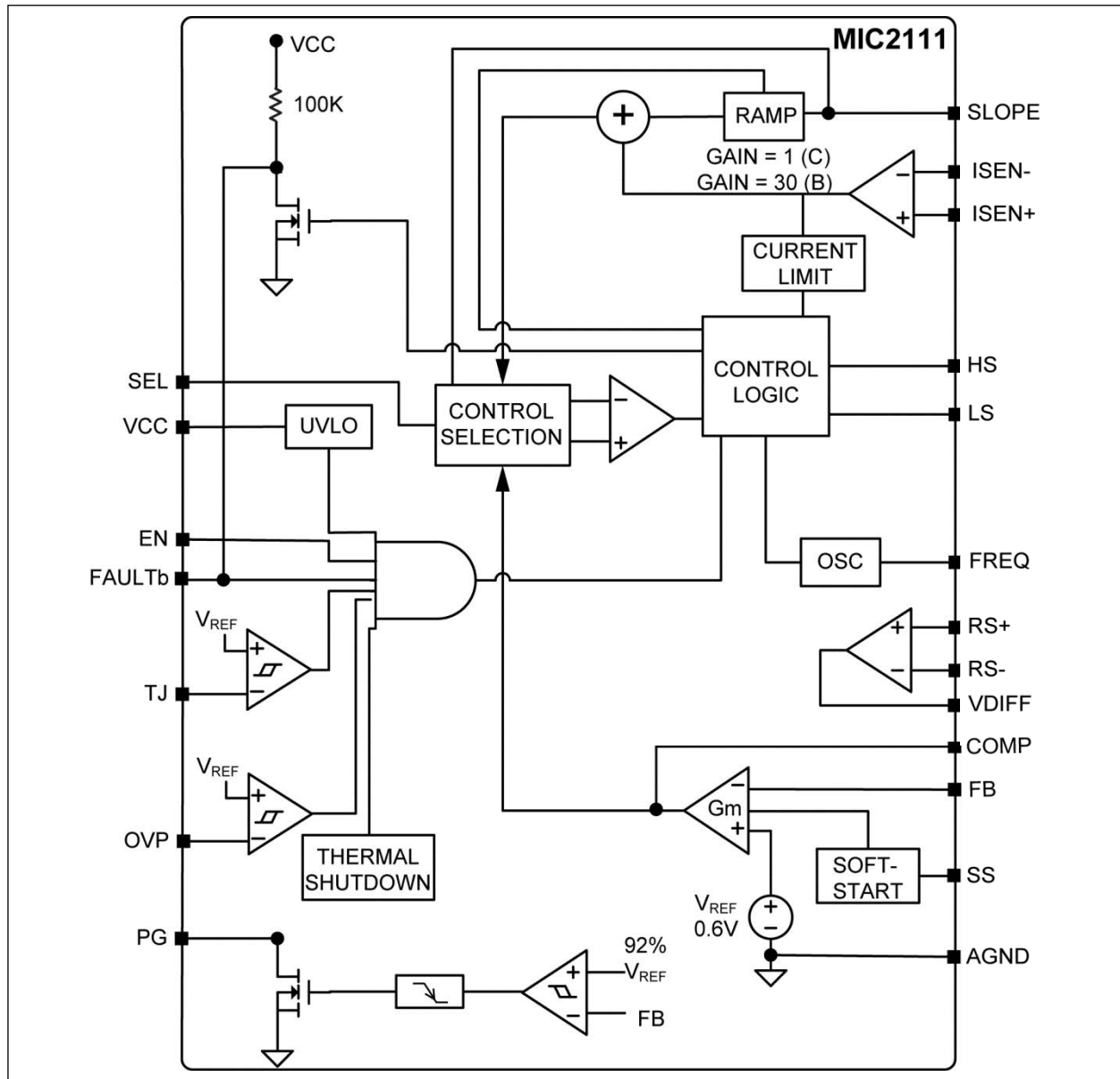


MIC2111B

Typical Application Circuit



Functional Block Diagram



MIC2111B

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{CC} to AGND.....	–0.3V to +6.0V
$V_{EN/SS}$, V_{FREQ} to AGND.....	–0.3V to (V_{CC} + 0.3V)
V_{OVP} , V_{TJ} , V_{FAULTb} to AGND.....	–0.3V to (V_{CC} + 0.3V)
$V_{RS\pm}$, $V_{HS/LS}$, $V_{ISEN\pm}$, V_{FB} to AGND.....	–0.3V to (V_{CC} + 0.3V)
V_{SLOPE} to AGND.....	–0.3V to +20V
ESD Rating	
Human Body Model (Note 1).....	2 kV
Machine Model.....	200V

Operating Ratings ‡

Supply Voltage (V_{CC}).....	+3.135V to +5.5V
Enable Input Voltage (V_{EN}).....	0V to V_{CC}

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions recommended. Human body model is 1.5 k Ω in series with 100 pF.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V; T_A = +25°C, unless noted. **Bold** values valid for $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$. [Note 1](#)

Parameter	Min.	Typ.	Max.	Units	Conditions
Power Supply Input (V_{CC})					
V_{CC} Input Voltage Range	3.135	—	5.5	V	Valley current mode, voltage mode
V_{CC} UVLO Threshold	2.75	2.85	2.95	V	V_{CC} rising
V_{CC} UVLO Hysteresis	—	100	—	mV	—
Quiescent Supply Current	—	2.1	—	mA	No switching, $V_{FB} > 0.8\text{V}$
Shutdown Supply Current	—	—	10	μA	$V_{EN} = 0\text{V}$
Output Voltage					
Output Voltage	0.6	—	3.46	V	—
Minimum V_{CC} -to-Output Set Point	—	—	1.3	V	Minimum $V_{CC} - V_{OUT}$ headroom required
Voltage Accuracy	0.594	0.6	0.606	V	($RS+$) – ($RS-$)
Remote Sense Amplifier Gain	0.997	1.000	1.003	V/V	$V_{DIFF}/[(V_{RS+}) - (V_{RS-})]$, $V_{RS-} = 0\text{V}$; $V_{RS+} = 3.6\text{V}$
Remote Sense Amplifier Source/Sink Current	550	—	—	μA	—
$RS+$ Input Impedance	—	175	—	k Ω	—
$RS-$ Input Impedance	—	87	—	k Ω	—
$RS+/RS-$ Common Mode Voltage	100	—	—	mV	—
FB Bias Current	—	5	100	nA	$V_{FB} = 0.6\text{V}$
Transconductance Error Amplifier					
Error Amplifier Transconductance	—	2	—	ms	FB-to-COMP g_m

ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_{CC} = 5V$; $T_A = +25^\circ C$, unless noted. **Bold** values valid for $-40^\circ C \leq T_J \leq +125^\circ C$. [Note 1](#)

Parameter	Min.	Typ.	Max.	Units	Conditions
Error Amplifier Source/Sink Current	175	220	—	μA	—
Enable/Soft-Start/Soft-Stop					
EN Threshold Voltage	1.0	1.2	1.3	V	EN rising, point at which the output is enabled
EN Hysteresis	—	50	—	mV	—
Soft-Start Time	—	2	—	ms	$R_{SS} = \text{Floating}$
Soft-Stop Time (Note 2)	—	2	—	ms	$R_{SS} = \text{Floating}$
Oscillator and PWM					
Switching Frequency	1.6	2	2.4	MHz	$R_{FREQ} = 49.9 \text{ k}\Omega$
	0.85	1	1.15		$R_{FREQ} = 100 \text{ k}\Omega$
	0.16	0.2	0.24		$R_{FREQ} = 499 \text{ k}\Omega$
Minimum Duty Cycle	—	0	—	%	$V_{FB} = 0.8V$
Minimum Off-Time	—	100	—	ns	CCM
Minimum On-Time	—	40	—	ns	CCM
HS, LS Logic High Voltage	4	—	—	V	$I_{LOAD} = 50 \text{ mA}$
HS, LS Logic Low Voltage	—	—	0.8	V	$I_{LOAD} = 50 \text{ mA}$
HS Tri-State Leakage Current	-1	—	1	μA	$V_{HS} = 1.5V$
LS Tri-State Leakage Current	-1	—	1	μA	$V_{LS} = 1.5V$
HS, LS Rise/Fall Time	—	1	—	ns	$C_{LOAD} = 20 \text{ pF}$
Outside Audio DCM Time	—	32	—	μs	No Load
Current-Sense Amplifier					
Current Amplifier Gain	—	30	—	V/V	—
Current Amplifier Bandwidth	—	10	—	MHz	3 dB bandwidth
Current Limit Threshold	15	18.3	22.5	mV	LS = 0.5V
	20	23.3	27.5		LS = 0.7V
ISEN+/ISEN- Input Bias Current	—	0.01	0.1	μA	—
Slope Compensation					
V_{SLOPE} Common-Mode Range	0.6	—	3.46	V	—
SLOPE Sink Current	—	—	280	μA	Valley Current Mode
Power Good (PG)					
Power Good Threshold Voltage	90	92	95	% V_{OUT}	FB rising
Power Good Hysteresis	—	2	—	% V_{OUT}	—
Power Good Delay	—	200	—	μs	FB rising, delay from FB high to PG high
Power Good Low Voltage	—	12	200	mV	$V_{FB} < 90\% \times V_{NOM}$, $I_{PG} = 1 \text{ mA}$
FAULTb					
FAULTb Threshold Voltage	2	3.1	—	V	FAULTb rising
FAULTb Hysteresis	—	1.1	—	V	—
FAULTb Low Voltage	—	10	50	mV	$I_{LOAD} = 500 \mu A$
FAULTb Leakage Current	—	—	1	μA	—
OVP					
OVP Threshold Voltage	0.585	0.6	0.615	V	OVP rising
OVP Hysteresis	—	20	—	mV	—
Thermal Shutdown					

MIC2111B

ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_{CC} = 5V$; $T_A = +25^{\circ}C$, unless noted. **Bold** values valid for $-40^{\circ}C \leq T_J \leq +125^{\circ}C$. [Note 1](#)

Parameter	Min.	Typ.	Max.	Units	Conditions
T_J Threshold Voltage	0.585	0.6	0.615	V	T_J rising
T_J Hysteresis	—	50	—	mV	—
Internal Thermal Shutdown	—	155	—	$^{\circ}C$	Temperature rising
Internal Thermal Shutdown Hysteresis	—	20	—	$^{\circ}C$	—

Note 1: Specifications for packaged product only.

2: Soft-stop is disabled by default. Contact factory to enable soft-stop.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	-40	—	+125	$^{\circ}C$	—
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+150	$^{\circ}C$	—
Storage Temperature Range	T_S	-65	—	+150	$^{\circ}C$	—
Lead Temperature	T_{LEAD}	—	—	+260	$^{\circ}C$	Soldering, 10 sec.
Package Thermal Resistances						
Thermal Resistance, WQFN 20-Ld	θ_{JA}	—	60	—	$^{\circ}C/W$	—
	θ_{JC}	—	10	—	$^{\circ}C/W$	—

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

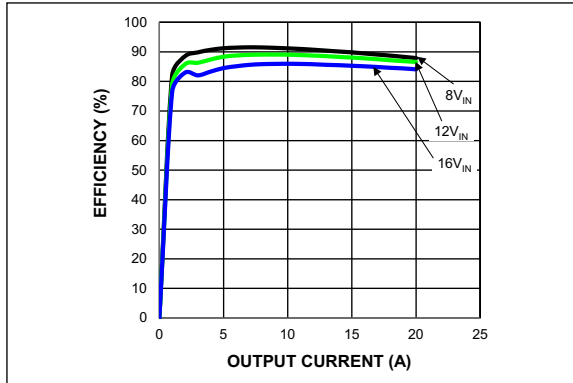


FIGURE 2-1: Efficiency vs. Output Current ($V_{OUT} = 1.2V$).

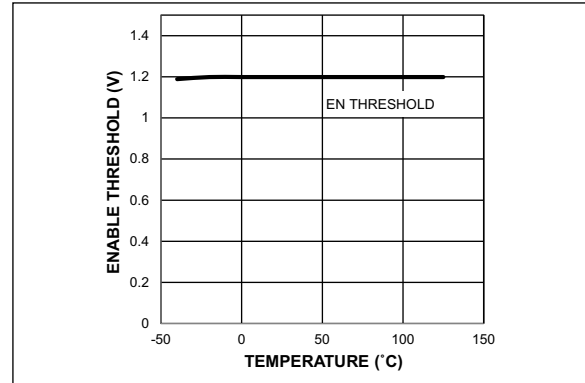


FIGURE 2-4: EN Threshold vs. Temperature.

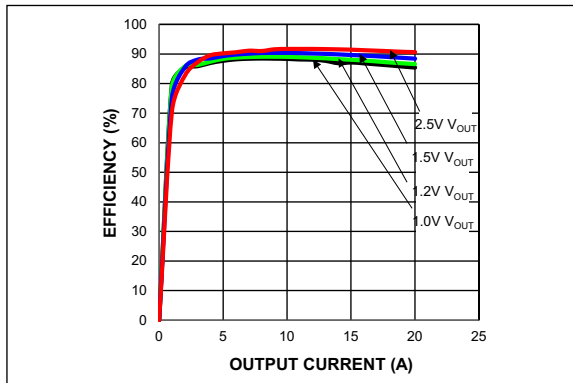


FIGURE 2-2: Efficiency vs. Output Current ($V_{OUT} = 12V$).

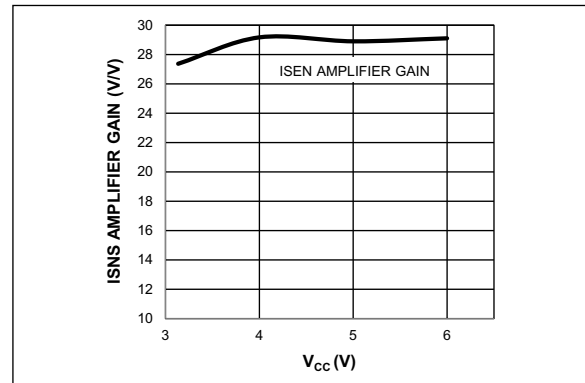


FIGURE 2-5: ISEN Amplifier Gain vs. V_{CC} .

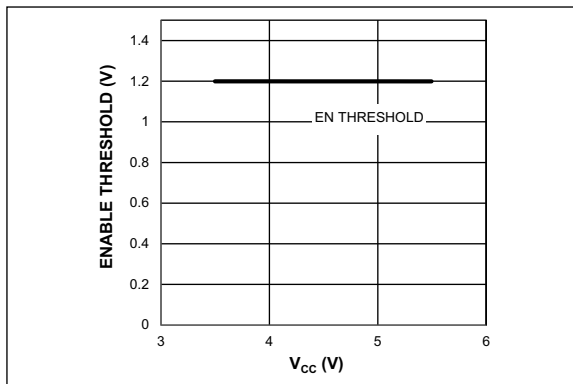


FIGURE 2-3: EN Threshold vs. V_{CC} Change.

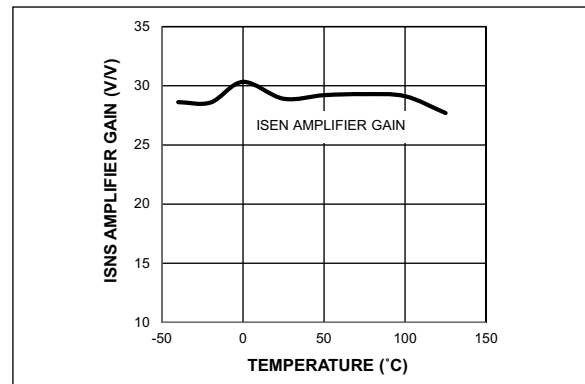


FIGURE 2-6: ISEN Amplifier Gain vs. Temperature.

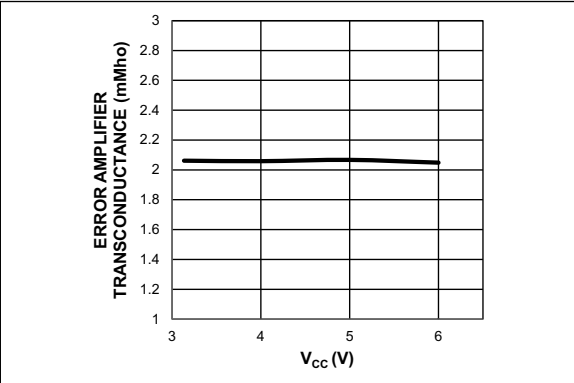


FIGURE 2-7: Error Amplifier Transconductance vs. V_{CC} (T = 25°C).

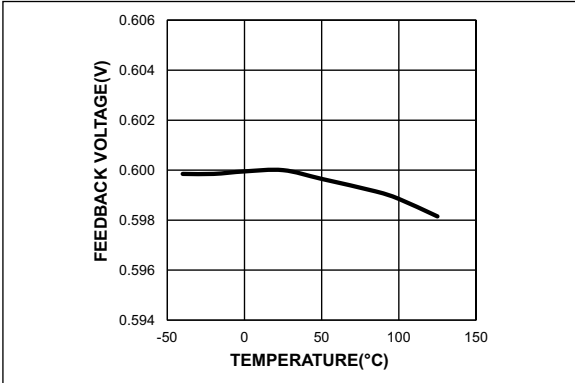


FIGURE 2-10: Feedback Voltage vs. Temperature.

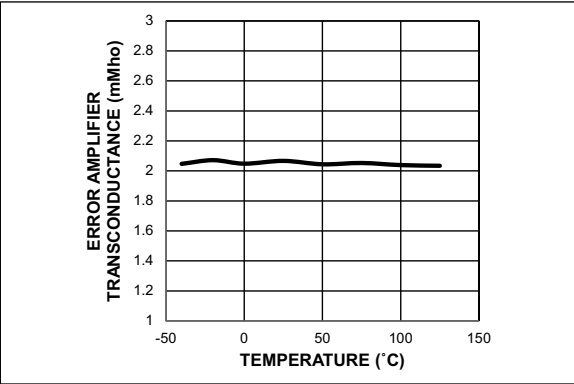


FIGURE 2-8: Error Amplifier Transconductance vs. Temperature (V_{CC} = 5V).

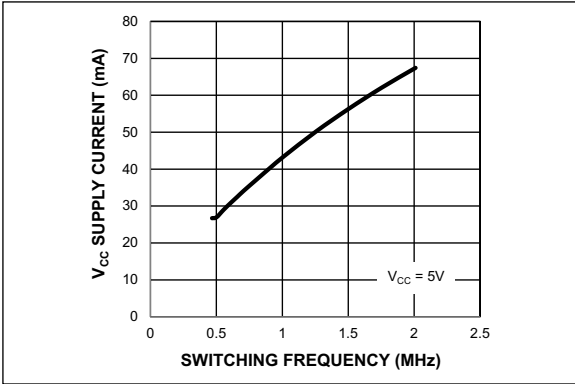


FIGURE 2-11: V_{CC} Supply Current vs. Switching Frequency.

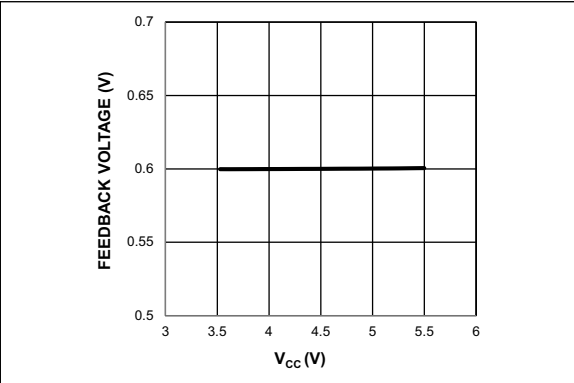


FIGURE 2-9: Feedback Voltage vs. V_{CC}.

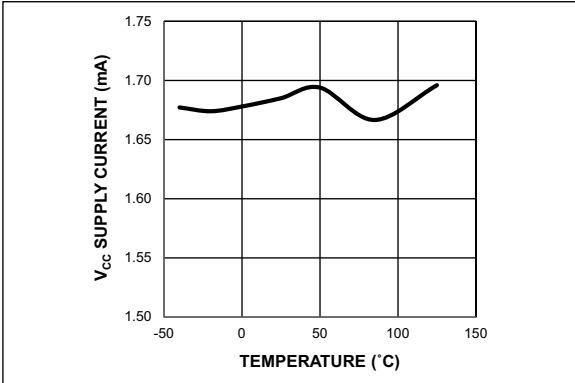


FIGURE 2-12: V_{CC} Supply Current vs. Temperature.

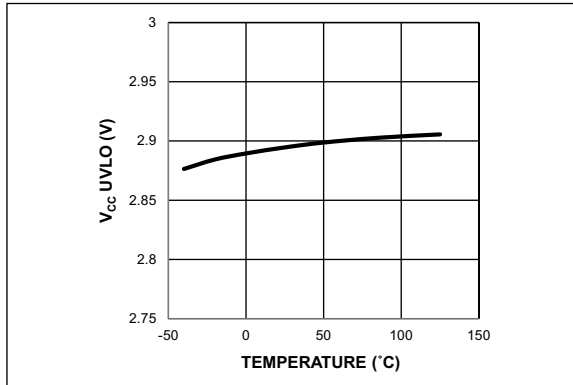


FIGURE 2-13: V_{CC} UVLO vs. Temperature.

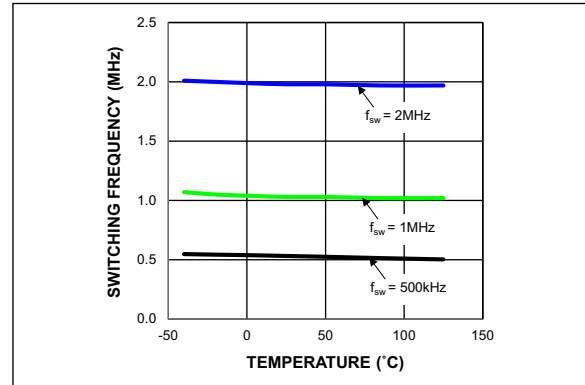


FIGURE 2-16: Switching Frequency vs. Temperature.

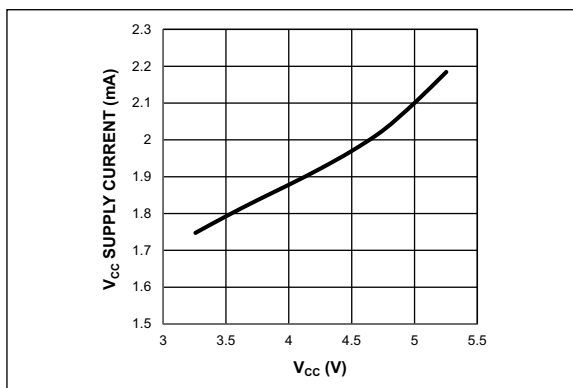


FIGURE 2-14: V_{CC} Quiescent Current vs. V_{CC} Voltage.

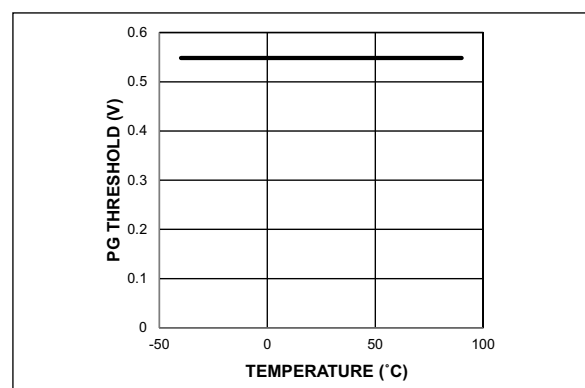


FIGURE 2-17: PG Threshold vs. Temperature.

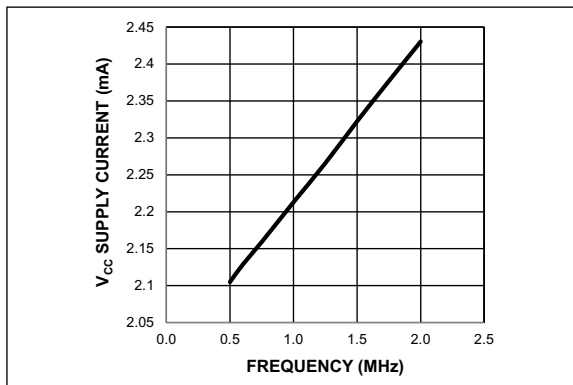


FIGURE 2-15: V_{CC} Quiescent Current vs. Frequency.

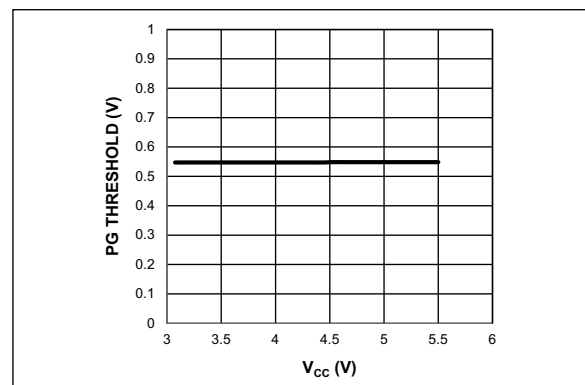


FIGURE 2-18: PG Threshold vs. V_{CC} .

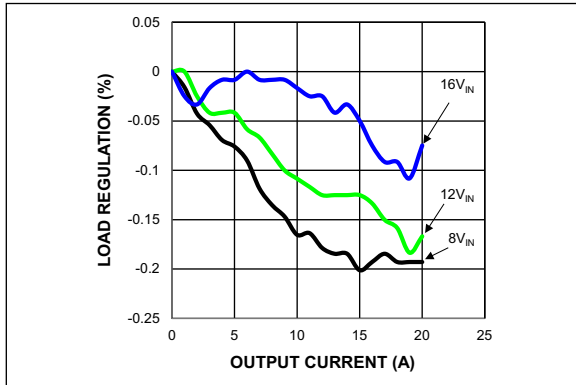


FIGURE 2-19: Load Regulation vs. Output Current.

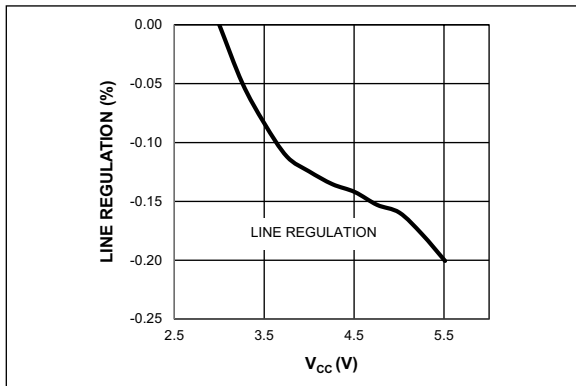


FIGURE 2-20: Line Regulation vs. V_{CC} ($V_{IN} = 12V$, $V_{OUT} = 1.2V$, 5A Load).

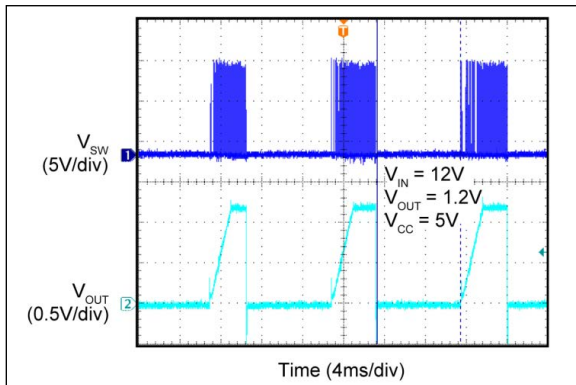


FIGURE 2-21: Short Circuit.

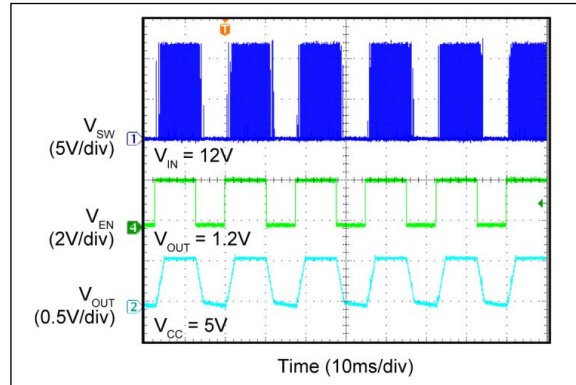


FIGURE 2-22: Enable Start and Disable Toggling.

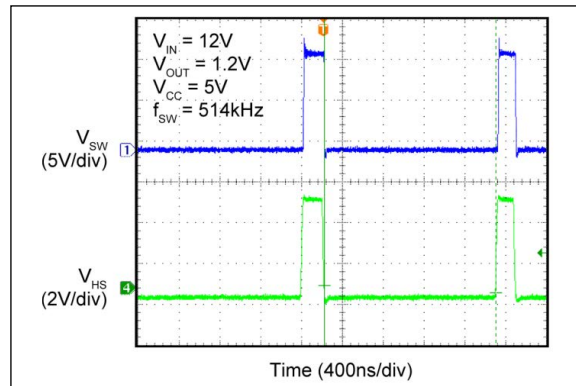


FIGURE 2-23: Switching Waveforms.

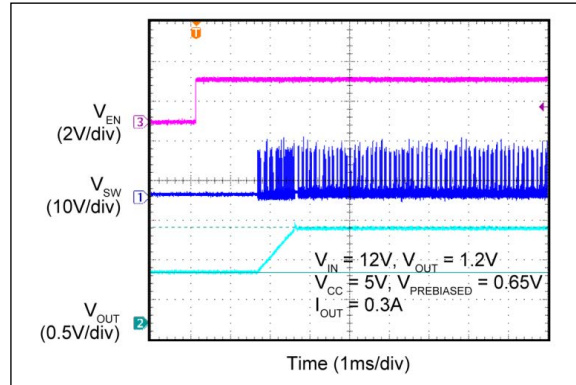


FIGURE 2-24: Pre-Biased Start-Up.

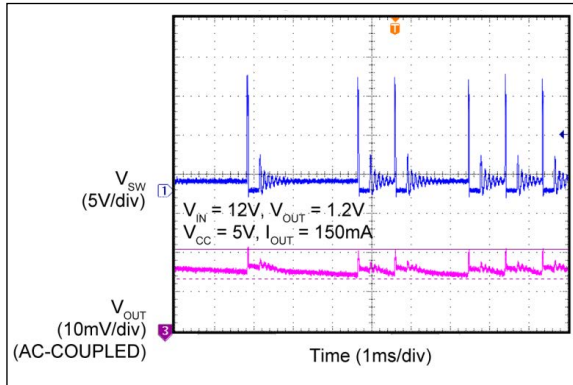


FIGURE 2-25: Switching Waveforms (Light Load Conditions).

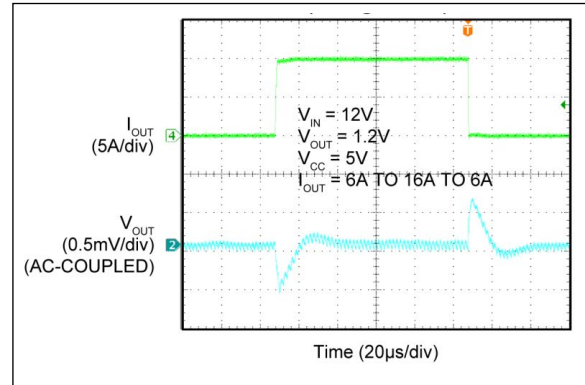


FIGURE 2-28: Transient Condition (Voltage Mode).

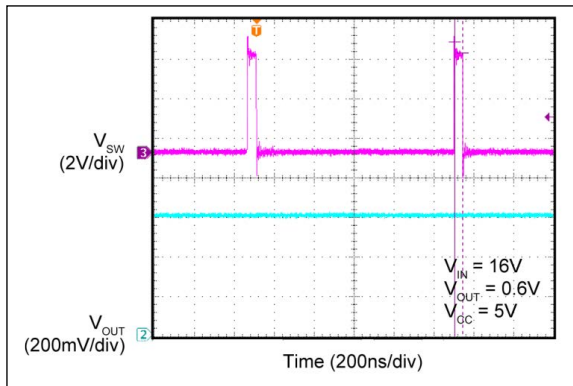


FIGURE 2-26: Minimum On-Time.

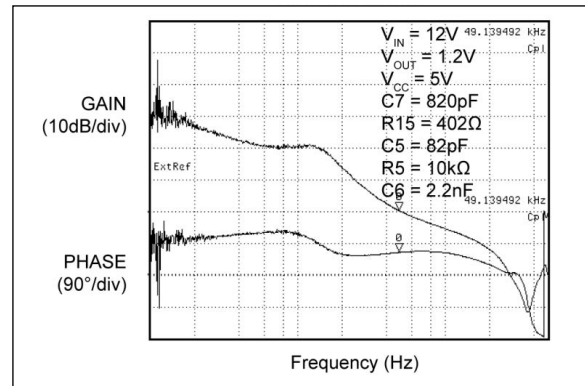


FIGURE 2-29: Bode Plot (Voltage Mode).

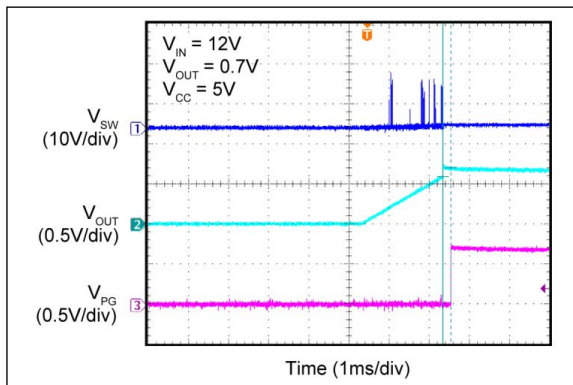


FIGURE 2-27: Start-Up Condition.

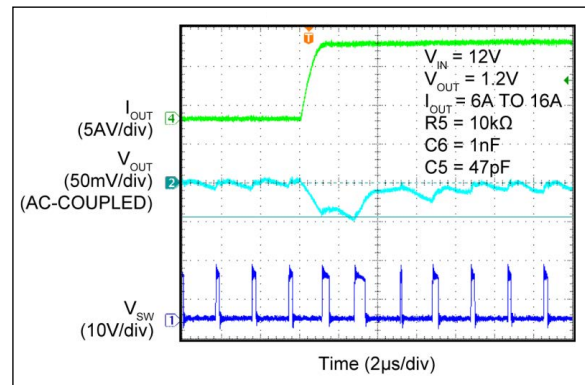


FIGURE 2-30: Transient Response (Valley Current Mode).

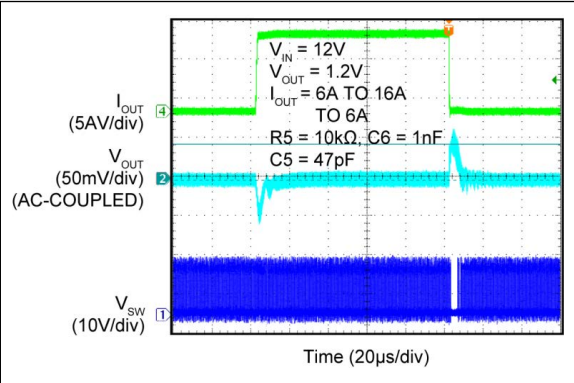


FIGURE 2-31: Transient Response (Valley Current Mode).

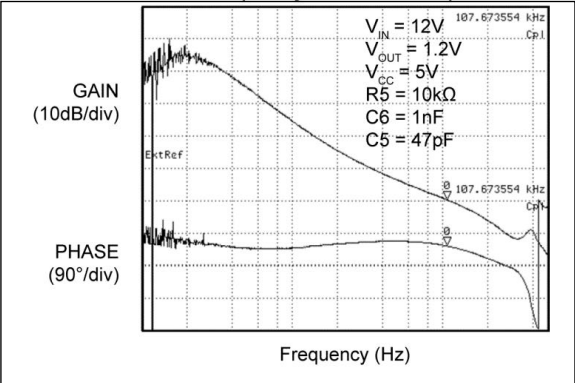


FIGURE 2-32: Bode Plot (Valley Current Mode).

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	I/O	Pin Name	Description
1	I	SLOPE	Valley Current Mode: Slope compensation can be adjusted by adding a resistor from this pin to VIN (input power supply). Voltage Mode: Artificial ramp controlled by SLOPE resistor.
2	I	EN	Enable (Input): A logic signal to enable or disable the controller. The EN pin is CMOS compatible. Logic high = enable, logic low = disable or shutdown. Do not leave floating.
3	I	SEL	Control Mode Selection Pin: Connect this pin to AGND for valley current mode operation. Leave this pin open for voltage mode control operation.
4	I	OVP	Output OVP programming pin. Connect a resistive divider to set OVP. OVP pin has 0.6V reference (see Functional Description for more details).
5	I	FREQ	Switching Frequency Adjust (Input): Connect a resistor from this pin to GND to set the switching frequency.
6	I	TJ	Power Module Temperature Sense Pin. Connect resistor divider to program TJ. TJ comparator has 0.6V reference (see Functional Description for more details).
7	O	PG	Power Good (Output): Open-drain output, an external resistor to VOUT is required for pull-up.
8	I	SS	Soft-start pin for limiting inrush current. A resistor from this pin to ground sets the soft-start time. If enabled, soft-stop time is same as soft-start. Contact factory for soft-stop.
9	I/O	LS	Low-Side Logic Output. Connect this pin to the module mode pin for outside audio operation. Leave this pin open if outside audio (>25 kHz) operation is not required. Current limit can be adjusted by connecting a resistor from LS to AGND (see Table 4-1 for details).
10	O	HS	High-Side Logic of Power Module Top FET. Connect this pin to the PWM pin of power module. This pin has tri-state capability.
11	P	VCC	5V Supply Input. A 1 μ F ceramic capacitor from VCC to AGND is required for decoupling.
12	P	AGND	Analog Ground.
13	I	ISEN–	Negative pin of the inductor current sense input.
14	I	ISEN+	Positive pin of the inductor current sense input.
15	I/O	FAULTb	Bi-Directional Pin. This pin goes low if controller or module is not ready. This pin goes low if V _{CC} is less than UVLO, or if a TJ or OVP fault is triggered. Either VCC cycling or EN cycling is required to clear the fault. This pin has an internal 100 k Ω pull-up resistor to VCC.
16	I	RS+	The non-inverting input of the remote sensing amplifier. Remote sense for output voltage.
17	I	RS–	The inverting input of the remote sensing amplifier. Remote sense for GND.
18	O	VDIFF	Output of differential amplifier. Connect a resistor divider from VDIFF to set output voltage
19	I	FB	The inverting input of the error amplifier.
20	I/O	COMP	Transconductance Amplifier Output. Connect compensation network from COMP node for frequency response.

4.0 FUNCTIONAL DESCRIPTION

The MIC2111B is a pin-programmable control mode, single phase PWM buck controller. The control mode can be programmed to either valley current mode or voltage mode through a single pin. The device provides the control and protection features necessary for driving intelligent power stages in high current, step-down, DC/DC converters. The MIC2111B is also compatible with DrMOS power stages and drivers that use current sensing across the inductor. The MIC2111B provides a single tri-state, PWM logic signal that works with either power stage modules or discrete driver MOSFETs. It has precision enable and power good (PG) functions for sequencing of multiple power supplies and its frequency can be programmed from 200 kHz to 2 MHz, thereby optimizing system size and system efficiency.

The device supports power saving mode at light loads when the MODE pin of the power stage is connected to GND. Optional outside audio range operation is also possible when the power stage is configured in light load mode. The MIC2111B uses differential current sensing for better current limit accuracy. It also uses a dedicated differential amplifier for remote output sensing to achieve accurate output voltage control. The MIC2111B has a high gain transconductance amplifier for easier loop compensation. External slope compensation can be added through a resistor to avoid sub-harmonic oscillations. The MIC2111B has programmable OCP, output OVP and thermal OTP protections and offers Microchip's proprietary bi-directional, single-wire fault communication for total system protection.

4.1 Control Architecture

The MIC2111B is a pin-programmable multi-mode, single phase PWM buck controller that can be operated under valley current mode and voltage mode control architectures.

4.1.1 VALLEY CURRENT MODE

When MIC2111B is programmed to a fixed-frequency, valley current mode control architecture, the inductor current is sensed by the voltage drop measured across the DCR of the inductor (MIC2111B). The current is sensed during the off period of the switching cycle and is conditioned with the internal current sense amplifier. The gain of the current sense amplifier is 30V/V. The output signal of the current sense amplifier is compared with the current programmed by the error amplifier to determine the correct duty cycle. Slope compensation is added via a resistor between VIN and the SLOPE pin. The MIC2111B generates a $(V_{IN} - V_{OUT})$ proportional current and passes it through a capacitor to generate the slope compensation ramp.

This slope compensation ramp is then added to comp signal to avoid sub-harmonic oscillations for duty cycles of less than 50%.

Calculation of R_{SLOPE} can be found in the [Application Information](#) section.

4.1.2 VOLTAGE MODE

The MIC2111B can also be configured as voltage mode control scheme for noise sensitive applications. Control loop compensation is external for providing maximum flexibility in choosing the operating frequency and output LC filter components. Ramp is generated by connecting a resistor between VIN and SLOPE. An internal transconductance error amplifier produces an integrated error voltage at COMP that helps to provide higher DC accuracy. The voltage at COMP sets the duty cycle using a PWM comparator and a ramp generator. On the rising edge of an internal clock, the PWM turns on. During this ON time, inductor current ramps up. Internal comparator turn OFF PWM once appropriate duty cycle is reached. During this time inductor releases the stored energy as the inductor current ramps down, providing current to the output.

4.2 Oscillator Frequency

The MIC2111B has an internal oscillator wherein the frequency can be set through an external resistor at the FREQ pin. The switching frequency can be programmed from 200 kHz to 2 MHz using Equation 4-1:

EQUATION 4-1:

$$R_{FREQ} = 10^{11} / f_{SW}[\Omega]$$

Where:

f_{SW} = Desired switching frequency in Hz.

4.3 PWM Modes and Logic Levels

There are multiple versions of power stages currently on the market that support different load currents. These include DrMOS and other intelligent power stages. All these power stages contain a MOSFET driver, high-side and low-side MOSFETs. These power stages require a single tri-stated PWM control signal for control and protection ([Table 4-1](#)).

TABLE 4-1: PWM TRUTH TABLE

LS	HS	High-Side FET	Low-Side FET	Switch Node
0	0	OFF	ON-to-OFF	Diode Emulation
0	1	ON	OFF	High
X	Tri-State	OFF	OFF	Tri-State (Pre-Bias/Fault Shut-down)
1	0	OFF	ON	Low
1	1	ON	OFF	High

The MIC2111B will output a PWM signal on the HS pin with levels of 0 (turn on the low-side driver) and 1 (turn on the high-side driver). HS will be turned high-impedance (tri-state) when a fault condition exists which should be interpreted by the power stage to turn-off both the high-side driver and low-side driver. MIC2111B supports 3.3V logic-compatible PWM thresholds on HS. These levels can found in the “Oscillator and PWM” section of the [Electrical Characteristics](#) table.

4.4 Programmable Current Limit and Hiccup Mode

MIC2111B has a dedicated current sense amplifier and can support high load currents up to 40A in single phase configuration. The MIC2111B also features differential current sense input pins (ISEN+ and ISEN-).

With the MIC2111B, it is possible to sense current across inductor DCRs for low-cost applications. As the DCR of the inductor will be less than 1 mΩ for a high current application, the MIC2111B features a current sense amplifier with a gain of 30V/V. This amplified signal is used for control and cycle-by-cycle current limit. These high current applications need thermal compensation from the current sense signal because of DCR variation with temperature. External thermal compensation could be provided using an NTC resistor in series with the RC across the inductor. See the [Application Information](#) section for more details about thermal compensation and filter calculations.

Current limit can be programmed through an external resistor connected at the LS pin. The MIC2111B provides two selectable current limit thresholds. During start-up, a current source of 8 μA is injected into the external resistor connected between the LS pin and GND. The voltage developed across the resistor is measured as part of the power-up sequence and the current threshold determined as illustrated in [Table 4-2](#).

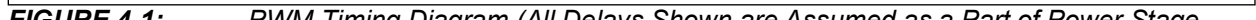
Once the voltage has been measured, the current source is turned off. If LS is connected to the MODE pin of DrMOS, current limit setting resistance must be adjusted for the input resistance of the MODE pin.

Many high current applications require hiccup mode protection for current limit because they can see peak load currents for a very short duration. The MIC2111B uses a proprietary hiccup current limit algorithm to avoid inductor saturation. An internal counter increments by two in each cycle over current is detected, and decrements by one each cycle when the current is not over the limit. When the counter reaches 16, the part will shut down and wait for 8 ms before restarting again ([Figure 4-2](#) and [Figure 4-3](#)).

E24 Range Resistance	Current Limit Threshold
88 kΩ	23.3 mV
63 kΩ	18.3 mV

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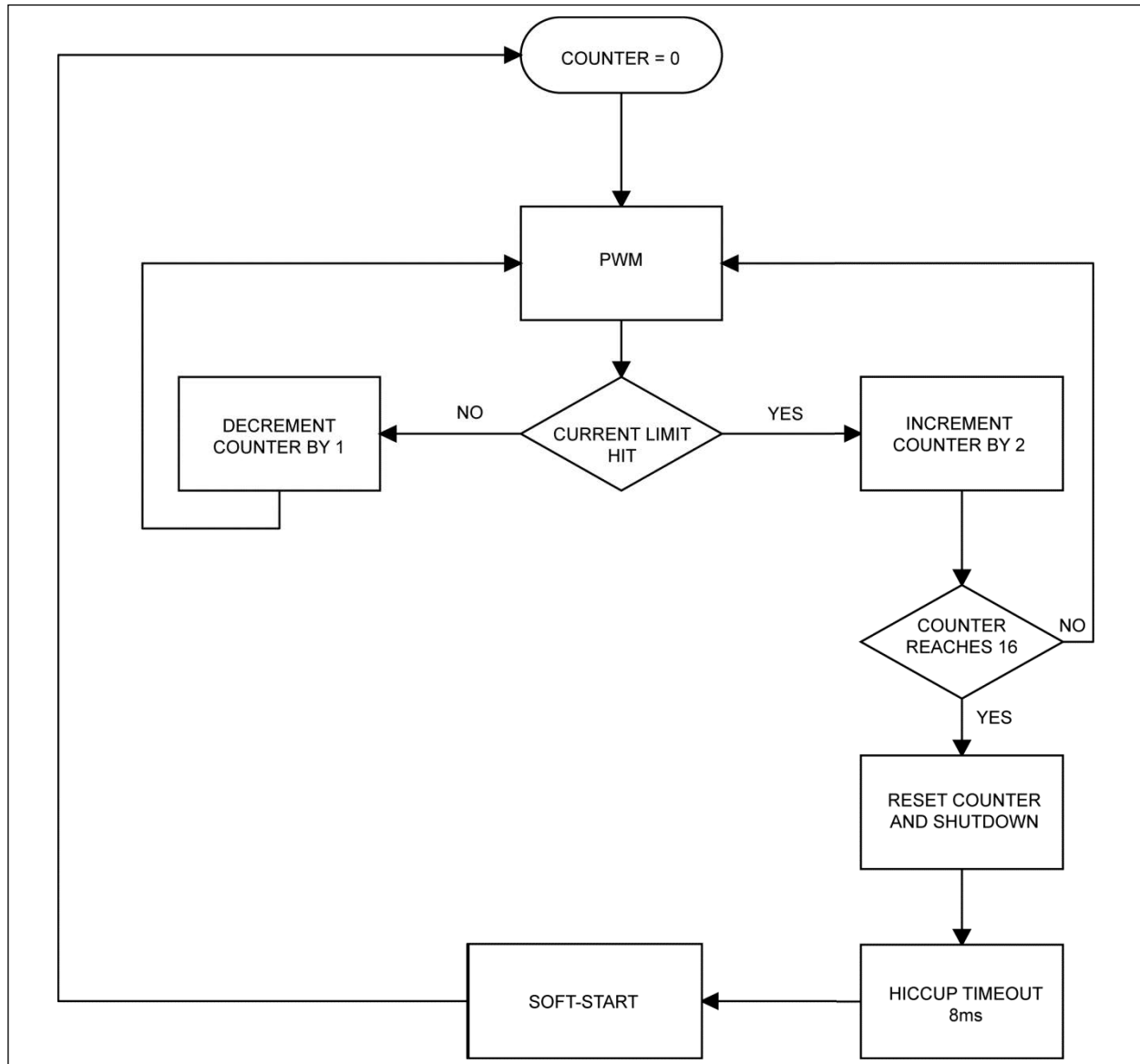


FIGURE 4-3: Hiccup Limit Flow Chart.

4.5 VCC Undervoltage Lockout (UVLO)

The MIC2111B operates from a single 3.3V or 5V supply and has only 2 mA of quiescent current. When bias voltage at V_{CC} is less than the undervoltage lockout (UVLO) level of 2.85V, HS will be high impedance to drive both MOSFETs to tri-state. UVLO has 100 mV hysteresis to avoid an undesirable turn-on. If the same supply voltage is used for the power module and the MIC2111B, it is recommended to use a series RC filter (1 Ω and 1 μ F) for MIC2111B bypassing.

4.6 Enable/Disable (EN) Control

The precision EN pin is used to enable or disable the MIC2111B. The typical threshold is 1.2V. When the voltage at EN rises above the threshold, the controller is enabled and starts normal operation after initialization of the internal oscillator, references, current limit settings, and the soft-start period. The MIC2111B has initialization delay of 250 μ s before the PWM output starts.

When the voltage at EN drops 100 mV or more (hysteresis) below the threshold voltage, then the internal controller circuits in the MIC2111B are turned off. It is possible to use the EN pin for sequencing multiple power supplies along with the power good (PG) pin. Do not float the EN pin. An external RC delay may be added to achieve sequencing.

MIC2111B

4.7 Power Good (PG)

The power good (PG) pin is an open-drain output. External pull-up resistance is required between PG and an external voltage. When the feedback voltage, V_{FB} , rises above the PG threshold, the PG output is pulled high after a delay of 200 μ s (contact Microchip for other PG delays).

4.8 Bi-Directional Fault Communication (FAULTb)

The MIC2111B adopts Microchip's proprietary fault (FAULTb) communication protocol. There are multiple system faults possible in a high current environment. The MIC2111B features internal pull-up of 100 k Ω between the VCC and FAULTb pin.

4.9 Soft-Start/Soft-Stop (SS)

The MIC2111B has digital soft-start/soft-stop (SS) to avoid high inrush current in the input supply lines. Soft-start time can be programmed with an external resistor connected from the SS pin to GND. [Table 4-3](#) illustrates resistor values and soft-start time. Soft-stop time is the same as the programmed soft-start time (contact Microchip for instructions on enabling soft-stop).

TABLE 4-3: SOFT-START PROGRAMMING

E96 Range Resistance	Soft-Start Time
6.19 k Ω	64 μ s
19.1 k Ω	128 μ s
30.9 k Ω	256 μ s
44.2 k Ω	512 μ s
56.2 k Ω	768 μ s
68.1 k Ω	1024 μ s
80.6 k Ω	1536 μ s
93.1 k Ω	2048 μ s
105 k Ω	3072 μ s
118 k Ω	4096 μ s
130 k Ω	6144 μ s
143 k Ω	8192 μ s
154 k Ω	16384 μ s
169 k Ω	24576 μ s
182 k Ω	32768 μ s
Open	2048 μ s

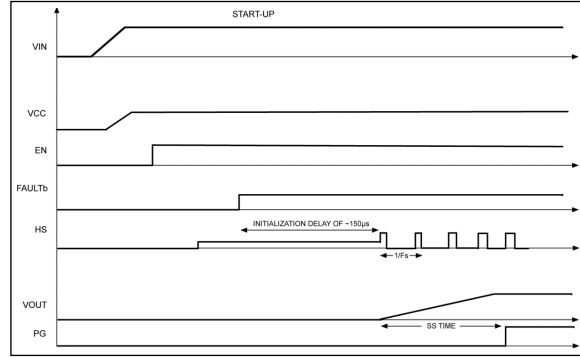


FIGURE 4-4: Typical System Soft-Start.

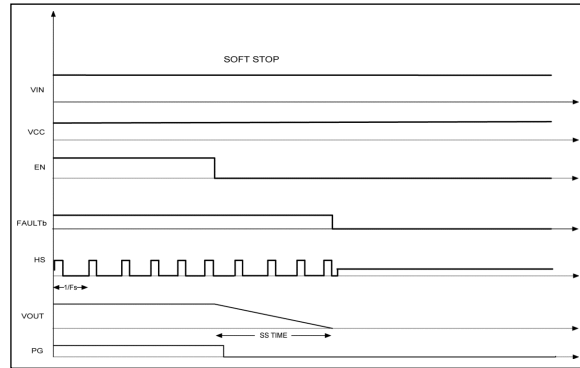


FIGURE 4-5: Typical Soft-Stop.

4.10 Light Load Operation (DCM)

The MIC2111B supports pulse skip mode for good light efficiency. Connecting the MODE or SMOD# pin of the power module to GND is required to enable the light load mode. To avoid discharging the output during light load mode, the power module zero current detector disables the low-side FET once inductor current reaches zero. The MIC2111B generates the next PWM signal based on COMP voltage. This will cause discontinuous conduction mode at the switch node as shown below.

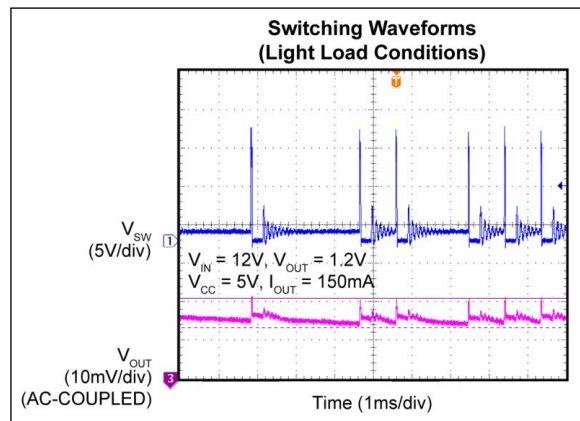


FIGURE 4-6: Light Load Operation (DCM).

4.11 Outside Audio Operation

Some systems require outside audio operation during light load mode. When the system load reduces during light load mode, the system will change from CCM to DCM and, as the load reduces further, the switching frequency reduces as well. If the effective switching frequency reduces below a certain threshold, the MIC2111B will enter outside audio mode, attempting to maintain the effective switching frequency above the audio band. For the outside audio mode to function, the LS output of the MIC2111B must be connected to the MODE pin of the DrMOS. While in this mode, if the MIC2111B detects that the period between HS pulses is longer than 32 μ s, it forces LS a logic-1, which turns on the low-side driver. This results in current flowing from the output capacitor through the inductor and low-side MOSFET. This can cause the output voltage to fall and initiate a PWM cycle with HS going high and LS going low.

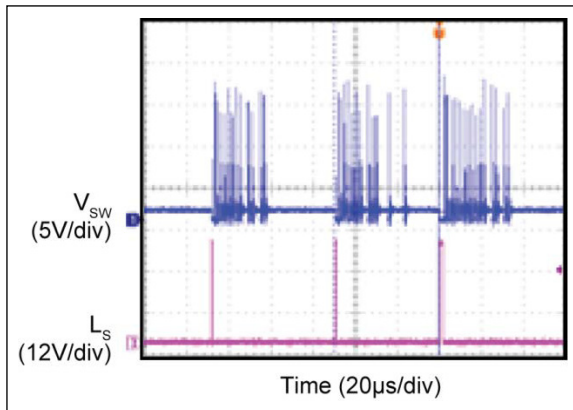


FIGURE 4-7: Outside Audio Waveform.

4.12 Output Overvoltage Protection (OVP)

The MIC2111B has a dedicated pin for overvoltage protection (OVP). The OVP pin senses the output voltage through a voltage divider. If this voltage is higher than the reference voltage, the overvoltage protection engages and FAULTb is pulled low.

This OVP function typically protects against open feedback loop or V_{FB} short-to-GND. This will protect the costly load from being damaged by the DC/DC converter.

The OVP level can be programmed through a resistive divider at the OVP pin as follows. Select R4 same as lower feedback resistor. R1 can be calculated based upon required OVP level as illustrated in Equation 4-2 and Figure 4-8.

EQUATION 4-2:

$$R1 = R4 \times \left(\frac{V_{OUT} - 0.6V}{0.6V} \right)$$

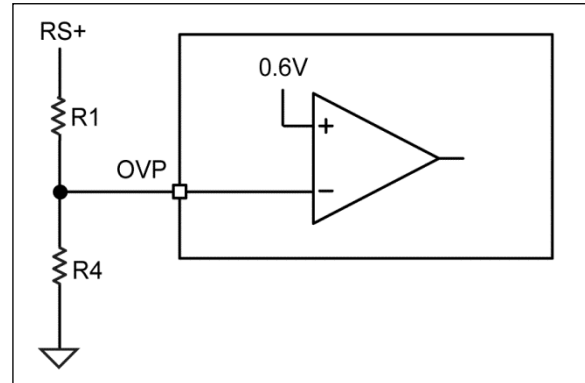


FIGURE 4-8: OVP Programming.

After the OVP fault is triggered, the system will be shut down and latched off. It is required to cycle either VCC or EN for enabling the converter.

4.13 Temperature Sense Input

The MIC2111B has a dedicated input for thermal sense from intelligent power stages. The temperature sense pin (TJ) senses the voltage divided from the thermal sense signal and sends it to the comparator. If this voltage is higher than the reference voltage, the thermal shutdown engages and FAULTb is pulled low. The thermal shutdown threshold can be programmed through a resistive divider from TJ.

EQUATION 4-3:

$$R1 = R4 \times \left(\frac{V_{TSENSE} - 0.6V}{0.6V} \right)$$

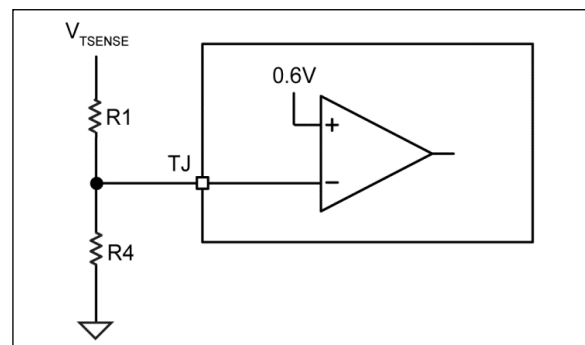


FIGURE 4-9: Thermal Shutdown Programming.

Output will be turned off by pulling FAULTb low after TJ fault is triggered. The fault will be released after hysteresis of 50 mV is achieved.

5.0 APPLICATION INFORMATION

5.1 Programming Output Voltage with RS Amplifier Diagram

The output voltage is set using a resistive voltage divider from the output of differential amplifier to FB (Figure 5-1). For R1, use a 1 kΩ to 10 kΩ resistor. Choose R4 to set the output voltage by using Equation 5-1.

EQUATION 5-1:

$$R4 = R1 \times \left(\frac{V_{FB}}{V_{OUT} - V_{FB}} \right)$$

Where:

$$V_{FB} = 0.6V$$

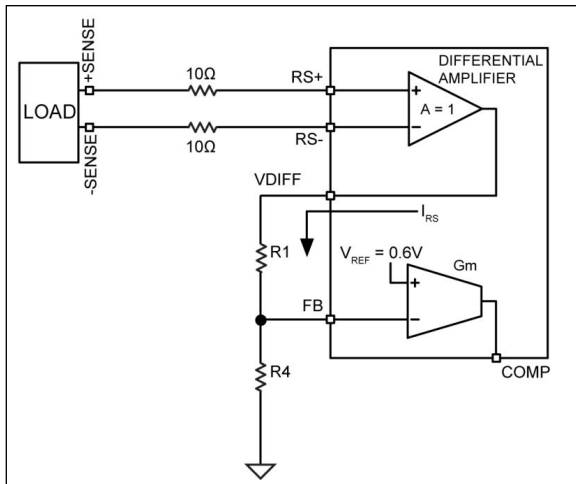


FIGURE 5-1: Programming Output Voltage.

5.2 Current Sensing and Current Limit

MIC2111B has differential current sense input with a dedicated current sense amplifier. It has a current sense amplifier gain of 30V/V and uses lossless inductor current sensing. This offers the advantage of lower power loss and lower cost over using a discrete resistor in series with the inductor.

The inductor sense circuit is shown in Figure 5-2. It extracts the voltage drop across the inductor's DC winding resistance.

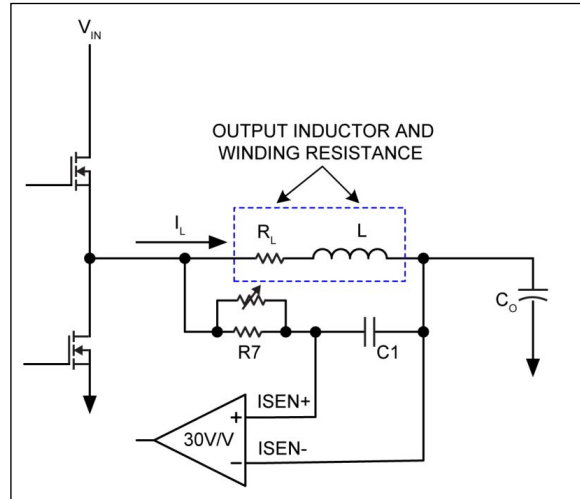


FIGURE 5-2: Current Sensing.

The voltage across capacitor C1 is illustrated in Equation 5-2:

EQUATION 5-2:

$$V_S = I_L \times R_L \times \left[\frac{\frac{sL}{R_L} + 1}{sC1 \times R7 + 1} \right]$$

If the R7 x C1 time constant is equal to the L/RL time constant, then the voltage across capacitor C1 equals RL x IL. Figure 5-3 is a plot of Equation 5-2. It assumes an inductance of 1.5 μH, RL = 0.01Ω (-40 dB), C1 = 0.1 μF and R7 = 1.5 kΩ. The time constants are equal and diverge at the same rate. The overall impedance, H(s), equals RL for all frequencies.

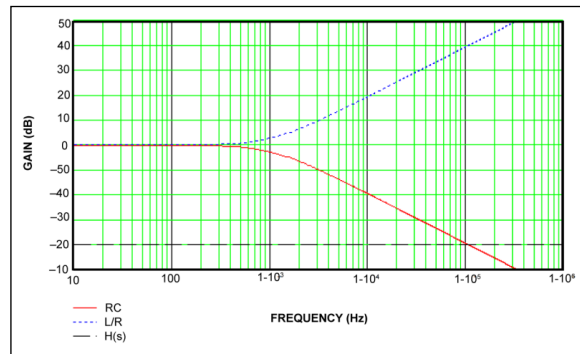


FIGURE 5-3: Current Sense Gain/Phase Plot.

For a system employing the MIC2111B with inductor current sensing, the absolute current limit threshold is:

EQUATION 5-3:

$$I_{LIM} = \frac{V_{THRESH}}{R_{DCR}}$$

Here, R_{DCR} is the inductor DC resistance. For $R_{DCR} = 1\text{ m}\Omega$ and a 23.3 mV current limit voltage threshold, the absolute current limit would be:

EQUATION 5-4:

$$I_{LIM} = \frac{V_{THRESH}}{R_{DCR}} = 0.0233\text{ V} / 1\text{ m}\Omega = 23.3\text{ A}$$

For compensating the inductor's DCR variation with temperature, an NTC is placed in parallel with the resistor (R7) in Figure 5-2.

5.3 Slope Compensation

Slope compensation is required in most conditions for current mode PWM controllers. The MIC2111B applies slope compensation dependent on the system input voltage, output voltage, and inductance by a single resistor. The resistor is connected between V_{IN} and the SLOPE pin.

In Valley Current Mode, 1x slope compensation is implemented by selecting the following resistor value:

- $R_{SLOPE} = K_{SLOPE} \times L / [(A_{ISENAMP} \times R_{SENSE})]$
- $K_{SLOPE} = 1.33 \times 10^{10} \Omega/\text{s}$
- L = Inductor value
- $A_{ISENAMP}$ = Internal current amplifier gain (30 in MIC2111B)
- R_{SENSE} = External current sense gain

For low-frequency applications (less than 500 kHz) and noisy systems, increasing the slope compensation by a factor of 2 is recommended.

Because slope compensation is not needed in Voltage Mode, the SLOPE pin is used to generate the sawtooth ramp. A 1V peak-to-peak ramp at the PWM comparator input is implemented by selecting the following resistor value:

- $R_{SLOPE} = K_{SLOPE} \times T \times (V_{IN} - V_{OUT})$
- $K_{SLOPE} = 1.33 \times 10^{10} \Omega/\text{s}$
- T = Switching period (1/switching frequency)
- V_{IN} = System input voltage
- V_{OUT} = Output voltage

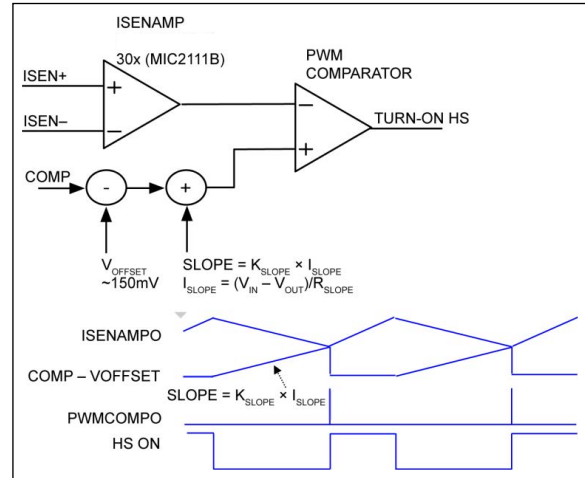


FIGURE 5-4: Valley Current Mode Compensation.

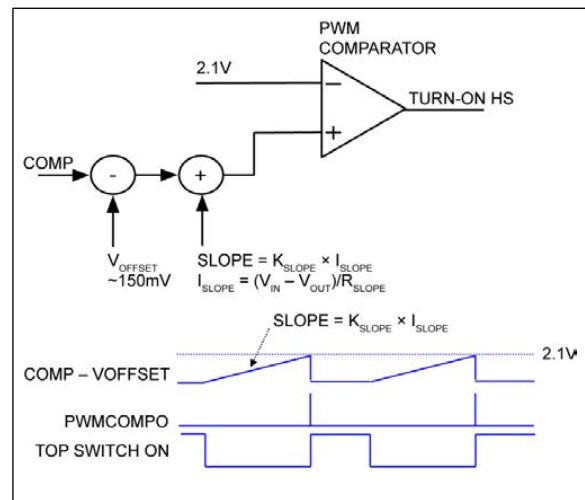


FIGURE 5-5: Voltage Mode Ramp Generation.

5.4 Loop Compensation

5.4.1 CURRENT MODE (TYPE II METHOD)

The MIC2111B uses an internal transconductance error amplifier wherein the output compensates the control loop. The external inductor, output capacitor, slope compensation resistor, and compensation network all determine the loop stability. The inductor and output capacitors are chosen based on performance, size, and cost. The MIC2111B is configured in a valley current mode control scheme when the SEL pin is connected to AGND. In this mode, the MIC2111B regulates the output voltage by forcing the required current through the external inductor. Current mode control eliminates the double pole in the feedback loop, which is caused by the inductor and output capacitor. This results in a smaller phase shift and requires less elaborate error amplifier

compensation than voltage mode control. A simple series R_C and C_C is all that is needed to have a stable, high bandwidth loop in applications where ceramic capacitors are used for output filtering. For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed loop crossover frequency. To stabilize a non-ceramic output capacitor loop, one would need to add another compensation capacitor from COMP to GND as it cancels this ESR to zero. The basic regulator loop is modeled as a power modulator, an output feedback divider and an error amplifier.

The power modulator has DC gain ($A_{MOD(DC)}$), is set by R_L , (output load, equivalent resistance) with a pole and zero pair set by R_L , the output capacitor (C_{OUT}) and its equivalent series resistance (R_{ESR}). Equation 5-5 defines the power modulator (Figure 5-6):

EQUATION 5-5:

$$A_{MOD(DC)} = \frac{1}{A_{CS}} \times \frac{R_L}{1 + \frac{R_L}{R_{SLOPE}}}$$

Where:

$$A_{CS} = A_{ISENAMP} \times R_{SENSE}$$

As current mode control separates the complex LC double pole, a pole is formed by load resistance and output capacitance.

EQUATION 5-6:

$$f_{PO} = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

$$f_{ZO} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

The feedback voltage divider has a gain of $A_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is equal to 0.6V. The transconductance error amplifier has a DC gain, $A_{EA(DC)} = g_{mEA} \times R_O$, where g_{mEA} is the error amplifier transconductance, which is equal to 2 ms, and R_O is the output resistance of the error amplifier, which is 50 MΩ. A dominant pole (f_{pdEA}) is set by the compensation capacitor (C_C), the amplifier output resistance (R_O), and the compensation resistor (R_C); a zero (f_{zEA}) is set by the compensation resistor (R_C), and the compensation capacitor (C_C). There is an optional pole (f_{pEA}), set by C_{Cf} and R_C , to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C):

EQUATION 5-7:

$$f_{pdEA} = \frac{1}{2\pi \times (R_O + R_C) \times C_C}$$

$$f_{zEA} = \frac{1}{2\pi \times R_C \times C_C}$$

$$f_{pEA} = \frac{1}{2\pi \times R_C \times C_{Cf}}$$

The crossover frequency, f_O , should be much higher than the power modulator pole f_{PO} . Also, f_C should be less than or equal to 1/5 the switching frequency:

EQUATION 5-8:

$$f_{PO} \ll f_O \leq \frac{f_{SW}}{5}$$

Choosing a lower crossover frequency reduces the effects of noise pickup into the feedback loop, such as jittery duty cycle.

At the crossover frequency, the total loop gain must equal 1, and is expressed as:

EQUATION 5-9:

$$A_{MOD(f_O)} \times A_{EA(f_O)} \times A_{FB} = 1$$

Mid-band gain is decided by the g_m and R_C :

EQUATION 5-10:

$$A_{EA(f_O)} = g_m \times R_C$$

Where:

$$g_m = 2 \text{ ms}$$

EQUATION 5-11:

$$A_{MOD(f_O)} = A_{MOD(DC)} \times \frac{f_{PO}}{f_O}$$

Then R_C and C_C can be calculated as:

EQUATION 5-12:

$$R_C = \frac{A_{FB}}{g_m \times A_{MOD(f_O)}}$$

$$C_C = \frac{1}{2\pi \times R_C \times f_{PO}}$$

For high current applications, it is recommended to place C_{CF} to cancel the effect of ESR zero:

EQUATION 5-13:

$$C_{CF} = \frac{1}{2\pi \times R_C \times f_{PO}}$$

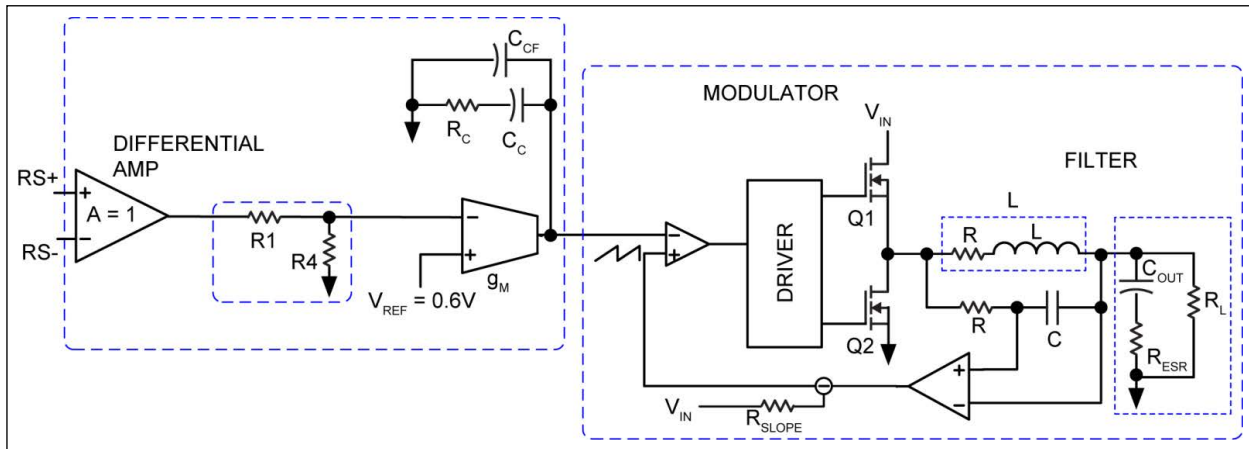


FIGURE 5-6: Valley Current Mode Loop Compensation.

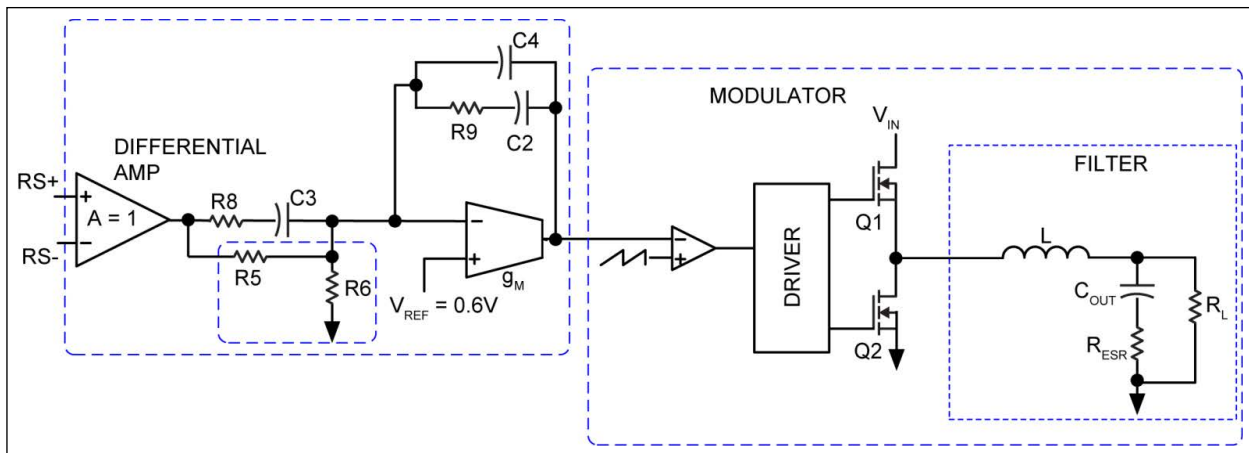


FIGURE 5-7: Voltage Mode Loop Compensation.

Equation 5-8 assumes crossover frequency to be much less than half of the switching frequency. There is a sampling effect at the half switching frequency that introduces the double pole. For high crossover applications, it is recommended to run a bode plot to optimize the transient response.

5.4.2 VOLTAGE MODE (TYPE III METHOD)

The MIC2111B provides an internal transconductance amplifier with the inverting input (FB) and the output (COMP) available for external frequency compensation. The flexibility of external compensation allows for a wide selection of output filtering components, especially the output capacitor. The use of high-ESR aluminum electrolytic capacitors is recommended for cost sensitive applications. Use low-ESR POSCAPs or ceramic capacitors at the output for size sensitive applications. The high switching

frequency of the MIC2111B allows the use of ceramic capacitors at the output. Choose all passive power components to meet the output ripple, component size, and component cost requirements. Choose the compensation components for the error amplifier to achieve the desired closed-loop bandwidth and phase margin.

To choose the appropriate compensation network type, the power supply poles and zeroes, the zero crossover frequency, and the type of the output capacitor must be determined first.

In a buck converter, the LC filter in the output stage introduces a pair of complex poles at the following frequency:

EQUATION 5-14:

$$f_{PO} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

The output capacitor introduces a zero at:

EQUATION 5-15:

$$f_{ZO} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

Where:

R_{ESR} = The equivalent series resistance of the output capacitor.

The loop-gain crossover frequency (f_O), where the loop gain equals 1 (0 dB) should be set below 1/10th of the switching frequency as in:

EQUATION 5-16:

$$f_O \leq \frac{f_{SW}}{10}$$

Choosing a lower crossover frequency reduces the effects of noise pick-up into the feedback loop, such as jitter duty cycle.

In order to maintain a stable system, two stability criteria must be met:

1. The phase shift at the crossover frequency (f_O) must be less than 180° . In other words, the phase margin of the loop must be greater than zero.
2. The gain at the frequency where the phase shift is -180° (gain margin) must be less than 1.

Maintain a phase margin of around 60° to achieve a robust loop stability and well-behaved transient response.

When using an electrolytic or large-ESR POSCAP output capacitor the capacitor ESR zero (f_{ZO}) typically occurs between the LC poles and the crossover frequency f_O ($f_{PO} < f_{ZO} < f_O$). Choose Type II Proportional and Integral (PI) compensation network as previously specified.

When using a ceramic or low-ESR tantalum output capacitor the capacitor ESR zero typically occurs above the desired crossover frequency f_O ($f_{PO} < f_{ZO} < f_O$). Choose Type III proportional, integral, and derivative (PID) compensation network.

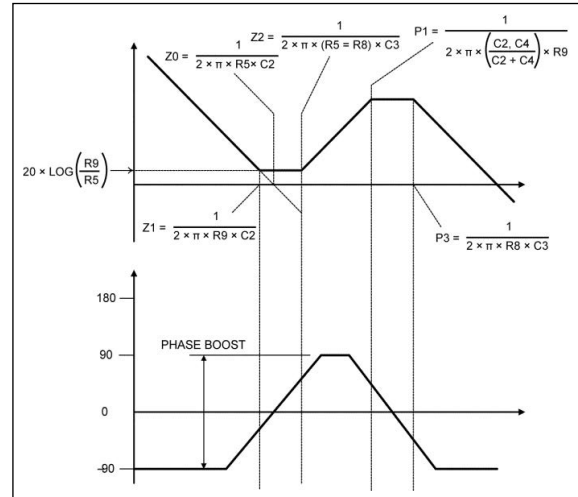


FIGURE 5-8: Type III Compensation Pole and Zero Locations.

Referring to [Figure 5-7](#), ensure that $R9 > 1/g_m$ and the parallel resistance of $R8$, $R5$, and $R6$ is greater than $1/g_m$. Otherwise, a 180° phase shift is introduced to the response making the loop unstable. Use the following compensation procedures:

1. With $R9 \geq 10 \text{ k}\Omega$, place the first zero (f_{Z1}) at $0.8 \times f_{PO}$:

EQUATION 5-17:

$$f_{Z1} = \frac{1}{2\pi \times R9 \times C2} = 0.8 \times f_{PO}$$

So,

EQUATION 5-18:

$$C2 = \frac{1}{2\pi \times R9 \times 0.8 \times f_{PO}}$$

2. The gain of the modulator (A_{MOD}), comprises the pulse width modulator, LC filter, feedback divider, and associated circuitry at crossover frequency is:

EQUATION 5-19:

$$A_{MOD} = \frac{V_{IN}}{V_{RAMP}} \times \frac{1}{(2\pi \times f_O)^2 \times L_{OUT} \times C_{OUT}}$$

The gain of the error amplifier (A_{EA}) in mid-band frequencies is:

EQUATION 5-20:

$$A_{EA} = 2\pi \times f_O \times C3 \times R9$$

The total loop gain as the product of the modulator gain and the error amplifier gain at f_O is 1:

EQUATION 5-21:

$$A_{MOD} \times A_{EA} = 1$$

So,

EQUATION 5-22:

$$\frac{V_{IN}}{V_{RAMP}} \times \frac{1}{(2\pi \times f_O)^2 \times C_{OUT} \times L} \times 2\pi \times f_O \times C3 \times R9 = 1$$

Solving for C3:

EQUATION 5-23:

$$C3 = \frac{V_{RAMP} \times (2\pi \times f_O \times L \times C_{OUT})}{V_{IN} \times R9}$$

- Use the second pole (f_{P2}) to cancel f_{ZO} when $f_{PO} < f_O < f_{ZO} < f_{SW}/2$. The frequency response of the loop gain does not flatten out soon after the 0 dB crossover, and maintains -20 dB/decade slope up to 1/2 of the switching frequency. This is likely to occur if the output capacitor is a low-ESR tantalum. Set $f_{P2} = f_{ZO}$. When using a ceramic capacitor the capacitor ESR zero f_{ZO} is likely to be located even above one half of the switching frequency, $f_{PO} < f_O < f_{SW}/2 < f_{ZO}$. In this case, place the frequency of the second pole (f_{P2}) high enough in order not to erode significantly the phase margin at the crossover frequency. For example, set f_{P2} at $5 \times f_O$ so that the contribution to phase loss at the crossover frequency f_O is only about 11°:

EQUATION 5-24:

$$f_{P2} = 5 \times f_O$$

Once f_{P2} is known, calculate R8:

EQUATION 5-25:

$$R8 = \frac{1}{2\pi \times f_{P2} \times C3}$$

- Place the second zero (f_{Z2}) at $0.2 \times f_O$ or at f_{PO} , whichever is lower, and calculate R5 using the following equation:

EQUATION 5-26:

$$R5 = \frac{1}{2\pi \times f_{Z2} \times C3} - R8$$

- Place the third pole (f_{P3}) at 1/2 the switching frequency and calculate C_{CF} :

EQUATION 5-27:

$$C4 = \frac{C2}{(2\pi \times 0.5 \times f_{SW} \times R9 \times C2) - 1}$$

- Calculate R6 as:

EQUATION 5-28:

$$R6 = \frac{V_{FB}}{V_{OUT} - V_{FB}} - R5$$

5.5 Design and Layout Checklist

- Ceramic capacitor placed between the VIN and PGND pins, close to power module input.
- Output ceramic capacitors should be placed next to inductor output node for high-frequency decoupling.
- The signal and power ground planes must be separated to prevent high current and fast switching signals from interfering with the low level, noise sensitive analog signals. These planes should be connected at only one point.
- The following signals and their components should be decoupled or referenced to the power ground plane:
 - VIN, VCC, PGND
- These analog signals should be referenced or decoupled to the analog ground plane:
 - VCC, SS, PG, COMP, FB, VOUT, and AGND
- Place the current sense lines in differential way. The trace coming from the switch node to this resistor has high dv/dt and should be routed away from other noise sensitive components and traces.
- The remote sense traces must be routed close together or on adjacent layers to minimize noise pickup. The traces should be routed away from the switch node, inductors, and other high dv/dt or di/dt sources.

6.0 TYPICAL APPLICATION SCHEMATIC

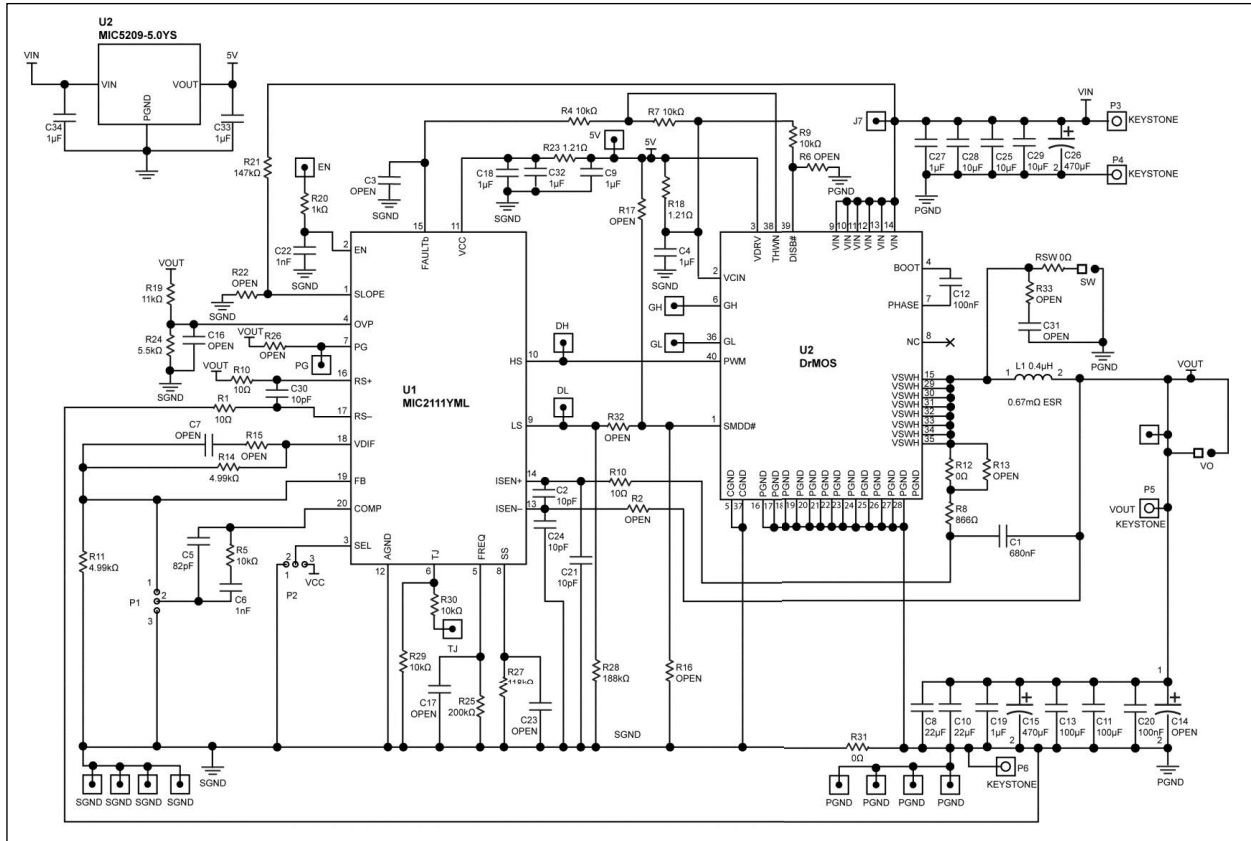


TABLE 6-1: BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty.
C1	C1608X7R1C684K080AC	TDK	0.68 μ F Ceramic Capacitor, X7R, 0603 Size, 16V	1
C2, C21, C24, C30	C1608C0G1H100D	TDK	10 pF Ceramic Capacitor, COG, 0603 Size, 50V	4
C3, C7, C16, C17, C23, C31, R2, R6, R13, R15, R16, R17, R22, R26	OPEN	—	—	—
C4, C9, C18, C19, C27, C32, C33, C34	C1608X5R1E105K	TDK	1 μ F Ceramic Capacitor, X5R, 0603 Size, 25V	8
C5	C1608C0G1H820J	TDK	82 pF Ceramic Capacitor, COG, 0603 Size, 50V	1
C6, C22	C1608C0G1H102J	TDK	1 nF Ceramic Capacitor, COG, 0603 Size, 50V	2
C8, C10	C3225X5R0J226M/1.60	TDK	22 μ F Ceramic Capacitor, X5R, 1210 Size, 6.3V	2
C11, C13	C3225X5R0J107M	TDK	100 μ F Ceramic Capacitor, X5R, 1210 Size, 6.3V	2
C12, C20	C1608X7R1E104K	TDK	100 nF Ceramic Capacitor, X7R, 0603 Size, 25V	2
C15	6SVP470MX	Panasonic	470 μ F OS-CON Capacitor, 6.3V	1

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TABLE 6-1: BILL OF MATERIALS (CONTINUED)

Item	Part Number	Manufacturer	Description	Qty.
C25, C28, C29	C3225X5R1E106M	TDK	10 μ F Ceramic Capacitor, X5R, 1210 Size, 25V	3
C26	EEEF1E471AP	Panasonic	470 μ F Aluminum Capacitor, 25V	1
L1	744325040	Würth Electric	0.4 μ H Inductor, 37A Saturation Current	1
R1, R2, R3, R10	CRCW060310R0FKEA	Vishay Dale	10 Ω Resistor, 0603 Size, 1%	4
R4, R5, R7, R9, R29, R30	CRCW060310K0FKEA	Vishay Dale	10 k Ω Resistor, 0603 Size, 1%	6
R8	CRCW0603866RFKEA	Vishay Dale	866 Ω Resistor, 0603 Size, 1%	1
R11, R14	CRCW06034K99FKEA	Vishay Dale	4.99 k Ω Resistor, 0603 Size, 1%	2
R12, R31, RSW	CRCW06030000Z0EA	Vishay Dale	0 Ω Resistor, 0603 Size, 1%	3
R18, R23	CRCW06031R21FKEA	Vishay Dale	1.21 Ω Resistor, 0603 Size, 1%	2
R19	CRCW060311K0FKEA	Vishay Dale	11 k Ω Resistor, 0603 Size, 1%	1
R20	CRCW06031K00FKEA	Vishay Dale	1 k Ω Resistor, 0603 Size, 1%	1
R21	CRCW0603147KFKEA	Vishay Dale	147 k Ω Resistor, 0603 Size, 1%	1
R24	CRCW06035K49FKEA	Vishay Dale	5.5 k Ω Resistor, 0603 Size, 1%	1
R25	CRCW0603200KFKEA	Vishay Dale	200 k Ω Resistor, 0603 Size, 1%	1
R27	CRCW0603118KFKEA	Vishay Dale	118 k Ω Resistor, 0603 Size, 1%	1
R28	CRCW0603188KFKEA	Vishay Dale	188 k Ω Resistor, 0603 Size, 1%	1
U1	MIC2111B	Microchip	High-Performance, Multi-Mode, Step-Down Controller	1
U2	SiC769ACD	Vishay Dale	35A, DrMOS Module	1
U3	MIC5209-5.0YS	Microchip	500 mA, Low-Noise LDO Regulator	1

7.0 PCB LAYOUT RECOMMENDATIONS

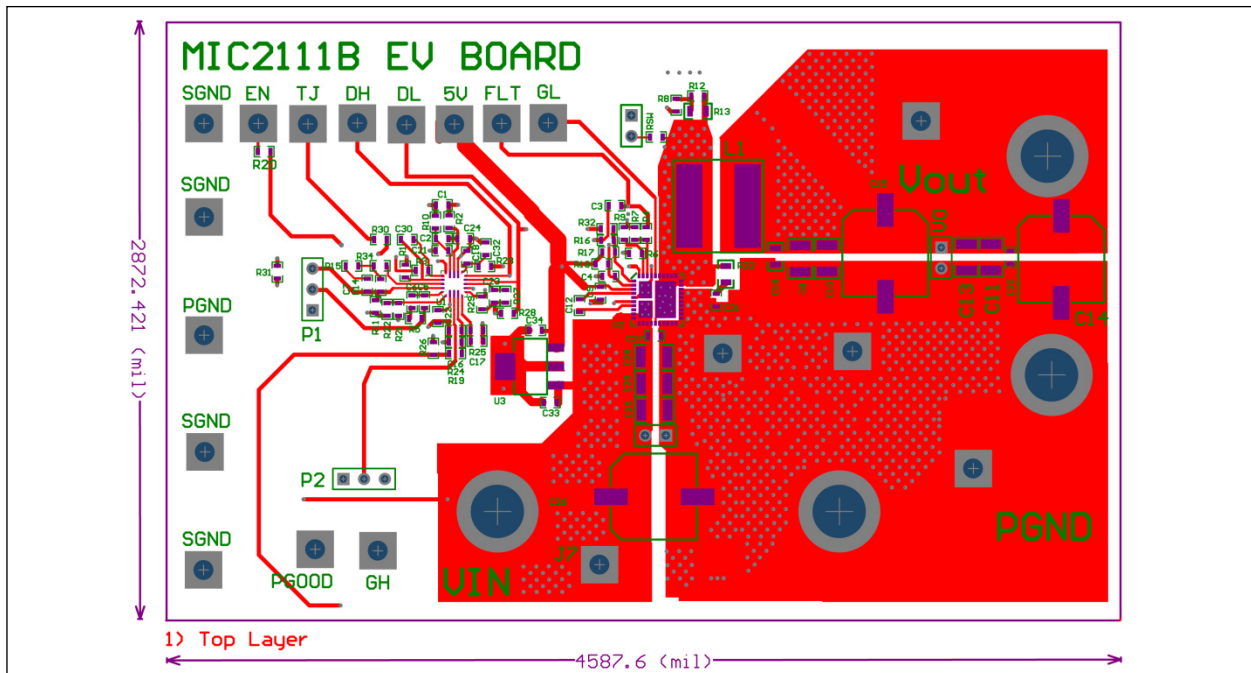


FIGURE 7-1: Top Layer.

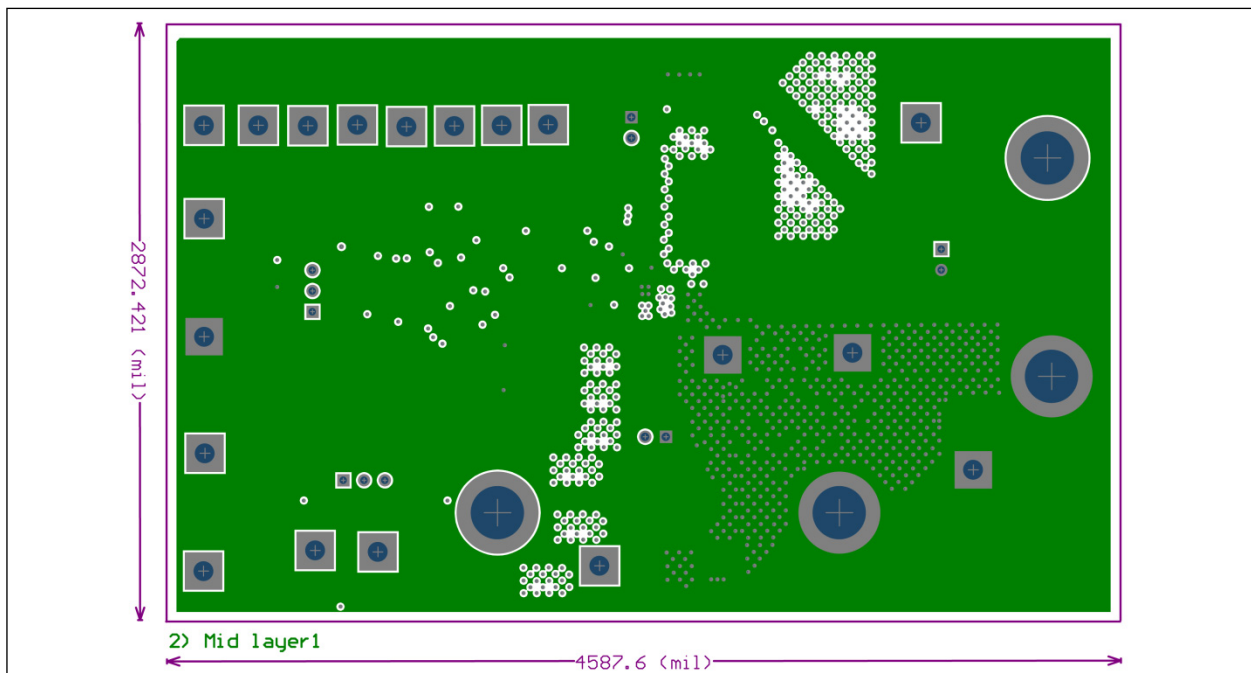


FIGURE 7-2: Mid Layer 1.

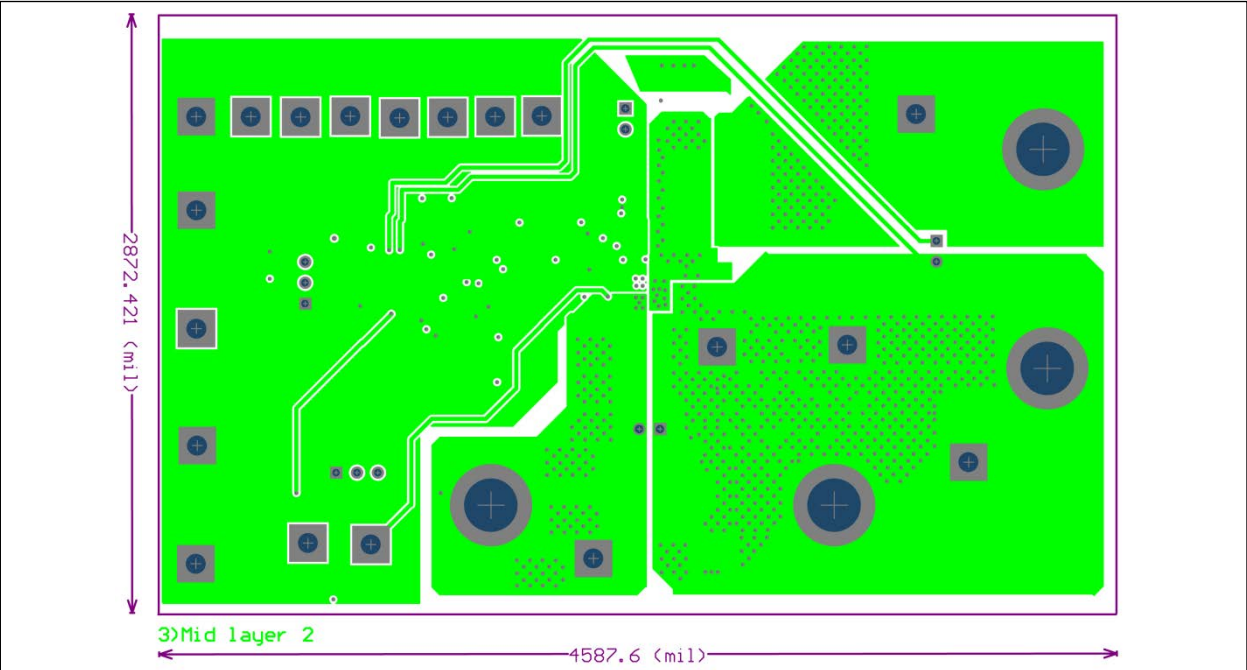


FIGURE 7-3: Mid Layer 2.

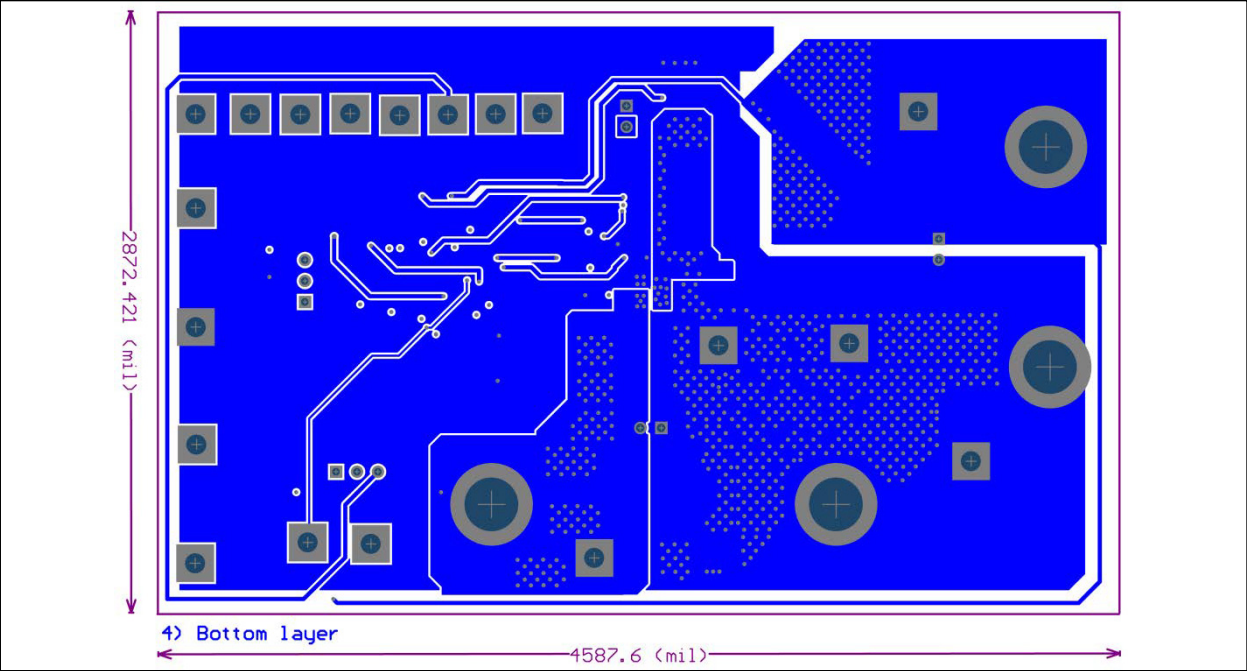
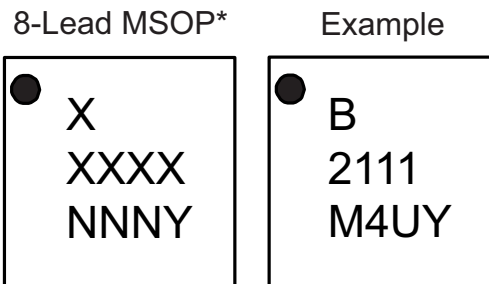


FIGURE 7-4: Bottom Layer.

8.0 PACKAGING INFORMATION

8.1 Package Marking Information



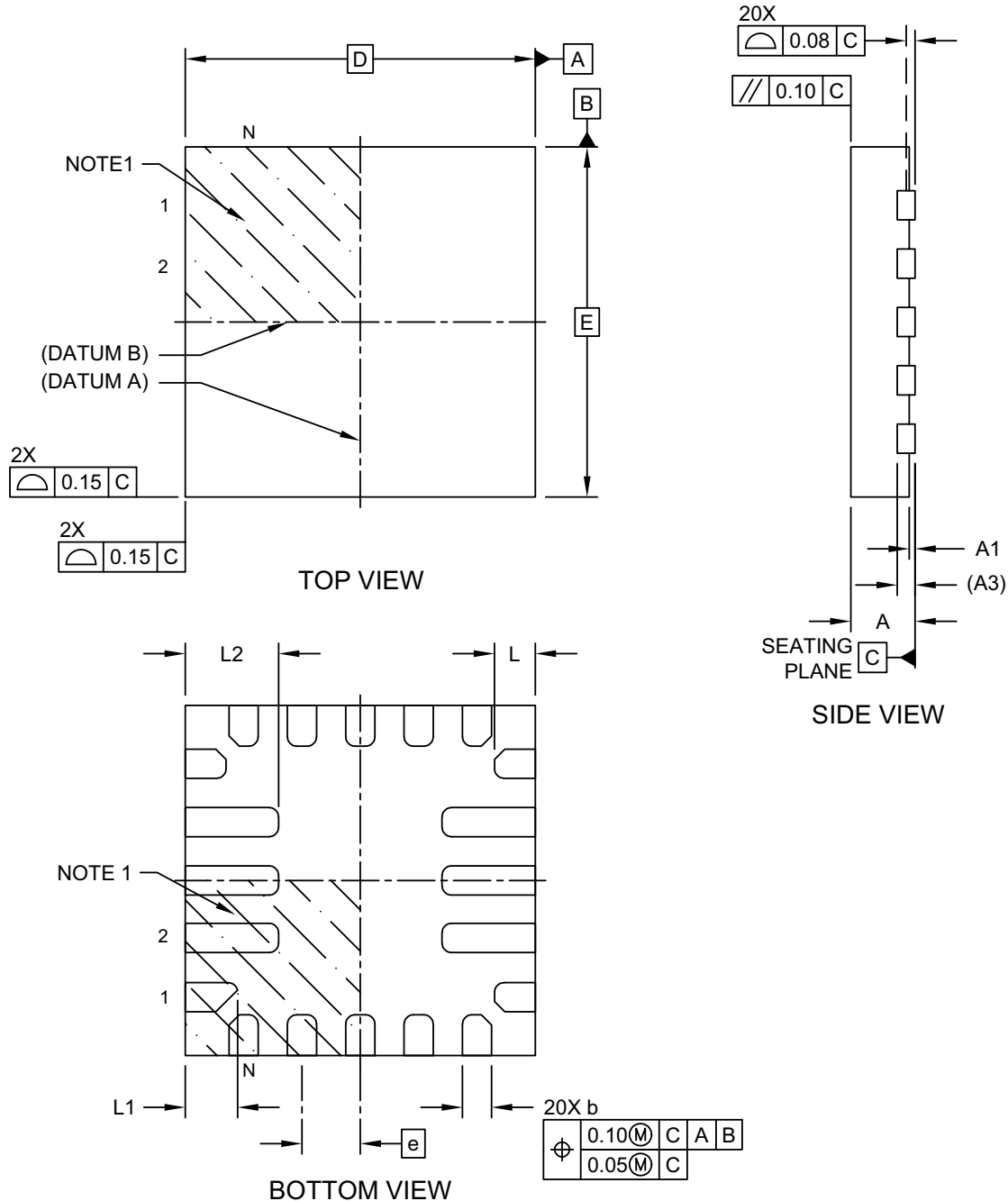
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. Underbar (_) and/or Overbar (¯) symbol may not be to scale.		

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
 6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
 2 Characters = NN; 1 Character = N

MIC2111B

20-Lead Very, Very Thin Quad Flatpack, No Leads (QAA) - 3x3x0.6 mm Body [WQFN] Micrel Legacy Package CTQFN-20L

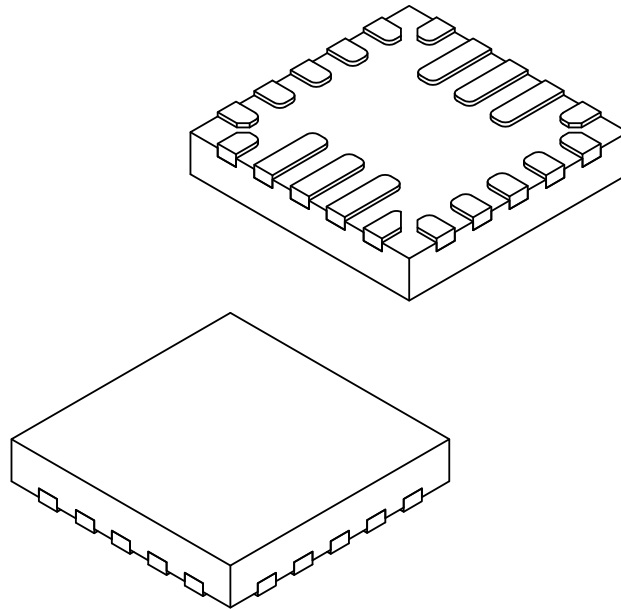
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-01013 Rev A Sheet 1 of 2

20-Lead Very, Very Thin Quad Flatpack, No Leads (QAA) - 3x3x0.6 mm Body [WQFN] Micrel Legacy Package CTQFN-20L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	20		
Pitch	e	0.50 BSC		
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.152 REF		
Overall Length	D	3.00 BSC		
Overall Width	E	3.00 BSC		
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal Length	L1	0.40	0.45	0.50
Terminal Length	L2	0.75	0.80	0.85

Notes:

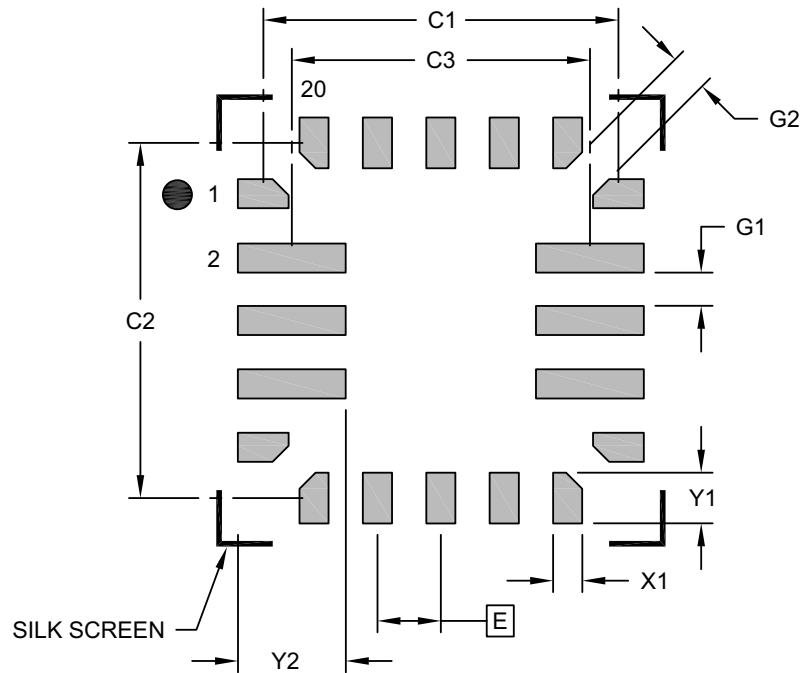
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-01013 Rev A Sheet 2 of 2

MIC2111B

20-Lead Very, Very Thin Quad Flatpack, No Leads (QAA) - 3x3x0.6 mm Body [WQFN] [Micrel Legacy Package CTQFN-20L]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		2.80	
Contact Pad Spacing	C2		2.80	
Contact Pad Spacing	C3		2.35	
Contact Pad Width (X20)	X1			0.23
Contact Pad Length (X14)	Y1			0.40
Contact Pad Length (X6)	Y2			0.85
Contact Pad To Contact Pad (X16)	G1	0.26		
Contact Pad To Contact Pad (X4)	G2	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-03013 Rev A

APPENDIX A: REVISION HISTORY

Revision A (May 2026)

- Converted Micrel document MIC2111B to Microchip data sheet DS20007146A.
- Minor text changes throughout.
- Added a list of obsolete devices.

MIC2111B

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>Part Number</u>	<u>X</u>	<u>XX</u>	<u>-XX</u>	Examples:
Device	Temp. Range	Package	Media Type	
Device:	MIC2111B:	High Performance, Multi-Mode, Step-Down Controller		a) MIC2111BYMT-TR: MIC2111B, -40°C to +125°C Temp. Range, 20-Lead WQFN, 1,000/Reel Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Temperature Range:	Y	=	-40°C to +125°C	
Package:	MT	=	20-Lead 3 mm x 3 mm WQFN	
Media Type:	TR	=	1,000/Reel	
Obsolete Devices: MIC2111BYMT-T5				

MIC2111B

NOTES:

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