OS-68338
ACMOS/TTL Hybrid Clock Oscillator
Hi-Rel Standard

General

	Rev	Cage Code
Vectron® Oscillators	U	00136

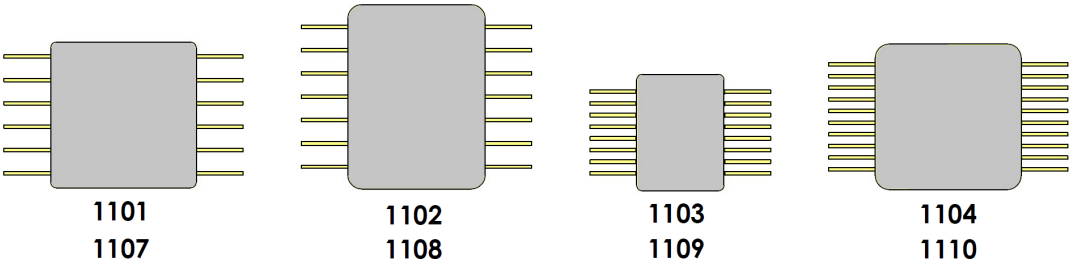
This specification defines the design, assembly and functional evaluation of high reliability, Space qualified, hybrid clock oscillators produced by Microchip. Devices delivered to this specification represent the standardized Parts, Materials and Processes (PMP) Program developed, implemented, and certified for advanced applications and extended environments.

For more information see Space Oscillators.

For technical support regarding this Hi-Rel Standard, please contact VOP-Support@microchip.com.

Applications Overview

The designs represented by these products were primarily developed for the MIL-Aerospace community. The lesser Design Pedigrees and Screening Options imbedded within OS-68338 bridge the gap between Space and COTS hardware by providing custom hardware with measures of mechanical, assembly and reliability assurance needed for Military or Ruggedized COTS environments.

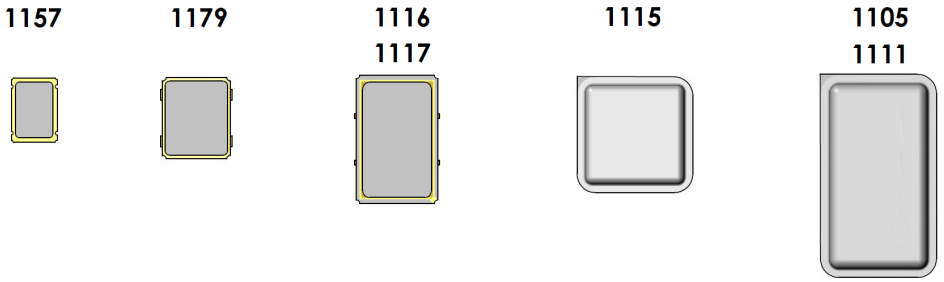


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1. Applicable Documents

1.1. Specifications and Standards

The following specifications and standards form a part of this document to the extent specified herein. The issue currently in effect on the date of quotation will be the product baseline, unless otherwise specified. In the event of conflict between the text of any references cited herein, the text of this document shall take precedence.

Table 1-1. Military

Document	Title
MIL-PRF-55310	Oscillators, Crystal Controlled, General Specification For
MIL-PRF-38534	Hybrid Microcircuits, General Specification For

Table 1-2. Standards

Document	Title
MIL-STD-202	Test Method Standard, Electronic and Electrical Component Parts
MIL-STD-883	Test Methods and Procedures for Microelectronics

Table 1-3. Other

Document	Title
DOC007131	Test Specification, OS-68338 Hybrids, Hi-Rel Standard
QSP-90100	Quality Systems Manual, Microchip
DOC011627	Identification Common Documents, Materials and Processes, Hi-Rel XO
DOC203982	DPA Specification
QSP-91502	Procedure for Electrostatic Discharge Precautions
DOC208191	Enhanced Element Evaluation for Space Level Hybrid Oscillators
DOC220429	Packaging Standards, Hi-Rel Series

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2. General Requirements

2.1. Classification

All devices delivered to this specification are of hybrid technology conforming to Type 1, Class 2 of MIL-PRF-55310. Primarily developed as a Class S equivalent specification, options are imbedded within it to also produce Class B, Engineering Model and Ruggedized COTS devices. Devices carry a Class 2 ESDS classification per MIL-PRF-38534.

2.2. Item Identification

External packaging choices are of metal flatpacks, DIPs and ceramic with either TTL or ACMOS logic output. Unique Model Number Series' are utilized to identify device package configurations and output logic as listed in Table 6-1.

2.3. Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings

Parameter	Value
Supply Voltage Range (V_{CC})	−0.5 Vdc to +7.0 Vdc
Storage Temperature Range (T_{STG})	−65 °C to +125 °C
Junction Temperature (T_J)	+175 °C
Lead Temperature (soldering, 10 seconds)	+300 °C
Output Source/Sink Current	±70 mA

2.4. Design, Parts, Materials and Processes, Assembly, Inspection and Test

2.4.1. Design

The ruggedized designs implemented for these devices are proven in military and space applications under extreme environments. All designs (except 5x7 mm) utilize a 4-point crystal mount. All designs (except 5x7 mm and 7x9 mm) use Established Reliability (MIL-ER) componentry. The 5x7 mm models utilize a 3-point crystal mount. When specified, radiation tolerant active devices up to 100 krad (Si) (RHA level R) can be included without altering the device's internal topography.

2.4.1.1. Design and Configuration Stability

Barring changes to improve performance by reselecting passive chip component values to offset component tolerances, there will not be fundamental changes to the design or assembly or parts, materials, and processes after first product delivery of that item without notification.

2.4.1.2. Environmental Integrity

Designs have passed the environmental qualification levels of MIL-PRF-55310. These designs have also passed extended dynamic levels of at least:

a. Sine Vibration: MIL-STD-202, Method 204, Condition G (30g pk.)

b. Random Vibration: MIL-STD-202, Method 214, Condition II-J (43.92g rms, three- minute duration in each of three mutually perpendicular directions)

c. Mechanical Shock: MIL-STD-202, Method 213, Condition F (1500g, 0.5ms)

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2.4.2. Prohibited Parts, Materials and Processes

The items listed are prohibited for use in high reliability devices produced to this specification.

a. Gold metallization of package elements without a barrier metal.

b. Zinc chromate as a finish.

c. Cadmium, zinc, or pure tin external or internal to the device.

d. Plastic encapsulated semiconductor devices.

e. Ultrasonically cleaned electronic parts.

f. Heterojunction Bipolar Transistor (HBT) technology.

g. 'Getter' materials

2.4.3. Assembly

Manufacturing utilizes standardized procedures, processes, and verification methods to produce MIL-PRF-55310 Class S / MIL-PRF-38534 Class K equivalent devices. MIL-PRF-38534 Group B Option 1 in-line inspection is included on design pedigrees E, R and V to further verify lot pedigree. Devices are handled in accordance with Microchip document QSP-91502 (Procedure for Electrostatic Discharge Precautions). Element replacement will be as specified in MIL-PRF-38534, Rev L.

2.4.4. Inspection

The inspection requirements of MIL-PRF-55310 apply to all devices delivered to this document. Inspection conditions and standards are documented in accordance with the Quality Assurance, ISO-9001 and AS9100 derived, System of QSP-90100.

2.4.5. Test

The Screening test matrix in Table 6-6 is tailored for selectable-combination testing to eliminate costs associated with the development/maintenance of device-specific documentation packages while maintaining performance integrity.

2.4.6. Marking

Device marking shall be in accordance with the requirements of MIL-PRF-55310. In addition, when devices are identified with laser marking, the Resistance to Solvents test specified in MIL-PRF-55310 Group C, MIL-PRF-55310 Qualification or MIL-PRF-38534 Group B Inspection will not be performed.

2.4.7. Ruggedized COTS Design Implementation

Design Pedigree "D" devices (see 4.2. Optional Design, Test, and Data Parameters) use the same robust designs found in the other device pedigrees. They do not include the provisions of traceability or the Class-qualified componentry noted in 2.4.3. Assembly and 3.1. Components.

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3. Detail Requirements

3.1. Components

3.1.1. Crystals

Cultured quartz crystal resonators are used to provide the selected frequency for the devices. The optional use of Premium Q swept quartz can, because of its processing to remove impurities, be specified to minimize frequency drift when operating in radiation environments. In accordance with MIL-PRF-55310, the manufacturer has a documented crystal element evaluation program.

3.1.2. Passive Components

3.1.2.1. Design Pedigree E

Where available, resistors shall be Established Reliability, Failure Rate R (as a minimum) and capacitors shall be Failure Rate S. Where resistors and capacitors are not available as ER parts, and for all other passive components, the parts shall be from homogeneous manufacturing lots that have successfully completed the Enhanced Element Evaluation of DOC208191 which meets the requirements of MIL-PRF-38534 Revision L for Class K.

3.1.2.2. Design Pedigree R, V, and X

Where available, resistors shall be Established Reliability, Failure Rate R (as a minimum) and capacitors shall be Failure Rate S. Where resistors and capacitors are not available as ER parts, and for all other passive components, the parts shall be from homogeneous manufacturing lots that have successfully completed the Class K Element Evaluation of MIL-PRF-38534 Revision K for Class K.

3.1.2.3. Design Pedigrees B and C

All passive elements shall comply with the Element Evaluation requirements of MIL-PRF-55310 Class B as a minimum.

3.1.2.4. Design Pedigree D

Passive elements will be COTS level or higher.

3.1.2.5. Inductors

When used, inductors will be open construction and may use up to 48-gauge wire.

3.1.3. Microcircuits

3.1.3.1. Design Pedigree E

Microcircuits shall be from homogeneous wafer lots that meet the Enhanced Element Evaluation requirements in DOC208191 and meet the requirements of MIL-PRF-38534 Revision L for Class K.

3.1.3.2. Design Pedigree R, V and X

Microcircuits shall be from homogeneous wafer lots that have successfully completed the MIL-PRF-38534, Revision K Lot Acceptance Tests for Class K.

3.1.3.3. Design Pedigrees B and C

Microcircuits are procured from wafer lots that have successfully completed the MIL-PRF-55310 Lot Acceptance Tests for Class B as a minimum.

3.1.3.4. Design Pedigree D

Microcircuits can be COTS level or higher.

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3.1.4. Radiation

Microcircuits for Design Pedigrees E, R and V are certified to 100krad (Si) total ionizing dose (TID), RHA level R (2X minimum margin). NSC, as the original 54ACT designer, rates the SEU LET up to 40 MeV-cm^2/mg and SEL LET up to 120 MeV-cm^2/mg for the FACT™ family (AN-932). Microchip conducted additional SEE testing in 2008 to verify this performance since our lot wafer testing does not include these parameters and determinations. In addition, Microchip has conducted neutron displacement damage testing to confirm a tolerance of 6E11 n/cm^2, 1MeV equivalent. Prompt dose (dose rate) testing of the 54ACT device shows that the part is immune to latch-up/burnout up to at least 1.39E10 rad(Si)/s and +125 °C. The parts exhibited no transients at a dose rate of 1E8 rad(Si)/s. At dose rates up to 1.39E10, all parts recovered to pre-shot function and supply current within three to four microseconds.

3.1.5. Packages

Packages are procured that meet the construction, lead materials and finishes as specified in MIL-PRF-55310. All leads are Kovar with gold plating over a nickel underplate. Package lots are evaluated in accordance with the requirements of MIL-PRF-38534. Microchip will not perform Salt Spray testing as part of MIL-PRF-55310 Group C/Qualification. In accordance with MIL-PRF-55310, package evaluation results for salt atmosphere will be substituted for Salt Spray testing during MIL-PRF-55310 Group C/Qualification. In addition, we perform Terminal Strength testing per MIL-STD-202, Method 211, Test Condition C with the following exceptions: Load shall be 3 oz ± 0.3 oz, three bends at 90°.

3.1.6. Traceability and Homogeneity

All design pedigrees except option D have active device lots that are traceable to the manufacturer's individual wafer; all other elements and materials are traceable to their manufacturer and incoming inspection lots. Design pedigrees E, R, V and X have homogeneous material. In addition, swept quartz crystals are traceable to the quartz bar and the processing details of the autoclave lot.
A production lot, as defined by Microchip, is all oscillators that have been kitted and built as a single group. The maximum deliverable quantity with a single lot date code is 225 units. Order quantities that exceed 225 units will be delivered in multiple lot date codes with deliveries separated by 2 weeks. If applicable, each production lot will be kitted with homogeneous material which is then allocated across multiple lot date code builds to satisfy the deliverable order quantity. When ordered, Group C Inspection, lot qualifications, and/or DPA will be performed on the first build lot within the production lot unless otherwise stated on the purchase order.

3.2. Mechanical

3.2.1. Package Outline

Table 6-1 links each Hi-Rel Standard Model Number of this specification to a corresponding package style. Mechanical outline information of each package style is found in the referenced figure.

3.2.2. Thermal Characteristics

The worst-case thermal characteristics of each package style are found in Table 6-4.

3.2.3. Lead Forming

When the lead forming option is specified, the applicable leak test specified in screening will be performed after forming.

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3.3. Electrical

3.3.1. Input Power

Devices are available with an input voltage of either +5.0 Vdc (±10%) or +3.3 Vdc (±10%). Current is measured, no load, at maximum rated operating voltage.

3.3.2. Temperature Range

Operating range is −55 °C to +125 °C.

3.3.3. Frequency Tolerance

Initial accuracy at +23 °C is ±15 ppm maximum. Frequency-Temperature Stability is ±50 ppm maximum from +23 °C reference. Frequency-Voltage Tolerance is ±4 ppm maximum.

3.3.4. Frequency Aging

Aging limits, and when tested in accordance with MIL-PRF-55310 Group B inspection, shall not exceed ±1.5 ppm the first 30 days, ±5 ppm Year 1 and ±2 ppm per year thereafter.

3.3.4.1. Frequency Aging Duration Option

For Screening Option S, the Aging test will be terminated after 15 days if the measured aging rate is less than half of the specified aging rate. This is a common method of expediting 30-day Aging without incurring risk to the hardware and used quite successfully for numerous customers. It is based on the 'least squares fit' determinations of MIL-PRF-55310 paragraph 4.8.35. The 'half the time/half the spec' limit is generally conservative as roughly 2/3 of a unit's Aging deviation occurs within that period of time. Microchip's automated aging systems take about 6 data points per day, so a large amount of data is available to do very accurate projections, much more data than what is required by MIL-PRF-55310. The delivered data includes the Aging plots projected to 30 days. If the units do not perform within that limit, then they continue to the full 30-day term. For all other screening options, please make a note on the purchase order if this is an acceptable option as it assists in job planning and minimizes lead time.

3.3.5. Operating Characteristics

Symmetrical square wave limits are dependent on the device frequency and are in accordance with Table 6-2. Waveform measurement points and logic limits are in accordance with MIL-PRF-55310. Start-up time is 10.0 ms maximum.

3.3.6. Output Load

Standard TTL (6 or 10) and ACMOS (10 kΩ, 15 pF) test loads are in accordance with MIL-PRF-55310.

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4. Quality Assurance Provisions and Verification

4.1. Verification and Test

Device lots shall be tested prior to delivery in accordance with the applicable Screening Option letter as stated by the 15th character of the part number. Table 6-6 tests are conducted in the order shown and annotated on the appropriate process travelers and data sheets of the governing test procedure. For devices that require Screening Options that include MIL-PRF-55310 Group A testing, the Post-Burn-In Electrical Test and the Group A Electrical Test are combined into one operation.

4.1.1. Screening Options

The Screening Options, by letter, are summarized as:

Table 4-1. Screening Options

Screening Option	Description
A	Modified MIL-PRF-38534 Class K Screening
B	Modified MIL-PRF-55310 Class B Screening & Group A QCI
C	Modified MIL-PRF-55310 (Rev E) Class S Screening & Group A QCI
D	Modified MIL-PRF-38534 Class K Screening & 30-day Aging
E	Modified MIL-PRF-55310 Class B Screening & Groups A & B QCI
F	Modified MIL-PRF-55310 (Rev E) Class S Screening & Groups A & B QCI
G	Modified MIL-PRF-55310 Class B Screening & Post BI Nominal Electricals
S	MIL-PRF-55310 (Rev F) Class S Screening & Groups A & B QCI
X	Engineering Model (EM)

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4.2. Optional Design, Test, and Data Parameters

The following is a list of design, assembly, inspection, and test options that can be selected or added by purchase order request.

a. Design Pedigree (choose one as the 5th character in the part number)

Table 4-2. Design Pedigree

Design Pedigree	Description
E	Enhanced Element Evaluation (MIL-PRF-38534 Rev L for Class K components as specified in DOC208191), 100 krad die, Premium Q Swept Quartz
R	Hi-Rel design with 100 krad Class K die, Premium Q Swept Quartz
V	Hi-Rel design with 100 krad Class K die, Non-Swept Quartz
X	Hi-Rel design with Non-Swept Quartz, Class K die
B	Hi-Rel design with Premium Q Swept Quartz, Class B die
C	Hi-Rel design with Non-Swept Quartz, Class B die
D	Hi-Rel design with Non-Swept Quartz and commercial grade components

b. Input Voltage as the 14th character. See Ordering Part Number

c. Not Used

d. Radiographic Inspection

e. Group C Inspection: In accordance with (IAW) MIL-PRF-55310, Rev E (requires 8 destruct specimens). For Models 1105 and 1115, MIL-PRF-55310/26 frequency-environmental tolerance does not apply.

f. Group C Inspection: IAW MIL-PRF-55310, Rev F (requires 8 destruct specimens, includes Random Vibration, MIL-STD-883, Method 1014 Leak Test and Life Test). For Models 1105 and 1115, MIL-PRF-55310/26 frequency-environmental tolerance does not apply.

g. Group C Inspection: IAW MIL-PRF-38534, Table C-Xc, Condition PI (requires 8 destruct specimens – 5 pc. Life, 3 pc. RGA). Subgroup 1 fine leak test to be performed per MIL-STD-202, Method 112, Condition C.

h. Internal Water-Vapor Content (RGA) samples and test performance

i. MTBF Reliability Calculations: IAW MIL-HDBK-217 unless otherwise specified

j. Worst Case Circuit Analysis: IAW MIL-HDBK-1547 unless otherwise specified

k. Derating and Thermal Analysis: IAW MIL-HDBK-1547 with Tj Max = +105 °C; Derated Maximum Operating Temp = Tj Max – ΔTj unless otherwise specified

l. Process Identification Documentation (PID)

m. Customer Source Inspection (pre-crystal mount pre-cap, post-crystal mount pre-cap and final). Due to components being mounted underneath the crystal blank, the following model numbers should be considered for pre-crystal mount pre-cap inspection: 1103, 1109, 1115, 1116, 1117, 1119, 1157, 1167, 1177, 1187, 1179, 1189 and 1199.

n. Destruct Physical Analysis (DPA): IAW MIL-STD-1580 with exceptions as specified in Microchip DOC203982. When ordering destruct specimens for DPA performance on 1157, 1167, 1177 or 1187 platforms, you must order separate destruct specimens for RGA testing and the balance of DPA due to the likelihood of crystal damage during the puncturing of the 5x7 mm enclosure. The DPA leak test specified will agree with the screening option selected.

o. Qualification: IAW MIL-PRF-55310, Rev F, Table IV (requires 16 destruct specimens). Includes Group III, SG1 through SG6 only. ESD (SG7) not performed.

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p. Qualification: IAW EEE-INST-002, Section C4, Table 3, Level 1 or 2 (requires 11 destruct specimens)

q. High Resolution Digital Pre-Cap Photographs (20 Megapixels minimum for all devices except 1157, 1167, 1177 and 1187 which will use 10 Megapixels minimum).

r. Hot solder dip of leads with Sn63/Pb37 solder prior to shipping.

s. As Designed Parts, Materials and Processes List

4.2.1. NASA EEE-INST-002 Compliance

A combination of Design Pedigree R, Option S Screening, and performance of Qualification per EEE-INST-002, Section C4, Table 3 on 11 destruct specimens, meet the requirements of Level 1 and Level 2 device reliability.

4.3. Test Conditions

Unless otherwise stated herein, inspections are performed in accordance with those specified in MIL-PRF-55310. Process travelers identify the applicable methods, conditions, and procedures to be used. Examples of electrical test procedures that correspond to MIL-PRF-55310 requirements are shown in Table 6-3.

4.4. Delta Limit Exception

When MIL-PRF-55310, Revision F was being reviewed for release by manufacturers and users, Microchip and other organizations recommended that burn-in delta limits not be applied to logic-level measurements due to the inconsistency in attempting to measure small changes in logic levels which inherently have ringing in the signal. This is especially true in higher frequency oscillators measured in automated test systems that are affected by cable length that is not representative of the user's application and contact resistance in test fixtures that do not provide a consistent Vcc or Ground connection. The exact test setup conditions may vary slightly from pre-burn-in to post-burn-in and cause small artificial deltas in logic-level measurements that are not indicative of an issue. Any significant changes in logic levels will be reflected in supply current deltas and/or logic levels that exceed the min/max limits. As a result, we take exception to MIL-PRF-55310, Revision F, Para. 4.4.5 and the delta limit for Output Low Level as specified in 4.4.5(c) shall not be applied to Burn-in PDA.

4.5. Deliverable Data

The manufacturer supplies the following data, as a minimum, with each lot of devices:

a. As applicable to the Screening Option chosen, completed assembly and screening lot travelers, screening data, including radiographic images, and rework history.

b. Electrical test variables data, identified by unique serial number.

c. Special items when required by purchase order such as Group C, DPA, and RGA data. Unless otherwise specified on purchase order, all destruct specimens will be shipped. As delivered, all destruct specimens will be identified by subgroup (if applicable) and packaged separately from flight units.

d. For Design Pedigrees E, R, V, and X, traceability, component LAT, enclosure LAT, and wafer lot specific RLAT data for non-SMD active devices (if applicable).

e. Certificate of Conformance.

4.6. Discrepant Material

All MRB authority resides with the procuring activity.

4.7. Failure Analysis

Any failure during Qualification or Group C Inspection will be evaluated for root cause. The customer will be notified after occurrence and upon completion of the evaluation.

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5. Preparation for Delivery

5.1. Packaging

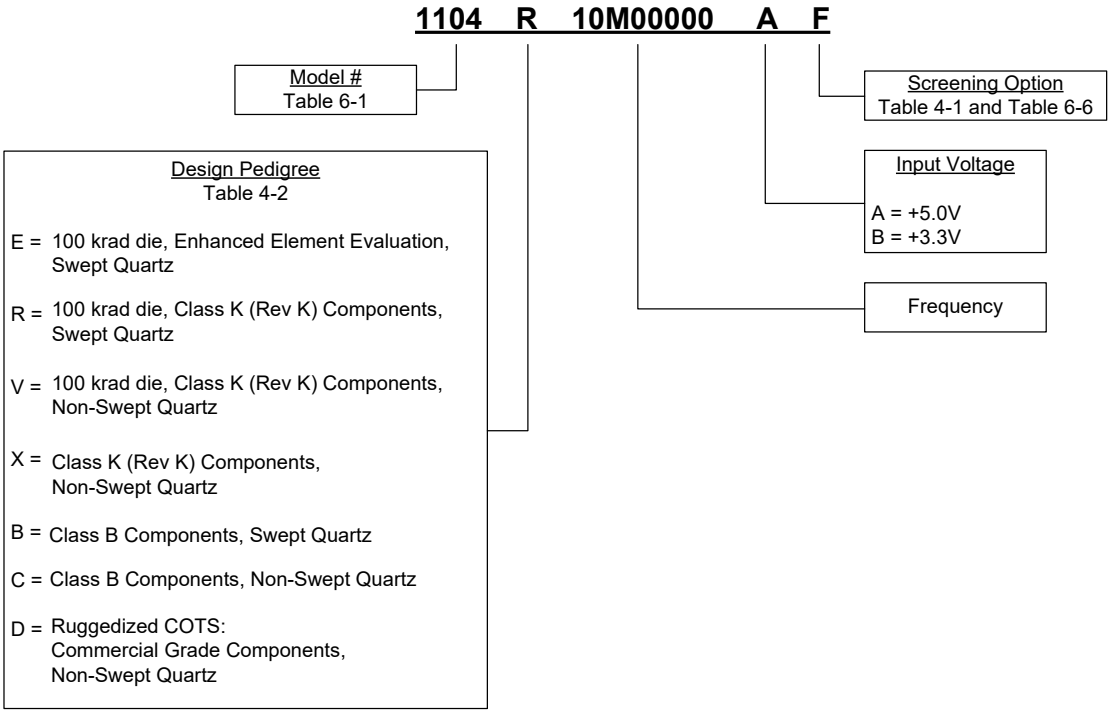
Devices will be packaged in a manner that prevents handling and transit damage during shipping. Devices will be handled in accordance with ANSI/ESD S20.20. Devices will be packaged for transport in accordance with DOC220429. Please note that “one unit per package” is available for a fee; however, this service must be requested as part of the official RFQ.

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6. Ordering Information

6.1. Ordering Part Number

The ordering part number consists of an alphanumeric string of 15 continuous characters, without spaces.



6.1.1. Model Number

The device model number is the four (4) digit number assigned to a corresponding package and output combination per Table 6-1.

6.1.2. Design Pedigree

Class S designs are identified by the letters “E,” “R,” “V,” or “X,” while Class B designs are indicated by either the letter “B” or “C”. Ruggedized COTS, which utilize commercial grade components, are designated by the letter “D”.

6.1.3. Output Frequency

The nominal output frequency is expressed in the format as specified in MIL-PRF-55310 utilizing eight (8) total characters. (Example: 32.768 kHz = 32K76800, 12 MHz = 12M00000, 100 MHz = 100M0000)

6.1.4. Input Voltage

Voltage is the 14th character, letters “A” representing +5.0V and “B” for +3.3V.

6.1.5. Screening Options

The 15th character is the Screening Option selected from Table 6-6.

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6.2. Electrical Characteristics and Test Parameters

Optional test and documentation requirements shall be specified by separate purchase order line items (as listed in 4.2. Optional Design, Test, and Data Parameters).

Table 6-1. Item Identification and Package Outline

Hi-Rel Standard Model #	Package	Output, Square Wave	Pin I/O[1]				Mechanical Outline
			Vcc	Out	Gnd/ Case	E/D[2]	
1101	12 Lead Flatpack	ACMOS	12	7	6	na	Figure 6-1
1102	14 Lead Flatpack	ACMOS	14	8	7	na	Figure 6-2
1103	16 Lead Flatpack	ACMOS	8	10	9	na	Figure 6-3
1104	20 Lead Flatpack	ACMOS	13, 20	11	10	na	Figure 6-5
1105	14 Pin DIP	ACMOS	14	8	7	na	Figure 6-6
1115	4 pin ½ DIP	ACMOS	8	5	4	na	Figure 6-4
1116	J-lead SMT	ACMOS	4	3	2	1	Figure 6-7
1157[3]	4 pad 5 x 7mm	ACMOS	4	3	2	1	Figure 6-8
1119[4]	16 Lead Flatpack	ACMOS	8	10	9	na	Figure 6-9
1120[4]	20 Lead Flatpack	ACMOS	13, 20	11	10	na	Figure 6-10
1121[4]	12 Lead Flatpack	ACMOS	12	7	6	na	Figure 6-11
1122[4]	14 Lead Flatpack	ACMOS	14	8	7	na	Figure 6-12
1167	5 x 7mm, Straight Lead	ACMOS	4	3	2	1	Figure 6-13
1177	5 x 7mm, Inward Lead	ACMOS	4	3	2	1	Figure 6-14
1187	5 x 7mm, Outward Lead	ACMOS	4	3	2	1	Figure 6-15
1179	7 x 9mm, Straight Lead	ACMOS	4	3	2	1	Figure 6-16
1189	7 x 9mm, Inward Lead	ACMOS	4	3	2	1	Figure 6-17
1199	7 x 9mm, Outward Lead	ACMOS	4	3	2	1	Figure 6-18
1107	12 Lead Flatpack	TTL	12	7	6	na	Figure 6-1
1108	14 Lead Flatpack	TTL	14	8	7	na	Figure 6-2
1109	16 Lead Flatpack	TTL	8	10	9	na	Figure 6-3
1110	20 Lead Flatpack	TTL	13, 20	11	10	na	Figure 6-5
1111	14 Pin DIP	TTL	14	8	7	na	Figure 6-6
1117	J-lead SMT	TTL	4	3	2	1	Figure 6-7

Notes:

1. All unassigned pins have no internal connections or ties. We recommend all unassigned pins be tied to ground. Lids are internally tied to case ground.
2. A logic “1” (>+2.0V) or open on pin 1 will enable the output. A logic “0” (<+0.8V) will disable the output.
3. Model 1157 replaces previous Model 1118.
4. Models 1119 through 1122 are lead formed versions of Models 1101 through 1104.
   See 7. Recommended Land Patterns for recommended land patterns.

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Table 6-2. Electrical Performance Characteristics

Parameter	Value
Frequency Range	12.0 kHz to 100.0 MHz[3, 4, 5]
Temperature Range	-55°C to +125°C
Frequency Tolerance, Initial Accuracy @ +23°C	±15 ppm max.
Frequency-Temperature Stability from +23°C ref.	±50 ppm max.
Frequency-Voltage Tolerance	±4 ppm max. (Vcc ±10%)
Frequency Aging	±1.5 ppm max. 1st 30 days, ±5 ppm max. Year 1, ±2 ppm max. Year 2+ (Estimated maximum aging for 20 years will be <10 ppm due to the non-linear characteristics of crystal aging)
Start-up Time	10.0 ms max.

Frequency Range (MHz)[3, 4, 5]	Current (mA) (max. no load)		Models 1157 thru 1187 Only Current (mA) (max. no load)		Rise /Fall Times[1] (ns max.)	Duty Cycle[1] (%)		Fan-out (if TTL)[2]
	+5.5V	+3.63V	+5.5V	+3.63V		CMOS	TTL	
.012 – 0.35	8	4	N/A	N/A	6	45 to 55	45 to 55	10
>0.35 - 4.0	10	6	10	6	6	45 to 55	45 to 55	10
>4.0 – 12.0	15	8	15	8	5	45 to 55	45 to 55	10
>12.0 – 24.0	15	10	15	10	5	45 to 55	40 to 60	10
>24.0 – 40.0	20	15	20	15	5	45 to 55	40 to 60	6
>40.0 – 65.0	35	20	40	25	5	45 to 55	40 to 60	6
>65.0 – 85.0	45	25	50	30	3	45 to 55	40 to 60	6
>85.0 – 100	55	30	N/A	35	3	40 to 60	40 to 60	6

Notes:

1. Waveform measurement points and logic limits are in accordance with MIL-PRF-55310, Para 3.6.20.3.
2. For +3.3V TTL option, R_L=160Ω for 10 TTL loads and R_L=270Ω for 6 TTL loads.
3. Exception: Models 1157/1167/1177/1187 frequency range is 0.75 MHz to 100 MHz.
   Maximum frequency limit with +5.0V supply voltage is 85 MHz.
4. Exception: Models 1179/1189/1199 maximum frequency limit is 70 MHz.
5. 0.012-0.35 MHz only available in Models 1103 and 1119.

Table 6-3. Electrical Test Parameters

Operation Listing	Requirements and Conditions
PERFORMED DURING ALL ELECTRICAL TESTS	
Input Current (no load)	MIL-PRF-55310, Para 4.8.5.1
Initial Accuracy at Reference Temperature	MIL-PRF-55310, Para 4.8.6
Output Logic Voltage Levels	MIL-PRF-55310, Para 4.8.21.3
Rise and Fall Times	MIL-PRF-55310, Para 4.8.22
Duty Cycle	MIL-PRF-55310, Para 4.8.23
PERFORMED DURING POST BURN-IN ELECTRICAL ONLY	
Overvoltage Survivability	MIL-PRF-55310, Para 4.8.4
Initial Frequency – Temperature Accuracy	MIL-PRF-55310, Para 4.8.10.1
Frequency – Voltage Tolerance	MIL-PRF-55310, Para 4.8.14
Start-up Time	MIL-PRF-55310, Para 4.8.29

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Table 6-4. Typical Thermal Characteristics and Weight

Model #	Typical Thermal Resistance Junction to Case θ_{jc} (°C/W)	Δ Junction Temperature T_j (°C @ max. Icc)[1]	Typical Weight (grams)
1101/1107/1121	30.77	9.31	3.0
1102/1108/1122	30.77	9.31	3.3
1103/1109/1119	27.88	8.44	1.4
1104/1110/1120	30.05	9.09	2.9
1105/1111	27.88	8.44	3.9
1115	29.92	9.05	2.2
1116/1117	31.62	9.57	1.2
1157/1167/1177/1187	12.84	3.53	0.2
1179/1189/1199	15.80	3.91	0.5

Note:
Maximum operating power from Table 6-2 is used to calculate Δ junction temperatures.

Table 6-5. Typical Jitter Performance

	Vcc=+5.0V			Vcc=+3.3V		
Frequency	Period Jitter 1 sigma (ps)	Phase Jitter 12 kHz to 20 MHz (ps)	Period Jitter pk-pk (ps)	Period Jitter 1 sigma (ps)	Phase Jitter 12 kHz to 20 MHz (ps)	Period Jitter pk-pk (ps)
24 MHz	6	0.22	48	4.2	0.33	35
40 MHz	5	0.16	40	3.7	0.25	26
80 MHz	5	0.08	40	3.6	0.14	28
100 MHz	4	0.08	32	3.3	0.14	23

Note: Period Jitter measured at +23°C and Nominal Voltage.

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Table 6-6. Screening Test Matrix

OPN. NO.	Operation Listing	Requirements and Conditions	Option A	Option B	Option C	Option D	Option E	Option F	Option G	Option S	Option X
	SCREENING	MIL Class Similarity (MIL-PRF-55310, Class S/B or MIL-PRF-38534, Class K)	K 100%	B- 100%	S- 100%	K+ 100%	B 100%	S (Rev E) 100%	— 100%	S (Rev F) 100%	EM 100%
1	Non-Destruct Bond Pull	MIL-STD-883, Method 2023	X	NR	X	X	NR	X	NR	X	NR
2	Internal Visual	MIL-STD-883, Method 2017 Class K, Method 2032 Class K	X	X	X	X	X	X	X	X	X
3	Stabilization (Vacuum) Bake	MIL-STD-883, Method 1008, Cond. C, 150 °C	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 24 hrs.
4	Random Vibration	MIL-STD-883, Method 2026, Cond. I-B, 15 mins in each axis	NR	NR	NR	NR	NR	NR	NR	X	NR
5	Thermal Shock	MIL-STD-883, Method 1011, Cond. A	NR	NR	X	NR	NR	X	NR	X	NR
6	Temperature Cycle	MIL-STD-883, Method 1010, Cond. B (except Option S), 10 cycles min.	X	X	X	X	X	X	X	X Cond. C	NR
7	Constant Acceleration	MIL-STD-883, Method 2001, Cond. A,Y1 plane only, 5000g	X	X	X	X	X	X	X	X	NR
8	Particle Impact Noise Detection	MIL-STD-883, Method 2020, Cond. B (except Option S)	X	X	X	X	X	X	NR	X Cond. A	X[5]
9	Electrical Testing, Pre Burn-In	Perform tests in Table 6-3. Nominal Vcc, nominal temperature	X	X	X	X	X	X	X	X	X
10	1st Burn-In	MIL-STD-883, Method 1015, Cond. B	X 160 hrs.	X 160 hrs.	X 240 hrs.	X 160 hrs.	X 160 hrs.	X 240 hrs.	X 160 hrs.	X 240 hrs.	NR
11	Electrical Testing, Intermediate	Perform tests in Table 6-3. Nominal Vcc, nominal temperature	X	NR	NR	X	NR	NR	NR	NR	NR
12	2nd Burn-In	MIL-STD-883, Method 1015, Cond. B	X 160 hrs.	NR	NR	X 160 hrs.	NR	NR	NR	NR	NR
13	Electrical Testing, Post Burn-In (Group A)[4]	Perform tests in Table 6-3. Nominal Vcc and extremes, nominal temperature and extremes	X	X	X	X	X	X	X nom. Vcc	X	NR
14	Seal: Fine Leak Seal: Gross Leak	MIL-STD-202, Method 112, Cond. C (5×10^{-8} atm cc/sec max) MIL-STD-202, Method 112, Cond. D	X	X	X	X	X	X	X	NR	X
15	Seal: Fine Leak Seal: Gross Leak	MIL-STD-883, Method 1014, Cond. A2 or B1 MIL-STD-883, Method 1014, Cond. B2 or B3	NR	NR	NR	NR	NR	NR	NR	X	NR
16	Radiographic Inspection	MIL-STD-883, Method 2012	X	AR	AR	X	AR	X	NR	X	NR
17	Solderability	MIL-STD-883, Method 2003	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]	NR
18	External Visual and Mechanical	MIL-STD-883, Method 2009	X[2]	X[2]	X[2]	X[2]	X[2]	X[2]	X[2]	X[2]	X[2]
19	Aging, 30 Day[3] (M55310 Group B)	MIL-PRF-55310, para. 4.8.35.1	NR	NR	NR	X	13 pcs.	X	NR	X	NR
20	Group C Inspection (optional)	See 4.2. Optional Design, Test, and Data Parameters for details of supplier recommended Group C Inspection options	4.2(g)	4.2(e)	4.2(e)	4.2(g)	4.2(e)	4.2(e)	4.2(e)	4.2(f)	NR

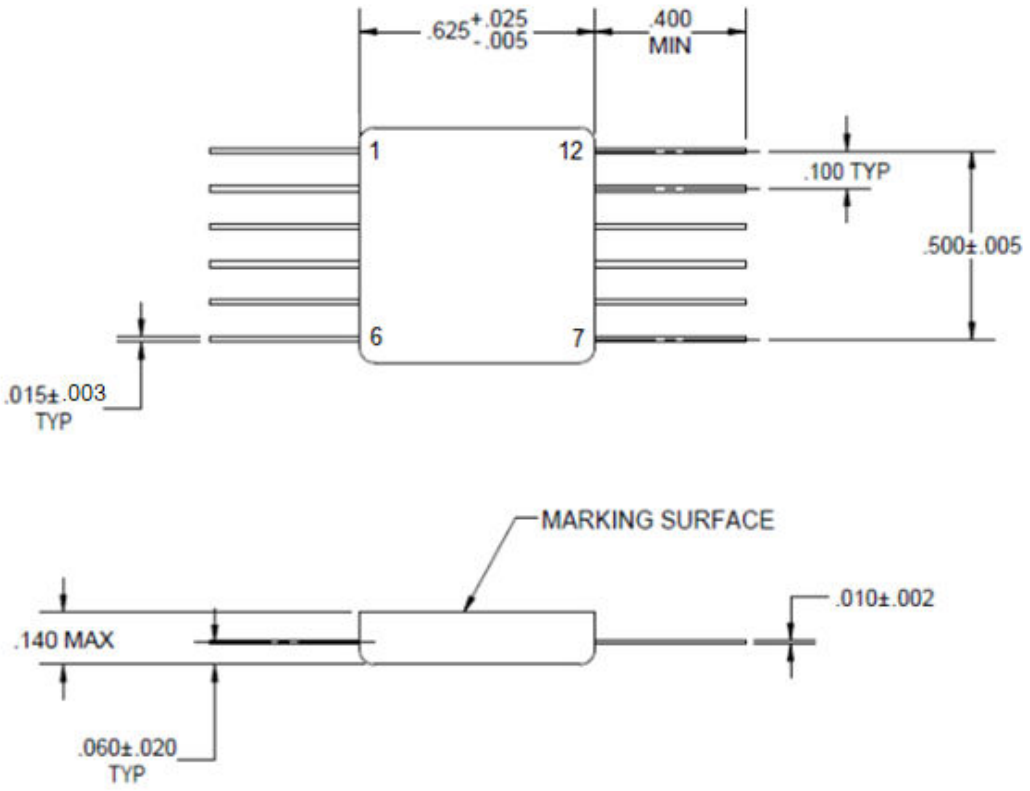
Legend: X = Required, NR = Not Required, AR = As Required

Notes:

1. Performed at package LAT. Include LAT data sheet.
2. When specified, RGA samples will be removed from the lot after completion of this operation. Use of Screening failures require customer concurrence.
3. See 3.3.4.1. Frequency Aging Duration Option.
4. See 4.4. Delta Limit Exception.
5. PIND PDA does not apply.

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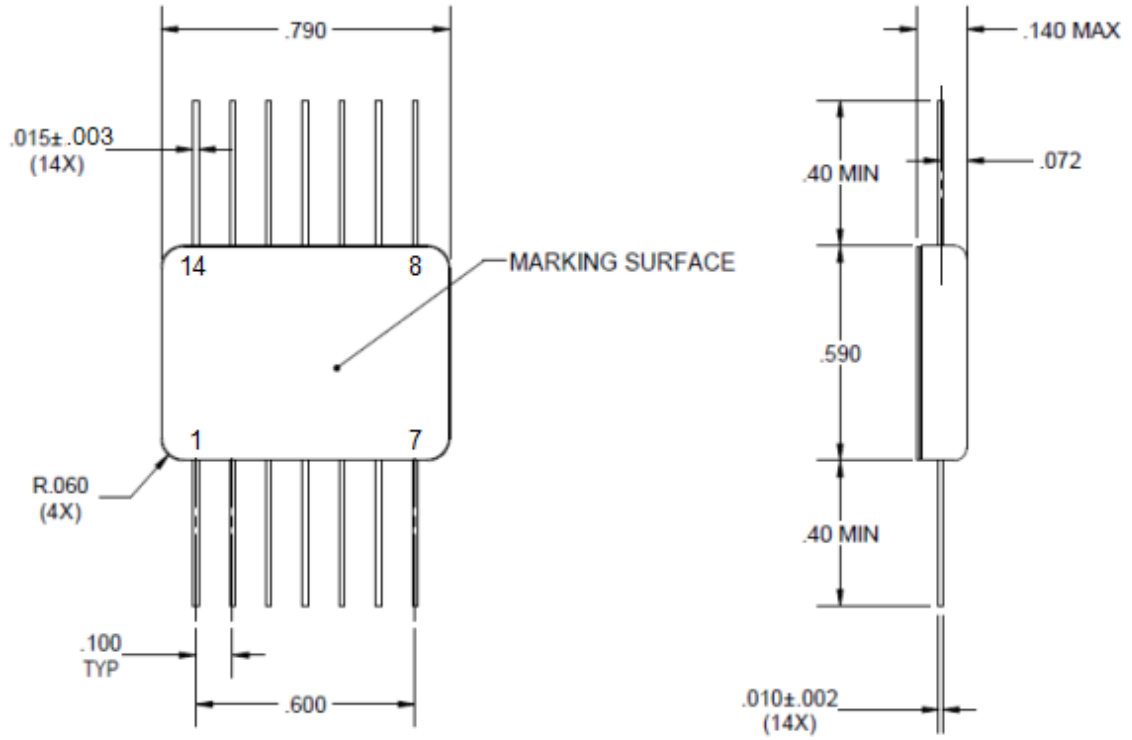
Figure 6-1. Models 1101/1107 Package Outline



Pin	Function
6	GND/Case
7	Output
12	Vcc
All Others	No Internal Connection

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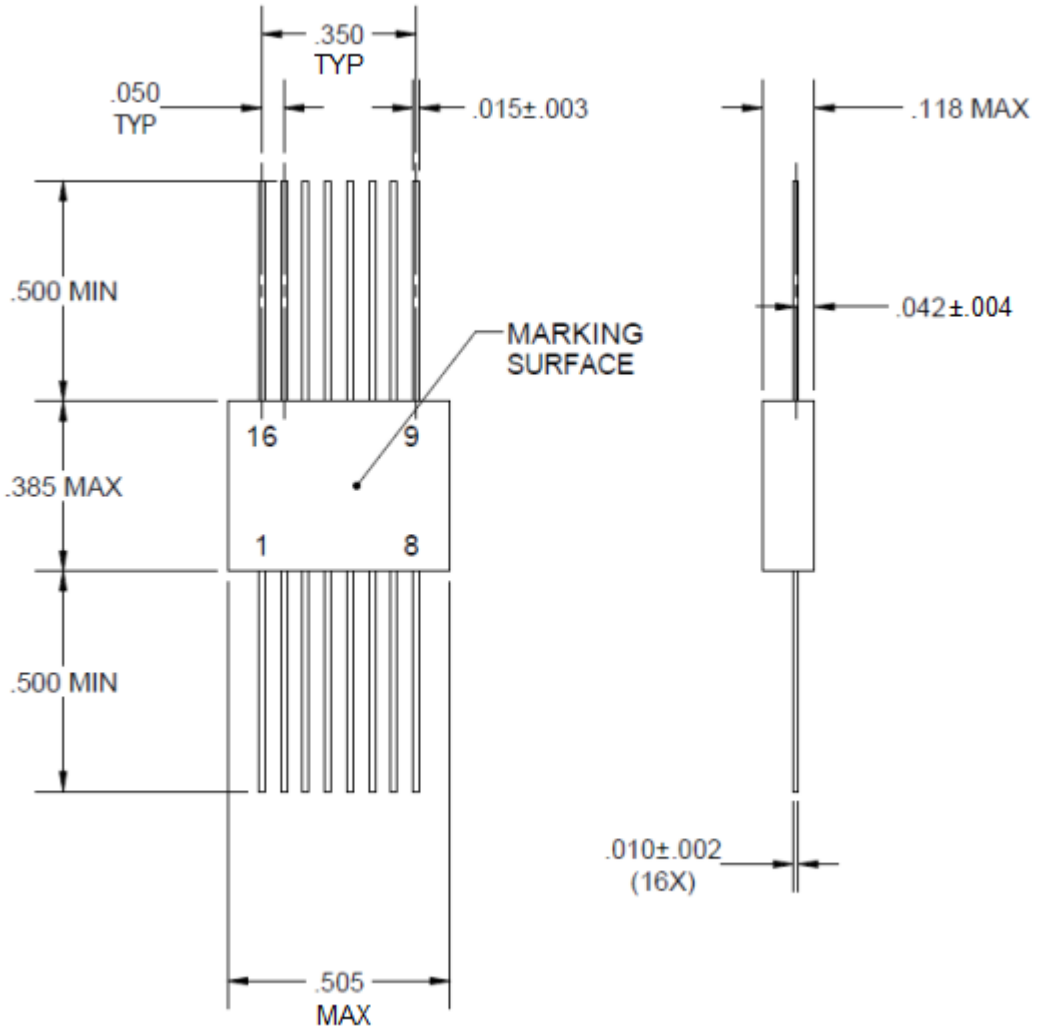
Figure 6-2. Models 1102/1108 Package Outline



Pin	Function
7	GND/Case
8	Output
14	Vcc
All Others	No Internal Connection
Note: Tolerances: Unspecified = ±0.010”	

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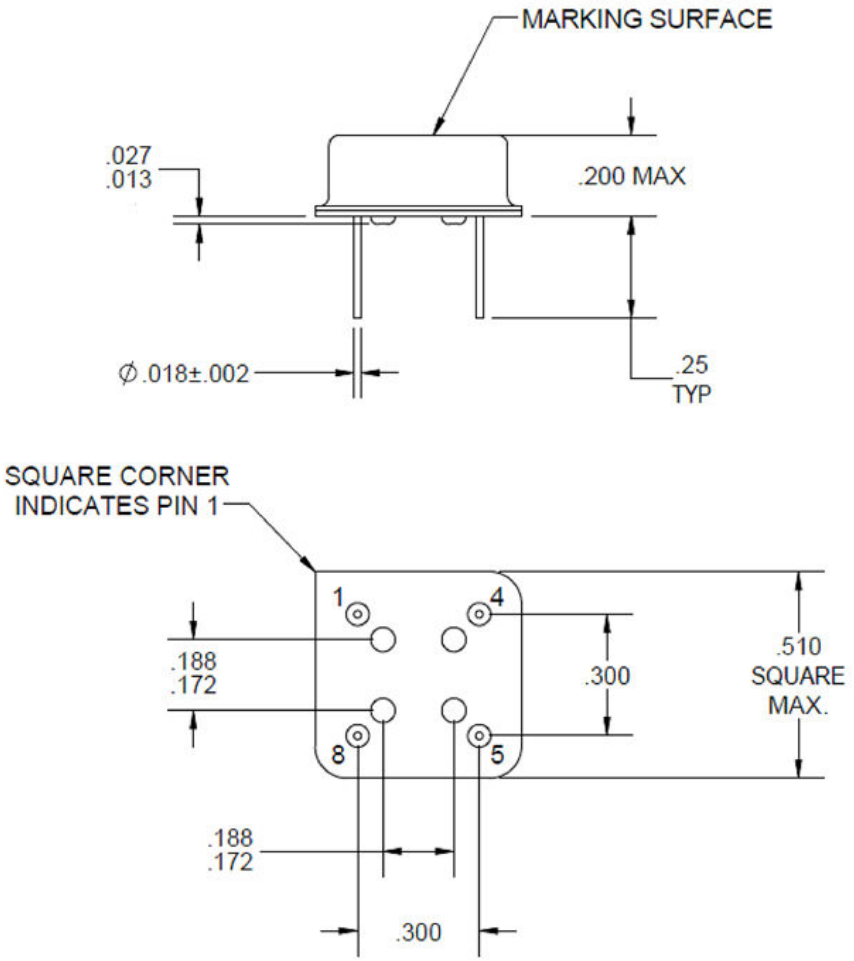
Figure 6-3. Models 1103/1109 Package Outline



Pin	Function
9	GND/Case
10	Output
8	Vcc
All Others	No Internal Connection

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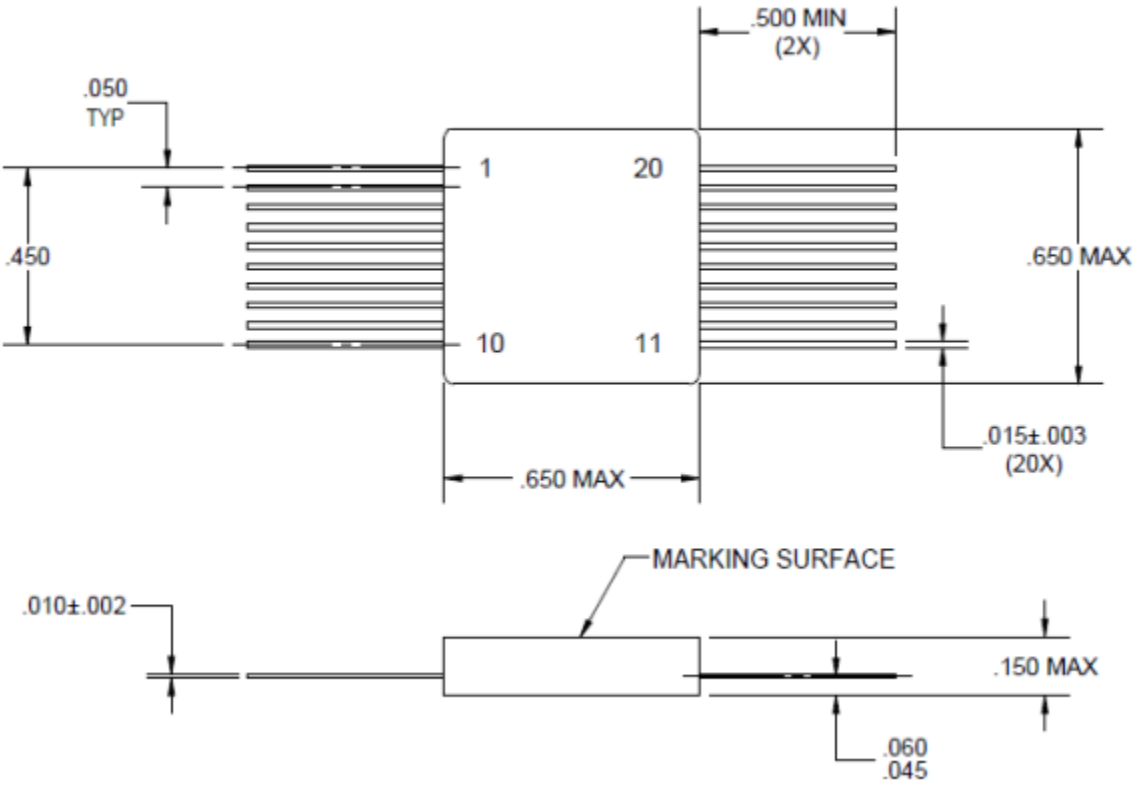
Figure 6-4. Model 1115 Package Outline



Pin	Function
4	GND/Case
5	Output
8	Vcc
All Others	No Internal Connection
Note: Tolerances: Unspecified = ±0.010”	

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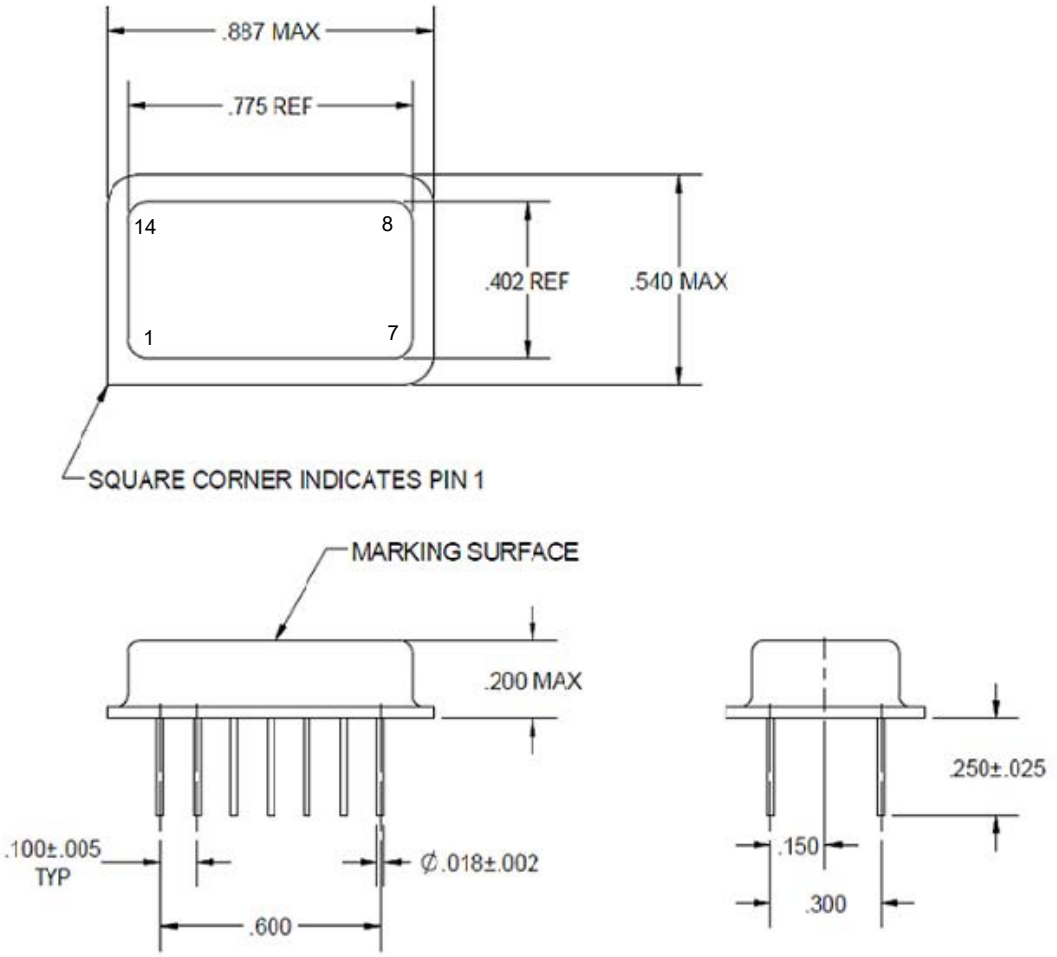
Figure 6-5. Model 1104/1110 Package Outline



Pin	Function
10	GND/Case
11	Output
13, 20	Vcc
All Others	No Internal Connection
Note: Tolerances: Unspecified = ±0.010”	

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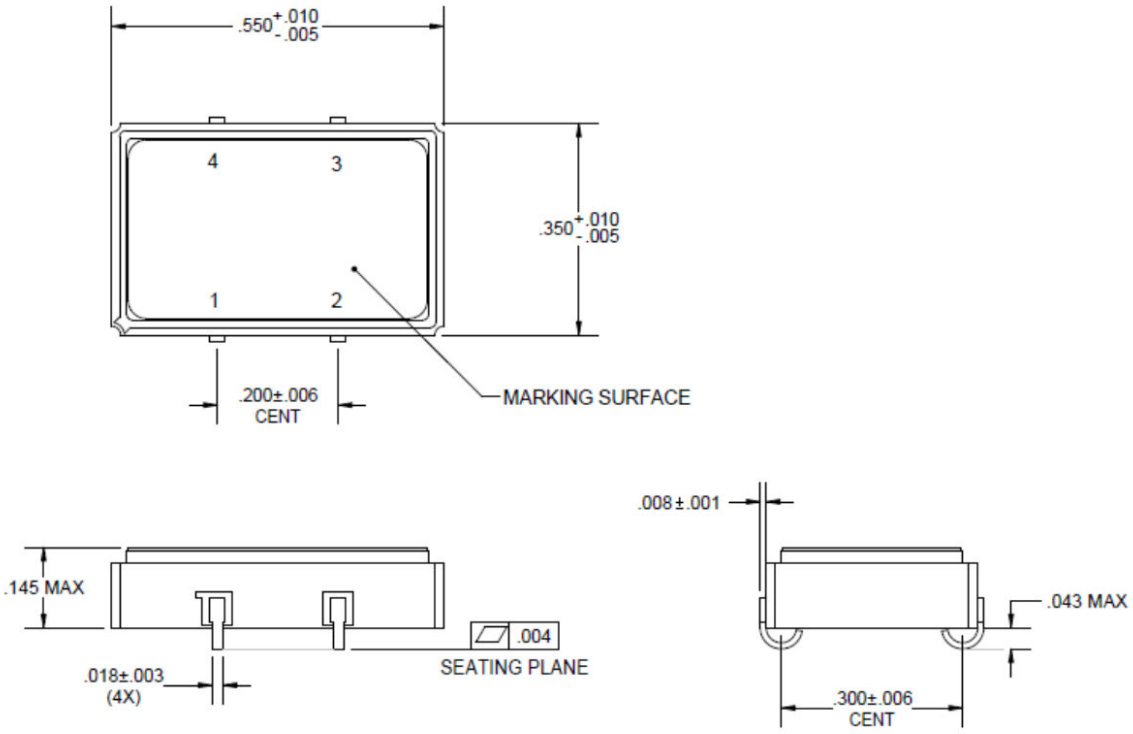
Figure 6-6. Model 1105/1111 Package Outline



Pin	Function
7	GND/Case
8	Output
14	Vcc
All Others	No Internal Connection
Note: Tolerances: Unspecified = ±0.010”	

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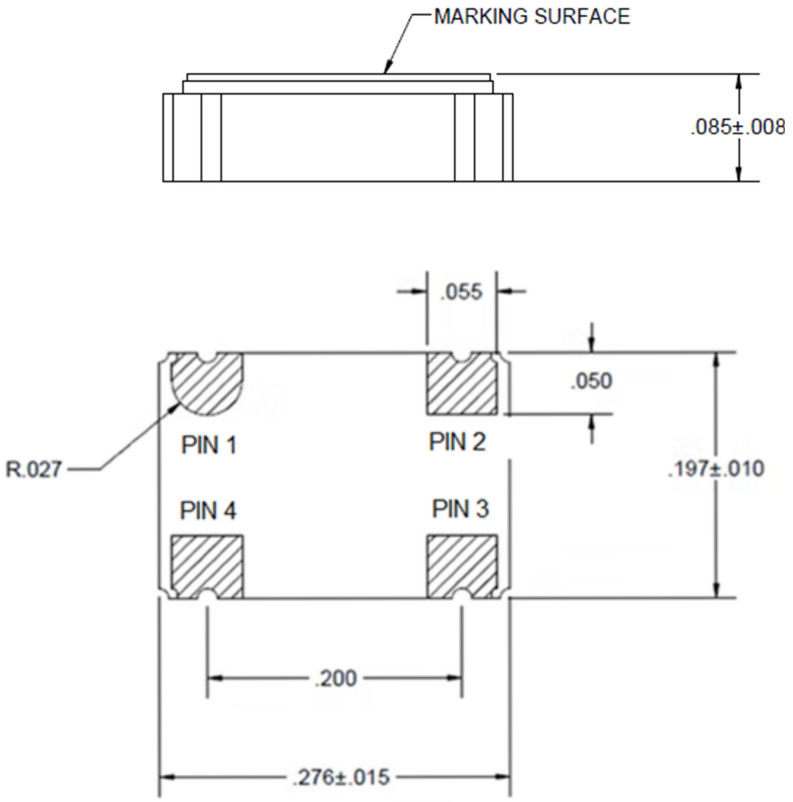
Figure 6-7. Model 1116/1117 Package Outline



Pin	Function
1	Enable/Disable
2	GND/Case
3	Output
4	Vcc

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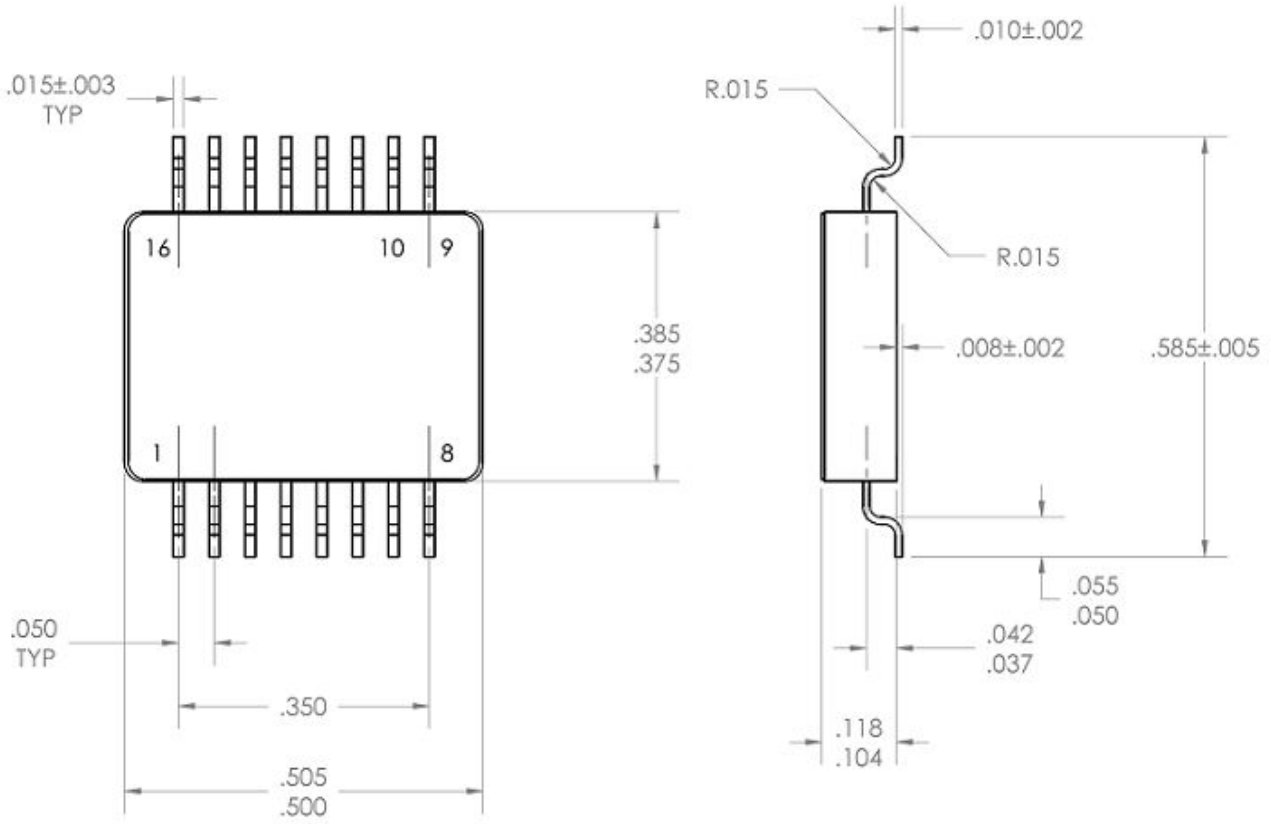
Figure 6-8. Model 1157 Package Outline



Pin	Function
1	Enable/Disable
2	GND/Case
3	Output
4	Vcc
Note: Tolerances: Unspecified = ±0.010”	

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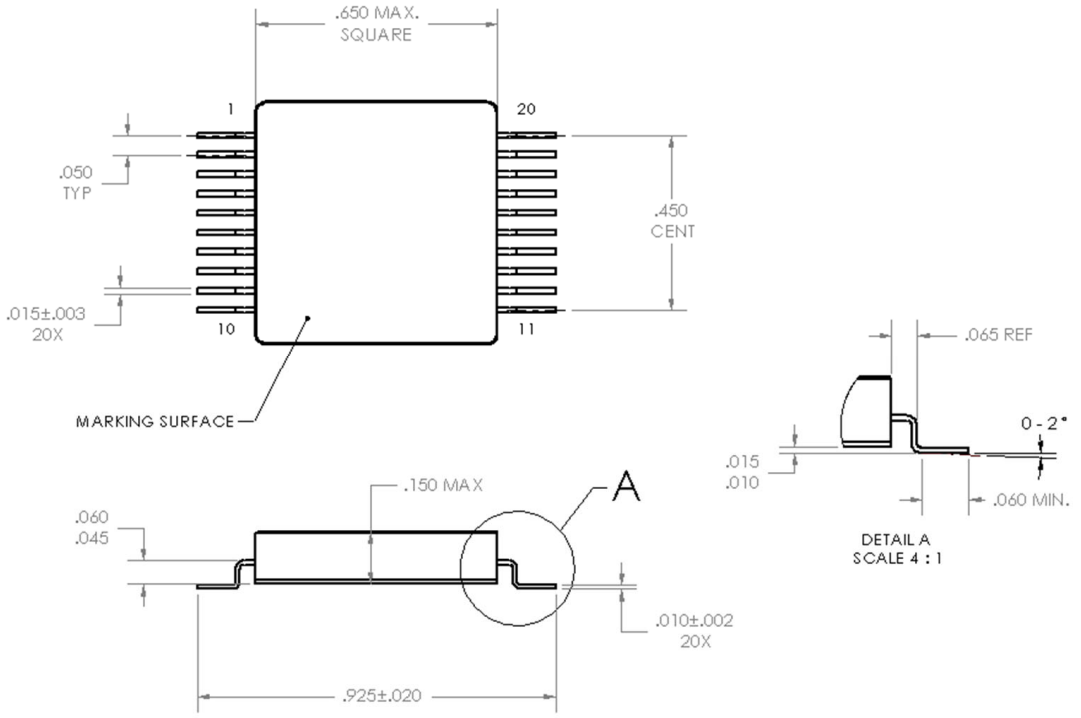
Figure 6-9. Model 1119 Package Outline



Pin	Function
9	GND/Case
10	Output
8	Vcc
All Others	No Internal Connection
Note: Tolerances: Unspecified = ±0.010”	

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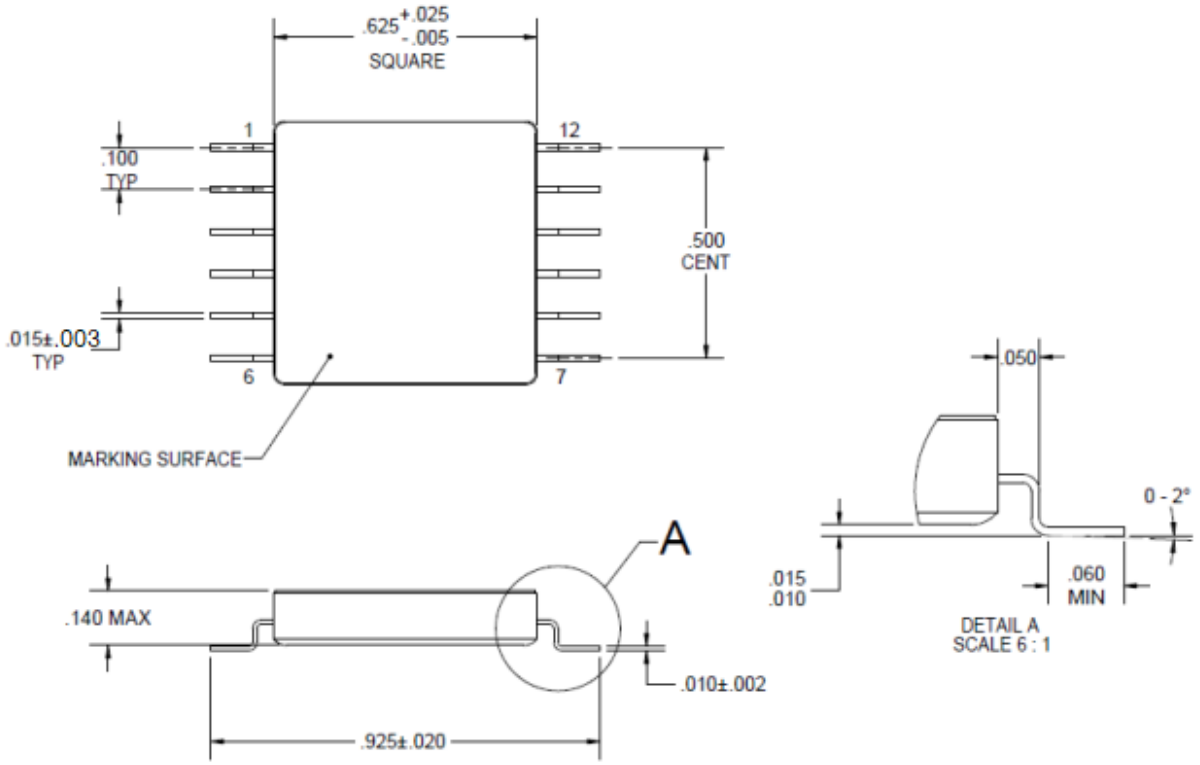
Figure 6-10. Model 1120 Package Outline



Pin	Function
10	GND/Case
11	Output
13, 20	Vcc
All Others	No Internal Connection
Note: Tolerances: Unspecified = ±0.010”	

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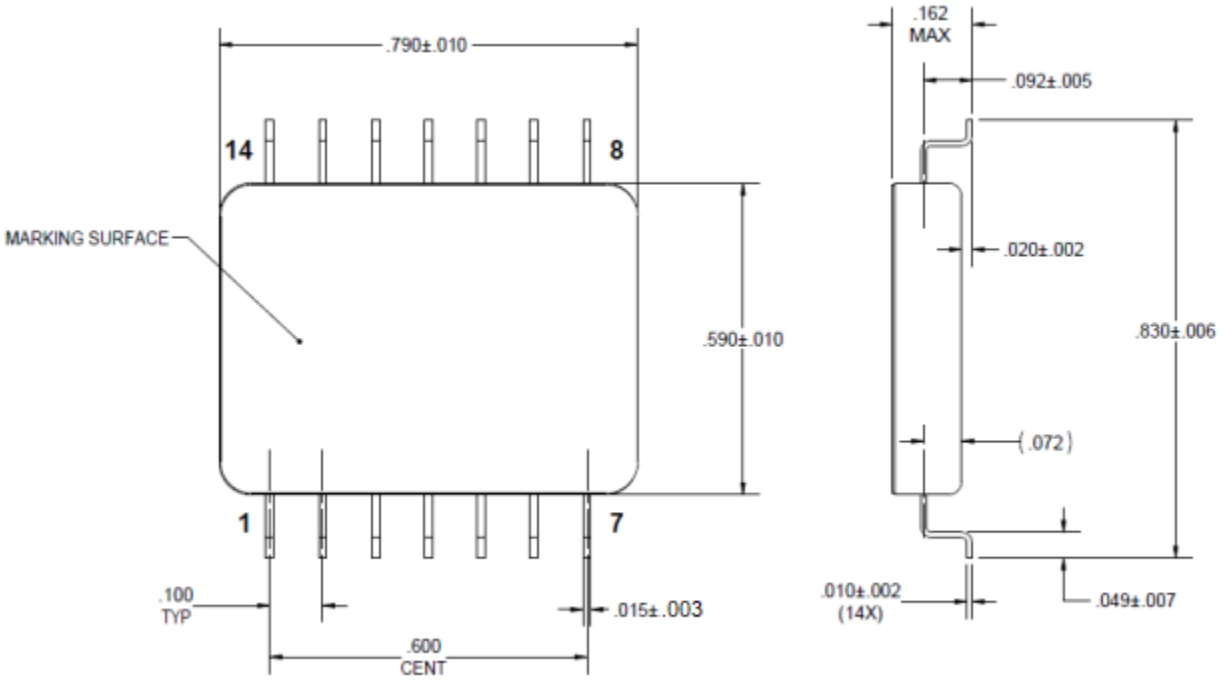
Figure 6-11. Model 1121 Package Outline



Pin	Function
6	GND/Case
7	Output
12	Vcc
All Others	No Internal Connection
Note: Tolerances: Unspecified = ±0.010”	

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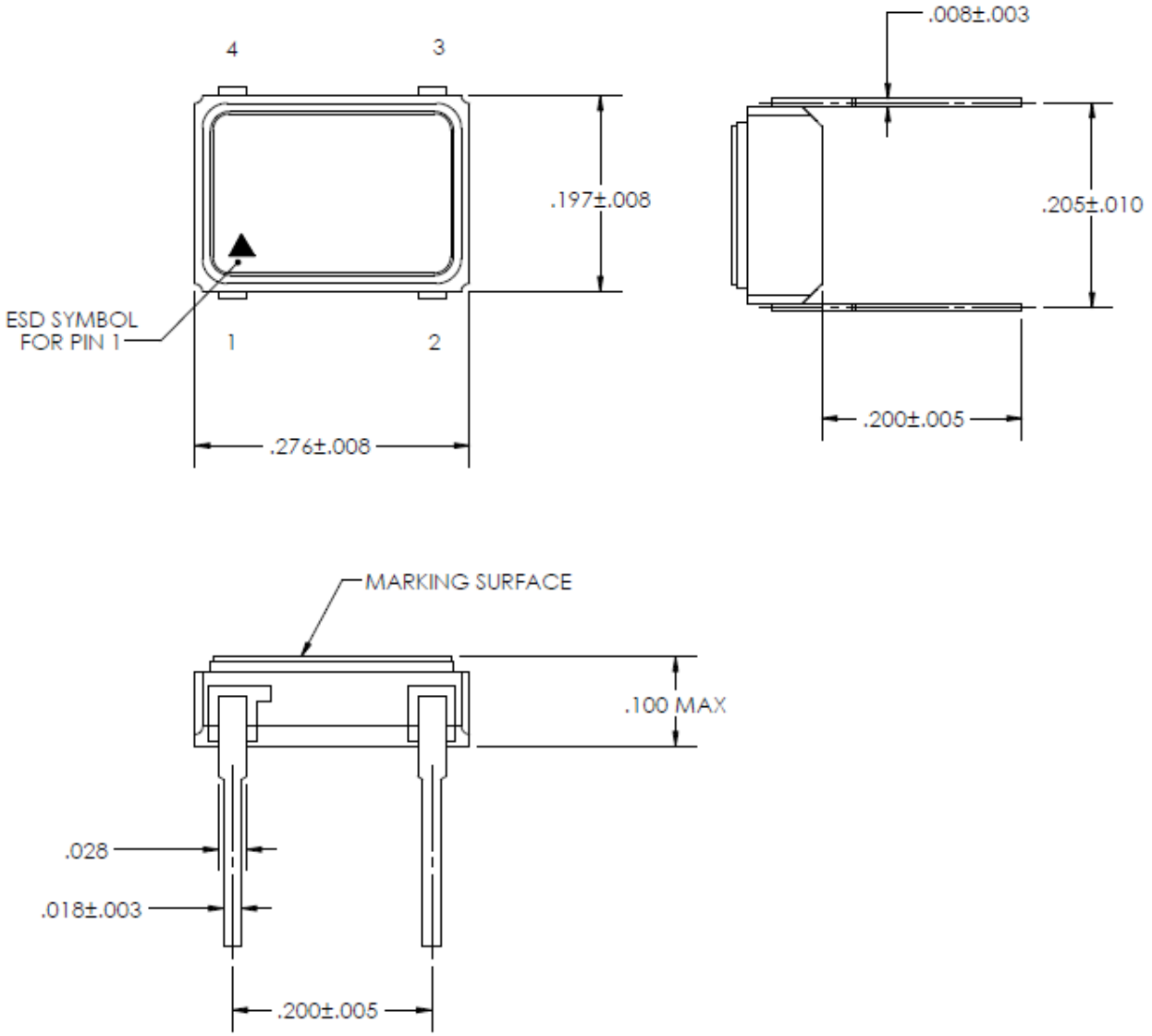
Figure 6-12. Model 1122 Package Outline



Pin	Function
7	GND/Case
8	Output
14	Vcc
All Others	No Internal Connection

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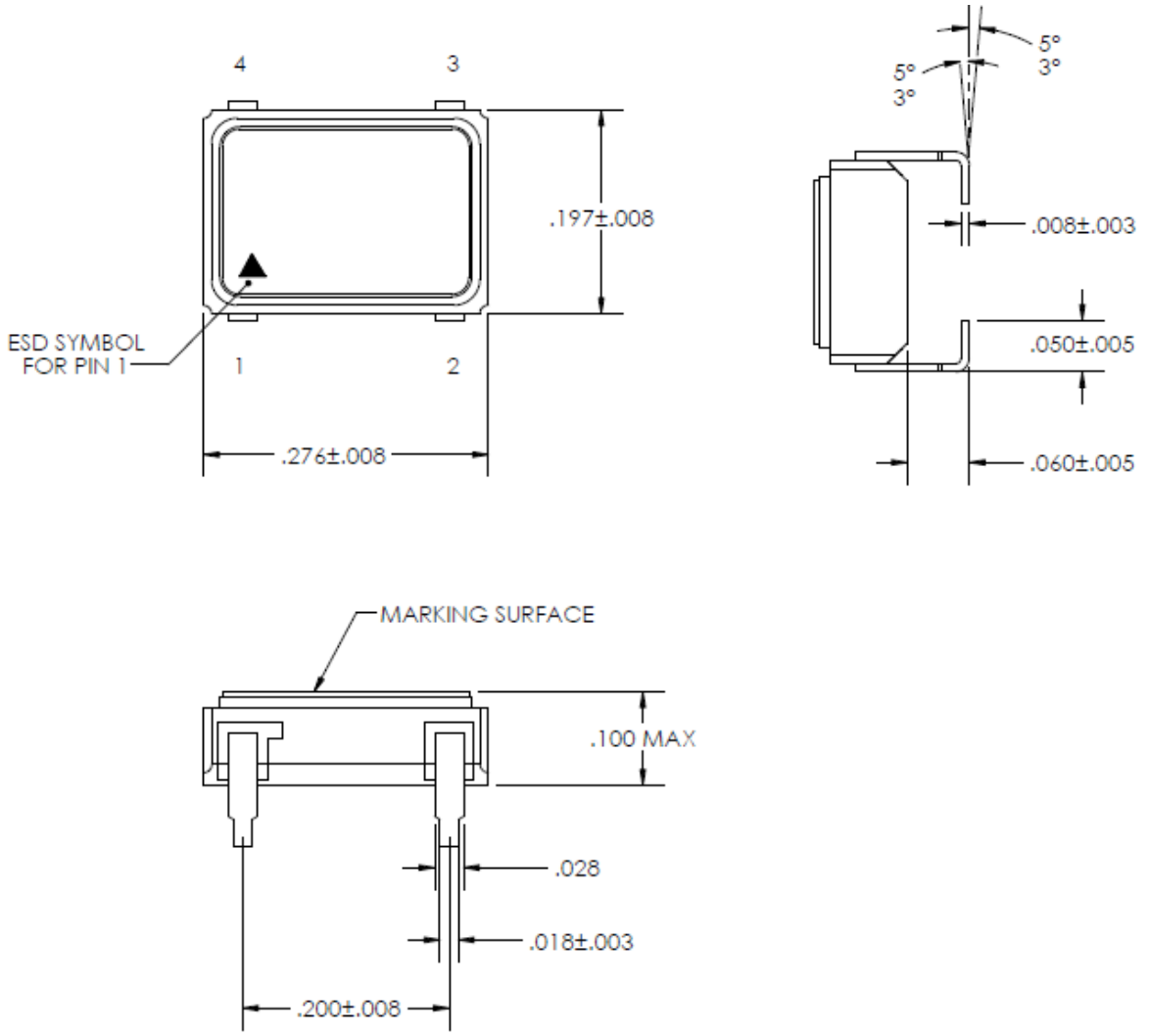
Figure 6-13. Model 1167 Package Outline



Pin	Function
1	Enable/Disable
2	GND/Case
3	Output
4	Vcc

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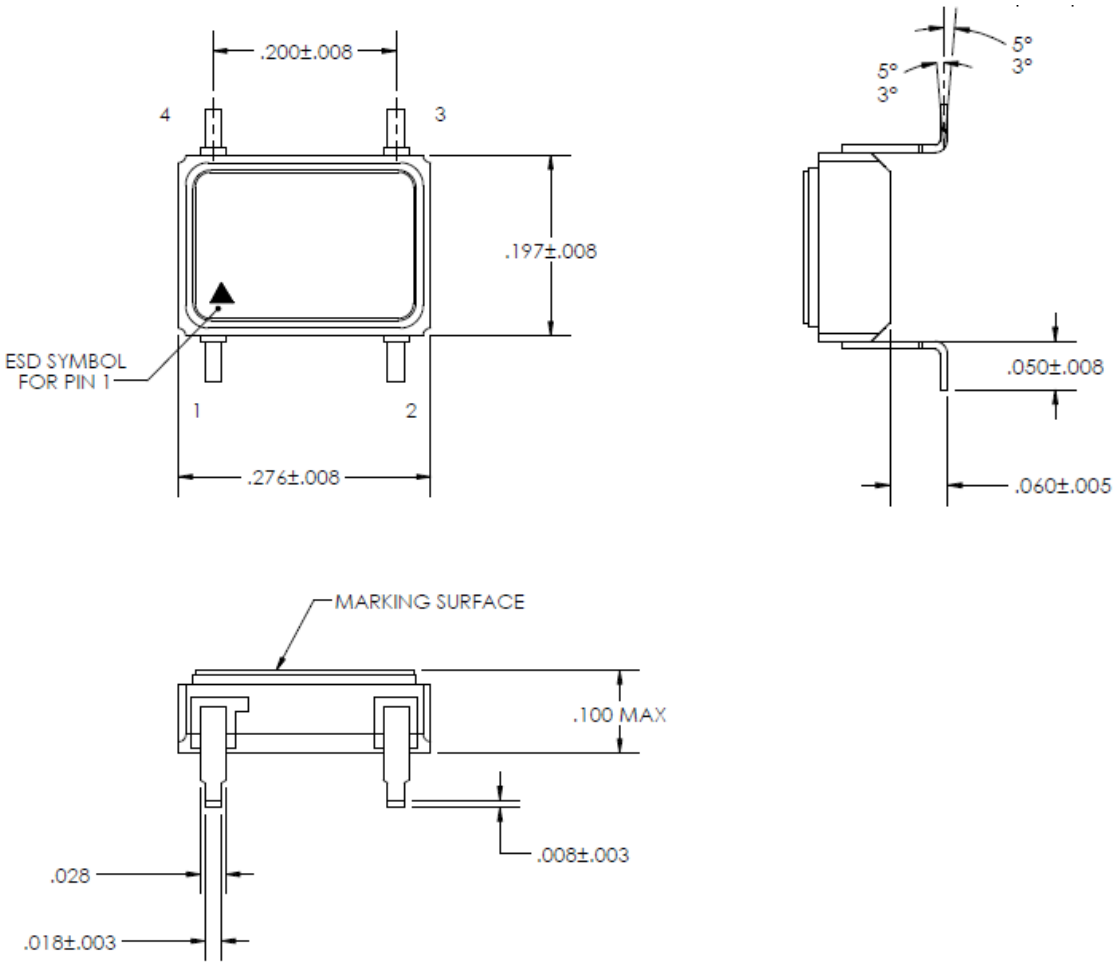
Figure 6-14. Model 1177 Package Outline



Pin	Function
1	Enable/Disable
2	GND/Case
3	Output
4	Vcc

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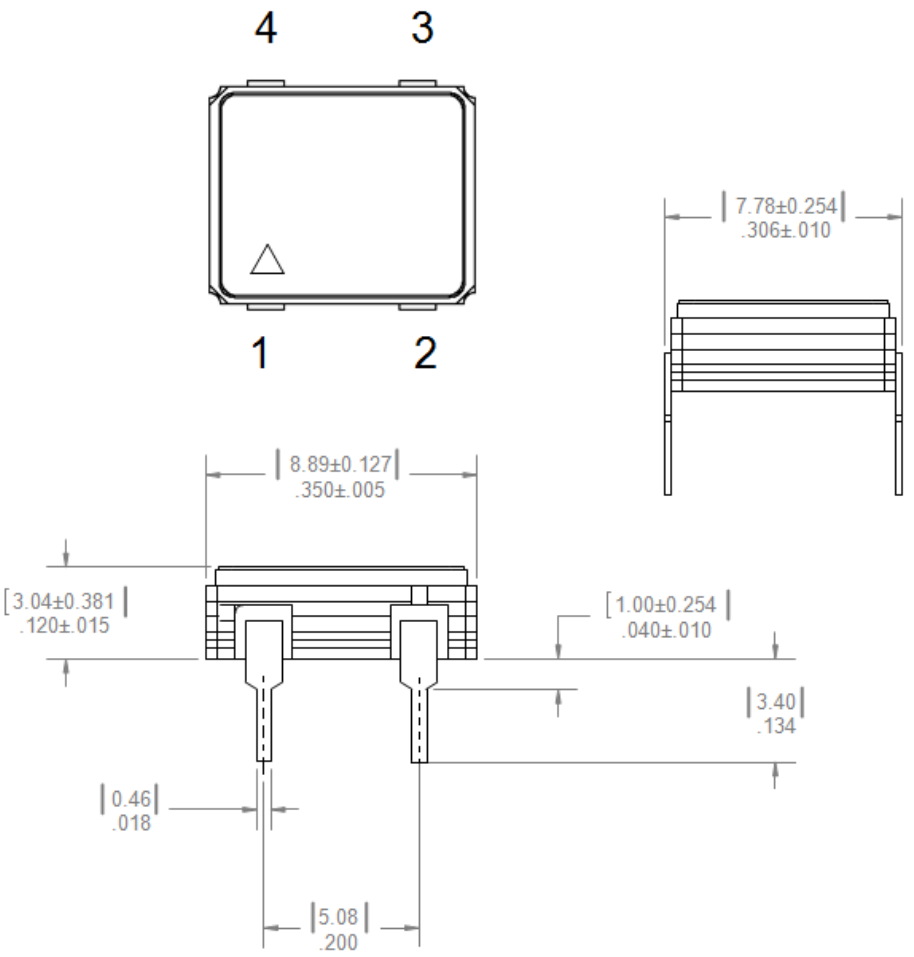
Figure 6-15. Model 1187 Package Outline



Pin	Function
1	Enable/Disable
2	GND/Case
3	Output
4	Vcc

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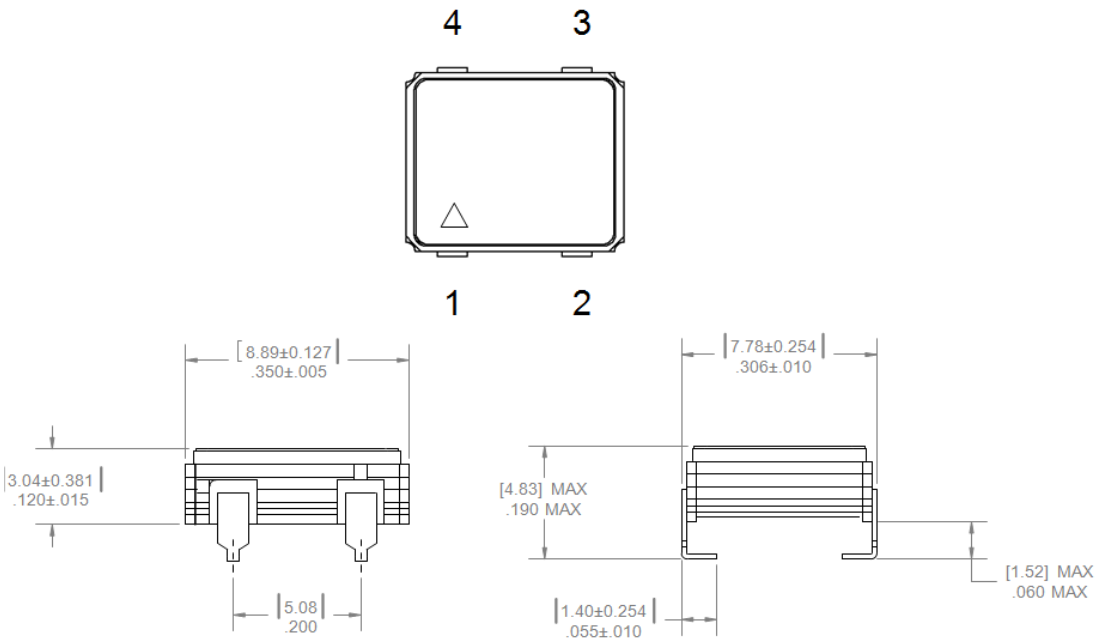
Figure 6-16. Model 1179 Package Outline



Pin	Function
1	Enable/Disable
2	GND
3	Out
4	Vcc

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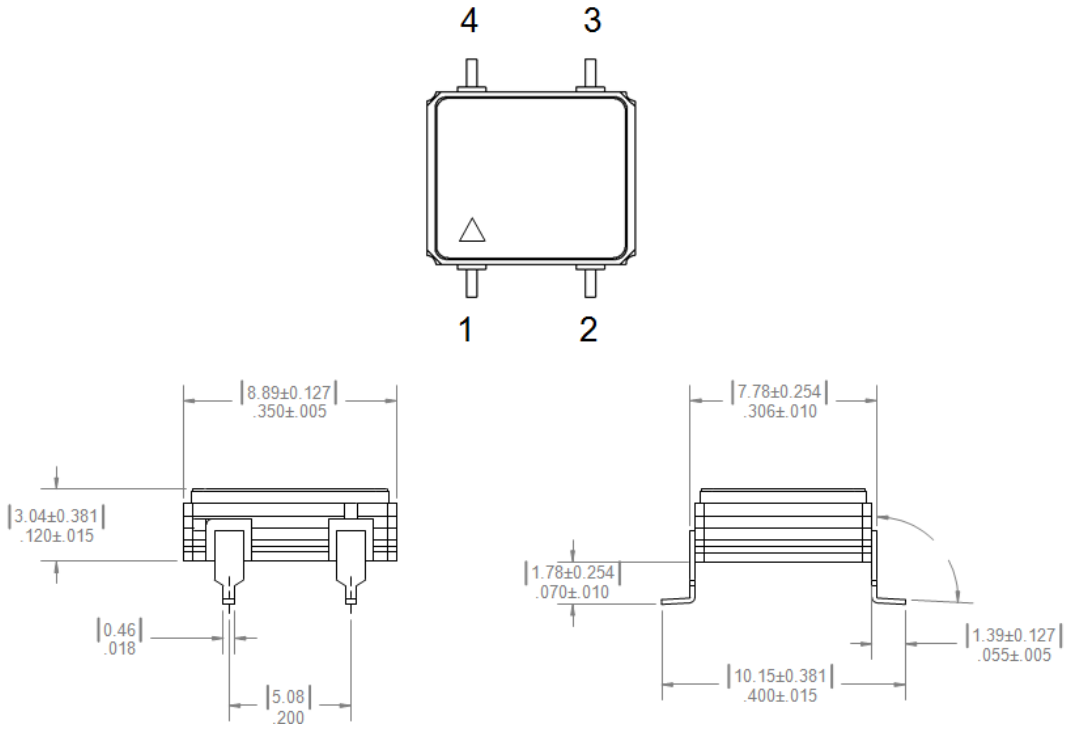
Figure 6-17. Model 1189 Package Outline



Pin	Function
1	Enable/Disable
2	GND
3	Out
4	Vcc

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Figure 6-18. Model 1199 Package Outline

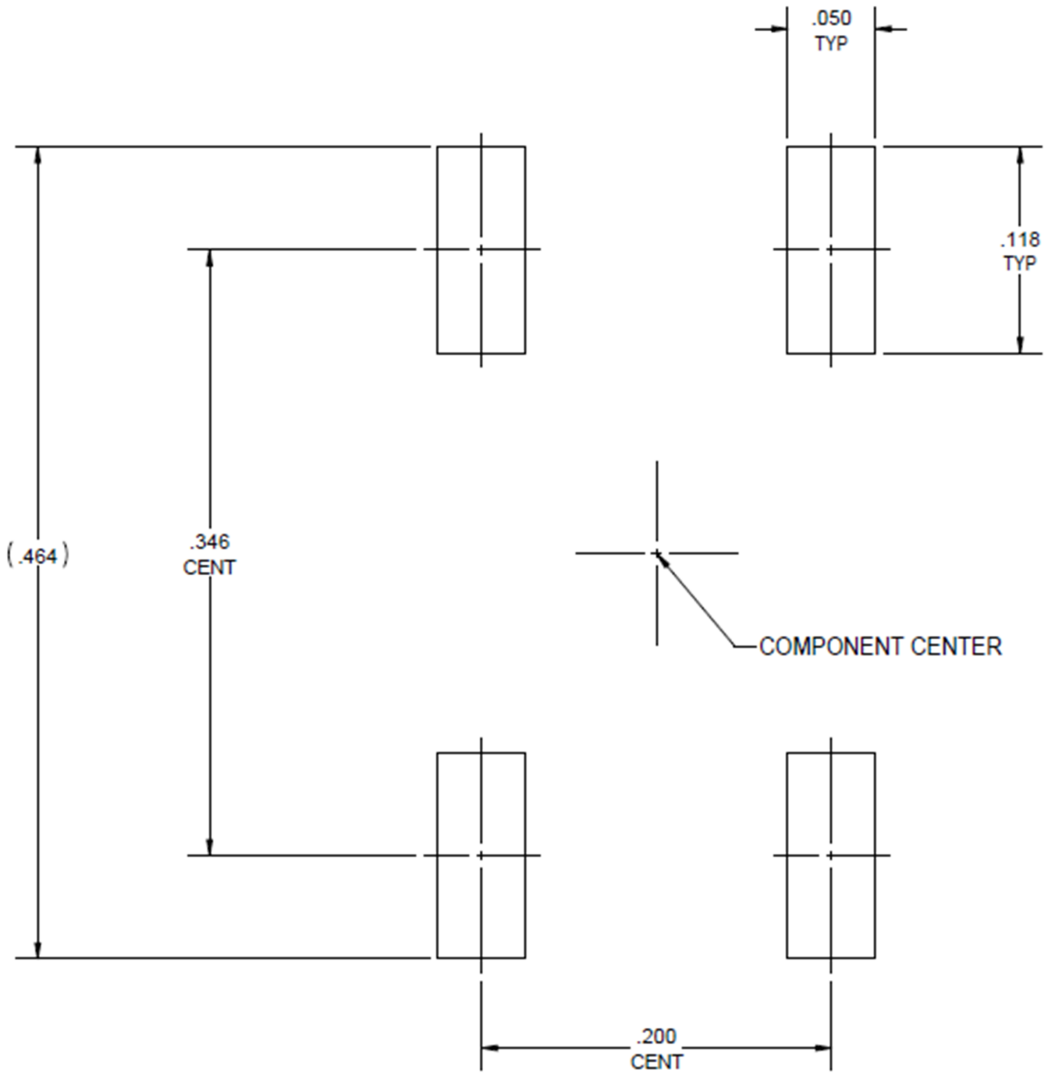


Pin	Function
1	Enable/Disable
2	GND
3	Out
4	Vcc

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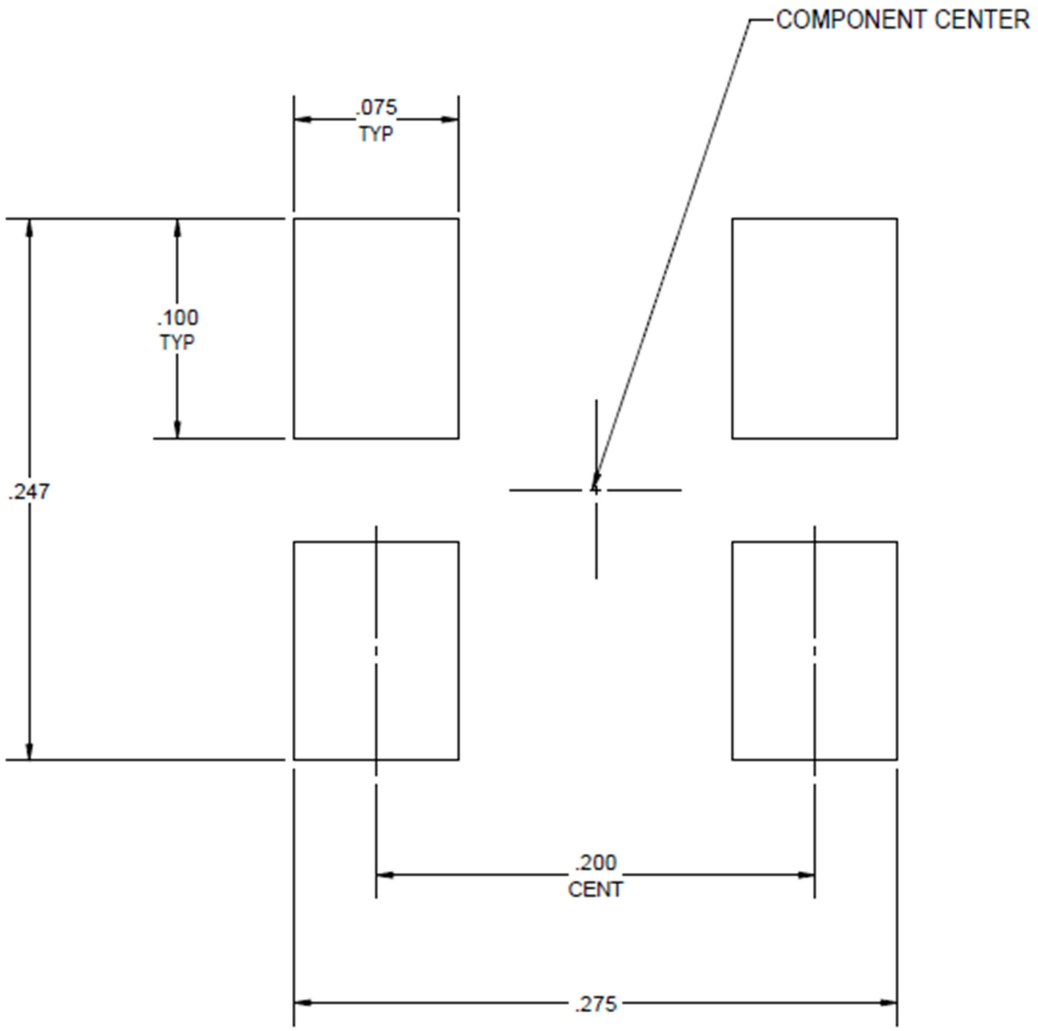
7. Recommended Land Patterns

Figure 7-1. Model 1116/1117



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Figure 7-2. Model 1157



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Figure 7-3. Model 1119

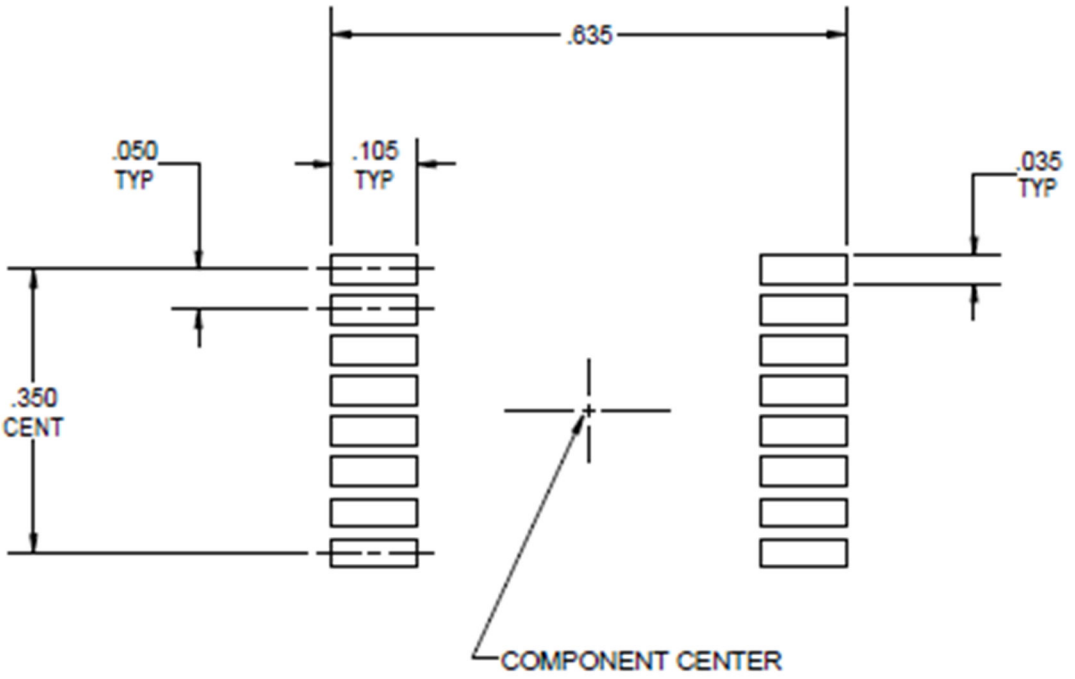
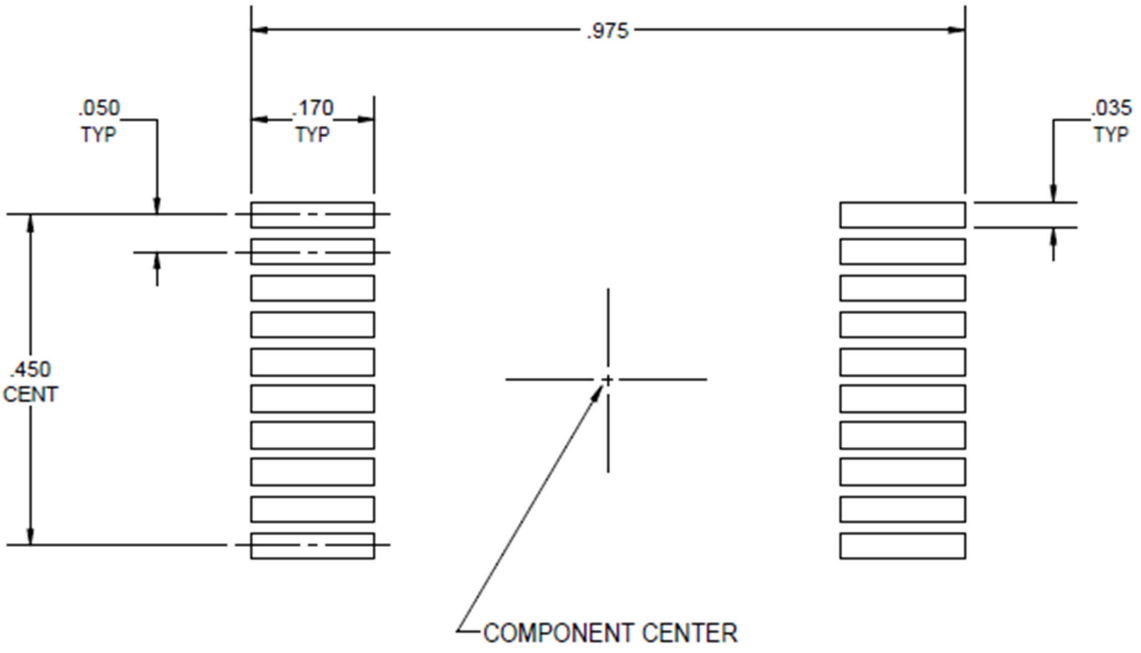


Figure 7-4. Model 1120



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Figure 7-5. Model 1121

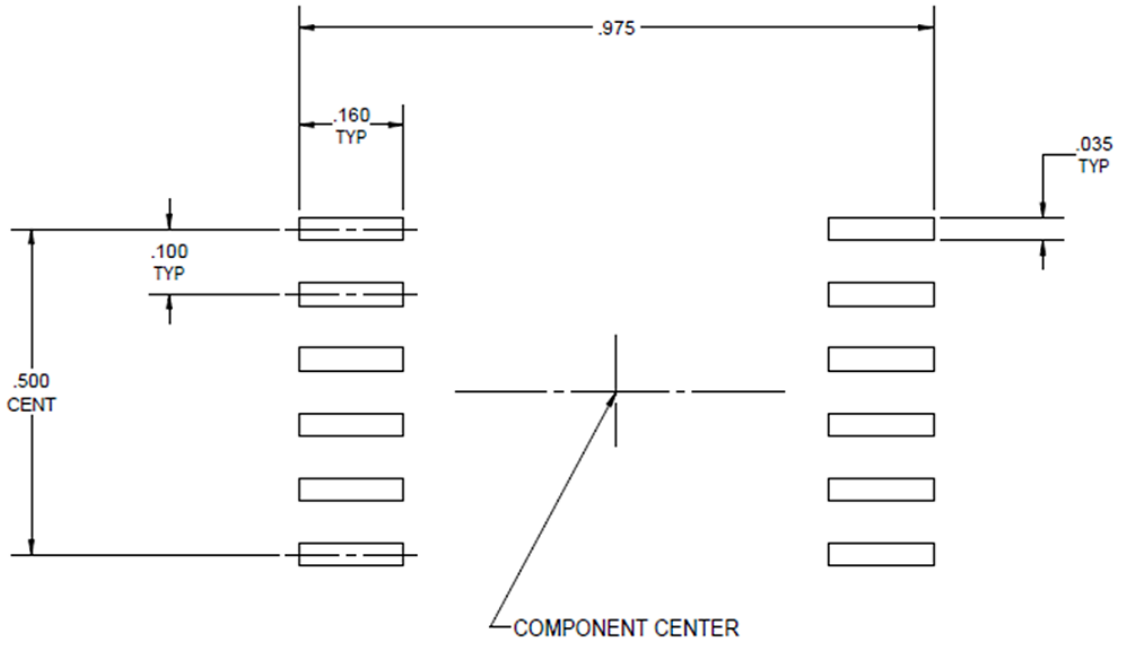
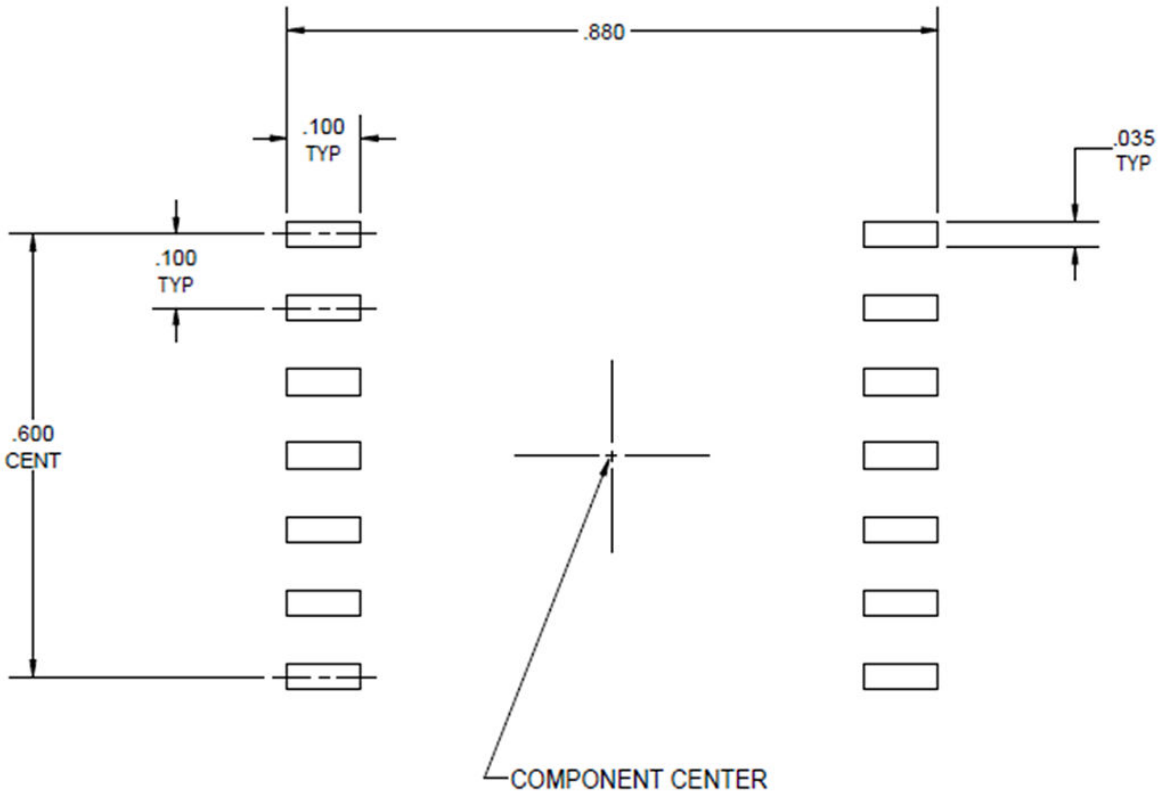


Figure 7-6. Model 1122



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Figure 7-7. Model 1177

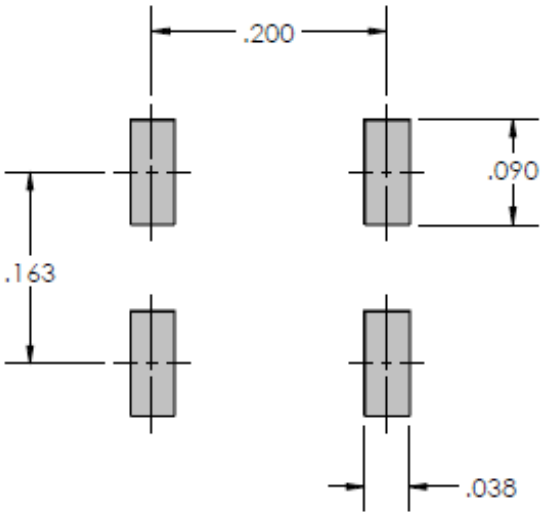
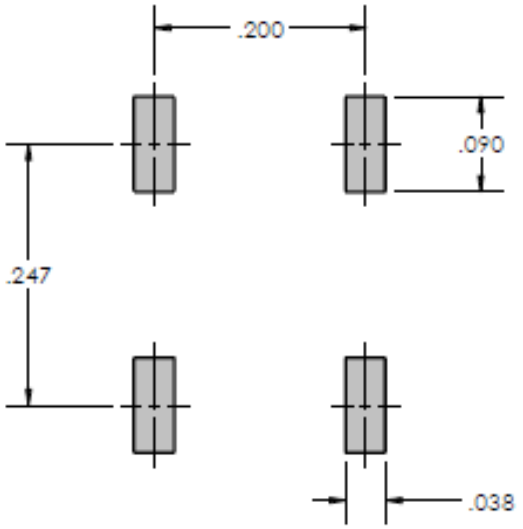


Figure 7-8. Model 1187



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Figure 7-9. Model 1189

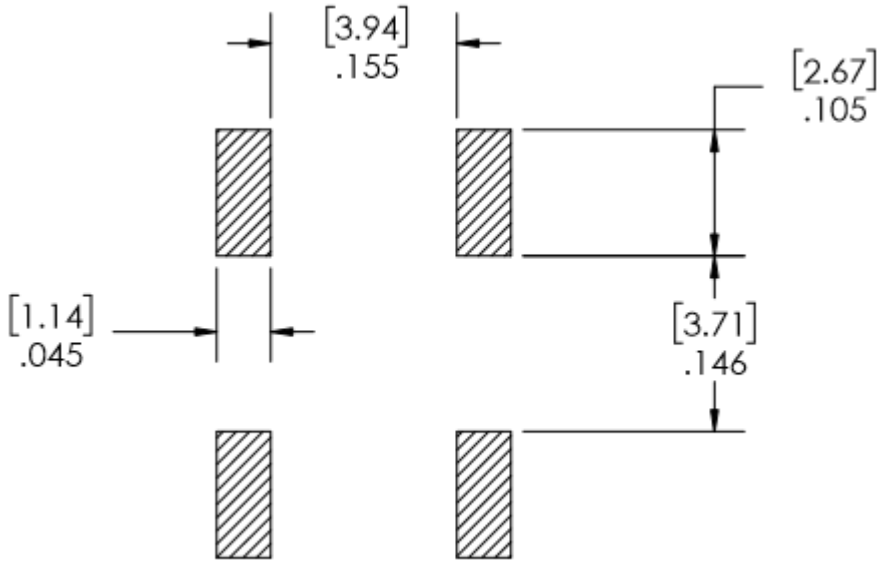
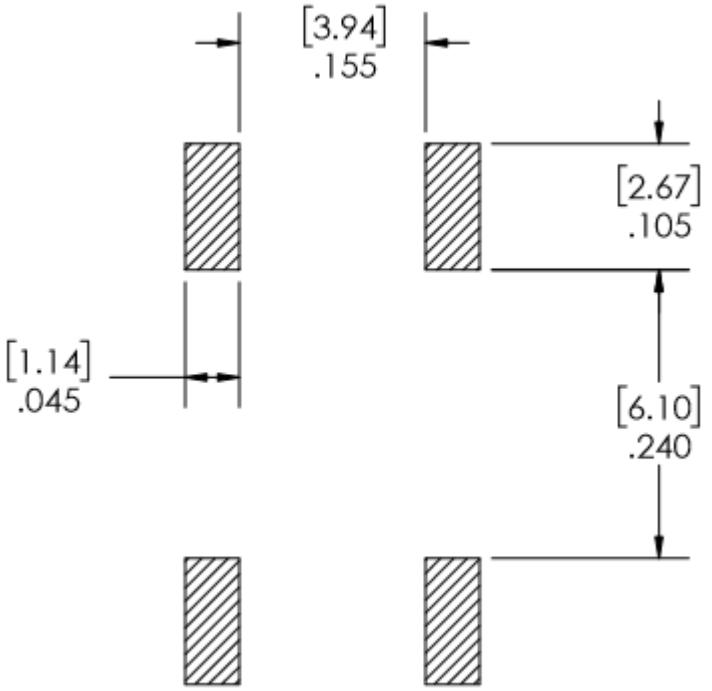


Figure 7-10. Model 1199



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8. Revision History

Revision	Date	Description
C	02/2026	• Minor grammatical changes throughout • Added support email to General • Added MIL-PRF and DOC information to row E and Premium Q to row B of Table 4-2 Design Pedigree • Added cross reference to line b in Section 4.2 Optional Design, Test, and Data Parameters • Removed destruct specimens from line g in Section 4.2 Optional Design, Test, and Data Parameters • Moved Section 4.3.1 Delta Limit Exception to 4.4 • Updated Section 4.5 Deliverable Data line c to include destruct specimens • Reworded Section 6.1.2 Design Pedigree • Added example to Section 6.1.3 Output Frequency • Moved Recommended Land Patterns to Section 7.0 • Incorporated notes into tables throughout
B	10/2025	• Updated Hi-Rel Standard revision to U • Updated temperature formatting throughout • Made minor grammatical changes throughout • Added information to Section 3.1.4 Radiation regarding the SEU LET • Added information to the end of Section 3.1.5 Packages • Updated Section 4.2 Optional Design, Test, and Data Parameters – Added information to line e – Added information to line f – Added information to line g – Added information to line i – Added information to line n • Updated Section 4.2.1 NASA EEE-INST-002 Compliance • Updated the title of Section 4.3.1 to Delta Limit Exception • Added information to line c of Section 4.4 Deliverable Data • Section 5.1 Packaging MIL-STD-1686 for Class 1 devices updated to ANSI/ESD S20.20. • Section 6.1 Ordering Part Number paragraph cleaned up and figure reformatted • Input Voltage moved from Section 6.1.2.1 to Section 6.1.4 • Changed title of Section 6.2 to Electrical Characteristics and Test Parameters • Added Note 5 to Table 6-6 Screening Test Matrix
A	12/2024	Converted Vectron Hi-Rel Standard revision T to Microchip branding with document number DS00005706 revision A. Minor text changes throughout.

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