

Product Overview

MMA121AA is a DC–67GHz, Gallium Arsenide (GaAs) Monolithic Microwave Integrated Circuit (MMIC) Pseudomorphic High–Electron–Mobility Transistor (pHEMT) distributed amplifier. It is ideal for test instrumentation, wide–band A&D, and space applications. The amplifier provides at typical gain of 13 dB across the operating frequency range and P1dB in the upper frequency bands ranging from 20 dBm at 40 GHz to 15 dBm at 67 GHz with a nominal bias condition of 200 mA from a 7V supply. Noise figure is typically 4 dB. The die has an on-chip bias network allowing for smooth operation from 1 GHz to 67 GHz. For operation below 1 GHz, an external choke network should be used. The MMA121AA amplifier is DC coupled, and features RF I/Os that are internally matched to 50Ω.

Key Features

- Frequency range: DC to 67 GHz
- Gain: 13 dB
- P1dBm > 20 dBm at 40 GHz, P1dBm > 17 dBm at 50 GHz, P1dBm > 15 dBm at 60 GHz,
- Supply: 7V at 200 mA
- Integrated on–chip bias
- Die input power handling up to 20 dBm (CW)
- 50Ω matched input/output
- Die size: 1.65 mm × 1.2 mm × 0.1 mm

Applications

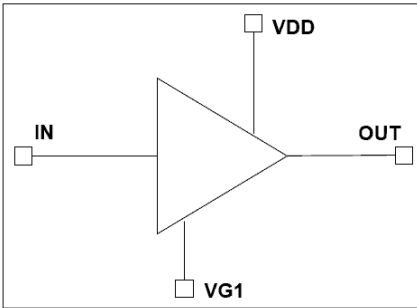
- Test and measurement instrumentation
- Electronic warfare (EW), electronic countermeasures (ECM), and electronic counter-countermeasures (ECCM)
- Military, A&D, space, SATCOM
- Telecom infrastructure, wideband microwave radios
- Microwave and millimeter-wave communications systems

Performance Overview

Parameter	Typ.	Units
Operational frequency Range	DC–67	GHz
Gain	13	dB
Noise figure	4	dB
P1dB at 50 GHz	17	dBm
Psat at 50 GHz	20	dBm
IM3 at 50 GHz and 10 dBm	–33	dBc
Current at +7V Supply	200	mA

Export Classification: 3A001.b.2.d

Functional Block Diagram



Performance Curves

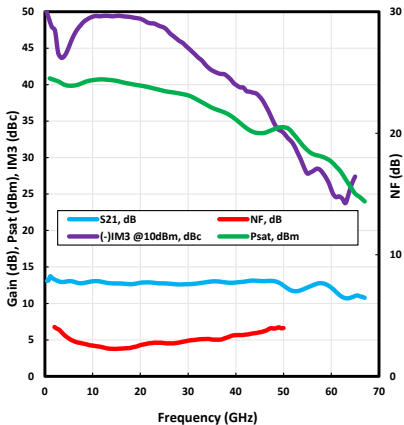


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1. Electrical Specifications

1.1 Typical Electrical Performance

Table 1-1. Typical Electrical Performance at 25 °C, $V_{DD} = 7V$, $I_{DD} = 200\text{ mA}$ (Unless otherwise mentioned).

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		DC		67	GHz
Gain	DC – 20 GHz	12	13		dB
	20 GHz – 40 GHz	12	13		
	40 GHz – 67 GHz	12	13		
Gain flatness	DC – 20 GHz		±1		dB
	20 GHz – 40 GHz		±1		
	40 GHz – 67 GHz		±1		
Noise figure	DC – 20 GHz		4	7	dB
	20 GHz – 40 GHz		5	6	
	40 GHz – 67 GHz				
Input return loss	DC – 20 GHz	13	15		dB
	20 GHz – 40 GHz	13	15		
	40 GHz – 67 GHz	8	12		
Output return loss	DC – 20 GHz	11	15		dB
	20 GHz – 40 GHz	10	13		
	40 GHz – 67 GHz	9	12		
P1dB	DC – 20 GHz	20	22		dBm
	20 GHz – 40 GHz	18	20		
	40 GHz – 67 GHz	11	17		
Psat	DC – 20 GHz	22	24		dBm
	20 GHz – 40 GHz	19	22		
	40 GHz – 67 GHz	14	17		
OIP3	DC – 20 GHz	31	34		dBm
	20 GHz – 40 GHz	29	32		
	40 GHz – 67 GHz	20	26		
V_{DD} (drain voltage supply)			7		V
I_{DD} (drain current)			200		mA

1.2 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the MMA121AA at 25 °C, unless otherwise specified. Exceeding any of the maximum ratings could cause damage and/or latent defects to the device.

Table 1-2. Absolute Maximum Ratings

Parameters	Rating
Drain bias voltage (V_{DD})	8V
Gate bias voltage (V_G)	-2V to 0.5V
RF input power (P_{in})	20 dBm (CW)
Channel temperature	165 °C
Drain bias current (I_{DD})	300 mA
DC power dissipation ($T = 85$ °C)	1.7W
Thermal resistance	47 °C/W
Storage temperature	-65 °C to 150 °C



ESD Sensitive Device

1.3 Typical Performance Curves

1.3.1 Typical Performances vs. Temperature

The graphs shown in this section represent the typical performance versus temperature curves of the MMA121AA under specific bias conditions. All measurements were taken using the test circuit shown in [Figure 3-2](#).

Figure 1-1. Gain vs. Temperature at 6V/150 mA

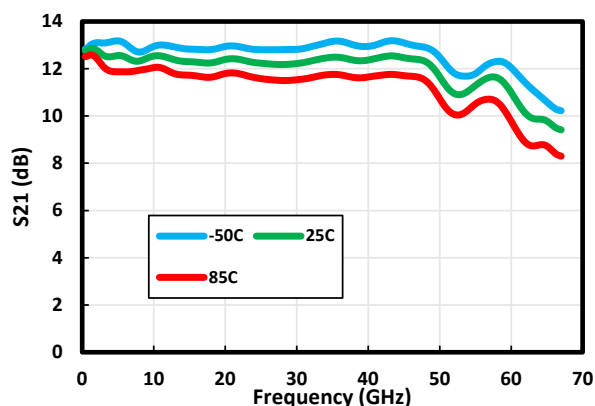


Figure 1-2. Gain vs. Temperature at 7V/200 mA

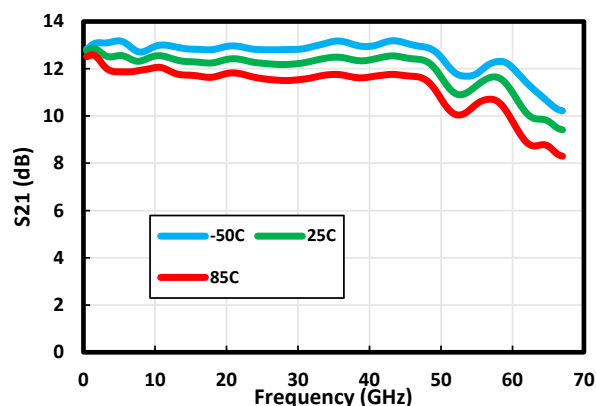


Figure 1-3. Gain vs. Temperature at 7.5V/250 mA

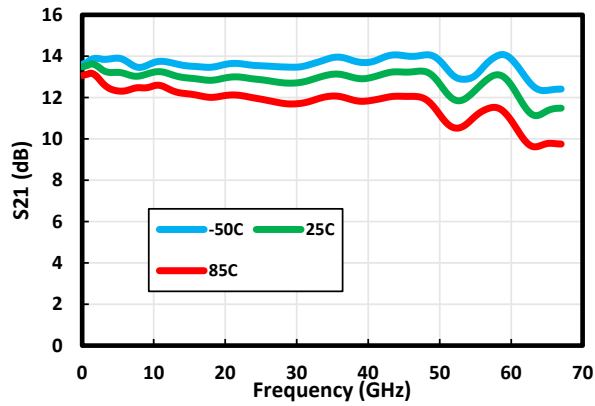


Figure 1-4. Gain vs. Temperature at 8V/300 mA

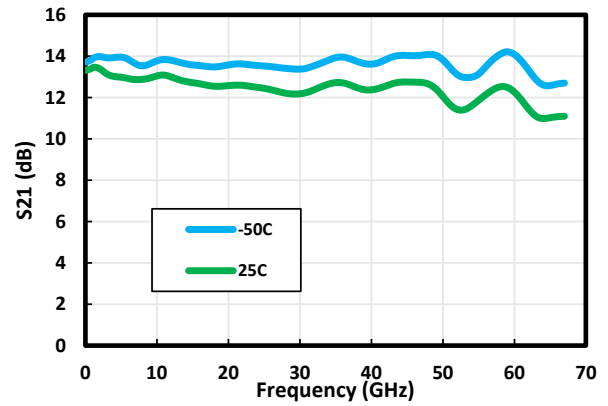


Figure 1-5. S11 vs. Temperature at 6V/150mA

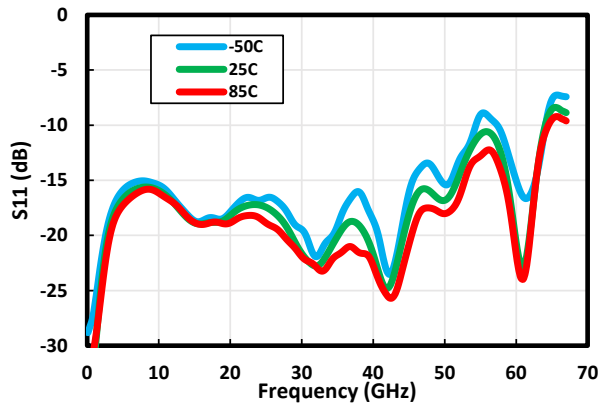


Figure 1-6. S11 vs. Temperature at 7V/200 mA

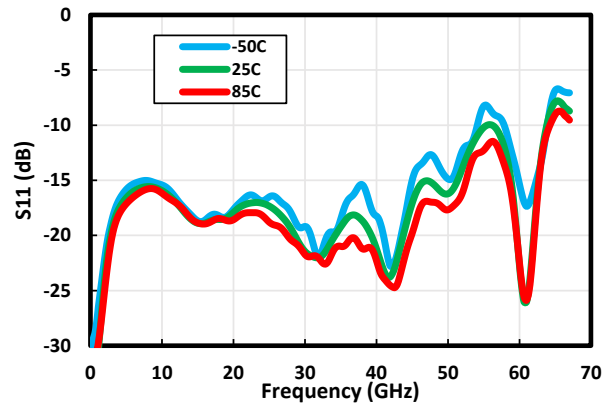


Figure 1-7. S11 vs. Temperature at 7.5V/250 mA

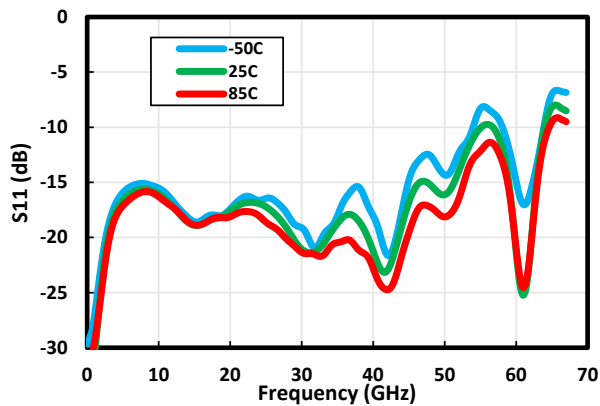


Figure 1-8. S11 vs. Temperature at 8V/300 mA

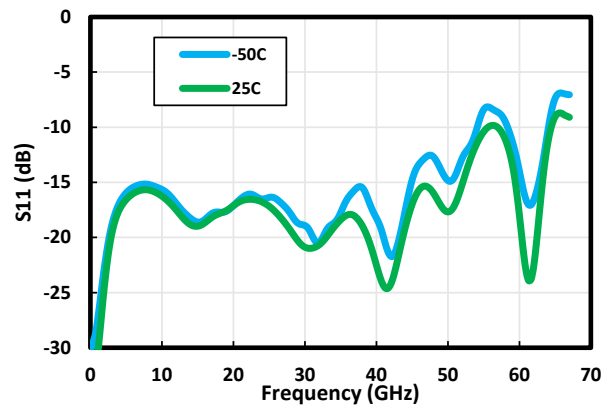


Figure 1-9. S22 vs. Temperature at 6V/150 mA

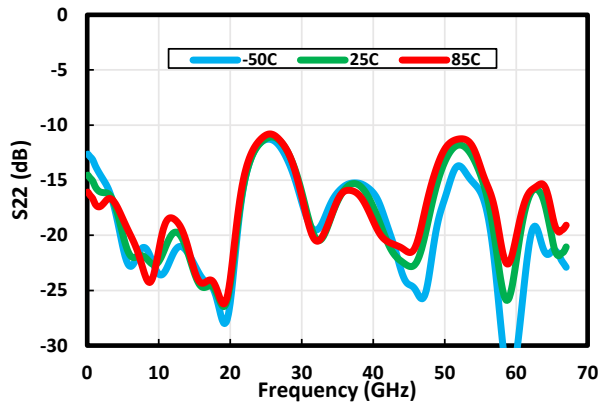


Figure 1-10. S22 vs. Temperature at 7V/200 mA

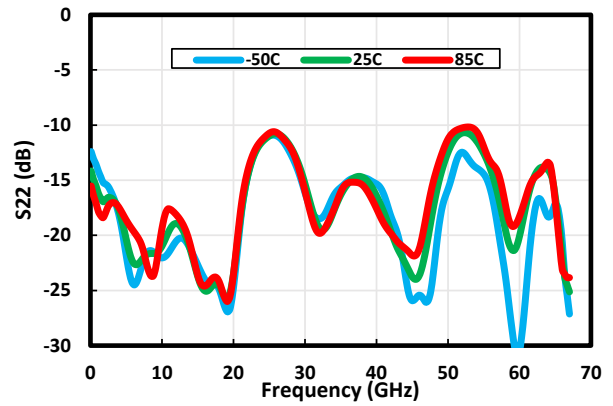


Figure 1-11. S22 vs. Temperature at 7.5V/250 mA

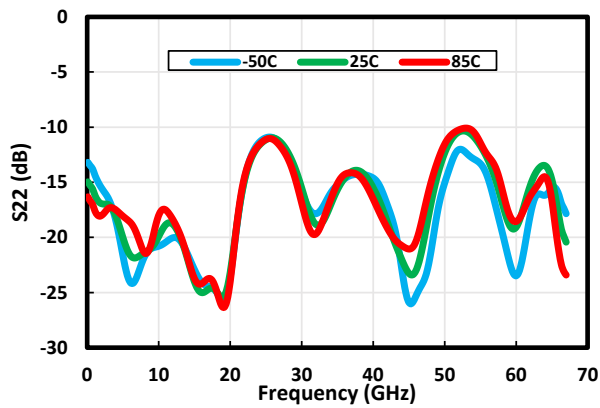


Figure 1-12. S12 vs. Temperature at 6V/150 mA

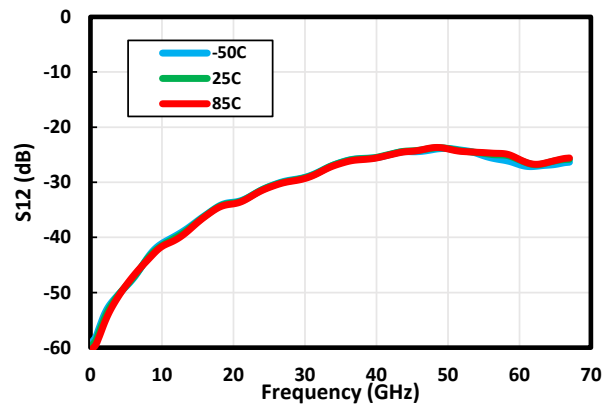


Figure 1-13. S12 vs. Temperature at 7V/200 mA

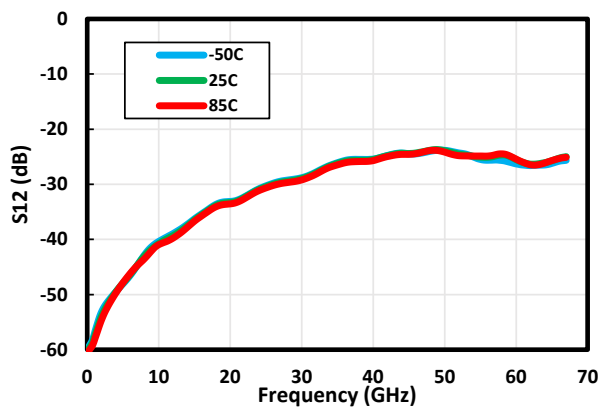


Figure 1-14. S12 vs. Temperature at 7.5V/250 mA

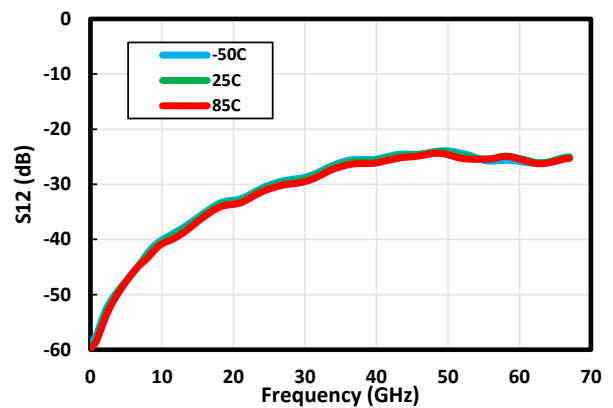


Figure 1-15. NF vs. Temperature at 6V/150 mA

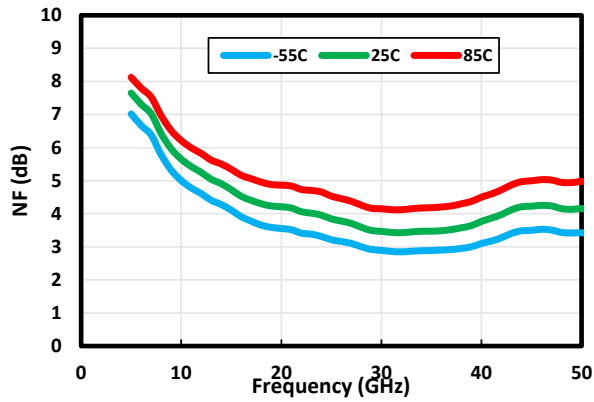


Figure 1-16. NF vs. Temperature at 7V/200 mA

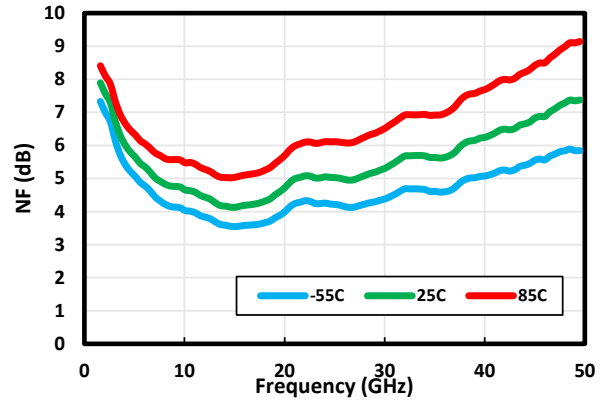


Figure 1-17. NF vs. Temperature at 7.5V/250 mA

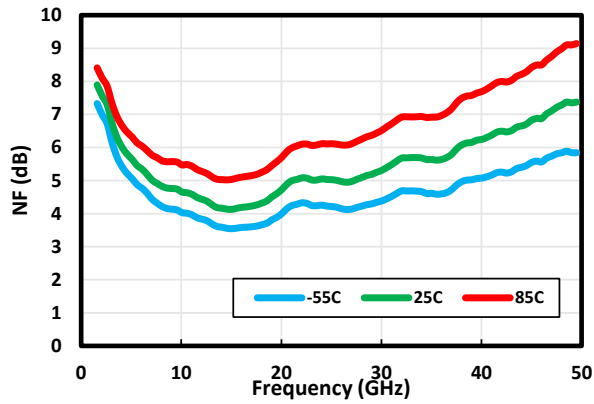


Figure 1-18. P1dB vs. Temperature at 6V/150 mA

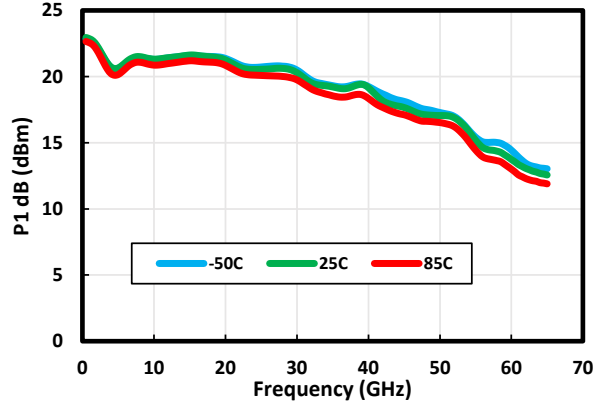


Figure 1-19. P1dB vs. Temperature at 7V/200 mA

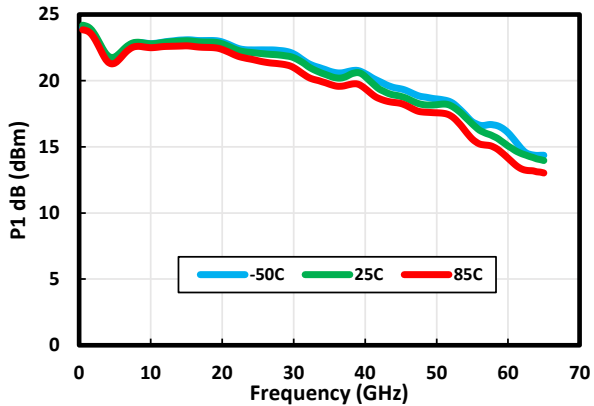


Figure 1-20. P1dB vs. Temperature at 7.5V/250 mA

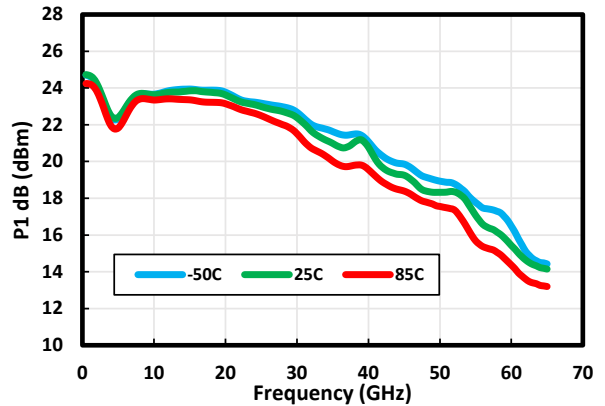


Figure 1-21. Psat vs. Temperature at 6V/150 mA

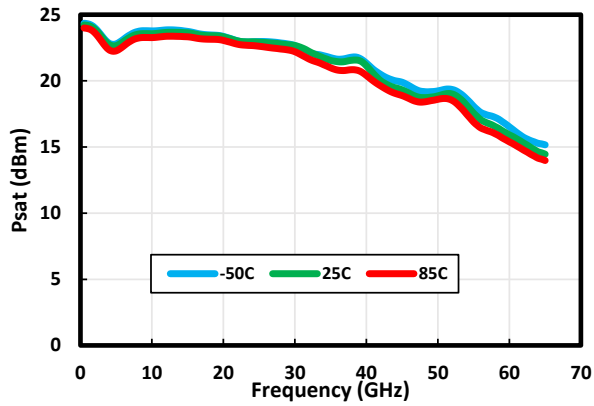


Figure 1-22. Psat vs. Temperature at 7V/200 mA

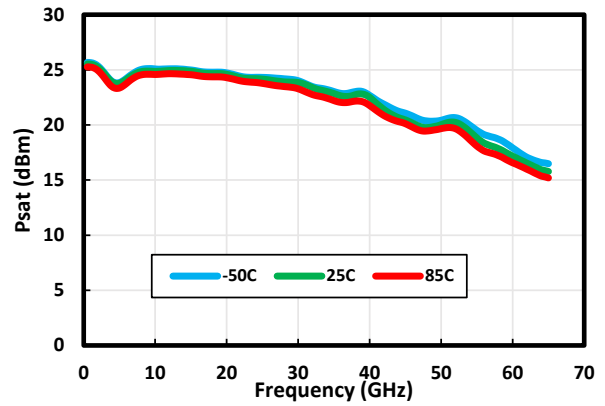


Figure 1-23. Psat vs. Temperature at 7.5V/250 mA

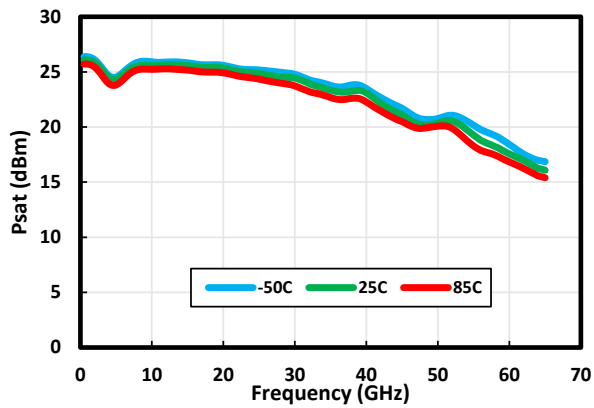


Figure 1-24. IM2 (low) vs. Temperature at 6V/150 mA
at 10 dBm per tone

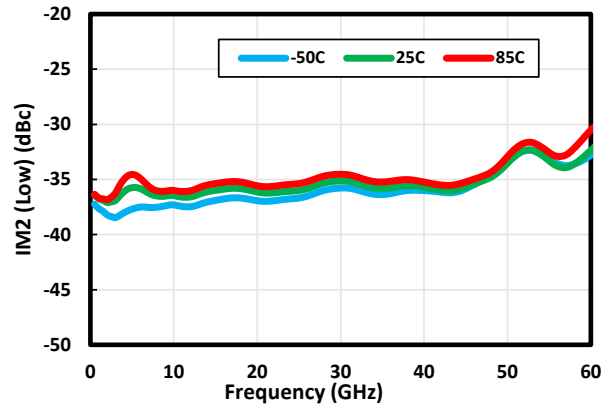


Figure 1-25. IM2 (low) vs. Temperature at 7V/200 mA
at 10 dBm per tone

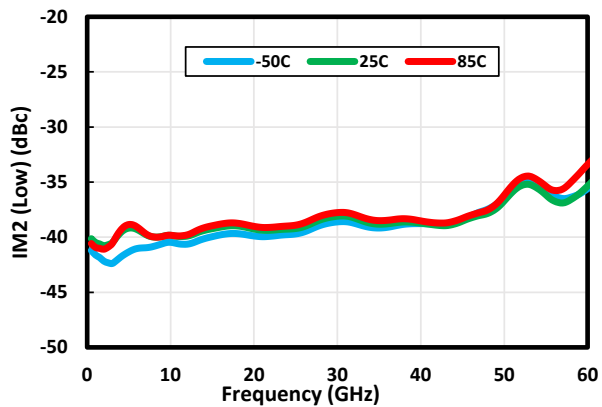


Figure 1-26. IM2 (low) vs. Temperature at 8V/300 mA
at 10 dBm per tone

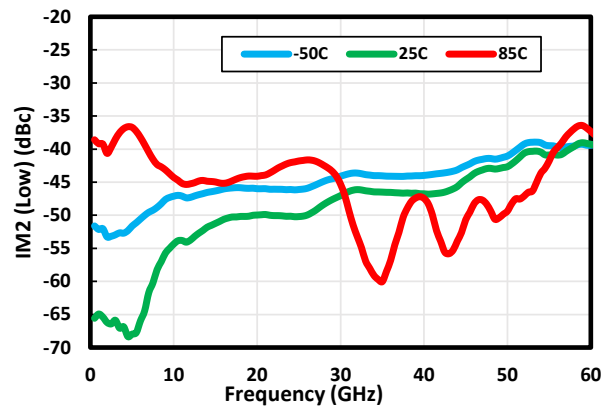


Figure 1-27. IM3 vs. Temperature at 6V/150 mA
10 dBm (per tone)

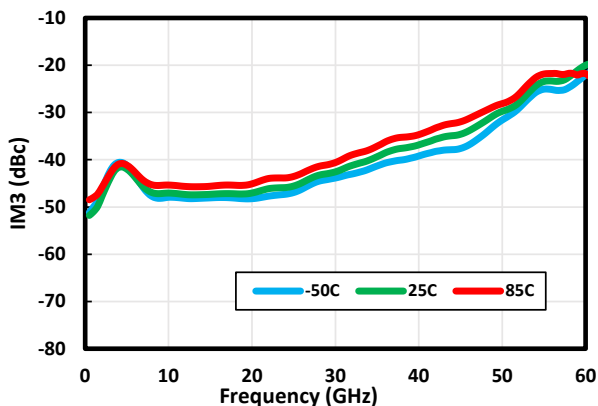


Figure 1-28. IM3 vs. Temperature at 7V/200 mA
10 dBm (per tone)

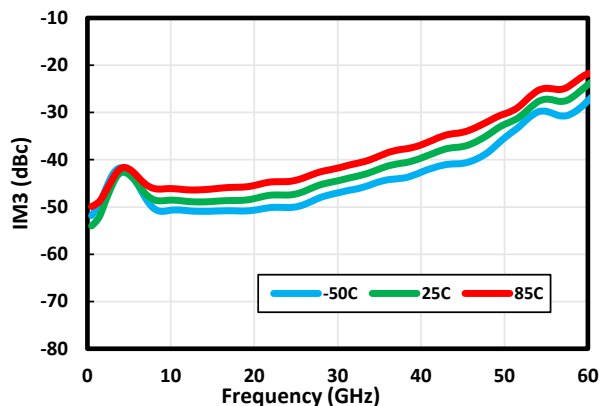
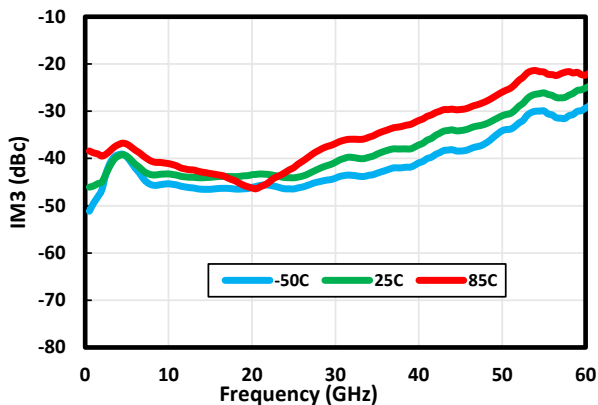


Figure 1-29. IM3 vs. Temperature at 8V/300 mA
10 dBm (per tone)



1.3.2 Typical Performances vs. Bias

The graphs shown in this section represent the typical performance versus bias curves of the MMA121AA under constant temperature of 25 °C. All measurements were taken using the test circuit shown in [Figure 3-2](#).

Figure 1-30. Gain vs. V_{DD} at 150 mA

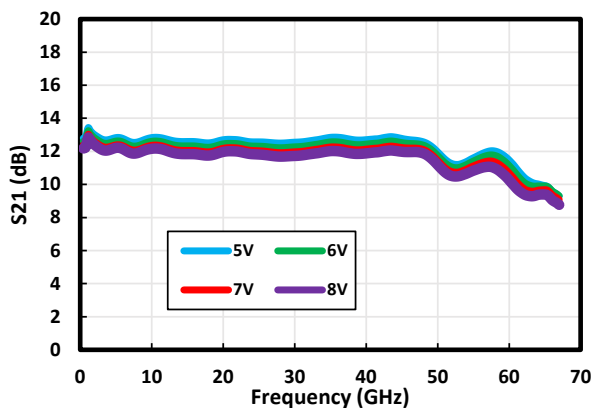


Figure 1-31. Gain vs. V_{DD} at 200 mA

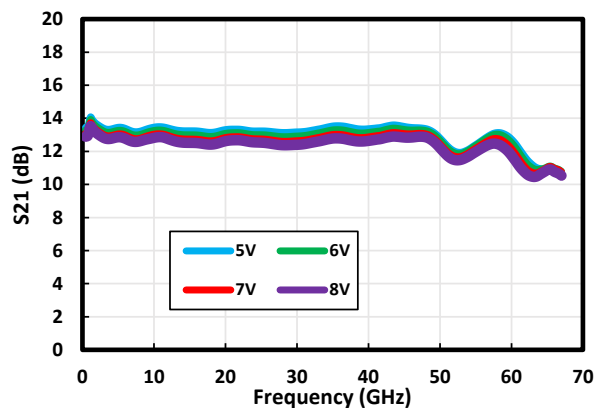


Figure 1-32. Gain vs. V_{DD} at 250 mA

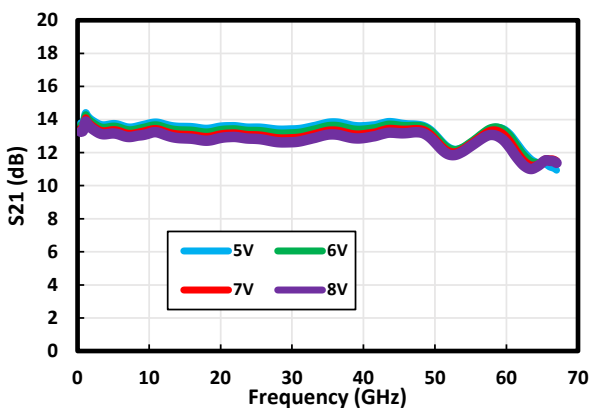


Figure 1-33. Gain vs. V_{DD} at 300 mA

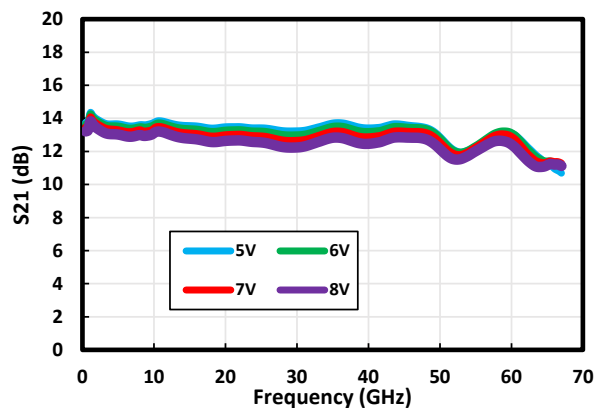


Figure 1-34. NF vs. V_{DD} at 150 mA

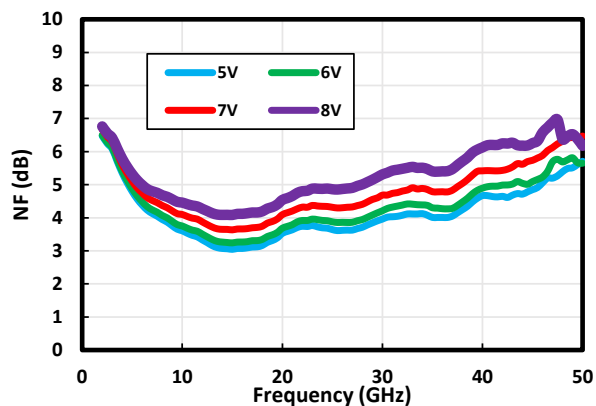


Figure 1-35. NF vs. V_{DD} at 200 mA

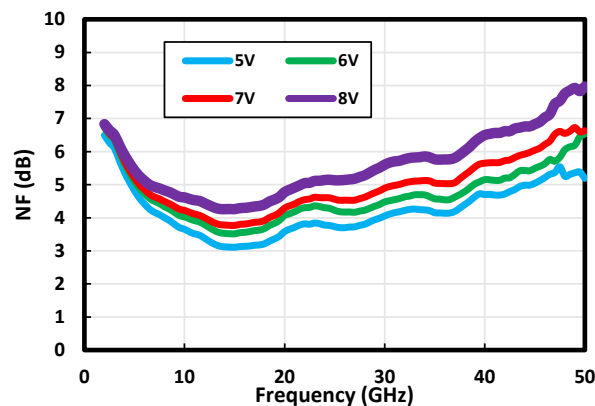


Figure 1-36. NF vs. V_{DD} at 250 mA

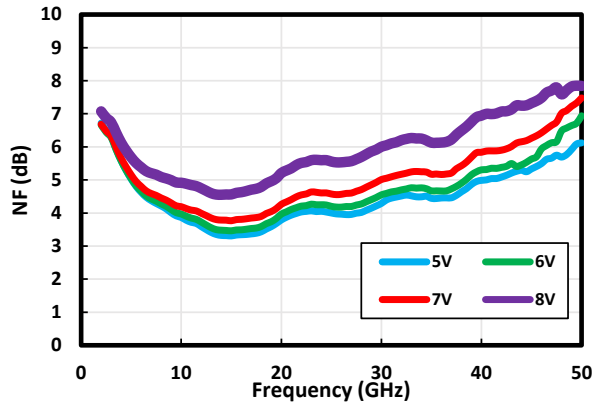


Figure 1-37. NF vs. V_{DD} at 300 mA

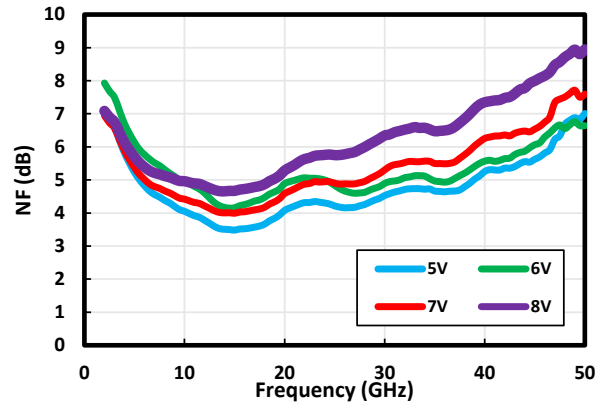


Figure 1-38. P1dB vs. Bias

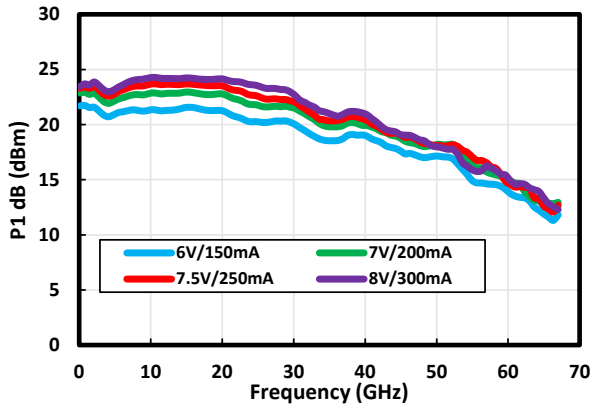


Figure 1-39. P_{sat} vs. Bias

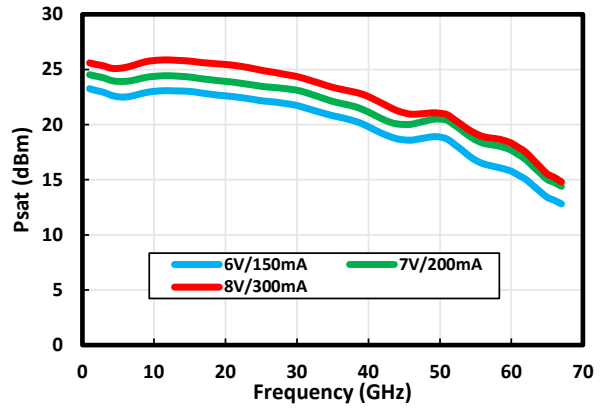


Figure 1-40. OIP3 vs. Bias

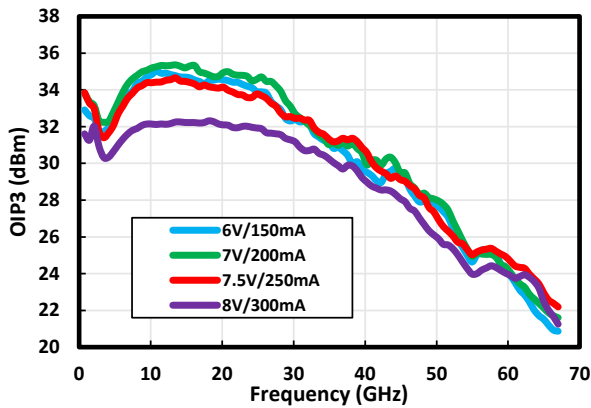


Figure 1-41. IM3 vs. Bias at 10 dBm per tone

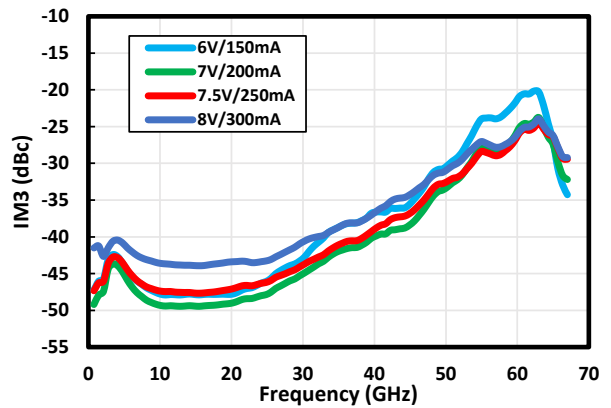
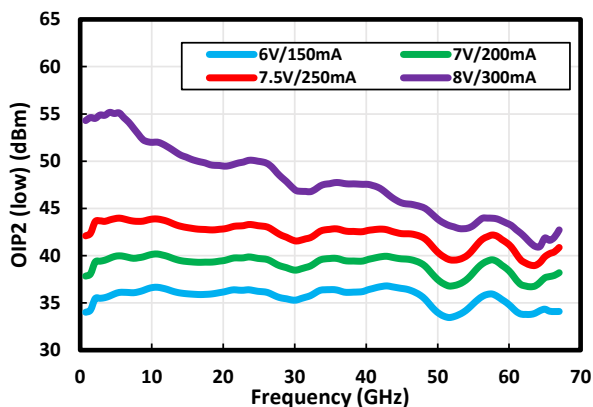


Figure 1-42. OIP2 (Low at $\Delta = 10$ MHz) vs. Bias



1.3.3 Typical Performances vs. Output Power

The graphs shown in this section represent the typical performance versus output power curves of the MMA121AA under constant temperature of 25 °C. All measurements were taken using the test circuit shown in Figure 3-2.

Figure 1-43. IM2 vs. Power at 6V/150 mA

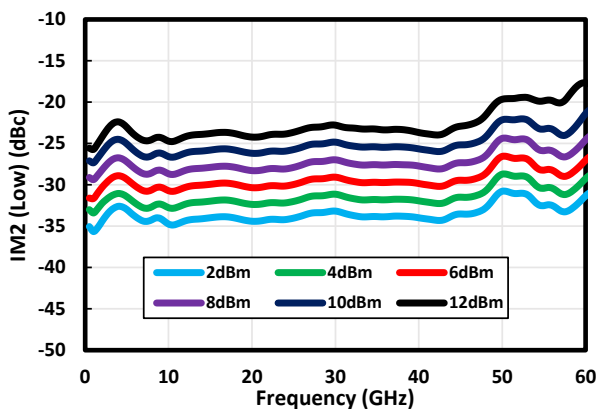


Figure 1-44. IM2 vs. Power at 7V/200 mA

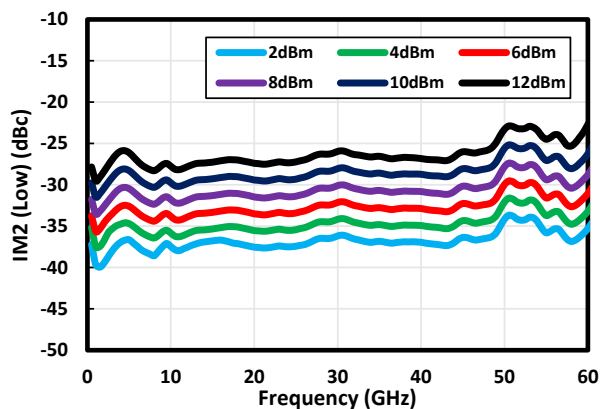


Figure 1-45. IM2 vs. Power at 7.5V/250 mA

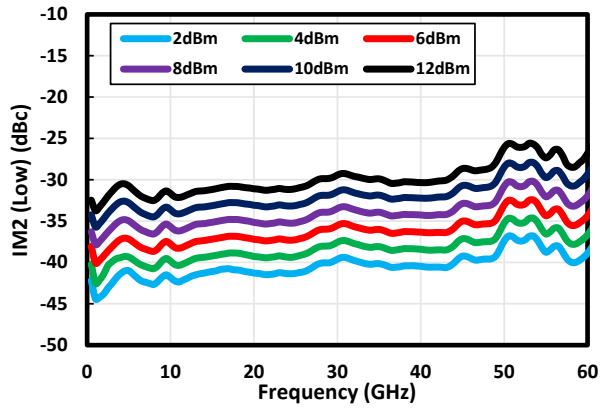


Figure 1-46. IM2 vs. Power at 8V/300 mA

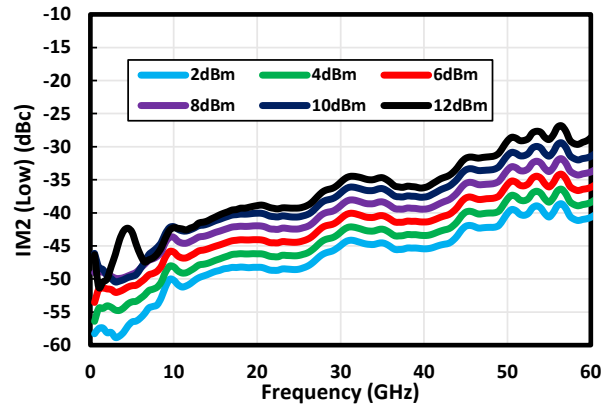


Figure 1-47. IM3 vs. Power at 6V/150 mA

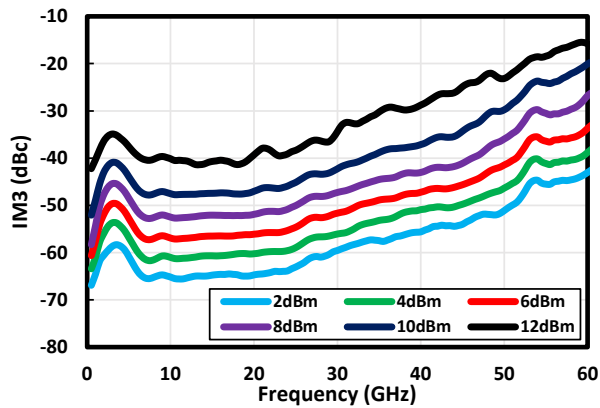


Figure 1-48. IM3 vs. Power at 7V/200 mA

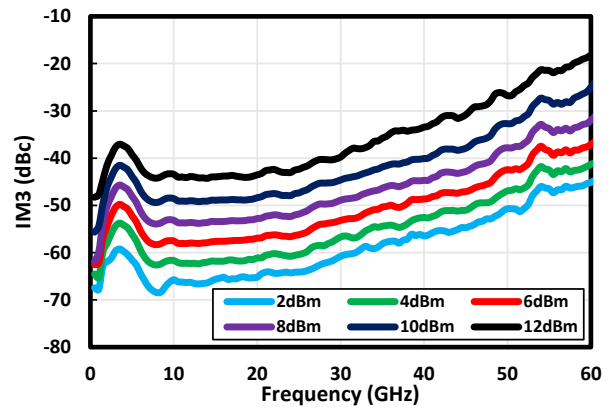


Figure 1-49. IM3 vs. Power at 7.5V/250 mA

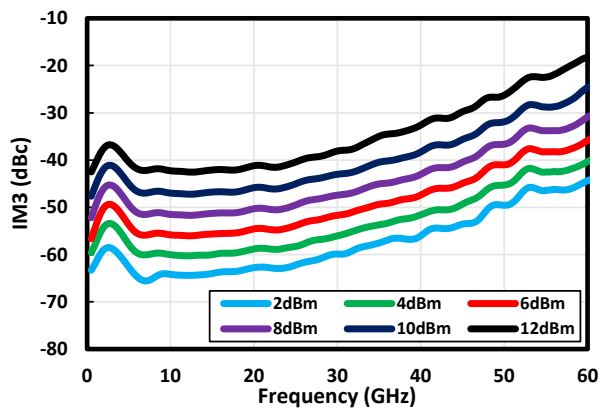


Figure 1-50. IM3 vs. Power at 8V/250 mA

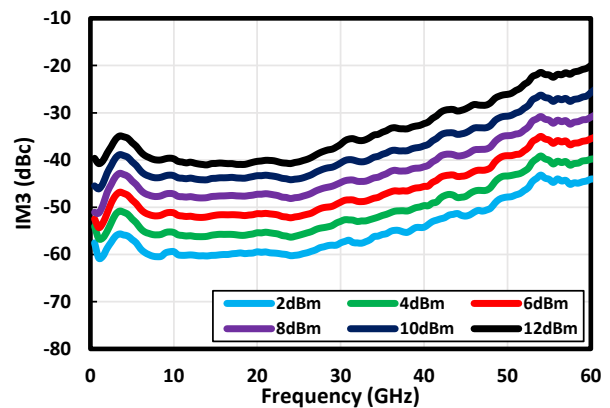


Figure 1-51. 2nd Harmonic vs. Power at 6V/150 mA

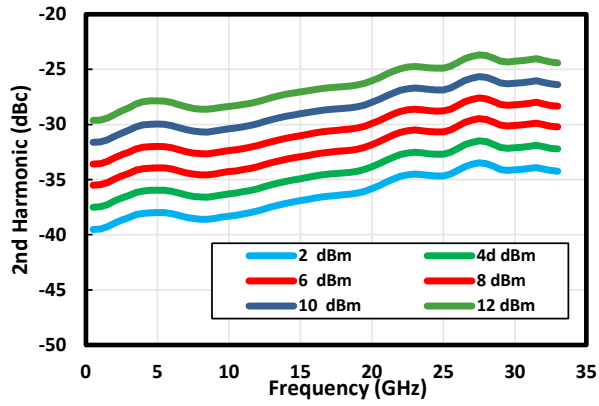


Figure 1-52. 2nd Harmonic vs. Power at 7V/200 mA

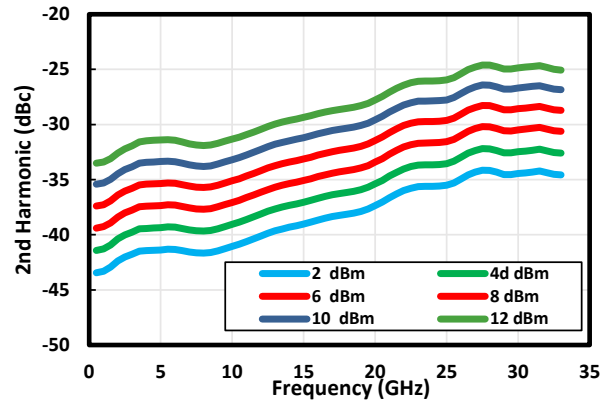
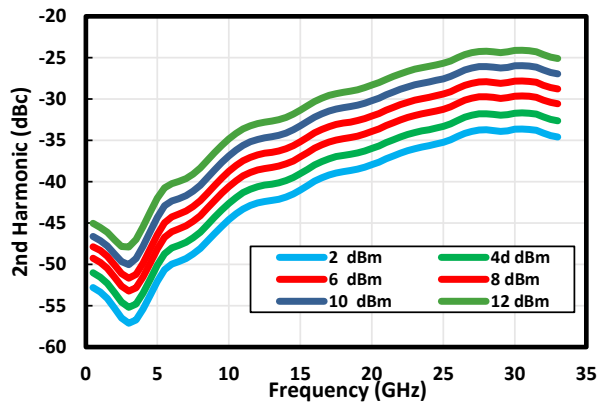


Figure 1-53. 2nd Harmonic vs. Power at 8V/300 mA



2. Die Specifications

The following illustration shows the chip outline of the MMA121AA device. Dimensions are in millimeters and are relative to the zero datum locations shown in the drawing. Nominal Die dimensions are 1.65 mm × 1.2 mm × 0.1 mm. The minimum bond pad size is 0.1 mm × 0.1 mm. Both the bond pad surface and the backside metal have 3 μm thick gold. The die thickness is 0.1 mm. The backside is the DC/RF ground. The polygon region labeled “DO NOT TOUCH” are areas containing delicate airbridge areas on the die that should be avoided.

Figure 2-1. Die Outline Drawing (μm)

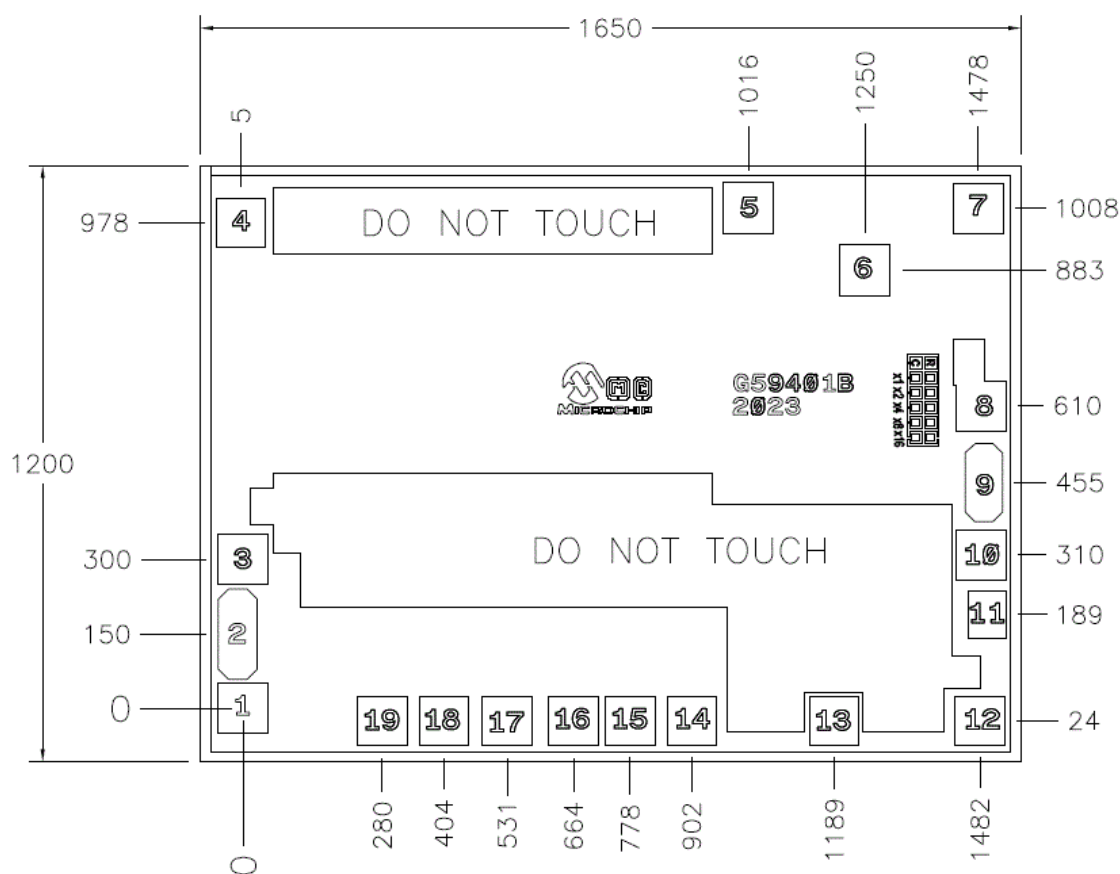


Table 2-1. I/O Description

Pad Number	Pad Name	Pad Description (Effective Pad Size in μm)
2	RF _{IN}	This pad RF/DC coupled to the FET gates and matched to 50 Ω (73 $\times$ 178).
9	RF _{OUT}	This pad is RF/DC coupled to the FET drains and matched to 50 Ω (70 $\times$ 152).
4, 5	V _{DDB} , V _{DDA}	V _{DDA} , V _{DDB} low-frequency termination for drain ballast, DC coupled to the FET drains (96 $\times$ 96).
6	V _{DD}	V _{DD} bias pad (96 $\times$ 96)
11	V _{G2}	Access to Gate 2 bias (70 $\times$ 90)
12, 14	V _{G1A} , V _{G1}	First gate low-frequency terminations DC coupled to the Gate 1 and used to set the die bias current (96 $\times$ 96)
15, 16, 17, 18, 19	V _{G1B} , V _{G1C} , V _{G1D} , V _{G1E} , V _{G1F}	Complimentary low-frequency terminations for the Gate 1, used to control low-frequency response slope (96 $\times$ 96)
1, 3, 7, 8, 10, 13	Ground	Ground connections used for die test purposes; DC/RF ground is using die backside metal (96 $\times$ 96)

3. Application Circuit

Figure 3-1. Application Circuit: Schematic

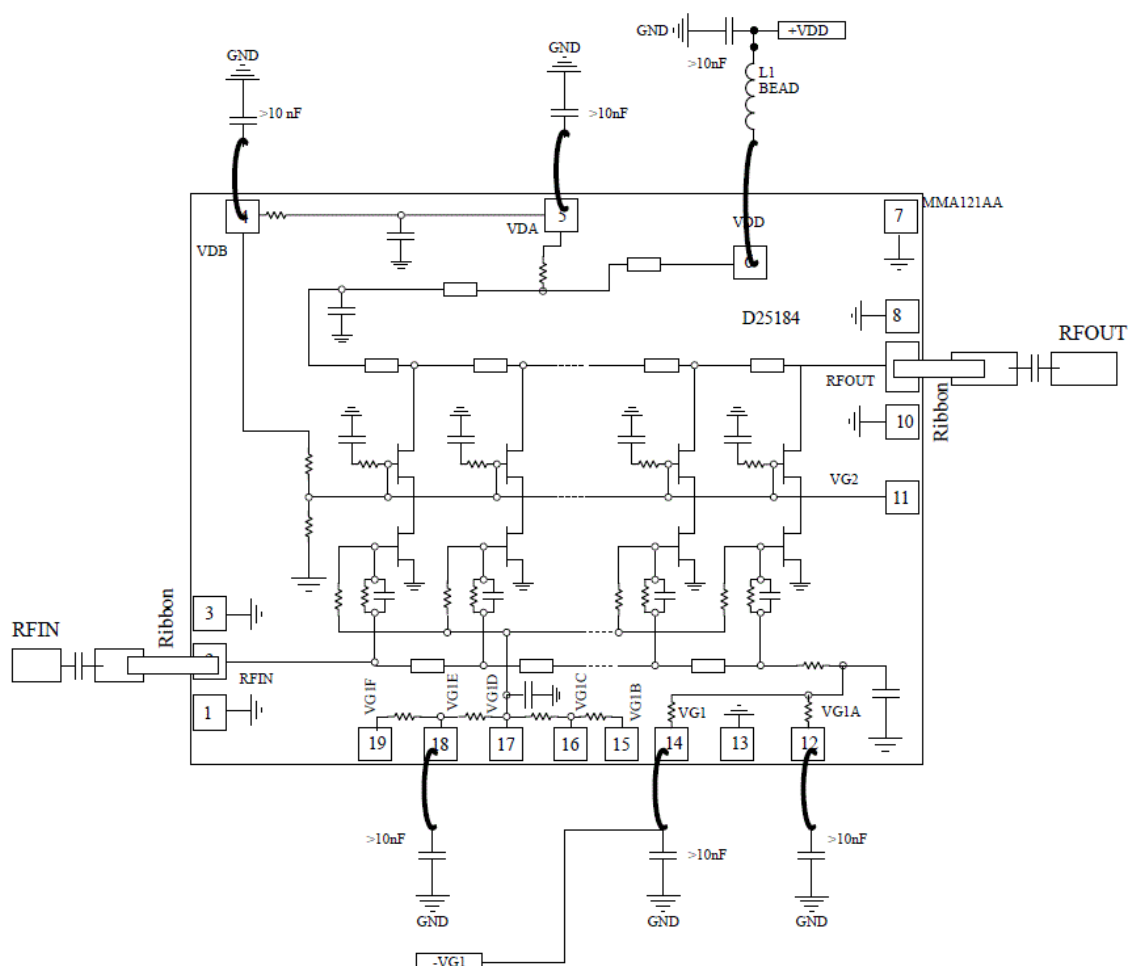
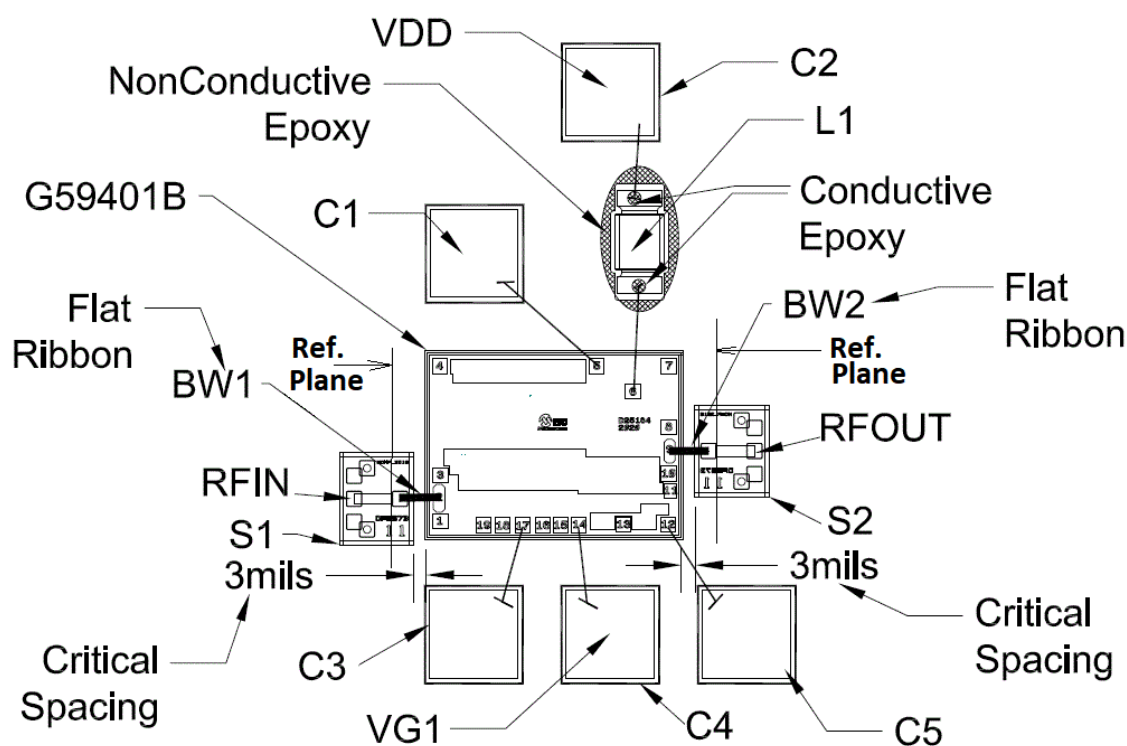


Figure 3-2. Die Test Circuit: Assembly Drawing**Table 3-1.** List of Material for Test Circuit

Reference	Part Number	Description
G59401B	MMA121AA	MMA121AA amplifier die
C1, C2, C3, C4, C5	160U02A102MT4W	Johanson dielectric, cer. cap 1 nF
S1, S2	E57311	Probe launchers
L1	0201 AF-330XRK	Coilcraft 0201 ferrite inductor
Epoxy	EpoTech Conductive H20E	Conductive epoxy for die and cap mount
Non-Conductive Epoxy	Non-Conductive Epoxy-H70E	Used for ferrite inductor L1 attach.

4. Ordering, Shipping, and Handling

4.1 Handling Recommendations

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4.2 Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
MMA121AA	Die

4.3 Packing Information

Standard Format
Gel pack
50 pieces per pack

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	10/2024	Document created.

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