

6A Peak, Low-Side MOSFET Driver

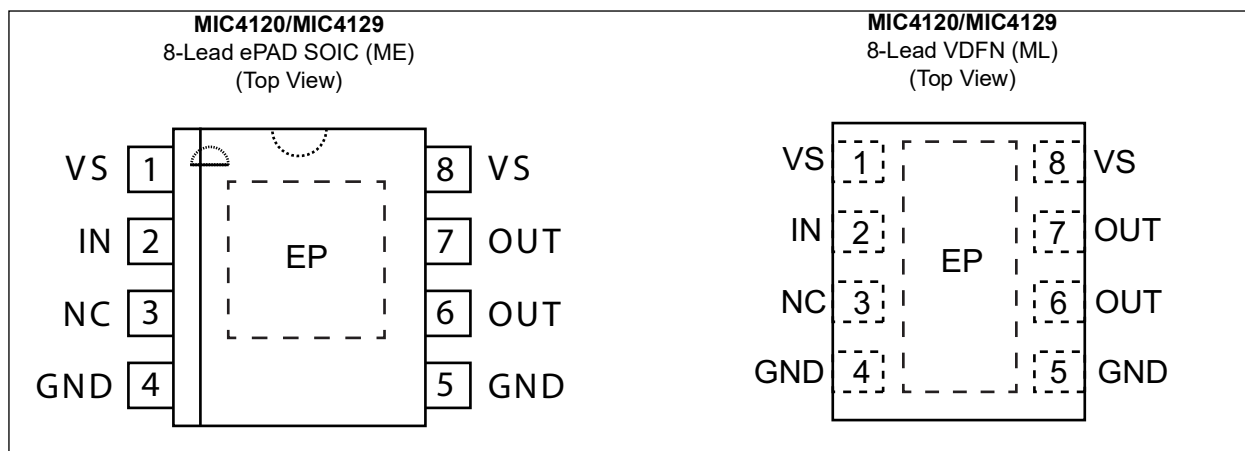
Features

- CMOS Construction
- Latch-Up Protected: Will Withstand >200 mA Reverse Output Current
- Logic Input Withstands Negative Swing up to 5V
- Matched Rise and Fall Times: 25 ns
- High Peak Output Current: 6A
- Wide Operating Voltage Range: 4.5V to 20V
- High Capacitive Load Drive: 10,000 pF
- Low Delay Time: 55 ns Typical
- Logic High Input for Any Voltage from 2.4V to V_S
- Low Equivalent Input Capacitance: 6 pF Typical
- Low Supply Current: 450 μ A with Logic 1 Input
- Low Output Impedance: 2.5 Ω
- Output Voltage Swing within 25 mV of Ground or V_S
- Exposed Backside Pad Packaging Reduces Heat
 - ePAD SOIC-8 ($\theta_{JA} = 58^\circ\text{C/W}$)
 - 3 mm x 3 mm VDFN-8 ($\theta_{JA} = 60^\circ\text{C/W}$)

Applications

- Switch Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class-D Switching Amplifiers

Package Types



General Description

The MIC4120 and MIC4129 MOSFET drivers are resilient, efficient, and easy to use. The MIC4129 is an inverting driver, while the MIC4120 is a non-inverting driver. The MIC4120 and MIC4129 are improved versions of the MIC4420 and MIC4429.

The drivers are capable of 6A (peak) output and can drive the largest MOSFETs with an improved safe operating margin. The MIC4120/29 accept any logic input from 2.4V to V_S without external speed-up capacitors or resistor networks. Proprietary circuits allow the input to swing negative by as much as 5V without damaging the part. Additional circuits protect against damage from electrostatic discharge.

The MIC4120/29 drivers can replace three or more discrete components, reducing PCB area requirements, simplifying product design, and reducing assembly cost.

Modern BiCMOS/DMOS construction ensures freedom from latch-up. The rail-to-rail swing capability insures adequate gate voltage to the MOSFET during power up/down sequencing.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage	+24V
Input Voltage	$V_S + 0.3V$ to GND – 5V
Input Current ($V_{IN} > V_S$)	50 mA
ESD Rating	(Note 1)

Operating Ratings ‡

Supply Voltage (V_{IN})	+4.5V to +20V
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† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Static-sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent damage from static discharge.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Device is ESD sensitive. Handling precautions are recommended. Human body model: 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

$T_A = +25^\circ\text{C}$ with $4.5V \leq V_S \leq 20V$ unless otherwise specified. [Note 1](#) Input Voltage slew rate $>1V/\mu s$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input						
Logic 1 Input Voltage	V _{IH}	2.4	1.9	—	V	—
Logic 0 Input Voltage	V _{IL}	—	1.5	0.8	V	—
Input Voltage Range	V _{IN}	–5	—	V _S + 0.3		—
Input Current	I _{IN}	–10	—	10	μA	0V ≤ V _{IN} ≤ V _S
Output						
Output High Voltage	V _{OH}	V _S – 0.025	—	—	V	Figure 1-1
Output Low Voltage	V _{OL}	—	—	0.025	V	Figure 1-1
Output Resistance, Output Low	R _{OL}	—	1.4	5	Ω	I _{OUT} = 10 mA, V _S = 20V
Output Resistance, Output High	R _{OH}	—	1.5	5	Ω	I _{OUT} = 10 mA, V _S = 20V
Peak Output Current	I _{OUT(PK)}	—	6	—	A	V _S = 20V, Figure 4-2
Latch-Up Protection from Reverse Current	I _R	200	—	—	mA	—
Switching Time						
Rise Time	t _R	—	12	30	ns	Figure 1-1, C _L = 2200 pF.
		—	—	35		
Fall Time	t _F	—	13	30	ns	Figure 1-1, C _L = 2200 pF.
		—	—	35		
Delay Time	t _{D1}	—	45	75	ns	Figure 1-1
		—	—	100		
Delay Time	t _{D2}	—	50	75	ns	Figure 1-1
		—	—	100		
Power Supply						
Power Supply Current	I _S	—	0.45	3	mA	V _{IN} = 3V
		—	60	400	μA	V _{IN} = 0V
Operating Input Voltage	V _S	4.5	—	20	V	—

Note 1: Specifications for packaged product only.

MIC4120/29

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	-40	—	+125	°C	—
Storage Temperature Range	T_S	-65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	300	°C	Soldering, 10 sec.
Package Thermal Resistances						
Thermal Resistance, ePAD SOIC 8-Ld	θ_{JA}	—	60	—	°C/W	—
Thermal Resistance, VDFN 8-Ld	θ_{JA}	—	58	—	°C/W	—

Test Circuits

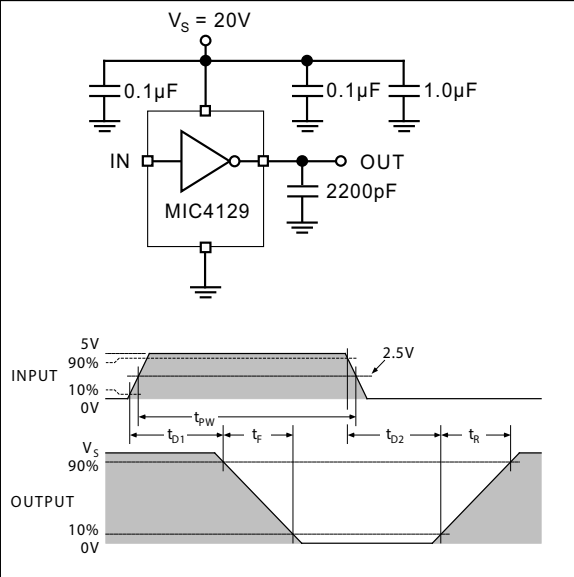


FIGURE 1-1: Inverting Driver Switching Time.

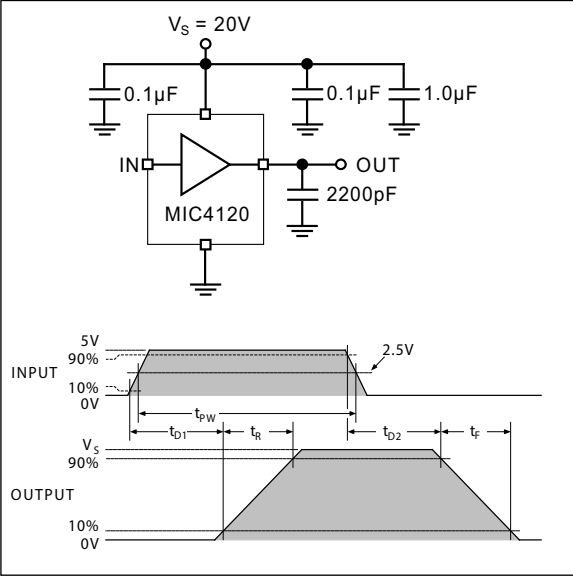


FIGURE 1-2: Non-inverting Driver Switching Time.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

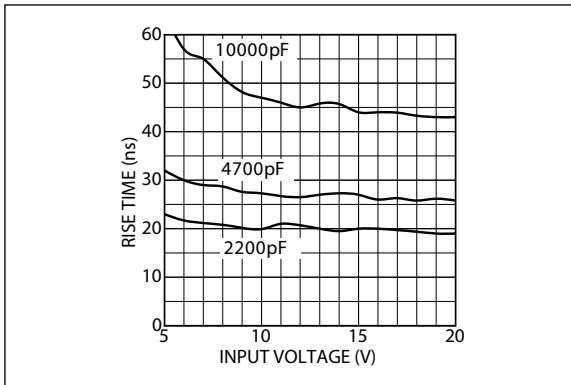


FIGURE 2-1: Rise Time.

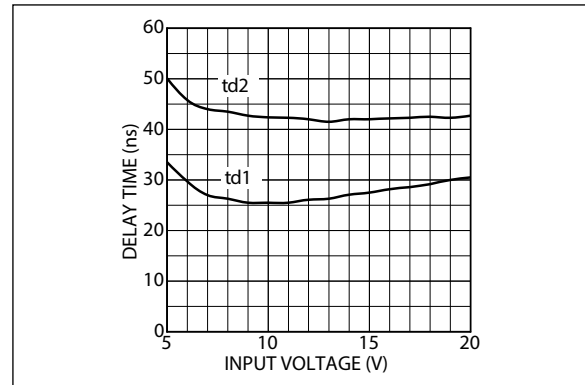


FIGURE 2-3: Delay Time vs. Input Voltage.

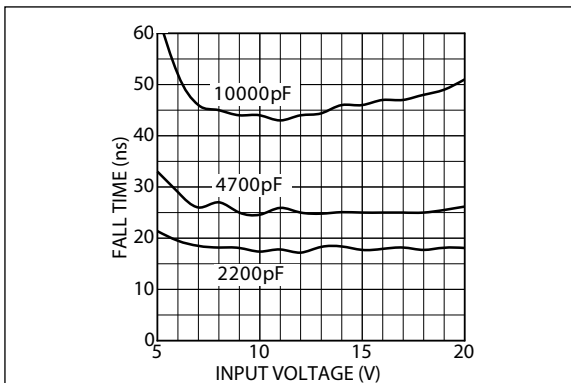


FIGURE 2-2: Fall Time.

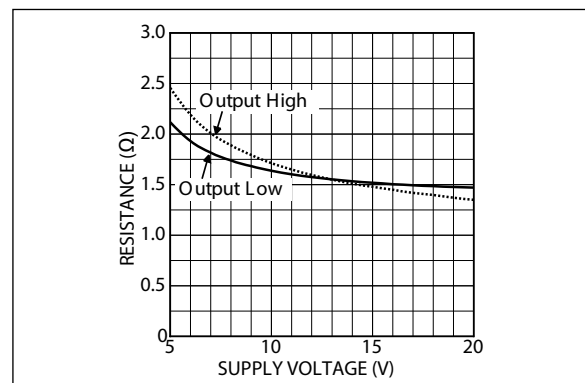


FIGURE 2-4: Output Resistance vs. Supply Voltage.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
2	IN	Control Input.
4, 5	GND	Ground. Duplicate pins must be externally connected together.
1, 8	VS	Supply Input. Duplicate pins must be externally connected together.
6, 7	OUT	Output. Duplicate pins must be externally connected together.
3	NC	Not connected.
ePAD	GND	Ground: Backside.

4.4 Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 and 74C have outputs that can only supply a few milliamperes of current and even shorting outputs to ground will not force enough current to destroy the device. The MIC4120 and MIC 4129, on the other hand, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

Table 4-1 lists the maximum safe operating frequency for several power supply voltages when driving a 2500 pF load. More accurate power dissipation figures can be obtained by summing the three dissipation sources.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-lead ePAD SOIC package, from the data sheet, is 60°C/W. In a +25°C ambient; then, using a maximum junction temperature of +150°C, this package will dissipate 2W.

Accurate power dissipation numbers can be obtained by totaling the three sources of power dissipation in the device:

- Load power dissipation (P_L)
- Quiescent power dissipation (P_Q)
- Transition power dissipation (P_T)

Calculation of load power dissipation differs depending upon whether the load is capacitive, resistive, or inductive.

TABLE 4-1: MIC4129 MAXIMUM OPERATING FREQUENCY

V_S	f_{MAX}
20V	1 MHz
15V	1.5 MHz
10V	3.5 MHz

Conditions: $T_A = +25^\circ\text{C}$, $CL = 2500 \text{ pF}$

4.5 Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

EQUATION 4-1:

$$P_L = I^2 \times R_O \times D$$

Where:

I = The current drawn by the load.

R_O = The output resistance of the driver when the output is high at the power supply voltage used (see data sheet).

D = Fraction of time the load is conducting (duty cycle).

4.6 Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the following equation:

EQUATION 4-2:

$$E = 1/2 \times C \times V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the "1/2" is removed. This equation also shows that it is good practice not to place more voltage on the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

EQUATION 4-3:

$$P_L = f \times C \times V_S^2$$

Where:

f = Operating frequency.

C = Load capacitance.

V_S = Driver supply voltage.

4.7 Inductive Load Power Dissipation

For inductive loads, the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

EQUATION 4-4:

$$P_{L1} = I^2 \times R_O \times D$$

However, in this instance, the R_O required may be either the ON resistance of the driver when its output is in the high state, or its ON resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as:

EQUATION 4-5:

$$P_{L2} = I \times V_D \times (1 - D)$$

Where:

V_D = The forward drop of the clamp diode in the driver (generally around 0.7V).

The two parts of the load dissipation must be summed ($P_{L1} + P_{L2} = P_L$) in to produce P_L .

4.8 Quiescent Power Dissipation

Quiescent power dissipation (P_Q) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤ 0.2 mA; a logic high will result in a current drain of ≤ 2.0 mA. Quiescent power can therefore be found from:

EQUATION 4-6:

$$P_Q = V_S \times [D \times I_H + (1 - D) \times I_L]$$

Where:

I_H = Quiescent current with input high.

I_L = Quiescent current with input low.

D = Fraction of time input is high (duty cycle).

V_S = Power supply voltage.

4.9 Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously and a current is conducted through them from $+V_S$ to Ground. The transition power dissipation is approximately:

EQUATION 4-7:

$$P_T = 2 \times f \times V_S \times (A \times s)$$

Where:

($A \times s$) = A time-current factor derived from the typical characteristic curves.

Total power dissipation (P_D) then, as previously described, is: $P_D = P_L + P_Q + P_T$

4.10 Definitions

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

f = Operating Frequency of the driver in Hertz.

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

P_L = Power dissipated in the driver due to the driver's load in Watts.

P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts.

Note: The "shoot-through" current from a dual transition (once up, once down) for both drivers must be multiplied by the number of repetitions per second (frequency) to find Watts.

R_O = Output resistance of a driver in Ohms.

V_S = Power supply voltage to the IC in Volts.

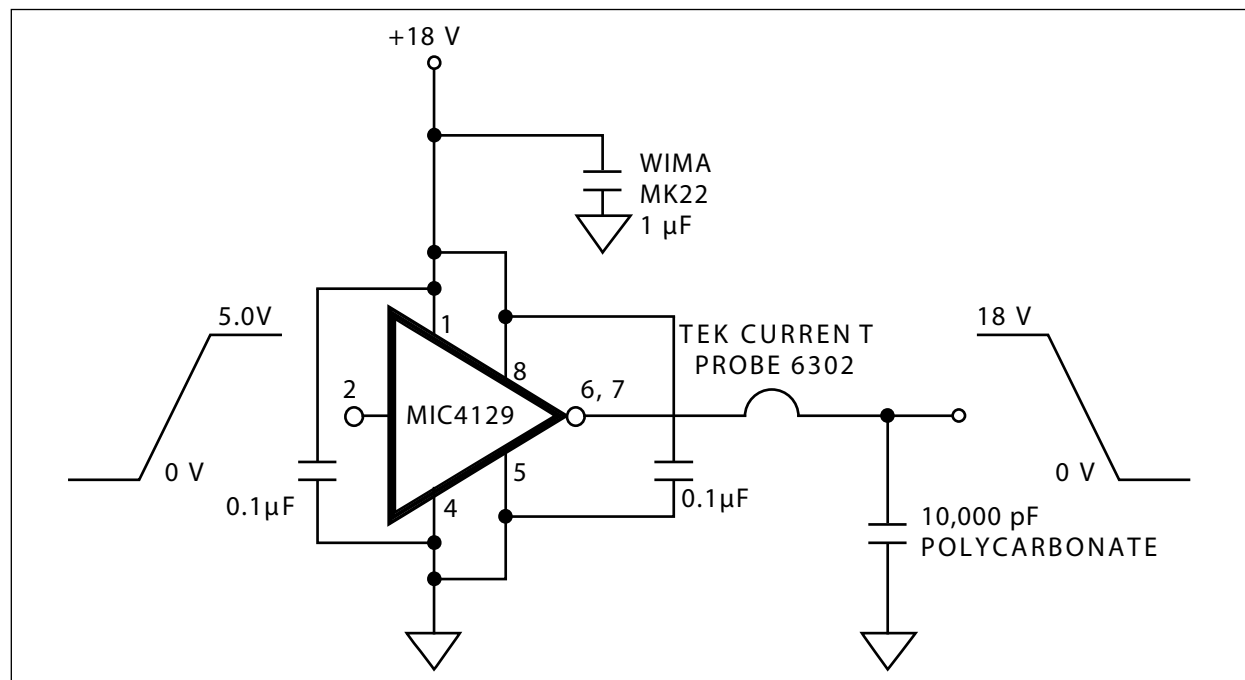
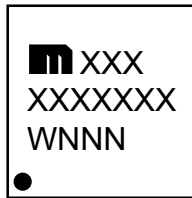


FIGURE 4-2: Peak Output Current Test Circuit.

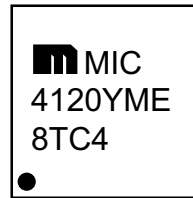
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

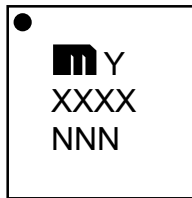
8-Lead SOIC*



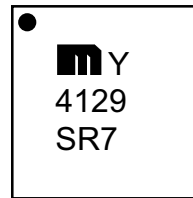
Example



8-Lead VDFN*



Example

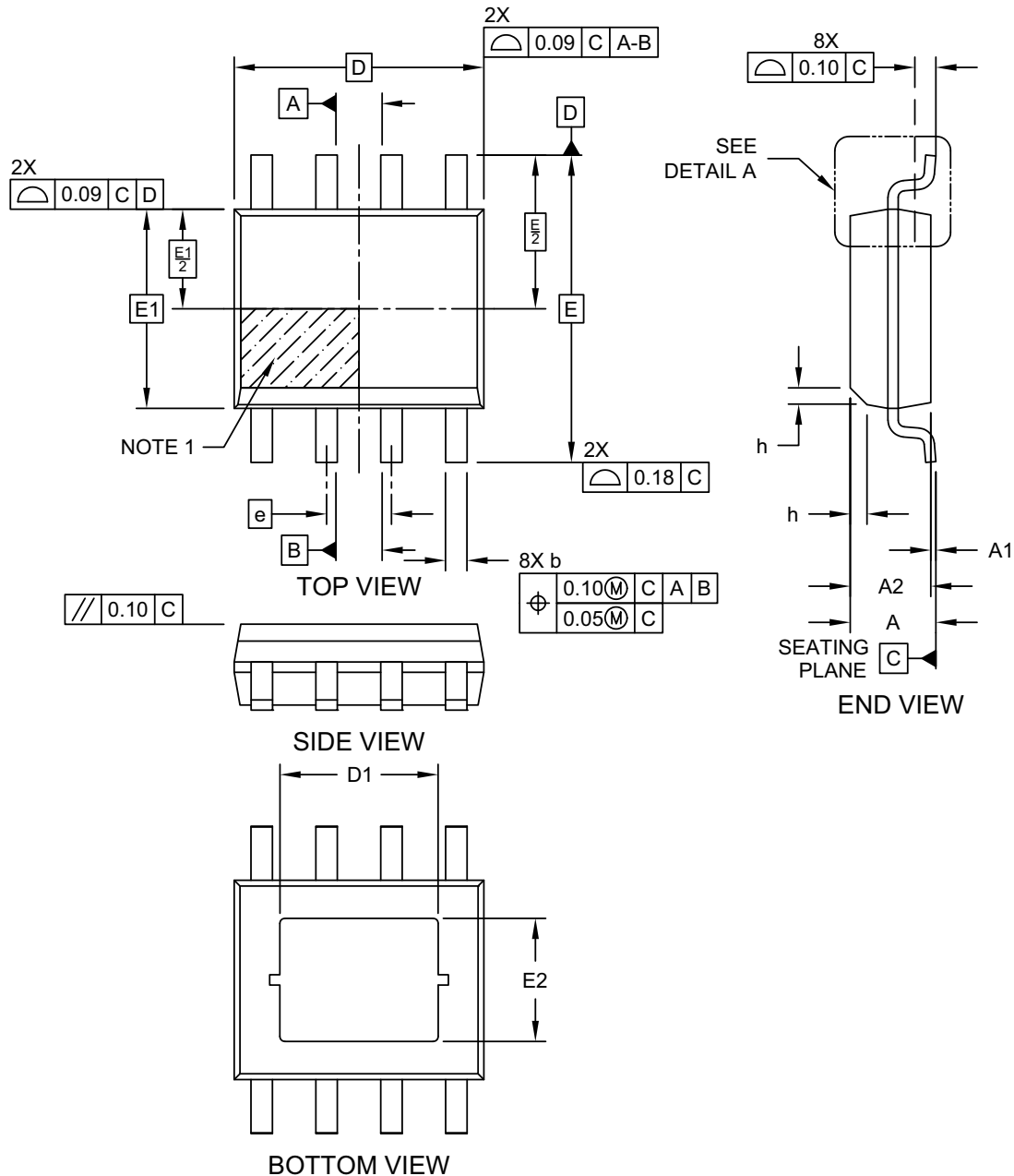


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
 6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
 2 Characters = NN; 1 Character = N

8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

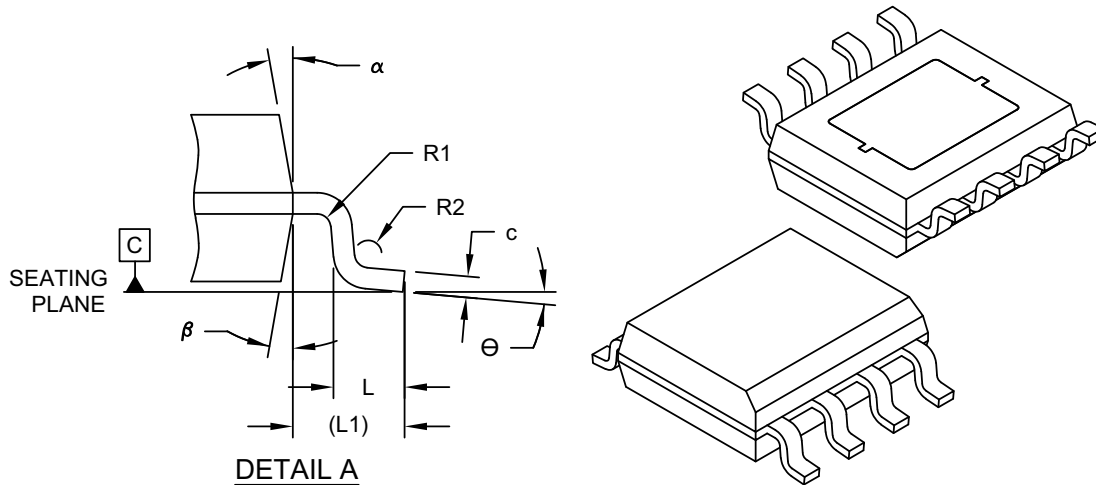
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-1136 Rev C Sheet 1 of 2

8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	1.43	1.55	1.68
Standoff	A1	0.00	0.05	0.10
Molded Package Thickness	A2	1.25	-	-
Overall Length	D	4.89 BSC		
Exposed Pad Length	D1	-	3.10	-
Overall Width	E	6.02 BSC		
Molded Package Width	E1	3.90 BSC		
Exposed Pad Width	E2	-	2.41	-
Pin 1 Chamfer	h	-	0.33	-
Terminal Width	b	0.35	0.41	0.49
Lead Thickness	c	0.19	0.20	0.25
Terminal Length	L	0.41	0.64	0.89
Footprint	L1	1.04 REF		
Foot Angle	Θ	0°	5°	8°
Lead Bend Radius	R1	0.07	-	-
Lead Bend Radius	R2	0.07	-	-
Mold Draft Angle	α	5°	-	15°
Mold Draft Angle	β	5°	-	15°

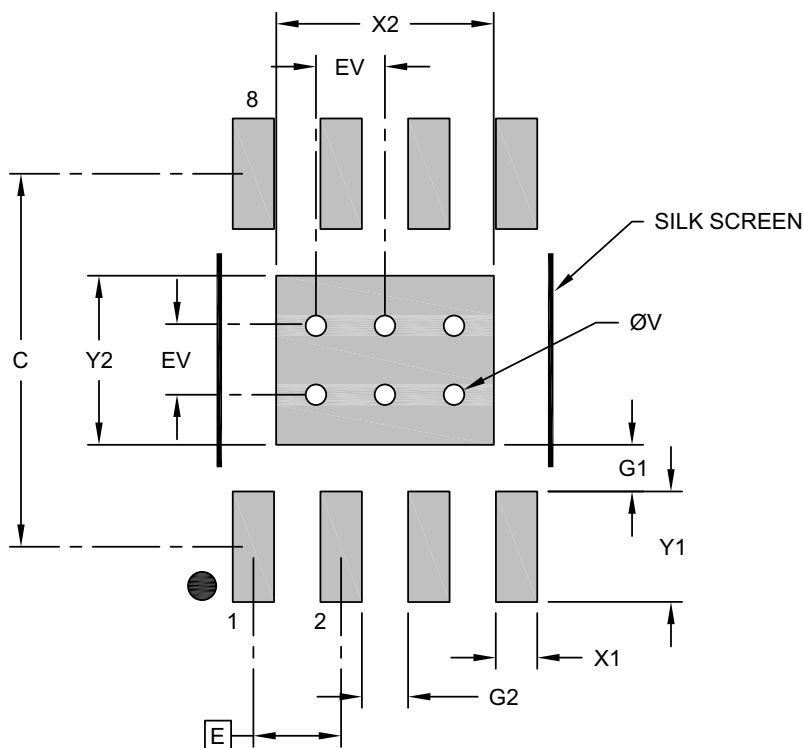
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1136 Rev C Sheet 2 of 2

8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Optional Center Pad Width	X2			3.15
Optional Center Pad Length	Y2			2.45
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.60
Contact Pad to Center Pad (X8)	G1	0.68		
Contact Pad to Contact Pad (X6)	G2	0.67		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

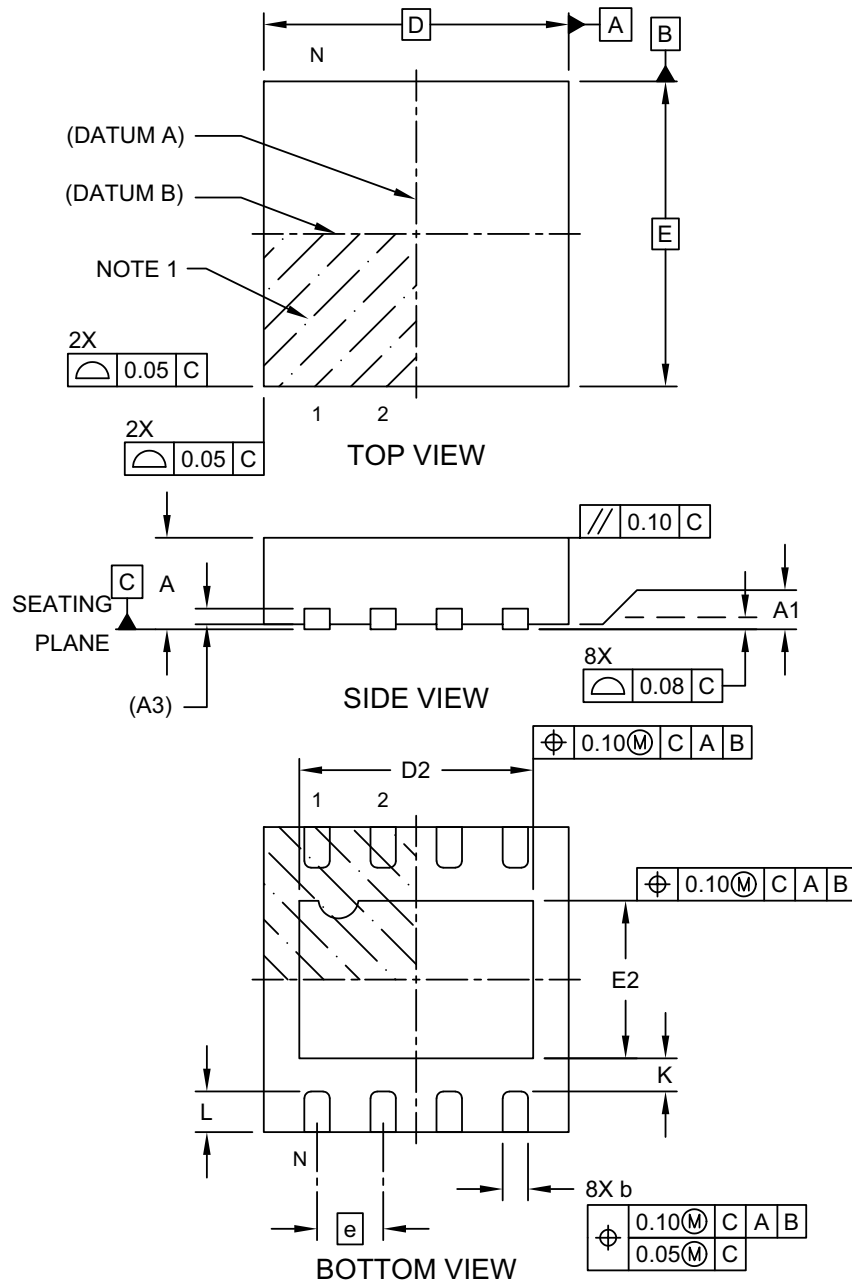
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3136 Rev C

8-Lead Very Thin Plastic Dual Flat, No Lead Package (JMA) - 3x3x0.9 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

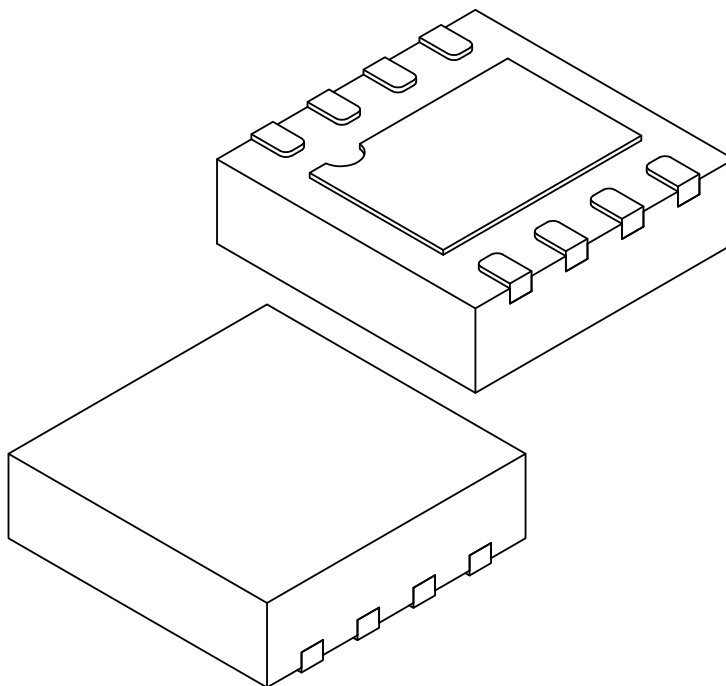


Microchip Technology Drawing C04-1021 Rev.C Sheet 1 of 2

MIC4120/29

8-Lead Very Thin Plastic Dual Flat, No Lead Package (JMA) - 3x3x0.9 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Length	D2	2.25	2.30	2.35
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.33	-	-

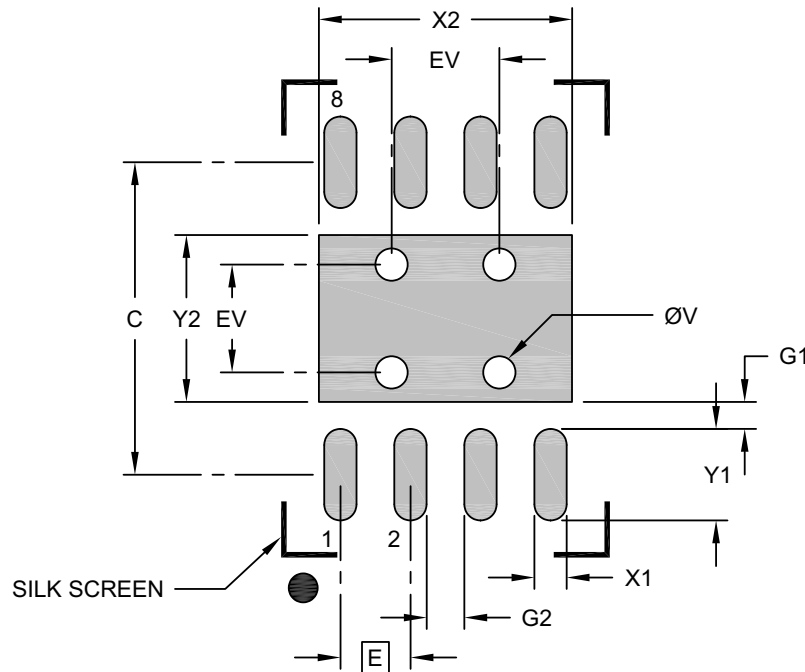
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1021 Rev.C Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (JMA) - 3x3x0.9 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension	Units	MILLIMETERS		
	Limits	MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Center Pad Width	X2			2.35
Center Pad Length	Y2			1.55
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.23		
Contact Pad to Contact Pad (X6)	G2	0.35		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3021 Rev C

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2025)

- Converted Micrel document MIC4120/29 to Microchip data sheet DS20007054A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>Part Number</u>	<u>X</u>	<u>XX</u>	<u>-XX</u>	Examples:
Device	Temp. Range	Package	Media Type	
Device:	MIC4120:	Non-Inverting 6A Peak, Low-Side MOSFET Driver		a) MIC4120YME: MIC4120, -40°C to +125°C Temp. Range, 8-Lead ePAD SOIC, 95/Tube
	MIC4129:	Inverting 6A Peak, Low-Side MOSFET Driver		b) MIC4129YML-TR: MIC4129, -40°C to +125°C Temp. Range, 8-Lead VDFN, 5,000/Reel
Temperature Range:	Y	=	-40°C to +125°C	c) MIC4120YML-TR: MIC4120, -40°C to +125°C Temp. Range, 8-Lead ePAD SOIC, 2,500/Reel
Package:	ME	=	8-Lead ePAD SOIC	d) MIC4129YME: MIC4129, -40°C to +125°C Temp. Range, 8-Lead ePAD SOIC, 95/Tube
	ML	=	8-Lead VDFN	
Media Type:	<blank>	=	95/Tube (SOIC only)	Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
	TR	=	2,500/Reel (SOIC only)	
	TR	=	5,000/Reel (VDFN only)	

NOTES:

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