25CS160

16-Kbit SPI Serial EEPROM with 128-Bit Serial Number

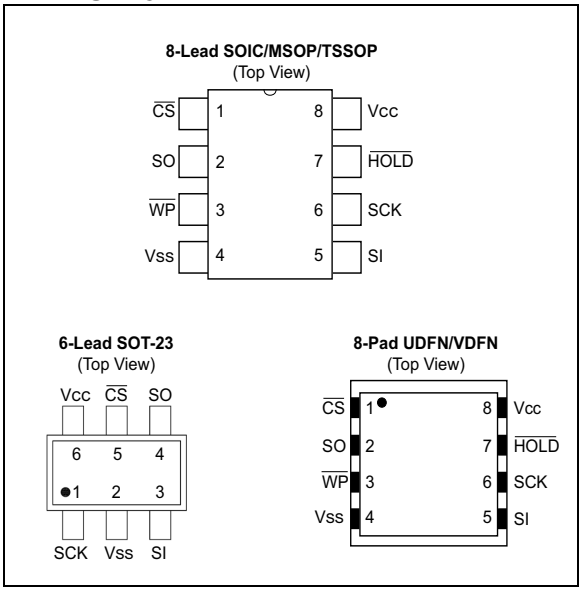
Features

- 16-Kbit Serial EEPROM:
  - 2,048 x 8 bit organization
  - Page size of 32 bytes
  - Byte or sequential reads
  - Byte or page writes
  - Self-timed write cycle (4 ms maximum)
- Backward Compatible with 25AA160D/25LC160D and AT25160B Serial EEPROMs
- Security Register:
  - Preprogrammed 128-bit serial number
  - 32-byte user-programmable, lockable ID page
- Built-in Error Correction Code (ECC) Logic:
  - ECC Status bit via the STATUS register
- Programmable Undervoltage Lockout Detection
- JEDEC® SPI Manufacturer Read ID Support
- High-Speed Clock Frequency:
  - 20 MHz at VCC ≥ 4.5V
  - 10 MHz at VCC ≥ 2.5V
  - 5 MHz at VCC ≥ 1.7V
- Block Write Protection:
  - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection:
  - Power on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- Low-Power CMOS Technology:
  - Voltage range: 1.7V to 5.5V
  - Write current: 3.0 mA at 5.5V
  - Read current: 3.0 mA at 4.5V, 10 MHz
  - Standby current: 1.0 µA at 5.5V (I-Temp.)
- High Reliability:
  - More than four million erase/write cycles
  - Built-in ECC logic for increased reliability
  - Data retention: > 200 years
  - ESD protection: > 4000V
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
  - Extended (H): -40°C to +150°C
- AEC-Q100 Automotive Qualified

Packages

- 8-Lead MSOP, 8-Lead SOIC, 6-Lead SOT-23, 8-Lead TSSOP, 8-Pad UDFN and 8-Pad Wettable Flanks VDFN

Package Types (not to scale)



Pin Function Table

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write-Protect Pin
Vss	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Hold Input
VCC	Supply Voltage

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General Description

The Microchip Technology Inc. 25CS160 provides 16 Kbits of Serial EEPROM utilizing the Serial Peripheral Interface (SPI) compatible bus. The device is organized as 2,048 bytes of 8 bits each (2-Kbyte) and is optimized for use in consumer, industrial and automotive applications where reliable and dependable nonvolatile memory storage is essential. The 25CS160 is capable of operation across a broad voltage range (1.7V to 5.5V).

The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{CS}$) input. Communication to the device can be paused via the $\overline{HOLD}$ pin. While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher-priority interrupts.

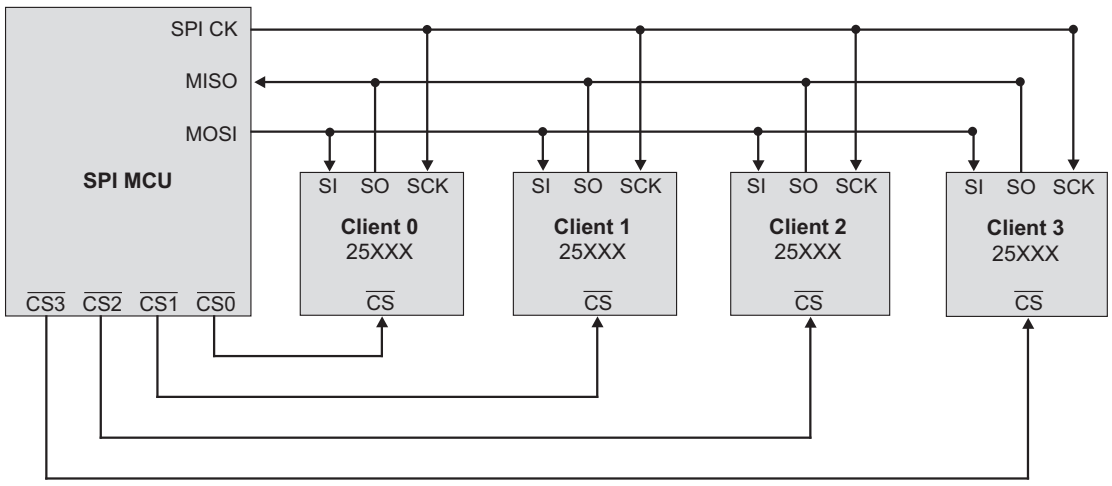
The 25CS160 features a nonvolatile Security register independent of the 16-Kbit main memory array. The first half of the Security register is read-only and contains a factory-programmed, globally unique, 128-bit serial number in the first 16 bytes. The 128-bit serial number is unique across the entire CS series of Serial EEPROM products and eliminates the time-consuming step of performing and ensuring serialization of a product on a manufacturing line. The 128-bit read-only serial number is followed by an additional 32 bytes of user-programmable EEPROM. The user-programmable section of the Security register can later be permanently write-protected via a software sequence.

To protect against brown-out events, an undervoltage lockout detection circuit inhibits all write sequences when V_{CC} supply voltage drops below the set voltage level. The voltage level is configurable via the Undervoltage Lockout Detection (UVLO) register.

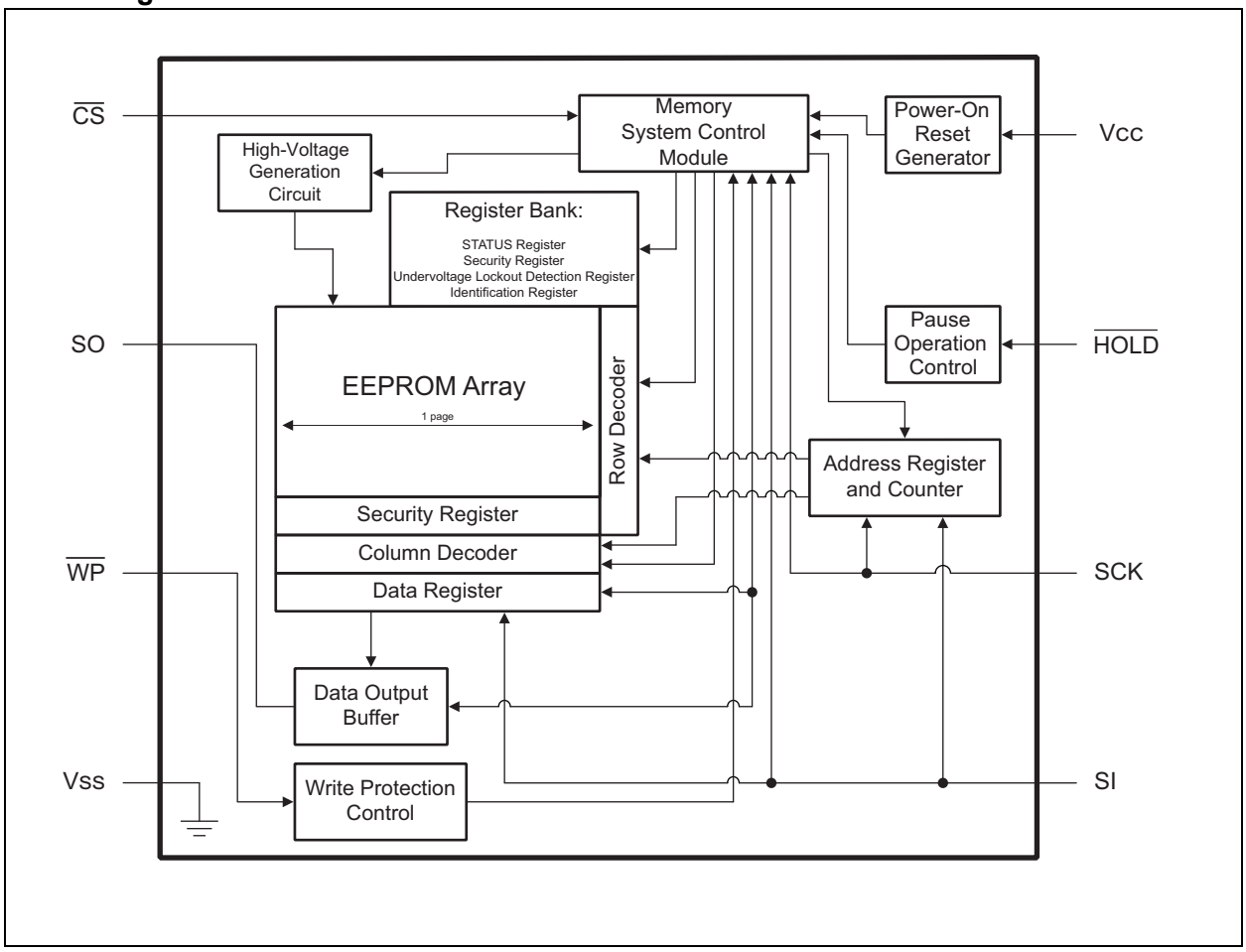
For added reliability, the 25CS160 utilizes a built-in Error Correction Code (ECC) scheme. This scheme can correct up to one incorrectly read bit within a one-byte readout. Additionally, the 25CS160 includes a flag in the STATUS register to report if any errors were detected and corrected in the most recent memory array read sequence.

The 25CS160 features an Identification register that contains identification information that can be read from the device. This enables the application to electronically query and identify the 25CS160 while it is in the system. The identification method and the instruction opcode comply with the JEDEC® standard for “Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices”. The type of information that can be read from the device includes the JEDEC®-defined Manufacturer ID, the vendor-specific Device ID and the vendor-specific Extended Device Information (EDI).

Bus Connections for the 25CS160



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V_{CC} 6.25V

All inputs and outputs w.r.t. V_{SS} ..... 0.6V to V_{CC} +1.0V

Storage temperature ..... -65°C to +155°C

Ambient temperature under bias ..... -40°C to +150°C(1)

ESD protection on all pins ..... 4 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time between +125°C and +150°C exceeds 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): T_{AMB} = -40°C to +85°C V_{CC} = 1.7V to 5.5V Extended (E): T_{AMB} = -40°C to +125°C V_{CC} = 1.8V to 5.5V Extended (H): T_{AMB} = -40°C to +150°C V_{CC} = 2.5V to 5.5V				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typical**	**Max.**	**Units**	**Test Conditions**
D001	V_{IH}	High-Level Input Voltage	V_{CC} x 0.7	—	V_{CC} + 1	V	
D002	V_{IL}	Low-Level Input Voltage	-0.6	—	V_{CC} x 0.3	V	
D003	V_{OL}	Low-Level Output Voltage	—	—	0.4	V	I_{OL} = 3.0 mA, V_{CC} = 4.5V
			—	—	0.2	V	I_{OL} = 1.0 mA, V_{CC} = 2.5V
D004	V_{OH}	High-Level Output Voltage	V_{CC} - 0.5	—	—	V	I_{OH} = -400 µA
D005	I_{LI}	Input Leakage Current	—	—	±1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}
D006	I_{LO}	Output Leakage Current	—	—	±1	µA	$\overline{CS}$ = V_{CC}, V_{OUT} = V_{SS} or V_{CC}
D007	C_{INT}	Internal Capacitance (all inputs and outputs)	—	—	6	pF	T_{AMB} = +25°C, F_{CLK} = 1.0 MHz, V_{CC} = 5.0V (**Note 1**)
D008	I_{CCREAD}	Operating Current	—	—	5	mA	V_{CC} = 5.5V, F_{CLK} = 20 MHz, SO = Open
			—	—	3	mA	V_{CC} = 4.5V, F_{CLK} = 10 MHz, SO = Open
			—	—	2	mA	V_{CC} = 2.5V, F_{CLK} = 5 MHz, SO = Open
D009	$I_{CCWRITE}$	Operating Current	—	—	3	mA	V_{CC} = 5.5V
			—	—	2	mA	V_{CC} = 2.5V

Note 1: This parameter is not 100% tested but is ensured by characterization.

TABLE 1-1: DC CHARACTERISTICS (CONTINUED)

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TAMB = -40°C to +85°C VCC = 1.7V to 5.5V Extended (E): TAMB = -40°C to +125°C VCC = 1.8V to 5.5V Extended (H): TAMB = -40°C to +150°C VCC = 2.5V to 5.5V				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typical**	**Max.**	**Units**	**Test Conditions**
D010	ICCS	Standby Current	—	—	10	µA	$\overline{CS}$ = VCC = 5.5V, TAMB = +150°C, VIN = VCC or VSS
			—	—	3	µA	$\overline{CS}$ = VCC = 5.5V, TAMB = +125°C, VIN = VCC or VSS
			—	—	1	µA	$\overline{CS}$ = VCC = 5.5V, TAMB = +85°C, VIN = VCC or VSS
D011	VUVL	Undervoltage Lockout Level (**Note 1**)	1.4	1.5	1.6	V	VUVL[4:0] = 00000
			1.5	1.6	1.7	V	VUVL[4:0] = 00001
			1.6	1.7	1.8	V	VUVL[4:0] = 00010
			1.7	1.8	1.9	V	VUVL[4:0] = 00011
			1.8	1.9	2.0	V	VUVL[4:0] = 00100
			1.9	2.0	2.1	V	VUVL[4:0] = 00101
			2.0	2.1	2.2	V	VUVL[4:0] = 00110
			2.1	2.2	2.3	V	VUVL[4:0] = 00111
			2.2	2.3	2.4	V	VUVL[4:0] = 01000
			2.3	2.4	2.5	V	VUVL[4:0] = 01001
			2.4	2.5	2.6	V	VUVL[4:0] = 01010
			2.5	2.6	2.7	V	VUVL[4:0] = 01011
			2.5	2.7	2.9	V	VUVL[4:0] = 01100
			2.6	2.8	3.0	V	VUVL[4:0] = 01101
			2.7	2.9	3.1	V	VUVL[4:0] = 01110
			2.8	3.0	3.2	V	VUVL[4:0] = 01111
			2.9	3.1	3.3	V	VUVL[4:0] = 10000
			3.0	3.2	3.4	V	VUVL[4:0] = 10001
			3.1	3.3	3.5	V	VUVL[4:0] = 10010
			3.2	3.4	3.6	V	VUVL[4:0] = 10011
			3.3	3.5	3.7	V	VUVL[4:0] = 10100
			3.4	3.6	3.8	V	VUVL[4:0] = 10101
			3.5	3.7	3.9	V	VUVL[4:0] = 10110
			3.6	3.8	4.0	V	VUVL[4:0] = 10111
			3.7	3.9	4.1	V	VUVL[4:0] = 11000
			3.8	4.0	4.2	V	VUVL[4:0] = 11001
			3.9	4.1	4.3	V	VUVL[4:0] = 11010
			4.0	4.2	4.4	V	VUVL[4:0] = 11011
			4.1	4.3	4.5	V	VUVL[4:0] = 11100
			4.2	4.4	4.6	V	VUVL[4:0] = 11101
			4.3	4.5	4.7	V	VUVL[4:0] = 11110
			4.4	4.6	4.8	V	VUVL[4:0] = 11111

Note 1: This parameter is not 100% tested but is ensured by characterization.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): T_{AMB} = -40°C to +85°C V_{CC} = 1.7V to 5.5V Extended (E): T_{AMB} = -40°C to +125°C V_{CC} = 1.8V to 5.5V Extended (H): T_{AMB} = -40°C to +150°C V_{CC} = 2.5V to 5.5V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	F_{CLK}	Clock Frequency	—	20	MHz	V_{CC} ≥ 4.5V, T_{AMB} ≤ +125°C
			—	10	MHz	V_{CC} ≥ 2.5V
			—	5	MHz	V_{CC} ≥ 1.7V
2	T_{CSS}	$\overline{CS}$ Setup Time	15	—	ns	V_{CC} ≥ 4.5V, T_{AMB} ≤ +125°C
			30	—	ns	V_{CC} ≥ 2.5V
			60	—	ns	V_{CC} ≥ 1.7V
3	T_{CSH}	$\overline{CS}$ Hold Time	15	—	ns	V_{CC} ≥ 4.5V, T_{AMB} ≤ +125°C
			30	—	ns	V_{CC} ≥ 2.5V
			60	—	ns	V_{CC} ≥ 1.7V
4	T_{CSD}	$\overline{CS}$ Disable Time	50	—	ns	
5	T_{SU}	Data Setup Time	5	—	ns	V_{CC} ≥ 4.5V, T_{AMB} ≤ +125°C
			10	—	ns	V_{CC} ≥ 2.5V
			20	—	ns	V_{CC} ≥ 1.7V
6	T_{HD}	Data Hold Time	5	—	ns	V_{CC} ≥ 4.5V, T_{AMB} ≤ +125°C
			10	—	ns	V_{CC} ≥ 2.5V
			20	—	ns	V_{CC} ≥ 1.7V
7	T_R	CLK Rise Time	—	2	µs	**Note 1**
8	T_F	CLK Fall Time	—	2	µs	**Note 1**
9	T_{HI}	Clock High Time	20	—	ns	V_{CC} ≥ 4.5V, T_{AMB} ≤ +125°C
			40	—	ns	V_{CC} ≥ 2.5V
			80	—	ns	V_{CC} ≥ 1.7V
10	T_{LO}	Clock Low Time	20	—	ns	V_{CC} ≥ 4.5V, T_{AMB} ≤ +125°C
			40	—	ns	V_{CC} ≥ 2.5V
			80	—	ns	V_{CC} ≥ 1.7V
11	T_{CLD}	Clock Delay Time	50	—	ns	
12	T_{CLE}	Clock Enable Time	50	—	ns	
13	T_V	Output Valid from Clock Low	—	20	ns	V_{CC} ≥ 4.5V, T_{AMB} ≤ +125°C
			—	40	ns	V_{CC} ≥ 2.5V
			—	80	ns	V_{CC} ≥ 1.7V
14	T_{HO}	Output Hold Time	0	—	ns	**Note 1**
15	T_{DIS}	Output Disable Time	—	20	ns	V_{CC} ≥ 4.5V, T_{AMB} ≤ 125°C (**Note 1**)
			—	40	ns	V_{CC} ≥ 2.5V (**Note 1**)
			—	80	ns	V_{CC} ≥ 1.7V (**Note 1**)
16	T_{HS}	$\overline{HOLD}$ Setup Time	5	—	ns	V_{CC} ≥ 4.5V, T_{AMB} ≤ +125°C
			10	—	ns	V_{CC} ≥ 2.5V
			20	—	ns	V_{CC} ≥ 1.7V

Note 1: This parameter is not 100% tested but is ensured by characterization.

2: T_{WC} begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TAMB = -40°C to +85°C VCC = 1.7V to 5.5V Extended (E): TAMB = -40°C to +125°C VCC = 1.8V to 5.5V Extended (H): TAMB = -40°C to +150°C VCC = 2.5V to 5.5V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
17	THH	$\overline{\text{HOLD}}$ Hold Time	5	—	ns	VCC ≥ 4.5V, TAMB ≤ +125°C
			10	—	ns	VCC ≥ 2.5V
			20	—	ns	VCC ≥ 1.7V
18	THZ	$\overline{\text{HOLD}}$ Low to Output High Z	—	30	ns	VCC ≥ 4.5V, TAMB ≤ +125°C (**Note 1**)
			—	60	ns	VCC ≥ 2.5V (**Note 1**)
			—	160	ns	VCC ≥ 1.7V (**Note 1**)
19	THV	$\overline{\text{HOLD}}$ High to Output Valid	—	30	ns	VCC ≥ 4.5V, TAMB ≤ +125°C
			—	60	ns	VCC ≥ 2.5V
			—	160	ns	VCC ≥ 1.7V
20	TUVL	UVLO Detection Time	50	—	µs	
21	TWC	Internal Write Cycle Time	—	4	ms	**Note 2**

Note 1: This parameter is not 100% tested but is ensured by characterization.

2: TWC begins on the rising edge of $\overline{\text{CS}}$ after a valid write sequence and ends when the internal write cycle is complete.

FIGURE 1-1: INPUT TEST WAVEFORMS AND MEASUREMENT LEVELS

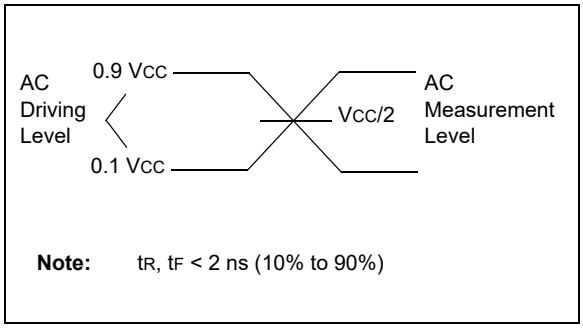


FIGURE 1-2: OUTPUT TEST LOAD

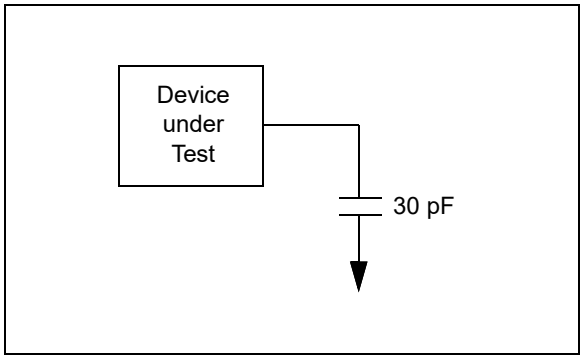


FIGURE 1-3: SERIAL INPUT TIMING

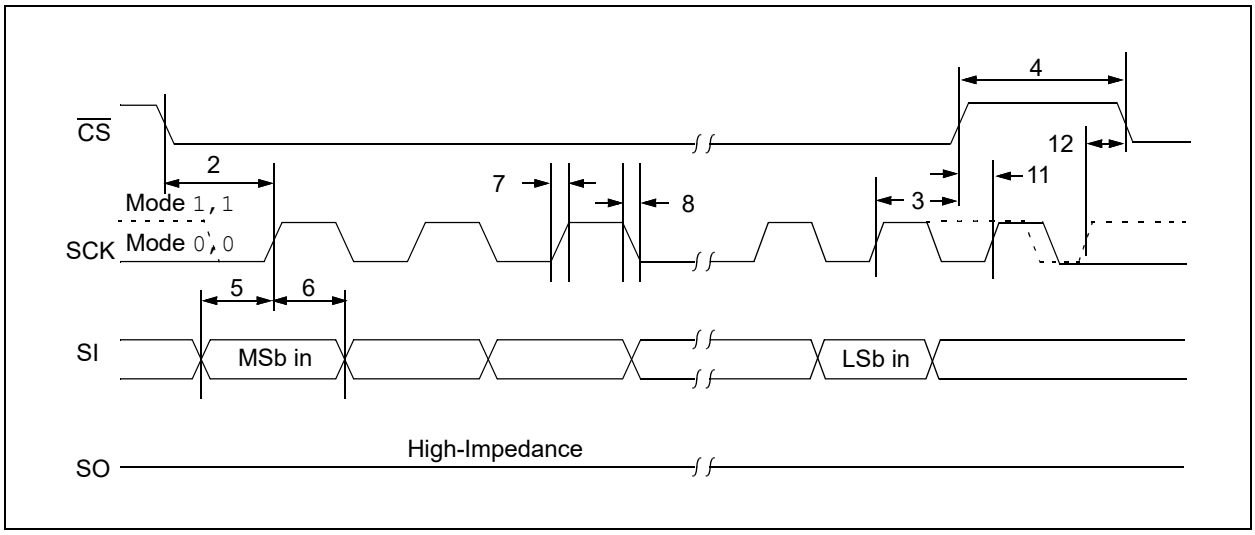


FIGURE 1-4: SERIAL OUTPUT TIMING

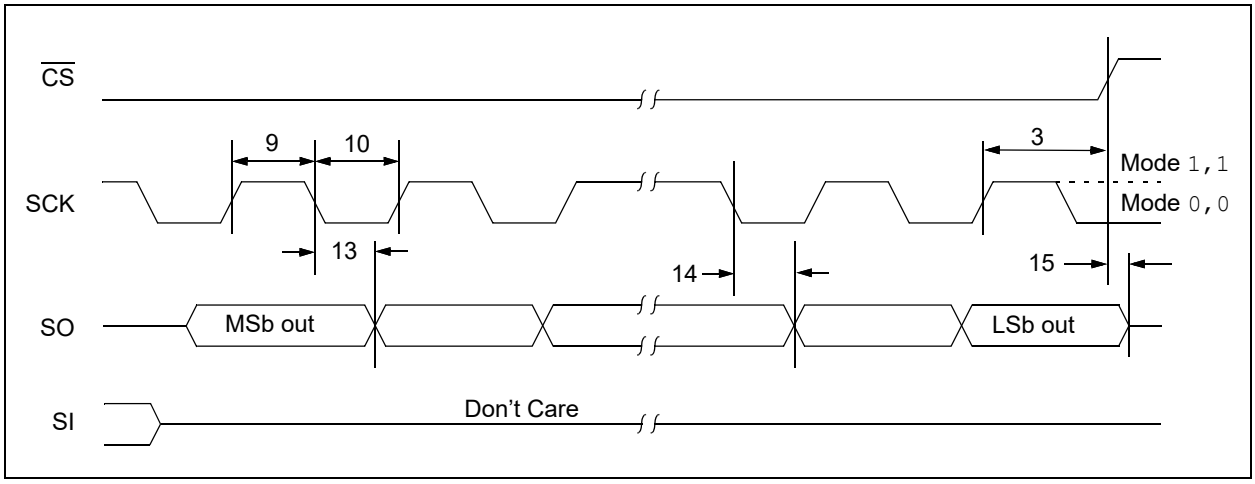


FIGURE 1-5: HOLD TIMING

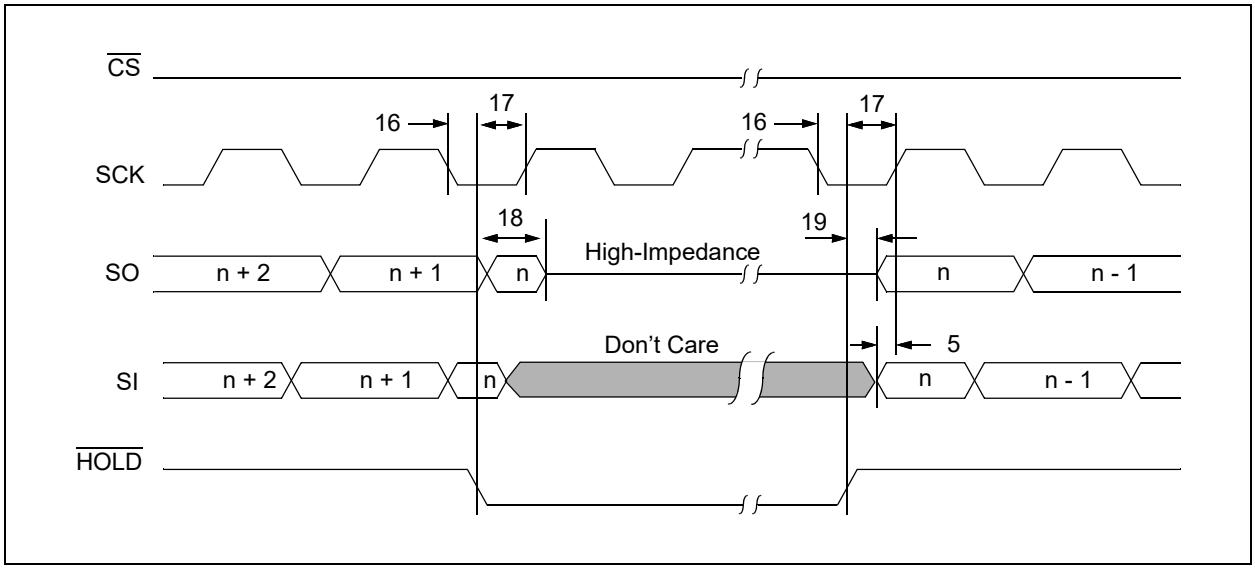


TABLE 1-3: EEPROM CELL PERFORMANCE CHARACTERISTICS

Operation	Test Condition	Min.	Max.	Units
Write Endurance(1)	T_A = +25°C	4,000,000	—	Write Cycles
	T_A = +85°C	1,200,000	—	
	T_A = +125°C	600,000	—	
	T_A = +150°C	400,000	—	
Data Retention(1)	T_A = +55°C	200	—	Years

Note 1: Performance is determined through characterization and the qualification process.

1.1 Power-Up Requirements and Default Conditions

During a power-up sequence, the V_{CC} supplied to the 25CS160 should monotonically rise from V_{SS} to the minimum V_{CC} level, as specified in Table 1-1, with a slew rate no faster than 0.1 V/µs.

1.1.1 DEVICE POWER-ON RESET

TABLE 1-4: POWER-UP CONDITIONS

Symbol	Parameter	Min.	Max.	Units
T_{VCSL}	Minimum V_{CC} to Chip Select Low Time	100	—	µs
V_{POR}	Power-On Reset Threshold Voltage	—	1.5	V
T_{POFF}	Minimum time at V_{CC} = 0V between power cycles	1	—	ms

To prevent spurious events from happening during a power-up sequence, the 25CS160 includes a Power-On Reset (POR) circuit. Upon power-up, the device will not respond to any instructions until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode.

Microchip recommends that $\overline{CS}$ follows the rise of V_{CC} at power-up through the use of a pull-up resistor. The system designer must ensure that no instruction is sent to the device and $\overline{CS}$ is driven high until the V_{CC} supply reaches a stable value greater than the minimum V_{CC} level. Once V_{CC} has surpassed the minimum level, the SPI host must wait at least T_{VCSL} before asserting the $\overline{CS}$ pin. See Table 1-4 for the values associated with these power-up parameters.

If an event occurs in the system where the V_{CC} level supplied to the 25CS160 drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed by first driving the V_{CC} pin to V_{SS}, waiting at least the minimum T_{POFF} time and then performing a new power-up sequence in compliance with the requirements defined in this section.

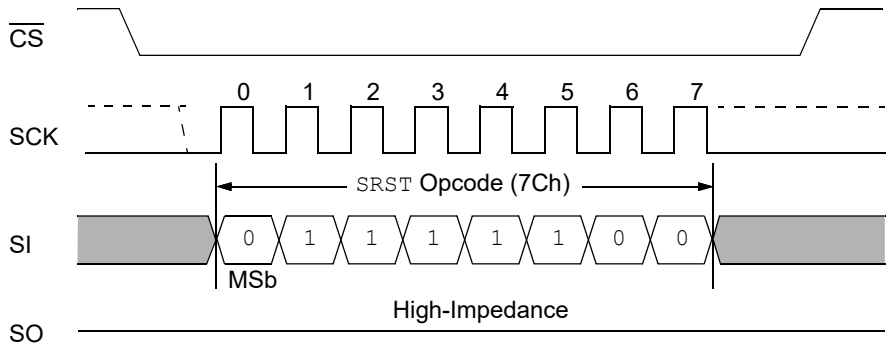
1.1.2 SOFTWARE DEVICE RESET

The 25CS160 includes a Software Device Reset (SRST) instruction that gives the user the opportunity to reset the device to its power-on default behavior (**Section 1.2 "Device Default State"**) without the need to power cycle the device. To execute this Reset, the $\overline{CS}$ pin must first be driven low to select the device, and then a 7Ch opcode is clocked in on the SI pin.

Then the $\overline{CS}$ pin can be driven high, and the Reset mechanism will engage. The Reset will have internally completed by the time the minimum T_{CSD} time is satisfied.

Note: The SRST instruction cannot interrupt the device while it is in a Busy state (**Section 6.1.4 "Ready/BUSY STATUS LATCH"**).

FIGURE 1-6: SOFTWARE DEVICE RESET (SRST) INSTRUCTION



1.2 Device Default State

1.2.1 POWER-UP DEFAULT STATE

The 25CS160 default state upon power-up consists of:

- Standby power mode ($\overline{CS}$ = HIGH)
- A high-to-low-level transition on $\overline{CS}$, which is required to enter active state
- Write Enable Latch (WEL) bit in the STATUS register = 0
- Error Correction State Latch (ECS) bit in the STATUS register = 0
- Write Lockout State (WLS) bit in the STATUS register = 0
- $\overline{\text{Ready}}$/Busy ($\overline{RDY}$/BUSY) bit in the STATUS register = 0, indicating the device is ready to accept a new instruction

1.2.2 DEVICE FACTORY DEFAULT CONDITION

The 25CS160 is shipped to the customer with the EEPROM array set to an all FFh data pattern (logic '1' state).

The Security register contains a preprogrammed, 128-bit serial number in the lower 16 bytes. The user-programmable portion (lockable ID page) is unlocked and is set to logic '1', resulting in 32 bytes of FFh data.

In the various device registers, the following nonvolatile bits are set:

- Write Protection Enable (WPEN) bit in the STATUS register is set to logic '0' to allow writing to the STATUS register (see Table 1-5)
- Block Write-Protect (BP[1:0]) bits in the STATUS register are logic '0', indicating no write protection set when in Legacy mode (see Table 1-5)
- Undervoltage Lockout Detection (UVLO) register is set to 00h, indicating that the UVLO function is not enabled and the undervoltage lockout detection level (V_{UVL}) is set to the minimum level (see Table 1-7)

TABLE 1-5: STATUS REGISTER BITS – BYTE 0 (FACTORY DEFAULT)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	Reserved	Reserved	Reserved	BP1	BP0	WEL(1)	$\overline{RDY}$/BUSY(1)
0	0	0	0	0	0	0	0

Note 1: These bits are volatile and are reset to this value upon power-up.

TABLE 1-6: STATUS REGISTER BITS – BYTE 1 (FACTORY DEFAULT)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	ECS(1)	Reserved	Reserved	Reserved	WLS(1)	Reserved	$\overline{RDY}$/BUSY(1)
0	0	0	0	0	0	0	0

Note 1: These bits are volatile and are reset to this value upon power-up.

TABLE 1-7: UNDERVOLTAGE LOCKOUT DETECTION REGISTER (FACTORY DEFAULT)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	UVLOEN	VUVL4	VUVL3	VUVL2	VUVL1	VUVL0
0	0	0	0	0	0	0	0

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	MSOP	SOIC	SOT-23	TSSOP	UDFN(1)	VDFN(1)	Function
$\overline{CS}$	1	1	5	1	1	1	Chip Select Input
SO	2	2	4	2	2	2	Serial Data Output
$\overline{WP}$	3	3	—	3	3	3	Write-Protect
VSS	4	4	2	4	4	4	Ground
SI	5	5	3	5	5	5	Serial Data Input
SCK	6	6	1	6	6	6	Serial Clock Input
$\overline{HOLD}$	7	7	—	7	7	7	Hold Input
VCC	8	8	6	8	8	8	Device Power Supply

Note 1: Exposed pad on UDFN/VDFN can be connected to VSS or left floating.

2.1 Chip Select ($\overline{CS}$)

Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device will be deselected and placed in Standby mode, and the SO pin will be in a high-impedance state. When the device is deselected, data will not be accepted on the SI pin.

A high-to-low transition on the $\overline{CS}$ pin is required to start a sequence, and a low-to-high transition is required to end a sequence. For write sequences, the device will not enter Standby mode until the completion of the self-timed internal write cycle.

2.2 Serial Data Output (SO)

The SO pin is used to shift data out from the device. Data on the SO pin are always clocked out on the falling edge of SCK. The SO pin is in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted) as well as when the Hold function is engaged.

2.3 Write-Protect Pin ($\overline{WP}$)

The Write-Protect ($\overline{WP}$) pin can be used to protect the STATUS register and memory array contents via the Block Protection modes when Legacy Write Protection mode is enabled.

2.4 Serial Data Input (SI)

Instructions, addresses and data are latched by the 25CS160 on the rising edge of the Serial Clock (SCK) line via the Serial Data Input (SI) pin.

2.5 Serial Clock (SCK)

The Serial Clock (SCK) pin is used to provide a clock signal to the device and is used to synchronize the flow of data to and from the device. Instructions, addresses and data present on SI pin are always latched in on the rising edge of SCK, while output data on the SO pin are always clocked out on the falling edge of SCK.

2.6 Hold ($\overline{HOLD}$)

When the device is selected and a serial communication sequence is underway, $\overline{HOLD}$ can be used to pause the communication with the host device without resetting the serial sequence.

3.0 MEMORY ORGANIZATION

3.1 EEPROM Organization

The 25CS160 is internally organized as 64 pages of 32 bytes each.

3.2 Device Registers

The 25CS160 contains four types of registers that modulate device operation and/or report on the current status of the device. These registers are:

- STATUS register
- Security register
- Undervoltage Lockout Detection (UVLO) register
- Identification register

3.2.1 STATUS REGISTER

The STATUS register is a 16-bit combination of volatile and nonvolatile bits. It is used to modify the write protection functions as well as store various aspects of the current status of the device. Details about the STATUS register are covered in **Section 6.0 "STATUS Register"**.

3.2.2 SECURITY REGISTER

The Security register is split into a read-only section and a user-programmable, lockable ID page section. The read-only section contains a preprogrammed, globally unique, 128-bit serial number.

The user-programmable (lockable ID page) section of the Security register is ideal for applications that need to irreversibly protect critical or sensitive application data from ever being altered. See **Section 9.0 "Security Register"** for more details about the Security register.

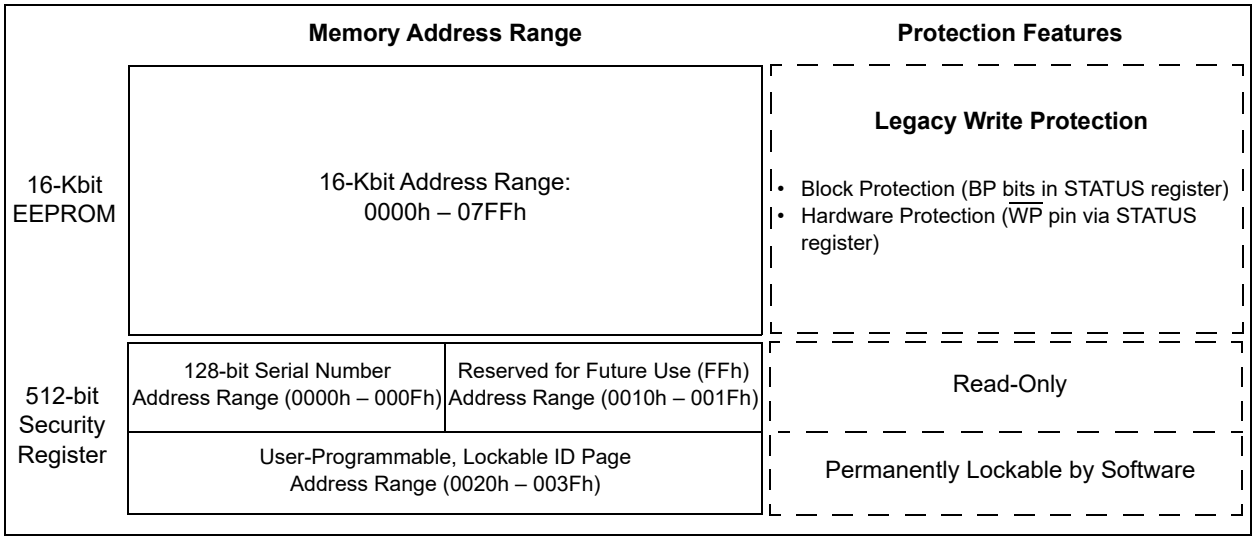
3.2.3 UNDERVOLTAGE LOCKOUT REGISTER

The Undervoltage Lockout Detection (UVLO) register is an 8-bit nonvolatile register that can be used to modify the threshold of the undervoltage detection circuit. Information on this function can be found in **Section 10.0 "Programmable UnderVoltage Lockout"**.

3.2.4 IDENTIFICATION REGISTER

The Identification register is a 40-bit nonvolatile, read-only register that contains device identification data in compliance with the JEDEC® standard for "Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices." The contents and format of the Identification register can be reviewed in **Section 11.0 "Identification Register"**.

FIGURE 3-1: MEMORY ORGANIZATION



4.0 FUNCTIONAL DESCRIPTION

4.1 Device Operation

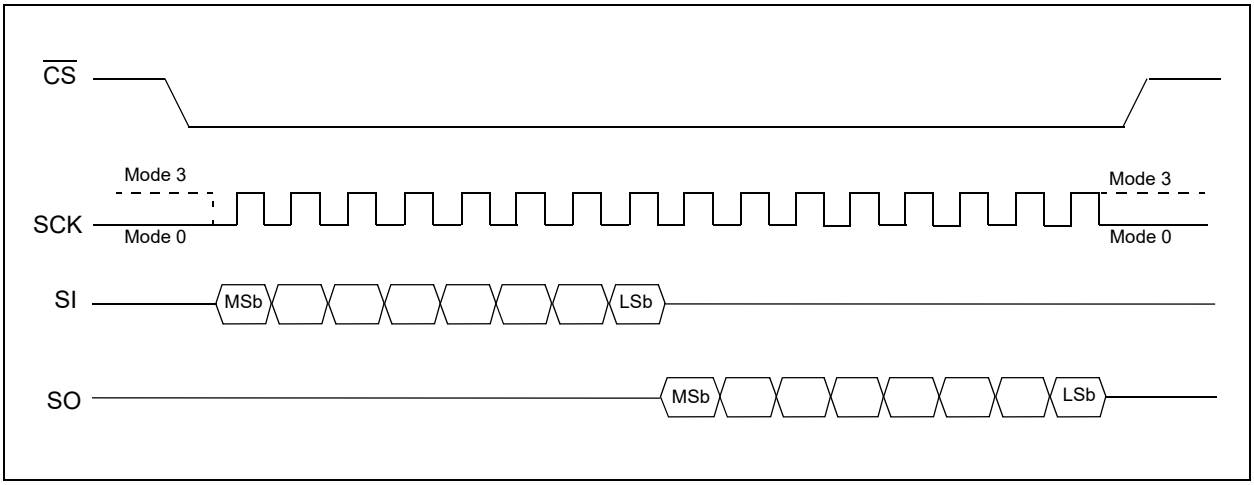
The 25CS160 is controlled by a set of instructions that are sent from a host controller, commonly referred to as the SPI host. The SPI host communicates with the 25CS160 via the SPI bus, which is comprised of four signal lines:

- Chip Select ($\overline{CS}$)
- Serial Clock (SCK)
- Serial Input (SI)
- Serial Output (SO)

The SPI protocol defines a total of four modes of operation (Mode 0, 1, 2 or 3), with each mode differing in respect to the SCK polarity and phase and how the polarity and phase control the flow of data on the SPI bus. The 25CS160 supports the two most common modes, SPI Modes 0 and 3. With SPI Modes 0 and 3, data are always latched in on the rising edge of SCK and always output on the falling edge of SCK. The only difference between SPI Modes 0 and 3 is the polarity of the SCK signal when in the inactive state (when the SPI host is in Standby mode and not transferring any data). SPI Mode 0 is defined as a low SCK while $\overline{CS}$ is not asserted (high), and SPI Mode 3 has SCK high in the inactive state. The SCK Idle state must match when the $\overline{CS}$ is deasserted both before and after the communication sequence in SPI Mode 0 and 3.

The figures in this document depict Mode 0 with a solid line on SCK while $\overline{CS}$ is inactive and Mode 3 with a dotted line.

FIGURE 4-1: SPI MODE 0 AND MODE 3



4.2 Interfacing the 25CS160 on the SPI Bus

Communication to and from the 25CS160 must be initiated by the SPI host device. The SPI host device must generate the serial clock for the 25CS160 on the SCK pin. The 25CS160 always operates as a client because the Serial Clock pin (SCK) is always an input.

4.2.1 SELECTING THE DEVICE

The 25CS160 is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the SO pin will remain in a high-impedance state.

4.2.2 SENDING DATA TO THE DEVICE

The 25CS160 uses the Serial Data Input (SI) pin to receive information. All instructions, addresses and data input bytes are clocked into the device with the Most Significant bit (MSb) first. The SI pin begins sampling on the first rising edge of the SCK line after the $\overline{CS}$ has been asserted.

4.2.3 RECEIVING DATA FROM THE DEVICE

Data output from the device is transmitted on the Serial Data Output (SO) pin with the MSb output first. The SO data are latched on the falling edge of the first SCK clock cycle after the instruction and address bytes, if necessary, have been clocked into the device.

4.3 Device Opcodes

4.3.1 SERIAL OPCODE

After the device is selected by driving $\overline{CS}$ low, the first byte sent must be the opcode that defines the sequence to be performed.

The 25CS160 utilizes an 8-bit instruction register. The list of instructions and their operation codes or opcodes are contained in Table 4-1. All instructions, addresses and data are transferred with the MSb first and are initiated with a high-to-low $\overline{CS}$ transition.

TABLE 4-1: INSTRUCTION SET FOR 25CS160

Instruction	Instruction Description	Opcode		Address Bytes	Data Bytes	Reference Section
STATUS Register Instructions						
RDSR	Read STATUS Register	05h	0000 0101	0	1 or 2	6.2
WREN	Set Write Enable Latch (WEL)	06h	0000 0110	0	0	5.1
WRDI	Reset Write Enable Latch (WEL)	04h	0000 0100	0	0	5.2
WRSR	Write STATUS Register	01h	0000 0001	0	1 or 2	6.3
EEPROM and Security Register Instructions						
READ	Read from EEPROM Array	03h	0000 0011	2	1+	7.1
WRITE	Write to EEPROM Array (1 to 32 bytes)	02h	0000 0010	2	1+	8.0
RDEX	Read from the Security Register	83h	1000 0011	2	1+	9.1
WREX	Write to the Security Register	82h	1000 0010	2	1+	9.2
LOCK	Lock the Security Register (permanent)	82h	1000 0010	2	1	9.2.1
CHLK	Check Lock Status of Security Register	83h	1000 0011	2	1	9.2.2
Identification Register Instructions						
SPID	Read the SPI Manufacturer ID Data	9Fh	1001 1111	0	5	11.1
Undervoltage Lockout Register Instructions						
RUVL	Read the Undervoltage Lockout Register	15h	0001 0101	0	1	10.2.1
WUVL	Write Undervoltage Lockout Register	11h	0001 0001	0	1	10.2.2
Device Reset Instruction						
SRST	Software Device Reset	7Ch	0111 1100	0	0	1.1.2

4.4 Hold Function

The $\overline{HOLD}$ pin is used to pause the serial communication with the device without having to stop or reset the clock sequence. Hold mode, however, does not affect the internal write cycle. Therefore, if a write cycle is in progress, asserting the $\overline{HOLD}$ pin will not pause the operation, and the write cycle will continue until it is finished.

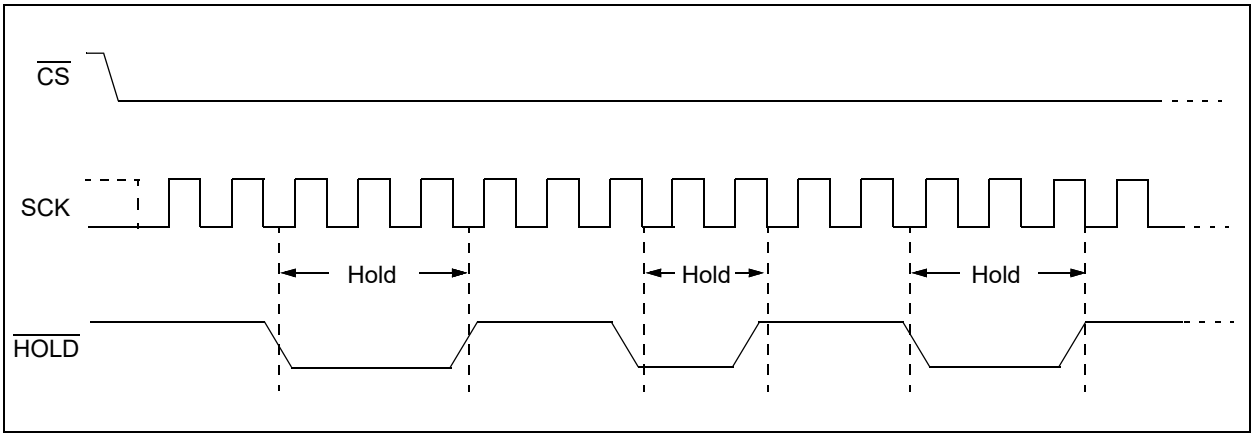
Hold mode can only be entered while the $\overline{CS}$ pin is asserted. Hold mode is activated by asserting the $\overline{HOLD}$ pin during the SCK low pulse. If the $\overline{HOLD}$ pin is asserted during the SCK high pulse, then Hold mode will not start until the beginning of the next SCK low pulse. The device will remain in Hold mode as long as the $\overline{HOLD}$ and $\overline{CS}$ pins are asserted.

While in Hold mode, the SO pin will be in a high-impedance state. In addition, both the SI pin and the SCK pin will be ignored. The $\overline{WP}$ pin, however, can still be asserted or deasserted while in Hold mode.

To end Hold mode and resume serial communication, the $\overline{HOLD}$ pin must be deasserted during the SCK low pulse. If the $\overline{HOLD}$ pin is deasserted during the SCK high pulse, then Hold mode will not end until the beginning of the next SCK low pulse.

If the $\overline{CS}$ pin is deasserted while the $\overline{HOLD}$ pin is still asserted, then any sequence that may have been started will be aborted.

FIGURE 4-2: HOLD MODE



4.5 Write Protection

The EEPROM array can only be programmed in accordance with how the Block Protect bits in the STATUS register are programmed. Refer to **Section 6.1.2 “Block Write-Protect Bits”** for details.

Additionally, the contents of the STATUS register can be protected by enabling the Write-Protect Enable (WPEN) bit in the STATUS register.

When the WPEN function is enabled, the STATUS register contents will be protected when the $\overline{WP}$ pin is asserted (low). Details about the WPEN function are provided in **Section 6.1.1 “Write-Protect Enable Bit”**.

5.0 WRITE ENABLE AND DISABLE

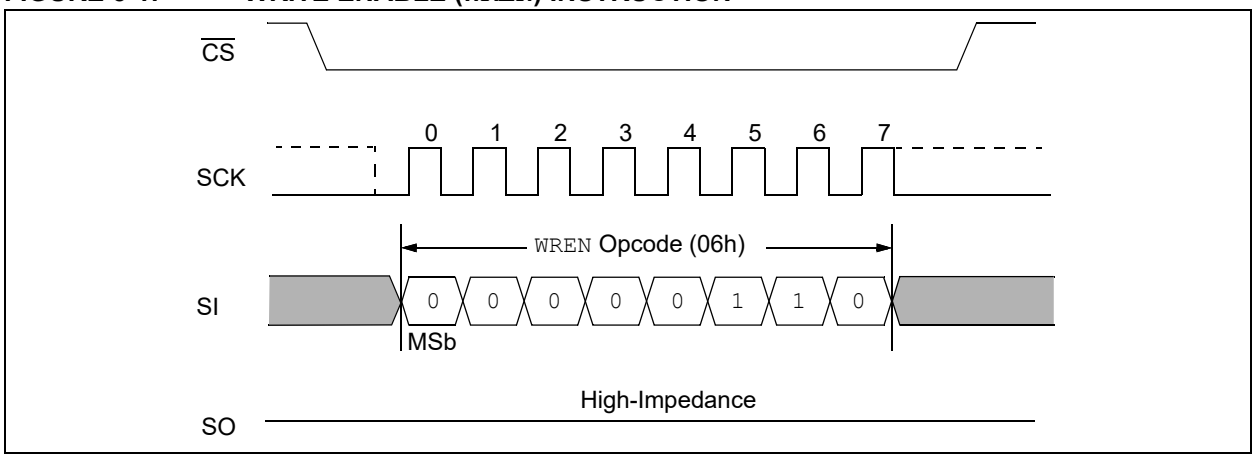
5.1 Write Enable Instruction (WREN)

The Write Enable Latch (WEL) bit of the STATUS register must be set to a logic '1' prior to each WRSR, WRITE, WREX, or LOCK instruction. The WEL bit is set to a logic '1' by sending a WREN (06h) instruction to the 25CS160. First, the $\overline{CS}$ pin is driven low to select the device, and then a 06h instruction is clocked in on the SI pin. After that, the $\overline{CS}$ pin is driven high. The WEL bit will be immediately updated in the STATUS register to a logic '1'.

The WEL bit will be reset to a logic '0' in the following circumstances:

- Upon power-up, as the power-on default condition is in the Write Disable state (**Section 1.2.2 "Device Factory Default Condition"**)
- Upon the successful completion of any write sequence (WRITE, WRSR, WREX)
- Upon execution of a Write Disable (WRDI) instruction (**Section 5.2 "Write Disable (WRDI) Instruction"**)
- Upon execution of a Software Device Reset (SRST) instruction

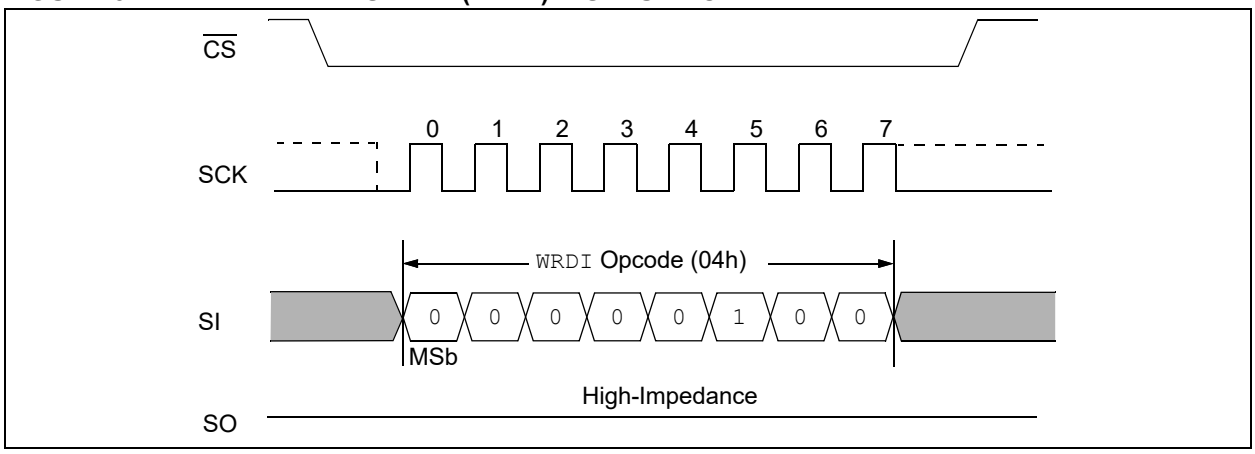
FIGURE 5-1: WRITE ENABLE (WREN) INSTRUCTION



5.2 Write Disable (WRDI) Instruction

To protect the device against inadvertent write sequences, the Write Disable (04h) instruction disables all programming modes by setting the WEL bit to a logic '0'. The WRDI instruction is independent of the $\overline{WP}$ pin state.

FIGURE 5-2: WRITE DISABLE (WRDI) INSTRUCTION



6.0 STATUS REGISTER

6.1 STATUS Register Bit Definition

The 25CS160 includes a 2-byte STATUS register, which is a combination of six nonvolatile bits of EEPROM and six volatile latches. The STATUS register bits modulate various features of the device, as shown in Register 6-1 and Register 6-2. These bits can be read or modified by specific instructions that are detailed in the subsequent sections.

REGISTER 6-1: STATUS REGISTER (BYTE 0)

R/W	U-0	U-0	U-0	R/W	R/W	R-0	R-0
WPEN	—	—	—	BP1	BP0	WEL	$\overline{\text{RDY}}$/BSY
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **WPEN:** Write-Protect Enable
1 = Write-Protect pin is enabled
0 = Write-Protect pin is ignored

bit 6-4 **Unimplemented:** Read as ‘0’

bit 3-2 **BP[1:0]:** Block Protection (see Table 6-2)
00 = No array write protection
01 = Upper quarter memory array protection
10 = Upper half memory array protection
11 = Entire memory array protection

bit 1 **WEL:** Write Enable Latch
1 = WREN instruction has been executed, and device is enabled for writing
0 = Device is not write-enabled

bit 0 **$\overline{\text{RDY}}$/BSY:** $\overline{\text{Ready}}$/Busy Status Latch
1 = Device is busy with an internal write cycle
0 = Device is ready for a new sequence

REGISTER 6-2: STATUS REGISTER (BYTE 1)

U-0	R-0	U-0	U-0	U-0	R-0	U-0	R-0
—	ECS	—	—	—	WLS	—	$\overline{\text{RDY}}$/BSY
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **ECS:** Error Correction State Latch
1 = The previous executed read sequence did require the Error Correction Code (ECC)
0 = The previous executed read sequence did not require the Error Correction Code (ECC)

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **WLS:** Write Lockout State
1 = The previous nonvolatile write sequence was blocked by the UVLO
0 = The previous nonvolatile write sequence was not blocked by the UVLO

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **$\overline{\text{RDY}}$/BSY:** $\overline{\text{Ready}}$/Busy Status Latch
1 = Device is busy with an internal write cycle
0 = Device is ready for a new sequence

6.1.1 WRITE-PROTECT ENABLE BIT

The Write-Protect Enable (WPEN) bit in the STATUS register (bit 7, byte 0) can be used in conjunction with the $\overline{\text{WP}}$ pin to inhibit writing to the various registers within the device.

The device is hardware write-protected when *both* the $\overline{\text{WP}}$ pin is low and the WPEN bit has been set to a logic ‘1’.

TABLE 6-1: WRITE-PROTECT FUNCTIONALITY MATRIX

Write Protection Mode	$\overline{\text{WP}}$ Pin	WPEN Bit	STATUS Register	UVLO Register
Legacy	Low	0	Not Protected	Not Protected
	Low	1	Protected	Protected
	High	X	Not Protected	Not Protected

Note 1: When the WPEN bit is a logic ‘1’, it cannot be changed back to a logic ‘0’ as long as the $\overline{\text{WP}}$ pin is asserted (low).

When the device is hardware write-protected, the nonvolatile bits of the STATUS register (WPEN, BP1, BP0) become read-only and the Write STATUS Register (WRSR), Lock the Security Register (LOCK) and Writing the Undervoltage Lockout Detector (WUVL) instructions will not be accepted.

6.1.2 BLOCK WRITE-PROTECT BITS

The 25CS160 contains four levels of EEPROM write protection using the Block Protection function. The nonvolatile Block Write-Protect bits (BP1, BP0) are located in bits three and two of the first STATUS register byte and define the region of the EEPROM and Security register that is to be treated as read-only.

The four levels of array protection are:

- **Level 0**: No portion of the EEPROM is protected, while the lower 32 bytes of the Security register are read-only.
- **Level 1**: The upper quarter address range is write-protected, meaning the highest order 4 Kbits in the EEPROM are read-only. The lower 32 bytes of the Security register are read-only.
- **Level 2**: The upper half address range is write-protected, meaning the highest order 8 Kbits in the EEPROM are read-only. The lower 32 bytes of the Security register are read-only.
- **Level 3**: Both the EEPROM and Security register are write-protected, meaning all addresses are read-only.

The address ranges that are protected for each Block Write Protection level and corresponding STATUS register control bits are shown in Table 6-2.

TABLE 6-2: BLOCK WRITE-PROTECT BITS

Level	STATUS Register Byte 0 Bits [3:2]		Protected Address Range	
	BP1	BP0	Memory Region	25CS160
0	0	0	EEPROM	None
			Security Register	0000h-001Fh
1	0	1	EEPROM	0600h-07FFh
			Security Register	0000h-001Fh
2	1	0	EEPROM	0400h-07FFh
			Security Register	0000h-001Fh
3	1	1	EEPROM	0000h-07FFh
			Security Register	0000h-003Fh

6.1.3 WRITE ENABLE LATCH

Enabling and disabling writing to any nonvolatile register, the EEPROM array, and the Security register is accomplished through the Write Enable (WREN) instruction, as shown in **Section 5.1 "Write Enable Instruction (WREN)"**, and the Write Disable (WRDI) instruction, as shown in **Section 5.2 "Write Disable (WRDI) Instruction"**. These functions change the state of the Write Enable Latch (WEL) bit (byte 0, bit 1) in the STATUS register.

A logic '1' bit indicates that the device is currently busy performing a nonvolatile write sequence. During this time, only the Read STATUS Register (RDSR) instruction will be executed by the device.

A logic '0' bit in this position indicates the device is ready to accept new instructions.

6.1.4 $\overline{\text{READY}}$/BUSY STATUS LATCH

The $\overline{\text{Ready}}$/Busy Status Latch ($\overline{\text{RDY}}$/BSY) is used to indicate whether the device is currently active in a nonvolatile write sequence. This bit is read-only and automatically updated by the device. It is provided in bit 0 of both STATUS register bytes.

A logic '1' bit indicates that the device is currently busy performing a nonvolatile write sequence. During this time, only the Read STATUS Register (RDSR) and the Write Ready/Busy Poll (WRBP) instructions will be executed by the device.

A logic '0' bit in this position indicates the device is ready to accept new instructions.

6.1.5 ERROR CORRECTION STATE LATCH

The Error Correction State (ECS) bit indicates whether the on-chip Error Correction Code (ECC) logic scheme was invoked during the previous read sequence. For more information related to ECC, refer to **Section 8.2 "Error Correction Code (ECC) Architecture"**.

The ECS bit will be set to logic '0' unless the previously executed read sequence required the use of the ECC logic scheme. When this occurs, the ECS bit will be set to logic '1'.

The ECS bit will continue to read a logic '1' until another read sequence occurs where the use of the ECC logic scheme is not required, a Power-On Reset (POR) event occurs or a Software Device Reset (SRST) instruction is sent to the 25CS160.

6.1.6 WRITE LOCKOUT STATE BIT

The Write Lockout State (WLS) bit is located in byte 1, bit 2 of the STATUS register. This bit indicates whether the last write sequence was inhibited by the UVLO detection circuit (see **Section 10.0 "Programmable UnderVoltage Lockout"**).

A logic '1' in this bit position indicates that the previous write sequence was inhibited by UVLO. A logic '0' indicates the previous write sequence was not inhibited by UVLO.

The WLS bit will continue to read out a logic '1' until one of the following occurs:

- A Power-On Reset (POR) event occurs (**Section 1.1.1 "Device Power-On Reset"**)
- A nonvolatile write opcode is sent to the device (WRITE, WRSR, WREX, LOCK, WUVL)
- A Software Device Reset (SRST) instruction is executed

Note:	The Write Lockout State (WLS) bit is only valid if the undervoltage lockout function is enabled.

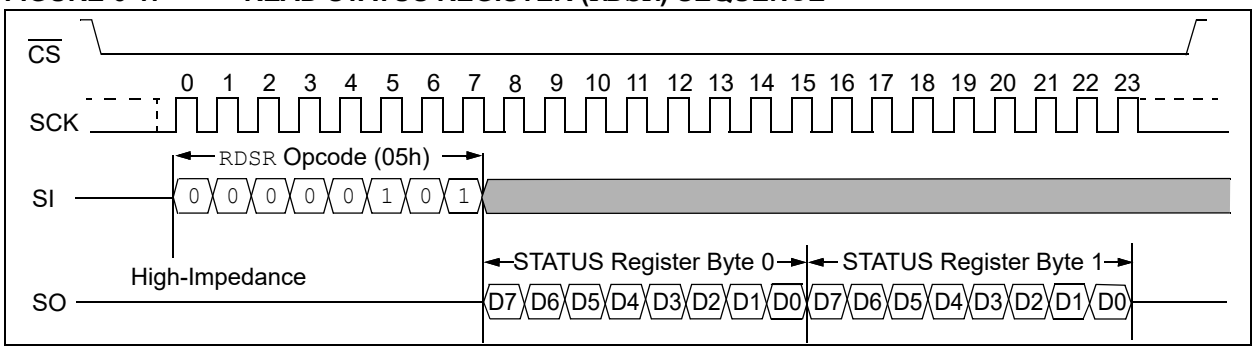
6.2 Read STATUS Register (RDSR)

The Read STATUS Register (RDSR) instruction provides access to the contents of the STATUS register. The STATUS register is read by asserting the $\overline{\text{CS}}$ pin and then sending a 05h opcode. The device will return the 16-bit STATUS register value on the SO pin.

The STATUS register can be continuously read for data by continuing to read beyond the first 8-bit value returned. The 25CS160 will update the value of the $\overline{\text{RDY}}$/BSY and WEL bits in the STATUS register upon the completion of every eight bits, thereby allowing new STATUS register values to be read without having to issue a new RDSR instruction.

A new RDSR instruction needs to be initiated for the nonvolatile bits (WPEN, BP0 and BP1) in the STATUS register to be updated.

FIGURE 6-1: READ STATUS REGISTER (RDSR) SEQUENCE



6.3 Write STATUS Register (WRSR)

The Write STATUS Register (WRSR) instruction enables the SPI host to change selected bits of the STATUS register. Before a WRSR sequence can be initiated, a WREN instruction must be executed to set the WEL bit to logic '1'. Upon completion of a WREN instruction, a WRSR sequence can be executed.

The WRSR instruction will only modify:

- Byte 0: bit 7, bit 3 and bit 2

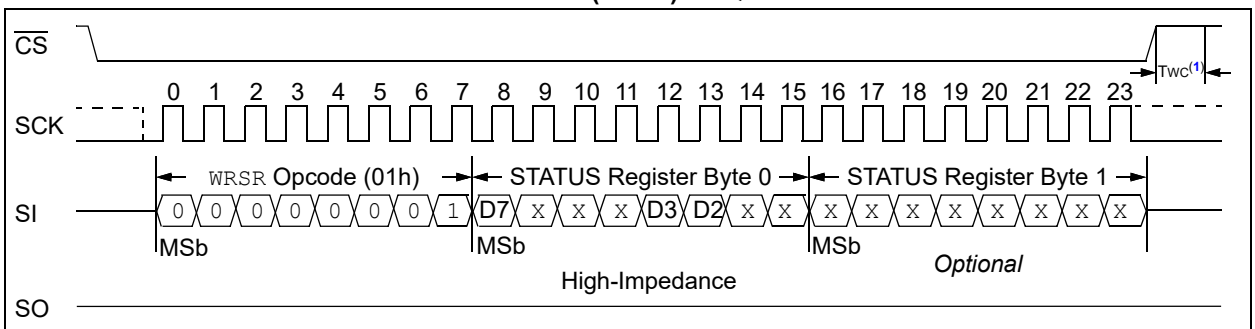
These modifiable bits are the Write-Protect Enable (WPEN) bit and the Block Protect (BP1, BP0) bits.

These three bits are nonvolatile and have the same properties and functions as regular EEPROM bits. Their values are retained while power is removed from the device.

Note:	If the $\overline{CS}$ pin is deasserted anywhere other than the end of an 8-bit byte boundary, the sequence will be aborted, and no write cycle will take place.

The 25CS160 will not respond to instructions other than a RDSR or a WRSR sequence until the self-timed internal write cycle has completed. When the write cycle has completed, the WEL bit in the STATUS register is reset to a logic '0'.

FIGURE 6-2: WRITE STATUS REGISTER (WRSR) SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

7.0 READ SEQUENCES

7.1 Reading from the EEPROM

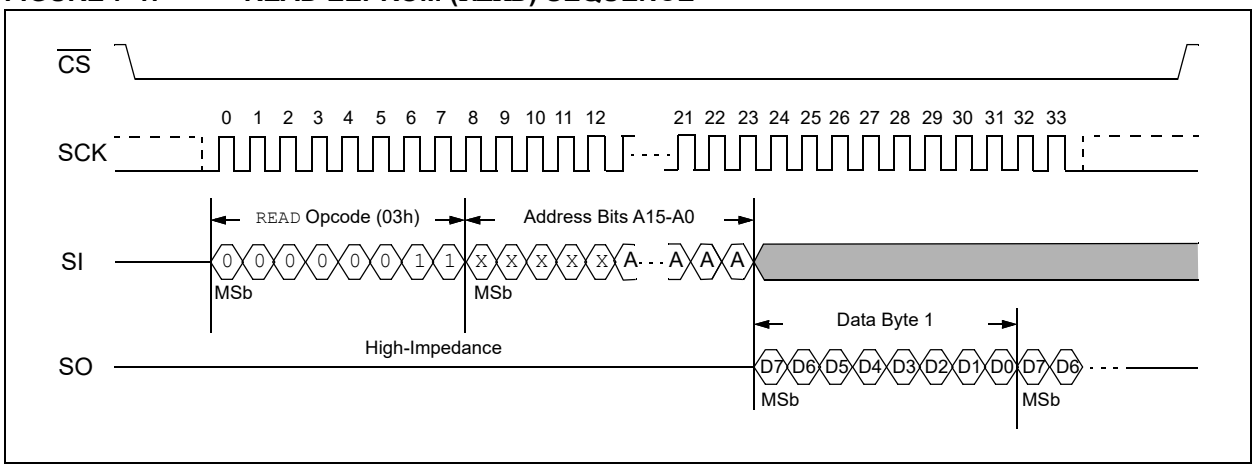
Reading the EEPROM contents can be done whenever the device is not in an internal write cycle, as indicated by the Ready/Busy bit of the STATUS register. To read the EEPROM, the CS line is pulled low to select the device, and the READ (03h) instruction is transmitted via the SI line, followed by the 16-bit address to be read. Address bits A15 through A11 are “don't care” bits because they do not fall within the addressable memory range.

Upon completion of the 16-bit address, any data on the SI line will be ignored. The data (D7–D0) at the specified address are then shifted out onto the SO line. If only one byte is to be read, the CS line should be driven high after the data are clocked out.

The read sequence can be continued since the byte address is automatically incremented, and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address (0000h), allowing the entire memory to be read in one continuous read cycle, regardless of the starting address.

The read sequence can be terminated at any point in the sequence, driving CS high.

FIGURE 7-1: READ EEPROM (READ) SEQUENCE



8.0 WRITE SEQUENCES

To program the EEPROM in the 25CS160, the device must be write-enabled via the Write Enable (WREN) instruction. If the device is not write-enabled, it will ignore the WRITE instruction and will return to the Standby state when $\overline{CS}$ is brought high. The address of the memory location(s) to be programmed must be outside the protected address range(s) selected by the Block Write Protection level. During an internal write cycle, all instructions will be ignored except the RDSR instruction.

8.1 Write Instruction Sequences

8.1.1 BYTE WRITE

Once a WREN instruction has been completed, a byte write sequence can be performed, as shown in Figure 8-1. After the $\overline{CS}$ line is pulled low to select the device, the WRITE (02h) instruction is transmitted via the SI line, followed by the 16-bit address and the data (D7-D0) to be programmed.

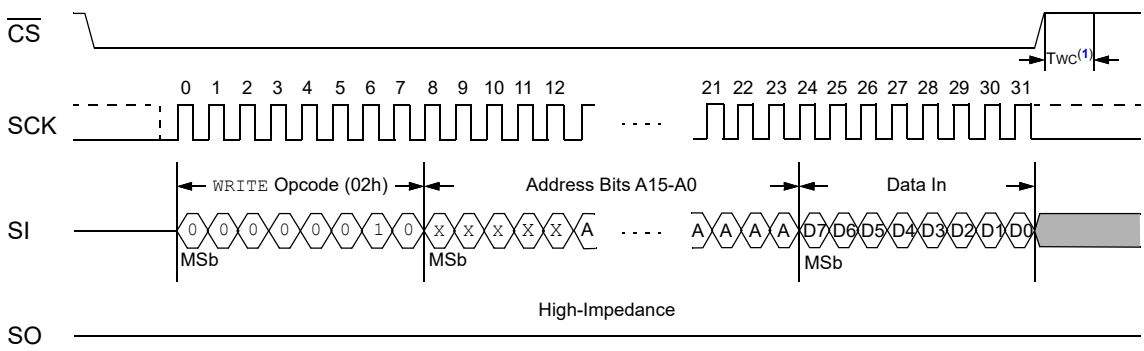
Address bits A15 through A11 are “don't care” bits because they do not fall within the addressable memory range.

Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low time (Mode 0) and SCK high time (Mode 3) immediately after clocking in the D0 (LSB) data bit.

Note:	If the $\overline{CS}$ pin is deasserted anywhere other than at the end of an 8-bit byte boundary, the sequence will be aborted, and no write cycle will take place.

The 25CS160 is automatically returned to the Write Disable state (STATUS register bit WEL = 0) at the completion of a write cycle.

FIGURE 8-1: BYTE WRITE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

8.1.2 PAGE WRITE

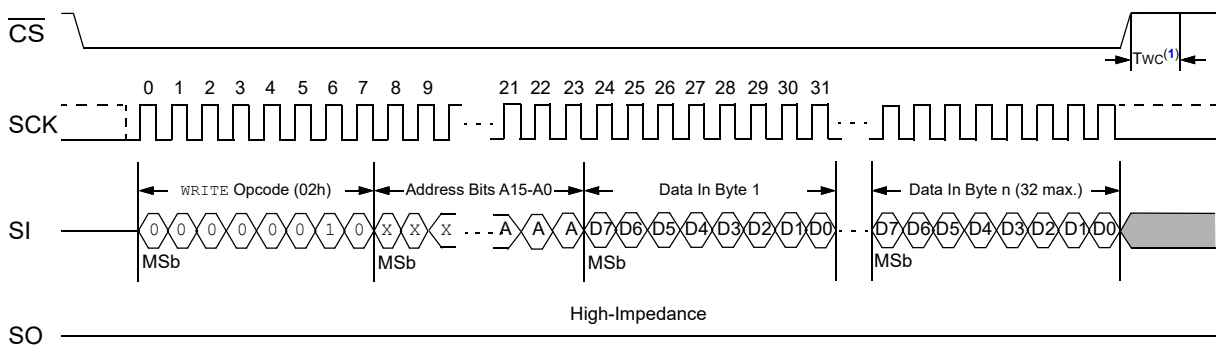
A page write sequence is the same as a byte write; however, it allows up to 32 bytes to be written in the same write cycle, provided that all bytes are in the same page of the memory array (where addresses A10 through A5 are the same). Partial page writes of less than 32 bytes are allowed. After each byte of data is received, the five lowest order address bits are internally incremented by one, and the remaining address bits remain constant.

If more bytes of data are transmitted than will fit at the end of that memory page, the address counter will roll over to the beginning of the same page, and only the last 32 bytes of data received will be written to the device.

Upon completion of a write cycle, the 25CS160 automatically returns to the Write Disable state (STATUS register bit WEL = 0).

Note:	If the $\overline{CS}$ pin is deasserted anywhere other than at the end of an 8-bit byte boundary, the sequence will be aborted, and no write cycle will take place.

FIGURE 8-2: PAGE WRITE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

8.2 Error Correction Code (ECC) Architecture

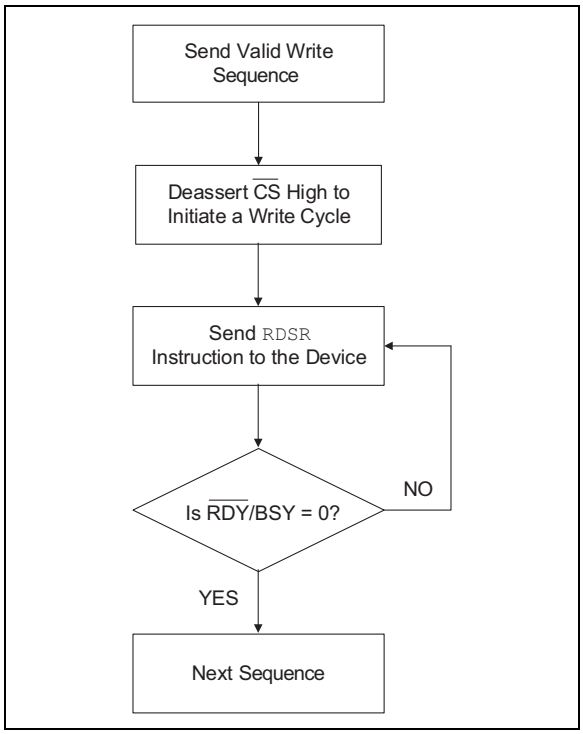
The 25CS160 incorporates a built-in Error Correction Code (ECC) logic scheme. The EEPROM array is internally organized as one byte plus an additional 4 ECC parity bits of EEPROM. These 12 bits are referred to as the internal physical data word. During a read sequence, the ECC logic compares each physical data byte with its corresponding four ECC parity bits. If a single bit out of the 1-byte region happens to read incorrectly, the ECC logic will detect the bad bit and replace it with a correct value before the data are serially clocked out. This architecture significantly improves the reliability of the 25CS160 compared to a device that does not utilize ECC.

8.3 Polling Routine

A polling routine can be implemented to optimize time-sensitive applications that would prefer not to wait the fixed maximum write cycle time (TWC). This method allows the application to query whether the Serial EEPROM has completed the write sequence. This polling routine should be initiated once the internally timed write sequence has begun.

The polling routine involves repeatedly sending the Read STATUS Register (`RDSR`) instruction to determine if the device has completed its self-timed internal write cycle (see Figure 8-3). If the $\overline{RDY}$/BSY bit = `1` from `RDSR`, the write cycle is still in progress. If $\overline{RDY}$/BSY bit = `0` from `RDSR`, this indicates the write cycle has ended. If the device is still in a busy state, the `RDSR` instruction can be repeatedly executed until the $\overline{RDY}$/BSY bit = `0`, signaling that the device is ready to execute a new instruction. Only the `RDSR` instruction is enabled during the write cycle.

FIGURE 8-3: POLLING FLOW



9.0 SECURITY REGISTER

The Security register is segmented into one 32-byte read-only page and one 32-byte user-programmable, lockable ID page. The user-programmable, lockable ID page supports both byte write and page write sequences. The user-programmable, lockable ID page may be permanently locked at any time with the `LOCK` instruction. The Security register lock state can be verified at any time with `CHLK` instruction.

TABLE 9-1: SECURITY REGISTER ORGANIZATION

Security Register Byte Number									
0	1	...	30	31	32	33	...	62	63
Factory-Programmed (Read-Only) 0-15: Device Serial Number 16-31: Reserved for Future Use					User-Programmable (Lockable)				

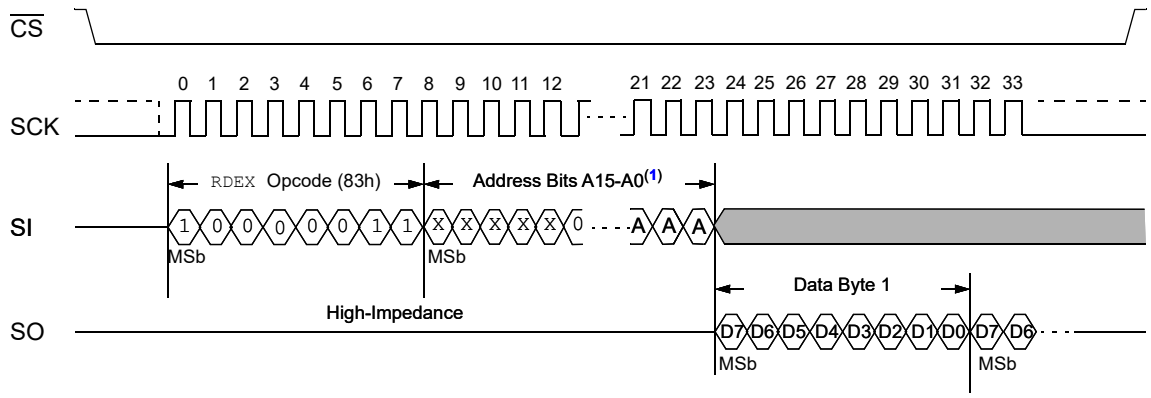
9.1 Reading from the Security Register

Reading the Security register contents from the 25CS160 follows a similar sequence to reading the EEPROM, but a different opcode and specific address data are required. To read the Security register, first drive the $\overline{CS}$ low to select the device, then send the `RDEX` (83h) instruction via the SI line, followed by the 16-bit address to be read.

> **Note:** Address bits A15 through A6 are “don't care” bits, except for A10, which must be a logic ‘`0`’.

Upon completion of the 16-bit address, any data on the SI line will be ignored. The data (D7-D0) at the specified address are then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data are output. The read sequence can be continued since the byte address is automatically incremented, and data will continue to be shifted out. When the highest address is reached (003Fh), the address counter will roll over to the lowest address (0000h), allowing the entire Security register to be read in one continuous read cycle regardless of the starting address.

FIGURE 9-1: READ SECURITY REGISTER (`RDEX`) SEQUENCE



Note 1: Address bit A10 must be logic ‘`0`’ to read the Security register.

9.1.1 READING THE FACTORY-PROGRAMMED 128-BIT SERIAL NUMBER

The Security register contains a factory-programmed, globally unique, read-only 128-bit serial number. This serial number is unique across all varieties of Microchip CS series EEPROM, and it is located in the lower 16 bytes of the Security register (bytes 0h-Fh). Reading the serial number is accomplished in the same way as the reading of any other data in the Security register.

Note:	To ensure a unique number, the 128-bit serial number must be read from the starting address. Additionally, the entire serial number must be read to realize a completely unique value.

9.2 Writing to the Security Register

Executing a write sequence to the Security register is identical to writing to the EEPROM, as described in **Section 8.1.1 "Byte Write"** and **Section 8.1.2 "Page Write"**, with the exception that the `WREX` (82h) instruction is used while A10 must be a logic '`0`' and A5 must be a logic '`1`' to write the user-programmable, lockable ID page. In Legacy Write Protection mode, the Security register is write-protected when the BP[1:0] bits (bits 3-2, byte 0) of the STATUS register = `11`. There is no dependency on the WPEN bit (bit 7, byte 0) of the STATUS register or the $\overline{\text{WP}}$ pin.

The user-programmable, lockable ID page of the Security register can also be permanently locked, making its contents read-only. This is accomplished with the `LOCK` instruction. The `CHLK` instruction can determine if the device has been previously locked. If the Security register is locked, any subsequent `WREX` instructions will be ignored.

Note:	If the $\overline{\text{CS}}$ pin is deasserted anywhere other than at the end of an 8-bit byte boundary, the sequence will be aborted, and no write cycle will take place.

9.2.1 LOCKING THE SECURITY REGISTER

The upper 32 bytes of the Security register are shipped by Microchip in a user-programmable state. Once the desired data are written, the user-programmable, lockable ID page of the Security register can be permanently write-protected with the `LOCK` instruction.

Note:	The `LOCK` instruction will be ignored if the WPEN bit (bit 7, byte 0) of the STATUS register is set to a logic '`1`' and the $\overline{\text{WP}}$ pin is asserted.

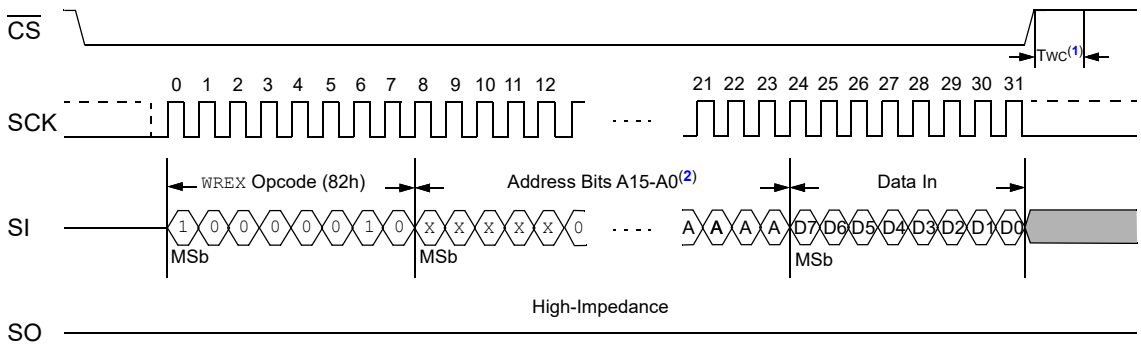
The `LOCK` instruction is irreversible and will permanently prevent all future write sequences to the upper 32 bytes of the Security register on the 25CS160, thereby rendering the entire 64-byte Security register read-only.

Note:	Once the Security register has been locked, *it is not possible to unlock it*.

The `LOCK` instruction emulates a write sequence in that a `WREN` instruction must first be sent to set the WEL bit in the STATUS register to logic '`1`'. As shown in Figure 9-4, the `LOCK` (82h) instruction is clocked in on the SI line, followed by a dummy address where bits A15 through A0 are "don't care" bits, with the exception that bit A10 must be set to logic '`1`'. Finally, a confirmation data byte of `xxxxxx1xb` is sent, and the self-timed internal write cycle will begin once the $\overline{\text{CS}}$ pin is driven high.

Note:	If the $\overline{\text{CS}}$ pin is deasserted before the end of the 32-bit sequence, the sequence will be aborted, and no write cycle will take place.

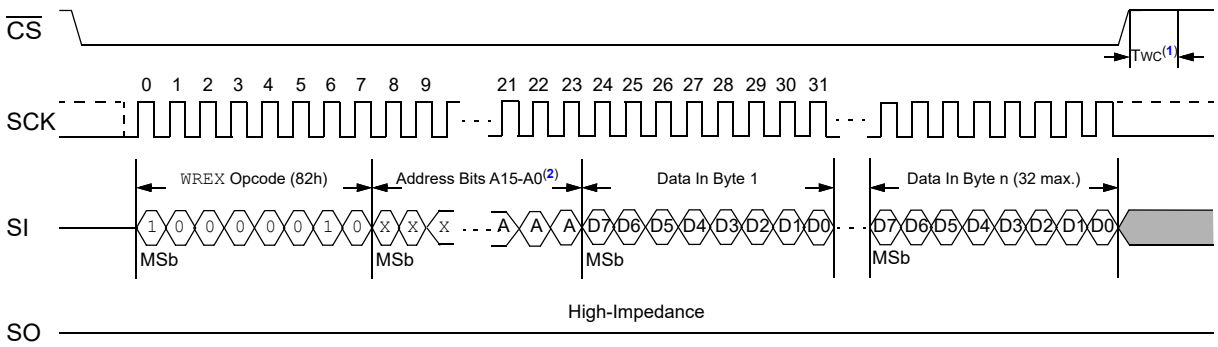
FIGURE 9-2: WRITE SECURITY REGISTER (WREX) BYTE WRITE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

2: A15 through A6 are "don't care" bits, except for A10, which must be a logic '0', and A5, which must be a logic '1', in order to write to the user-programmable, lockable ID page.

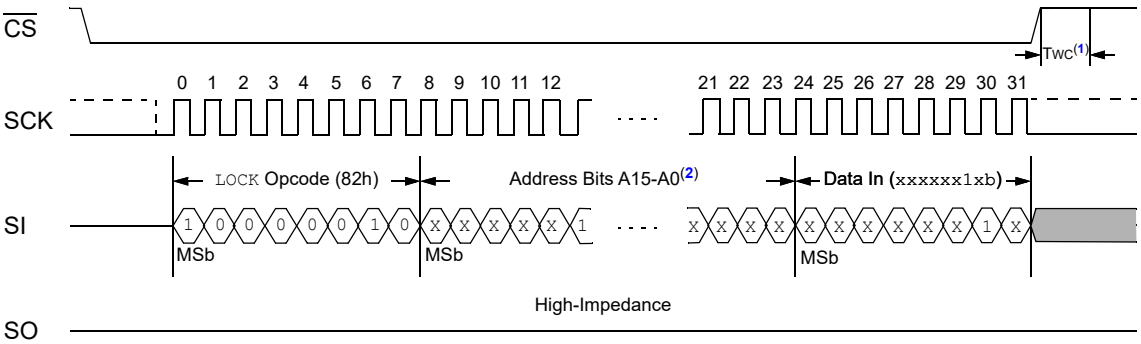
FIGURE 9-3: WRITE SECURITY REGISTER (WREX) PAGE WRITE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

2: A15 through A6 are "don't care" bits, except for A10 which must be a logic '0', and A5, which must be a logic '1', in order to write to the user-programmable, lockable ID page.

FIGURE 9-4: LOCK SECURITY REGISTER (LOCK) SEQUENCE



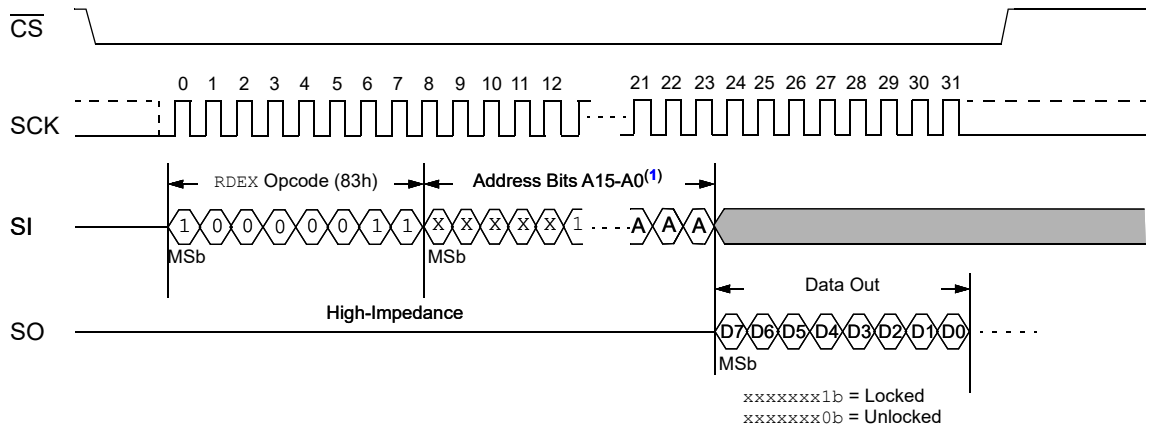
Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

2: A15 through A0 are "don't care" bits, except for A10, which must be a logic '1'.

9.2.2 DETERMINING THE LOCK STATE OF THE SECURITY REGISTER

To determine whether or not the user-programmable, lockable ID page of the Security register is locked, the 25CS160 includes a `CHLK` instruction. To determine the lock status, the opcode 83h must be clocked into the device on the SI line. The address bit A10 must be equal to logic '`1`', while the other address bits are "don't care". Data bit 0 of the data byte clocked out on the SO line determines the lock state; the other bits of the data byte are "don't care" bits. A data response of `xxxxxxx1b` indicates the region is locked, while a `xxxxxxx0b` response indicates that the region is not locked.

FIGURE 9-5: CHECK SECURITY REGISTER LOCK (`CHLK`) SEQUENCE



Note 1: A15 through A0 are "don't care" bits, except for A10, which must be a logic '`1`'.

10.0 PROGRAMMABLE UNDERVOLTAGE LOCKOUT

The 25CS160 is equipped with an undervoltage lockout detection circuit, which looks for brown-out events or device VCC power supply levels deemed too low for a given application.

To prevent spurious application events that could negatively affect the EEPROM contents of the device, the 25CS160 employs a circuit that monitors the VCC line voltage. Because the safe power supply voltage level will vary by application, the threshold that defines a brown-out event can be modified in the device from the default level.

10.1 Undervoltage Lockout Detection Register

The 25CS160 contains a nonvolatile, 8-bit Undervoltage Lockout Detection (UVLO) register that can be modified to change the undervoltage detection threshold (VUVL). When the detector is enabled (bit 5 must be set to logic '1'), the device will sample the VCC supply level upon the detection of the $\overline{CS}$ pin going high (which starts the internal write cycle) and compare it to VUVL. If VCC remains below VUVL for the minimum UVLO detection time (TUVL) after the CS goes high, the UVLO detection circuit will inhibit the write operation. The WLS bit in the STATUS register can be checked to determine if the previous write sequence was inhibited. If the WLS bit is a logic '1', VCC was less than VUVL, and the previous write sequence was inhibited. The WLS bit is only valid if the UVLO function is enabled. See **Section 6.0 "STATUS Register"** for more details.

The instructions that will be inhibited include the following:

- WRITE, WRSR, WREX, LOCK, WUVL

The UVLO register has one bit (UVLOEN) that controls if the undervoltage detection function is enabled. Five other bits (VUVL[4:0]) determine the undervoltage threshold level. Refer to Table 1-1 for the specific threshold levels.

The STATUS register contains a volatile bit called Write Lockout State (WLS, byte 1, bit 2). In the event that a write sequence to nonvolatile memory is inhibited by the undervoltage lockout detector circuit, the WLS bit will read out as a logic '1'.

The WLS bit will continue to read out a logic '1' until one of the following occurs:

- A Power-On Reset (POR) event occurs (**Section 1.1.1, Device Power-On Reset**)
- A nonvolatile write opcode is sent to the device (WRITE, WRSR, WREX, LOCK, WUVL)
- A Software Device Reset (SRST) instruction is executed

The organization of the register is depicted below in Register 10-1.

Note:	If the STATUS register is read during the UVLO detection time (TUVL), the device will report a busy state, indicated by RDY/BSY = 1. If the write is inhibited due to the UVLO, the RDY/BSY bit will clear, and the WLS bit will be set.

Note:	Setting the undervoltage detection threshold (VUVL) above VCC will cause all write sequences to be ignored. VCC must be above VUVL to reprogram the VUVL.

REGISTER 10-1: UNDERVOLTAGE LOCKOUT DETECTOR REGISTER

U-0	U-0	R/W	R/W	R/W	R/W	R/W	R/W
—	—	UVLOEN	VUVL4	VUVL3	VUVL2	VUVL1	VUVL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **UVLOEN:** Enable Undervoltage Lockout Function
1 = UVLO is enabled
0 = UVLO is not enabled

bit 4-0 **VUVL[4:0]:** Undervoltage Lockout Detection Level(1)
00000 = Minimum
•
•
•
11111 = Maximum

Note 1: For specific UVLO levels, refer to Table 1-1.

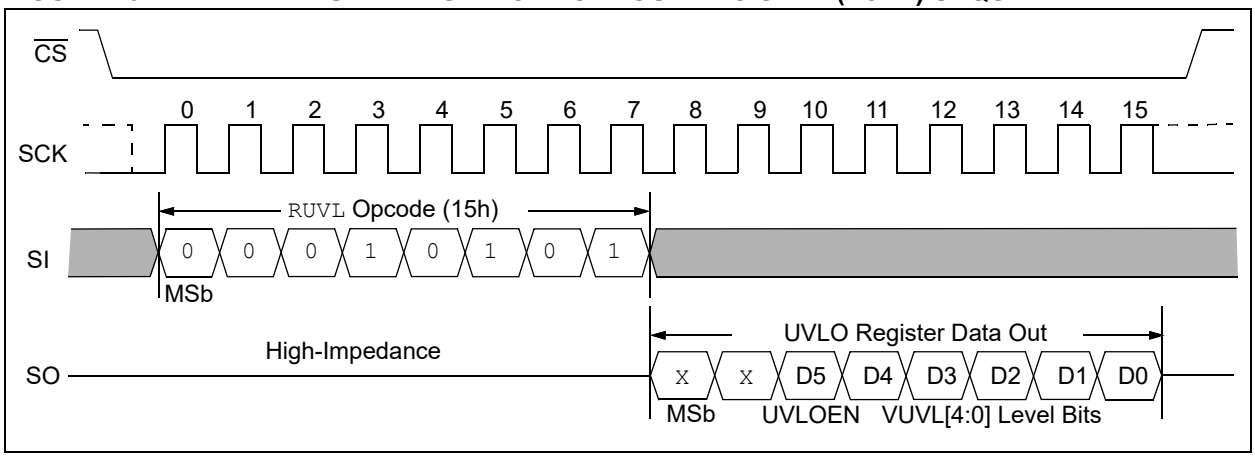
10.2 Accessing the Undervoltage Lockout Register

10.2.1 READING THE UNDERVOLTAGE LOCKOUT DETECTOR REGISTER

Reading the Undervoltage Lockout (UVLO) register is accomplished in a very similar manner to reading the STATUS register.

The UVLO register is read by asserting the $\overline{CS}$ pin, followed by sending in a 15h opcode, which corresponds to the RUVL instruction on the SI pin. Upon completion of the opcode, the device will return the 8-bit register value on the SO pin. The input conditions of the RUVL instruction are shown in Figure 10-1.

FIGURE 10-1: READ UNDERVOLTAGE LOCKOUT REGISTER (RUVL) SEQUENCE



10.2.2 WRITING THE UNDERVOLTAGE LOCKOUT DETECTOR REGISTER

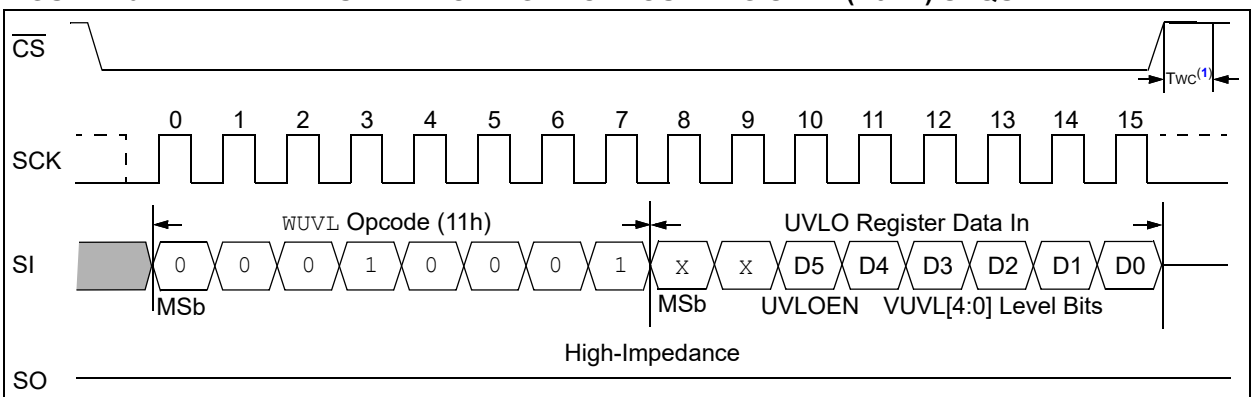
Writing to the UVLO register can be done by using the WUVL instruction. However, before a WUVL instruction can be initiated, a WREN instruction must be executed to set the WEL bit to logic '1' (see **Section 8.1.1 "Byte Write"**). The WUVL instruction is prevented if WPEN = 1 and $\overline{WP}$ is asserted. Upon completion of a WREN sequence, a WUVL instruction can be executed.

This begins by driving the $\overline{CS}$ pin low, followed by sending in an 11h opcode on the SI pin. Then continue by sending the desired 8-bit UVLO register value.

Note that bits 7 through bit 6 have no function, as shown in Register 10-1. The 25CS160 will only respond to a RDSR instruction after a WUVL sequence until the self-timed internal write cycle has completed, as the UVLO is a nonvolatile register. When the write cycle is completed, the WEL bit in the STATUS register is reset to logic '0'. The WUVL sequence is depicted in Figure 10-2.

> **Note:** If the $\overline{CS}$ pin is deasserted before the end of the 16-bit sequence, the sequence will be aborted, and no write cycle will take place.

FIGURE 10-2: WRITE UNDERVOLTAGE LOCKOUT REGISTER (WUVL) SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

11.0 IDENTIFICATION REGISTER

The Identification register contains identification information that can be read from the device to enable systems to electronically query and identify the 25CS160 while it is in system.

The identification method and the instruction opcode comply with the JEDEC® standard for “Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices”. The type of information that can be read from the device includes the JEDEC®-defined Manufacturer ID, the vendor-specific Device ID and the vendor-specific Extended Device Information (EDI).

11.1 Reading the Identification Register

To read the identification information, the $\overline{CS}$ pin must first be asserted, and the opcode of 9Fh must be clocked into the device. After the opcode has been clocked in, the device will begin outputting the identification data on the SO pin during the subsequent clock cycles. The first byte output will be the Manufacturer ID, followed by two bytes of Device ID information.

The fourth byte output will be the Extended Device Information (EDI) String Length, which, for the 25CS160, will be 01h, indicating that one byte of EDI data follows.

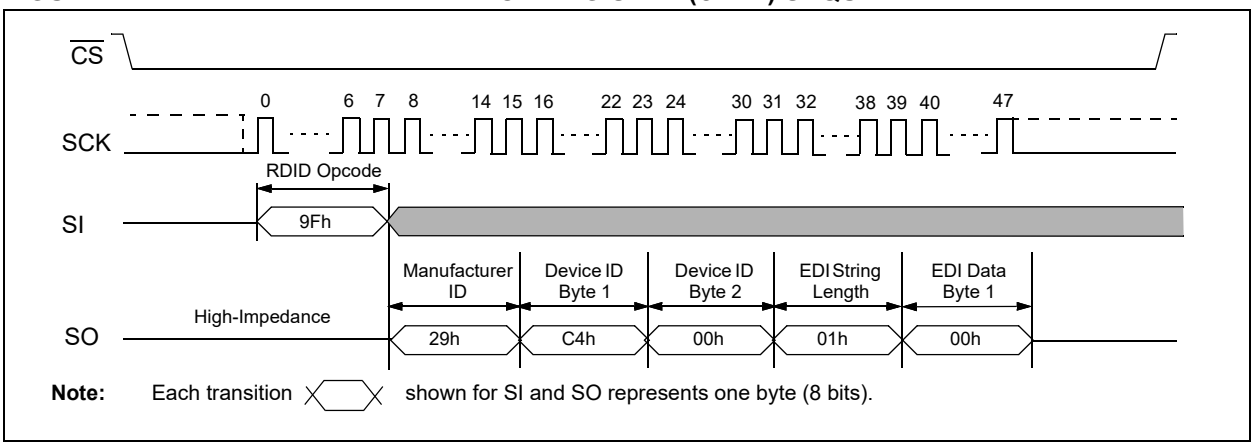
After one byte of EDI data is output, the SO pin will go into a high-impedance state; therefore, additional clock cycles will have no effect on the SO pin, and no data will be output. As indicated in the JEDEC® standard, reading the EDI String Length and any subsequent data is optional.

Deasserting the $\overline{CS}$ pin will terminate the Manufacturer and Device ID read sequence and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read. This sequence is depicted in Figure 11-1.

TABLE 11-1: IDENTIFICATION REGISTER DETAILS

Data Type	Byte No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
Manufacturer ID	1	JEDEC® Assigned Code								29h	JEDEC® Code: 0010 1001 (29h for Microchip)
		0	0	1	0	1	0	0	1		
Device ID (Part 1)	2	Family Code			Density Code						
		1	1	0	0	0	1	0	0	C4h	16-Kbit Density Code
Device ID (Part 2)	3	Sub Code			Product Variant						
		0	0	0	0	0	0	0	0	00h	Reserved for Future Use
EDI Length	4	0	0	0	0	0	0	0	1	01h	Indicates one EDI byte
EDI Byte 1 Device Revision	5	0	0	0	0	0	0	0	0	00h	First generation, SPI 16-Kbit device

FIGURE 11-1: READ IDENTIFICATION REGISTER (SPID) SEQUENCE



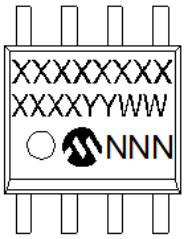
12.0 PACKAGING INFORMATION

12.1 Package Marking Information

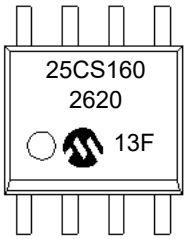
8-Lead MSOP

Example

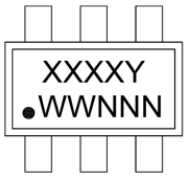
8-Lead SOIC



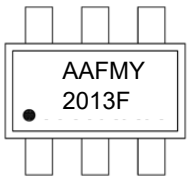
Example



6-Lead SOT-23



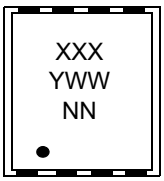
Example



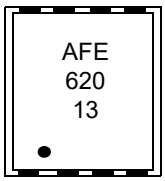
8-Lead TSSOP

Example

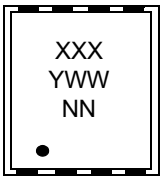
8-Lead UDFN (2x3x0.5 mm)



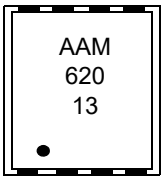
Example



8-Lead VDFN



Example



Part Number	1st Line Marking Codes					
	MSOP	SOIC	SOT-23	TSSOP	UDFN	VDFN
25CS160	5CS160	25CS160	AAFMY	AAER	AFE	AAM

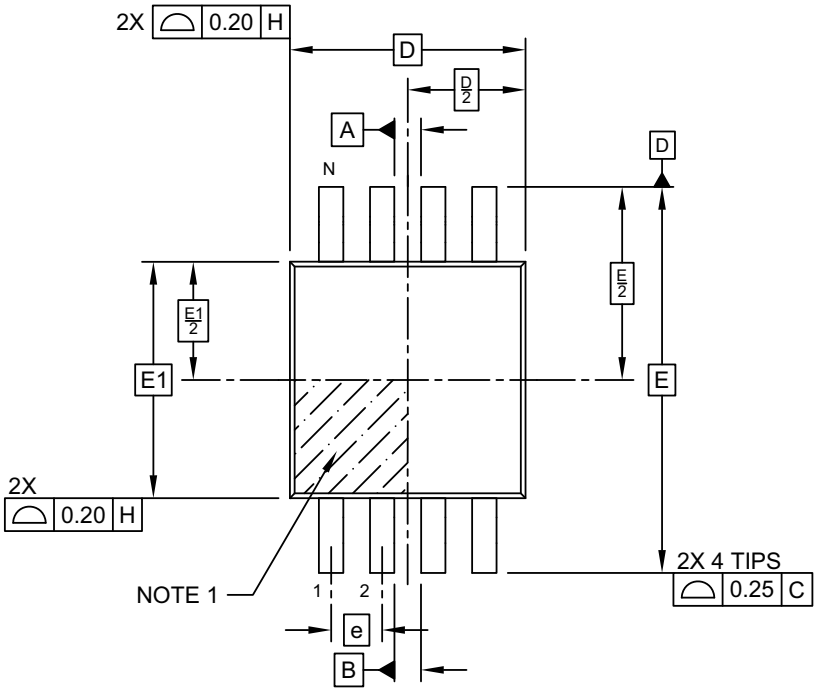
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code
*	This package is RoHs compliant. The JEDEC® designator can be found on the outer packaging for this package.

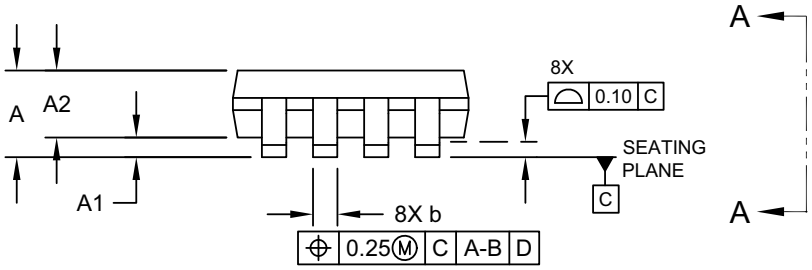
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

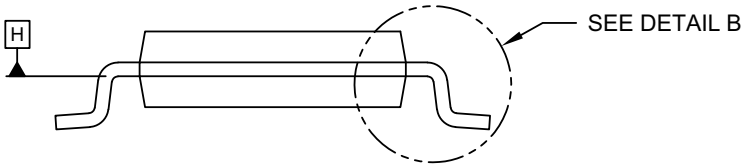
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

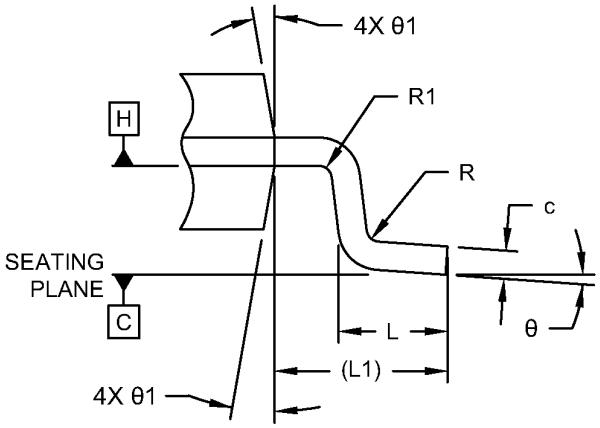


VIEW A–A

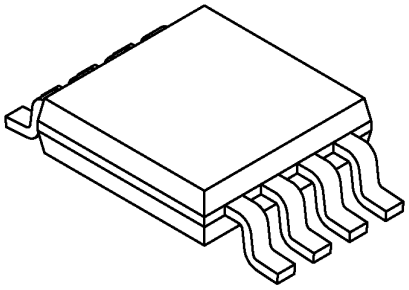
Microchip Technology Drawing C04-111-MS Rev F Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D	3.00 BSC		
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

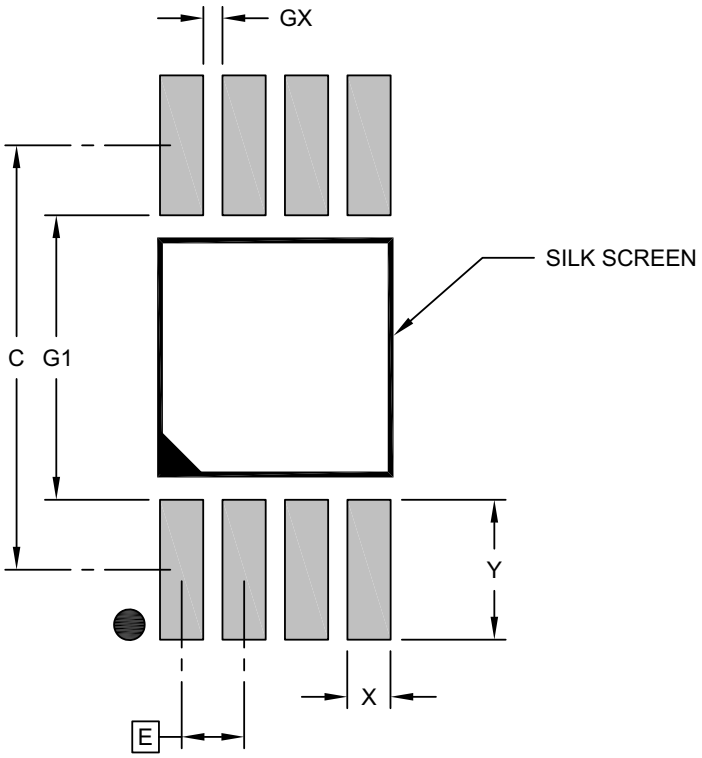
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev F Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

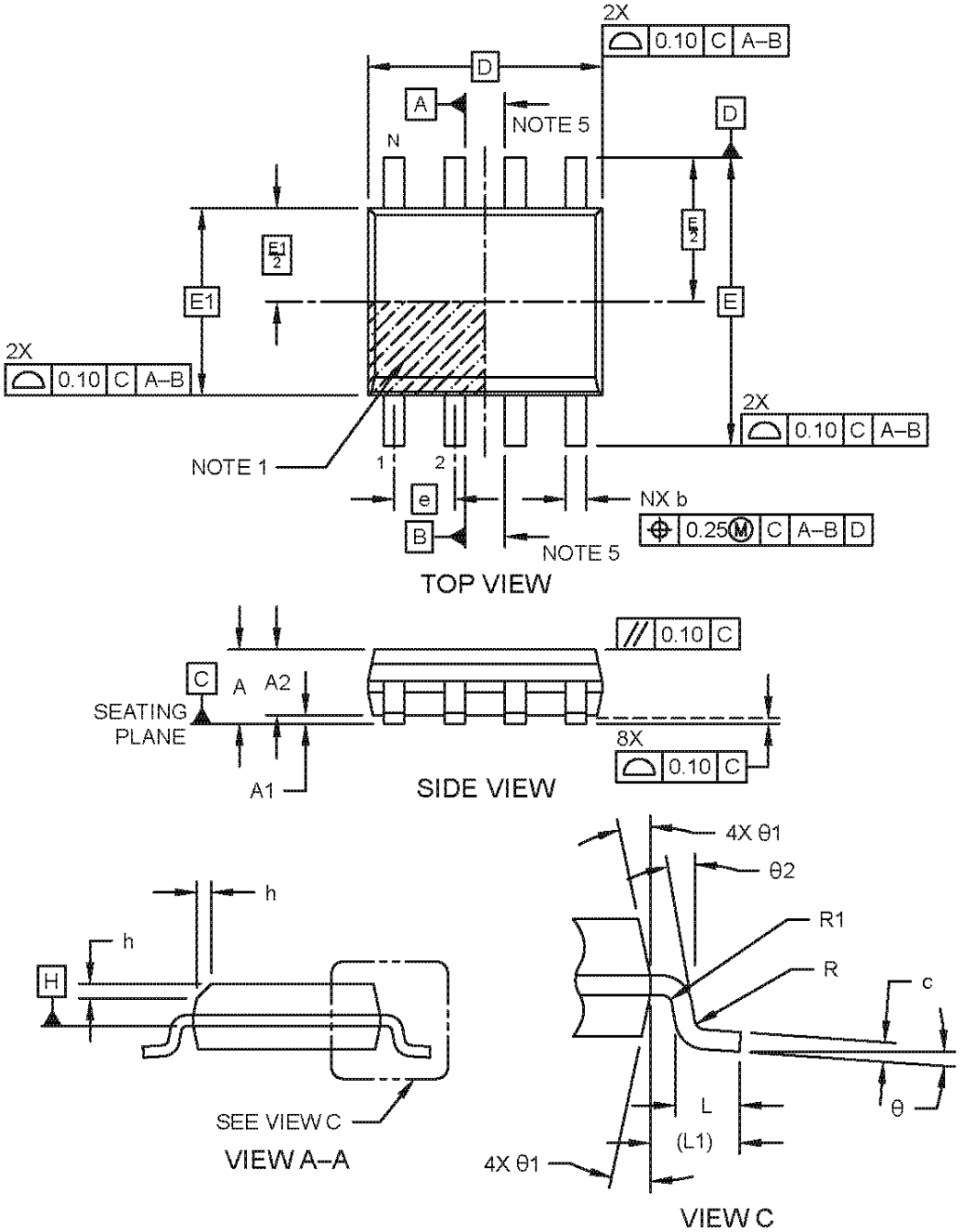
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-MS Rev F

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

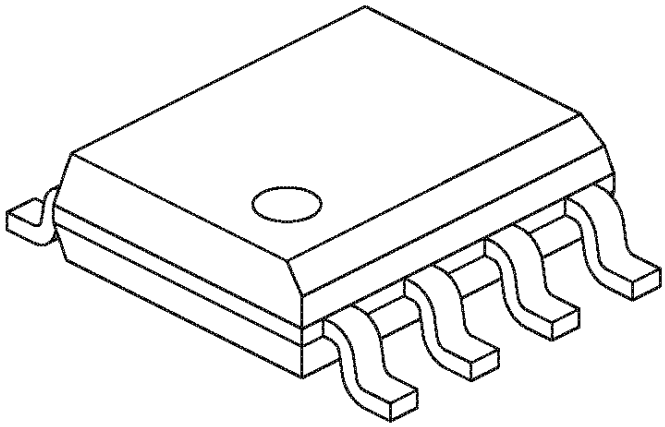
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

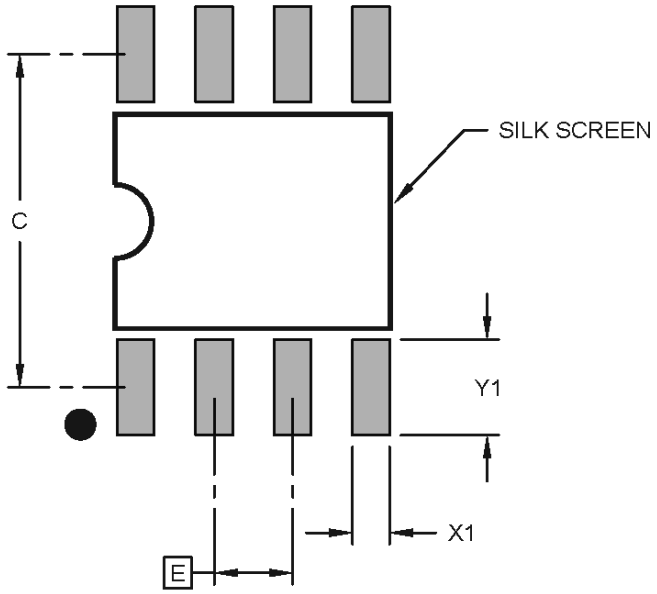
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

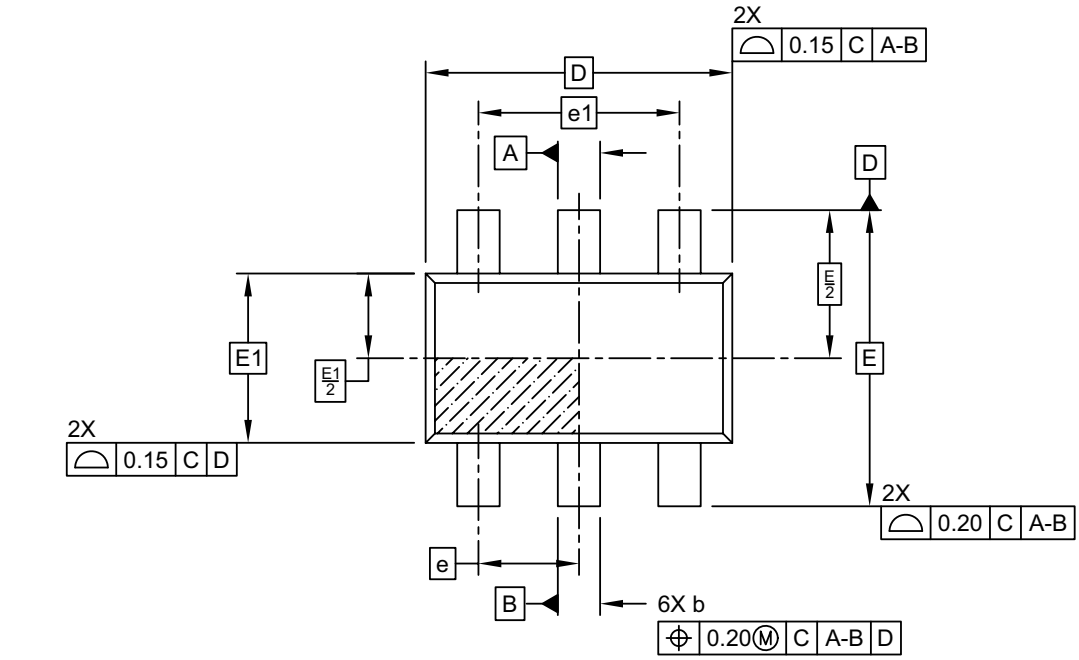
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

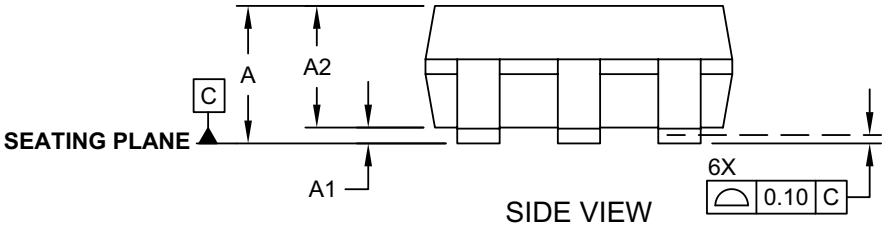
Microchip Technology Drawing C04-02057-SN Rev L

6-Lead Plastic Small Outline Transistor (C8X) [SOT-23]

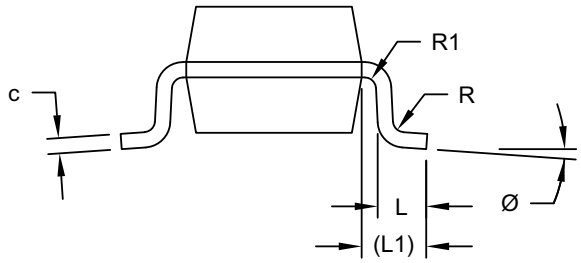
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

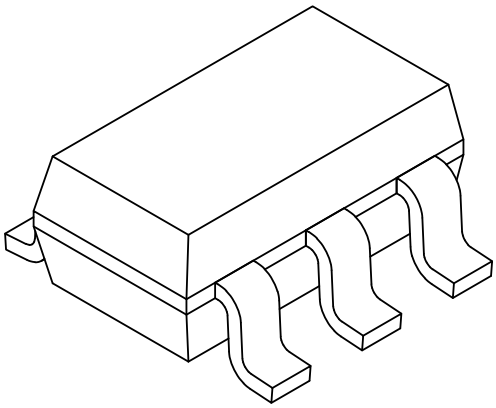


END VIEW

Microchip Technology Drawing C04-028-C8X Rev. F Sheet 1 of 2

6-Lead Plastic Small Outline Transistor (C8X) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	6		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	1.15	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	0.45	0.60
Footprint	L1	0.60 REF		
Foot Angle	Ø	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

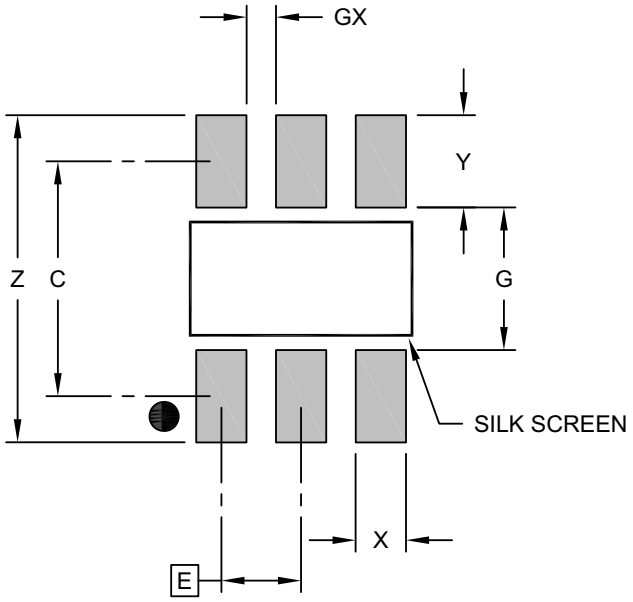
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028-C8X Rev. F Sheet 2 of 2

6-Lead Plastic Small Outline Transistor (C8X) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

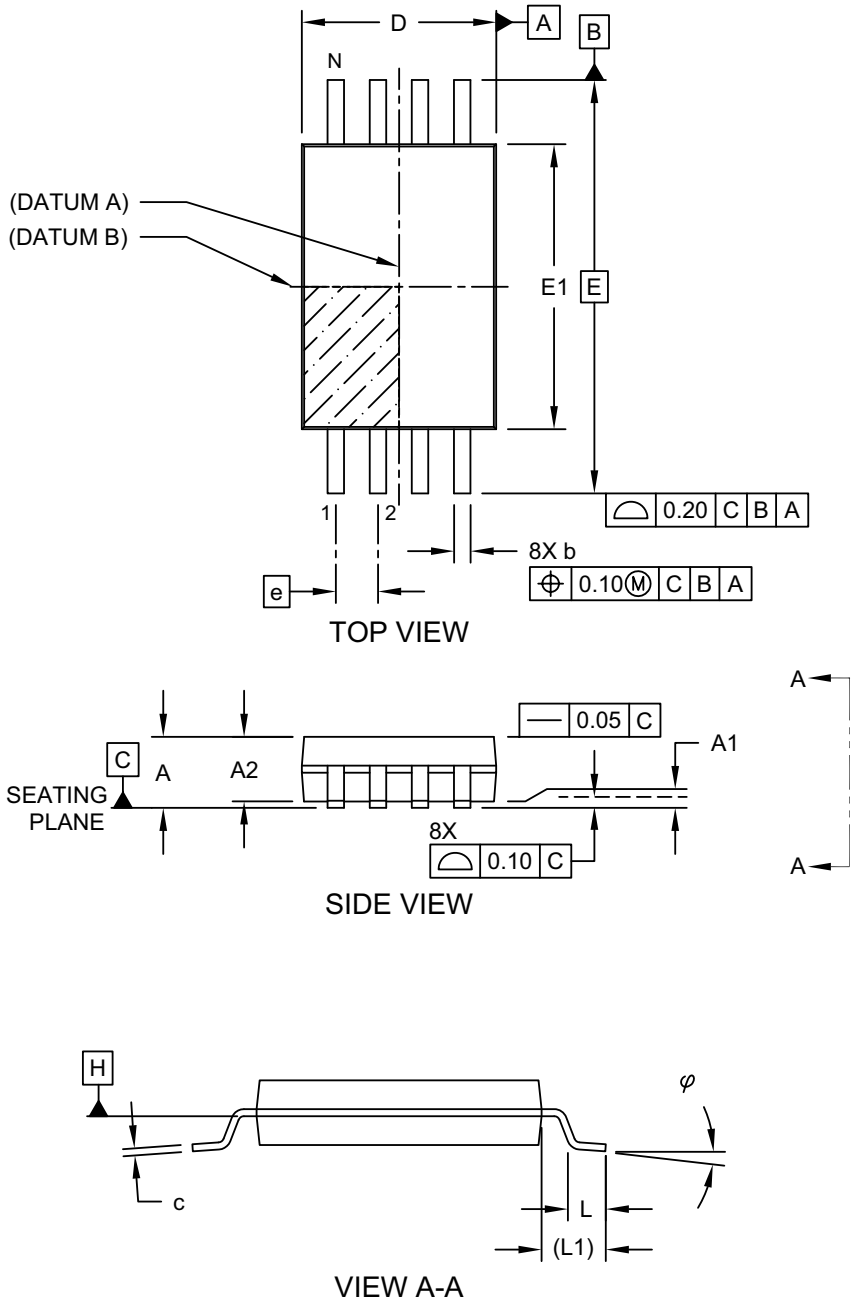
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028-C8X Rev.F

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

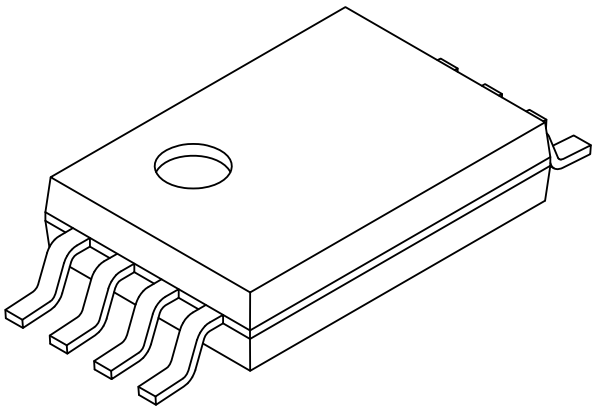
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	-
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Overall Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.19	-	0.30

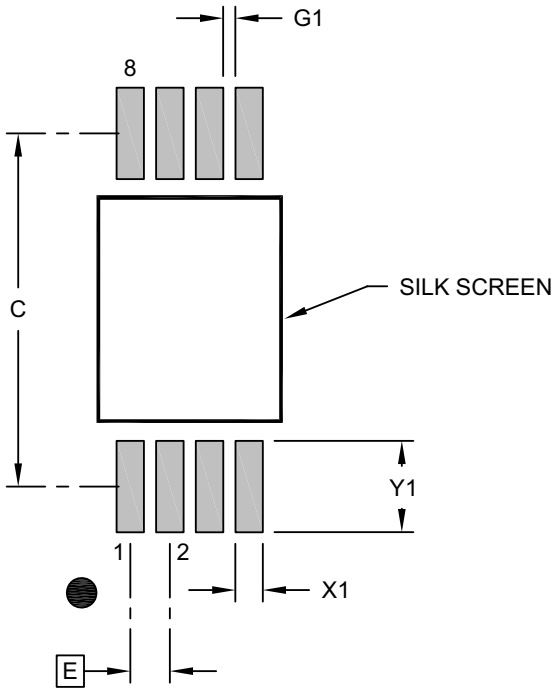
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.80	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.50
Contact Pad to Center Pad (X6)	G1	0.20		

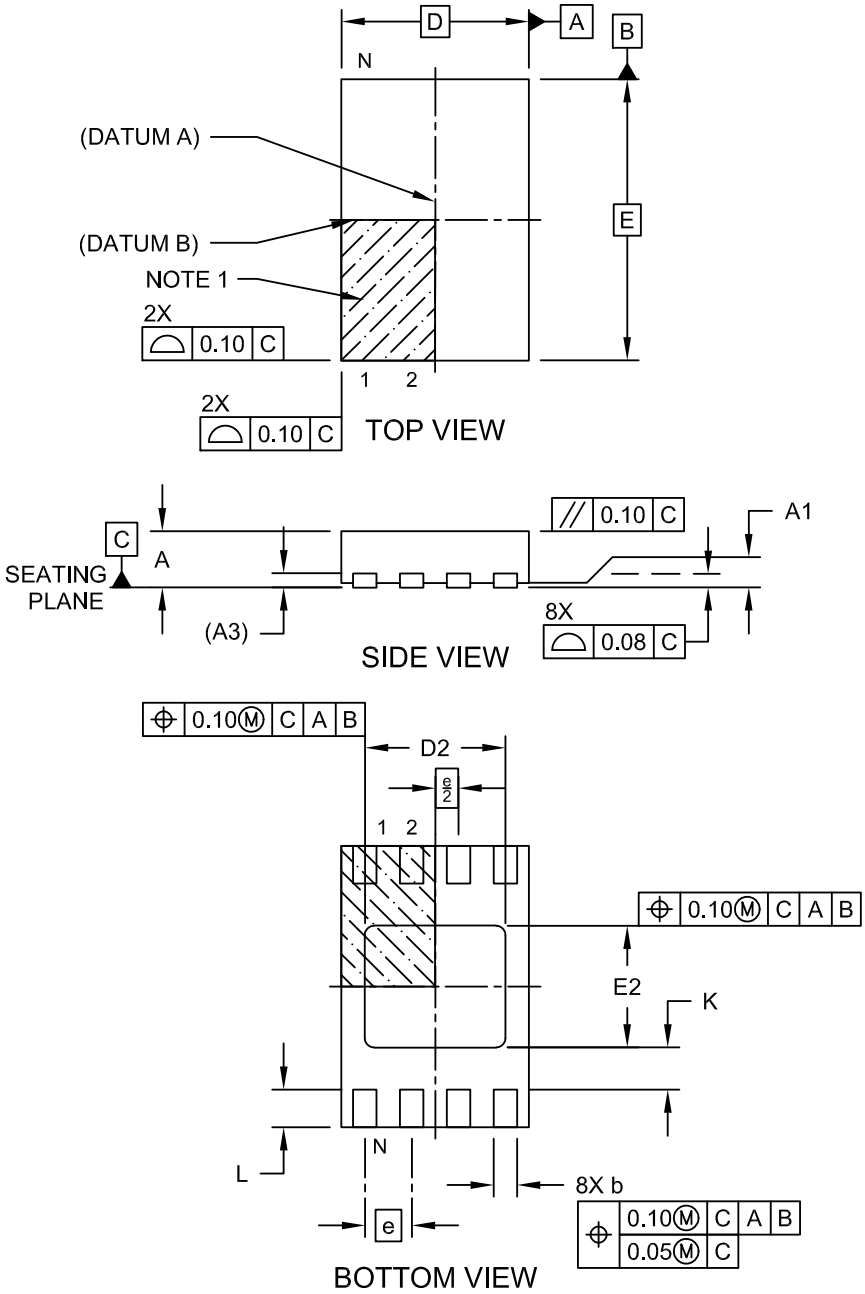
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

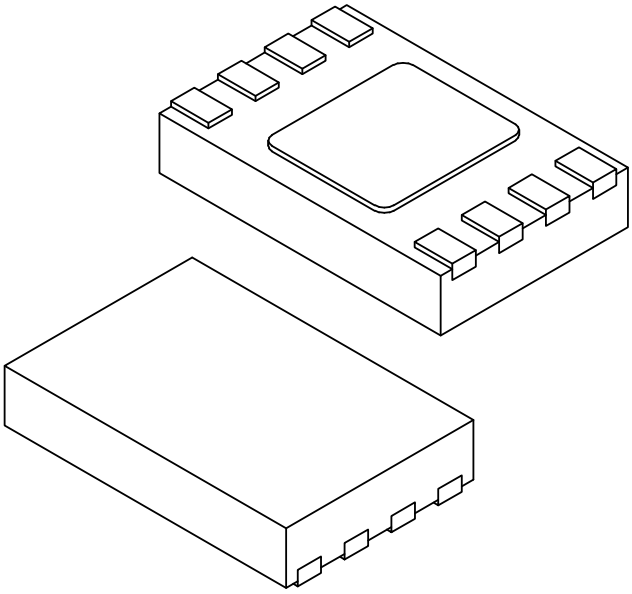
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21355-Q4B Rev C Sheet 1 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.152 REF		
Overall Length	D	2.00 BSC		
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.20	1.30	1.40
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.25	0.35	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

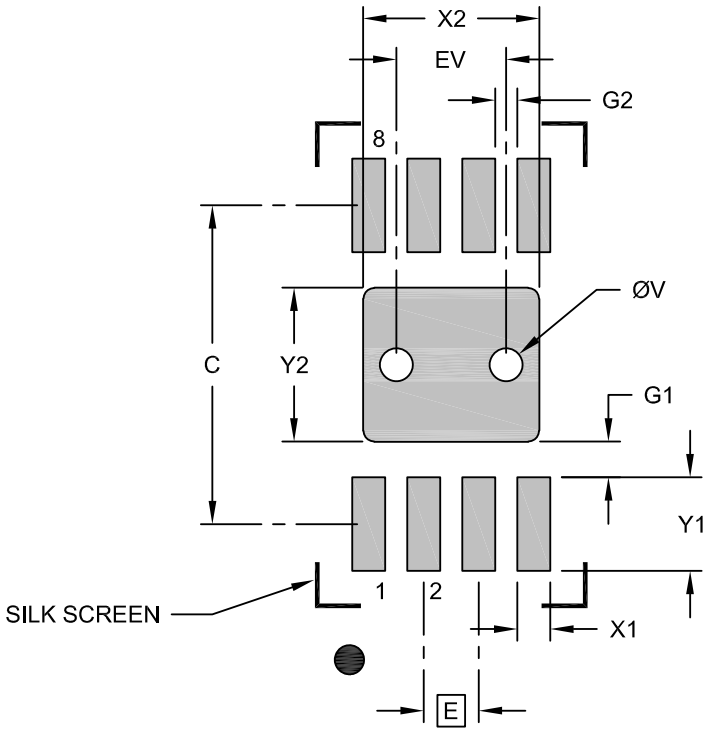
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21355-Q4B Rev C Sheet 2 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.40
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.33		
Contact Pad to Contact Pad (X6)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

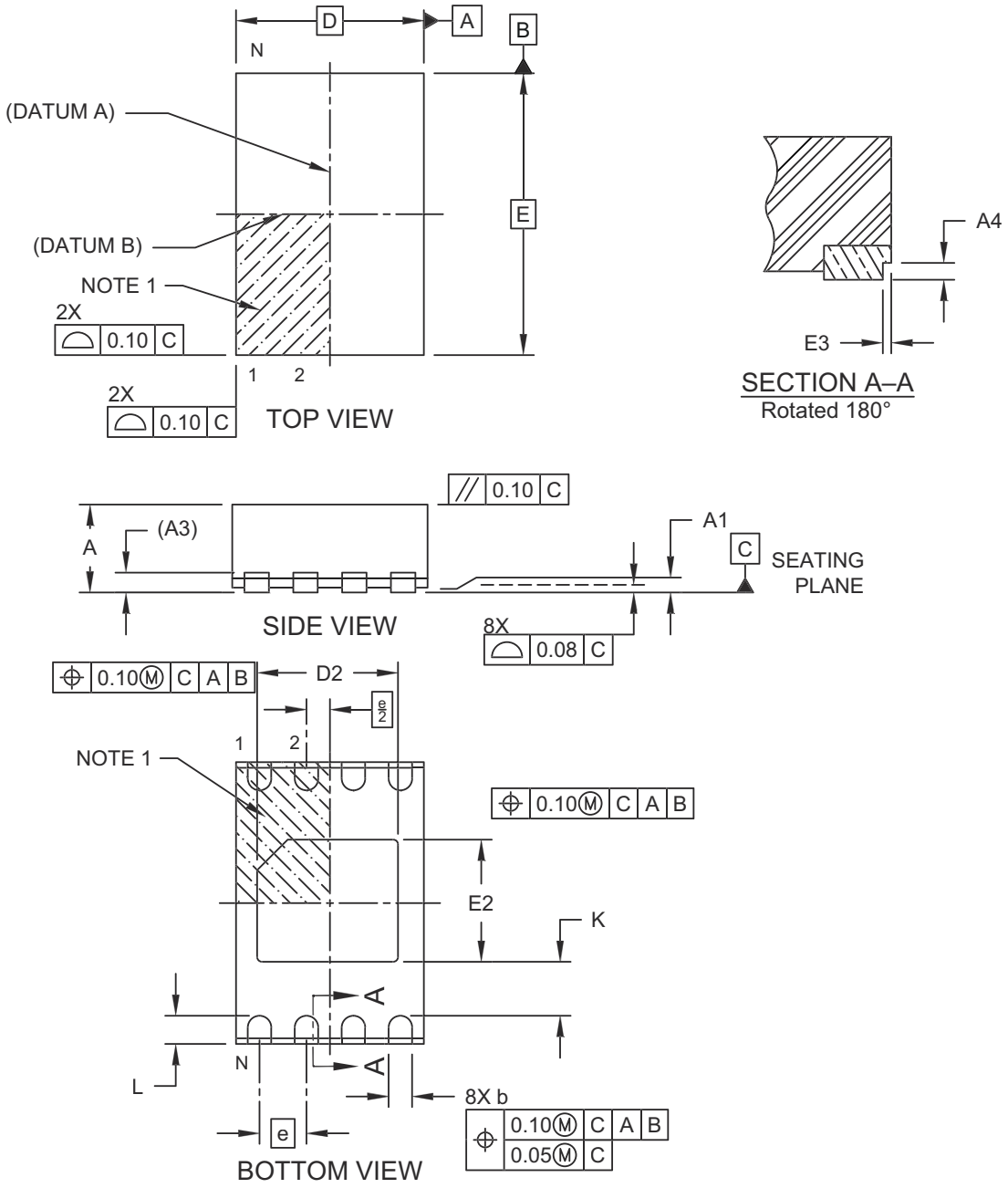
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23355-Q4B Rev C

8-Lead Very Thin Plastic Dual Flat, No Lead Package (MWF) - 2x3x1.0 mm Body [VDFN] 1.5x1.3 mm Exposed Pad Wettable Step Cut Flanks

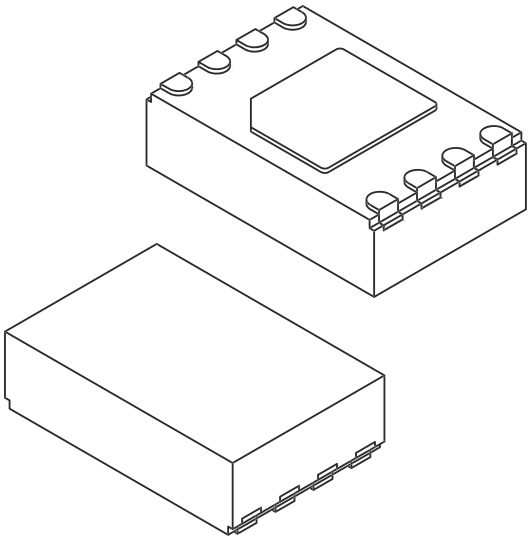
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00598 Rev E Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (MWF) - 2x3x1.0 mm Body [VDFN] 1.5x1.3 mm Exposed Pad Wettable Step Cut Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	008		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	2.00 BSC		
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.20	1.30	1.40
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.25	0.35	0.45
Terminal-to-Exposed-Pad	K	0.20	–	–
Wettable Flank Step Cut Width	E3	0.035	0.06	0.085
Wettable Flank Step Cut Depth	A4	0.100	–	0.190

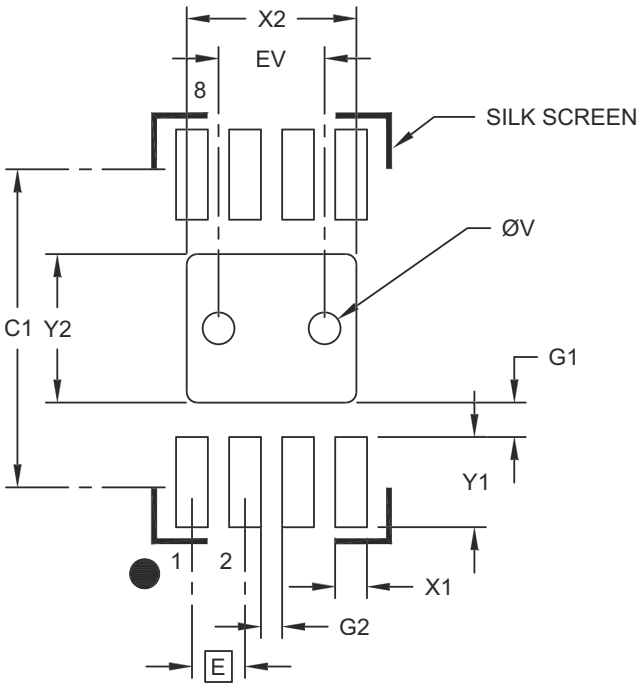
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00598 Rev E Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (MWF) - 2x3x1.0 mm Body [VDFN] 1.5x1.3 mm Exposed Pad Wettable Step Cut Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.40
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.33		
Contact Pad to Contact Pad (X6)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-02598 Rev E

APPENDIX A: REVISION HISTORY

Revision C (06/2026)

Added Automotive Product Identification System for new automotive products. Added VDFN wettable flanks package.

Revision B (01/2026)

Added “Preliminary” status; Minor editorial updates throughout the document.

Revision A (08/2025)

Initial release of this document.

PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][1]	–X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device: 25CS160 = 16-Kbit SPI Serial EEPROM with Security Register

Tape and Reel Option:
- Blank = Standard packaging (tube or tray)
- T = Tape and Reel[1]

Temperature Range:
- I = -40°C to +85°C (Industrial)
- E = -40°C to +125°C (Extended E-Temp.)
- H = -40°C to +150°C (Extended H-Temp.)

Package:
- MS = 8-Lead Plastic Micro Small Outline Package (MSOP)
- SN = 8-Lead Plastic Small Outline – Narrow, 3.90 mm Body (SOIC)
- OT = 6-Lead Plastic Small Outline Transistor (SOT-23) (Tape and Reel only)
- ST = 8-Lead Plastic Thin Shrink Small Outline – 4.4 mm Body (TSSOP)
- Q4B = 8-Lead Plastic Dual Flat, No Lead Package – 2x3 mm (UDFN) (Tape and Reel only)

Examples:

a) 25CS160T-I/MS = Tape and Reel, Industrial Temp., 1.7V-5.5V, MSOP package.

b) 25CS160-E/MS = Extended E-Temp., 1.8V-5.5V, MSOP package.

c) 25CS160T-I/SN = Tape and Reel, Industrial Temp., 1.7V-5.5V, SOIC package.

d) 25CS160T-E/SN = Tape and Reel, Extended E-Temp., 1.8V-5.5V, SOIC package.

e) 25CS160-H/SN = Extended H-Temp., 2.5V-5.5V, SOIC package.

f) 25CS160T-I/OT = Tape and Reel, Industrial Temp., 1.7V-5.5V, SOT-23 package.

g) 25CS160-I/ST = Industrial Temp., 1.7V-5.5V, TSSOP package.

h) 25CS160-E/ST = Extended E-Temp., 1.8V-5.5V, TSSOP package.

i) 25CS160T-H/ST = Tape and Reel, Extended H-Temp., 2.5V-5.5V, TSSOP package.

j) 25CS160T-I/Q4B = Tape and Reel, Industrial Temp., 1.7V-5.5V, UDFN package.

k) 25CS160T-E/Q4B = Tape and Reel, Extended E-Temp., 1.8V-5.5V, UDFN package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X (1)	–X	/XX	XXX (2,3)
Device	Tape and Reel Option	Temperature Range	Package	Variant

Device:	25CS160 = 16-Kbit SPI Serial EEPROM with Security Register		
Tape and Reel Option:	Blank	=	Standard packaging (tube or tray)
	T	=	Tape and Reel(1)
Temperature Range:	E	=	-40°C to +125°C (Extended E-Temp.)
	H	=	-40°C to +150°C (Extended H-Temp.)
Package:	MS	=	8-Lead Plastic Micro Small Outline Package (MSOP)
	SN	=	8-Lead Plastic Small Outline – Narrow, 3.90 mm Body (SOIC)
	ST	=	8-Lead Plastic Thin Shrink Small Outline – 4.4 mm Body (TSSOP)
	MWF	=	8-Lead Very Thin Plastic Dual Flat, No Lead Package – 2x3 mm (VDFN) (Tape and Reel only)
Variant:(2,3)	16KVAO	=	Standard Automotive, 16K Process
	16KVXX	=	Customer-Specific Automotive, 16K Process

Examples

a) 25CS160T-E/MS36KVAO = Tape and Reel, Extended E-Temp., 1.8V-5.5V, MSOP package.

b) 25CS160-E/SN36KVAO = Extended E-Temp., 1.8V-5.5V, SOIC package.

c) 25CS160T-E/SN36KVAO = Tape and Reel, Extended E-Temp., 1.8V-5.5V, SOIC package.

d) 25CS160-H/SN36KVAO = Extended H-Temp., 2.5V-5.5V, SOIC package.

e) 25CS160T-H/SN36KVAO = Tape and Reel, Extended H-Temp., 2.5V-5.5V, SOIC package.

f) 25CS160T-E/ST36KVAO = Tape and Reel, Extended E-Temp., 1.8V-5.5V, TSSOP package.

g) 25CS160T-H/ST36KVAO = Tape and Reel, Extended H-Temp., 2.5V-5.5V, TSSOP package.

h) 25CS160T-E/MWF36KVAO= Tape and Reel, Extended E-Temp., 1.8V-5.5V, VDFN package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

3: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

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