

126V, 5A, LCL/RLCL Programmable Current Limiting Power Switch For Space

Description

The [LX7712](#) is a radiation-hardened-by-design power switch for integration into spacecraft power distribution systems as an electronic fuse for power line protection. DC supplies from 18V to 126V with continuous current rating up to 5A can be easily turned on and off with slew rate programmability. The LX7712 includes a P-channel MOSFET power switch and catch diode for inductive loads.

The LX7712 is configurable as either a latching current limiter or a fold-back current limiter, with optional thermal shutdown. Multiple LX7712 devices can be paralleled to increase the current rating. The current limit, on/off slew rate, and fault response fault timers are programmed with passive external components.

The latching current limiter is configurable to either latch off (LCL) under fault conditions, or to attempt to restart in hiccup mode (RLCL). A fault time integrating function accumulates the thermal effects of short fault pulses. The fault timer is configurable for either a fixed duration or a duration that is a function of the voltage drop from line input to load output across the switch. A resistor programmable fault timer discharge function ensures that the LX7712 has dissipated excess energy to a safe level before restarting.

In fold-back current limit (FCL) mode, the profile of the fold-back load current versus load voltage curve is resistor programmable. Fold-back allows automatic fault recovery. An overload condition forces the current limit to a safe trickle level, and when the overload is removed the current limit returns to its normal level. This prevents soft-short fault situations which can cause the switch to over-dissipate.

A programmable current ramp function limits the slew rate of the current during turn on and turn off.

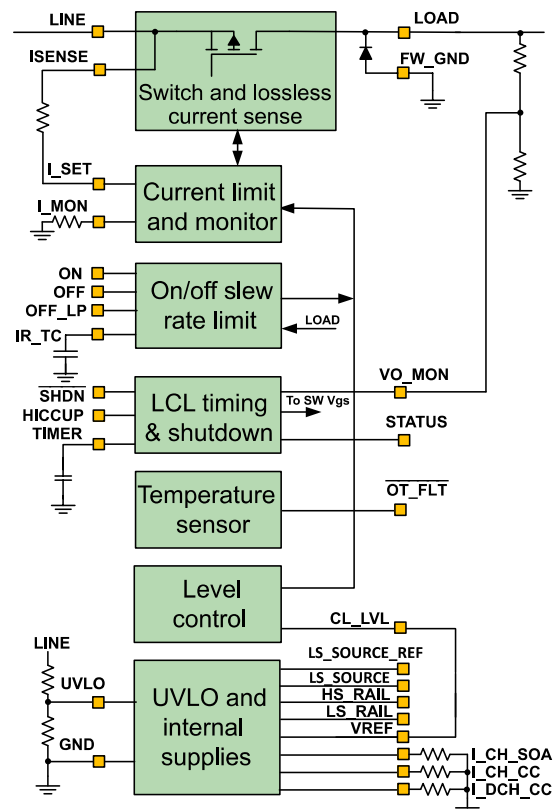
The LX7712MFQ is packaged in a 132-pin hermetic ceramic quad flat pack. It operates over a -55°C to 125°C temperature range and is radiation tolerant to a minimum of 100krad(Si) TID and a minimum of 50krad(Si) ELDRS, as well as single event effects.

Features

- Internal 126V, 5A rated power switch
- Internal catch diode for inductive loads
- Constant current or fold-back current limit
- Safe management of soft overload faults
- Optional hiccup automatic restart mode (RLCL)
- Programmable current levels
- Programmable fault timer
- Current monitor output
- Separate ON, OFF, and LOW POWER OFF control inputs
- Low power switch voltage drop
- Over temperature shutdown and optional restart
- Load current slew rate control
- Radiation tolerant: 100krad(Si) TID, 50krad(Si) ELDRS, Single Event Latch-up immune to 81.2MeV.cm²/mg at 120V

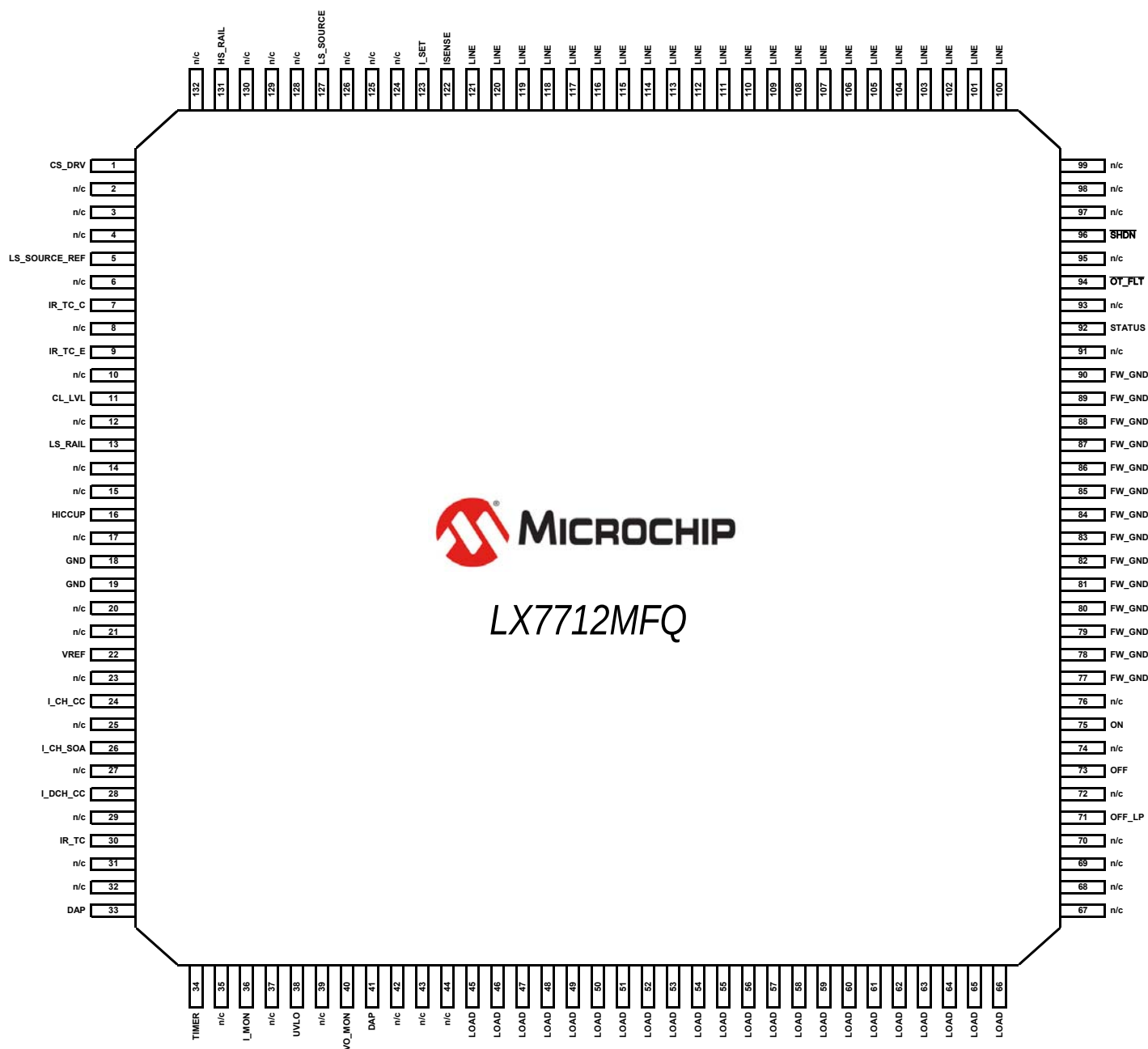
Applications

- Spacecraft power control and distribution



Typical Power Switch System

1 CQFP-132 Pin Configuration and Pinout



2 Ordering Information (subject to export restrictions under EAR9A515.e)

Operating Temperature	Package Type	Package	Part Number	SMD Number	Flow	Shipping Type
-55°C to 125°C	Hermetic Ceramic	CQFP 132L	LX7712MFQ-EV	TBD	MIL-PRF-38535 Class V	Tray
			LX7712MFQ-EQ	TBD	MIL-PRF-38535 Class Q	
			LX7712MFQ-ES ¹	-	Engineering Samples ¹	
	Ceramic		MECH-SAMPLE-CQFP132	-	Empty Package Sample	

¹ Engineering samples are intended for design evaluation purposes only. They are only tested and trimmed at room temperature, and do not undergo any thermal, environmental, or hermeticity testing

3 CQFP-132 Pin Numbering and Pin Descriptions

Pin	Name	Pin Type	Pin Function	Description
1	CS_DRV	Analog Output	Cold-Spare PFET Driver	Gate drive for optional external power PMOS in series with the power input rail and the LINE input pins which prevents reverse current flow from LOAD to the input supply when the LX7712's internal power switch is turned off. See section 19 on page 27
2-4	n/c	-	-	Pins are not bonded
5	LS_SOURCE_REF	Analog Output	Zener	Cathode of internal zener diode for optional biasing of external pass transistor when no low voltage LS_SOURCE supply is available. See section 12.4 on page 15
6	n/c	-	-	Pin is not bonded
7	IR_TC_C	Analog I/O	IR_TC NPN	Collector of internal NPN buffer for IR_TC current slew rate control
8	n/c	-	-	Pin is not bonded
9	IR_TC_E	Analog I/O	IR_TC NPN	Emitter of internal NPN buffer for IR_TC current slew rate control
10	n/c	-	-	Pin is not bonded
11	CL_LVL	Analog Input	Current Limit Level	The voltage on this pin sets the current limit reference level. A resistor network connects this pin to LOAD and/or VREF. See section 15 on page 19
12	n/c	-	-	Pin is not bonded
13	LS_RAIL	Power	Low-Side Rail	Output of an internal linear regulator delivering 10V $\pm$ 1V above GND. Regulator input is LS_SOURCE pin 127. Bypass LS_RAIL with a 10nF capacitor to GND. See the LS_SOURCE and LS_RAIL section 12.4 on page 15
14-15	n/c	-	-	Pins are not bonded
16	HICCUP	Logic Input (4M Ω to GND)	Hiccup Mode Enable	To enable hiccup mode, which resets a latched over-current fault under fault timer control, tie HICCUP to either VREF or to a 2.5V to 5V logic supply. To disable hiccup mode, leave HICCUP open or tie to GND. See the Fault Timer section 16 on page 20
17	n/c	-	-	Pin is not bonded
18-19	GND	Power	GND	All GND pins 17 to 19 must be used, and are the GND point for analog and logic signals
20-21	n/c	-	-	Pins are not bonded
22	VREF	Analog Output	5V Reference	Output of an internal +5V $\pm$ 4% reference voltage. VREF can source up to 2mA into external loads such as configuration resistor networks. Bypass VREF with a 100nF capacitor to GND
23	n/c	-	-	Pin is not bonded
24	I_CH_CC	Analog Input	Fault Timer Static Charge Current Programming	Connect resistor R _{I_CH_CC} from I_CH_CC to GND to set a static reference current to charge the fault timer capacitor. Leave open if not used. See the Fault Timer section 16 on page 20
25	n/c	-	-	Pin is not bonded
26	I_CH_SOA	Analog Input	Fault Timer Dynamic Charge Current Programming	Connect resistor R _{I_CH_SOA} from I_CH_SOA to GND to set a dynamic reference current to charge the fault timer capacitor. Leave open if not used. See the Fault Timer section 16 on page 20
27	n/c	-	-	Pin is not bonded
28	I_DCH_CC	Analog Input	Fault Timer Discharge Current Programming	Connect resistor R _{I_DCH_CC} from I_DCH_CC to GND to set a static reference current to discharge the fault timer capacitor, and to set the slew rate during power switch turn on and turn off. See the Fault Timer section 16 on page 20
29	n/c	-	-	Pin is not bonded
30	IR_TC	Analog Input	Current Ramping Timing Capacitor	Connect capacitor C _{IR_TC} from IR_TC to GND to set the slew rate during power switch turn on and turn off or leave open. R _{I_DCH_CC} on I_DCH_CC pin 28 is the other programming element. See the Fault Timer section 16 on page 20
31-32	n/c	-	-	Pins are not bonded
33	DAP	Power	Die Attach Pad	This pin must be connected to GND

Pin	Name	Pin Type	Pin Function	Description
34	TIMER	Analog Input	Latchable Current Limit Fault Timer	Connect capacitor C_{TIMER} from TIMER to GND to set the programmable fault timer time constant together with resistors $R_{I_{CH_CC}}$, $R_{I_{DCH_CC}}$, and $R_{I_{DCH_CC}}$. Grounding TIMER disables the fault timer function. See the Fault Timer section 16 on page 20
35	n/c	-	-	Pin is not bonded
36	I_MON	Analog Output	Load Current Monitor	Connect resistor R_{I_MON} from I_MON to GND to monitor the load current. The output current on this pin is $1/5000 \times$ the load current. Short I_MON to GND if load current monitoring isn't required. See the Current Monitoring section 14 on page 18
37	n/c	-	-	Pin is not bonded
38	UVLO	Analog Input	LINE Under-Voltage Lock-Out	This input is used to monitor the LINE voltage. The under-voltage level is set with a LINE to GND external voltage divider. See the External Voltage Monitor Inputs section 13.4 on page 17
39	n/c	-	-	Pin is not bonded
40	VO_MON	Analog Input	LOAD Voltage Monitor	This input is used to monitor the LOAD voltage. The under-voltage level is set with a LOAD to GND external voltage divider. See the External Voltage Monitor Inputs section 13.4 on page 17
41	DAP	Power	Die Attach Pad	This pin must be connected to GND
42-44	n/c	-	-	Pins are not bonded
45-66	LOAD	Power	Power Switch Output	All LOAD pins 45 to 66 must be used, connected to the external load. An internal reverse biased diode from LOAD to FW_GND clamps inductive flyback voltages on turn-off
67-70	n/c	-	-	Pins are not bonded
71	OFF_LP	Power (2.4M Ω to GND)	OFF (Low Power) Control	A logic high level on OFF_LP will turn off the power switch and enter low power mode by shutting down internal power supplies
72	n/c	-	-	Pin is not bonded
73	OFF	Logic Input (4M Ω to GND)	OFF Control	A logic high pulse or level on this pin will turn off the power switch. The OFF input has priority over the ON pin if both are high
74	n/c	-	-	Pin is not bonded
75	ON	Logic Input (4M Ω to GND)	ON Control	A logic high pulse or level on this pin will turn on the power switch
76	n/c	-	-	Pin is not bonded
77-90	FW_GND	Power GND	Free-wheel Diode Ground	All FW_GND pins 77 to 90 must be used, to provide a path for current to flow through the free-wheeling diode that provides a path of inductive load current if the power switch shuts off abruptly
91	n/c	-	-	Pin is not bonded
92	STATUS	Open Collector Logic Output	On/Off Status	A low level on this open collector output indicates that the switch is on, and that the VO_MON is monitoring a LOAD voltage greater than the under-voltage threshold
93	n/c	-	-	Pin is not bonded
94	$\overline{OT_FLT}$	Open Collector Logic I/O	Over Temperature Fault	A low level on this open collector output indicates that an over-temperature fault has occurred. The over-temperature sensor has hysteresis and resets after cooling down. This pin can be connected to SHDN. Multiple devices can have $\overline{OT_FLT}$ and SHDN connected
95	n/c	-	-	Pin is not bonded
96	$\overline{SHDN}$	Open Collector Logic I/O (1M Ω to LS_RAIL)	Shutdown Fault	A low logic output signal indicates that an LCL timeout has triggered the shutdown latch. This pin can also be used as an input from another device or from the temperature monitor output $\overline{OT_FLT}$ to conditionally shutdown the switch. Multiple devices can have $\overline{SHDN}$ connected
97-99	n/c	-	-	Pins are not bonded
100-121	LINE	Power	Power Switch Input	All LINE pins 100 to 121 must be used, connected to the 18V to 126V power supply to be switched. LINE is also the power input for the HS_RAIL regulator. Bypass the group of LINE pins with a single 100nF capacitor to GND
122	ISENSE	Power Kelvin Sense Input	Current Monitor Input	Connect a resistor $R_{I_SET} = 10k\Omega$ between ISENSE and I_SET to bias the power switch's current sensing. ISENSE is internally bonded to LINE and provides a Kelvin connection to LINE since it does not carry any of the LINE/LOAD current
123	I_SET	Analog Input	Current Monitor Reference	
124-126	n/c	-	-	Pins are not bonded

Pin	Name	Pin Type	Pin Function	Description
127	LS_SOURCE	Power	Low-Side Rail Power Source	Input to the LS_RAIL linear regulator with output at pin 13. Bypass LS_SOURCE with a 100nF capacitor to GND. See the LS_SOURCE and LS_RAIL section 12.4 on page 15
128-130	n/c	-	-	Pins are not bonded
131	HS_RAIL	Power	High-Side Rail	Output of an internal linear regulator delivering 10V $\pm$ 1V below LINE. Bypass HS_RAIL with 100nF to LINE (<i>not</i> to GND). See the HS_RAIL section 12.3 on page 15
132	n/c	-	-	Pin is not bonded

Notes

1. Pins that are shown as not bonded may be connected to any potential, such as an adjacent pin or GND, subject to the creepage and clearance requirements of the PCB layout
2. It is recommended to:
 - a. Create a partial ground plane for the LX7712's analog and control components, and connect this plane to system GND at the signal GND pins 18 and 19 and the die attach pins 33 and 41. This avoids modulation of the analog ground by load currents
 - b. Connect the power FW_GND pins 77 to 90 via a separate low-impedance path to system GND

4 Absolute Maximum Ratings

Stresses above those listed in ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Parameter	Min	Max	Units
V_{LINE}	-3	150	V
V_{LOAD}	-2	$V_{LINE} + 1.5$	V
V_{HS_SINK}	-0.3	V_{LINE}	V
V_{LS_SOURCE}	-0.3	27	V
P_{HS_SINK} (HS_SINK regulator dissipation)		610	mW
P_{LS_SOURCE} (LS_SOURCE regulator dissipation)		300	mW
$I_{LS_SOURCE_REF}$	-5	3	mA
$I_{IR_TC_C}$, $I_{IR_TC_E}$	-3	3	mA
I_{CS_DRV}		3	mA
I_{LINE} , I_{LOAD}	-7.5	7.5	A
I_{FW_GND}	0	7.5	A
V_{HS_RAIL}	Self-regulated	V_{LINE}	V
V_{I_SET}	$V_{LINE} - 7.5$	V_{LINE}	V
V_{LS_RAIL}	-0.3	15	V
V_{VREF}	-0.3	Self-regulated	V
V_{IMON}	-0.3	5.6	V
V_{CL_LVL} , V_{TIMER}	-0.3	9	V
V_{UVLO} , V_{VO_MON}	-0.3	15	V
$V_{I_CH_CC}$, $V_{I_CH_SOA}$, $V_{I_DCH_CC}$, V_{IR_TC}	-0.3	11	V
V_{HICCUP} , V_{OFF_LP} , V_{OFF} , V_{ON} , V_{STATUS} , V_{OT_FLT} , V_{SHDN}	-0.3	12	V
STATUS, $\overline{SHDN}$, and $\overline{OT_FLT}$ sink current	0	3	mA
I_{MON} pin current	-1	0	mA
Operating Junction Temperature	-55	150	°C
Storage Junction Temperature	-65	160	°C
Peak Lead Solder Temperature (10 seconds)		260 (+0, -5)	°C

5 Electrostatic Discharge Ratings

JEDEC JEP155 states that 500V HBM allows safe manufacturing with a standard ESD controlled process. JEDEC JEP157 states that 250V CDM allows safe manufacturing with a standard ESD controlled process. ESD ratings apply to all pins.

ESD Test	Minimum Capability
HBM: Human Body Model, per MIL-STD-883 TM3015	±2kV
CDM: Charged Device Model, per ANSI/ESDA/JEDEC JS-002	±500V (±750V TBD)

6 Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Parameter	Min	Max	Units
V _{LINE} , V _{LOAD} (using R _{I_MON} = 5kΩ)	22	126	V
V _{LINE} , V _{LOAD} (using R _{I_MON} = 1kΩ)	18	126	V
P _{HS_SINK} (HS_SINK regulator dissipation)		480	mW
P _{LS_SOURCE} (LS_SOURCE regulator dissipation)		225	mW
I _{LS_SOURCE_REF}	-2	2	mA
I _{IR_TC_C} , I _{IR_TC_E}		2	mA
I _{CS_DRV} (peak current when charging or discharging the gate of an external PFET)	-2	2	mA
V _{LS_SOURCE}	12	20	V
V _{HS_SINK}	0	V _{LINE} - 12	V
V _{I_SET}	V _{LINE} - 6	V _{LINE}	V
V _{CL_LVL}	0	5.3	V
V _{UVLO} , V _{VO_MON}	0	13	V
V _{I_CH_CC} , V _{I_CH_SOA} , V _{I_DCH_CC} , V _{IR_TC} , V _{TIMER} , V _{HICCUP} , V _{OFF_LP} , V _{OFF} , V _{ON}	0	6	V
V _{STATUS} , V _{OT_FLT} , V _{SHDN}	0	V _{LS_RAIL}	V
V _{IMON}	0	(V _{I_SET} - 5) up to 5.5 max	V
STATUS, SHDN, and OT_FLT sink current	0	2	mA
I _{LINE} , -I _{LOAD} (peak current when switch body diode or catch diode is forward biased)	-5	5	A
I _{FWD_CatchD} (maximum continuous current through catch diode)		0.5	A
P _{FWD_CatchD} (maximum average power dissipated by catch diode during pulsed regime)		0.5	W
Q _{FWD_CatchD} (maximum average charge dissipated by catch diode during pulsed regime)		40	mC

7 Electrical Characteristics

The following specifications apply over the operating ambient temperature of -55°C ≤ T_A ≤ 125°C except where otherwise noted with the following test conditions: V_{ON} = V_{HICCUP} = 6V; V_{OFF} = V_{OFF_LP} = V_{HS_SINK} = GND; V_{LS_SOURCE} = 17V; 18V < V_{LINE} < 126V. R_{I_MON} = 1kΩ. Typical parameters refer to T_J = 25°C. Positive currents flow into a pin.

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Operating Currents and Voltages						
I _{LINE}	Internal IC current consumption flowing to LINE	Switch On or Off, No Load		3.5	6.5	mA
		Switch Off (low power)		0.6	1.9	mA
I _{HS_SINK}	Current for internal linear regulator HS_RAIL	OFF_LP = logic low		-1	-1.5	mA
I _{LS_SOURCE}	Current for internal linear regulator LS_RAIL (part of I _{GND})	LS_SOURCE is supply for LS_RAIL regulator. OFF_LP = logic low	3.5	6.5	10	mA
I _{LS_RAIL}	Current into LS_RAIL	LS_RAIL supplied with external 11V, LS_SOURCE floating	2	7	9	mA
V _{LINE_UVLO}	LINE UVLO	V _{LINE} rising, with both LS_RAIL and VREF operating normally	9		10.3	V
V _{LINE_HYST}	LINE UVLO hysteresis		0.02	0.3	0.9	V
V _{LS_RAIL_UVLO}	LS_RAIL UVLO	VREF voltage rising	7.3	7.9	8.5	V
V _{HS_RAIL_UVLO}	HS_RAIL UVLO	(V _{LINE} - V _{HS_RAIL}) voltage rising	7.3	7.9	8.5	V
V _{VREF_UVLO}	VREF UVLO	LS_RAIL voltage rising	4.2	4.45	4.65	V
V _{HS_RAIL}	Voltage below line	V _{LINE} - V _{HS_RAIL}	9	10	11	V
V _{LS_RAIL}	Voltage above ground	-1mA < I _{LS_RAIL} < 0 drawn externally	9	10	11	V
V _{LS_SOURCE_REF}	Zener voltage	I _{LS_SOURCE_REF} = TBD μA. Zener comprises 3 nominally 6V zener diodes in series	TBD	18	TBD	V

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
V _{VREF}	Output voltage	-2mA < I _{VREF} < 0	4.8	5	5.2	V
I _{VREF}	Current limit	VREF shorted to ground	-2	-12	-25	mA
Logic Inputs ON, OFF, HICCUP, OFF_LP						
V _{INPUT}	Input logic high level	ON, OFF, HICCUP	2			V
		OFF_LP	2.2			
	Input logic low level	ON, OFF, HICCUP, OFF_LP			0.8	V
	Leakage Current	V _{INPUT} = 5V (OFF_LP)	0.5		10	μA
		V _{INPUT} = 5V (ON, OFF, HICCUP)	0.25		5	
V _{INPUT} = 0V		-1		1		
T _{LATCH}	Pulse Width to latch for ON, OFF and HICCUP	Either ON or OFF	1			μs
Logic Input SHDN						
V _{SHDN}	Input logic high level	SHDN as input	2.0			V
	Input logic low level				0.8	
	Leakage Current	SHDN as input; 0V < V _{SHDN} < V _{LS_RAIL}	-50		50	μA
Logic Outputs STATUS, OT_FLT, SHDN						
V _{STATUS} , V _{OT_FLT} , V _{SHDN}	Logic levels SHDN as output	High output voltage; 10kΩ pull-up to LS_RAIL	8.5	10	11	V
		Low output voltage; I _{SINK} = 1mA	0	0.3	0.5	V
		I _{SINK} internal current limit	2	6	10	mA
External Under-Voltage Lockout (UVLO)						
V _{UVLO}	Voltage threshold	Voltage rising	49	50	51	%VREF
V _{UVLO}	Hysteresis		1	3	4.5	%VREF
I _{UVLO}	UVLO monitor leakage	0V < V _{UVLO} < 13V	-10		10	μA
T _{D UVLO}	UVLO to STATUS delay	UVLO 5V to 0V step, R _{STATUS} = 10kΩ, C _{STATUS} = 100pF, 50% to 50%	0.3		1.5	ms
VO_MON						
V _{VO_MON}	VO_MON threshold	Voltage rising	49	50	51	%VREF
V _{VO_MON}	VO_MON hysteresis	Hysteresis	1	3	4.5	%VREF
I _{VO_MON}	VO_MON leakage	0 < V _{VO_MON} < 13V	-10		10	μA
T _{D VO_MON}	VO_MON to STATUS delay time	VO_MON 5V to 0V step, R _{STATUS} = 10kΩ, C _{STATUS} = 100pF, 50% to 50%		4	10	μs
Power Switch						
$\frac{\Delta I_{LOAD_TRIP}}{\Delta V_{CL_LVL}}$	CL_LVL input voltage to LOAD current gain (transconductance)	R _{I_SET} = 10kΩ, for V _{CL_LVL} = 1V to 5V	0.9		1.1	Ω ⁻¹
I _{LOAD_TRIP_LINEARITY}	Error from ideal line with respect to 5A scale	R _{I_SET} = 10kΩ, for V _{CL_LVL} = 1V to 5V	-1		1	%
I _{LOAD_TRIP_offset}	Load current trip value extrapolated at 0V	R _{I_SET} = 10kΩ, V _{CL_LVL} = 1V, V _{CL_LVL} = 2V; T _J = 25°C - 125°C	-0.4	-0.2	0.1	A
		R _{I_SET} = 10kΩ, V _{CL_LVL} = 1V, V _{CL_LVL} = 2V; T _J = -55°C	-0.75	-0.3	0.1	A
I _{LOAD_TRIP_1V}	Load current trip error from 0.8A with respect to 5A scale at 1V	R _{I_SET} = 10kΩ, for V _{CL_LVL} = 1V; T _J = 25°C	-4		4	%
			-0.2		0.2	A
		R _{I_SET} = 10kΩ, for V _{CL_LVL} = 1V	-10		5	%
			-0.5		0.25	A
I _{LOAD_TRIP_4V}	Load current trip error from 3.8A with respect to 5A scale at 4V	R _{I_SET} = 10kΩ, for V _{CL_LVL} = 4V	-9		7	%
			-0.45		0.35	A
I _{I_MON_LINEARITY}	Error from ideal line with respect to 5A scale	I _{LOAD} = 0-4A, V _{CL_LVL} = 5.25V, R _{I_MON} = 1kΩ, R _{I_SET} = 10kΩ;	-0.5		0.5	%
I _{I_MON_0A}	I _{I_MON} current at I _{LOAD} = 0A	I _{LOAD} = 0A, V _{CL_LVL} = 5.25V, R _{I_MON} = 1kΩ, R _{I_SET} = 10kΩ; T _J = 25°C - 125°C	-1	-40	-70	μA
		I _{LOAD} = 0A, V _{CL_LVL} = 5.25V, R _{I_MON} = 1kΩ, R _{I_SET} = 10kΩ; T _J = -55°C	-30		-125	μA

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
$I_{L_MON_1A}$	I_{L_MON} error from 240 μ A with respect to 5A scale at $I_{LOAD} = 1A$	$I_{LOAD} = 1A$, $V_{CL_LVL} = 5.25V$, $R_{L_MON} = 1k\Omega$, $R_{I_SET} = 10k\Omega$	-4		7	%
$I_{L_MON_2A}$	I_{L_MON} error from 440 μ A with respect to 5A scale at $I_{LOAD} = 2A$	$I_{LOAD} = 2A$, $V_{CL_LVL} = 5.25V$, $R_{L_MON} = 1k\Omega$, $R_{I_SET} = 10k\Omega$	-4		7	%
$I_{L_MON_4A}$	I_{L_MON} error from 840 μ A with respect to 5A scale at $I_{LOAD} = 4A$	$I_{LOAD} = 4A$, $V_{CL_LVL} = 5.25V$, $R_{L_MON} = 1k\Omega$, $R_{I_SET} = 10k\Omega$ $I_{LOAD} = 4A$, $V_{LINE} = 20V$, $V_{CL_LVL} = 5.25V$, $R_{L_MON} = 5k\Omega$, $R_{I_SET} = 10k\Omega$	-5		7	%
$\frac{\Delta I_{LOAD_CLIM}}{\Delta V_{CL_LVL}}$	CL_LVL input voltage to LOAD current limit gain (transconductance)	$R_{I_SET} = 10k\Omega$, for $V_{CL_LVL} = 1V$ to 5V	0.65	0.9	1.1	Ω^{-1}
$I_{LOAD_CLIM_1V}$	Load current limit error from 0.6A with respect to 5A scale at 1V	$R_{I_SET} = 10k\Omega$, for $V_{CL_LVL} = 1V$;	-10		10	%
$I_{LOAD_CLIM_5V}$	Load current limit error from 4.2A with respect to 5A scale at 5V	$R_{I_SET} = 10k\Omega$, for $V_{CL_LVL} = 5V$;	-20		20	%
V_{LINE_LOAD}	Switch voltage drop	$I_{LOAD} = 1A$		120	220	mV
R_{LINE_LOAD}	Switch on-resistance	$I_{LOAD} = 1A$		120	220	m Ω
I_{LINE_LOAD}	Switch off leakage	In short circuit; $T_J = -55^{\circ}C - 25^{\circ}C$		0.1	20	μA
		In short circuit; $T_J = 125^{\circ}C$		30	125	μA
t_{PWR_ON}	Switch turn on time	From ON to LOAD; $IR_TC = open$			200	μs
t_{LP_ON}	Switch turn on time from low power mode	From OFF_LP de-assertion (50%) to LOAD (10%); ON = asserted; $IR_TC = open$			1.5	ms
t_{C_LIM}	Current limit reaction time	5A current limit, LOAD step from 10k Ω to 1m Ω , I_{LOAD} falls below 5A			10	μs
$V_{Reverse}$	On voltage for switchback diode	$I_{reverse} = 5A$		1	1.5	V
$I_{Reverse_sw}$	Maximum reverse current	DC			5	A
Catch Diode						
V_{FWD}	Forward voltage from FW_GND to LOAD	$I_{FW_GND} = 2A$ pulsed		2.8	3.5	V
I_{FW_GND}	Leakage current	$V_{LOAD} = 100V$		0	1	μA
Fault Timer						
I_{TIMER}	Fault timer charge current, under fault condition	$R_{I_CH_CC} = 100k\Omega$, $R_{I_CH_SOA} = open$, $V_{TIMER} = 2.5V$	-12	-10	-8	μA
		$R_{I_CH_CC} = open$; $R_{I_CH_SOA} = 100k$, $V_{LINE} - V_{LOAD} = 10V$, $V_{TIMER} = 2.5V$	-7	-5	-3	
I_{TIMER}	Fault timer discharge current	$R_{I_DCH_CC} = 10k\Omega$, $V_{TIMER} = 2.5V$, non-fault condition	2	8	12	μA
T_{RT_SHDN}	$\overline{SHDN}$ reaction time	Trip detected at $\overline{SHDN}$ to LOAD disconnect, $IR_TC = open$, 50% to 90%		35	50	μs
V_{TIMER}	Fault timer threshold voltage	Rising; detecting a fault	98	100	102	%VREF
		Falling; detecting end of rest state	19	20	21.5	
V_{TIMER}	Fault timer discharge voltage	At full discharge state			100	mV
T_{TIMER_PD}	Fault timer trip to $\overline{SHDN}$	Rising or falling fault timer. TIMER driven with external 0V to 5V square wave			6	μs
I_{CH_CC}, I_{CH_SOA}, I_{DCH_CC}						
$V_{I_CH_CC}$	Current program voltage	$R_{I_CH_CC} = 10k\Omega$ to 100k Ω	18	20	22	%VREF
$V_{I_DCH_CC}$	Current program voltage	$R_{I_DCH_CC} = 10k\Omega$ to 100k Ω	18	20	22	%VREF
$V_{I_CH_SOA}$	Current program voltage	$V_{LINE} = 120V$, $V_{LINE} - V_{LOAD} = 100V$, $R_{I_CH_SOA} = 10k\Omega$ to 100k Ω	4.8	5	5.2	V
		$V_{LINE} = 18V$, $V_{LINE} - V_{LOAD} = 10V$, $R_{I_CH_SOA} = 10k\Omega$ to 100k Ω	0.375	0.51	0.6	

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
IR_TC						
V_{I_SET}	IR_TC accuracy	$0.2V < V_{IR_TC} < V_{VREF}$, $V_{LINE} - (V_{I_SET} + V_{IR_TC})$	-100	0	100	mV
I_{IR_TC}	IR_TC current sink	$0.4V < V_{IR_TC} < V_{VREF}$, $R_{I_DCH_CC} = 10k\Omega$	88	100	108	μA
I_{IR_TC}	IR_TC current source	$0.4V < V_{IR_TC} < V_{VREF}$, $R_{I_DCH_CC} = 10k\Omega$	-108	-100	-88	μA
V_{IR_TC}	VIR_TC Off Voltage	$R_{I_DCH_CC} = 10k\Omega$		20	100	mV
NPN Buffer at IR_TC_C and IR_TC_E pins						
$V_{be_Q_IR_TC}$	Base-emitter voltage of the internal bipolar transistor	1 μA base current	450		850	mV
$h_{fe_Q_IR_TC}$	Current gain forward mode	TBD μA collector current	15		250	-
$V_{ce(sat)_Q_IR_TC}$	Saturation voltage	100 μA collector current			100	mV
$I_{CE0_Q_IR_TC}$	Collector cutoff current	$V_E = V_B = 0V$, $V_C = 5V$			100	nA
CS_DRV						
$t_{ON_CS_DRV}$	L $\rightarrow$ H output transition	1nF capacitive load	6		50	μs
$t_{OFF_CS_DRV}$	H $\rightarrow$ L output transition	1nF capacitive load	6		50	μs
R_{CS_DRV}	Output resistance			10		k Ω
Over Temperature Detect						
TEMP _{OT}	Over temperature threshold	Shutdown (die temperature rising)	150		175	$^{\circ}C$
	Over temperature hysteresis	Reset (die temperature falling)	20	35	50	$^{\circ}C$
t_{TEMP}	Reaction time	Delay from threshold event to OT fault detection		5	50	μs

8 Thermal Properties

Thermal resistance, θ_{JB} , is provided from die to the back surface of the package. Junction temperature T_J is calculated using $T_J = T_B + (PD \times \theta_{JB})$, where T_B is the temperature maintained on the back surface of the package.

Package	Thermal Resistance	Typ	Units
CQFP-132	θ_{JB}	1.2 (estimate)	°C/W

9 Heatsink Recommendations

The LX7712 dissipates up to 6.25W ($5A^2 \times 250m\Omega$) at full normal load, and so thermal considerations are usually necessary. It is strongly recommended to use the base of the ceramic package as the surface for conducting heat from the package. The metal package top is attached to the package body at the top of relatively thin cavity walls, and so has a much higher thermal resistance from the die than the base of the package. The leads can be formed to mount the part upside down if necessary.

It is also recommended to apply a thermal interface material between the base of the package and the heat dissipater. The heat dissipater can be copper layers within a multilayer circuit board to spread heat laterally across the board, or a direct mounted dissipation element.

10 Safe Operating Area

The safe operating area curve in Figure 1 shows the maximum operating time allowed versus voltage drop between LINE input and LOAD output for a given current limit setting with a 25°C heat sink. The device can dissipate 40W indefinitely if connected to a 25°C heat sink, and that the maximum safe limit energy dissipated during a current limit pulse is 3.2J. Peak die temperature increase due to a short pulse of 3.2J is 32°C as the energy is mostly absorbed in the die initially. Junction temperature stabilizes at nominally $92^\circ\text{C} - 25^\circ = 67^\circ$ above heatsink temperature under 40W dissipation (Figure 2), with the package base rising to $92^\circ\text{C} - (40\text{W} \times 1.2^\circ\text{C/W}) = 44^\circ\text{C}$.

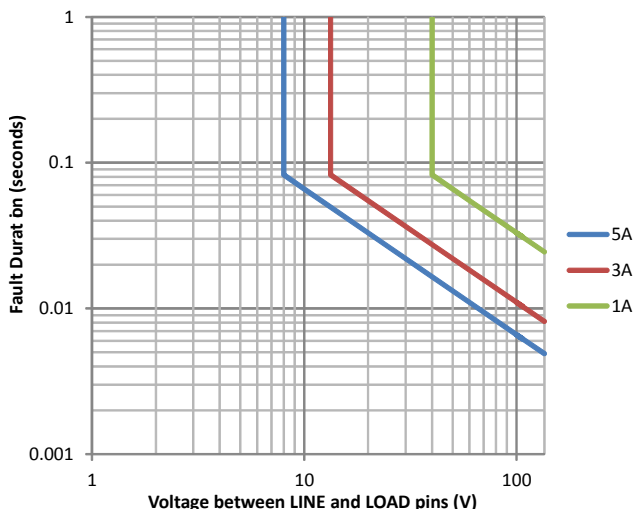


Figure 1. Maximum Safe Operating Curve

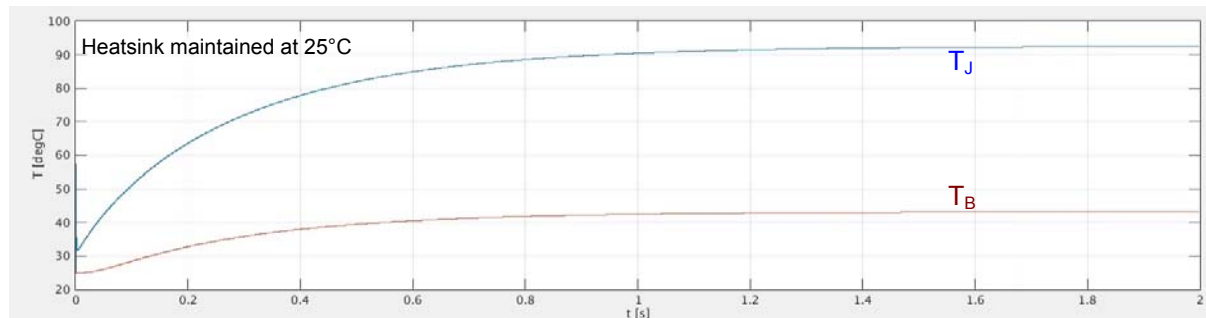


Figure 2. Die and Package Base Temperature Rise Over Time with 40W Dissipation

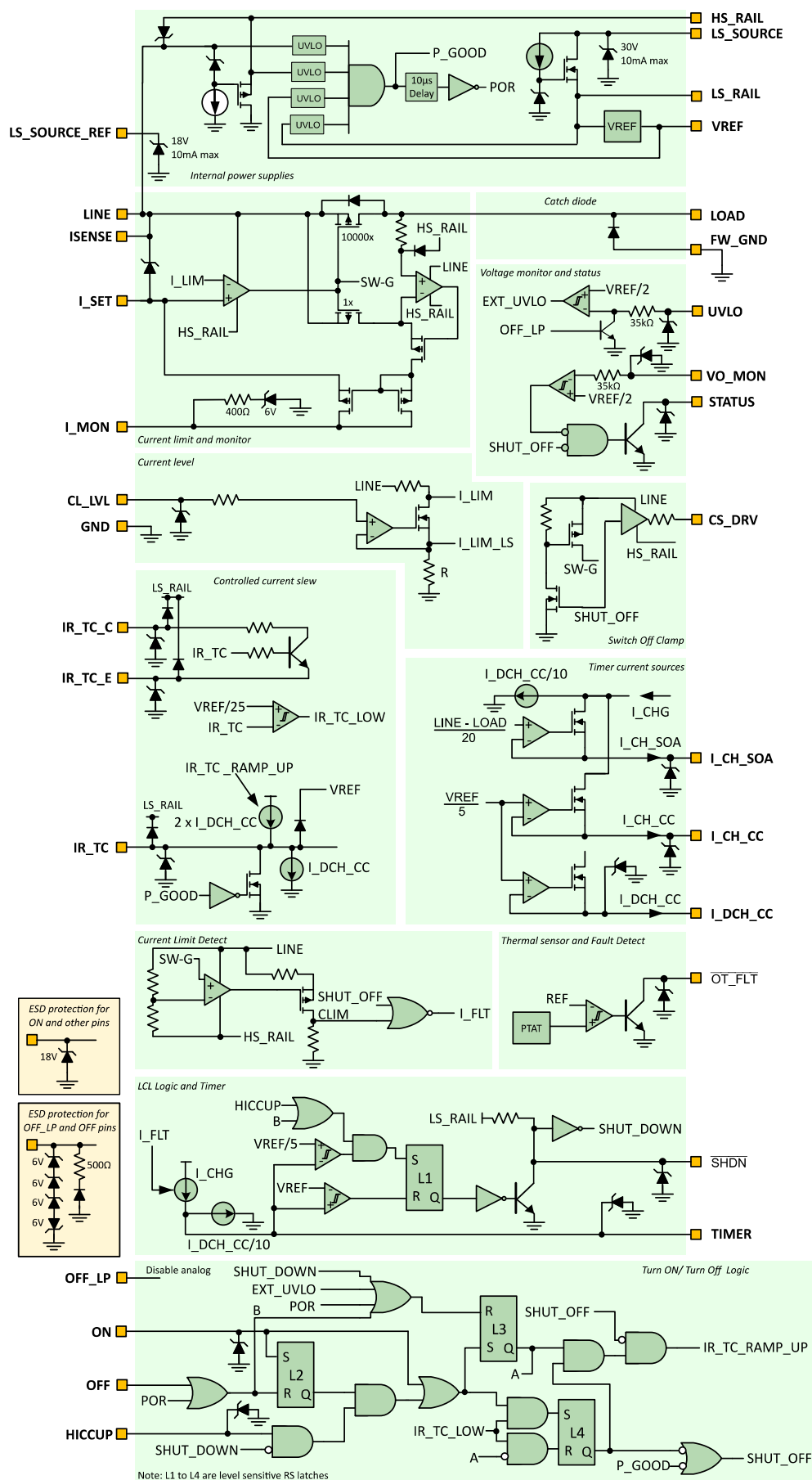


Figure 3. Functional Block Diagram

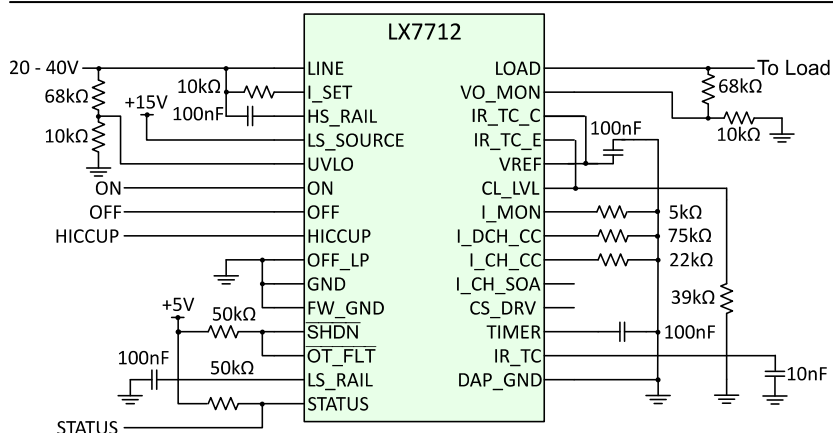


Figure 4. Example Application - Latching 4.8A Current Limit with 3.75ms Slew Time and 300ms Fault Timer

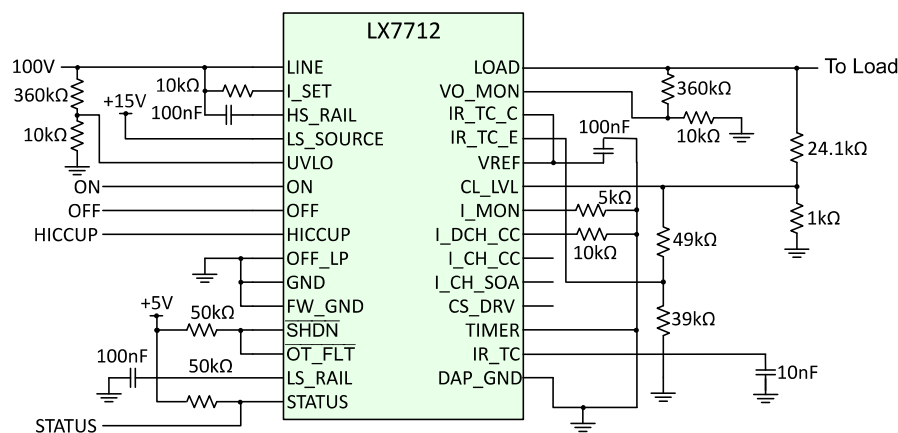


Figure 5. Example Application - Foldback 4A → 0.1A Current Limit with 50μs Slew Time

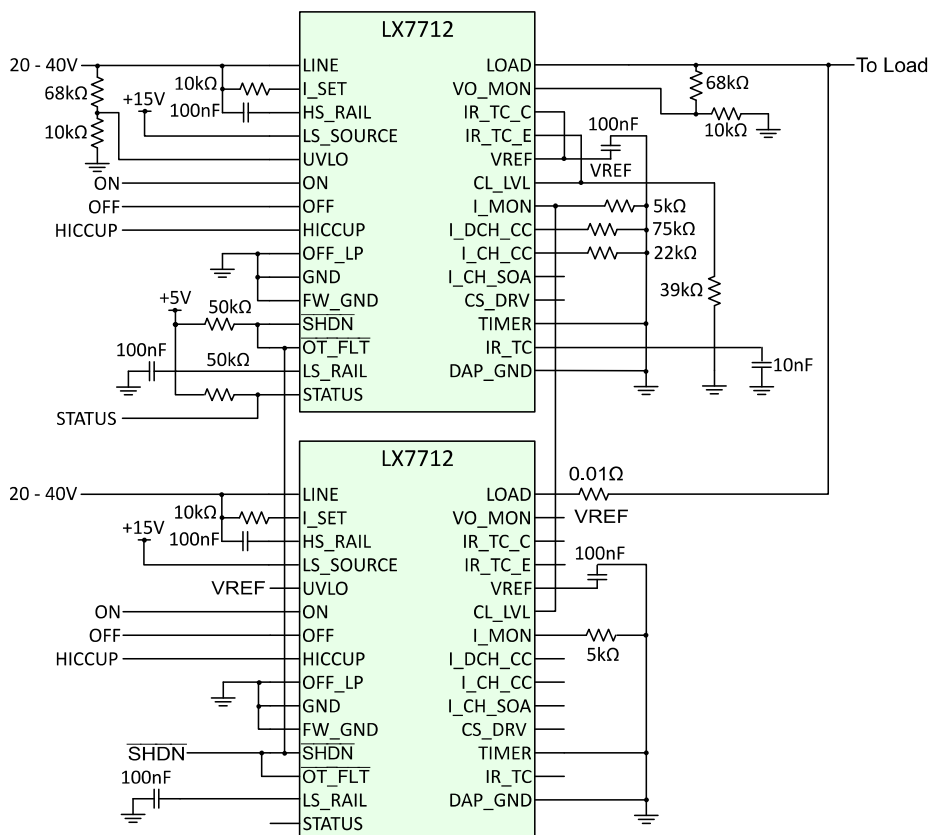


Figure 6. Example Application - Latching 9.5A Current Limit with 3.75ms Slew Time

11 LX7712 System Outline

The LX7712 is a versatile, configurable, resettable e-fuse with integrated PMOS power switch rated at 5A continuous current. The current sensing is performed using a SenseFET which contains a current sense FET buried in the main switch FET body. A closed-loop amplifier matches the operating conditions of the current sense device to the power switch, which ensures that the sense current represents a consistent fraction of the power switch current.

The LX7712's power switch has a reverse body diode, as shown in the Functional Block Diagram on page 12, which provides a path from the LOAD output to the LINE input when the power switch is turned off. See section 19 on page 27 for details how to add an external reverse PFET to block the reverse path automatically when the LX7712 is off.

The LX7712 operates as a power switch for voltages between 18V and 126V. The absolute maximum rating for the power switch is 150V, providing resilience to power line spikes.

The LX7712 functional blocks are:

- Internal power supplies and voltage reference (section 12 on page 14)
- ON, OFF, and OFF_LP control inputs (section 13 on page 16)
- STATUS output and $\overline{\text{SHDN}}$ I/O (sections 13.1 and 13.2 on page 17)
- Over-temperature detection (section 13.3 on page 17)
- Internal under-voltage lockouts and LINE and LOAD voltage monitoring and (sections 12.2 and 13.4 on page 17)
- Current monitoring system (section 14 on page 18)
- Current limiting with current ramp control, and both hard and foldback current limit options (section 15 on page 19)
- Overload fault energy integration fault timer and hiccup fault recovery fault timer (section 16 on page 20)

12 Internal Voltage Reference and Power Supplies

The LX7712 generates a 5V reference, VREF, a 10V-below-LINE output, HS_RAIL and a low-side 10V output, LS_RAIL, for the internal control circuits (Figure 7 below).

The 18V zener diode at LS_SOURCE_REF is intended for use as bias for an optional LS_SOURCE/LS_RAIL pre-regulator as discussed in section 12.4 on page 15, but can be used for other purposes. Limit current into or out from the LS_SOURCE_REF pin to $\pm 10\text{mA}$ maximum.

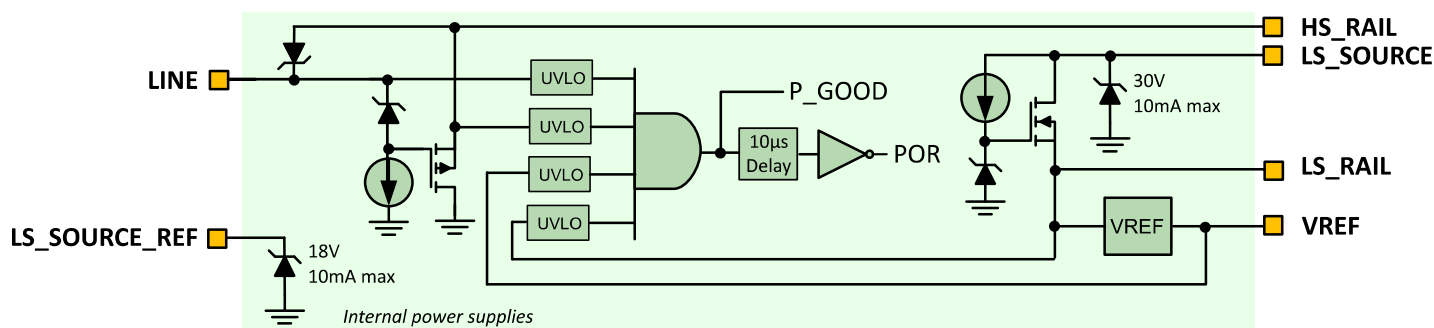


Figure 7. Internal HS_RAIL and LS_RAIL Regulators, Under Voltage Detectors, and VREF

12.1 Reference Output VREF

The 5V reference VREF is available to bias the external resistor configuration networks and is accurate to $\pm 4\%$ over LINE voltage variations with external loading up to 2mA, plus another $\pm 1\%$ tolerance over the -55°C to $+125^\circ\text{C}$ temperature range. Bypass VREF with a 100nF capacitor to GND, even if no external loading is applied.

12.2 Internal Under-Voltage Lockout

The LX7712 includes under-voltage comparators monitoring the LINE input voltage, the HS_RAIL regulated from LINE, the LS_RAIL regulated supply, and VREF. The power switch is turned off while any one of these supplies is under-voltage (Figure 7 above). If the ON input is high and both the OFF and OFF_LP inputs are low when under-voltage event(s) clear, such as after power-up, then the power switch will turn on.

12.3 HS_RAIL

HS_RAIL is the output of the internal linear regulator which floats at $10V \pm 1V$ below LINE (Figure 8 below). HS_RAIL only sinks current (acts as a return) up to 1.5mA for internal circuitry. Bypass HS_RAIL with 100nF to LINE (*not* to GND).

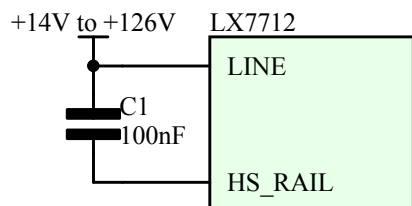


Figure 8. HS_RAIL Supply Connections

12.4 LS_SOURCE and LS_RAIL

LS_RAIL is the output of an internal linear regulator at LS_SOURCE which delivers $10V \pm 1V$ above GND. LS_SOURCE is ideally connected to a local supply voltage in the range 12V to 20V. Bypass LS_RAIL with 10nF to GND. LINE can range from 18V to 126V independent of the LS_SOURCE voltage, with no sequencing requirements.

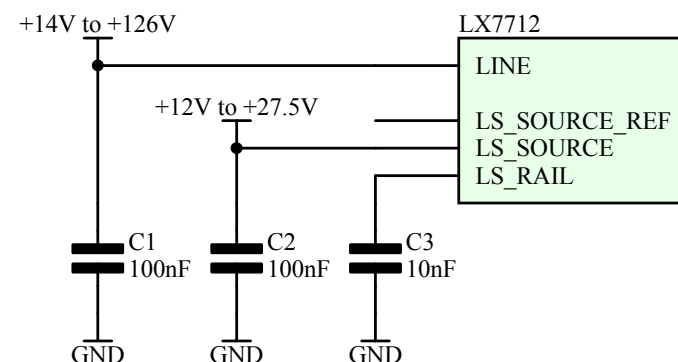


Figure 9. LS_SOURCE and LS_RAIL Supply Connections

If a suitable low voltage supply for LS_SOURCE is not available, then a simple pre-regulator can be added to drop the supply from another rail, typically LINE (Figure 10 below).

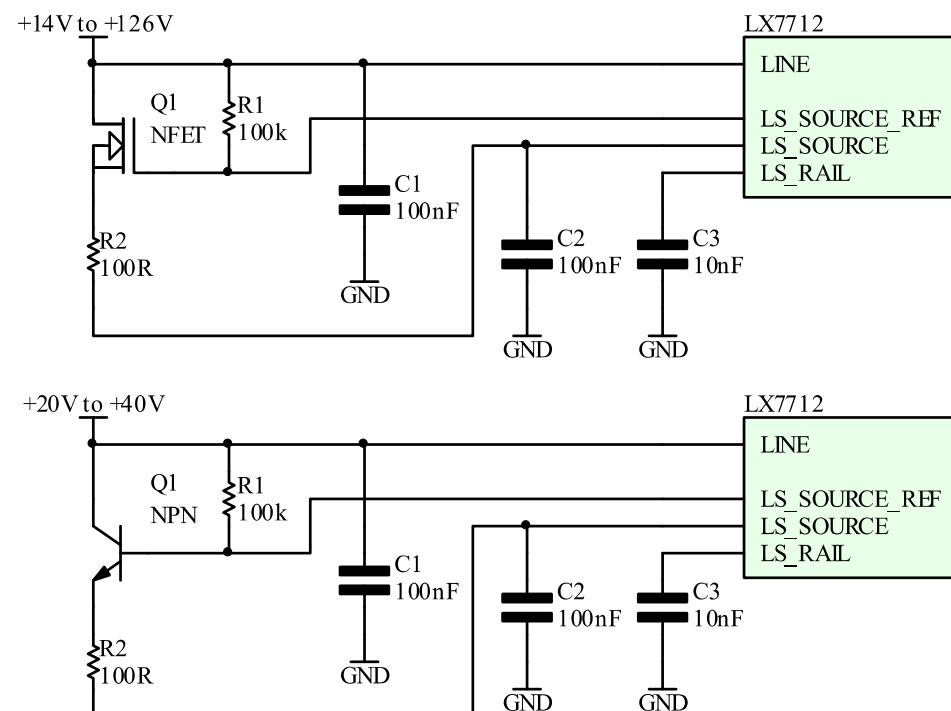


Figure 10. LS_SOURCE Pre-Regulator Option for High LINE Voltages

The pre-regulator is a source/emitter follower using an NMOS or NPN pass transistor biased by the internal 18V zener at LS_SOURCE_REF shown in Figure 7. The 100Ω resistor R2 limits the peak charging current into the capacitor C2 on power-up. Increase R2's resistance if desired to move dissipation from Q1 to R2. The NPN version can be designed for higher voltages than shown in the example by adjusting the value of R1. Ensure that the current entering LS_SOURCE_REF does not exceed 10mA.

The LS_SOURCE/LS_RAIL regulator supports a 5mA additional external load on LS_RAIL, in addition to the 10mA max internal load. The maximum allowed regulator dissipation is 225mW. Limit the LS_SOURCE supply to 27.5V with no external load on LS_RAIL, or 24V with a 5mA additional external load on LS_RAIL.

13 On and Off Controls

The basis of the power switch's on/off mechanism is an internal RS latch operated by the ON and OFF logic inputs, which initiate a programmable slew rate control which limits the rate of the load current increase during turn-on, and decrease during turn-off (see the Slew Rate section on page 19).

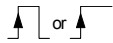
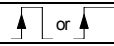
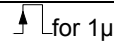
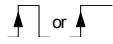
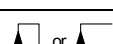
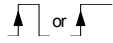
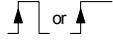
Control Mode	UVLO Input pin 27	SHDN I/O pin 47	ON Input pin 40	OFF Input pin 39	OFF_LP Input pin 38
Normal On/Off Operation in either LCL Mode (HICCUP = low or hi-z) or RLCL Mode (HICCUP = high)					
Switch on via ON input with slew control in LCL Mode (HICCUP = low or hi-z))	V _{UVLO} > VREF/2	High	 or 	Low	Low
Switch on via ON input with slew control in RLCL Mode (HICCUP = high)			High	Low	Low
Switch off with slew control via OFF input		High	x	 or 	Low
Switch off instantly into low power mode via OFF_LP input		High	x	x	High
Switch off instantly into low power mode via OFF and OFF_LP inputs connected together		High	x	High	
Switch off with slew control, and then sometime during or after the slew time enter low power mode via OFF and OFF_LP inputs connected together		High	x	 for 1μs to 10μs to initiate switch off with slew control. During or after slew time,  to enter low power mode	
Current Limit Fault Handling in LCL Mode (HICCUP = low or hi-z)					
Automatic switch off with slew control due to a timed-out and latched current limit fault	V _{UVLO} > VREF/2	Internally pulled down	 or 	Both low since power switch was turned on via ON input	
Check whether LX7712 is still in the cool-down timer period; the power switch cannot be turned-on again until the cool-down period has ended and SHDN → high (OFF and OFF_LP separate)		Internally pulled down (in cool-down period) → high (when cool-down ends and OFF is high)	x	High	Low
Check whether LX7712 is still in the cool-down timer period; the power switch cannot be turned-on again until the cool-down period has ended and SHDN → high (OFF and OFF_LP inputs connected together)		Internally pulled down (in cool-down period) → high (when cool-down ends and OFF is high)	x	 for 1μs to 10μs to clear SHDN	Low
Switch back on via ON input with slew control once the cool-down period has ended		Must be high before; remains high after	 or 	Low	Low
Current Limit Fault Handling in RLCL Mode (HICCUP = high)					
Automatic switch off with slew control due to a timed-out and latched current limit fault	V _{UVLO} > VREF/2	Internally pulled down	 or 	Both low since power switch was turned on via ON input	
Automatic switch on with slew control once the cool-down period has ended		High	 or 	Both low since power switch was turned on via ON input	
Behavior Under Under-Voltage Conditions and using SHDN pin					
Automatic switch off due to under-voltage on either LINE or LS_RAIL	x	x	x	x	x
Switch off with slew control via SHDN pin	V _{UVLO} > VREF/2	Externally pulled down	x	x	x
Switch off with slew control via UVLO pin	V _{UVLO} < VREF/2	x	x	x	x

Table 1. On and Off Controls

The power switch is turned on by either a logic-high level or a high pulse $\geq 1\mu\text{s}$ on the ON input. The ON control is overridden, and the power switch turned off, by either a logic-high level or a high pulse $\geq 1\mu\text{s}$ on the OFF logic input, by a logic-high level on the OFF_LP or $\overline{\text{SHDN}}$ inputs, by the UVLO comparator input, by a latched current limit fault, or by under-voltage on a supply rail. When operating with $V_{\text{LINE}} \leq 13\text{V}$, take care to protect the OFF input from negative going glitches below -0.5V since these can put the internal RS latch into the OFF state and turn off the load.

There is negligible difference in LX7712 power consumption whether the power switch is on or off. The optional OFF_LP input reduces power consumption for long standby periods by powering down the internal HS_RAIL and LS_RAIL regulators and therefore much of the internal circuitry by. Note:

- Taking OFF_LP high overrides the ON and OFF inputs
- The OFF_LP input is not latched, unlike the ON and OFF inputs, and must be kept high during low power mode
- The OFF and OFF_LP inputs can be tied together, and a $1\mu\text{s}$ to $10\mu\text{s}$ pulse high used to set the internal RS latch OFF without the LX7712 entering low power mode ($C_{\text{LS_SOURCE}} \geq 100\text{nF}$)

13.1 Status Output STATUS

The open-collector STATUS output is low when the power switch is on and the VO_MON comparator indicates the LOAD voltage is above the user-configured LOAD minimum voltage. Fit a resistor from STATUS to a supply up to 6V to provide the desired logic high output.

13.2 Shutdown I/O $\overline{\text{SHDN}}$

The $\overline{\text{SHDN}}$ pin is an open-collector I/O. As an output, a low logic output signal indicates that an LCL timeout has triggered the shutdown latch. $\overline{\text{SHDN}}$ can also be used as a shutdown input from another device, and multiple LX7712s can interconnect $\overline{\text{SHDN}}$ to cross-couple shutdown events. Fit a resistor from $\overline{\text{SHDN}}$ to a supply up to 6V to provide the desired logic high output.

13.3 Over Temperature Output $\overline{\text{OT_FLT}}$

The $\overline{\text{OT_FLT}}$ output trips active low on die over-temperature, with 50°C typical hysteresis (Figure 11 below). $\overline{\text{OT_FLT}}$ can be connected to $\overline{\text{SHDN}}$ to shut down the LX7712 automatically during over-temperature faults. Fit a resistor from $\overline{\text{OT_FLT}}$ to a supply up to 6V to provide the desired logic high output, unless connected to $\overline{\text{SHDN}}$ with an existing pullup resistor.

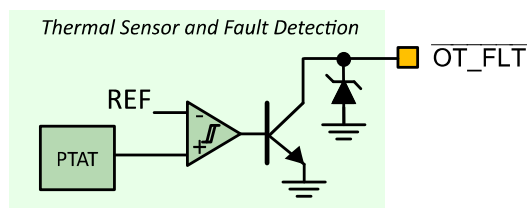


Figure 11. Over-Temperature Fault Output

13.4 External Voltage Monitor Inputs UVLO and VO_MON

The LX7712 includes two under-voltage comparators with a threshold of $V_{\text{REF}}/2$, nominally 2.5V (Figure 12 below).

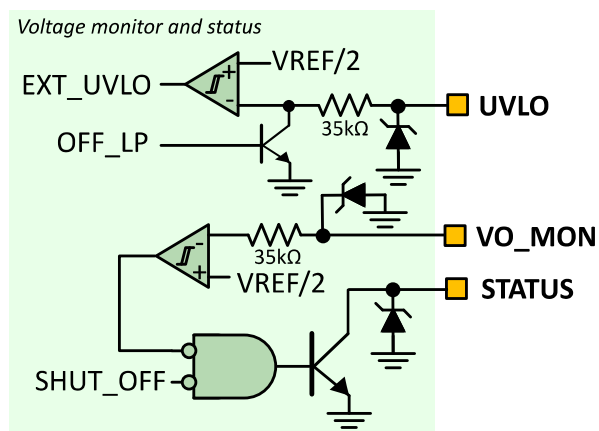


Figure 12. External UVLO

UVLO is intended to monitor the LINE input via a 2-resistor potential divider from LINE to GND. If a voltage under $V_{REF}/2$ is detected on UVLO, a power switch turn off with slew rate control is initiated. When the voltage on the UVLO pin exceeds $V_{REF}/2$, the power switch will remain off or turn on with slew rate control depending on the state of the ON, OFF, and OFF_LP inputs. Tie UVLO to VREF if unused.

VO_MON is intended to monitor the LOAD output via a 2-resistor potential divider from LOAD to GND. If a voltage under $V_{REF}/2$ is detected on VO_MON, the STATUS output goes hi-z to indicate that LOAD output is under-voltage. Tie VO_MON to VREF if unused.

A 10kΩ resistor is recommended for the GND-side resistor in the potential dividers. The value of the high-side resistor (to LINE or LOAD) is therefore $\{(4 \times V_{TRIP}) - 10\}$ kΩ, where V_{TRIP} is the desired nominal under-voltage trip threshold.

14 Current Monitoring and Current Limit Circuit

The LX7712 contains a high-side PFET as the switch pass element. Since the switch is high-side, the load current sensing and current limit control circuit are high-side also. The sensed load current, I_{SET} , is also mirrored from being V_{LINE} referred to being GND referred. This GND referenced copy of the load current measurement is at the I_{MON} pin.

The current limit itself is set by the I_{LIM} voltage. I_{LIM} is also V_{LINE} referred, but is level shifted up from the GND referred components that configure it (Figure 14 on page 19). I_{LIM} may slewed up and down for soft start/stop (section 15.1 on page 19), and is configured with an external resistor network to set up the current limit.

The LX7712 uses a SenseFET architecture comprising a current sense PFET buried in the power switch PFET body. The current sense PFET is 1/10,000 the size of the power switch PFET, and mirrors 1/10,000 of the load current if its V_{DS} is kept the same as the power switch PFET's V_{DS} , which is $V_{LINE} - V_{LOAD}$. This is managed by the sense amplifier (Figure 13).

The sense amplifier sources the sense current (1/10,000 of the switch current) into the right-hand side of the sense current mirror. This mirror sinks the same current from the LINE input supply through the external resistor R_{I_SET} via the I_{SET} pin. The combined current from the two sides of the mirror, 1/5,000 of the switch current, goes to ground through the external resistor R_{I_MON} via the I_{MON} pin. The voltage at I_{MON} provides a ground-referenced measure of the load current passing through the switch. The minimum current sourced from I_{MON} is typically 40μA (1μA minimum over the full operating temperature range) to allow open wire fault detection of the current sensing wiring.

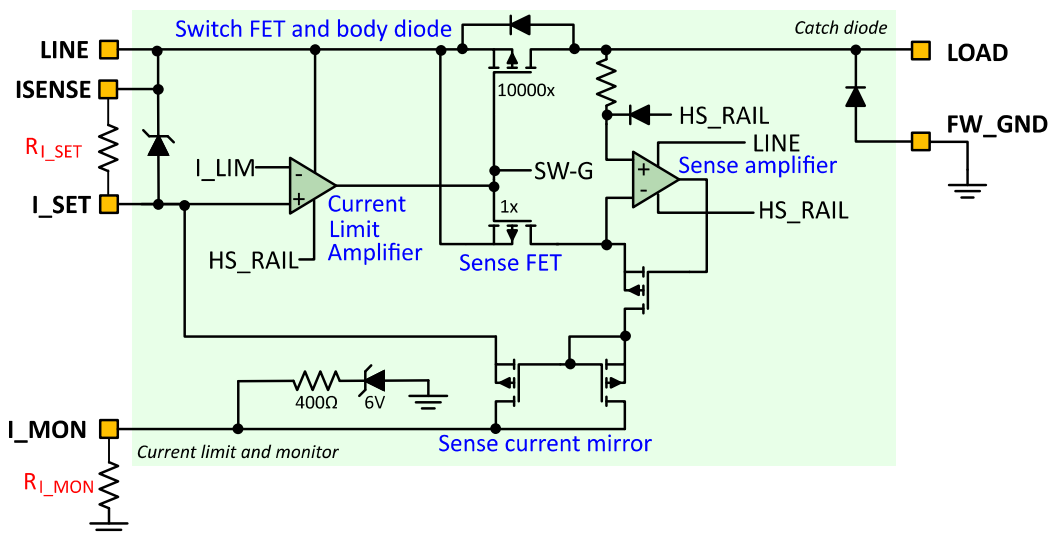


Figure 13. Power Switch and Current Sense Circuit

The maximum value for R_{I_MON} is 5kΩ maximum for a 5A current limit requirement, with $V_{LINE} \geq 22V$. This sets a 5V full-scale output V_{I_MON} for load current monitoring (Equation 1). For $V_{LINE} < 22V$, the maximum full-scale output is 1V, so use $R_{I_MON} = 1k\Omega$ maximum for a 5A current limit. There is no lower limit for R_{I_MON} , but there must be a DC path to GND from the I_{MON} pin. Short I_{MON} to GND if load current monitoring isn't required.

$$\text{Equation 1. } V_{I_MON} = \frac{I_{LOAD} \times R_{I_MON}}{5000} \text{ V}$$

If the LX7712 is configured for a lower than 5A current limit (I_{LOAD}), then the value of R_{I_MON} can be increased to maintain a 5V ($V_{LINE} \geq 22V$) or 1V ($V_{LINE} < 22V$) full scale output V_{I_MON} at the lower current. For example, use $R_{I_MON} = 12.5k\Omega$ for a 2A current limit application (Equation 2).

$$\text{Equation 2. } R_{I_MON(max)} = \frac{V_{I_MON} \times 5000}{I_{LOAD}} = \frac{5 \times 5000}{I_{LOAD}} = \frac{25000}{I_{LOAD}} \Omega \text{ for } V_{LINE} \geq 22V$$

$$\text{Equation 3. } R_{I_MON(max)} = \frac{V_{I_MON} \times 5000}{I_{LOAD}} = \frac{1 \times 5000}{I_{LOAD}} = \frac{5000}{I_{LOAD}} \Omega \text{ for } V_{LINE} < 22V$$

15 Slew Rate Control (Current Limiting) During Turn-On and Turn-Off

The LX7712 has configurable current limiting with slew rate control during power switch turn-on and turn-off. The power switch is in one of three modes when not in low-power shutdown:

- Off
- On: below current limit threshold, so switch is fully enhanced (120mΩ typical)
- On: current limit threshold has been reached, so in current limiting mode (subject to fault timer setting)

See the Fault Timer section 16 on page 20 on setting how long a sustained over-current fault (or multiple short over-current fault in quick succession) can be sustained before the power switch is turned off after the current limit trip point has been detected. The LX7712 does not distinguish between current limiting due to slew rate control and current limiting due to overload. If the fault timer is enabled, ensure that the fault time delay is set to longer than the slew time to avoid fault timeout when the power switch is turned on.

15.1 Slew Rate Limiting

The slew rate control limits the rate of the load current increase when the power switch is turned on, and an identical ramp down when the power switch is turned off. During the slew time, the power switch current limit ramps up from 0A to the configured current limit. The slew time is set by the combination of an external capacitor C_{IR_TC} on the IR_TC pin, and the constant current I_{DCH_CC} set by resistor R_{DCH_CC} on the I_DCH_CC pin (Figure 14 on page 19).

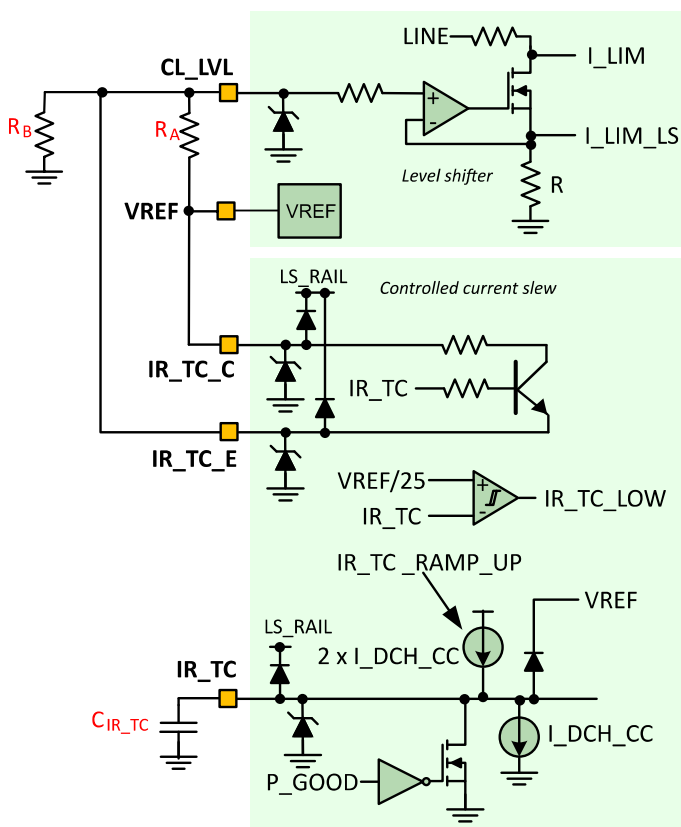


Figure 14. Slew Control and Current Limiting Without Foldback

At power switch turn-on, C_{IR_TC} starts discharged, and charges from 0V to VREF with constant current I_{DCH_CC} . At power switch turn-off, C_{IR_TC} discharges from VREF to 0V at I_{DCH_CC} , causing a matching power switch current limit ramp down.

The value of resistor R_{DCH_CC} is normally selected to suit the fault timer (section 16 on page 20). If the fault timer function is disabled, then select a value for R_{DCH_CC} in the range 10k Ω to 100k Ω from the I_{DCH_CC} pin to GND to suit the slew control requirements. Leave the IR_{TC} pin open (no external capacitor C_{IR_{TC}}) to select the fastest slew rate.

The complete slew time is the time taken to charge $C_{IR\ TC}$ from 0V to V_{REF} with constant current $I_{DCH\ CC}$:

$$\text{Equation 4: } t_{\text{SLEW}} = \frac{C_{\text{IR_TC}} \times V_{\text{REF}}}{I_{\text{DCH_CC}}} \text{ s}$$

Substituting $I_{DCH_CC} = \frac{V_{REF}}{5 \times R_{DCH_CC}}$ A from Table 2 on page 22, this simplifies to:

Equation 5: $t_{SLEW} = 5 \times C_{IR\ TC} \times R_{DCH\ CC} \text{ s}$

For example, the ramp time using $C_{IR\ TC} = 100nF$ and $R_{DCH\ CC} = 100k\Omega$ is $t_{STLEW} = 5 \times 100n \times 100k = 50ms$.

16 Fault Timer

The LX7712 uses a fault timer to determine how long an over-current fault can be sustained before the power switch is turned off. This fault timer is the LX7712's primary safe dissipation manager. The secondary system is the die over-temperature detection and associated auto-shutdown logic. The fault timer is configured by the user initially to maintain a fault energy pulse under the LX7712's 3.2J rating, and then to allow enough time for the system to remove the heat.

The fault timer operates as a dual-slope integrator around external capacitor C_{TIMER} , and external resistors $R_{\text{CH_CC}}$, $R_{\text{CH_SOA}}$, and $R_{\text{DCH_CC}}$ (Figure 15 below). The capacitor charge/discharge time constants emulate the cumulative ongoing energy absorption of the power switch, and the subsequent conduction of that thermal energy into the system's heatsink.

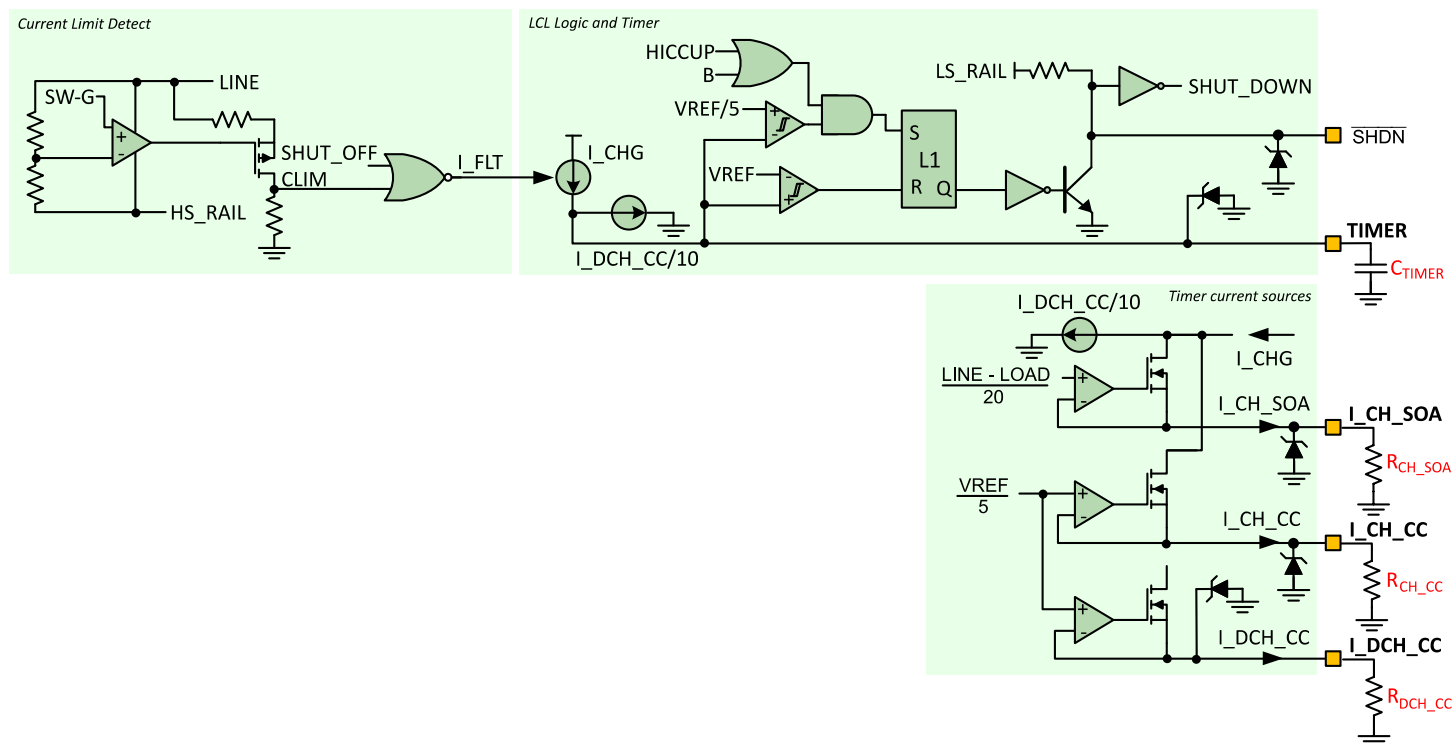


Figure 15. Fault Timer Current Sources and Sink

To disable the fault timer, tie the TIMER pin to GND, leave the I_{CH_SOA} and I_{CH_CC} pins open, and fit resistor R_{DCH_CC} in the range 10kΩ to 100kΩ from the I_{DCH_CC} pin to GND. The current I_{DCH_CC} set by R_{DCH_CC} is used for slew control (see the Slew Rate Limiting section 15.1 on page 19) even if the fault timer is unused.

R_{CH_CC} and R_{CH_SOA} set capacitor *charging* currents and define the time that an over-current fault is sustained before the power switch is turned off. Resistor R_{CH_CC} sets a fixed charge current. Resistor R_{CH_SOA} sets a charge current that is proportional to power switch dissipation, therefore varying with time depending on the nature of the load fault. The fault timer latches the power switch off when the voltage across C_{TIMER} rises to VREF (Figure 16 on page 21).

R_{DCH_CC} sets the capacitor *discharging* current and defines the time that the power switch must remain off. This emulates the heatsink's thermal time constant to dissipate the heat built up during a current limit fault. R_{DCH_CC} discharges C_{TIMER} from VREF to a trip point of VREF/5, after which the power switch can be turned back on. Note that the current set by R_{DCH_CC} is used as a reference current (I_{DCH_CC}) by the current limit and slew control circuits (Section 15 on page 19).

If any over-current fault is of too short a duration to trigger the fault timer threshold, C_{TIMER} still retains the voltage it charged to during the fault. This provides a cumulative effect, so multiple short over-current pulses occurring in a short period of time (before the discharge current clears C_{TIMER}) can eventually trigger the fault timer threshold.

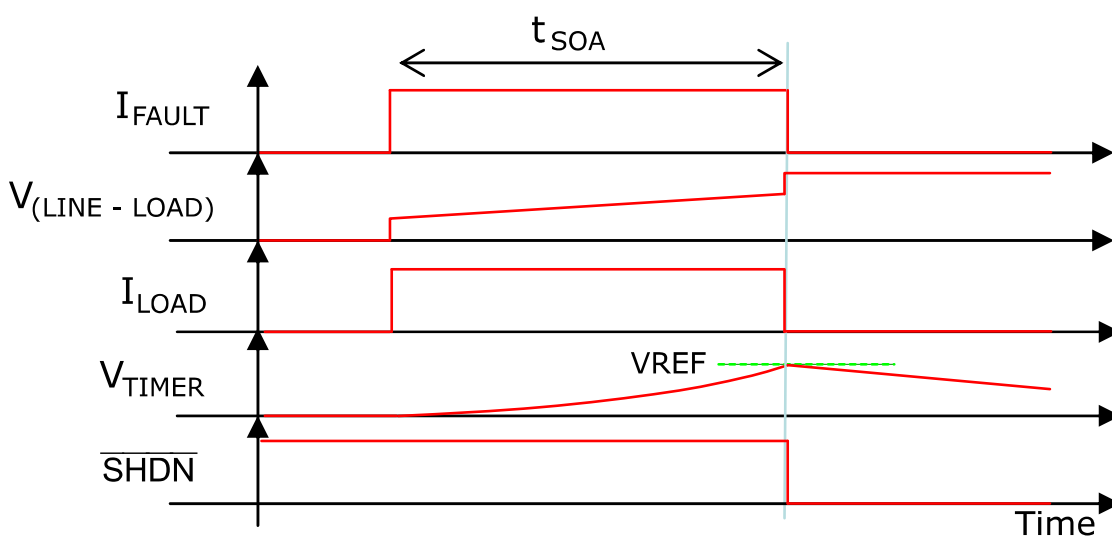


Figure 16. Power Switch Energy Rising During Fault

In LCL (latched current limiting) mode, the power switch remains latched off after the load switch is turned off due to an over-current fault. The LX7712 can be restarted through the ON logic input after the fault timer discharge time (C_{TIMER} discharged to VREF/5). To enable LCL mode, tie the HICCUP pin 13 to GND.

In RLCL (retriggerable latched current limiting) or hiccup mode, the power switch remains off until the fault timer discharge time has tripped (C_{TIMER} discharged to VREF/5), and then restarts automatically. To enable RLCL/hiccup mode, tie the HICCUP pin 13 to logic high (3.3V, 5V, or the 5V VREF pin 20).

16.1 Fault Timer Component Selection

The fault timer equations are given in Table 2 below, where:

- R_{CH_CC} is the external resistor from I_{CH_CC} pin 21 to GND which sets the current I_{CH_CC}
- R_{CH_SOA} is the external resistor from I_{CH_SOA} pin 22 to GND which sets the current I_{CH_SOA}
- R_{DCH_CC} is the external resistor from I_{DCH_CC} pin 23 to GND which sets the current I_{DCH_CC}
- C_{TIMER} is the external capacitor from TIMER pin 25 to GND
- VREF is the internal 5V reference voltage on pin 20
- V_{LINE} is the line input to the power switch, pins 1 to 8, and 48
- V_{LOAD} is the voltage at the output of the power switch, pins 29 to 37

The preferred range of values for R_{CH_CC}, R_{CH_SOA}, and R_{DCH_CC} are 10kΩ to 100kΩ, because the fault timer trip voltages are guaranteed in the electrical characteristics for this range. However, resistor currents up to 800μA may be programmed. This current limit corresponds to minimum resistor values shown in Table 2.

Resistor (minimum Ω)	Fault Timer Behavior	Constant Current Equation	Resistance Calculation (at nominal $V_{REF} = 5V$)
R_{CH_CC} ($\geq 1.25k\Omega$)	Sets a fixed charge current into capacitor C_{TIMER} and therefore sets a fixed time to power switch turn-off after an over-current fault	$I_{CH_CC} = \frac{V_{REF}}{5 \times R_{CH_CC}} \text{ A}$	$R_{CH_CC} = \frac{1}{I_{CH_CC}} \Omega$
R_{CH_SOA} ($\geq 7.5k\Omega$, $V_{LINE}=120V$) ($\geq 3.25k\Omega$, $V_{LINE}=52V$)	Sets a variable charge current into capacitor C_{TIMER} proportional to power switch voltage drop. This emulates the power switch's safe operating area (SOA) for energy absorption	$I_{CH_SOA} = \frac{V_{LINE} - V_{LOAD}}{20 \times R_{CH_SOA}} \text{ A}$	
R_{DCH_CC} ($\geq 1.25k\Omega$)	Sets a fixed discharge current of $I_{DCH_CC}/10$ from capacitor C_{TIMER} and therefore sets a fixed time after power switch turn-off before hiccup	$I_{DCH_CC} = \frac{V_{REF}}{5 \times R_{DCH_CC}} \text{ A}$	$R_{DCH_CC} = \frac{1}{I_{DCH_CC}} \Omega$

Table 2. Fault Timer Charge/Discharge Equations

The final charging current for the fault timer capacitor is the sum of I_{CH_CC} and I_{CH_SOA} :

Equation 6. $I_{CHG} = I_{CH_CC} + I_{CH_SOA} \text{ A}$

The final discharging current for the fault timer capacitor is a tenth of I_{DCH_CC} :

Equation 7. $I_{DISCHG} = \frac{I_{DCH_CC}}{10} \text{ A}$

16.1.1 EXAMPLE FIXED-FAULT TIMER COMPONENT DESIGN 1 (USING R_{CH_CC} AND R_{DCH_CC} ONLY)

Example specification: $V_{LINE} = 22V$ to $38V$, $I_{LIM} = 5A$, $E_{LIM} = 2J$, over-current fault dissipation recovery time = 300ms

To calculate the energy when R_{CH_CC} is the only setting for the fault timer, use the worst-case limit where there is the full V_{LINE} across the power switch during the fault:

Equation 8. $E_{LIM} = I_{LIM} \times V_{LINE} \times t = (I_{LIM} \times V_{LINE} \times C_{TIMER} \times 5 \times R_{CH_CC}) \text{ J}$

since: $t = \frac{C_{TIMER} \times V_{REF}}{I_{CH_CC}} = (C_{TIMER} \times 5 \times R_{CH_CC}) \text{ s}$

Rearranging Equation 8:

Equation 9. $C_{TIMER} = \frac{E_{LIM}}{I_{LIM} \times V_{LINE} \times 5 \times R_{CH_CC}} \text{ F}$

The recommended range of values for R_{CH_CC} is $10k\Omega$ to $100k\Omega$, so selecting the initial $R_{CH_CC} = 22k\Omega$ and putting the requirements into Equation 9 to calculate C_{TIMER} :

$$C_{TIMER} = \left(\frac{2}{5 \times 38 \times 5 \times 22k} \right) = 96nF$$

Selecting 100nF as the nearest standard capacitor value, and recalculate R_{CH_CC} (if desired):

$$R_{CH_CC} = \left(\frac{2}{5 \times 38 \times 5 \times 100n} \right) = 21.05k\Omega$$

The discharge current I_{DCH_CC} is calculated using the 300ms recovery time specified in the example, allowing R_{DCH_CC} to be determined. During this time, $I_{DISCHG} = I_{DCH_CC}/10$ discharges C_{TIMER} from V_{REF} to the $V_{REF}/5$ trip point, which is a ΔV of 4/5ths V_{REF} :

$$I_{DISCHG} = \frac{C_{TIMER} \times (0.8 \times V_{REF})}{t} = \frac{100n \times 4}{0.3} = 1.33\mu A$$

Therefore $R_{DCH_CC} = \frac{1}{10 \times I_{DISCHG}} = \frac{1}{10 \times 1.33\mu} = 75k\Omega$

16.1.2 EXAMPLE SOA-FAULT TIMER COMPONENT DESIGN 2 (USING R_{CH_CC} , R_{CH_SOA} AND R_{DCH_CC})

Example specification: $V_{LINE} = 22V$ to $38V$, $I_{LIM} = 5A$, $E_{LIM} = 2J$, over-current fault dissipation recovery time = $2s$

In this example, R_{CH_SOA} is used to adjust the timeout according to the real time voltage across power switch during the fault. However, R_{CH_CC} is also used to set a small fraction of the minimum timeout delay (5% to 10%) independently, to guarantee a reasonably short timeout in the event of a soft fault. A soft fault trips the over-current threshold but has sufficiently high resistance that the voltage drop across the power switch remains small when current limiting. If R_{CH_SOA} is used to adjust the timeout alone, then the timeout would be long in such a fault scenario with a low voltage drop across the power switch.

Since the capacitor C_{TIMER} will be charged simultaneously from two sources (I_{CH_SOA} and I_{CH_CC}), Equation 8 from the first example is rearranged to reflect the sum of these currents instead of a single resistor:

Equation 10.
$$E_{LIM} = I_{LIM} \times V_{LINE} \times t = \frac{I_{LIM} \times V_{LINE} \times C_{TIMER} \times 5}{I_{CH_SOA} + I_{CH_CC}} J$$

since:
$$t = \frac{C_{TIMER} \times V_{REF}}{I_{CH_SOA} + I_{CH_CC}} = \frac{C_{TIMER} \times 5}{I_{CH_SOA} + I_{CH_CC}} s$$

Rearranging Equation 10:

Equation 11.
$$C_{TIMER} = \frac{E_{LIM} \times (I_{CH_SOA} + I_{CH_CC})}{I_{LIM} \times V_{LINE} \times 5} F$$

Select $200\mu A$ current (split to 90% from I_{CH_SOA} , 10% from I_{CH_CC}) into C_{TIMER} at worst case dissipation point $V_{LINE} = 38V$ and $V_{LOAD} = 0V$. Putting our requirements into Equation 11 to calculate C_{TIMER} :

$$C_{TIMER} = \left(\frac{2 \times 200\mu}{5 \times 38 \times 5} \right) = 421nF$$

Selecting $470nF$ as the nearest standard capacitor value, and recalculating the charging current:

$$I_{CH_SOA} + I_{CH_CC} = \frac{C_{TIMER} \times I_{LIM} \times V_{LINE} \times 5}{E_{LIM}} = \frac{470n \times 5 \times 38 \times 5}{2} = 233\mu A$$

From this $I_{CH_SOA} = 0.9 \times 233\mu A = 210\mu A$ and $I_{CH_CC} = 0.1 \times 233\mu A = 23\mu A$. Now R_{CH_CC} and R_{CH_SOA} can be calculated. R_{CH_SOA} is calculated at the worst-case limit where there is the full V_{LINE} across the power switch during the fault:

$$R_{CH_CC} = \frac{1}{I_{CH_CC}} = \frac{1}{23\mu} = 43.5k\Omega$$

$$R_{CH_SOA} = \frac{V_{LINE} - V_{LOAD}}{20 \times I_{CH_SOA}} = \frac{38 - 0}{20 \times 233\mu} = 8.15k\Omega$$

The shortest time from over-current fault to fault timer cutoff is when there is the full V_{LINE} across the power switch:

$$t = \frac{C_{TIMER} \times V_{REF}}{I_{CH_SOA} + I_{CH_CC}} = \frac{470n \times 5}{233\mu} = 10.1ms$$

The longest time from over-current fault to fault timer cutoff is when there is essentially no voltage across the power switch:

$$t = \frac{C_{TIMER} \times V_{REF}}{I_{CH_CC}} = \frac{470n \times 5}{23\mu} = 102ms$$

The discharge current I_{DCH_CC} is calculated using the 2s recovery time specified in the example, allowing R_{DCH_CC} to be determined. During this time, I_{DCH_CC} discharges C_{TIMER} from V_{REF} to the $V_{REF}/5$ trip point, which is a ΔV of 4/5ths V_{REF} :

$$I_{CH_SOA} = \frac{C_{TIMER} \times (0.8 \times V_{REF})}{t} = \frac{0.47\mu \times 4}{2} = 0.94\mu A$$

$$\text{Therefore: } R_{DCH_CC} = \frac{1}{10 \times I_{DCH_CC}} = \frac{1}{10 \times 0.94\mu} = 106.4k\Omega$$

17 Current Limit Trip Point

The current limit trip point is set by the voltage at the CL_LVL pin, and follows the equation $I_{TRIP} = V_{CL_LVL}$ with $R_{I_SET} = 10k\Omega$. The trip is detected by monitoring the power switch's gate drive voltage (SW-G in Figure 3 on page 12), which reduces when current limiting starts to occur.

Trip point accuracy is highest at $I_{LOAD_TRIP_4V}$ and $I_{LOAD_TRIP_1V}$ for the conditions $V_{CL_LVL} = 4V$ and $V_{CL_LVL} = 1V$ respectively, with $R_{I_SET} = 10k\Omega$. These two trip points are 3.8A -0.45A/+0.35A and 0.8A -0.5A/+0.25A. For other trip points in the range $1V \leq V_{CL_LVL} \leq 5V$, there is an additional $I_{LOAD_TRIP_LINEARITY}$ error budget of $\pm 1\%$. The R_{I_SET} resistor tolerance and the V_{REF} potential divider setting I_{LOAD_TRIP} must also be taken into account.

For efuse applications, the design procedure ensures that the desired working load current can pass under worst case tolerances without tripping the current limit.

For a 0.8A minimum current trip limit, we use the $I_{LOAD_TRIP_1V}$ specification with $R_{I_SET} = 10k\Omega$:

$$\text{Equation 12. } I_{TRIP_MIN} = 0.8 - I_{LOAD_TRIP_1V_MIN} = 0.8 + 0.5 = 1.3 A$$

And calculate the minimum voltage at the CL_LVL pin:

$$\text{Equation 13. } V_{CL_LVL_MIN} = I_{TRIP_MIN} = 1.3 V$$

Presuming that this voltage is derived with a 2-resistor (R_A and R_B) potential divider from V_{REF} (Figure 17),

$$\text{Equation 14. } V_{CL_LVL_MIN} = 1.5 V = V_{REF_MIN} \times \frac{R_B}{R_A + R_B} \times (1 - R_{tolAB}) \times (1 - R_{tolI_SET})$$

where T_{tolAB} and R_{tolI_SET} are the tolerances of the R_A and R_B resistors and R_{I_SET} resistor.

$$\text{Equation 15. } I_{TRIP} = \frac{V_{CL_LVL} \times 10000}{R_{I_SET}} A$$

17.1 Current Limiting

The current limit after tripping is set by the same voltage at the CL_LVL pin as current limit trip point. The current accuracy after tripping and in constant current mode is less accurate at -35%, +10% ($\frac{\Delta I_{LOAD_CLIM}}{\Delta V_{CL_LVL}}$ in the Electrical Characteristics tables).

17.2 Setting the Current Limit Trip

Configure a hard current limit trip by applying a bias voltage at the CL_LVL according to the current limit required. The current limit is V_{CL_LVL} . Set $V_{CL_LVL} = 5V$ for a 5A trip current.

The trip current limit can be set by resistor potential divider from V_{REF} to GND at the CL_LVL pin, for trip points up to 5A. This is shown as R_A and R_B in Figure 17 below. It could also be controlled by an external DAC or digital pot to provide an adjustable limit.

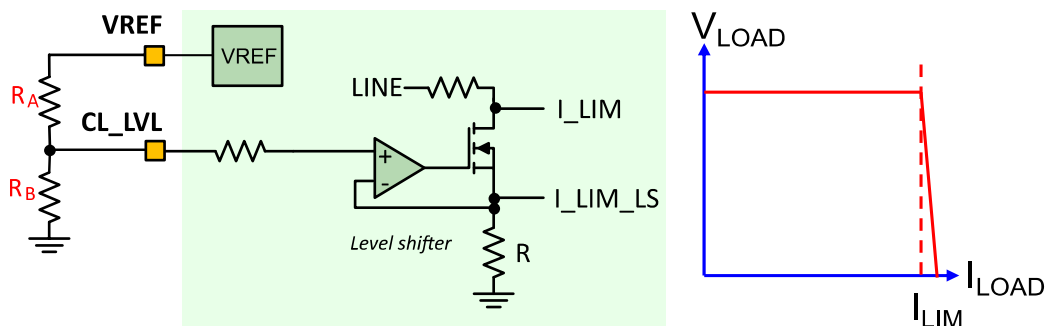


Figure 17. Current Limiting Without Foldback

When using resistors R_A and R_B as a potential divider from V_{REF} , the current trip equation is:

Equation 16. $I_{LIM} = V_{CL_LVL} = \frac{V_{REF} \times R_B}{R_A + R_B} \text{ A}$

Solving for R_A this simplifies to:

Equation 17. $R_A = R_B \times \left(\frac{V_{REF}}{I_{LIM}} - 1 \right) \Omega$

Table 3 below shows typical ideal resistor values, using $V_{REF} = 5V$.

Current Limit	R_A	R_B
5A	Tie to V_{REF}	-
4.5A	2k Ω	18k Ω
4A	4k Ω	16k Ω
3.5A	6k Ω	14k Ω
3A	8k Ω	12k Ω
2.5A	10k Ω	10k Ω
2A	12k Ω	8k Ω
1.5A	14k Ω	6k Ω
1A	16k Ω	4k Ω
0.5A	18k Ω	2k Ω

Table 3. Example Current Limit Resistor Values

The fold back current limit mode is selected by using a resistive network that drives CL_LVL based on V_{REF} and $LOAD$ voltage levels. The fold back current limit is designed to reduce the current to a safe level in the event of a load fault and provide automatic recovery when the fault is removed. The switch will dissipate power if operated with a high current in linear mode; this occurs when using the traditional feedback mode. To prevent excessive die temperature with a soft short, an over temperature detect circuit can be configured to force a latched shutdown. For a traditional current foldback configured part, the current limit is determined by the following equations. Picking a value for R_A allows R_B and R_C to be determined.

Equation 18. $I_{LIM} = \left(V_{REF} \times \frac{(R_A \parallel R_C)}{R_B + (R_A \parallel R_C)} \right) + \left(V_{LOAD} \times \frac{(R_B \parallel R_C)}{R_A + (R_B \parallel R_C)} \right) \text{ A}$

Equation 19. $I_{SC} = V_{REF} \times \frac{(R_A \parallel R_C)}{R_B + (R_A \parallel R_C)} \text{ A}$

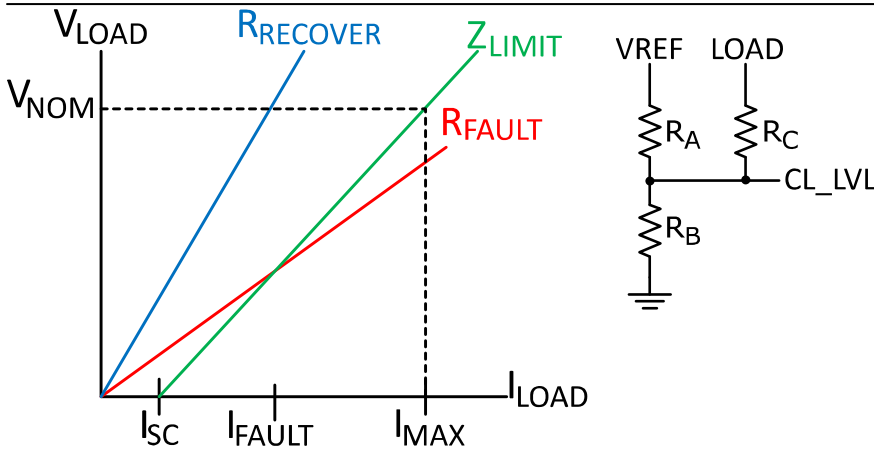


Figure 18. Current Limiting With Traditional Foldback

The bi-level fold back configuration contains a provision to prevent soft short scenarios that deter stable operation under high switch current with high switch voltage conditions. The current limit load line is purposely tilted so that a resistive over load will not settle at an intermediate level of fault current. The level of negative offset is determined by the forward voltage of the diode on the LOAD divider. The fault current is determined by the voltage applied to the CL_LVL pin (assuming that R_E is large compared to both R_B and R_D , and that the forward voltage of both diodes is V_{FD}).

Equation 20.
$$I_{LIM} = \frac{V_{LOAD} \times R_D}{R_C + R_D} - V_{FD} \text{ A}$$

Equation 21.
$$I_{FAULT} = \frac{V_{REF} \times R_B}{R_A + R_B} - V_{FD} \text{ A}$$

The current limit is the greater of I_{LIMIT} or I_{FAULT} and $I_{LIMIT} = I_{MAX}$ when $V_{LOAD} = V_{NOM}$. Automatic recovery occurs when the load is reduced to the point that $V_{LOAD} = I_{FAULT} \times R_{LOAD}$ is equal to:

Equation 22.
$$V_{LOAD} = \frac{V_{REF} \times R_B}{R_A + R_B} \times \frac{R_C + R_D}{R_D} \text{ V}$$

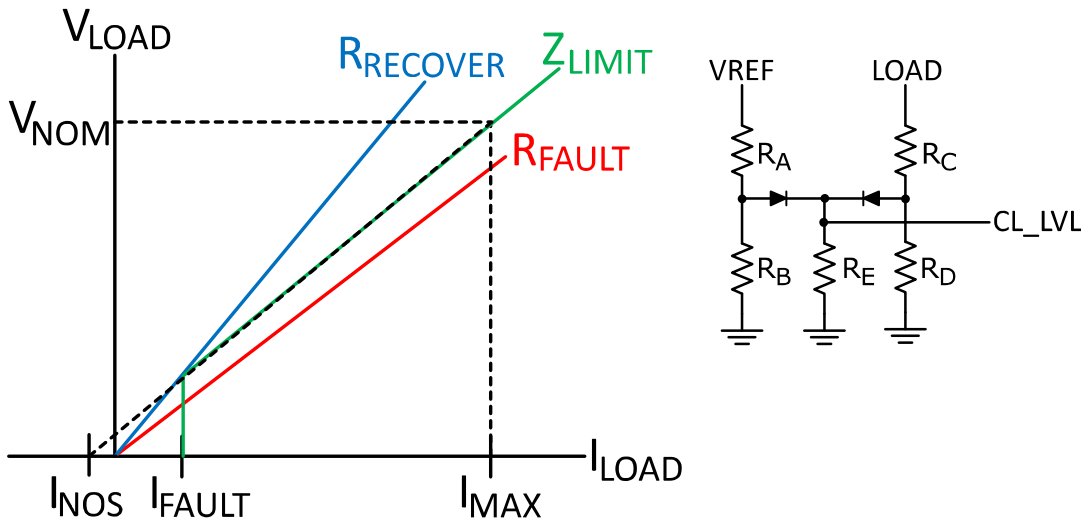


Figure 19. Current Limiting With Bi-Level Foldback

18 Parallel Operation of Multiple LX7712s

Multiple LX7712s can be paralleled for load higher than 5A by configuring one LX7712 as the control unit with instrumentation, and the other(s) to mimic the control unit's settings (Figure 6 on page 13). The control unit sets its current limit using CL_LVL in the normal way, and the mimic devices use the control unit's I_MON output to set their current limit at CL_LVL as a copy of the control unit's actual current.

Derate the 5A maximum current per mimic switch by 10% to 4.5A to account for worst-case differences between switch on-resistances and resultant current sharing and to ensure that the control LX7712 is taking the most current. This can be done with a 90% potential divider from the control unit's I_MON output. In the Figure 6 example, the 500Ω and 4.5kΩ network presents a 5kΩ load for current monitoring, and sets the mimic LX7712's current limit 10% lower than the control unit. The total load current capability is 5A for the control unit, plus 4.5A for the second device.

19 Power Switch Reverse Current Protection

The LX7712's power switch has a reverse body diode (Figure 13 on page 18) which provides a path from the LOAD output to the LINE input when the power switch is turned off. If LX7712s are used to hot-swap multiple supplies to a load, then an external reverse PFET can be added to each LX7712 to block the reverse path when the LX7712 is off.

The LX7712's CS_DRV pin is a gate driver for an optional external PFET in reverse-series with the internal PMOS from LINE to LOAD for cold sparing. The gate is driven to either LINE (in the OFF state) or to HS_SOURCE (in the ON state) via a drive output resistance of typically 10kΩ (Figure 20 below). To ensure that the external PFET is off should its gate connection to CS_DRV be open, add a high value (220kΩ for example) resistor from gate to LINE. Alternatively, to ensure that the external PFET is on should its gate connection to CS_DRV be open, connect the resistor from gate to HS_SOURCE. Do not add circuitry that would pull CS_DRV below HS_SOURCE.

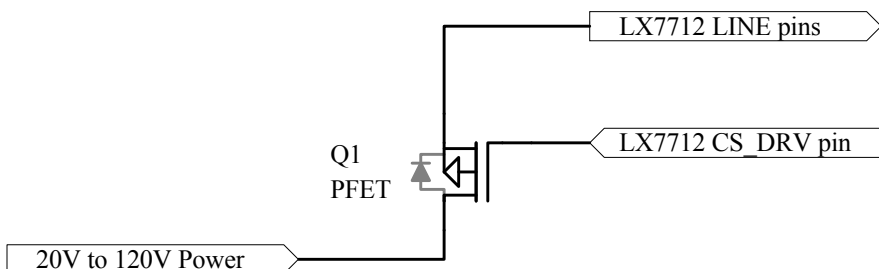


Figure 20. Adding a Back-to-Back PFET for Reverse Current Protection

20 CQFP-132 (Ceramic Quad Flat Pack) Dimensions

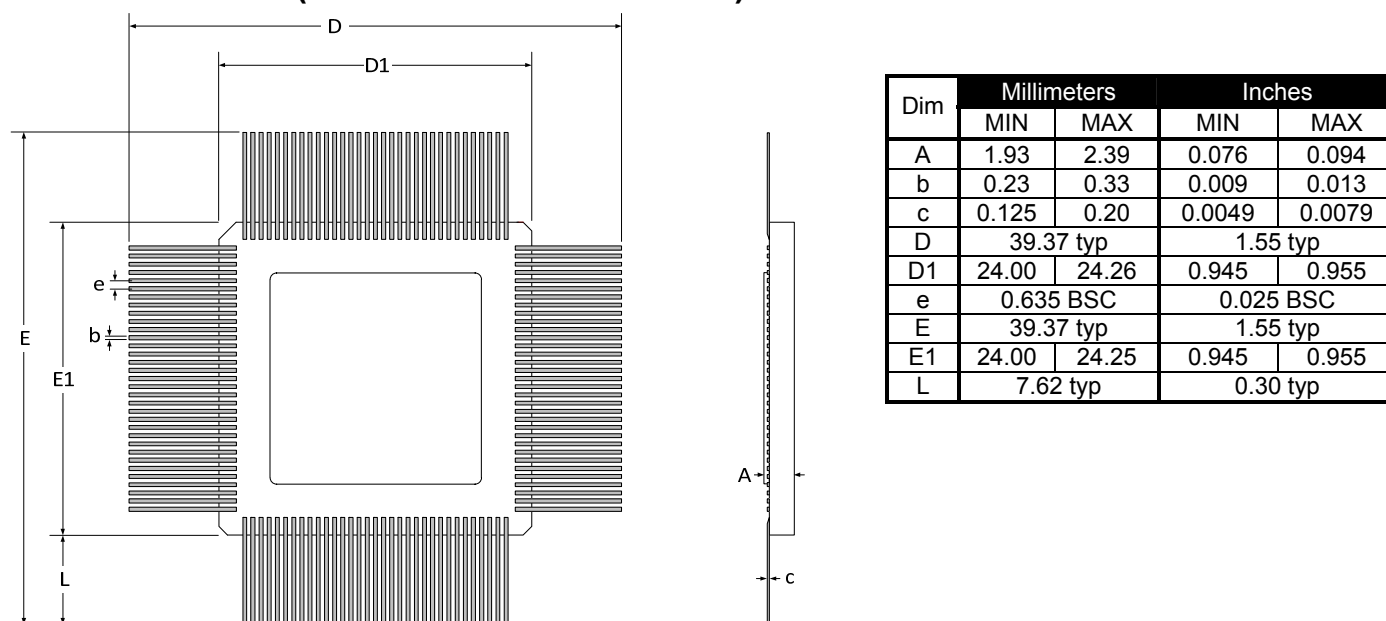


Figure 21. CQFP-132 Package Dimensions

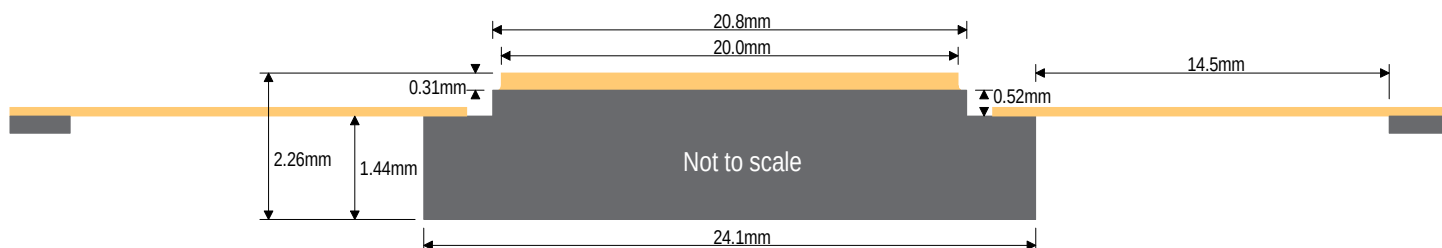


Figure 22. Package Cross-Section Nominal Dimensions as Shipped with Tie-Bars

Note:

1. Controlling dimensions are in mm. Imperial (inch) equivalents are shown for general information
2. Package includes non-conductive ceramic tie-bars mechanically connected to all pins
3. Parts are shipped with untrimmed and unformed leads
4. Package mass is 4.6g typical with 14mm leads (trimmed flush with ceramic tie-bars, tie bars discarded)
5. Lead material is Kovar with NiAu plating (nickel under-plate followed by gold plating)
6. Lid material is Kovar or Alloy 42 with NiAu plating (nickel under-plate followed by gold plating)
7. Lid is electrically isolated from the leads, and is bonded hermetically to the ceramic body using AuSn solder
8. Use the (electrically non-conductive) base of the package as the surface for conducting heat from the package

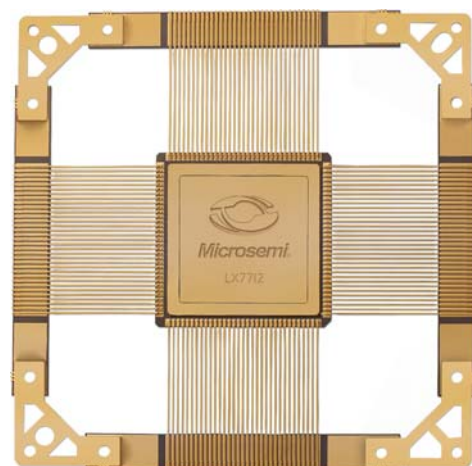


Figure 23. Package as shipped with non-conductive ceramic tie-bars, untrimmed and unformed leads

21 Revision History

21.1 Revision 0.93 - October 2023

Pre-release. Changes not logged.

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