

Introduction

General Description

Microchip's VC-709 Crystal Oscillator is a quartz stabilized, differential output oscillator, operating off a 2.5V or 3.3V supply in a hermetically sealed 7.0mm × 5.0mm ceramic package.

Features

- Ultra Low Jitter Performance, Third OT, or Fundamental Crystal Design
- 13.500MHz–220.000MHz Output Frequencies
- Low Power
- 400ps Max. Rise and Fall Time
- Excellent Power Supply Rejection Ratio
- Enable/Disable
- 2.5V or 3.3V Operation
- –10/70°C or –40/85°C Operation
- Hermetically Sealed 7.0mm × 5.0mm Ceramic Package
- Product is Compliant to RoHS Directive and Fully Compatible with Lead-free Assembly (except for the _SNPB option)

Applications

- PCI Express
- Ethernet, GbE, Synchronous Ethernet
- Fiber Channel
- Enterprise Servers
- Telecom
- Clock Source for A/D's, D/A's
- Driving FPGAs
- Test and Measurement
- PON
- Medical
- COTS

Phase Noise Plot

Figure 2. Phase Noise Plot Diagram

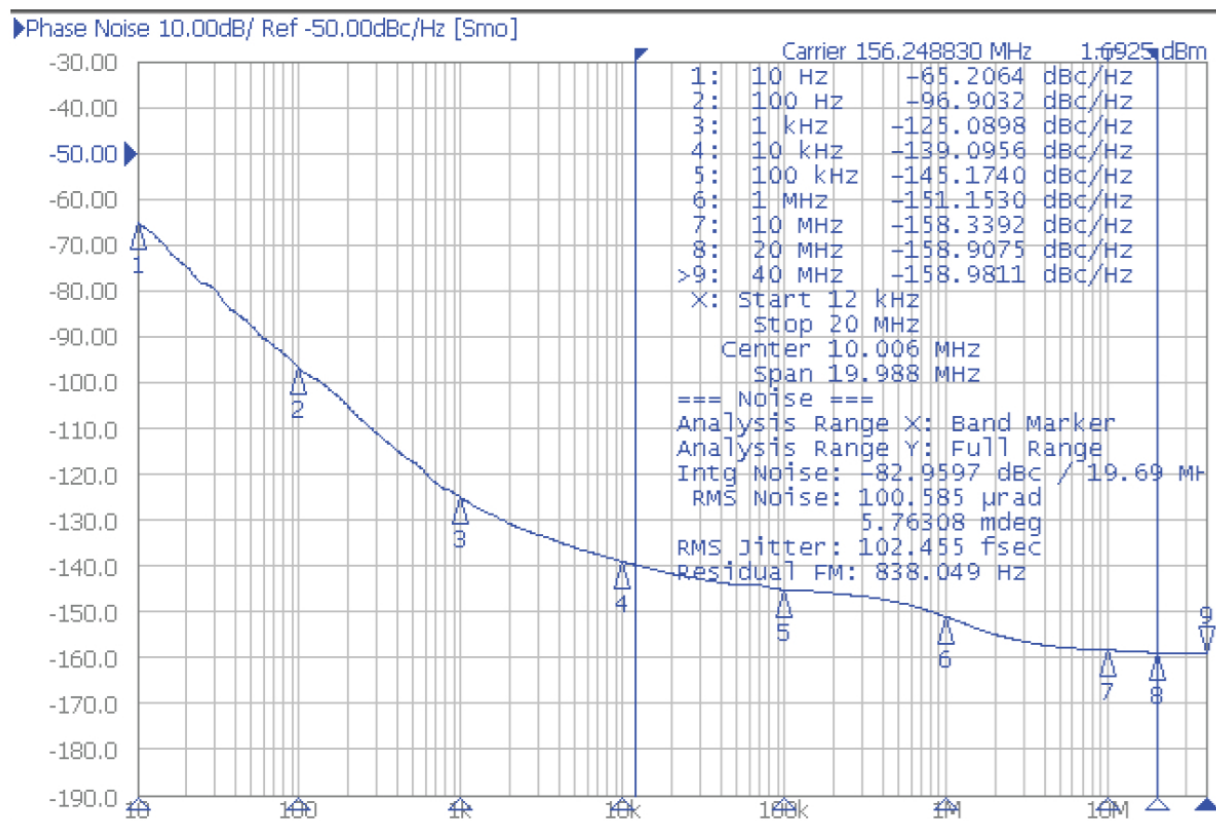


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1. Electrical Characteristics

1.1. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Table 1-1. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Storage Temperature	T_S	-50/+125	°C
Junction Temperature	T_J	150	°C
Supply Voltage	V_{DD}	-0.5/7.0	V
Enable/Disable Voltage	—	-0.5 to $V_{DD} + 0.5$	V

1.2. ESD Ratings

Although ESD protection circuitry has been designed into the VC-709, proper precautions should be taken when handling and mounting. Microchip employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5k Ω and capacitance of 100pF is widely used and therefore can be used for comparison purposes.

Table 1-2. ESD Ratings

Parameter	Rating	Units
Human Body Model	1500V	MIL-STD-883, Method 3015
Charged Device Model	1000V	JESD22-C101

1.3. Electrical Specifications

1.3.1. Electrical Performance, HCSL

Table 1-3. Electrical Performance, HCSL

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply					
Voltage (Note 1)	V_{DD}	2.375	2.5	2.625	V
		3.165	3.3	3.465	V
Current (Note 2)	I_{DD}	—	—	39	mA
Frequency					
Nominal Frequency	f_N	13.5	—	170	MHz

Notes:

1. The VC-709 power supply pin should be filtered, e.g., a 10 μ f, 0.1 μ f and 0.01 μ f capacitor.
2. [Figure 1-1](#) defines the test circuit and [Figure 1-2](#) defines these parameters.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Duty Cycle is defined as the On Time/Period.
5. Measured using an Agilent E5052.
6. Measured using a LeCroy Wavemaster 8600A, 90K samples.
7. Measured using a Wavecrest SIA3300C, 90K samples.
8. Outputs will be Enabled if the Enable/Disable pad is left open.

Table 1-3. Electrical Performance, HCSL (continued)

Parameter	Symbol	Min.	Typ.	Max.	Units
Stability (Ordering Option, Note 3)	—	±25, ±50, ±100			ppm
Outputs					
Output High, 2.5V	V _{OH}	580	—	850	mV
Output High, 3.3V	V _{OH}	600	—	850	mV
Output Low	V _{OH}	–150	—	150	mV
Output Logic Swing, 2.5V	V _{OPP}	0.60	—	—	V
Output Logic Swing, 3.3V	V _{OPP}	0.65		—	V
Output Rise and Fall Time (Note 3)	t _R /t _F	—	—	500	ps
Load	—	50Ω to ground			—
Duty Cycle (Note 4)	—	45	—	55	%
Jitter 100.000MHz (Note 5), 12kHz–20MHz	ϕ _J	—	—	300	fs
Jitter 100.000MHz (Note 6),	ϕ _J	PCIe Gen 1 – Gen 7 Compliant			—
Enable/Disable					
Outputs Enabled (Note 8)	V _{IH}	0.7 × V _{DD}	—	—	V
Outputs Disabled	V _{IL}	—	—	0.3 × V _{DD}	V
Disable Time	t _D	—	—	200	ns
Enable/Disable Leakage Current	I _{E/D}	—	—	±200	uA
Start-Up Time	t _{SU}	—	—	10	ms
Operating Temperature (Ordering Option)	T _{OP}	–10/70 or –40/85			°C

Notes:

1. The VC-709 power supply pin should be filtered, e.g., a 10 μf , 0.1 μf and 0.01 μf capacitor.
2. [Figure 1-1](#) defines the test circuit and [Figure 1-2](#) defines these parameters.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Duty Cycle is defined as the On Time/Period.
5. Measured using an Agilent E5052.
6. Measured using a LeCroy Wavemaster 8600A, 90K samples.
7. Measured using a Wavecrest SIA3300C, 90K samples.
8. Outputs will be Enabled if the Enable/Disable pad is left open.

Figure 1-1. HCSL Test Circuit

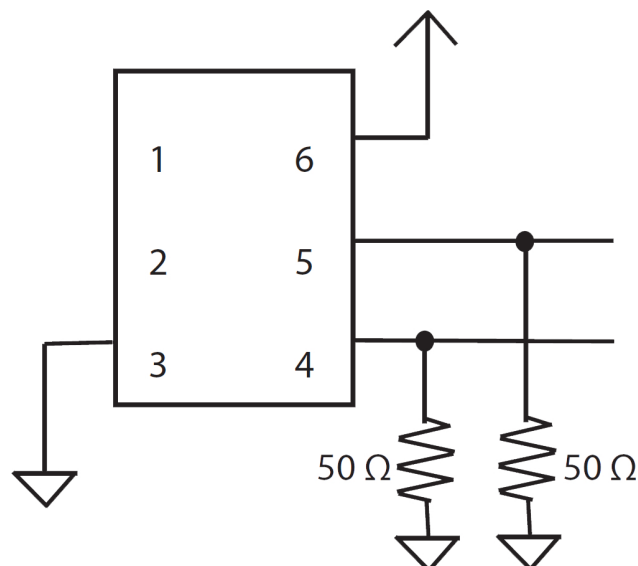
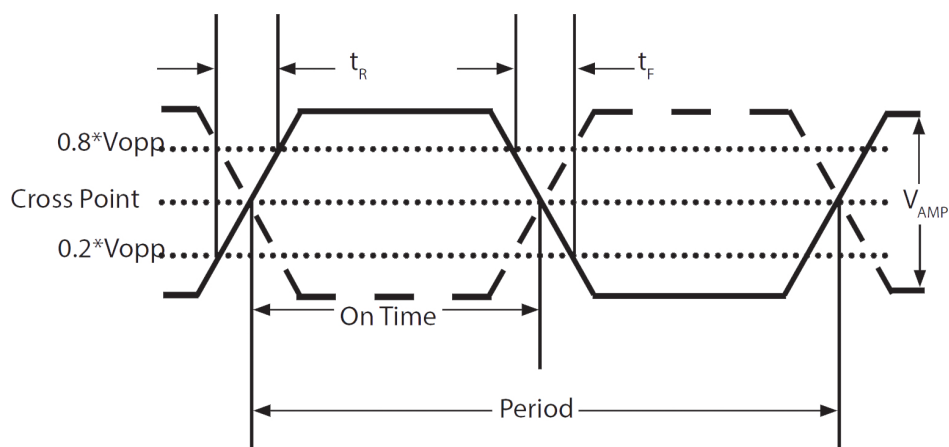


Figure 1-2. HCSL Output Parameters



1.3.2. Electrical Performance, LVDS

Table 1-4. Electrical Performance, LVDS

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply					
Voltage (Note 1)	V_{DD}	2.375	2.5	2.625	V
		3.135	3.3	3.465	V

Notes:

1. The VC-709 power supply pin should be filtered, e.g., a 10uf, 0.1uf and 0.01uf capacitor.
2. [Figure 1-4](#) defines these parameters and [Figure 1-3](#) defines the test circuit.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Duty Cycle is defined as the On/Time Period.
5. Measured using an Agilent E5052.
6. Measured using a LeCroy Wavemaster 8600A, 90K samples.
7. Measured using a Wavecrest SIA3300C, 90K samples.
8. Outputs will be Enabled if Enable/Disable is left open.

Table 1-4. Electrical Performance, LVDS (continued)

Parameter	Symbol	Min.	Typ.	Max.	Units
2.5V Current (Note 2)	I _{DD}	—	—	14	mA
3.3V Current (Note 2)	I _{DD}	—	—	17	mA
Frequency					
Nominal Frequency	f _N	13.5	—	220.0	MHz
Stability (Ordering Option, Note 2)	—	±20, ±25, ±50, ±100			ppm
Outputs					
Output Logic High (Note 2)	V _{OH}	—	1.43	1.6	V
Output Logic Low (Note 2)	V _{OL}	0.9	1.10	—	V
Output Amplitude	—	250	350	450	mV
Differential Output Error	—	—	—	50	mV
Output Leakage Current, Outputs Disabled	—	—	—	10	uA
Output Rise and Fall Time (Note 3)	t _R /t _F	—	—	400	ps
Load	—	100Ω differential			
Duty Cycle (Note 4)	—	45	—	55	%
Jitter, 156.250MHz (12kHz – 50MHz, Note 5)	ϕ _J	—	—	200	fs
Jitter, 156.250MHz (12kHz – 20MHz, Note 5)		—	—	150	fs
Jitter, 156.250MHz (10kHz – 1MHz, Note 5)		—	—	100	fs
Period Jitter, 156.250MHz (RMS, Note 6)	ϕ _J	—	1.1	2.2	ps
Period Jitter, 156.250MHz (P/P, Note 6)		—	10.5	21.0	ps
Cycle-Cycle Jitter (RMS, Note 6)		—	1.9	3.8	ps
Cycle-Cycle Jitter (P/P, Note 6)		—	17.7	35.4	ps
Random Jitter (Note 7)		—	2.2	4.4	ps
Deterministic Jitter (Note 7)		—	0	—	ps
Enable/Disable					
Outputs Enabled (Note 8)	V _{IH}	0.7 × V _{DD}	—	—	V
Output Disabled	V _{IL}	—	—	0.3 × V _{DD}	V
Disable Time	t _D	—	—	200	ns
Enable/Disable Leakage Current	I _{E/D}	—	—	±200	uA
Start-Up Time	t _{SU}	—	—	10	ms
Operating Temperature (Order Option)	T _{OP}	–10/70 or –40/85			°C

Notes:

1. The VC-709 power supply pin should be filtered, e.g., a 10uf, 0.1uf and 0.01uf capacitor.
2. [Figure 1-4](#) defines these parameters and [Figure 1-3](#) defines the test circuit.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Duty Cycle is defined as the On/Time Period.
5. Measured using an Agilent E5052.
6. Measured using a LeCroy Wavemaster 8600A, 90K samples.
7. Measured using a Wavecrest SIA3300C, 90K samples.
8. Outputs will be Enabled if Enable/Disable is left open.

Figure 1-3. LVDS Test Circuit

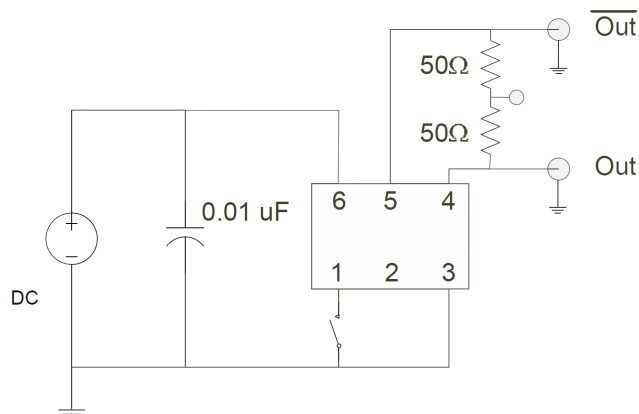
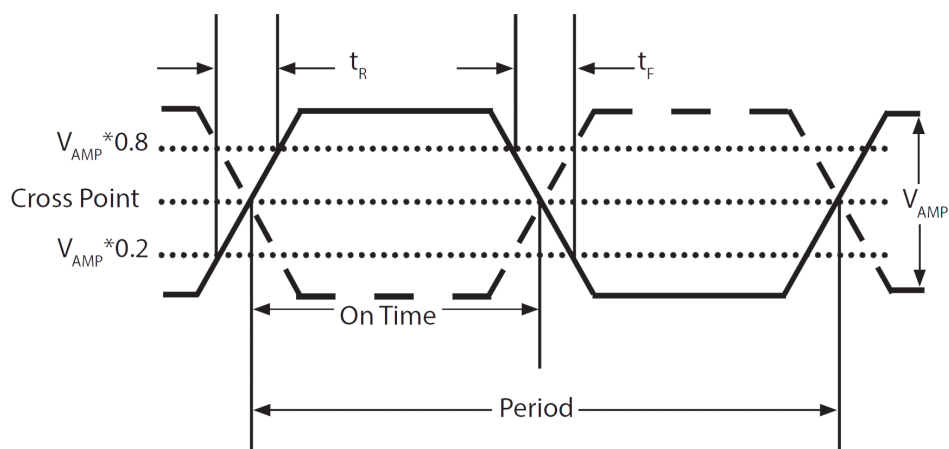


Figure 1-4. LVDS and LVPECL Output Parameters



1.3.3. Electrical Performance, LVPECL

Table 1-5. Electrical Performance, LVPECL

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply					
Voltage (Note 1)	V_{DD}	2.375	2.5	2.625	V
		3.135	3.3	3.465	V
2.5V Current (Note 2)	I_{DD}	—	—	42	mA
3.3V Current (Note 2)	I_{DD}	—	—	45	mA
Frequency					

Notes:

1. The VC-709 power supply pin should be filtered, e.g., a 10uf, 0.1uf and 0.01uf capacitor.
2. Figure 1-4 defines the test circuit and Figure 1-4 defines these parameters.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Duty Cycle is defined as the On/Time Period.
5. Measured using an Agilent E5052.
6. Measured using a LeCroy Wavemaster 8600A, 90K samples
7. Measured using a Wavecrest SIA3300C, 90K samples.
8. Outputs will be Enabled if Enable/Disable is left open.

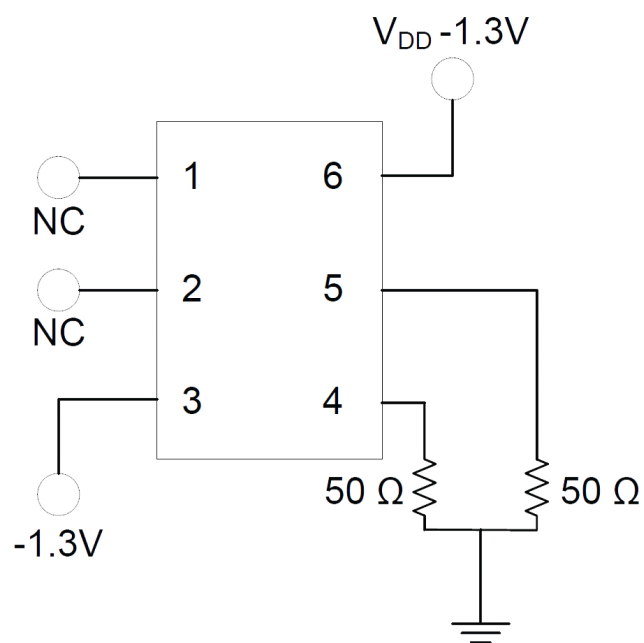
Table 1-5. Electrical Performance, LVPECL (continued)

Parameter	Symbol	Min.	Typ.	Max.	Units
2.5V Nominal Frequency	f _N	125.0	—	220.0	MHz
3.3V Nominal Frequency		13.5	—	220.0	MHz
Stability (Ordering Option, Note 3)	—	±20, ±25, ±50, ±100			ppm
Outputs					
Output Logic High (Note 2)	V _{OH}	V _{DD} – 1.025	—	V _{DD} – 0.880	V
Output Logic Low (Note 2)	V _{OL}	V _{DD} – 1.810	—	V _{DD} – 1.650	V
Output Rise and Fall Time (Note 32)	t _R /t _F	—	—	400	ps
Load	—	50Ω into V _{DD} – 2.0V			—
Duty Cycle (Note 4)	—	45	—	55	%
Jitter, 156.250MHz (12kHz – 50MHz, Note 5)	ϕ _J	—	—	200	fs
Jitter, 156.250MHz (12kHz – 20MHz, Note 5)		—	—	150	fs
Jitter, 156.250MHz (10kHz – 1MHz, Note 5)		—	—	100	fs
Period Jitter, 156.250MHz (RMS, Note 6)	ϕ _J	—	1.1	2.2	ps
Period Jitter, 156.250MHz (P/P, Note 6)		—	10.5	21.0	ps
Cycle-Cycle Jitter (RMS, Note 6)		—	1.9	3.8	ps
Cycle-Cycle Jitter (P/P, Note 6)		—	17.7	35.4	ps
Random Jitter (Note 7)		—	2.2	4.4	ps
Deterministic Jitter (Note 7)		—	0	—	ps
Enable/Disable					
Outputs Enabled (Note 8)	V _{IH}	0.7 × V _{DD}	—	—	V
Output Disabled	V _{IL}	—	—	0.3 × V _{DD}	V
Disable Time	t _D	—	—	200	ns
Enable/Disable Leakage Current	I _{E/D}	—	—	±200	uA
Start-Up Time	t _{SU}	—	—	10	ms
Operating Temperature (Order Option)	T _{OP}	–10/70 or –40/85			°C

Notes:

1. The VC-709 power supply pin should be filtered, e.g., a 10uf, 0.1uf and 0.01uf capacitor.
2. [Figure 1-4](#) defines the test circuit and [Figure 1-4](#) defines these parameters.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Duty Cycle is defined as the On/Time Period.
5. Measured using an Agilent E5052.
6. Measured using a LeCroy Wavemaster 8600A, 90K samples
7. Measured using a Wavecrest SIA3300C, 90K samples.
8. Outputs will be Enabled if Enable/Disable is left open.

Figure 1-5. LVPECL Test Circuit



1.4. Environmental Compliance

Table 1-6. Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Fine and Gross Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-202 Method 215
Moisture Sensitivity Level	MSL1
Contact Pads	Gold over Nickel (gold thickness is 0.3um–1.0um)
θ_{JC} (bottom of case)	31°C/W
Weight	167mg

2. Functional Descriptions

2.1. HCSL Application

The VC-709 incorporates a standard High Speed Current Logic, HCSL, output scheme which is a 15mA current source switched between Out and Complementary Out. Being unterminated drains, as shown in Figure 2-1, they require external 50Ω resistors to ground as shown in Figure 2-2. HCSL is a high impedance output with quick switching times, in can be advantageous to use a 10Ω to 30Ω series resistor as shown in Figure 2-3, to help reduce overshoot/ ringing.

Figure 2-1. Standard HCSL Output Configuration

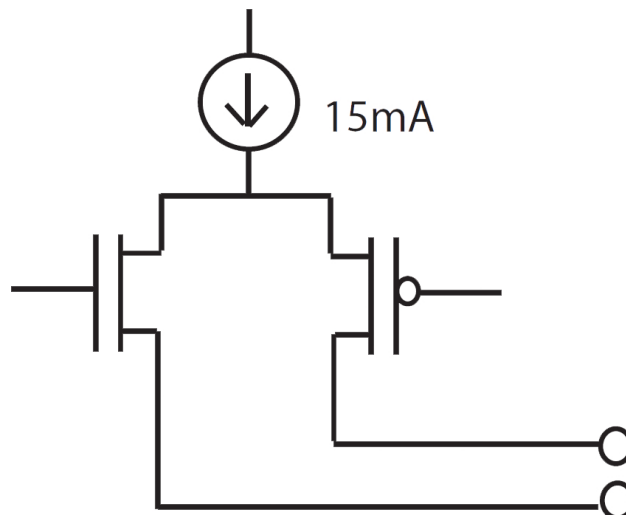


Figure 2-2. HCSL Single Resistor Termination Scheme

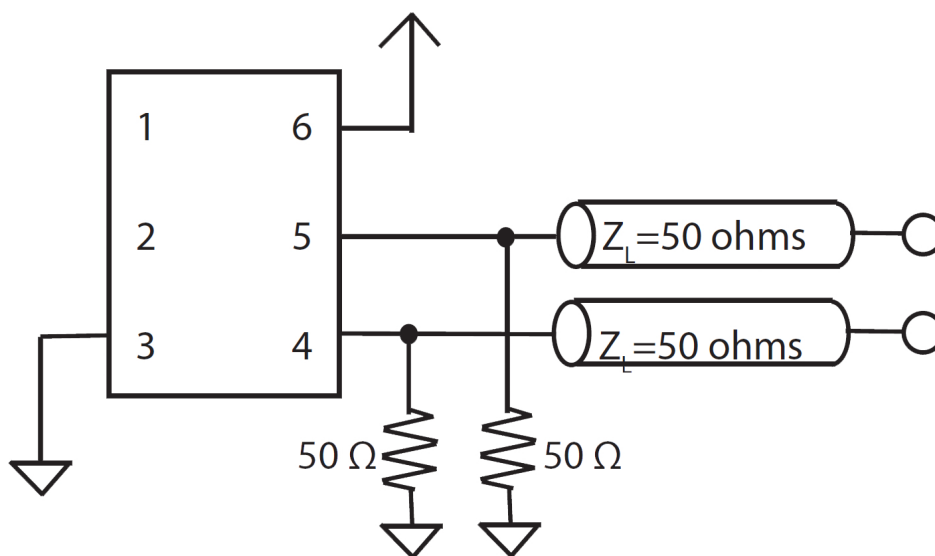
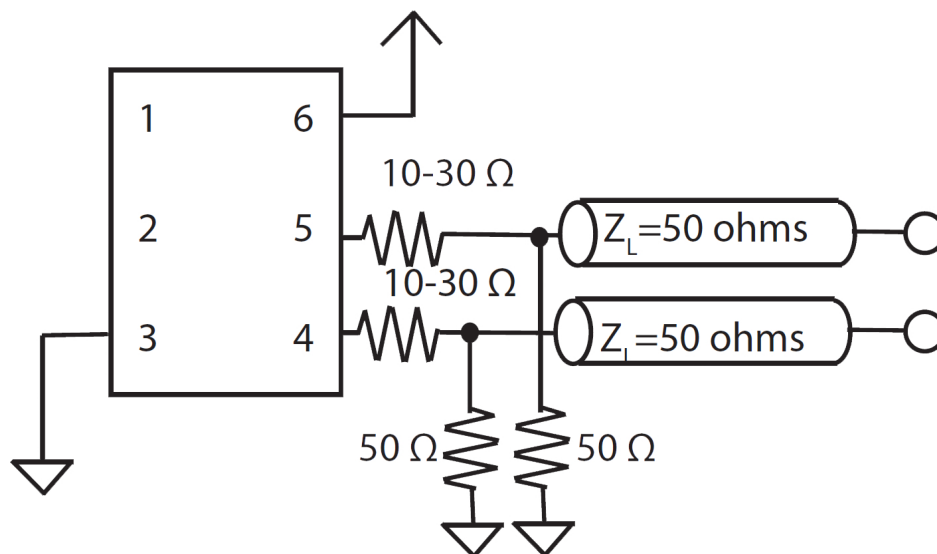


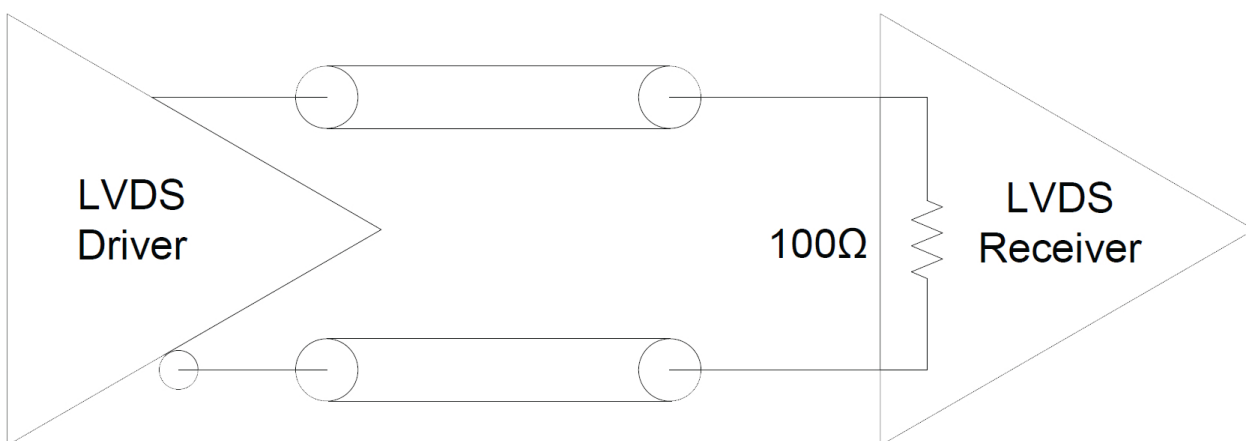
Figure 2-3. HCSL 10Ω–30Ω Series Resistor Occasionally Used to Help Reduce Overshoot

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left unterminated, and if one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50Ω impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

2.2. LVDS Application

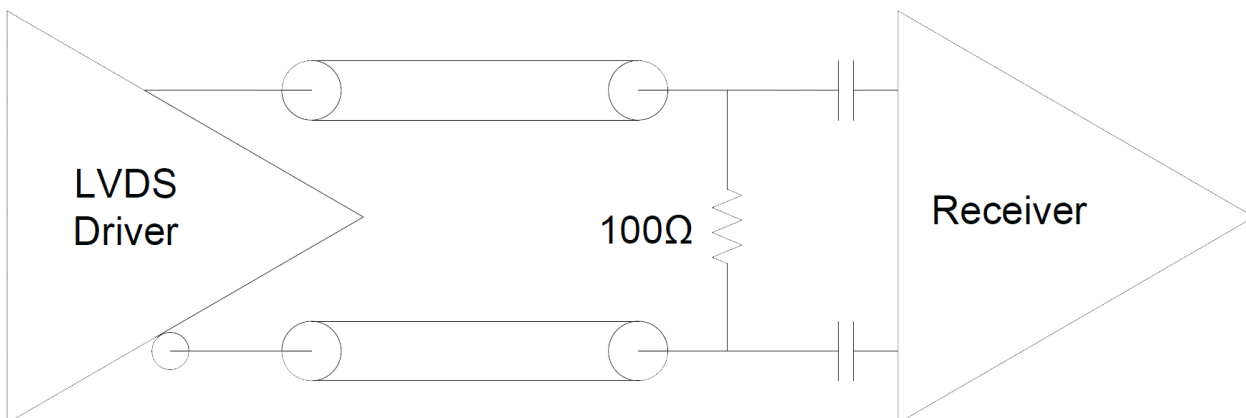
One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left unterminated, and if one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50Ω impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

As shown in [Figure 2-4](#), some LVDS structures have an internal 100Ω resistor on the input and do not need additional components. AC blocking capacitors can be used if the DC levels are incompatible.

Figure 2-4. LVDS to LVDS Connection, Internal 100Ω Resistor

As shown in [Figure 2-5](#), some input structures may not have an internal 100Ω resistor on the input and will need an external 100Ω resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

Figure 2-5. LVDS to LVDS Connection



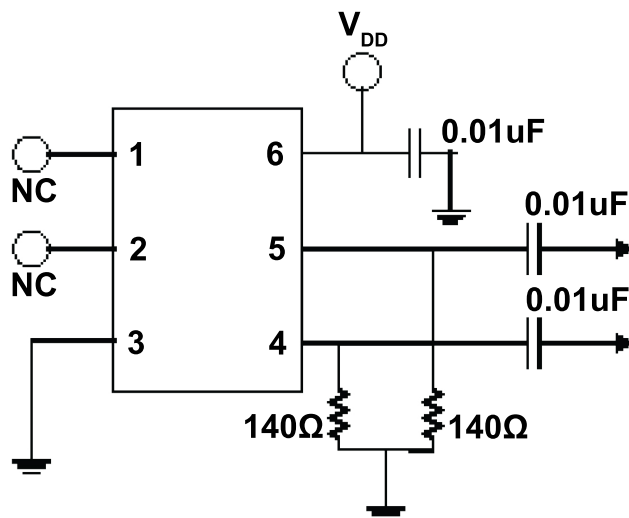
2.3. LVPECL Application

The VC-709 incorporates a standard PECL output scheme, which are unterminated FET drains. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, [Figure 2-6](#), or for best 50Ω matching a pull-up/pull-down scheme as shown in [Figure 2-7](#) should be used. AC coupling capacitors are optional, depending on the application and the input logic requirements of the next stage.

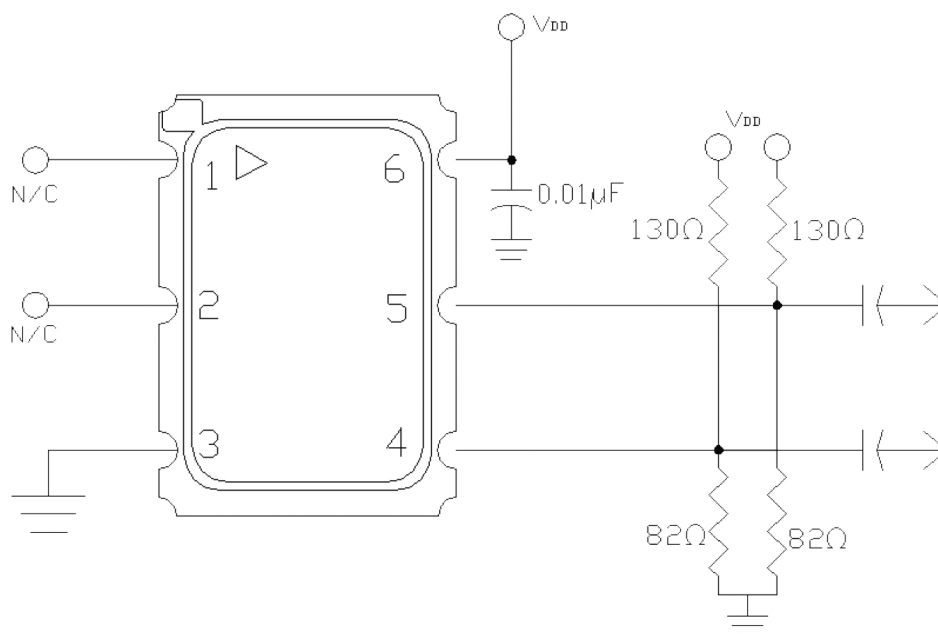
One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left unterminated, and if one of the two outputs is left open it will result in excessive jitter on both. PCB board layout must take this and 50Ω impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

As shown in the figure below, resistor values are typically 140Ω for 3.3V operation and 84Ω for 2.5V operation.

Figure 2-6. LVPECL Single Resistor Termination Scheme



As shown in the figure below, resistor values shown are typical for 3.3V operation. For 2.5V operation, the resistor to ground is 62Ω and the resistor to supply is 250Ω.

Figure 2-7. LVPECL Pull-Up Pull Down Termination

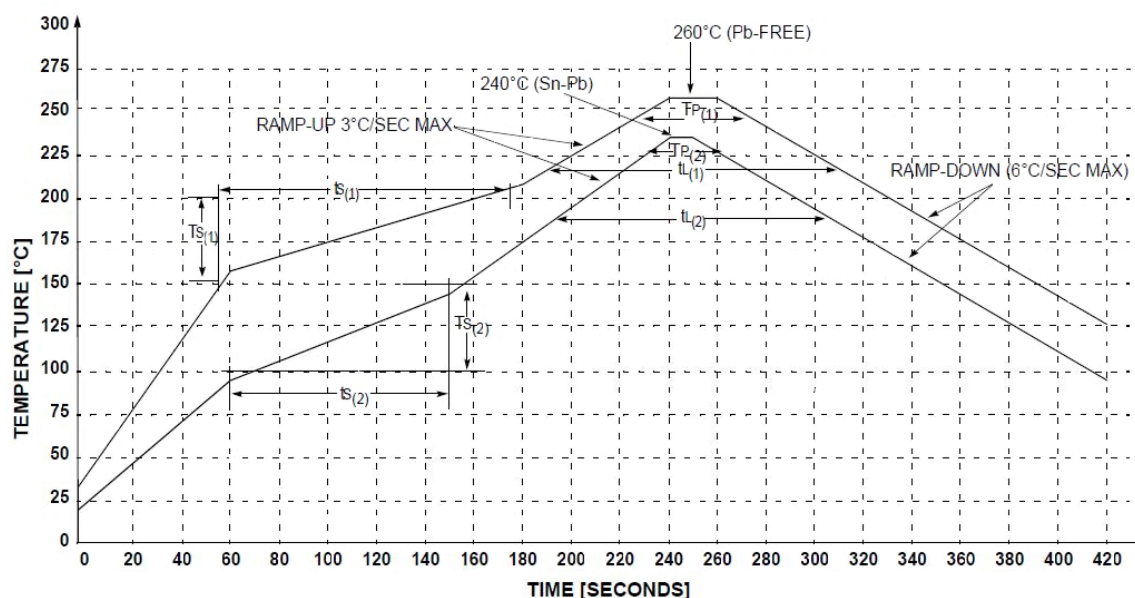
3. IR Reflow

Suggested IR Profile: Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 7. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220°C.

Table 3-1. Reflow Profile

Parameter Symbol	Minimum	Maximum	Conditions
$T_{S(1)}$	150°C	200°C	Pb-free
$T_{S(2)}$	100°C	150°C	_SNPB Option
$t_{S(1)}$	60 sec.	180 sec.	Pb-free
$t_{S(2)}$	60 sec.	120 sec.	_SNPB Option
$t_{L(1)}$	60 sec.	150 sec.	Pb-free
$t_{L(2)}$	60 sec.	150 sec.	_SNPB Option
$t_{P(1)}$	245°C	260°C	Pb-free
$t_{P(2)}$	225°C	240°C	_SNPB Option

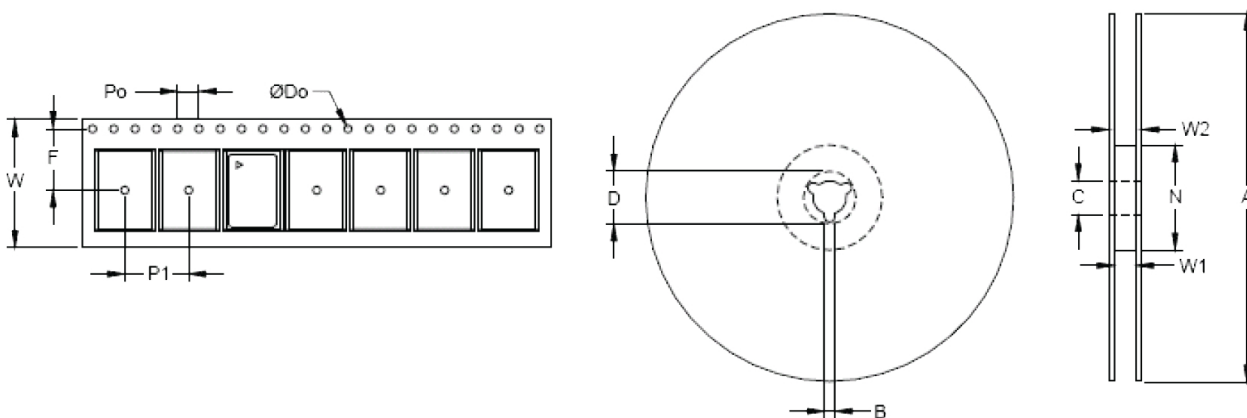
Figure 3-1. Solder Reflow



4. Tape and Reel

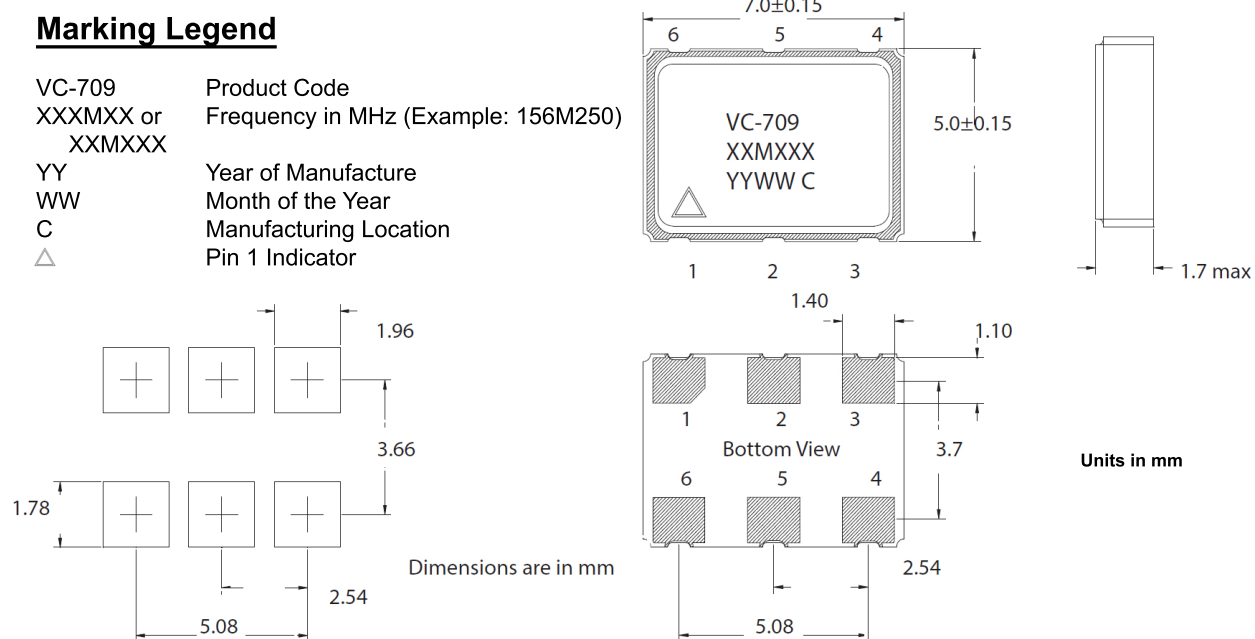
Table 4-1. Tape and Reel Information

Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
16	7.5	1.5	4	8	180	2	13	21	50	17	21	1000

Figure 4-1. Tape and Reel Diagram

5. Packaging Information

Figure 5-1. VC-709 Package Outline, Pad Layout, and Marking Drawings



6. Product Identification System

6.1. Standard Product Identification

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Table 6-1. Product Number Format

XX	-XXX	-X	X	X	-X	X	X	X	-xxxMxxxxxx	XX
Product Family	Package Size	Supply Voltage	Output	Operating Temperature	Stability Options	Enable/Disable Logic	Enable/Disable Pin	Other (Future Use)	Frequency	Packing Type

Table 6-2. Product Number Legend

Product Family:	VC	Crystal Oscillator
Package Size:	-709	6-Lead 5.0mm × 7.0mm LDFN
Supply Voltage:	-E	+3.3Vdc, ±5%
	-H	+2.5Vdc, ±5%
Output:	C	LVPECL
	D	LVDS
	H	HCSL
Operating Temperature:	W	-10/70°C
	E	-40/85°C
Stability Options:	-S	±100ppm
	-K	±50ppm
	-F	±25ppm
Enable/Disable Logic:	A	Output is Enabled with a Logic High or open, Output is Disabled with a Logic Low
Enable/Disable Pin:	A	Pin 1 (Pin 2 = No Connection)
	B	Pin 2 (Pin 1 = No Connection)
Other (Future Use):	N	Standard
Frequency:	-xxxMxxxxxx	MHz value {example: 156M250000 = 156.250000MHz}
Packing Type:	TR	Tape and Reel (Base Qty = 1000)
	<blank>	Nonstandard Tape and Reel (Base Qty = 1)
	_SNPB	Tin Lead Solder Dipped (Base Qty = 50)

Table 6-3. Examples:

a) VC-709-ECW-KAAN-125M000000
Crystal Oscillator (XO); 6-Lead 5.0mm × 7.0mm LDFN; +3.3Vdc, ±5% Supply Voltage; LVPECL Output; -10/70°C Operating Temperature; ±50ppm Stability Option; Output is Enabled with a Logic High or open, Output is Disabled with a Logic Low; Enable/Disable Pin 1 (Pin 2 = No Connection); Standard; 125.000000MHz Frequency; Nonstandard Tape and Reel (Base Qty = 1)
b) VC-709-EDE-FAAN-148M500000TR
Crystal Oscillator (XO); 6-Lead 5.0mm × 7.0mm LDFN; +3.3Vdc, ±5% Supply Voltage; LVDS Output; -40/85°C Operating Temperature; ±25ppm Stability Option; Output is Enabled with a Logic High or open, Output is Disabled with a Logic Low; Enable/Disable Pin 1 (Pin 2 = No Connection); Standard; 148.500000MHz Frequency; Tape and Reel (Base Qty = 1000)
c) VC-709-HDE-FAAN-156M250000_SNPB
Crystal Oscillator (XO); 6-Lead 5.0mm × 7.0mm LDFN; +3.3Vdc, ±5% Supply Voltage; HCSL Output; -40/85°C Operating Temperature; ±25ppm Stability Option; Output is Enabled with a Logic High or open, Output is Disabled with a Logic Low; Enable/Disable Pin 1 (Pin 2 = No Connection); Standard; 156.250000MHz Frequency; Tin Lead Solder Dipped (Base Qty = 50)

Note: Not all combination of options are available. Other specifications may be available upon request.

6.1.1. Ordering Options

Table 6-4. ± 20 ppm Options

VC-709-107-frequency= LVPECL, +3.3V, ± 20 ppm over -10/70°C, E/D on Pin1
VC-709-109-frequency= LVDS, +3.3V, ± 20 ppm over -10/70°C, E/D on Pin1
VC-709-110-frequency= LVPECL, +2.5V, ± 20 ppm over -10/70°C, E/D on Pin1
VC-709-111-frequency= LVDS, +2.5V, ± 20 ppm over -10/70°C, E/D on Pin1
VC-709-119-frequency= LVPECL, +3.3V, ± 20 ppm over -40/85°C, E/D on Pin1
VC-709-120-frequency= LVPECL, +2.5V, ± 20 ppm over -40/85°C, E/D on Pin1
VC-709-121-frequency= LVDS, +3.3V, ± 20 ppm over -40/85°C, E/D on Pin1
VC-709-122-frequency= LVDS, +2.5V, ± 20 ppm over -40/85°C, E/D on Pin1

6.2. PCI Express Product Identification

The VC-709 product options below are compliant with PCIe Generation 1-5 specifications. To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Table 6-5. Product Number Format

XX	-XXX	-X	X	X	-X	X	X	X	-xxxMxxxxxx	XX
Product Family	Package Size	Supply Voltage	Output	Operating Temperature	Stability Options	Enable/Disable Logic	Enable/Disable Pin	Other (Future Use)	Frequency	Packing Type

Table 6-6. Product Number Legend

Product Family:	VC	Crystal Oscillator
Package Size:	-709	6-Lead 5.0mm × 7.0mm LDFN
Supply Voltage:	-E	+3.3Vdc, ±5%
	-H	+2.5Vdc, ±5%
Output:	H	HCSL
Operating Temperature:	E	-40/85°C
Stability Options:	-K	±50ppm
Enable/Disable Logic:	A	Output is Enabled with a Logic High or open, Output is Disabled with a Logic Low
Enable/Disable Pin:	A	Pin 1 (Pin 2 = No Connection)
Other (Future Use):	N	Standard
Frequency:	-xxxMxxxxxx	MHz value {example: 100M000000 = 100.000000MHz}
Packing Type:	TR	Tape and Reel (Base Qty = 1000)
	<blank>	Nonstandard Tape and Reel (Base Qty = 1)
	_SNPB	Tin Lead Solder Dipped (Base Qty = 50)

Table 6-7. Examples:

a) VC-709-HHE-KAAN-156M250000
Crystal Oscillator (XO); 6-Lead 5.0mm × 7.0mm LDFN; +2.5Vdc, ±5% Supply Voltage; HCSL Output; -40/85°C Operating Temperature; ±50ppm Stability Option; Output is Enabled with a Logic High or open, Output is Disabled with a Logic Low; Enable/Disable Pin 1 (Pin 2 = No Connection); Standard; 156.250000MHz Frequency; Nonstandard Tape and Reel (Base Qty = 1)
b) VC-709-HHE-KAAN-156M250000TR
Crystal Oscillator (XO); 6-Lead 5.0mm × 7.0mm LDFN; +2.5Vdc, ±5% Supply Voltage; HCSL Output; -40/85°C Operating Temperature; ±50ppm Stability Option; Output is Enabled with a Logic High or open, Output is Disabled with a Logic Low; Enable/Disable Pin 1 (Pin 2 = No Connection); Standard; 156.250000MHz Frequency; Tape and Reel (Base Qty = 1000)
c) VC-709-HHE-KAAN-156M250000_SNPB
Crystal Oscillator (XO); 6-Lead 5.0mm × 7.0mm LDFN; +2.5Vdc, ±5% Supply Voltage; HCSL Output; -40/85°C Operating Temperature; ±50ppm Stability Option; Output is Enabled with a Logic High or open, Output is Disabled with a Logic Low; Enable/Disable Pin 1 (Pin 2 = No Connection); Standard; 156.250000MHz Frequency; Tin Lead Solder Dipped (Base Qty = 50)

Note: Not all combination of options are available. Other specifications may be available upon request.

7. Revision History

The revision history describes the changes that were implemented in the document.

Revision	Date	Section	Description
DS20007142A	06/2026	—	Initial release of this document.

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