

32-38GHz 12W GaN PA MMIC

ICP3540



Product Overview

Microchip’s ICP3540 is a four stage MMIC power amplifier in bare die form, fabricated using GaN on SiC technology. The PA operates from 32-38GHz with 41dBm output power, greater than 20% PAE and 25dB small signal gain. The die has integrated DC blocking capacitors and is matched to 50ohms on the RF input and output ports. ICP3540 is well suited to a variety of commercial and defense applications.

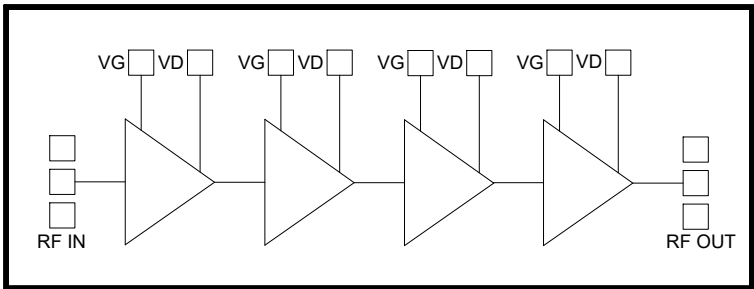
Key Features

- **Frequency Range:** 32-38GHz
- **P_{out}:** 41dBm @P_{in}=16dBm
- **PAE:** 20% @P_{in}=16dBm
- **Small Signal Gain:** 25dB
- **Bias:** V_D=28V, I_{DQ}=180mA
- **Technology:** GaN on SiC
- **Lead-free and RoHS compliant**
- **Die Dimensions:** 3.55mm x 2.80mm
- **Unconditionally Stable**

Applications

- Test and Measurement
- Communications
- Aerospace & Defense

Functional Block Diagram



Electrical Specifications

Parameter	Min.	Typ.	Max.	Units	Conditions ⁽¹⁾
Frequency	32		38	GHz	
Output Power		41		dBm	P _{in} = 16dBm
Power Added Efficiency, PAE		20		%	P _{in} = 16dBm
Small Signal Gain, S ₂₁		25		dB	
Input Return Loss		8		dB	
Output Return Loss		5		dB	

(1) Test Conditions unless otherwise stated: V_D=28V, I_{DQ}=180mA, T_A=25°C, Pulsed 10% (100µs/1ms)

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1. Electrical Specification

1.1. Absolute Maximum Ratings

Parameter	Absolute Maximum
Drain Voltage (V_D)	30V
Drain - Source Breakdown Voltage (V_{DSBKD})	120V
Drain Current (I_D)	2.3A
Power dissipation (CW) $T_A = 25^\circ\text{C}$	55.5W
Power dissipation (CW) $T_A = 85^\circ\text{C}$	42.2W
Gate Voltage (V_G)	-8 to 1.5V
CW Input Power 50 ohm, $T_A = 25^\circ\text{C}$	+24dBm
Channel Temperature	275°C
Storage Temperature	-65°C to +150°C
Eutectic Die Attach Temperature (30s)	320°C
Thermal Resistance (R_{TH})	TBC

Note:

Exceeding any one or combination of these limits may cause permanent damage to this device.

Microchip Technology Inc. does not recommend sustained operation near these survivability limits.

1.2. Small Signal Performance

Typical Data over T_A

Test conditions: $V_D=28V$, $I_{DQ}=180mA$

Figure 1-1. S_{21} vs Freq

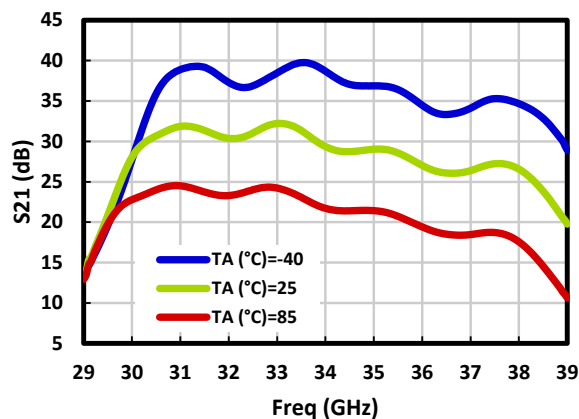


Figure 1-2. S_{11} vs Freq

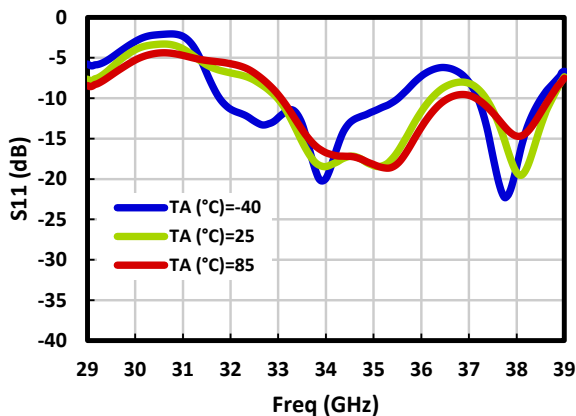
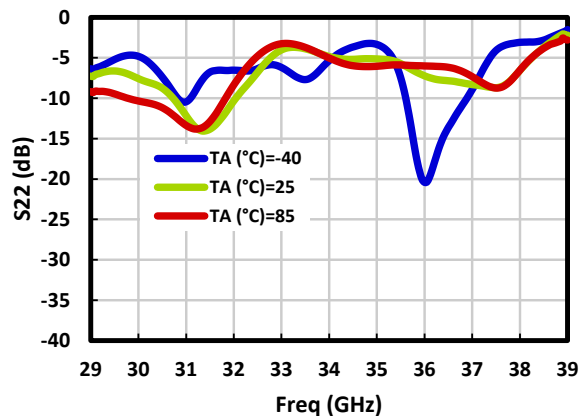


Figure 1-3. S_{22} vs Freq



Large Signal Performance

Typical Pulsed Power Data

Test conditions: $V_D=28V$, $I_{DQ}=180mA$, $T_A=25^\circ C$, Pulsed 10% (100 μs /1ms)

Figure 1-4. Pout vs. Pin

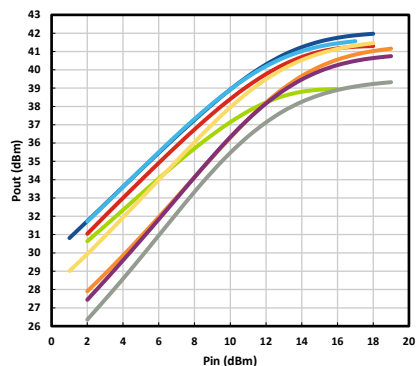


Figure 1-5. Gain vs. Pout

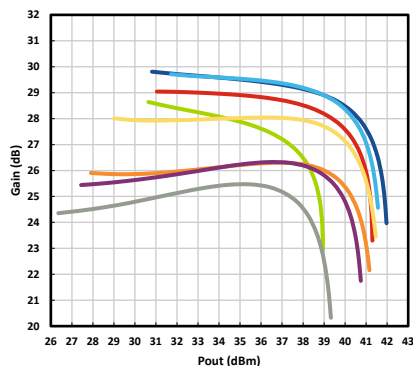


Figure 1-6. PAE vs. Pout

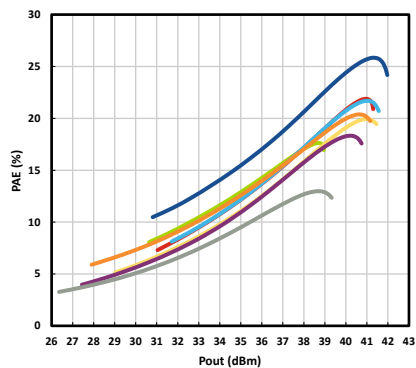


Figure 1-7. ID vs. Pout

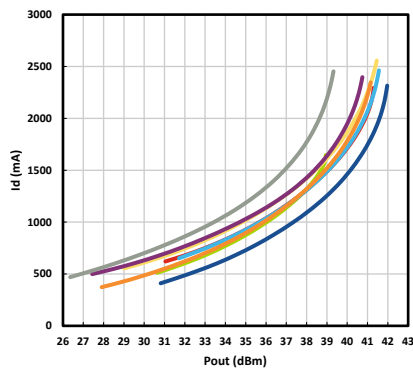


Figure 1-8. Pout vs. Freq.

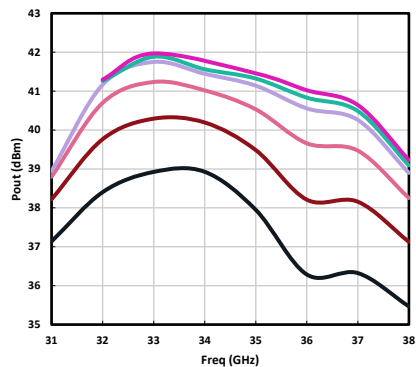
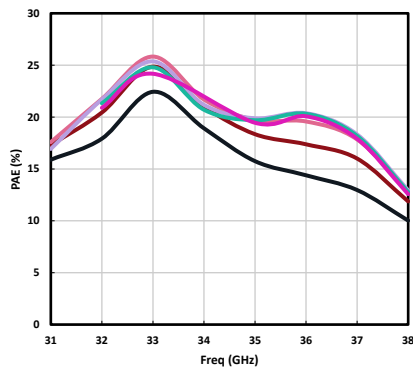


Figure 1-9. PAE vs. Freq.



Typical Pulsed Power Data over T_A

Test conditions: $V_D=28V$, $I_{DQ}=180mA$, Pulsed 10% (100 μs /1ms)

Figure 1-10. Pout vs. Pin @ 32GHz

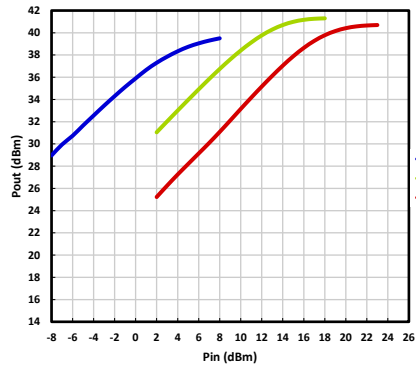


Figure 1-11. PAE vs. Pout, 32GHz

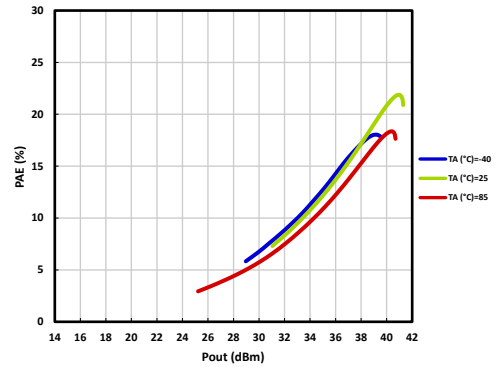


Figure 1-12. Pout vs. Pin @ 35GHz

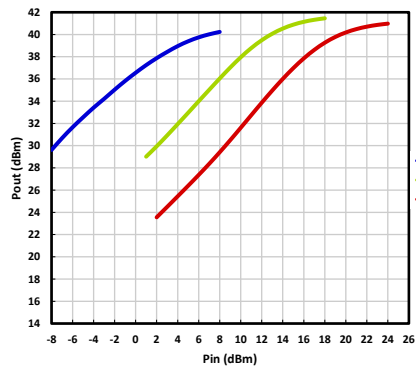


Figure 1-13. PAE vs. Pout @ 35GHz

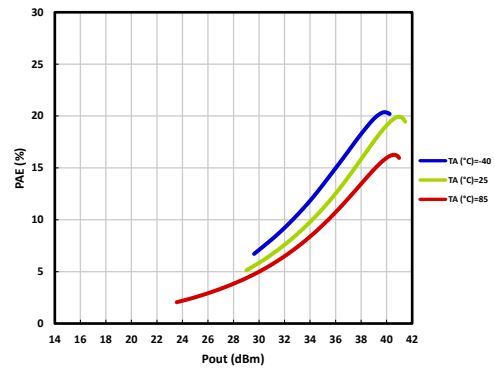


Figure 1-14. Pout vs. Pin @ 38GHz

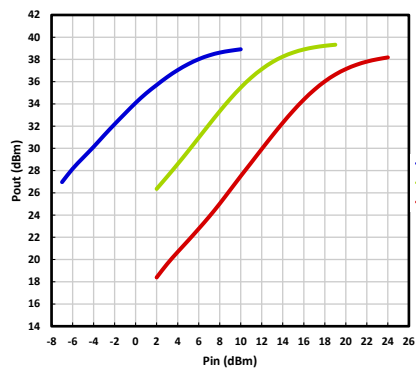
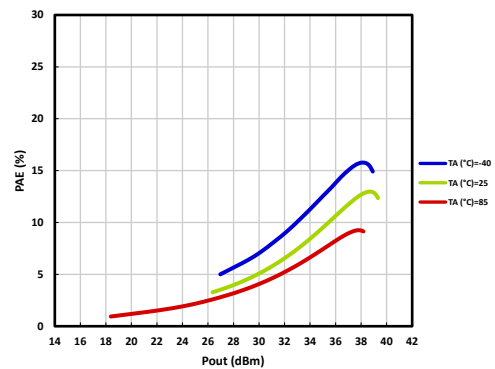
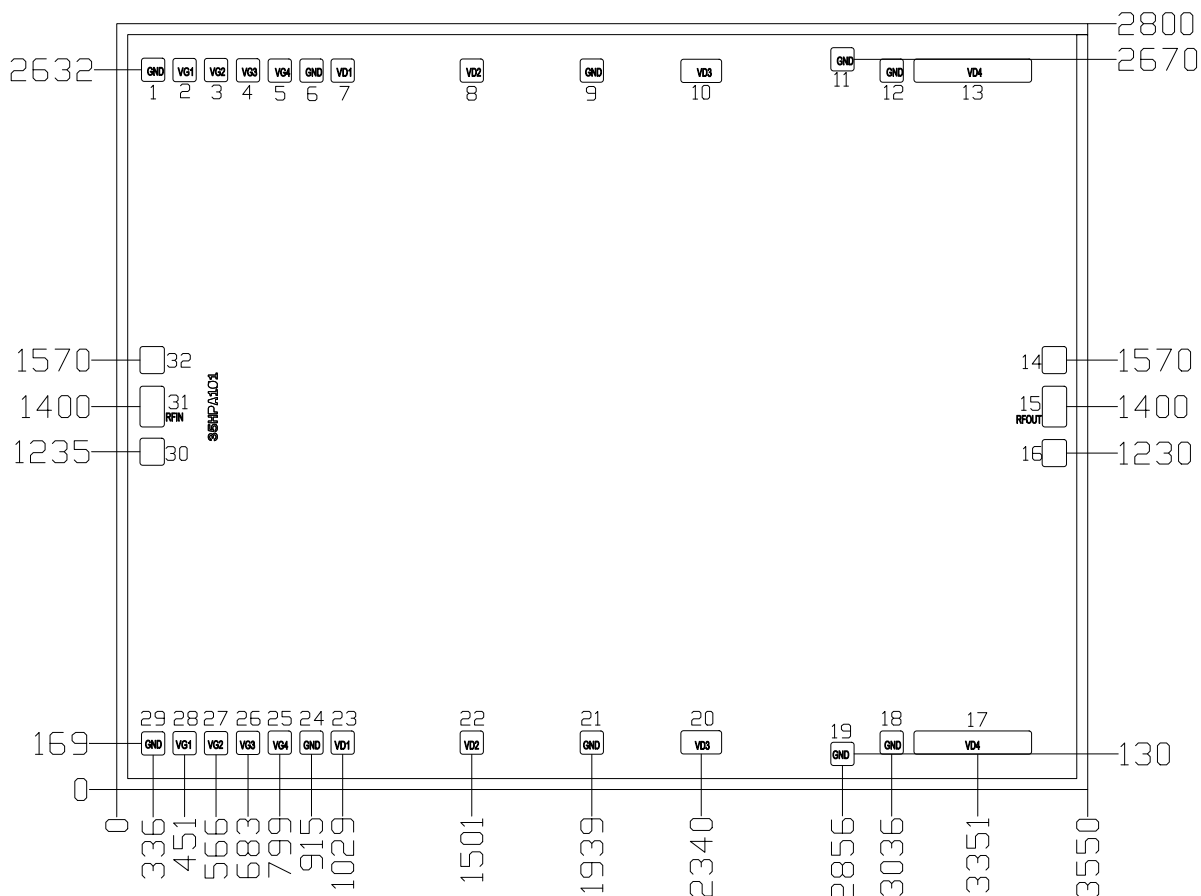


Figure 1-15. PAE vs. Pout @ 38GHz



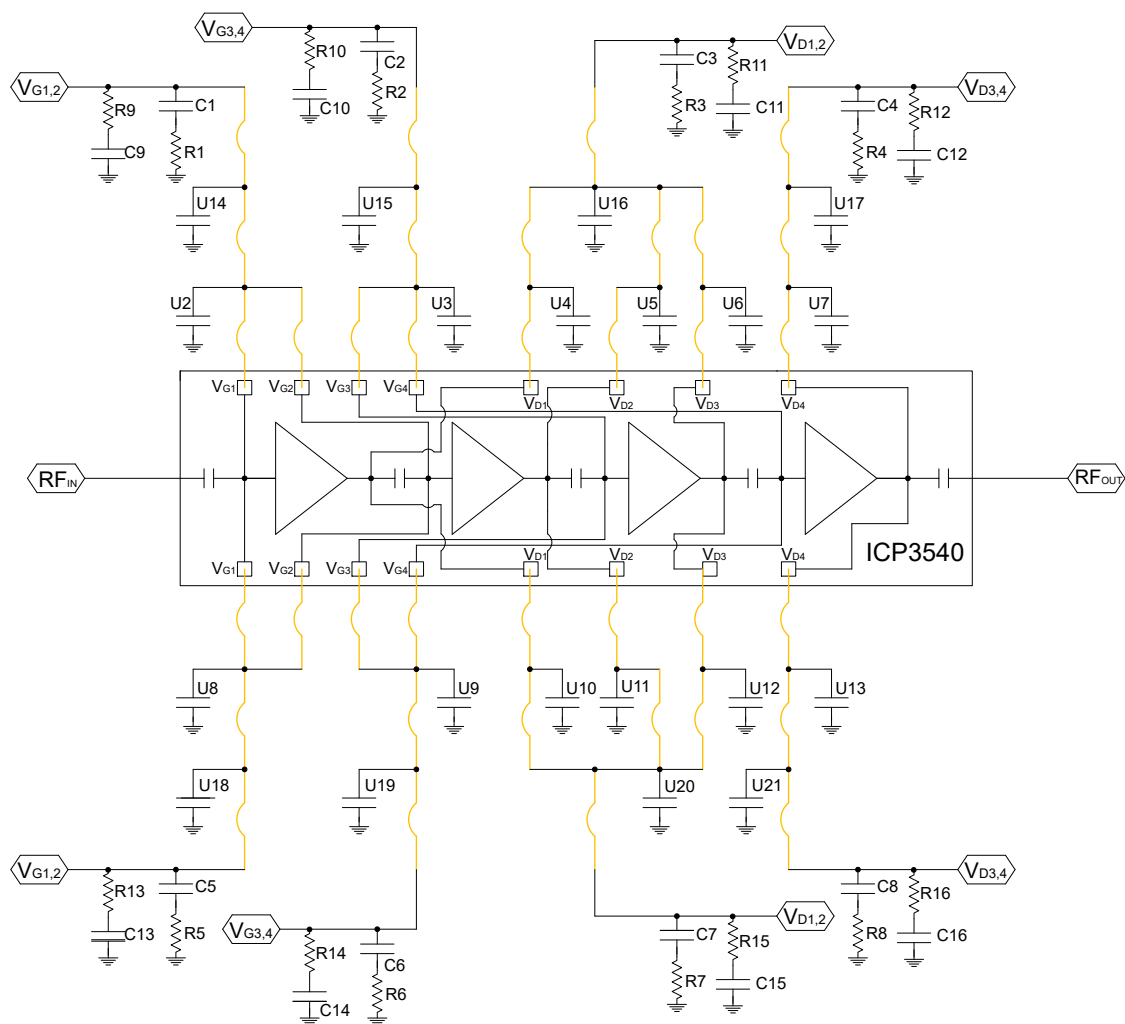
2. Mechanical Drawing



Units: μm | Thickness: 50 μm | Backside of Die is RF and DC ground

Pad No	Pad Size (μm)	Function	Description
1, 6, 9, 11, 12, 18, 19, 21, 24, 29	85x85	GND	Ground Pads
2, 28	85x85	V _{G1}	First stage gate voltage, decoupling and bypass caps required
3, 27	85x85	V _{G2}	Second stage gate voltage, decoupling and bypass caps required
4, 26	85x85	V _{G3}	Third stage gate voltage, decoupling and bypass caps required
5, 25	85x85	V _{G4}	Fourth stage gate voltage, decoupling and bypass caps required
7, 23	85x85	V _{D1}	First stage drain voltage, decoupling and bypass caps required
8, 22	85x85	V _{D2}	Second stage drain voltage, decoupling and bypass caps required
10, 20	150x85	V _{D3}	Third stage drain voltage, decoupling and bypass caps required
13, 17	430x85	V _{D4}	Fourth stage drain voltage, decoupling and bypass caps required
14, 16, 30, 32	90x100	GND	Ground Pads
15	90x150	RF _{OUT}	50ohm RF output, DC blocked
31	90x150	RF _{IN}	50ohm RF input, DC blocked

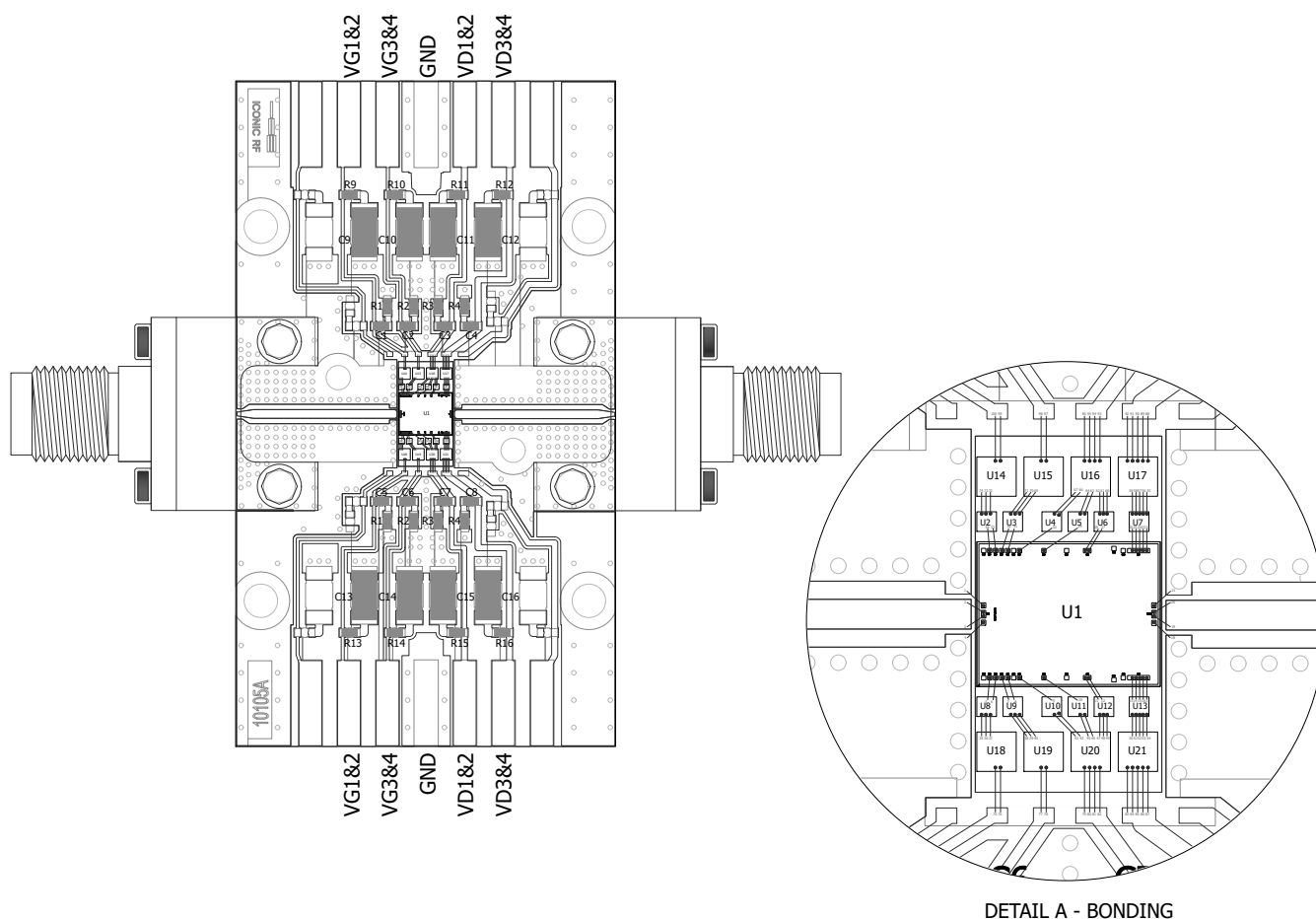
3. Application Circuit



Bill of materials

Component ID	Value	Details	Qty	Manufacturer Part No.
U2-U13	100pF	Johanson 100pF SLC	12	500U01A101MT4W
U14-U21	10nF	10nF SLC	8	V30BZ682M1SX
C1-C8	10nF	10nF Capacitor, 10%, 50V, 0402	8	Various
C9-C16	10μF	10μF Capacitor, 10%, 50V, 1206	8	Various
R1-R16	0Ω	0 Ohms Resistor, 0402	16	Various

4. Evaluation Board



DETAIL A - BONDING

PCB Construction	Material	Dimensions
METAL_1_TOP	Cu + ENIG	1oz Copper plated Electroless Nickel 3-5µm Immersion Gold 0.5µm
DIELECTRIC	RO6002	10mils (254µm)
METAL2_BOTTOM	Cu + ENIG	1oz Copper plated Electroless Nickel 3-5µm Immersion Gold 0.5µm

Key Features	Dimensions
VIA Drill	0.3mm
VIA Plating Thickness	50-70µm
50Ohm LINE WIDTH	525µm

5. Other considerations

Assembly Guidance

Interconnect Assembly Notes	Die Attach using Eutectic
- Ball bonding is preferred technique. - Force, time, and ultrasonic parameters are critical. - Aluminum wire bonding is not recommended. - Bond wire diameter of 1mil is recommended.	- Flux-less gold-tin (AuSn) (80% Au, 20% Sn with a melting point of 280 °C) preform is preferred between the die and attached surface. - Recommended preform should be approximately 0.0012" thick. - Die bonder using heated collet with a temperature of 310 °C and die scrubbing should be used to ensure wetting and prevent formation of voids. - Exposure to extreme temperature should be kept to a minimum. - The optimum die attach environment is nitrogen atmosphere.
Die Attach of Component using Adhesive	Re-flow Process
- Vacuum collets are preferred method of pickup. - Pickup method must consider the avoidance of die air bridges. - Die suitable for eutectic and epoxy die attach. - Where epoxy is used, high thermal conductivity Silver Sintered Epoxy is recommended. - Kyocera CT2700R7S - Namics H9889-1	- Maximum temperature 320 °C for 30 seconds. - Material matching for coefficient of thermal expansion is crucial for long-term reliability

Optimum RF power performance achieved by minimizing output RF bond wire length.

For optimum RF and thermal performance, Microchip recommends that the die assembly base plate be adequately bolted to a forced-air heat sink using a thermal graphite interface pad (Graphite Interface Material GCSP-017-G 170 μ m thick) for optimal heat transfer. There are many variables of the second-level assembly between the die base plate and heat sink that Microchip is unable to control and the following guidance is provided as information only. Fixing bolts should be provided as close to the die as possible to ensure an optimum pressure between the base plate and the heat sink. The bolting screws used to attach the PCB assembly to the heat sink must include washers and be tightened with a suitable tightening pattern to ensure a uniform pressure. It is advised that all surfaces be cleaned and be free of grease and dust prior to fully aligning the assembly with all screws located and tightened to finger tight. Further torquing of the screws must be achieved in multiple phases using a star shaped pattern to a recommended torque of 2.5 N/m.

Biasing

Bias-up procedure	Bias-down procedure
- Set V_G to -5V - Set V_D to 28V - Adjust V_G positive until I_D quiescent is 180mA - Limit I_D to 3A - Apply RF signal	- Turn off RF - Turn off V_D, allow drain capacitors to discharge - Turn off V_G

6. Ordering, Shipping, and Handling

Handling Recommendations

Integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Description
ICP3540-1-110I	Bare Die in Gelpak
EV56X26A	Evaluation Board Development Tool for ICP3540-1-110I

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