2-8GHz 25W PACKAGED GAN POWER AMPLIFIER

ICP0444P

Product Overview

ICONICRF's ICP0444P is a 3 stage MMIC power amplifier 50ohm matched in a flange package. Fabricated using a GaN on SiC process, the ICP0444P operates from 2-8GHz with over 44dBm CW output power and 25% PAE. ICP0444P is well suited to both commercial and defense applications.

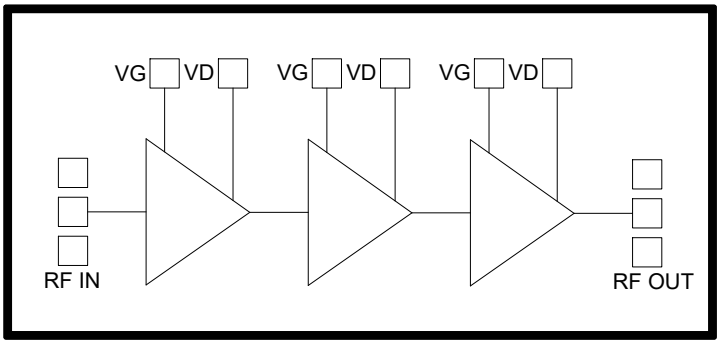
Key Features

- **Frequency Range: 2-8GHz**
- **P_{out}: 44dBm @P_{in}=23dBm**
- **PAE: 25% @P_{in}=23dBm**
- **Small Signal Gain: 25dB**
- **Bias: V_D=28V I_{DQ}=200mA**
- **Technology: GaN on SiC**
- **Lead-free and RoHS compliant**
- **Pulsed or CW operation**
- **Package Dimensions: 10mm x 20mm**

Applications

- Test and Measurement
- Communications
- Aerospace & Defense

Functional Block Diagram



Electrical Specifications

Parameter	Min.	Typ.	Max.	Units	Conditions[1]
Frequency	2		8	GHz	
Output Power	43.5	44.5		dBm	P_{in} = 23dBm, Freq = 2-6GHz
Output Power	43	44		dBm	P_{in} = 23dBm, Freq = 6-8GHz
Power Added Efficiency, PAE	18	25		%	P_{in} = 23dBm
Drain Current, I_{DRAIN}		4	5.6	A	P_{in} = 23dBm
Gate Current, I_{GATE}		0.1	10	mA	P_{in} = 23dBm
Small Signal Gain, S_{21}		25		dB	
Input Return Loss		5		dB	
Output Return Loss		6		dB	

Note: (1) Test conditions unless otherwise stated V_D = 28V, I_{DQ}=200mA, T_A = 25°C, CW

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1. Electrical Specification

1.1. Absolute Maximum Ratings

Parameter	Absolute Maximum
Drain Voltage (V_D)	32V
CW Input Power 50Ohm, T_A=25°C	+26dBm
Channel Temperature	275°C
Storage Temperature	-65°C to +150°C

Thermal and Reliability

Parameter	Value
Thermal Resistance	1.33 °C/W

- Thermal resistance calculated using IR measurement of the channel temperature.

Note:
Exceeding any one or combination of these limits may cause permanent damage to this device.

Microchip Technology Inc. does not recommend sustained operation near these survivability limits.

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1.2. Small Signal Performance

Typical Data over Temperature

Test conditions: V_D=28V, I_{DQ}=200mA

Figure 1-1. S_{21} vs Freq

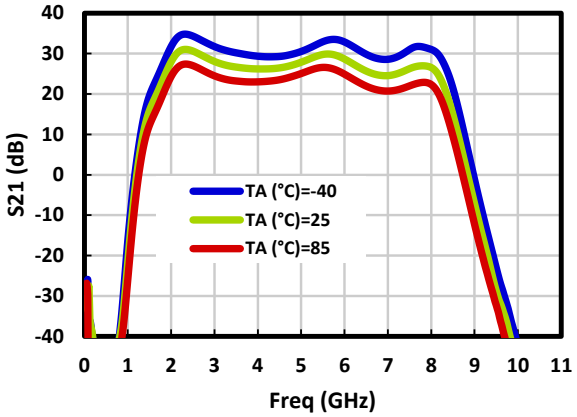


Figure 1-2. S_{11} vs Freq

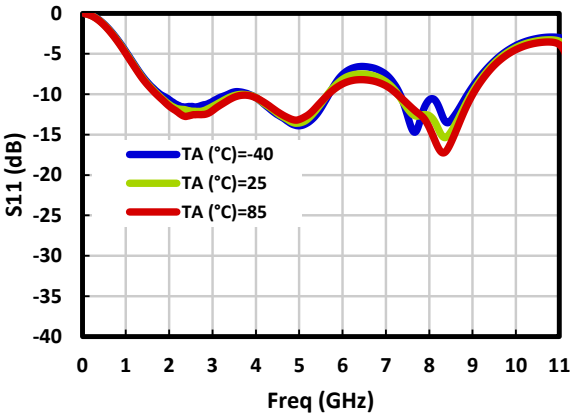
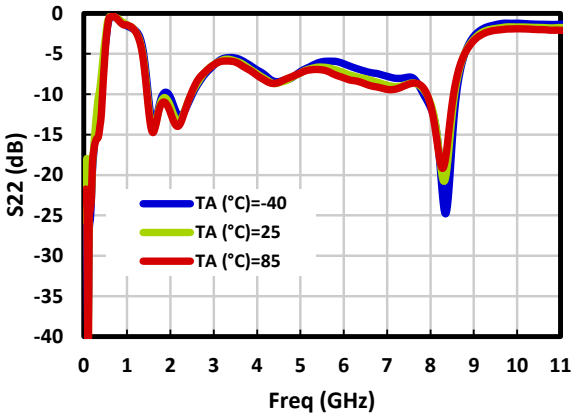


Figure 1-3. S_{22} vs Freq



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Typical Data over V_D

Test conditions: I_{DQ}=200mA

Figure 1-4. S_{21} vs Freq

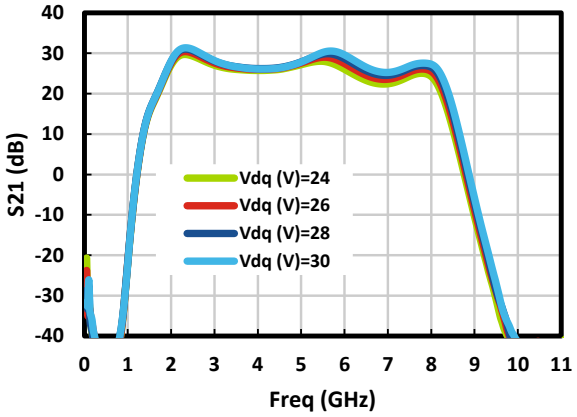


Figure 1-5. S_{11} vs Freq

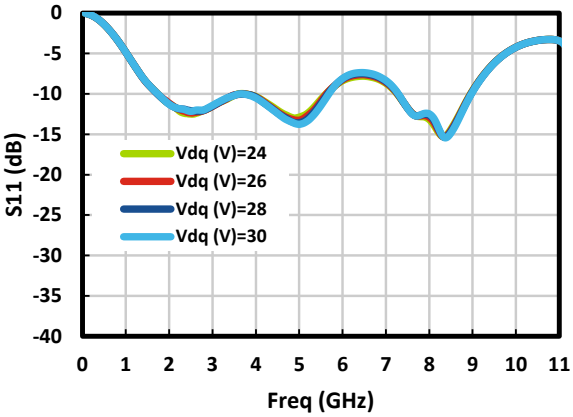
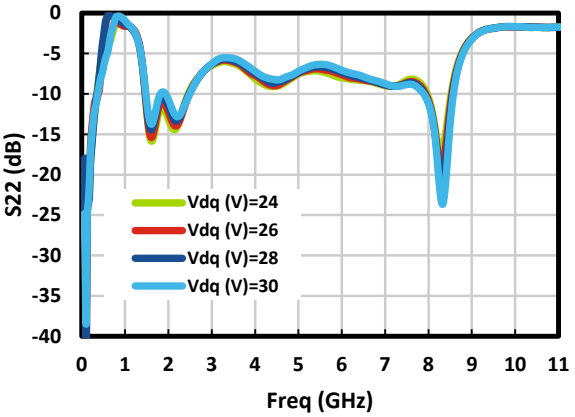


Figure 1-6. S_{22} vs Freq



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Typical Data over I_{DQ}

Test conditions: V_D=28V, T_A=25°C

Figure 1-7. S_{21} vs Freq

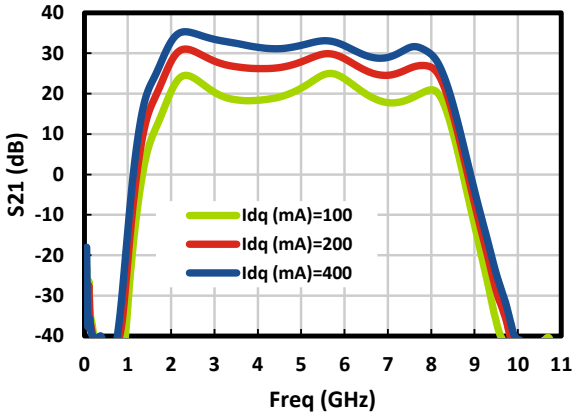


Figure 1-8. S_{11} vs Freq

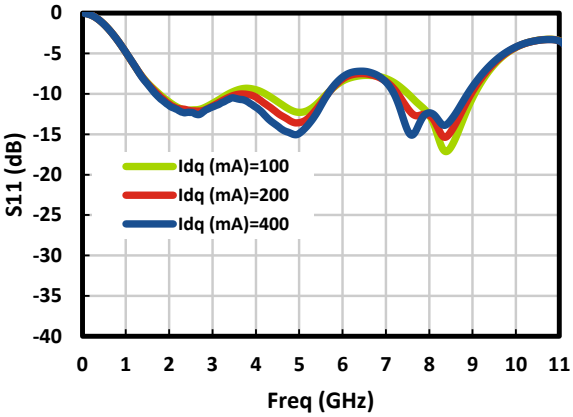
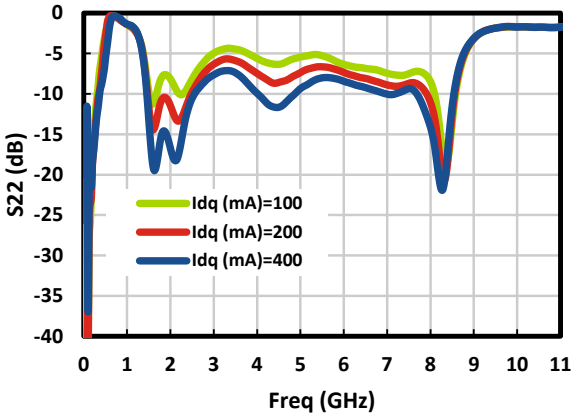


Figure 1-9. S_{22} vs Freq



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1.3. Large Signal Performance

Typical CW Power Data

Test conditions: V_D=28V, I_{DQ}=200mA, T_A=25°C

Figure 1-10. P_{out} vs. P_{in}

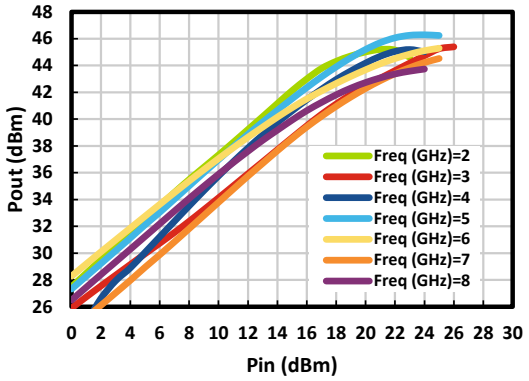


Figure 1-11. Gain vs. P_{out}

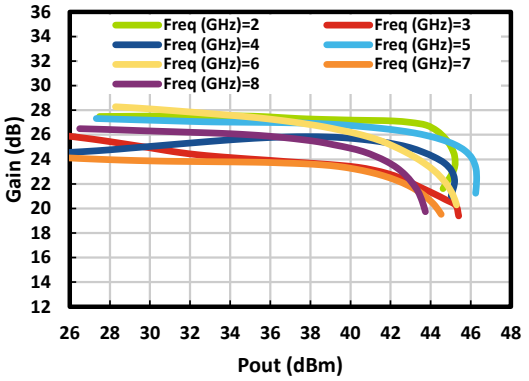


Figure 1-12. PAE vs. P_{out}

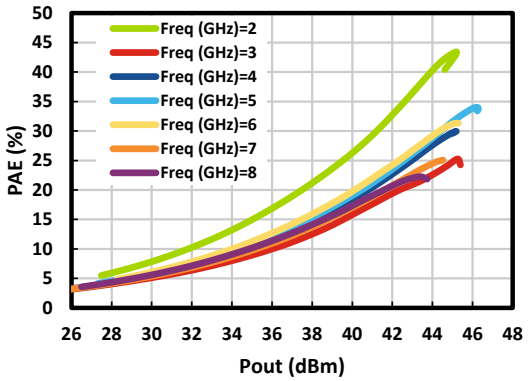


Figure 1-13. I_D vs. P_{out}

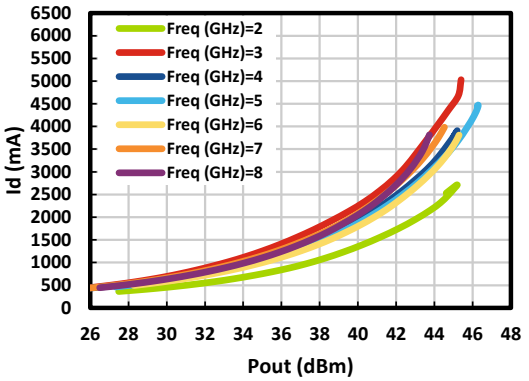


Figure 1-14. P_{out} vs. Freq.

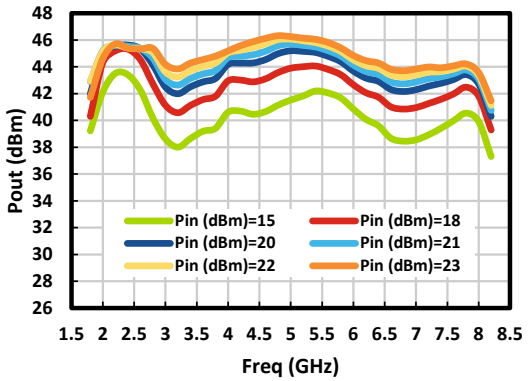
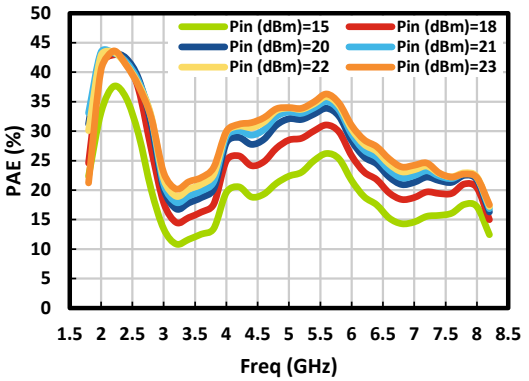


Figure 1-15. PAE vs. Freq.



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Typical CW Power Data over Ambient Temperature, T_A

Test conditions: V_D=28V, I_{DQ}=200mA

Figure 1-16. Gain vs. P_{out} at 2GHz

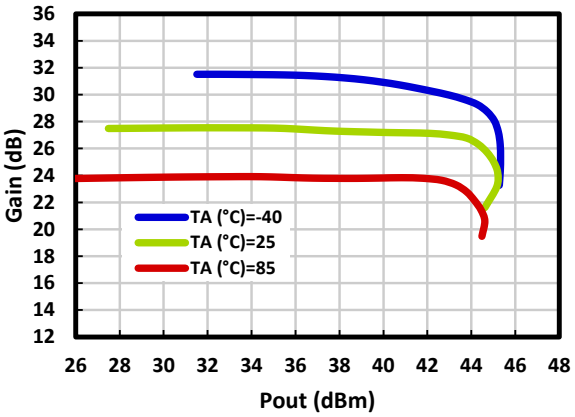


Figure 1-17. PAE vs. P_{out} at 2GHz

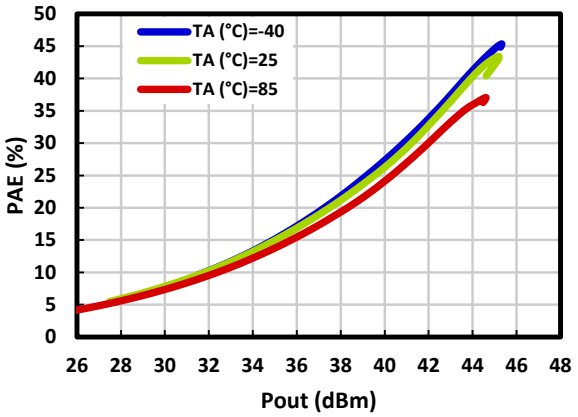


Figure 1-18. Gain vs. P_{out} at 3GHz

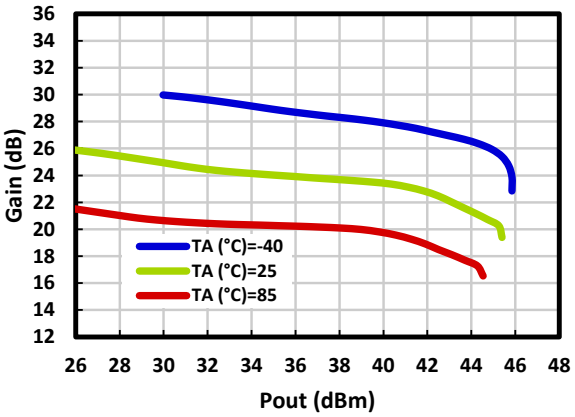


Figure 1-19. PAE vs. P_{out} at 3GHz

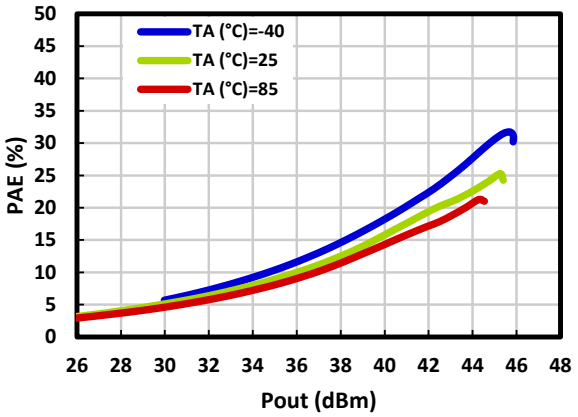


Figure 1-20. Gain vs. P_{out} at 4GHz

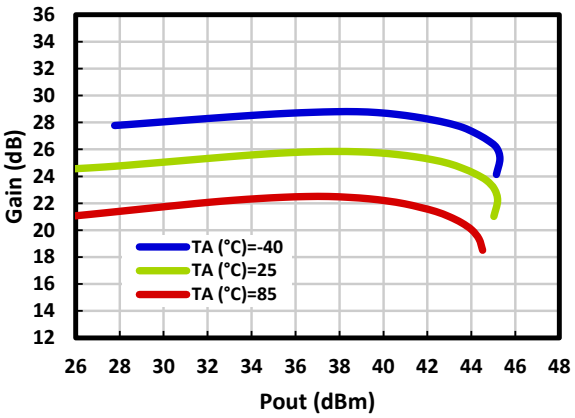
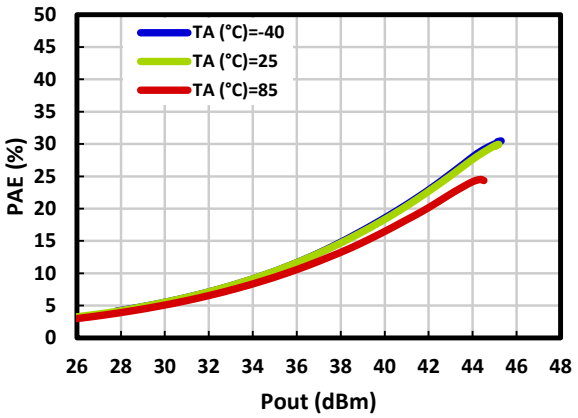


Figure 1-21. PAE vs. P_{out} at 4GHz



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Figure 1-22. Gain vs. P_{out} at 5GHz

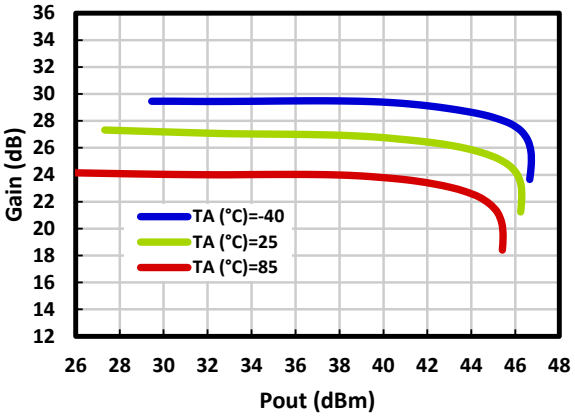


Figure 1-23. PAE vs. P_{out} at 5GHz

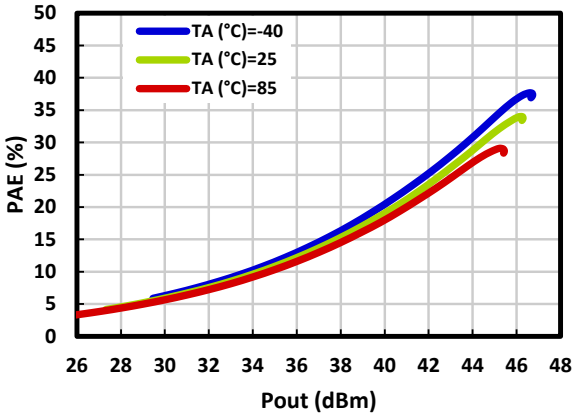


Figure 1-24. Gain vs. P_{out} at 6GHz

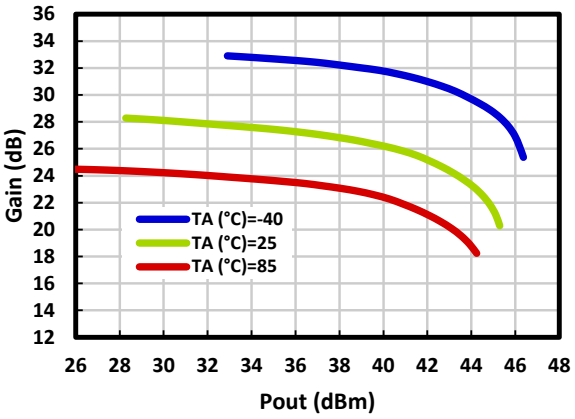


Figure 1-25. PAE vs. P_{out} at 6GHz

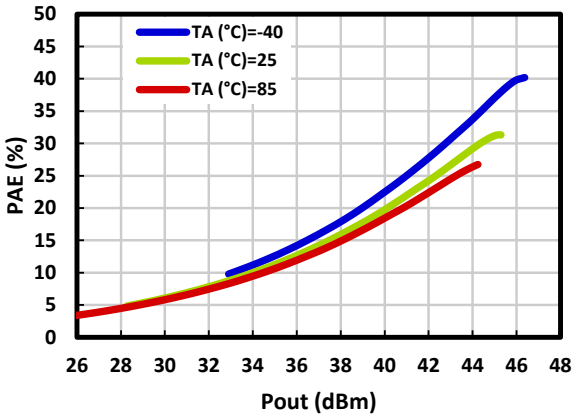


Figure 1-26. Gain vs. P_{out} at 7GHz

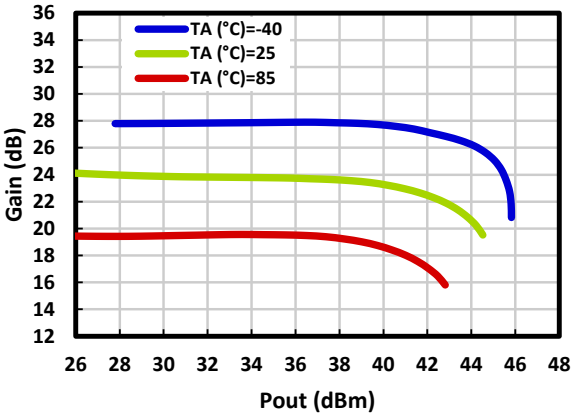
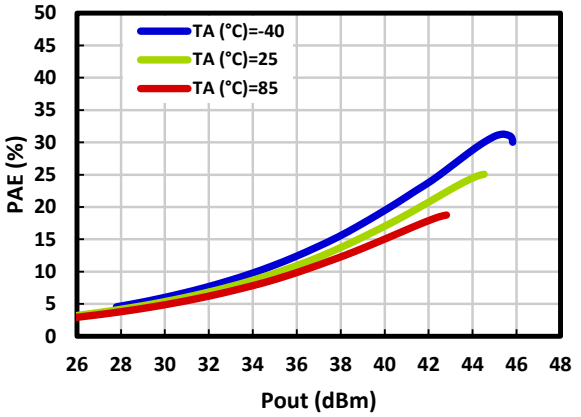


Figure 1-27. PAE vs. P_{out} at 7GHz



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Figure 1-28. Gain vs. P_{out} at 8GHz

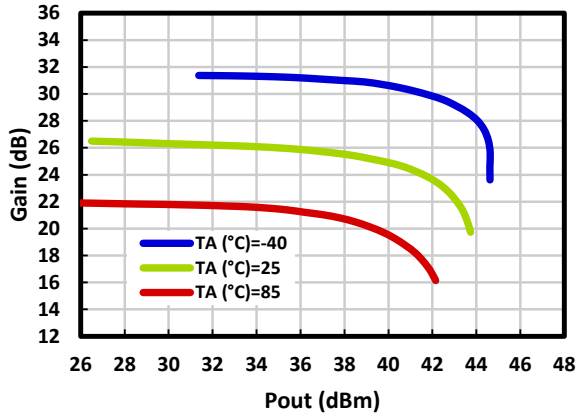


Figure 1-29. PAE vs. P_{out} at 8GHz

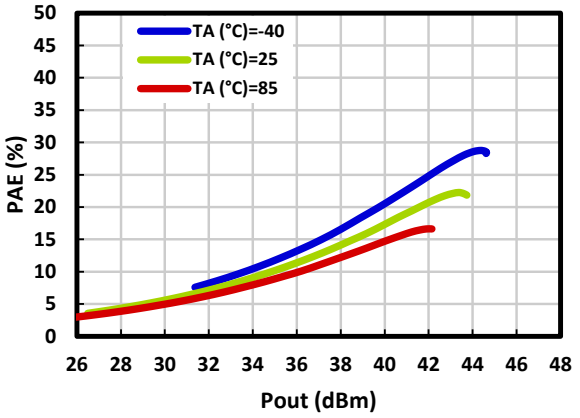


Figure 1-30. P_{out} vs. Freq.

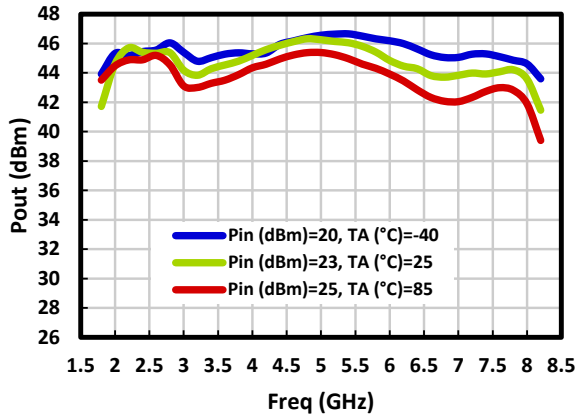
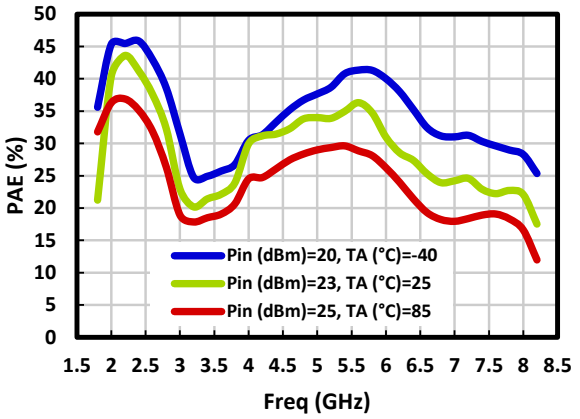


Figure 1-31. PAE vs. Freq.



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Typical CW Power Data over V_D

Test conditions: I_{DQ}=200mA, T_A=25°C

Figure 1-32. Gain vs. P_{out} at 2GHz

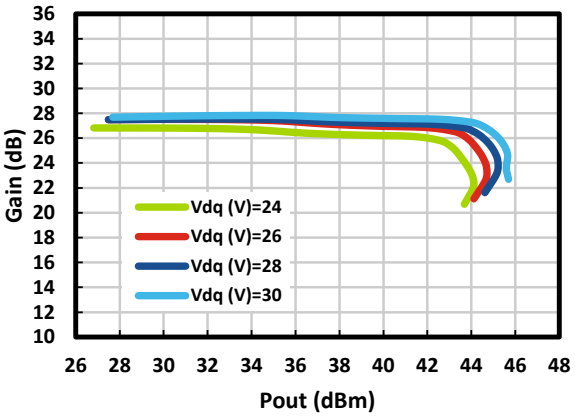


Figure 1-33. PAE vs. P_{out} at 2GHz

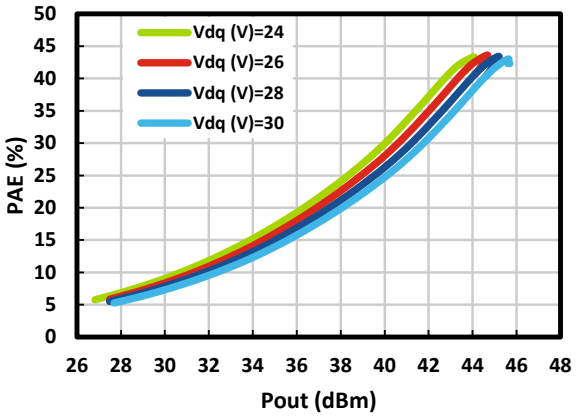


Figure 1-34. Gain vs. P_{out} at 3GHz

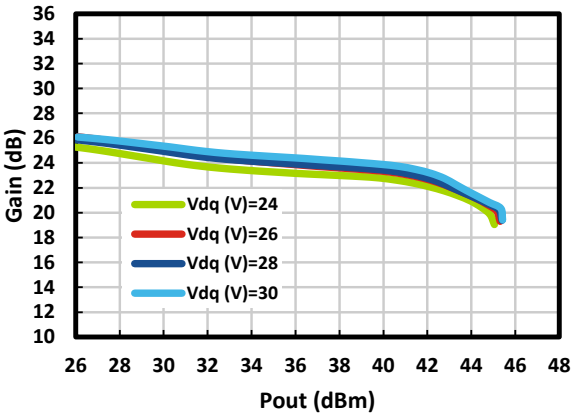


Figure 1-35. PAE vs. P_{out} at 3GHz

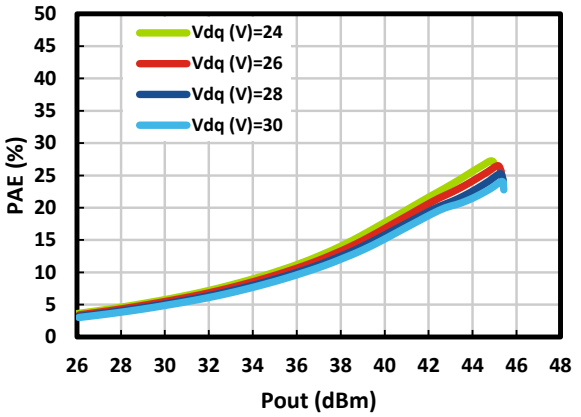


Figure 1-36. Gain vs. P_{out} at 4GHz

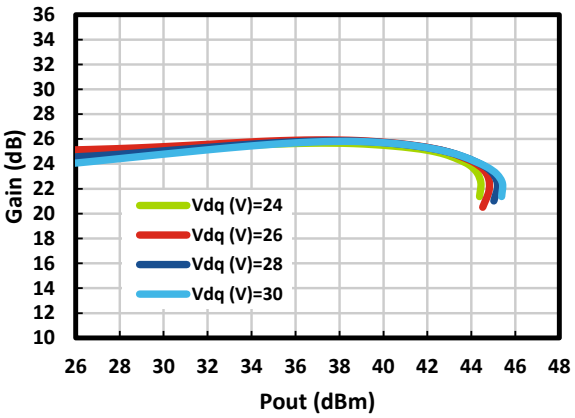
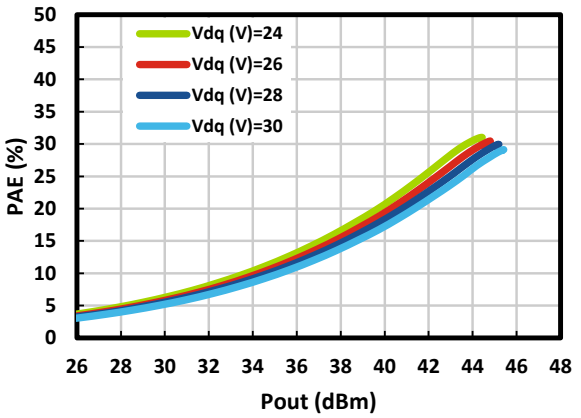


Figure 1-37. PAE vs. P_{out} at 4GHz



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Figure 1-38. Gain vs. P_{out} at 5GHz

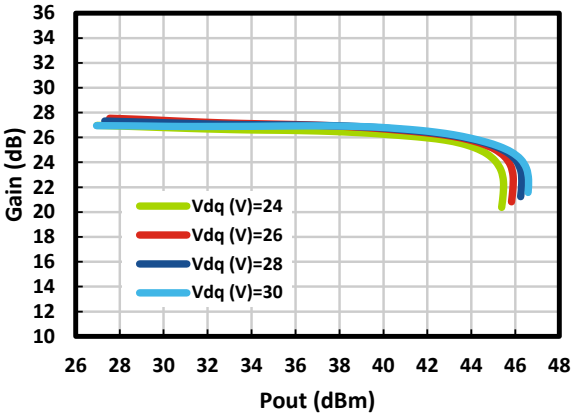


Figure 1-39. PAE vs. P_{out} at 5GHz

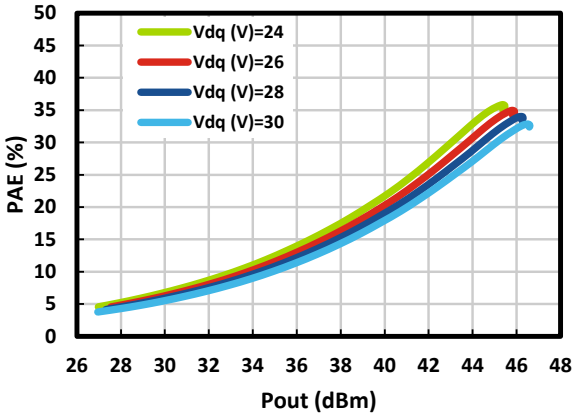


Figure 1-40. Gain vs. P_{out} at 6GHz

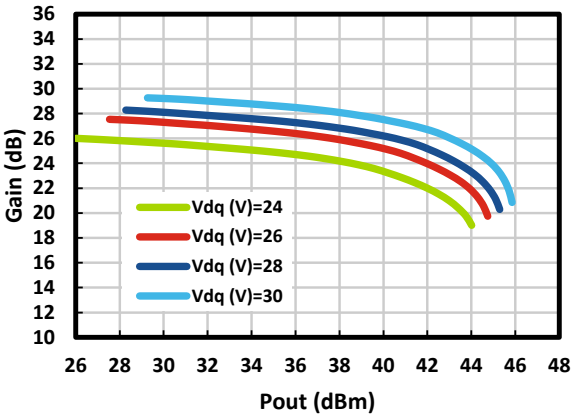


Figure 1-41. PAE vs. P_{out} at 6GHz

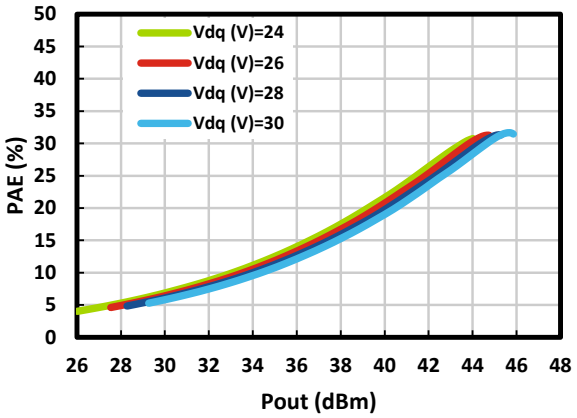


Figure 1-42. Gain vs. P_{out} at 7GHz

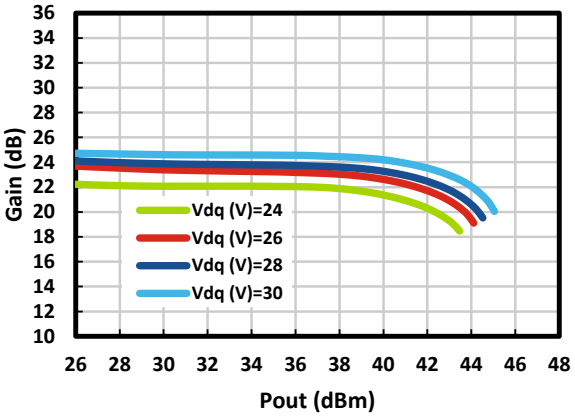
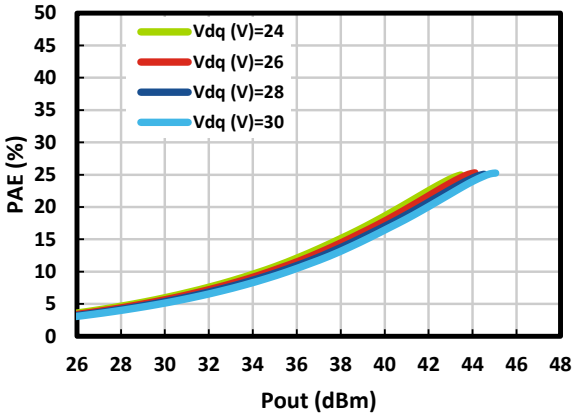


Figure 1-43. PAE vs. P_{out} at 7GHz



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Figure 1-44. Gain vs. P_{out} at 8GHz

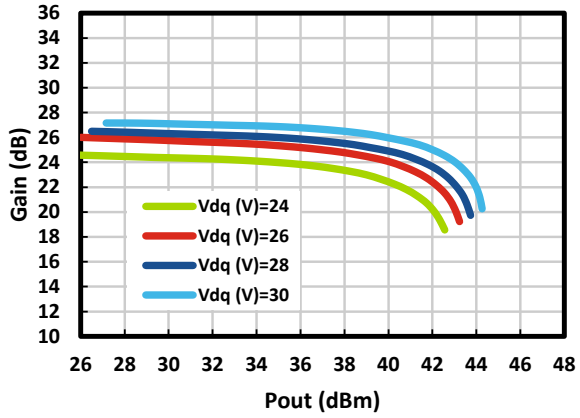


Figure 1-45. PAE vs. P_{out} at 8GHz

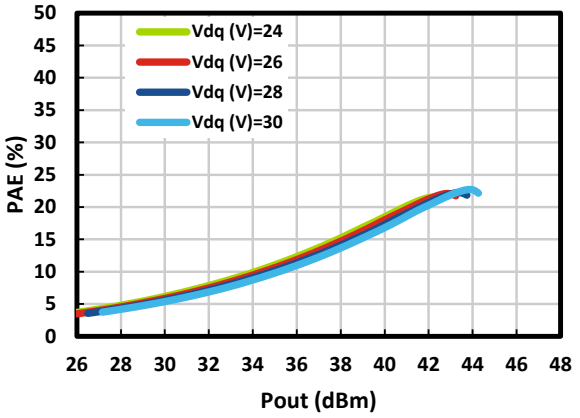


Figure 1-46. P_{out} vs. Freq., P_{in}=23dBm

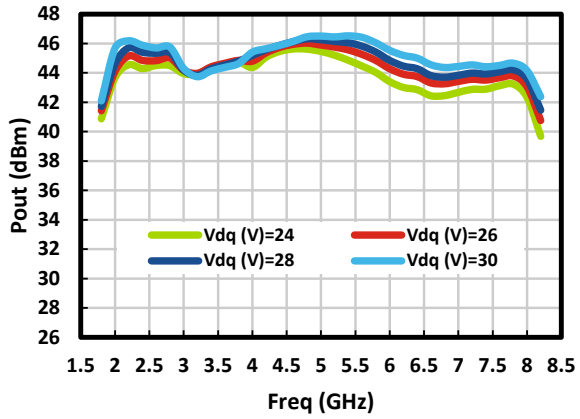
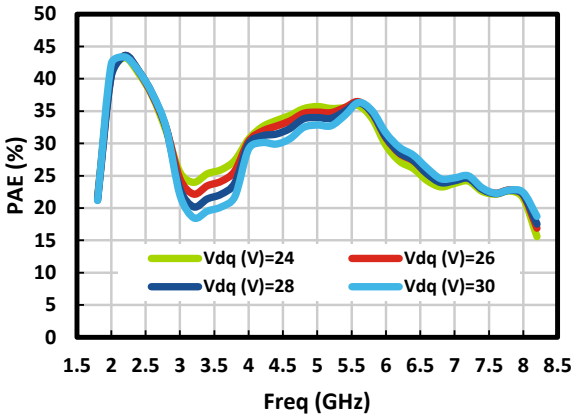


Figure 1-47. PAE vs. Freq., P_{in}=23dBm



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Typical CW Power Data over I_{DQ}

Test conditions: V_D=28V, T_A=25°C

Figure 1-48. Gain vs. P_{out} at 2GHz

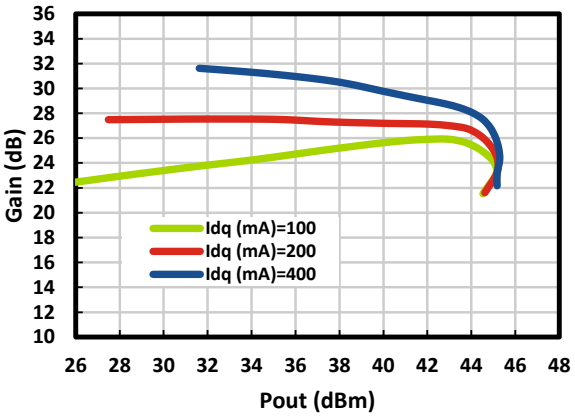


Figure 1-49. PAE vs. P_{out} at 2GHz

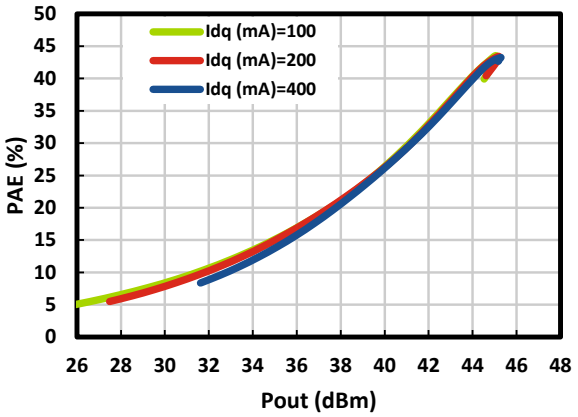


Figure 1-50. Gain vs. P_{out} at 3GHz

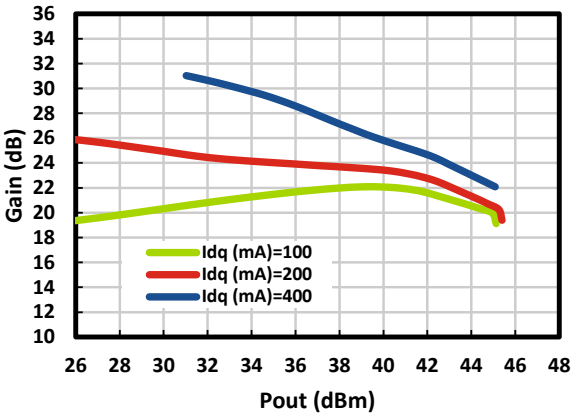


Figure 1-51. PAE vs. P_{out} at 3GHz

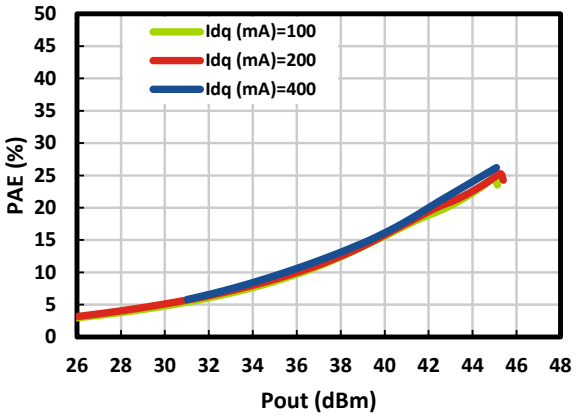


Figure 1-52. Gain vs. P_{out} at 4GHz

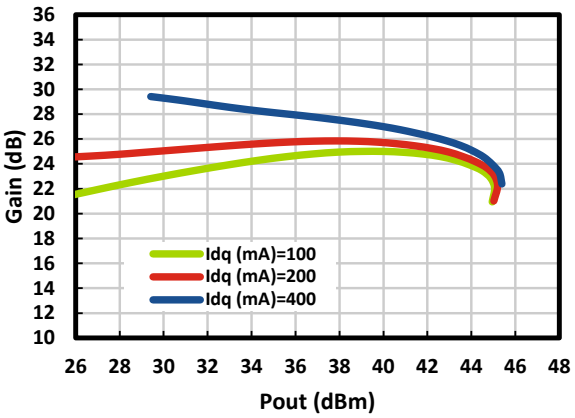
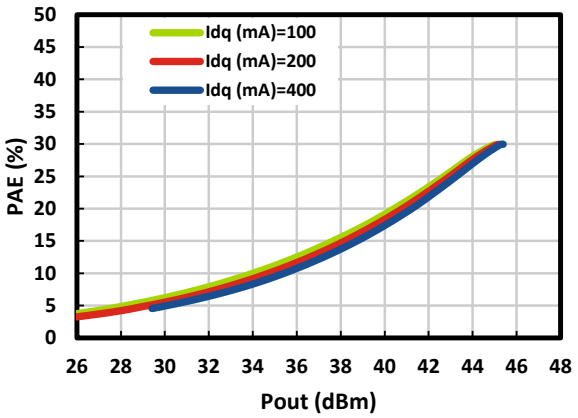


Figure 1-53. PAE vs. P_{out} at 4GHz



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Figure 1-54. Gain vs. P_{out} at 5GHz

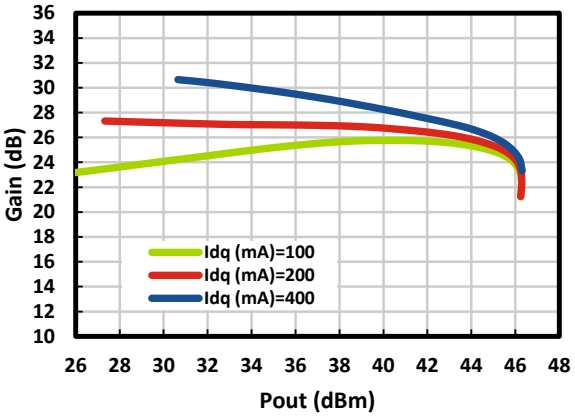


Figure 1-55. PAE vs. P_{out} at 5GHz

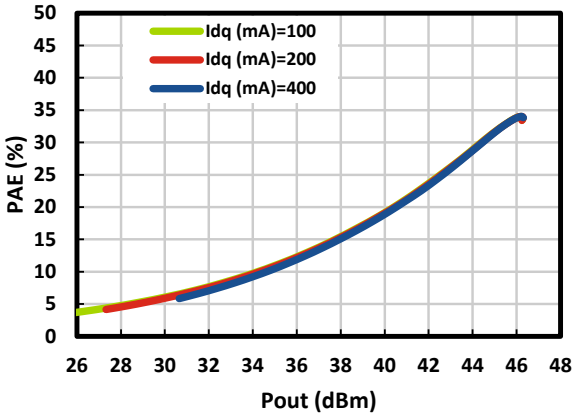


Figure 1-56. Gain vs. P_{out} at 6GHz

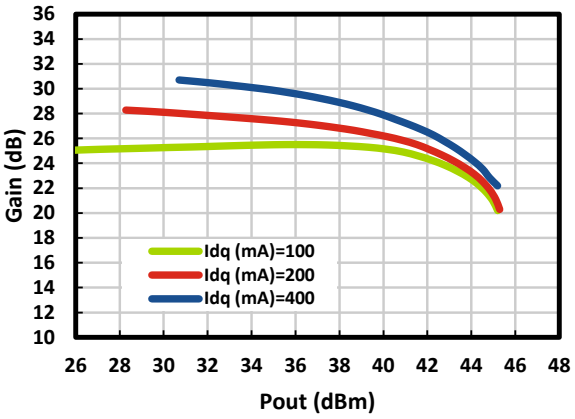


Figure 1-57. PAE vs. P_{out} at 6GHz

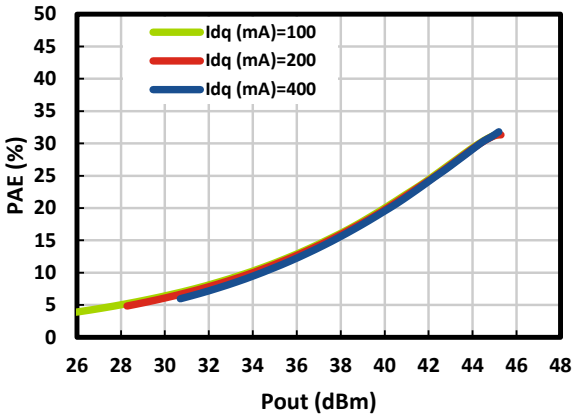


Figure 1-58. Gain vs. P_{out} at 7GHz

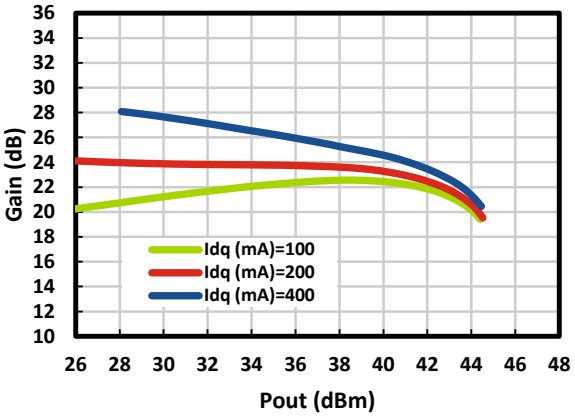
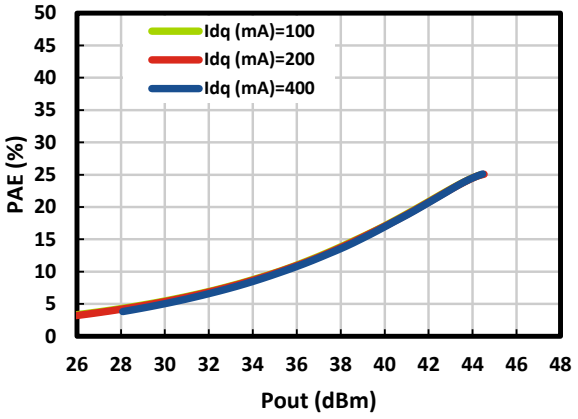


Figure 1-59. PAE vs. P_{out} at 7GHz



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Figure 1-60. Gain vs. P_{out} at 8GHz

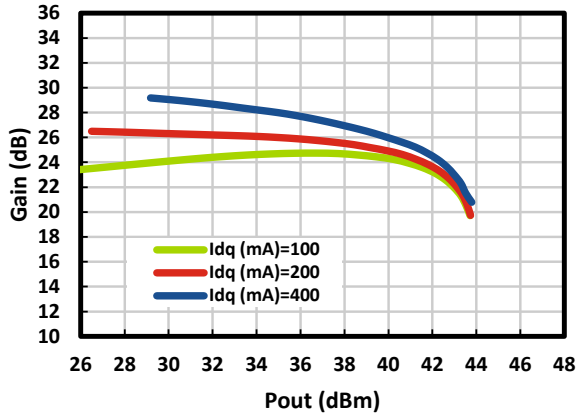


Figure 1-61. PAE vs. P_{out} at 8GHz

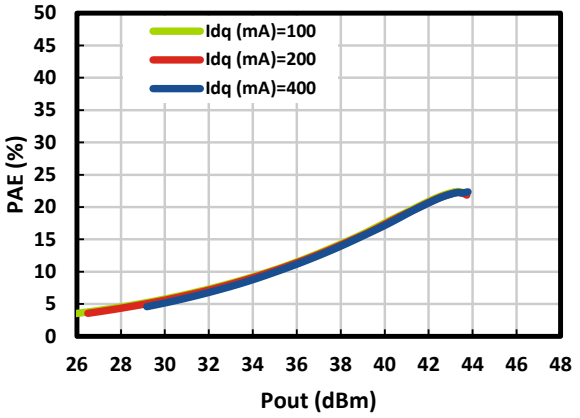


Figure 1-62. P_{out} vs. Freq., P_{in}=23dBm

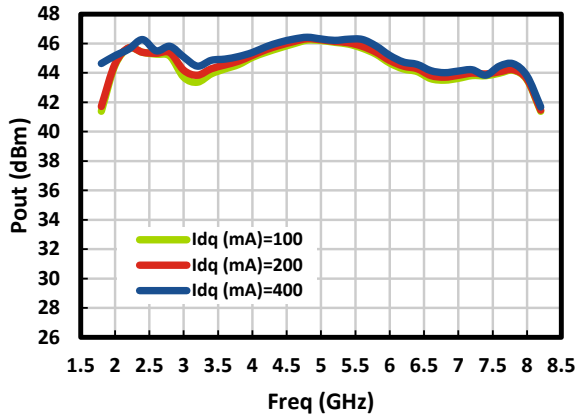
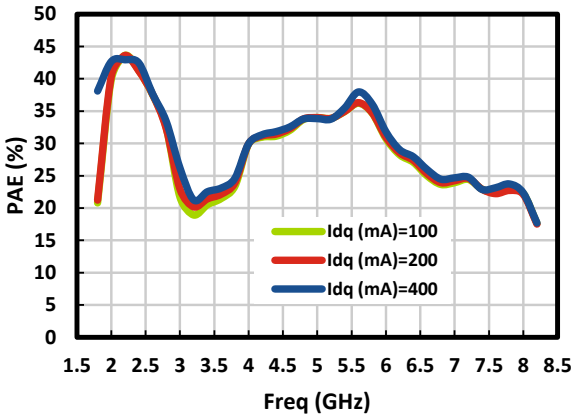
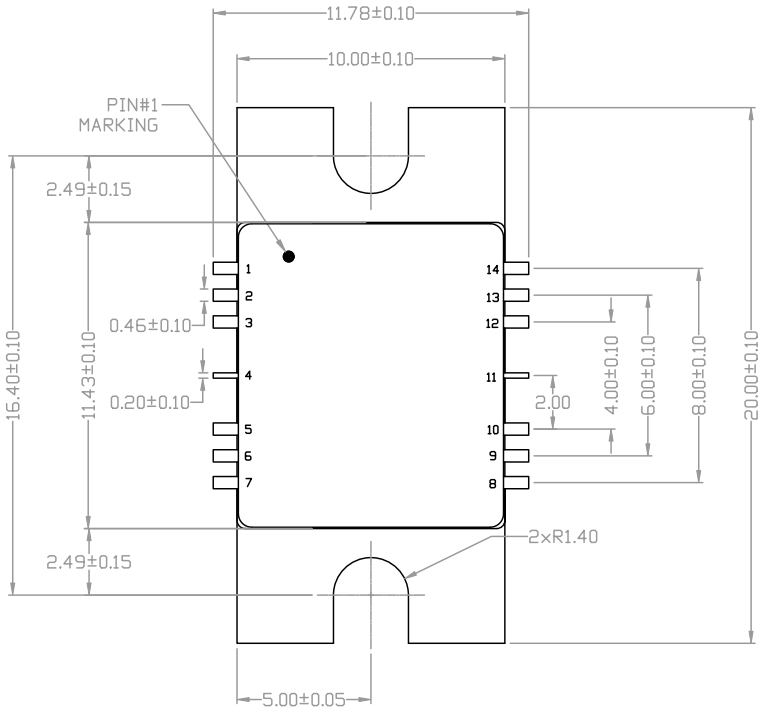


Figure 1-63. PAE vs. Freq., P_{in}=23dBm

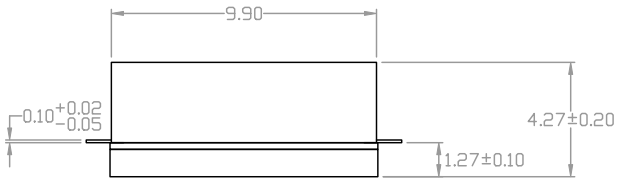


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2. Mechanical Drawing



TOP VIEW



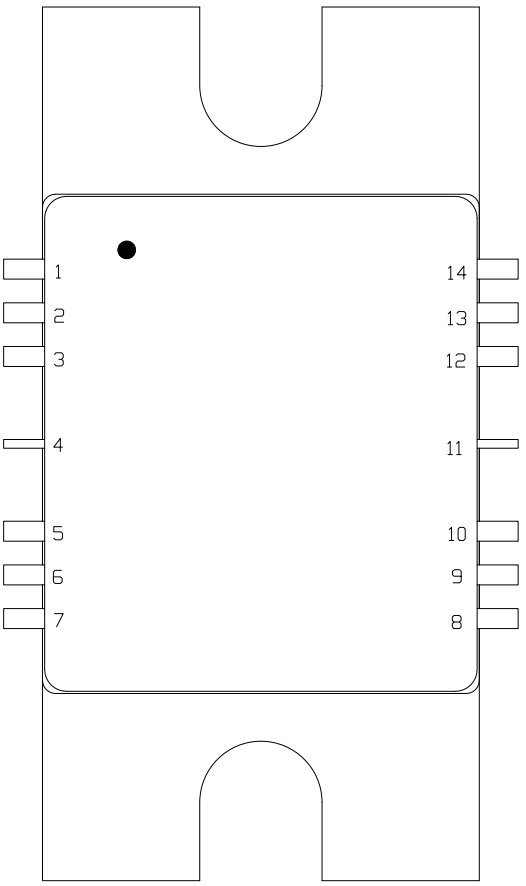
SIDE VIEW

Units: mm

Pin No	Function	Description
1	V_G	Gate bias, decoupling and bypass caps required.
2, 6, 7, 9, 13	No connect	Pins can be connected to ground or left open circuit
3, 5, 10, 12	GND	Ground connection
4	RF_{IN}	50Ω RF input. DC blocked
8, 14	V_D	Drain bias, decoupling and bypass caps required, bias must be applied to both pins.
11	RF_{OUT}	50Ω RF output. DC blocked
Flange	GND	RF and DC ground

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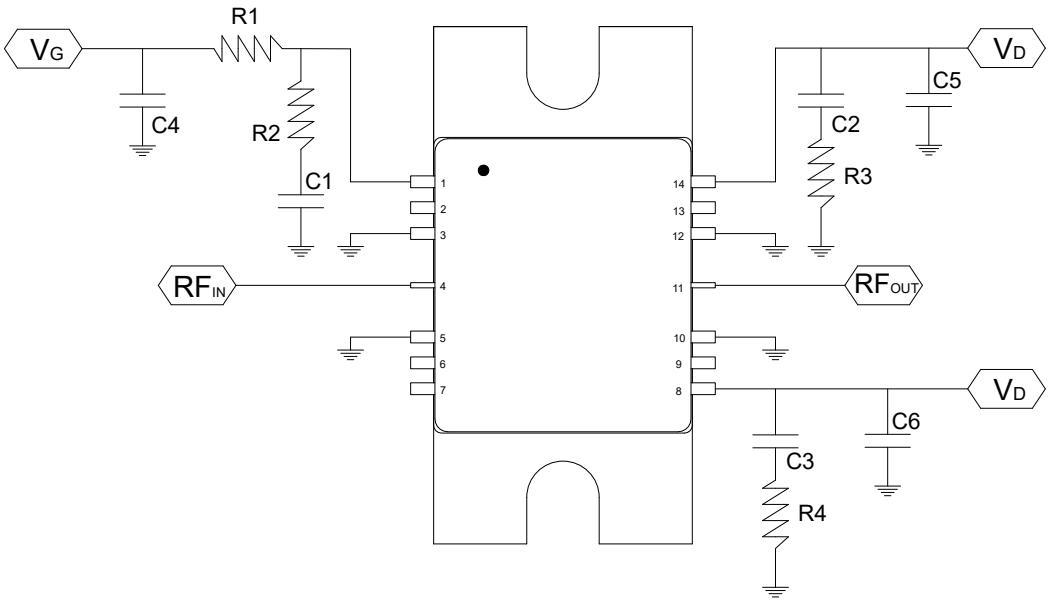
3. Pinout



Pin No	Function	Description
1	V_G	Gate bias, decoupling and bypass caps required
2, 6, 7, 9, 13	No Connect	Pin can be connected to ground or left open circuit
3, 5, 10, 12	GND	Ground connection
4	RF_{IN}	50Ω RF input. DC blocked
8, 14	V_D	Drain bias, decoupling and bypass caps required. Bias must be applied to both pins
11	RF_{OUT}	50Ω RF output. DC blocked
Flange	GND	RF and DC ground connection

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4. Application Circuit

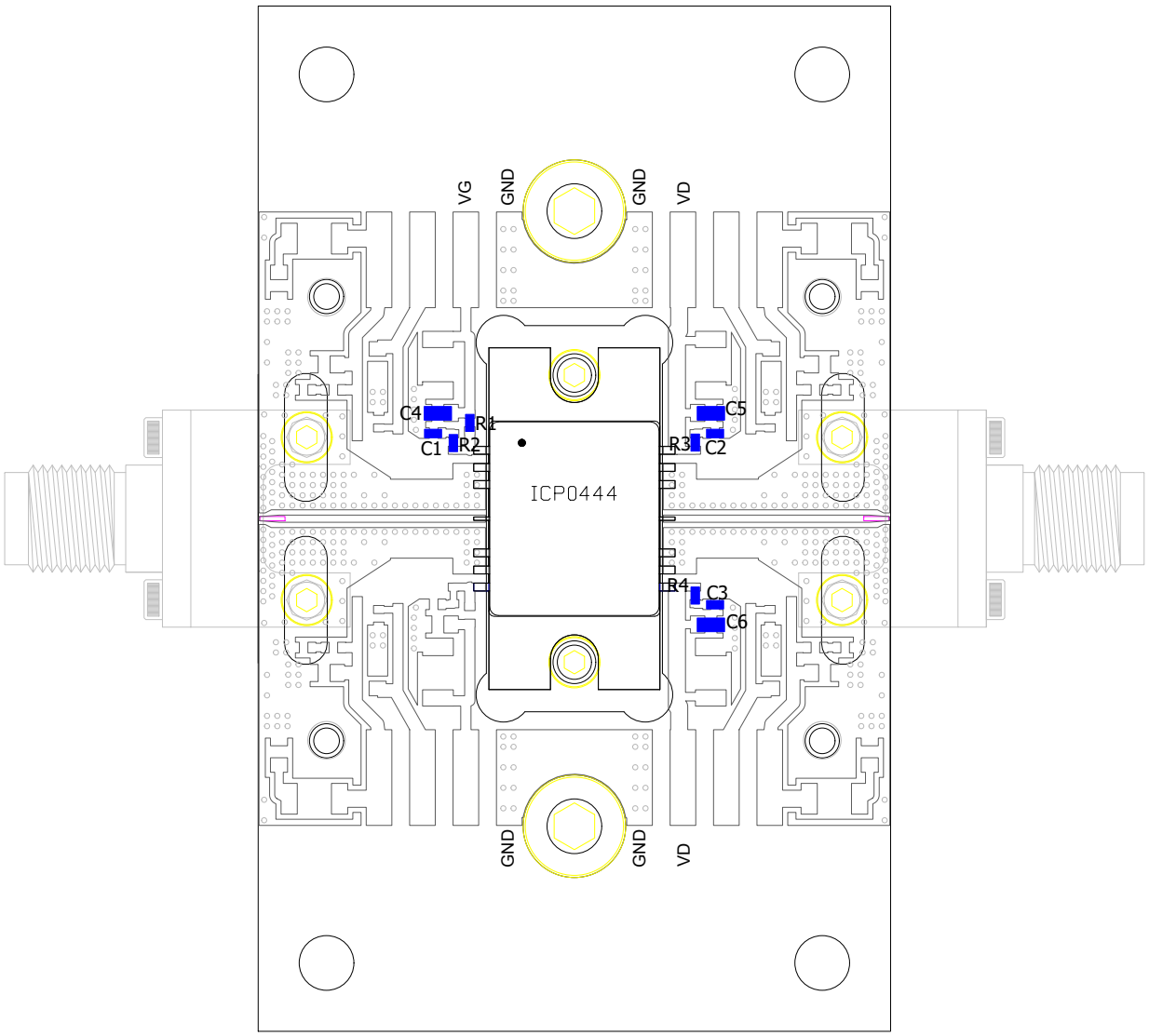


Bill of materials

Component ID	Value	Details	Manufacturer Part No.
C1 - C3	10nF	10nF Capacitor, 10%, 50V, 0402	Various
C4 - C6	1µF	1µF Capacitor, 10%, 35V, 0603	Various
R1	0Ω	0Ω Resistor, 0402	Various
R2- R4	5.1Ω	5.1Ω Resistor, 0402	Various

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5. Evaluation Board



PCB Fabrication

PCB Construction	Details
Top Layer	0.5oz Cu + ENEPIG Electroless Nickel 3-6μm Electroless Palladium 0.05-0.3μm Immersion Gold 0.04-0.06μm
Dielectric	RO4350B 10mil
Bottom Layer	0.5oz Cu + ENEPIG Electroless Nickel 3-6μm Electroless Palladium 0.05-0.3μm Immersion Gold 0.04-0.06μm

Key Features	Details
Overall Thickness	Approx 0.32mm
VIA Plating Thickness	>15μm

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6. Other considerations

Assembly Guidance

The package must be bolted to a thermally conductive base plate and the pins aligned with the PCB tracks. For optimum thermal transfer use an electrically conductive thermal compound before fixing the package.

Solderability

Its recommended to manually solder the leads to the PCB using a no-clean solder. This avoids washing the part after soldering.

Components are compatible with lead-free solder with a temperature of 260ºC

For optimum RF and thermal performance Microchip recommends the die assembly base plate is adequately bolted to a forced air heat sink using a thermal graphite interface pad (Graphite Interface Material GCSP-017-G 17µm thick) for optimal heat transfer.

There are many variables of the second level assembly between the die base plate and heat sink that Microchip are unable to control and the following guidance is provided as information only. Fixing bolts should be provided as close to the die as possible to ensure an optimum pressure between the base plate and heat sink.

The bolting screws used to attach the PCB assembly to the heat sink must include washers and be tightened with a suitable tightening pattern to ensure a uniform pressure. It is advised all surfaces are cleaned and free of grease and dust prior to fully aligning the assembly with all screws located and tightened to finger tight. Further torquing of the screws must be achieved in multiple phases using a star shaped pattern to a recommended torque of 2.5N/m.

Bias-up procedure

1. Set V_G to -5V
2. Set V_D to 28V
3. Adjust V_G positive until I_D quiescent is 200mA
4. Limit I_D to 7A
5. Apply RF signal

Bias-down procedure

1. Turn off RF
2. Turn off V_D, allow drain capacitors to discharge
3. Turn off V_G

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7. Ordering, Shipping, and Handling

Handling Recommendations

Integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity.

Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Description
ICP0444-1-451I	2-8GHz 25W Packaged GaN Power Amplifier, Ceramic Flange Package in Tube Format
EV-ICP0444-1-451I	Dev Tool for ICP0444-1-451I, Fully Assembled Evaluation Board with RF Test Data

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New York, NY			Tel: 46-31-704-60-40
Tel: 631-435-6000			**Sweden - Stockholm**
San Jose, CA			Tel: 46-8-5090-4654
Tel: 408-735-9110			**UK - Wokingham**
Tel: 408-436-4270			Tel: 44-118-921-5800
Canada - Toronto			Fax: 44-118-921-5820
Tel: 905-695-1980			
Fax: 905-695-2078			

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