PL671-01

PicoEMI™ Programmable Spread Spectrum Clock

FEATURES

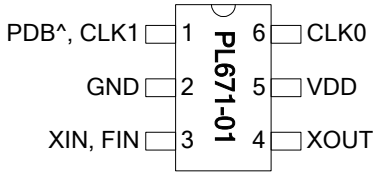
- Advanced programmable PLL with Spread Spectrum
- Crystal or Reference Clock input
  - Fundamental crystal: 10MHz to 40MHz
  - Reference input: 1MHz to 200MHz
- Accepts ≥0.1V reference signal input voltage
- Output frequency range: up to 166MHz @ 2.5V or up to 200MHz @ 3.3V operation
- Up to 3 programmable outputs
- Programmable Spread Spectrum Modulation Magnitude:
  - Center Spread: ±0.125% to ±2.0% in ±0.125% steps
  - Down Spread: -0.25% to -4.0% in 0.25% steps
- Spread Spectrum On/Off selection
- Programmable output drive (4mA, 8mA, 16mA)
- Low Cycle to Cycle jitter.
- Single 2.5V to 3.3V, ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 8-pin SOP, MSOP and 6-pin SOT GREEN/RoHS compliant packaging

DESCRIPTION

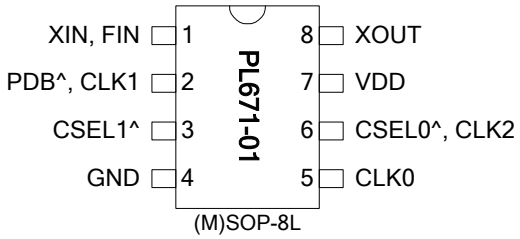
The PL671-01 is an advanced programmable Spread Spectrum clock generator (PSSCG), and a member of PicoPLL™ Programmable Clock family.

The PL671-01 offers up to three 200MHz outputs, and allows for programming the modulation type (Center or Down Spread) as well as 16 modulation magnitudes (±0.125% to ±2.0% or -0.25% to -4.0%). In addition, the CSEL[0:1] pins can be used to toggle the device thru 4 pre-programmed configurations. The option of being able to turn 'ON/OFF' the Spread Spectrum modulation allows for completing a design with PL671-01 and having the assurance of turning 'ON' the EMI modulation, if EMI becomes an issue. The PL671-01's frequency modulation greatly reduces the fundamental and harmonic frequencies' peak magnitude, therefore reducing the system level Electro Magnetic Interference (EMI), by as much as 20dB

PIN CONFIGURATION



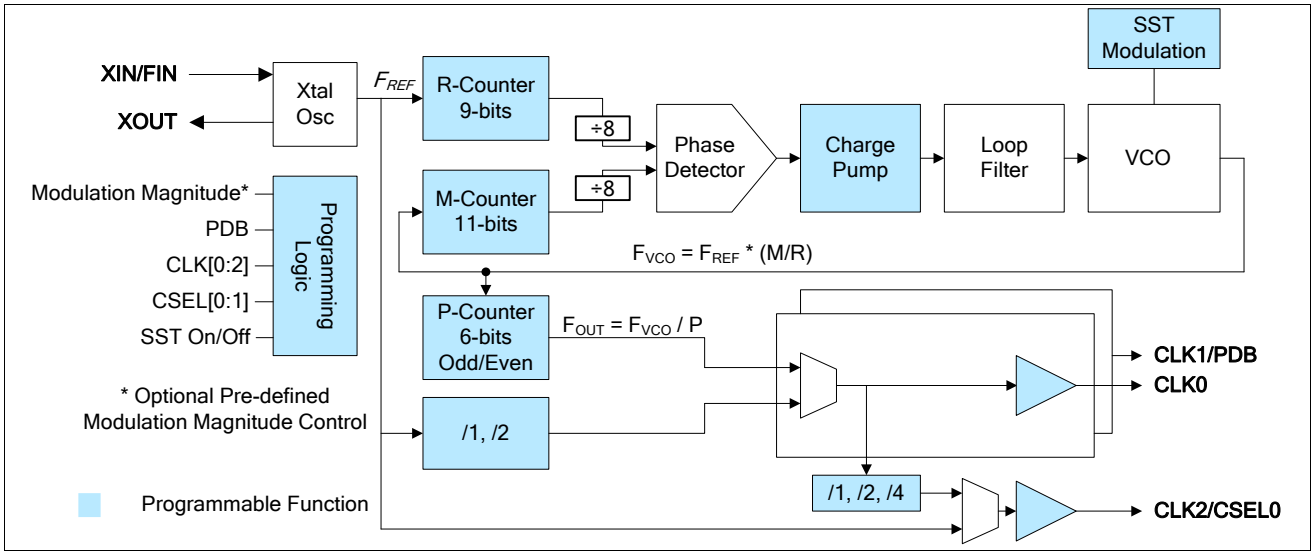
SOT23-6L



(M)SOP-8L

Note: ^ Denotes 60KΩ Pull-up resistor

BLOCK DIAGRAM



PicoEMI™ Programmable Spread Spectrum Clock

KEY PROGRAMMING PARAMETERS

CLK[0:2] Output Frequency	SST Modulation Magnitude (Spread Percentage)	Programmable Input/Output	Output Drive Strength
$F_{OUT} = F_{REF} * M / (R * P)$ where M =11 bit R = 9 bit P = 6 bit • CLK0= F_{REF}, $F_{REF}/2$ or F_{VCO}/P* • CLK1= F_{REF}, $F_{REF}/2$ or F_{VCO}/P* • CLK2= F_{REF}, CLK0, CLK0/2 or CLK0/4 * 'P' is a 6-bit Odd/Even divider.	16 programmable modulation magnitudes to choose from: • Center Spread: ±0.125% to ±2.0% in ±0.125% steps • Down Spread: -0.25% to -4.0% in 0.25% steps • SST On/Off Control.	Programmable I/O's include: • PDB – input • CSEL[0:1] Configuration Selection - input • CLK[0:2] - output	Three optional drive strengths to choose from: •Low: 4mA •Std: 8mA (default) •High: 16mA

PACKAGE PIN ASSIGNMENT

Name	(M)SOP-8L Pin #	SOT23-6L Pin #	Type	Description
XIN, FIN	1	3	I	Crystal or Reference input pin
PDB, CLK1	2	1	I/O	This pin can be programmed as PDB (input) or CLK1 (output). **Power Down (PDB)** input. This pin has an internal 60KΩ pull up resistor and turns off the oscillator and the output when pulled to logic "0". **Clock1 (CLK1)** output. This optional clock can be set to F_{REF}, $F_{REF}/2$ or F_{OUT} (Programmable PLL output).
CSEL1	3	-	I	Selector pin used to toggle between two pre-programmed configurations (When used in conjunction with CSEL0 there are four possible pre-defined configurations to choose from).
GND	4	2	P	GND connection
CLK0	5	6	O	Programmable Clock Output with spread spectrum.
CSEL0, CLK2	6	-	I/O	This pin can be programmed to function as CSEL0 (input) or CLK2 (output). **CSEL0** input. Selector pin used to toggle between two pre-programmed configurations (When used in conjunction with CSEL1 there are four possible pre-defined configurations to choose from). **CLK2** output. This optional clock can be set to F_{REF}, CLK0, CLK0/2 or CLK0/4.
VDD	7	5	P	VDD connection (2.25~3.63V)
XOUT	8	4	O	Crystal output pin. Do Not Connect when using FIN.

PDB Logic	Osc	PLL	Output
0	Off	Off	Hi Z (Default)
1	Normal Operation (Default)		

PicoEMI™ Programmable Spread Spectrum Clock

FUNCTIONAL DESCRIPTION

PL671-01 is a highly featured, very flexible, advanced programmable PLL design for high performance, low-power Spread Spectrum modulation applications. The PL671-01 accepts a fundamental input crystal of 10MHz to 40MHz or a reference clock input of 1MHz to 200MHz and is capable of producing three SST modulated outputs up to 200MHz. This flexible design allows the PL671-01 to deliver any PLL generated frequency, FREF (Crystal or Ref Clk) frequency or FREF /2 to CLK0, CLK1 and/or CLK2. Alternate configuration using CSEL0 & CSEL1 allows the device to choose from up to 4 different pre-defined settings providing a range of spread settings, drive levels and outputs to choose from. Some of the design features of the PL671-01 are mentioned below.

PLL Programming

The PLL in the PL671-01 is fully programmable. The PLL is equipped with a 9-bit input frequency divider (R-Counter), and an 11-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 6-bit post VCO Odd/Even divider (P-Counter). The output frequency is determined by the following formula [FOUT = (FREF * M)/(R*P).

Modulation Magnitude and Type

The PL671-01 provides the following programmable capabilities for Modulation Type and Modulation Magnitude (Spread Percentage):

Modulation Type	Modulation Magnitude	Programming Steps
Center Spread	±0.125% thru ±2.00%	±0.125%
Down Spread	-0.25% thru -4.00%	0.25%

Modulation Rate

The PL671-01 modulation rate is defined as FREF (Crystal or Ref Clk Frequency) divided by 8 times the R-counter, i.e. Modulation Rate = (FREF / 8R). The rate can be changed by choosing alternate R-Counter settings.

Clock Outputs (CLK[0:2])

CLK0 is the main clock output. The PL671-01 can also be programmed with additional clock outputs CLK1 and CLK2. The outputs of CLK[0:2] can be configured as described below:

- CLK0= FREF, FREF/2 or FVCO/P*
- CLK1= FREF, FREF/2 or FVCO/P*
- CLK2= FREF, CLK0, CLK0/2 or CLK0/4

Where

FREF - Reference (Crystal or Ref Clk) Frequency
FOUT = FREF * M / (R * P)

The output drive level of each output can be independently programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA). The output frequency can be programmed up to 200MHz at 3.3V (166MHz at 2.5V).

Power-Down Control (PDB)

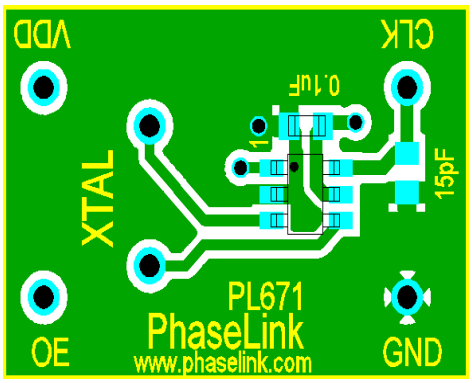
When activated (logic '0'), PDB 'Disables the PLL, the oscillator circuitry, counters, and all other active circuitry. In Power Down mode the IC consumes <10µA of power. The PDB input incorporates a pull up resistor giving a default condition of logic "1".

Configuration Selectors (CSEL[0:1])

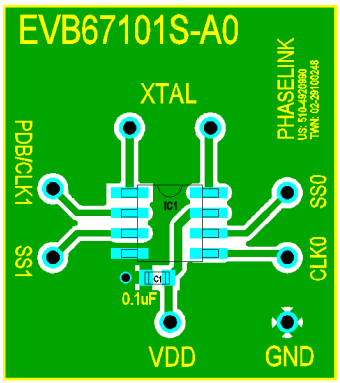
The PL671-01 has the capability to be programmed with 4 distinct configurations and to toggle "On the Fly" between these configurations using the selector pads CSEL0 and CSEL1. CSEL0 and CSEL1 both incorporate a 60kΩ pull up resistor giving a default condition of logic "1".

When the CSEL0, CLK2 pin is programmed to be CLK2, CSEL0 is set to a default of Logic 1. This means that two programmable configurations are available to be selected "On the Fly" using CSEL1.

LAYOUT RECOMMENDATIONS



Evaluation Board # EVB67101T-A0
SOT23-6 pin



Evaluation Board # EVB67101S-A0
SOP-8 pin

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces (>1 inch) as “striplines” or “microstrips” with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply

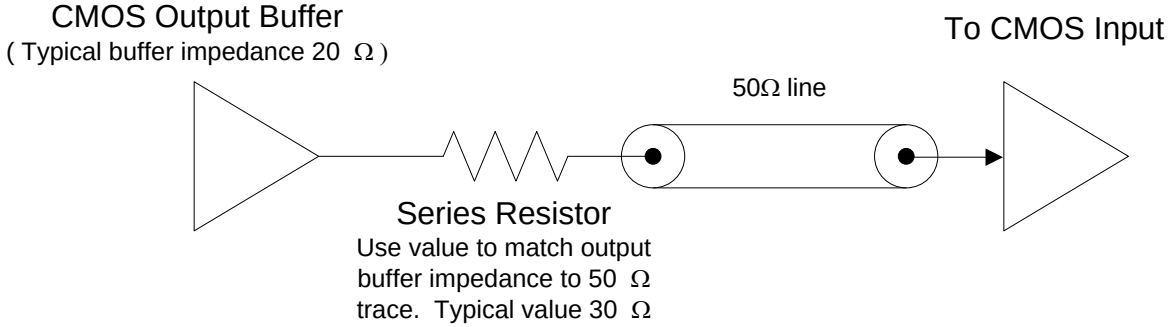
- Multiple VDD pins should be decoupled separately for best performance.

- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources

- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs using frequencies < 50MHz and 0.01μF for designs using frequencies > 50MHz.

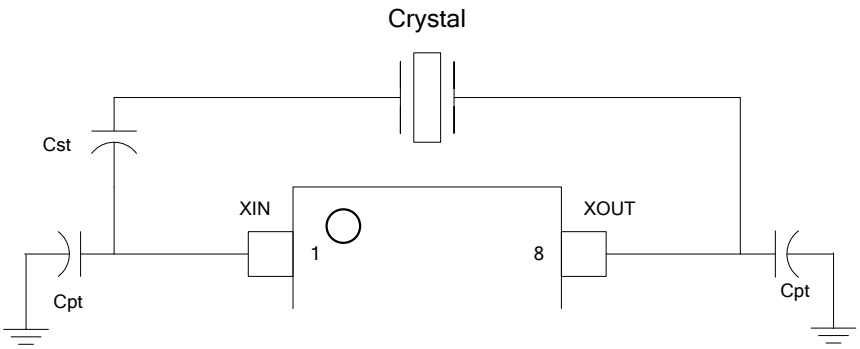
Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



Crystal Tuning Circuit

Series and parallel capacitors used to fine tune the crystal load to the circuit load.



CST – Series Capacitor, used to lower circuit load to match crystal load. Raises frequency offset. This can be eliminated by using a crystal with a Cload of equal or greater value than the oscillator.

CPT – Parallel Capacitors, Used to raise the circuit load to match the crystal load. Lowers frequency offset.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency(XIN)	Fundamental Crystal	10		40	MHz
Input (FIN) Frequency	@ V_{DD} =3.3V	1		200	MHz
	@ V_{DD} =2.5V			166	
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.9		V_{DD}	Vpp
Input (FIN) Signal Amplitude	Internally AC coupled (Low Frequency) 3.3V ≤50MHz, 2.5V ≤40MHz	0.1		V_{DD}	Vpp
Output Frequency	@ V_{DD} =3.3V			200	MHz
	@ V_{DD} =2.5V			166	
Settling Time	At power-up (after V_{DD} increases over 2.25V)			2	ms
Output Enable Time	PDB Function; Ta=25° C, 15pF Load			2	ms
Output Rise Time	15pF Load, 10/90% V_{DD}, Standard Drive		2.0	3.0	ns
	15pF Load, 10/90% V_{DD}, High Drive		1.2	1.7	
Output Fall Time	15pF Load, 90/10% V_{DD}, Standard Drive		2.0	3.0	ns
	15pF Load, 90/10% V_{DD}, High Drive		1.2	1.7	
Duty Cycle	At V_{DD} / 2	45	50	55	%
Cycle to Cycle Jitter*	$T_{CYC-CYC}$ Over output frequency range @ 3.3V			100	ps

* Note: Jitter performance depends on the programming parameters.

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic	I_{DD}	At 27MHz, 3.3V, load=15pF, (PDB=1)			15	mA
		PDB=0 [with reference input pin (FIN) pulled down]			10	µA
Operating Voltage	V_{DD}		2.25		3.63	V
Power Supply Ramp	t_{PU}	Time for V_{DD} to reach 90% V_{DD}. Power ramp must be monotonic.			100	ms
Output Low Voltage	V_{OL}	I_{OL} = +4mA (Std. Drive)			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA (Std. Drive)	V_{DD} – 0.4			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	4			mA
Output Current, Standard Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V	16			mA

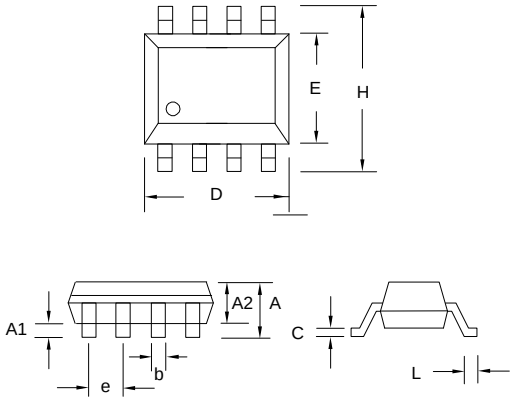
CRYSTAL SPECIFICATIONS

PARAMETERS		SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency		F_{XIN}	10		40	MHz
Crystal Loading Rating		$C_{L\ (xtal)}$		15		pF
Maximum Sustainable Drive Level					100	µW
Operating Drive Level				30		µW
Metal Can Crystal	Shunt Capacitance	C0			5.5	pF
	ESR Max	ESR			50	Ω
Small SMD Crystal	Shunt Capacitance	C0			2.5	pF
	ESR Max	ESR			80	Ω

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

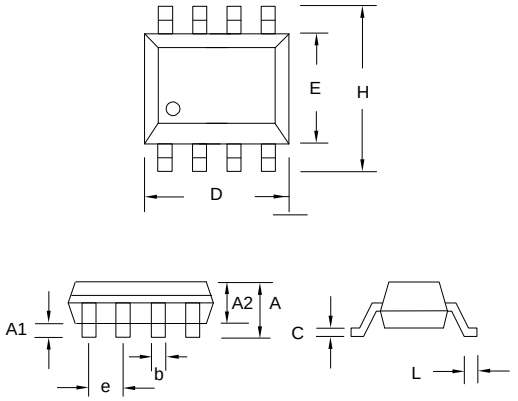
MSOP-8L

Symbol	Dimension in MM	
	Min.	Max.
A	---	1.10
A1	0.05	0.15
A2	0.81	0.91
B	0.25	0.40
C	0.13	0.23
D	2.90	3.10
E	2.90	3.10
H	4.90 BSC	
L	0.445	0.648
e	0.65 BSC	



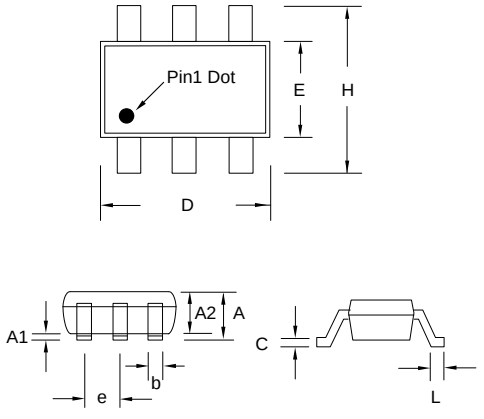
SOP-8L

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	



SOT23-6L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.00
L	0.35	0.55
e	0.95 BSC	



PicoEMI™ Programmable Spread Spectrum Clock

ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944 492-0800 • Fax: (408) 474-1000

PART NUMBER
The order number for this device is a combination of the following:
Part Number, Package Type and Operating Temperature Range

PL671-01-XXX X X - X

Part Number

3 DIGIT ID Code *
(will be assigned at programming time)

Package Type
M=MSOP-8L
S=SOP-8L
T-SOT23-6L

Temperature
C=Commercial (0°C to 70°C)
I=Industrial (-40°C to 85°C)

Shipping Option
None=Tube
R=Tape & Reel

* Micrel will assign a unique 3-digit ID code for each approved programmed part number.

Part/Order Number	Package Option
PL671-01-XXXMC	8-Pin MSOP (Tube)
PL671-01-XXXMC-R	8-Pin MSOP (Tape and Reel)
PL671-01-XXXSC	8-Pin SOP (Tube)
PL671-01-XXXSC-R	8-Pin SOP (Tape and Reel)
PL671-01-XXXTC-R	6-Pin SOT23 (Tape and Reel)

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