LAN8042

Quad 1G/10G/25G MACsec Optical Ethernet PHY Transceiver

Highlights

- Four 1G/10G/25G serial Host interfaces
  - IEEE 802.3-2018 compliant
  - Backplane Ethernet with KR/RS FEC
- Four 1G/10G/25G serial Line interfaces
  - IEEE 802.3-2018 compliant
  - SFP, XFP, SFP+, QSFP+, SFP28 & QSFP28
- Integrated cross-connect features
  - Any line port connectible to any host port
  - 1:1 and 1+1 host redundancy
- IEEE 802.1AE-2018 MACsec
- Unencrypted VLAN tags per IEEE 802.1AE-2018 (was 802.1AEcg)
- Encrypted Ethernet inside unencrypted MPLS headers
- TSN frame preemption
- PCS and MAC retimer modes
- 256-BALL HFC-BGA (14 x 14 mm)
- Extended temperature range -40°C (T_A) to +110°C (T_J)

Target Applications

- 5G Small Cell
- Industrial
- Enterprise IT
- Broadband

Key Benefits

- MACsec support
  - Compliant to IEEE 802.1AE-2018, providing Confidentiality, Anti-Replay Protection and Data Integrity
  - GCM-AES-128 and GCM-AES-256 configurable per-SA
  - Port-based and Flow-based encryption with 128 SAKs supporting up to 64 SAs per port, with statistics kept per SA, vPort, and Port
  - VLAN Tag Bypass (tag in clear) of up to four VLAN tags
  - Extended Packet Numbering (XPN)
  - TSN Support:
    - -Frame Preemption
    - -MACsec bandwidth expansion handled using TSN-friendly constant rate formats (Pause flow control also supported)
  - MACsec EtherType is configurable per-port
  - MACsec of Ethernet over MPLS (EoMPLS) with up to five MPLS labels (MPLS header unencrypted)
- PCS Retimer mode
  - Fully configurable Ethernet PHY on Host and Line
  - Host and Line must be of same speed but can be of different formats (e.g. Host is Backplane Ethernet with KR FEC, Line is Optical Ethernet with RS FEC)
  - Host and Line may be synchronous or may have PPM clock differences handled by rate adaptation
  - TSN Frame Preemption support
- MAC Retimer (Ethernet serial PHY with MACsec mode)
  - Fully configurable Ethernet MAC and PHY on Host and Line
  - Host and Line must be of the same speed (e.g., 25G Ethernet), but can be of different formats (e.g., KR FEC on Host and RS FEC on Line)
  - Host and Line may be fully synchronous or may have PPM clock differences handled by rate adaptation
  - TSN Frame Preemption support
  - MACsec support
- IEEE 802.3-2018 support for:
  - 1000BASE: KX, SX, LX
  - 10GBASE: “CR”, KR, SR, LR, ER
    - -KR: KR FEC, ANEG, Training
  - 25GBASE: CR, CR-S, KR, KR-S, SR, LR, ER
    - -KR FEC, RSE FEC,ANEG, Training
- Loopback support
- Diagnostics
  - RX Eye Monitor plot
  - PRBS generator/checker
- Support for jumbo frames up to 10 KB (10,240 bytes)
- PHY Management Interface is MDIO or SPI
  - High-speed SPI can be used simultaneously with MDIO to support high-bandwidth management needs of MACsec
- Pin-strapping options
- 40 GPIOs which alternately support:
  - Two-wire Module Management Interface per port
  - Two chip Interrupts
  - Two LEDs (Link, Activity) per port
- Coma mode support to eliminate port link bouncing at startup and to synchronize LEDs
- Power down and power saving modes

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- Reference clock inputs
  - System Reference Clock
- Synchronous Ethernet support
  - Two recovered clock outputs, each selectable to be from any Line recovered clock
  - Recovered clock outputs are optionally squelched when the applicable clock is deemed unreliable
- JTAG support

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1.0 INTRODUCTION

1.1 General Description

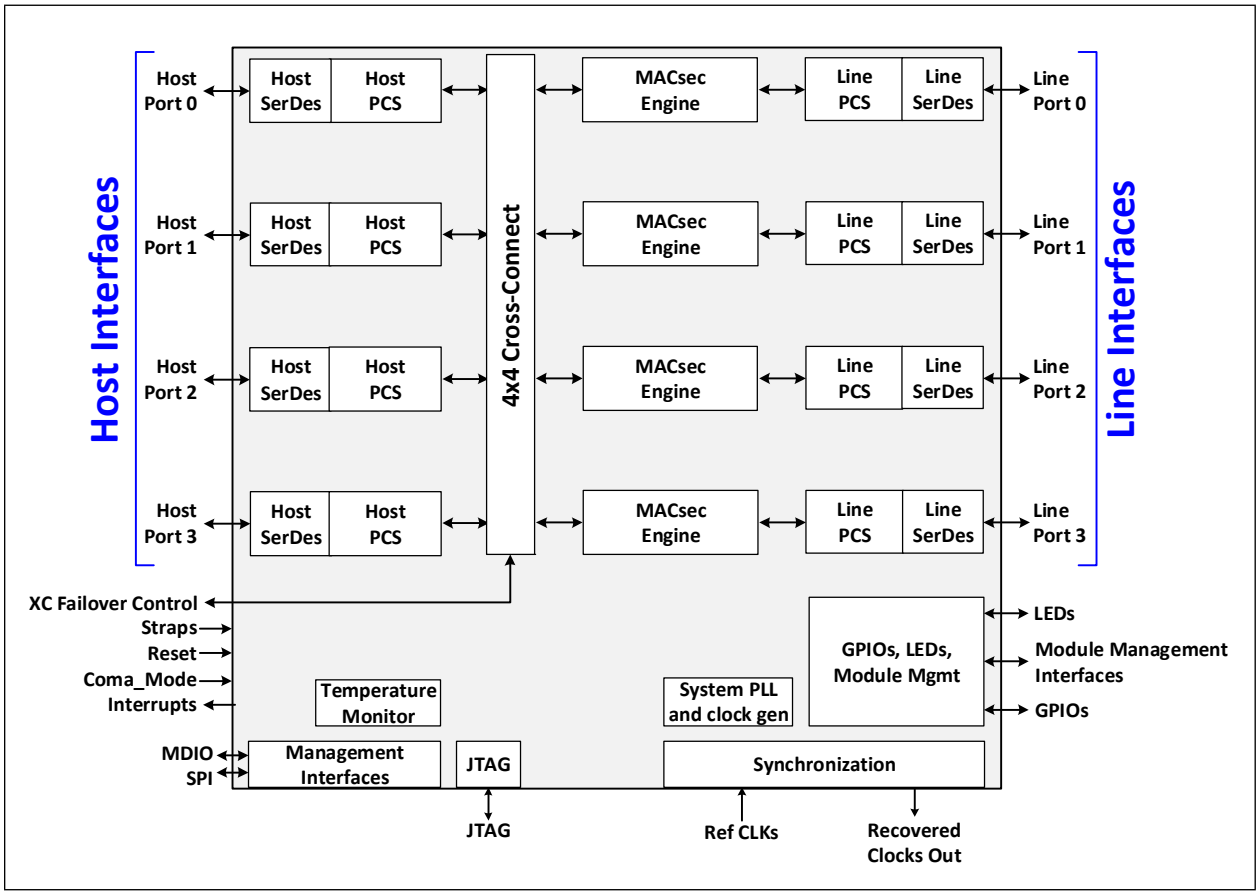
The Microchip LAN8042 is a quad-port 1G/10G/25G serial optical Ethernet PHY transceiver which provides multiple line and host interface options. On the line interfaces, the LAN8042 supports transmission and reception of data over a variety of optical module serial interfaces. These serial interfaces support both optical modules and copper cables. On the host interfaces, the LAN8042 supports transmission and reception of data over a variety of chip-to-chip and backplane serial interfaces. An integrated Cross-Connect function enables any line port to connect to any host port. Host Redundancy options are provided.

LAN8042 also supports Synchronous Ethernet (SyncE) and TSN Frame Preemption. Strong Ethernet security based on IEEE 802.1AE MACsec is supported, including advanced per-flow encryption and VLAN tag in the clear capabilities and both 128-bit and 256-bit AES encryption.

The LAN8042 provides a complete suite of on-chip instrumentation including built-in self-test (BIST) functions, line-side and client-side circuit loopbacks, pattern generation and error detection. It is well-suited for SFP+ and SFP28 optical modules and direct-attach copper (DAC) cabling as well as challenging backplane interface applications.

An internal block diagram of the LAN8042 is shown in Figure 1-1.

FIGURE 1-1: LAN8042 INTERNAL BLOCK DIAGRAM



The following diagrams illustrate three primary target use cases:

- PHY with MACsec
- PHY with Backplane Signal Reconditioning
- PHY with Backplane Signal Reconditioning and System Redundancy

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FIGURE 1-2: PHY WITH MACSEC

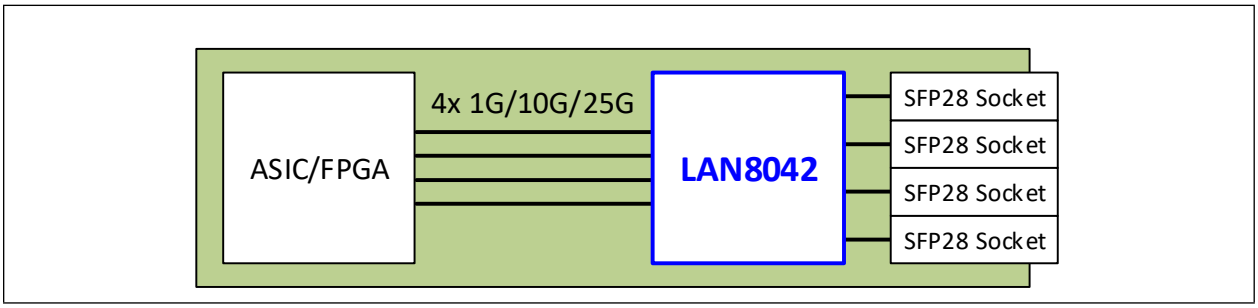

Figure 1-2 details a printed circuit board (PCB) which includes an ASIC/FPGA, LAN8042, and SFP28 sockets. The LAN8042 may be required in such a design for the following reasons:

- Addition of advanced MACsec functions
- Ethernet format conversion such as adding FEC or FEC termination / regeneration
- Standardization on the LAN8042 for all such interfaces

FIGURE 1-3: PHY WITH BACKPLANE SIGNAL RECONDITIONING

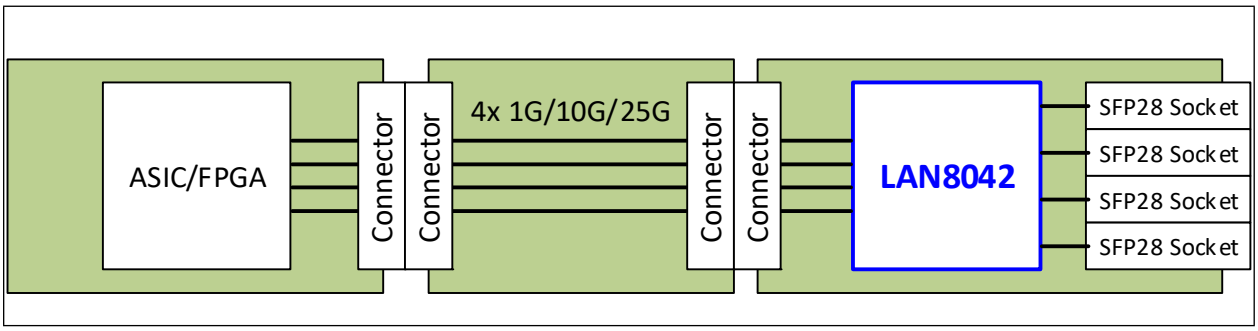

Figure 1-3 details a modular chassis system with the following elements:

- A pluggable switching or processing card containing an ASIC or FPGA with four serial interfaces to the backplane. Each interface is a separate 1G, 10G, or 25G Ethernet port.
- A backplane integrated into the chassis, supporting a variety of pluggable cards.
- A pluggable Optical Media Card with four SFP28 sockets. These sockets support pluggable optical modules such as 1 GbE SFP, 10 GbE SFP+, and 25 GbE SFP28. These sockets also support Direct Attach Copper (DAC) twi-nax cables.

The signals are connected over the backplane using backplane Ethernet formats (1GBASE-KX, 10GBASE-KR, or 25GBASE-KR). The LAN8042 terminates the backplane signals, processes the Ethernet frames, and generates clean signals into the network, meeting optical module or cable specifications (and performs similar functions in the opposite direction).

The LAN8042 can perform a range of processing functions in this role:

- Signal reconditioning across the backplane, both electrical and timing
- Ethernet format conversion functions between the backplane (host) and line interfaces, such as FEC termination / regeneration
- Advanced MACsec functions

Note:	The LAN8042 only supports individual Ethernet ports up to 25 Gbps and does not support multi-lane Ethernet ports such as 40 Gbps or 100 Gbps.

FIGURE 1-4: PHY WITH BACKPLANE SIGNAL RECONDITIONING AND SYSTEM REDUNDANCY

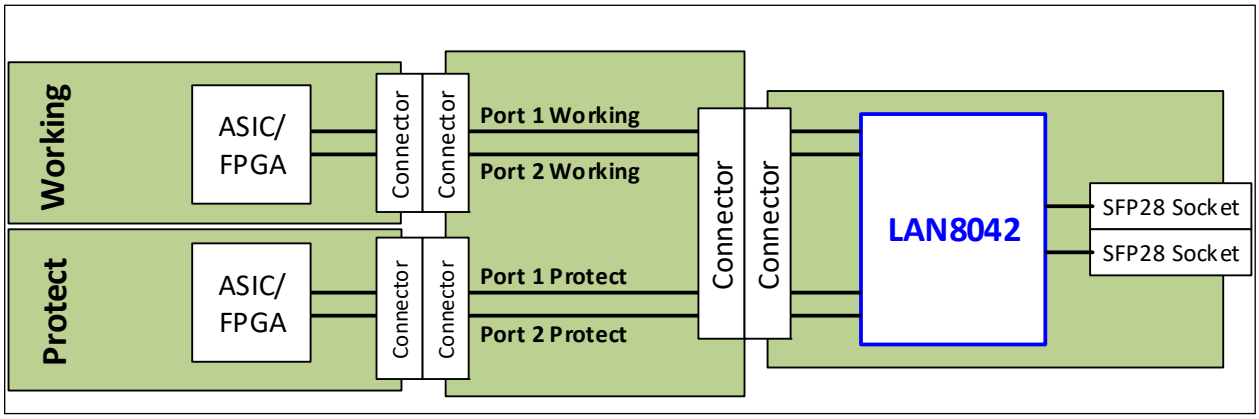

Figure 1-4 details a modular chassis system. It is similar to Figure 1-3 but also has a redundant pair of pluggable switching or processing cards, each containing an ASIC or FPGA and each having two serial interfaces across the backplane to the LAN8042. In this mode, the LAN8042 can only support two optical modules.

The LAN8042 still supports the previously mentioned signal reconditioning, Ethernet format conversion, and MACsec functions. However, in this example the LAN8042 additionally provides fault detection and fail-over capabilities, enabling redundant connections across the backplane.

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2.0 PIN DESCRIPTIONS

This chapter included the following sections:

- Pin Assignments
- PinDescriptions
- Buffer Types

2.1 Pin Assignments

FIGURE 2-1: 256-BGA BALL ASSIGNMENTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	RXIN0N	VDDHS_N	TXOUT0P	VDDHS_N	RXIN1N	VDDHS_N	TXOUT1P	VDDHS_N	RXIN2N	VDDHS_N	TXOUT2P	VDDHS_N	RXIN3N	VDDHS_N	VSS
B	VSS	RXIN0P	VSS	TXOUT0N	VSS	RXIN1P	VSS	TXOUT1N	VSS	RXIN2P	VSS	TXOUT2N	VSS	RXIN3P	VSS	TXOUT3P
C	GPIO32	GPIO33	FAILOVEROUT0 STRAP_RSVD_1	RESET_N	VSS	VDDHH18_N	VDDHH18_N	VDDHS_N	VDDHS_N	VDDHH18_N	VDDHH18_N	VSS	VSS	VSS	VSS	TXOUT3N
D	LREFCKP	LREFCKN	FAILOVERIN0	JTAG_SEL	COMA_MODE	VSS	VSS	VDDHV_N	VDDHV_N	VSS	VSS	VDD	GPIO39	GPIO38	GPIO37	VSS
E	TEST	TMS	TDO	TDI	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	GPIO36	GPIO31	GPIO30	GPIO29
F	TCK	RESERVED	RESERVED	RESERVED	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDO_B	GPIO28	GPIO27	GPIO26	GPIO25
G	RESERVED_L	RESERVED_L	RESERVED_L	RCKOUTB	VDDO_A	VSS	VSS	VSS	VSS	VSS	VSS	VDDO_B	GPIO24	GPIO23	GPIO22	GPIO21
H	SPI_CLIENT_MISO	SPI_CLIENT_MOSI	RCKOUTA	MDIO	VDDO_A	VDDO_A	VSS	VSS	VSS	VSS	VDDO_B	VDDO_B	GPIO20	GPIO19	GPIO18	GPIO17
J	SPI_CLIENT_SCK	SPI_CLIENT_SNN	MDC	GPIO35	VDDO_A	VDDO_A	VSS	VSS	VSS	VSS	VDDO_B	VDDO_B	GPIO16	GPIO15	GPIO14	GPIO13
K	VDDA_PLL	VSSA_PLL	GPIO34	TRST	VDDO_18	VSS	VSS	VSS	VSS	VSS	VSS	VDDO_18	GPIO12	GPIO11	GPIO10	GPIO9
L	RESERVED_18	RESERVED_L	PADDR4	PADDR3	VDDO_18	VDD	VDD	VDD	VDD	VDD	VDD	NC	THERMD_Sn	GPIO8	GPIO7	GPIO6
M	VDDA_SYSPLL	VSSA_SYSPLL	PADDR2	PADDR1	VDD	VDD	VDD	VDD	VDD	VDD	VDD	TESTA	THERMD_Sp	GPIO5	GPIO4	GPIO3
N	SYSREFCKP	SYSREFCKN	PADDR0	FAILOVEROUT1	VDD	VSS	VSS	VDDHV_S	VDDHV_S	VSS	VSS	VDD	THERMD_Fn	GPIO2	GPIO1	GPIO0
P	VSS	VSS	FAILOVERIN1	VDDO_A_MODE	VDDO_B_MODE	VDDHH18_S	VDDHH18_S	VDDHS_S	VDDHS_S	VDDHH18_S	VDDHH18_S	VSS	THERMD_Fp	VSS	VSS	TXIN3P
R	VSS	RXOUT0N	VSS	TXIN0P	VSS	RXOUT1N	VSS	TXIN1P	VSS	RXOUT2N	VSS	TXIN2P	VSS	RXOUT3N	VSS	TXIN3N
T	VSS	RXOUT0P	VDDHS_S	TXIN0N	VDDHS_S	RXOUT1P	VDDHS_S	TXIN1N	VDDHS_S	RXOUT2P	VDDHS_S	TXIN2N	VDDHS_S	RXOUT3P	VDDHS_S	VSS

Top of 256-HFC-BGA Package

Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

TABLE 2-1: 256-BGA BALL ASSIGNMENTS (1-8)

Ball	1	2	3	4	5	6	7	8
A	VSS	RXIN0N	VDDHS_N	TXOUT0P	VDDHS_N	RXIN1N	VDDHS_N	TXOUT1P
B	VSS	RXIN0P	VSS	TXOUT0N	VSS	RXIN1P	VSS	TXOUT1N
C	GPIO32	GPIO33	FAILOVEROUT0/ STRAP_RSVD_1	RESET_N	VSS	VDDH18_N	VDDH18_N	VDDHS_N
D	LREFCKP	LREFCKN	FAILOVERIN0	JTAG_SEL	COMA_MODE	VSS	VSS	VDDHV_N
E	TEST	TMS	TDO	TDI	VDD	VDD	VDD	VDD
F	TCK	RESERVED	RESERVED	RESERVED	VDD	VDD	VDD	VDD
G	RESERVED_L	RESERVED_L	RESERVED_L	RCKOUTB	VDDO_A	VSS	VSS	VSS
H	SPI_CLIENT _MISO	SPI_CLIENT _MOSI	RCKOUTA	MDIO	VDDO_A	VDDO_A	VSS	VSS
J	SPI_CLIENT _SCK	SPI_CLIENT _SSN	MDC	GPIO35	VDDO_A	VDDO_A	VSS	VSS
K	VDDA_PLL	VSSA_PLL	GPIO34	TRST	VDDO_18	VSS	VSS	VSS
L	RESERVED_18	RESERVED_L	PADDR4	PADDR3	VDDO_18	VDD	VDD	VDD
M	VDDA_SYSPLL	VSSA_SYSPLL	PADDR2	PADDR1	VDD	VDD	VDD	VDD
N	SYSREFCKP	SYSREFCKN	PADDR0	FAILOVEROUT1	VDD	VSS	VSS	VDDHV_S
P	VSS	VSS	FAILOVERIN1	VDDO_A_MODE	VDDO_B_MODE	VDDH18_S	VDDH18_S	VDDHS_S
R	VSS	RXOUT0N	VSS	TXIN0P	VSS	RXOUT1N	VSS	TXIN1P
T	VSS	RXOUT0P	VDDHS_S	TXIN0N	VDDHS_S	RXOUT1P	VDDHS_S	TXIN1N

TABLE 2-2: 256-BGA BALL ASSIGNMENTS (9-16)

Ball	9	10	11	12	13	14	15	16
A	VDDHS_N	RXIN2N	VDDHS_N	TXOUT2P	VDDHS_N	RXIN3N	VDDHS_N	VSS
B	VSS	RXIN2P	VSS	TXOUT2N	VSS	RXIN3P	VSS	TXOUT3P
C	VDDHS_N	VDDH18_N	VDDH18_N	VSS	VSS	VSS	VSS	TXOUT3N
D	VDDHV_N	VSS	VSS	VDD	GPIO39	GPIO38	GPIO37	VSS
E	VDD	VDD	VDD	VDD	GPIO36	GPIO31	GPIO30	GPIO29
F	VDD	VDD	VDD	VDDO_B	GPIO28	GPIO27	GPIO26	GPIO25
G	VSS	VSS	VSS	VDDO_B	GPIO24	GPIO23	GPIO22	GPIO21
H	VSS	VSS	VDDO_B	VDDO_B	GPIO20	GPIO19	GPIO18	GPIO17
J	VSS	VSS	VDDO_B	VDDO_B	GPIO16	GPIO15	GPIO14	GPIO13
K	VSS	VSS	VSS	VDDO_18	GPIO12	GPIO11	GPIO10	GPIO9
L	VDD	VDD	VDD	RESERVED	THERMD_Sn	GPIO8	GPIO7	GPIO6
M	VDD	VDD	VDD	TESTA	THERMD_Sp	GPIO5	GPIO4	GPIO3
N	VDDHV_S	VSS	VSS	VDD	THERMD_Fn	GPIO2	GPIO1	GPIO0
P	VDDHS_S	VDDH18_S	VDDH18_S	VSS	THERMD_Fp	VSS	VSS	TXIN3P
R	VSS	RXOUT2N	VSS	TXIN2P	VSS	RXOUT3N	VSS	TXIN3N
T	VDDHS_S	RXOUT2P	VDDHS_S	TXIN2N	VDDHS_S	RXOUT3P	VDDHS_S	VSS

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2.2 Pin Descriptions

This section contains descriptions of the various LAN8042 pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signal. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

TABLE 2-3: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Ethernet (Line Interface)			
Ethernet Line Port 0 Input Data Negative	**RXIN0N**	AI	Negative input signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 0 Input Data Positive	**RXIN0P**	AI	Positive input signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 1 Input Data Negative	**RXIN1N**	AI	Negative input signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 1 Input Data Positive	**RXIN1P**	AI	Positive input signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 2 Input Data Negative	**RXIN2N**	AI	Negative input signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 2 Input Data Positive	**RXIN2P**	AI	Positive input signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Ethernet Line Port 3 Input Data Negative	**RXIN3N**	AI	Negative input signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 3 Input Data Positive	**RXIN3P**	AI	Positive input signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 0 Output Data Negative	**TXOUT0N**	AO	Negative output signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 0 Output Data Positive	**TXOUT0P**	AO	Positive output signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 1 Output Data Negative	**TXOUT1N**	AO	Negative output signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 1 Output Data Positive	**TXOUT1P**	AO	Positive output signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 2 Output Data Negative	**TXOUT2N**	AO	Negative output signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 2 Output Data Positive	**TXOUT2P**	AO	Positive output signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.

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TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Ethernet Line Port 3 Output Data Negative	**TXOUT3N**	AO	Negative output signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 3 Output Data Positive	**TXOUT3P**	AO	Positive output signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet (Host Interface)			
Ethernet Host Port 0 Input Data Negative	**TXIN0N**	AI	Negative input signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 0 Input Data Positive	**TXIN0P**	AI	Positive input signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 1 Input Data Negative	**TXIN1N**	AI	Negative input signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 1 Input Data Positive	**TXIN1P**	AI	Positive input signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 2 Input Data Negative	**TXIN2N**	AI	Negative input signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 2 Input Data Positive	**TXIN2P**	AI	Positive input signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 3 Input Data Negative	**TXIN3N**	AI	Negative input signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Ethernet Host Port 3 Input Data Positive	**TXIN3P**	AI	Positive input signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 0 Output Data Negative	**RXOUT0N**	AO	Negative output signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required.
Ethernet Host Port 0 Output Data Positive	**RXOUT0P**	AO	Positive output signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 1 Output Data Negative	**RXOUT1N**	AO	Negative output signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required.
Ethernet Host Port 1 Output Data Positive	**RXOUT1P**	AO	Positive output signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 2 Output Data Negative	**RXOUT2N**	AO	Negative output signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required.
Ethernet Host Port 2 Output Data Positive	**RXOUT2P**	AO	Positive output signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required.
Ethernet Host Port 3 Output Data Negative	**RXOUT3N**	AO	Negative output signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required.
Ethernet Host Port 3 Output Data Positive	**RXOUT3P**	AO	Positive output signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required.
Reference Clocks			
Host Port / System Reference Clock Input Negative	**SYSREFCKN**	CLOCK	Negative input signal of differential pair. An external AC coupling capacitor is required. **Note:** Internal 100 Ohms (nominal) differential input termination.

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TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Host Port / System Reference Clock Input Positive	**SYSREFCKP**	CLOCK	Positive input signal of differential pair. An external AC coupling capacitor is required. **Note:** Internal 100 Ohms (nominal) differential input termination.
Line Port Reference Clock Input Negative	**LREFCKN**	CLOCK	Negative input signal of differential pair. An external AC coupling capacitor is required. **Note:** Internal 100 Ohms (nominal) differential input termination.
Line Port Reference Clock Input Positive	**LREFCKP**	CLOCK	Positive input signal of differential pair. An external AC coupling capacitor is required. **Note:** Internal 100 Ohms (nominal) differential input termination.
Recovered Output Clocks			
Recovered Clock Output A	**RCKOUTA**	LVCMOS Out (4 ma)	Output clock signal. Selectable from: • Any Host Port recovered clock • Any Line Port recovered clock • System PLL
Recovered Clock Output B	**RCKOUTB**	LVCMOS Out (4 ma)	Output clock signal. Selectable from: • Any Host Port recovered clock • Any Line Port recovered clock • System PLL
Cross Connect Failover Control			
System Port 0 Failover Control In	**FAILOVERIN0**	LVCMOS In (4 ma)	Cross Connect Failover indication. Indicates to the device that a Working / Protect pair failover was performed by the host system.
System Port 0 Failover Control Out	**FAILOVEROUT0**	LVCMOS Out	Cross Connect Failover indication. Indicates to the host system that a Working / Protect pair failover was performed by the device.
System Port 1 Failover Control In	**FAILOVERIN1**	LVCMOS In	Cross Connect Failover indication. Indicates to the device that a Working / Protect pair failover was performed by the host system.
System Port 1 Failover Control Out	**FAILOVEROUT1**	LVCMOS Out (4 ma)	Cross Connect Failover indication. Indicates to the host system that a Working / Protect pair failover was performed by the device.
PHY Management Interface			
PHY Management Interface Clock	**MDC**	LVCMOS In	PHY Management clock input
PHY Management Interface Data	**MDIO**	LVCMOS I/O (4 ma)	PHY Management data interface
PHY Base Address [4:0]	**PADDR[4:0]**	LVCMOS In	PHY MDIO Management Base Address [4:0] Any tie high or pull-up must be to **VDDO_A**.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
PHY SPI Client Clock	**SPI_CLIENT_SCK**	LVCMOS In	Client SPI can be used in place of or fully in parallel with **MDIO/MDC**.
PHY SPI Client Data Out	**SPI_CLIENT_MISO**	LVCMOS Out (4ma)	Client SPI can be used in place of or fully in parallel with **MDIO/MDC**.
PHY SPI Client Data In	**SPI_CLIENT_MOSI**	LVCMOS In	Client SPI can be used in place of or fully in parallel with **MDIO/MDC**.
PHY SPI Client Chip Select	**SPI_CLIENT_SSN**	LVCMOS In	Client SPI can be used in place of or fully in parallel with **MDIO/MDC**.
Miscellaneous			
GPIOs [39:0]	**GPIO[39:0]**	LVCMOS I/O (4 ma) (PU)	General Purpose Inputs/Outputs 39-0. Open-Drain/Push-Pull, configurable polarity. Many GPIOs are shared with other functions. Alternate function selection is configured via GPIO registers. Refer to Table 2-4 for additional details. **Note:** GPIO pins should not be allowed to float. Internal pull-ups are enabled by default.
System Reset	**RESET_N**	LVCMOS In (Schmitt)	Active low chip reset. At power-up, **RESET_N** must not be deasserted until all power and clocks have been stable for the specified minimum duration. Configuration strap values are latched at the deassertion (rising edge) of **RESET_N**.
Coma Mode Control	**COMA_MODE**	LVCMOS In	Drive high to activate Coma Mode. After all ports are configured, drive low to enable normal operation. Hold low to disable this feature.
Test Mode	**TEST**	LVCMOS In (PD) (Schmitt)	Enables test mode. For proper operation, this pin should be tied low. 0 = Functional Mode 1 = Test Mode
Thermal Diode Force Positive	**THERMD_Fp**	AI	Thermal Diode 1.5mA current source.
Thermal Diode Force Negative	**THERMD_Fn**	AI	Thermal Diode current ground.
Thermal Diode Sense Positive	**THERMD_Sp**	AO	Thermal Diode sense positive. **Note:** For measurement only; never drive current on this signal.
Thermal Diode Sense Negative	**THERMD_Sn**	AO	Thermal Diode sense negative. **Note:** For measurement only; never drive current on this signal.
Reserved	**TESTA**	LVCMOS I/O (PD) (Schmitt)	For proper operation, this pin should be tied low.

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TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Reserved	**RESERVED**	-	These pins are reserved for future use and should not be used.
Reserved	**RESERVED_L**	-	For proper operation, these pins should be tied low to VSS.
Reserved	**RESERVED_18**	-	For proper operation, this pin should be tied high to VDDO_18.
JTAG			
JTAG Test Data Input	**TDI**	LVCMOS In (Schmitt)	JTAG (IEEE 1149.1) data input. **Note:** When not used, tie this pin high.
JTAG Test Data Output	**TDO**	LVCMOS Out (8 ma)	JTAG (IEEE 1149.1) test data output.
JTAG Test Reset	**TRST**	LVCMOS In (PD) (Schmitt)	JTAG (IEEE 1149.1) test reset. Resets the TAP controller's state machine. For proper operation, this pin should be tied low.
JTAG Test Clock	**TCK**	LVCMOS In (Schmitt)	JTAG (IEEE 1149.1) test clock. **Note:** When not used, tie this pin low.
JTAG Test Mode Select	**TMS**	LVCMOS In (Schmitt)	JTAG (IEEE 1149.1) test mode select. **Note:** When not used, tie this pin low.
JTAG Select Input	**JTAG_SEL**	LVCMOS In (PD) (Schmitt)	For proper operation, this pin should be tied low.
Power			
+0.9V Digital Core Logic Power Supply Input	**VDD**	P	+0.9V digital core logic power supply input.
+1.8V SerDes Power Supply Input (North Side)	**VDDH18_N**	P	+1.8V SerDes power supply input. (North Side)
+1.0V SerDes Analog TX/RX Power Supply Input (North Side)	**VDDHS_N**	P	+1.0V SerDes analog TX/RX power supply input. (North Side)
+1.0V SerDes Analog VCO Power Supply Input (North Side)	**VDDHV_N**	P	+1.0V SerDes analog Voltage Controlled Oscillator (VCO) power supply input. (North Side)

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
+1.8V SerDes Power Supply Input (South Side)	**VDDH18_S**	P	+1.8V SerDes power supply input. (South Side)
+1.0V SerDes Analog TX/RX Power Supply Input (South Side)	**VDDHS_S**	P	+1.0V SerDes analog TX/RX power supply input. (South Side)
+1.0V SerDes Analog VCO Power Supply Input (South Side)	**VDDHV_S**	P	+1.0V SerDes analog Voltage Controlled Oscillator (VCO) power supply input. (South Side)
+1.8V/+3.3V LVCMOS I/O Group A Power Supply Input	**VDDO_A**	P	+1.8V/+3.3V LVCMOS I/O Group A power supply input.
+1.8V/+3.3V LVCMOS I/O Group B Power Supply Input	**VDDO_B**	P	+1.8V/+3.3V LVCMOS I/O Group B power supply input.
+1.8V LVCMOS I/O Group Fixed Voltage Power Supply Input	**VDDO_18**	P	+1.8V LVCMOS I/O group fixed voltage power supply input.
+1.8V PLL Analog Power Supply Input	**VDDA_PLL**	P	+1.8V PLL Analog power supply input.
Ground	**VSS**	P	Common ground.
PLL Analog Ground	**VSSA_PLL**	P	PLL analog ground.
+1.8V System PLL Analog Power Supply Input	**VDDA_SYSPLL**	P	PLL analog system.
System PLL Analog Ground	**VSSA_SYSPLL**	P	PLL analog system.
Power Supply Group A Voltage Mode	**VDDO_A_MODE**	LVCMOS In	Used to set the I/O voltage of group A signals. 1 = 3.3V 0 = 1.8V **Note:** If tied high or pulled up, these signals must be connected to 1.8V.

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TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Power Supply Group B Voltage Mode	**VDDO_B_MODE**	LVCMOS In	Used to set the I/O voltage of group B signals. 1 = 3.3V 0 = 1.8V **Note:** If tied high or pulled up, these signals must be connected to 1.8V.

Table 2-4 details the GPIO alternate functions and indicates the default function of each pin (GPIO or alternate).

Note: All GPIOs have an internal pull-up enabled by default. This pull-up can be disabled if not desired.

TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
General GPIOs				
GPIO32 (Default)	-	-	LVCMOS I/O (4 ma) (PU)	General Purpose Input/Output. Configurable Open-Drain/Push-Pull, configurable polarity. **Note:** GPIO pins should not be allowed to float. Internal pull-ups are enabled by default.
GPIO33 (Default)	-	-	LVCMOS I/O (4 ma) (PU)	General Purpose Input/Output. Configurable Open-Drain/Push-Pull, configurable polarity. **Note:** GPIO pins should not be allowed to float. Internal pull-ups are enabled by default.
PHY Management Interface Interrupt Outputs				
GPIO34 (Default)	PHY Interrupt A	**INTR_A**	LVCMOS Out (4 ma)	Programmable PHY interrupt A output. Open-drain, configurable polarity (typically active low).
GPIO35 (Default)	PHY Interrupt B	**INTR_B**	LVCMOS Out (4 ma)	Programmable PHY interrupt B output. Open-drain, configurable polarity (typically active low).

TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE (CONTINUED)

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
Fiber Module Management Interface				
GPIO0 (Default)	Port 0 Module Rate Select 0	**PORT0_RATESEL0**	LVCMOS Out (4 ma)	Port 0 rate select 0. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 0 Module Power Down	**PORT0_PDOWN**	LVCMOS Out (4 ma)	Port 0 power down. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 0 Module Reset	**PORT0_RST**	LVCMOS Out (4 ma)	Port 0 reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
GPIO1 (Default)	Port 0 Module Absent	**PORT0_MOD_ABS**	LVCMOS In (PU)	Port 0 module absent This input indicates if the optical module is attached. 0 = module present
GPIO2 (Default)	Port 0 Module TWI Host Clock	**PORT0_TWI_SCL**	LVCMOS I/O (4 ma) (PU)	Port 0 module management interface clock. Open-drain.
GPIO3 (Default)	Port 0 Module TWI Host Data	**PORT0_TWI_SDA**	LVCMOS I/O (4 ma) (PU)	Port 0 module management interface data. Open-drain.
GPIO4 (Default)	Port 0 Module Transmitter Disable	**PORT0_TX_DIS**	LVCMOS Out (4 ma)	Port 0 module transmitter disable / low power mode. Open drain, configurable polarity (typically high). This output is used to shut down the transmitter optical input or place it in a low power mode.
GPIO5 (Default)	Port 0 Module Transmitter Fault	**PORT0_TX_FAULT**	LVCMOS In (PU)	Port 0 TX fault. This GPIO input indicates a laser fault. 1 = fault

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TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE (CONTINUED)

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
GPIO6 (Default)	Port 0 Module Receiver Loss of Signal	**PORT0_RXLOS**	LVCMOS In (PU)	Port 0 RX loss of signal. Configurable polarity. This input indicates insufficient optical power for reliable signal reception. The polarity depends on the optical module type.
	Port 0 Module Interrupt	**PORT0_INTL**	LVCMOS In (PU)	Port 0 module interrupt. Typically active low, this input indicates an interrupt request from the module 0 = interrupt
GPIO8 (Default)	Port 1 Module Rate Select 0 / Power Down / Reset	**PORT1_RATESEL0**	LVCMOS Out (4 ma)	Port 1 rate select 0 / power down / reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 1 Module Power Down	**PORT1_PDOWN**	LVCMOS Out (4 ma)	Port 1 power down. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 1 Module Reset	**PORT1_RST**	LVCMOS Out (4 ma)	Port 1 reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
GPIO9 (Default)	Port 1 Module Absent	**PORT1_MOD_ABS**	LVCMOS In (PU)	Port 1 module absent This input indicates if the optical module is attached. 0 = module present
GPIO10 (Default)	Port 1 Module TWI Host Clock	**PORT1_TWI_SCL**	LVCMOS I/O (4 ma) (PU)	Port 1 module management interface clock. Open-drain.
GPIO11 (Default)	Port 1 Module TWI Host Data	**PORT1_TWI_SDA**	LVCMOS I/O (4 ma) (PU)	Port 1 module management interface data. Open-drain.
GPIO12 (Default)	Port 1 Module Transmitter Disable	**PORT1_TX_DIS**	LVCMOS Out (4 ma)	Port 1 module transmitter disable / low power mode. Open drain, configurable polarity (typically high). This output is used to shut down the transmitter optical input or place it in a low power mode.

TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE (CONTINUED)

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
GPIO13 (Default)	Port 1 Module Transmitter Fault	PORT1_TX_FAULT	LVCMOS In (PU)	Port 1 TX fault. This input indicates a laser fault. 1 = fault
GPIO14 (Default)	Port 1 Module Receiver Loss of Signal	PORT1_RXLOS	LVCMOS In (PU)	Port 1 RX loss of signal. Configurable polarity. This input indicates insufficient optical power for reliable signal reception. The polarity depends on the optical module type.
	Port 1 Module Interrupt	PORT1_INTL	LVCMOS In (PU)	Port 1 module interrupt. Typically active low, this input indicates an interrupt request from the module 0 = interrupt
GPIO16 (Default)	Port 2 Module Rate Select 0 / Power Down / Reset	PORT2_RATESEL0	LVCMOS Out (4 ma)	Port 2 rate select 0 / power down / reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 2 Module Power Down	PORT2_PDOWN	LVCMOS Out (4 ma)	Port 2 power down. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 2 Module Reset	PORT2_RST	LVCMOS Out (4 ma)	Port 2 reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
GPIO17 (Default)	Port 2 Module Absent	PORT2_MOD_ABS	LVCMOS In (PU)	Port 2 module absent This GPIO input indicates if the optical module is attached. 0 = module present
GPIO18 (Default)	Port 2 Module TWI Host Clock	PORT2_TWI_SCL	LVCMOS I/O (4 ma) (PU)	Port 2 module management interface clock. Open-drain.
GPIO19 (Default)	Port 2 Module TWI Host Data	PORT2_TWI_SDA	LVCMOS I/O (4 ma) (PU)	Port 2 module management interface data. Open-drain.

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TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE (CONTINUED)

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
GPIO20 (Default)	Port 2 Module Transmitter Disable	**PORT2_TX_DIS**	LVCMOS Out (4 ma)	Port 2 module transmitter disable / low power mode. Open drain, configurable polarity (typically high). This output is used to shut down the transmitter optical input or place it in a low power mode.
GPIO21 (Default)	Port 2 Module Transmitter Fault	**PORT2_TX_FAULT**	LVCMOS In (PU)	Port 2 TX fault. This input indicates a laser fault. 1 = fault
GPIO22 (Default)	Port 2 Module Receiver Loss of Signal	**PORT2_RXLOS**	LVCMOS In (PU)	Port 2 RX loss of signal. Configurable polarity. This input indicates insufficient optical power for reliable signal reception. The polarity depends on the optical module type.
	Port 2 Module Interrupt	**PORT2_INTL**	LVCMOS In (PU)	Port 2 module interrupt. Typically active low, this input indicates an interrupt request from the module 0 = interrupt
GPIO24 (Default)	Port 3 Module Rate Select 0 / Power Down / Reset	**PORT3_RATESEL0**	LVCMOS Out (4 ma)	Port 1 rate select 0 / power down / reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 3 Module Power Down	**PORT3_PDOWN**	LVCMOS Out (4 ma)	Port 3 power down. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 3 Module Reset	**PORT3_RST**	LVCMOS Out (4 ma)	Port 3 reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
GPIO25 (Default)	Port 3 Module Absent	**PORT3_MOD_ABS**	LVCMOS In (PU)	Port 3 module absent This input indicates if the optical module is attached. 0 = module present
GPIO26 (Default)	Port 3 Module TWI Host Clock	**PORT3_TWI_SCL**	LVCMOS I/O (4 ma) (PU)	Port 3 module management interface clock. Open-drain.

TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE (CONTINUED)

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
GPIO27 (Default)	Port 3 Module TWI Host Data	PORT3_TWI_SDA	LVCMOS I/O (4 ma) (PU)	Port 3 module management interface data. Open-drain.
GPIO28 (Default)	Port 3 Module Transmitter Disable	PORT3_TX_DIS	LVCMOS Out (4 ma)	Port 3 module transmitter disable / low power mode. Open drain, configurable polarity (typically high). This output is used to shut down the transmitter optical input or place it in a low power mode.
GPIO29 (Default)	Port 3 Module Transmitter Fault	PORT3_TX_FAULT	LVCMOS In (PU)	Port 3 TX fault. This input indicates a laser fault. 1 = fault
GPIO30 (Default)	Port 3 Module Receiver Loss of Signal	PORT3_RXLOS	LVCMOS In (PU)	Port 3 RX loss of signal. Configurable polarity. This input indicates insufficient optical power for reliable signal reception. The polarity depends on the optical module type.
	Port 3 Module Interrupt	PORT3_INTL	LVCMOS In (PU)	Port 3 module interrupt. Typically active low, this input indicates an interrupt request from the module 0 = interrupt
LEDs				
GPIO7 (Default)	Port 0 Link Up LED	PORT0_LINK_LED	LVCMOS Out (4 ma)	Line Port 0 Link LED. This signal displays Port 0's Line Side Link Status. Open-drain, active low.
GPIO36 (Default)	Port 0 Activity LED	PORT0_ACTIVITY_LED	LVCMOS Out (4 ma)	Line Port 0 Activity LED. This signal displays Port 0's Line Side Combined TX/RX Activity. Open-drain, active low.
GPIO15 (Default)	Port 1 Link Up LED	PORT1_LINK_LED	LVCMOS Out (4 ma)	Line Port 1 Link LED. This signal displays Port 1's Line Side Link Status. Open-drain, active low.
GPIO37 (Default)	Port 1 Activity LED	PORT1_ACTIVITY_LED	LVCMOS Out (4 ma)	Line Port 1 Activity LED. This signal displays Port 1's Line Side Combined TX/RX Activity. Open-drain, active low.

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TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE (CONTINUED)

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
GPIO23 (Default)	Port 2 Link Up LED	PORT2_LINK_LED	LVCMOS Out (4 ma)	Line Port 2 Link LED. This signal displays Port 2's Line Side Link Status. Open-drain, active low.
GPIO38 (Default)	Port 2 Activity LED	PORT2_ACTIVITY_LED	LVCMOS Out (4 ma)	Line Port 2 Activity LED. This signal displays Port 2's Line Side Combined TX/RX Activity. Open-drain, active low.
GPIO31 (Default)	Port 3 Link Up LED	PORT3_LINK_LED	LVCMOS Out (4 ma)	Line Port 3 Link LED. This signal displays Port 3's Line Side Link Status. Open-drain, active low.
GPIO39 (Default)	Port 3 Activity LED	PORT3_ACTIVITY_LED	LVCMOS Out (4 ma)	Line Port 3 Activity LED. This signal displays Port 3's Line Side Combined TX/RX Activity. Open-drain, active low.

TABLE 2-5: STRAP INPUTS

Name	Symbol	Buffer Type	Description
Strap Pins			
Reserved Strap 1	STRAP_RSVD_1	LVCMOS In (PD)	Reserved Strap. **Note:** Any tie high or pull-up must be to **VDDO_A.**

2.3 Buffer Types

TABLE 2-6: BUFFER TYPE DESCRIPTIONS

BUFFER	DESCRIPTION
AI	Analog input
AO	Analog output
CLOCK	Differential clock input
GND	Ground pin
LVCMOS In	LVCMOS input pin
LVCMOS I/O	LVCMOS I/O pin
LVCMOS Out	LVCMOS output pin
LVDS In	LVDS input pin
P	Power pin
PD	Internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
PU	Internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.

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3.0 FUNCTIONAL DESCRIPTIONS

The LAN8042 device is a quad-port 1G/10G/25G serial optical Ethernet PHY transceiver which provides multiple Line Port and Host Port options. On the line ports, the LAN8042 supports transmission and reception of data over a variety of serial interfaces. These serial interfaces support both optical modules and copper cables. On the Host Ports, the LAN8042 supports transmission and reception of data over a variety of chip-to-chip and backplane serial interfaces. An integrated Cross-Connect function enables any line port to connect to any host port. Host Redundancy options are provided.

This section includes a functional block diagram, information on the operating modes, and descriptions of the major functional blocks of the LAN8042 device.

3.1 IEEE 802.3 Alignment

The LAN8042 device offers IEEE 802.3-2018 compliance, and is fully compatible with the following interfaces:

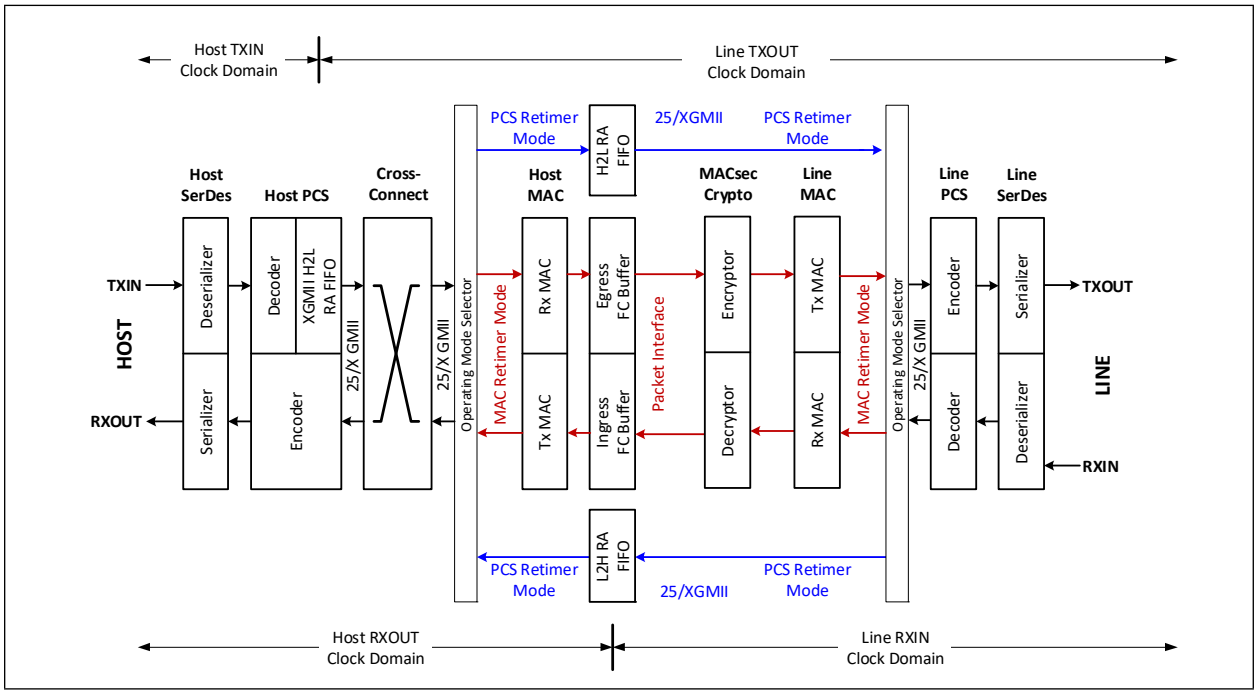
- 25GBASE-CR
- 25GBASE-CR-S
- 25GBASE-KR
- 25GBASE-KR-S
- 25GBASE-SR
- 25GBASE-LR
- 25GBASE-ER
- 25GBASE -AOC
- 10GBASE-KR
- 10GBASE-SR
- 10GBASE-LR
- 10GBASE-ER
- 10GBASE-AOC
- 10GBASE-DAC
- 1000BASE-KX
- 1000BASE-SX
- 1000BASE-LX

3.2 Data Path Overview

The LAN8042 device supports four Host ports and four Line ports, with a Cross-Connect to interconnect any Host with any Line (Host Redundancy options are covered later). Figure 3-1 illustrates the data path where one Line is connected to one Host, and includes the following functions:

- Fully configurable Ethernet PHY on Host and Line
  - Host and Line must be of the same speed (for example, 25G Ethernet), but can be of different formats (for example, KR FEC on Host and RS FEC on Line).
  - Host and Line may be fully synchronous or may have PPM clock differences handled by rate adaptation.
- Two Operating modes
  - PCS Retimer, which is a traditional PHY
  - MAC Retimer, which is an advanced mode with PHYs and MACs and optional MACsec encryption
- Synchronous Ethernet support
- TSN Frame Preemption support

FIGURE 3-1: LAN8042 DATA PATH



3.2.1 OPERATING MODES

Two basic data path modes are supported, which are selected by the Operating Mode Selectors:

- Ethernet PHY, PCS Retimer: This is a traditional PHY (PCS + SerDes) on both Host and Line. MAC and MACsec functions are not available.
- Ethernet PHY, MAC Retimer: This is the fully featured PHY with MACsec support and uses all data path blocks. Of special note, in this mode, there is both a MAC and a PHY on both the Host and Line ports. The MAC is required for MACsec operation, but is available for use without MACsec.

3.2.1.1 Ethernet PHY, PCS Retimer Mode

This mode is essentially a standard Ethernet PHY.

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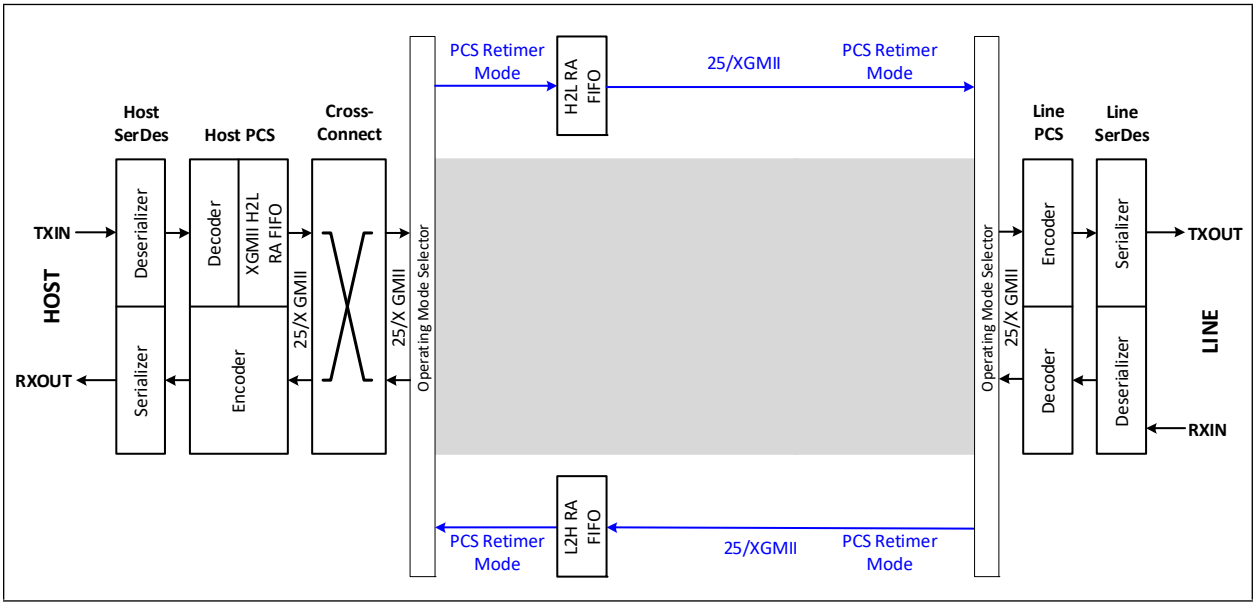
FIGURE 3-2: ETHERNET PHY, PCS RETIMER MODE DATA PATH



Data is received by the SerDes on one side (Host or Line), deserialized, processed by core logic and passed to the opposite side (Line or Host) SerDes. There, the data is serialized and transmitted.

In this mode, the transmit (serializer) clock is required to be the same nominal frequency as the clock recovered from the opposite receiver. PPM clock differences are allowed and are handled by rate adaptation logic (inserting or deleting idles to adapt to the slightly different frequency) associated with the XGMII H2L RA FIFO and the L2H RA FIFO. Each port is retimed to a port clock based on the System reference clock.

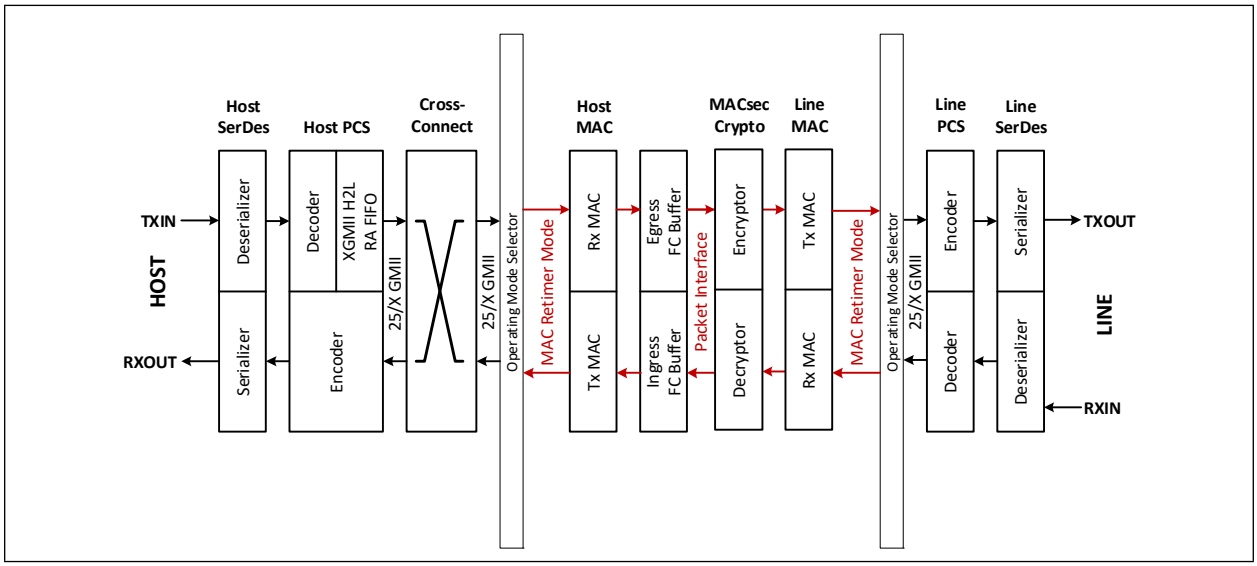
Note: Even though the nominal frequency of Line and Host must both be the same, it is possible to use different Ethernet PHY modes. So for example, the Host might be 25GBASE-KR with KR FEC and the Line might be 25GBASE-LR with RS FEC.

Synchronous Ethernet requires external timing functions, as described in Section 3.8.3.

3.2.1.2 Ethernet PHY, MAC Retimer Mode

This mode is an advanced Ethernet PHY MACs, supporting MACsec. Due to MACsec, this mode requires a MAC on each of the Host and Line Ports.

FIGURE 3-3: ETHERNET PHY, MAC RETIMER MODE DATA PATH



MAC Retimer mode is similar to the Ethernet PHY, PCS Retimer mode in that:

- Data is received by the SerDes on one side (Host or Line), deserialized, processed by core logic and passed to the opposite side (Line or Host) SerDes where the data is serialized and transmitted.
- The transmit (serializer) clock is required to be the same nominal frequency as the clock recovered from the opposite receiver. PPM clock differences are supported. Each port is retimed to a port clock based on the System reference clock.
- Synchronous Ethernet is supported.

The MACsec processing and presence of MACs are unique to MAC Retimer mode. Per IEEE standards, MACsec processing sits “behind” the Line MAC (at a higher Ethernet layer). The LAN8042 Line MAC communicates with the Line Link Partner's MAC and provides MAC-layer functions such as PAUSE, Line Fault Signaling (LFS), Frame preemption and port statistics.

The LAN8042 Host MAC communicates with the Host’s MAC.

MAC Retimer mode also supports use of the LAN8042 MACs without MACsec to provide MAC functions related to IFG, preamble and Pause.

3.2.2 MACSEC

MACsec exists as a higher-layer processor function.

- MACsec may be enabled toward the Line only in MAC Retimer operating mode, at any operating speed. Note that MACsec requires the use of MACs.

3.2.3 SERDES

The SD25G SerDes supports Ethernet 1 Gbps, 10 Gbps, and 25 Gbps operation by running at 1.25G baud, 10.3125G baud, and 25.78125G baud.

3.2.3.1 SD25G SerDes

The SD25G SerDes provides the following operational capabilities:

- RX 5-tap Decision Feedback Equalizer (DFE) to reduce Inter Symbol Interference (ISI). The DFE can operate adaptively or statically.
- RX Continuous Time Linear Equalizer (CTLE) for high-pass filtering.
- RX variable gain control
- RX Loss of Signal and Loss of Lock
- TX 3-tap Feed Forward Equalizer (FFE) for TX de-emphasis to compensate for frequency-dependent channel

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loss.

- TX output amplitude control

In addition, the SD25G provides the following support capabilities:

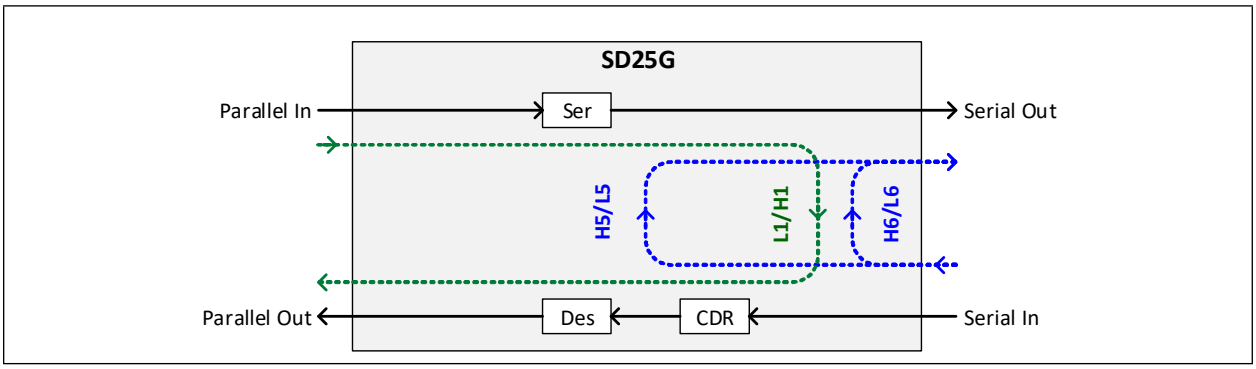
- RX Eye Monitor
- Loopbacks in multiple locations (see below and Section 3.2.10, "Loopbacks and Packet BIST").
- PRBS generator and checker, supporting PRBS-7, 9, 11, 15, 23 and 31. User-defined patterns are also supported.
- Polarity inversion control

Each CMU receives SYSREFCKP/N as input, and generates the TX_PMA_CK and RX_PMA_CK used by the data path. See Section 3.8.

The SD25G supports the following loopbacks

- LAN8042 H1/L1 Serial Out to Serial In Loopback
  In this loopback the data is internally looped at the SD25G serial interface back toward the LAN8042 core. The internal pma_rx_ck will be synchronous to the pma_tx_ck.
  This loopback is enabled by setting LN_CFG_TX2RX_LP_EN=1 and LN_CFG_TXLB_EN=1.
- LAN8042 H5/L5 Serial In to Serial Out Loopback, post-CDR
  In this loopback the data is internally looped back toward the serial interface. The data is retimed by the CDR but the link partner will still receive the looped data using the same timing that the link partner used to generate the data.
  This loopback is enabled by setting LN_CFG_RX2TX_LP_EN=1, LN_CFG_RXLB_EN=1, and LN_CFG_C-DRCK_EN=1
- LAN8042 H6/L6 Serial In to Serial Out Loopback
  In this loopback the data is internally looped back toward the serial interface without re-timing. The link partner will received the looped data using the same timing that the link partner used to generate the data.
  This loopback is enabled by setting LN_CFG_RX2TX_LP_EN=1, LN_CFG_RXLB_EN=1, and LN_CFG_C-DRCK_EN=0.

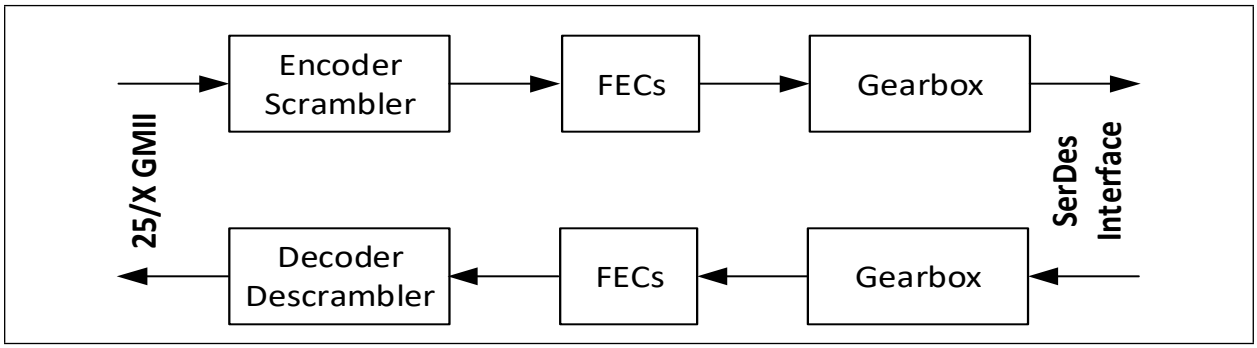
FIGURE 3-4: SD25G LOOPBACKS



3.2.4 PCS25G

The PCS25G block supports both10G and 25G port speeds.

FIGURE 3-5: PCS25G BLOCK DIAGRAM



The PCS25G supports the following features and capabilities:

- 25GBASE-R PCS per IEEE 802.3 Clause 107, which connects to an SFP28 / QSFP28 module (which can be optical or direct attach cable). PCS25G also supports Clause 111 25GBASE-KR/KR-S Backplane Ethernet. Operation is always 25 Gbps and full duplex. KR FEC and RS-FEC are both available.
- 10GBASE-R PCS per IEEE 802.3 Clause 49 which connects to an SFP+ / QSFP+ module (which can be optical or direct attach cable). PCS25G also supports Clause 72 10GBASE-KR Backplane Ethernet. Operation is always 10 Gbps and full duplex. KR FEC is available.
- BASE-R FEC per IEEE 802.3 Clause 74
  - Also called KR FEC
- 25GBASE-R RS-FEC per IEEE 802.3 Clause 108
- Test Pattern Generator per IEEE 802.3 Clause 49.2.8, and Test Pattern Checker per IEEE 802.3 Clause 49.2.12
- Auto-Negotiation is not supported for 10G and 25G ports other than the Clause 73 Backplane ANEG listed below.
- Bit Error Rate monitoring
- Local Fault detection - A Local Fault is detected by the receiver and indicated onto the XGMII RX interface based upon a loss of link (due to RS-FEC mode loss of alignment or FEC74 mode / no FEC mode loss of block lock). Local Fault is also indicated due to a high Bit Error Rate.

Note the following capabilities are supported external to PCS25G:

- Backplane ANEG is supported per IEEE 802.3 Clause 73 by the KR IP block.

LAN8042 H2/L2 and H3P/L3P Loopbacks. See Section 3.2.10, Loopbacks and Packet BIST for detailed descriptions.

3.2.4.1 KR Forward Error Correction (KR FEC)

The IEEE 802.3 Clause 74 defines a KR Forward Error Correction (KR FEC) sublayer for Base-R PHYs, which is optionally used on a SerDes lane. The KR FEC provides coding gain to increase the link budget and BER (Bit Error Rate) performance.

The KR FEC operates after the PCS on the 66bit datastream. It can only be used when the Reed Solomon (RS-FEC) is not used.

To enable KR FEC mode,

Set PCS25G_FEC74_CFG.FEC74_ENA_TX=1 and PCS25G_FEC74_CFG.FEC74_ENA_RX=1

3.2.5 1G PCS

The PCS1G supports the following features and capabilities:

- 1000BASE-X PCS per IEEE 802.3 Clause 36, which connects to a 1000BASE-X SFP optical module. PCS1G also supports Clause 70 1000BASE-KX Backplane Ethernet
- 1000BASE-X Auto-Negotiation (ANEG) per IEEE 802.3 Clause 37

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- 1000BASE-LX/SX (optical) ANEG is supported for Pause and Remote Fault Signaling. Operation is always 1 Gbps and full duplex
- If ANEG is not wanted, software can manually set up the link parameters. For this case SW_RESOLVE_ENA must be set to 1.

- Pattern Generation and Pattern Detect/Check per IEEE 802.3 Annex 36A.1-36A.5, supporting:
  - High frequency test pattern
  - Low frequency test pattern
  - Mixed frequency test pattern
  - Continuous random test pattern with long frames
  - Continuous random test pattern with short frames
- Unidirectional operation per 802.3 Clause 66.
- If a preamble less than 8 bytes is received, PCS1G will regenerate the full eight-byte preamble. This is enabled using REGEN_PREAMBLE_ENA, which must be set to 1 on both Line and Host to prevent XGMII bus errors.
- Note the following capabilities are performed external to PCS1G:
  - Backplane ANEG per IEEE Clause 73 is supported by the KR IP block
  - The LAN8042 H2/L2 and H3P/L3P Loopbacks. See Section 3.2.10, Loopbacks and Packet BIST for detailed descriptions

When using 1G PCS Retimer mode (no MACs), the minimum IPG might be 5 bytes instead of the required 8 bytes. This is a relatively minor violation as most implementations can accept 5 bytes of IPG. However if compliance is required the MACs can be enabled (MAC Retimer mode) to ensure minimum IPG requirements are met.

3.2.6 CROSS CONNECT

The LAN8042 Cross-Connect supports these system use cases:

- Any Line to Any Host
- 1:1 Host Protection
- 1+1 Host Protection

3.2.6.1 Any Line to Any Host

Figure 3-6 illustrates the Any Line to Any Host system use case. It shows:

- A LAN8042 having four external Line Ports [0, 1, 2 and 3]
- Four Host System Functions [A, B, C and D] connected to the four LAN8042 Host Ports [0, 1, 2 and 3]. The Cross-Connect enables any-to-any mapping of the four Line Ports [0, 1, 2 and 3] to the four Host System Functions [A, B, C and D]. It is possible to configure the mapping at any time, not just at startup, and also to reconfigure the mapping. However the mappings are considered “static”, meaning they are not expected to change often, and frame flow must be completely stopped on applicable Line and Host Ports during the reconfiguration and then re-enabled. An example scenario:
- Shortly after startup, Line Port 0 is initialized and mapped to Host System Function D (Host Port 3). Line Port 0 and Host Port 3 must be the same port speed.
- Much later, Line Port 1 is initialized and mapped to Host System Function A (Host Port 0). Line Port 1 and Host Port 0 must be the same port speed. Line Port 0 continues to be connected to Host System Function D (Host Port 3) without disruption.
- A while later, Line Port 0 is remapped to Host System Function C (Host Port 2). Frame flow on Line Port 0 will be interrupted during this remapping.

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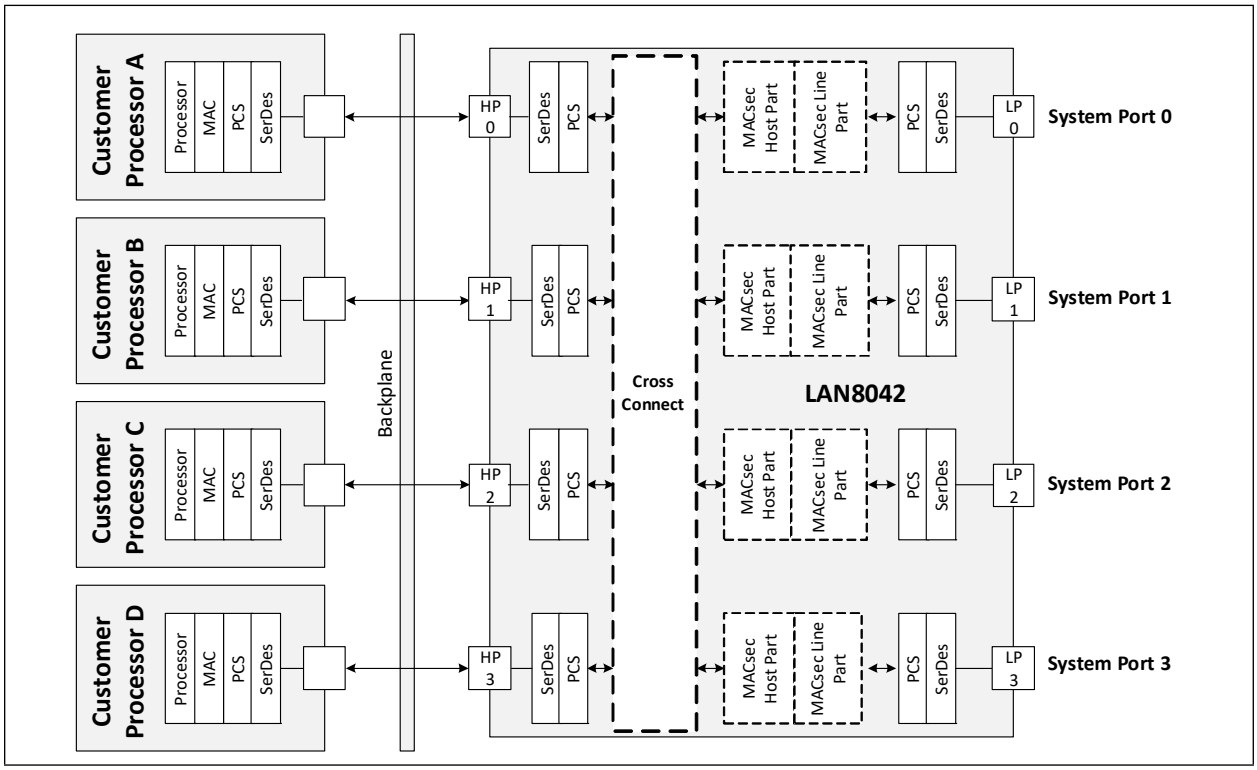
FIGURE 3-6: ANY LINE TO ANY HOST



3.2.6.2 1:1 or 1+1 Host Protection

Figure 3-7 illustrates the Host Protection system use cases. It shows:

- A Two-port Media Card consisting of a LAN8042 with two Line Ports and four Host Ports. In this mode only Line Ports 0 and 3 are available for use.
- The Cross-Connect in the LAN8042 implements a Working/Protect Switch for Line Port 0 (W/P Switch 0) and a Working/Protect Switch for Line port 1 (W/P Switch 1).
- A redundant pair of Host System Functions [A and B] connected over a backplane to the four LAN8042 Host Ports [0, 1, 2 and 3].
- System-specific Redundancy Logic which connects to the redundant pair of Host System Functions and the LAN8042.

This system configuration supports the following internal redundancy options:

- 1:1 Host System Function protection, where one Host System Function is actively using both LAN8042 Line Ports, and the other Host System Function is on standby ready to assume active duty in the event of a Host System Function fault.
- 1:1 Host System Function protection, where each Host System Function is actively using one LAN8042 Line Port. In the event of a Host System Function fault, that Host System Function's Line Port will be mapped to the remaining Host System Function.
- 1+1 Host System Function protection, where both Host System Functions are actively connected to the LAN8042 until a failure occurs. In other words, as seen in Figure 3-7, both Host Ports 0 and 1, as well as Host Ports 2 and 3 receive identical copies of each frame flowing between fabric card and the media card

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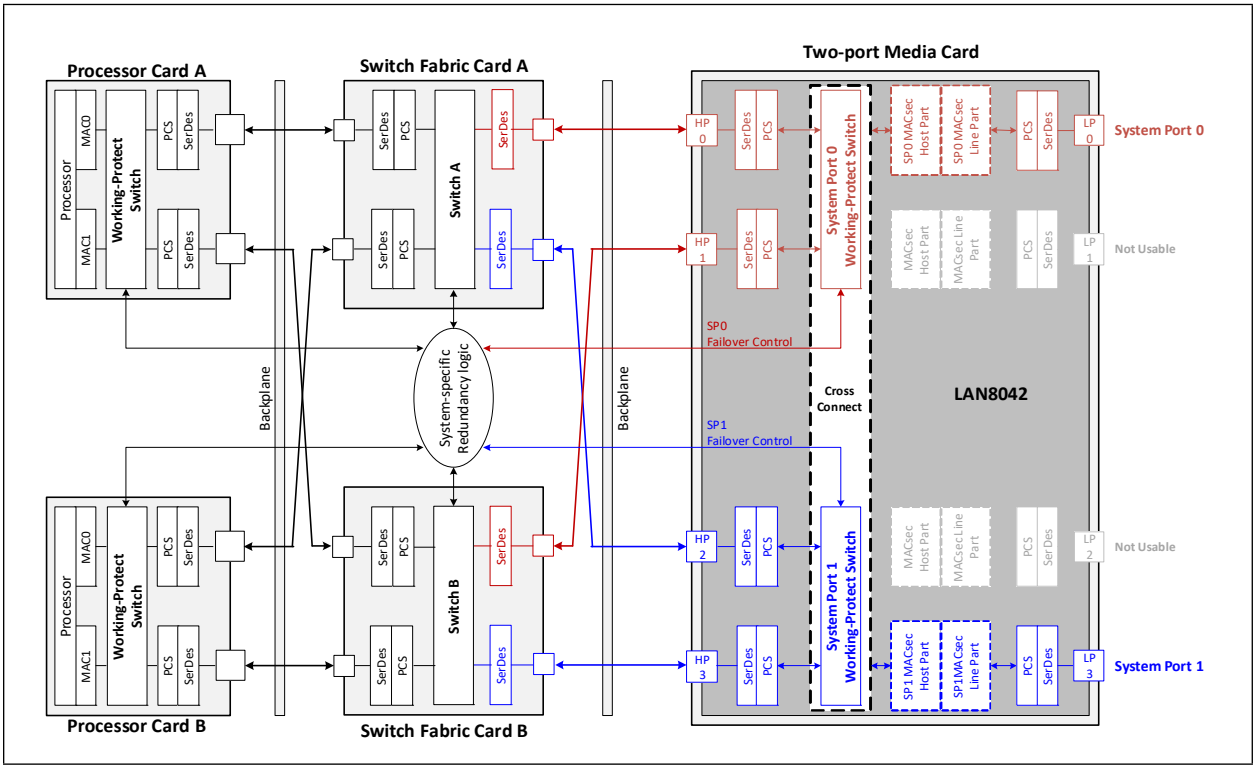
FIGURE 3-7: 1:1 OR 1+1 HOST PROTECTION



3.2.6.2.1 Host Protection Terminology

- Protected connection pair (PCP): two bi-directional serial links (connections) between the LAN8042 and a Host System Function, transporting bi-directional data for a single Line Port. The PCP can protect against a single Active Connection Fault by failing over to the Standby connection.
- 1:1-protected connection pair: a protection scheme where only one bi-directional connection carries data (“is Active” or “is in the Active state”). The other bi-directional connection carries no data (“is Standby” or “is in the Standby state”) but is prepared to take over if the active connection fails (“is Failed” or “is in the Failed state”).
- 1+1-protected connection pair: a protection scheme where both bi-directional connections carry data (assuming no Connection Fault) and the receiver selects which connection is Active and which is Standby. If a Connection Fault is detected, that connection becomes Failed and no longer carries data in either direction.
- Connection protect states: Once protection is configured and enabled, each connection may be in one of three protect states: Active, Standby, Failed
  - Active connection: the connection currently being used to transport data. It may be the Default_Active or Default_Standby connection, depending on the connection protect states.
  - Standby connection: the non-failed connection not being used to transport data, backing up the Active connection. It may be the Default_Active or Default_Standby connection, depending on the connection protect states.
  - Failed connection: a connection not capable of transporting data because of a Connection Fault. Either the Default_Active or Default_Standby connection, or even both, may be Failed.
- Default_Active and Default_Standby connections: one of the connections is designated through configuration to be the Default_Active connection, and the other connection is designated through configuration to be the Default_Standby connection.
- Connection Fault: A Hardware-detected fault on a PCP connection. If protection is enabled on the PCP, a Connection Fault will put that connection into the Failed state, and may trigger a W/P Switch failover.
- Failover Control (FC) Signals: Two FC signals connect each LAN8042 W/P Switch to the System-specific Redundancy Logic and implement a “shoot-shot” Failover Control functionality between each W/P Switch (local) and the System specific Redundancy Logic (remote).

- FC Signal Fault: When FC signal use is not disabled, when the W/P Switch initiates a failover, it expects to receive an FC Signal acknowledgment that the System-specific Redundancy Logic has also failed over. If this ACK is not received before the expiration of the configurable FC ACK Timer, an FC Signal Fault interrupt is generated which must be resolved by software. Also when the System-specific Redundancy Logic initiates a failover, the W/P Switch will send an FC Signal acknowledgment that the W/P Switch has also failed over.
- Working/Protect (W/P) Switch: The LAN8042 PCP protection switching hardware. A W/P Switch failover is a data path switching action performed by W/P Switch hardware to ensure the PCP can continue to pass data frames in the event of a single PCP Connection Fault.
- Working and Protect roles: Working and Protect roles must be tracked in software if wanted, the LAN8042 has no knowledge of these roles. The LAN8042 is only aware of Default_Active and Default_Standby roles.

3.2.6.2.2 Hardware W/P Switch Failover

1:1 and 1+1 Hardware W/P Switch Failover are supported as described below.

1:1 Automatic Hardware Protection:

In 1:1 protection in a fully working system each end of the PCP always receives only one copy of each frame.

- When the Default_Active connection is in the Active state the frame copies come over the Default_Active connection. The Default_Standby connection must be either in the Standby or Failed state, and no frames are delivered over the Default_Standby connection.
- When the Default_Standby connection is in the Active state the frame copies come over the Default_Standby connection. The Default_Active connection must be in the Failed state, and no frames are delivered over the Default_Active connection.
- Both the transmit and receive parts of both ends of the PCP use the same Active connection (protection is bidirectional - it is not allowed to use the Default_Active connection in one direction and the Default_Standby connection in the opposite direction except for a short interval during the protection switching operation).
- If a Connection Fault is detected on the Default_Active connection when in the Active state, and the Default_-Standby connection is in the Standby state, LAN8042 hardware automatically performs a W/P Switch failover to the Default_Standby connection. The Default_Standby connection is now in the Active state and carries frames, while the Default_Active connection is now in the Failed state and does not carry frames. No more hardware failover is possible without further software action, hardware protection is now effectively disabled.
- If a Connection Fault is detected on the Default_Active connection when in the Active state, and the Default_-Standby connection is in the Failed state, no W/P Switch failover is possible, and no connection can carry frames.

1+1 Automatic Hardware Protection:

In 1+1 protection in a fully working system each end of the PCP receives two copies of each frame, one copy from each connection.

- When the Default_Active connection is in the Active state the frame copies received over the Default_Active connection are used. If the Default_Standby connection is in the Standby state, frames are also delivered over the Default_Standby connection. If the Default_Standby connection is the Failed state, frames are only delivered over the Default_Active connection.
- When the Default_Standby connection is in the Active state the frame copies received over the Default_Standby connection are used. The Default_Active connection must be in the Failed state, and no frames are delivered over the Default_Active connection.
- The receive and transmit parts of both ends of the PCP always use the same Active connection (protection is bidirectional - it is not allowed to use the Default_Active connection in one direction and the Default_Standby connection in the opposite direction except for a short interval during the protection switching operation).
- If a Connection Fault is detected on the Default_Active connection when in the Active state, and the Default_-Standby connection is in the Standby state, LAN8042 hardware automatically performs a W/P Switch failover to the Default_Standby connection. The Default_Standby connection is now in the Active state and carries frames, while the Default_Active connection is now in the Failed state and does not carry frames. Hardware protection switching is now disarmed by hardware.

If a Connection Fault is detected on the Default_Active connection when in the Active state, and the Default_Standby connection is in the Failed state, no W/P Switch failover is possible, and no connection can carry frames.

Connection Fault detection:

Each of these conditions is configurable to be considered a Connection Fault:

- SD25G

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- PLL Loss of Lock
- Loss of Signal

- PCS25G
  - Link Down
- PCS1G
  - Link Down
  - PCS Sync Status

Connection Fault Detection filtering:

The enabled faults listed above are OR'd and then filtered such that the combined result must be continuously true for a minimum time. Similar, the combined result must be continuously false for a minimum time before a fault indication is cleared.

Software-controlled W/P Switch Failover:

Software may initiate a LAN8042 hardware W/P Switch failover action using W_P_SWITCH_m:WPS_FAILOVER_CTRL:WPS_FORCE_FAILOVER. The W/P Switch failover proceeds as if hardware had detected a Connection Fault, resulting in the applicable W/P Switch being in the [Default_Active/Failed, Default_Standby/Active] state (assuming no Connection Faults, and use of the FC signals is not disabled). No more hardware failover is possible without further software action, hardware protection is now effectively disabled.

FC Signals:

Each W/P Switch utilizes two FC signals as follows:

- FAILOVEROUT indicating a W/P Switch failover was initiated by the LAN8042.
- FAILOVERIN indicating a W/P Switch failover was initiated by the System-specific Redundancy Logic.
- In all use cases, failover initiated at one end of a PCP must be signaled to the other end of the PCP (if use of FC signals is enabled), triggering a partner failover. The partner must signal back to the initiator that the failover was executed.
  - Software is able to read the status of both FC signals at W_P_SWITCH_m:WPS_STATUS:WPS_FLOVR_CTRL_STS[1:0]
  - It is possible to disable use of the FC signals at W_P_SWITCH_m:WPS_FAILOVER_CONTROL:FC_SIGNAL_DISABLE
  - If FC signal use is not disabled, each end of the PCP accepts the FC signal input from the partner and uses it as described above. In this case, the partner is able to directly initiate a local W/P Switch failover, and the partner must not complete any failover until it receives an acknowledgment back from the local W/P Switch.
    - The W/P Switch acknowledgment wait time is configurable at W_P_SWITCH_m:WPS_FAILOVER_CONTROL:FC_ACK_TIMER
  - If FC signal use is disabled, the local W/P Switch does not accept the FC signal input from the partner. In this case, the partner is not able to directly initiate a local W/P Switch failover (indirect triggering is still possible through software), and the partner completes any failover without needing an acknowledgment back from the local W/P Switch. The local W/P Switch will also not look for the acknowledgment from the partner.

FC Signal Fault detection:

An acknowledgment from the partner is received by the local W/P Switch (if use of FC signals is not disabled). In the event that the local W/P Switch failed over but does not receive an acknowledgment from the partner, an interrupt is generated (if enabled) providing FC Signal Fault detection.

Interrupts:

The WPS_CONN_FAULT_INTR_m interrupt is generated (if enabled) when a Connection Fault is detected on the Default_Active connection.

The WPS_FC_ACK_TIMER_INTR_m interrupt is generated (if enabled) if a FC Signal Fault is detected (if use of FC signals is not disabled).

- The WPS_FAILOVER_INTR_m interrupt is generated (if enabled) whenever a W/P Switch failover occurs.

Interrupts also exist on all Host and Line Ports covering fault cases of interest. These interrupts are not part of the W/P Switch design, but are still available when hardware protection is enabled. One expected use of these interrupts is to notify software of a Standby connection failure (which is not monitored by the W/P Switch hardware).

3.2.7 MAC

The MAC is used on both the Line and Host side, and consists of the following major sub-functions:

- MAC Kernel supporting traditional 802.3 MAC layer functions
- MAC Merge supporting 802.3 Frame Preemption functions
- Packet Interface Wrapper which implements the Packet Interface and handles MACsec Host Port formats
- Port Statistics supporting p-MAC and e-MAC statistics per 802.3

3.2.7.1 MAC Kernel

The TX MAC Kernel performs the following tasks:

- Implement IEEE 802.3 Reconciliation Sublayer function
- Calculate and insert the CRC for all frames including CRC corruption for error cases.
- Convert frames received from the MAC Host Port to 25/X GMII format which includes adding appropriate framing control characters and FCS
  - Note in this case “MAC Host Port” refers to the interface between the MAC Kernel and the MAC Merge blocks, and exists in both the MACsec Host Part and MACsec Line Part
- Generate the interframe gap (IFG) on the 25/X GMII using the IEEE 802.3 Deficit Idle Count (DIC) algorithm to achieve an average IFG of 12 bytes
- Maintain TX statistics counters located in the Port Statistics function
- Support Link Fault Signaling (LFS, IEEE 802.3 clause 46.3.4) and Unidirectional Ethernet (IEEE 802.3 clause 66.4). Since LAN8042 has a MAC (not a normal PHY function), the LF/RF ordered sets can be terminated either by outside MAC or the LAN8042 Line MAC.
  - If it is desired that the LAN8042 Line MAC is to handle LFS [LFS Line Side Mode], then the Line MAC's LFS_-MODE_ENA must be set to 1, and LF_RELAY_ENA and RF_RELAY_ENA must both be set to 0. These registers must all be set to 0 on the Host MAC.
  - If the customer system MAC is to handle LFS [LFS Transparent Mode], then LFS_MODE_ENA must be set to 0 on both Host and Line MAC, and LF_RELAY_ENA and RF_RELAY_ENA must be set to 1 on both Host and Line MAC.
  - Unidirectional operation is independent of LFS handling, and is configured using LFS_UNIDIR_ENA.
  - The MAC can be controlled to generate LF or RF using force_lf_i or force_rf_i.

The RX MAC Kernel performs the following tasks:

- Implement IEEE 802.3 Reconciliation Sublayer function
- Calculate and check the CRC of each frame for validity and abort mark any frame with an invalid CRC
- Convert frames received in 25/X GMII format into the MAC host format which includes removing the framing control characters
  - Note in this case “MAC Host Port” refers to the interface between the MAC Kernel and the MAC Merge blocks, and exists in both the MACsec Host Part and MACsec Line Part
- Perform a variety of length checks including looking for runt frames (less than 64 bytes), oversized and jabber frames (longer than the configured maximum). Length checks are supported for frames with up to four VLAN tags.
- Maintain RX statistics counters located in the Port Statistics function
- Support LFS if enabled (see TX MAC Kernel description)
  - When the MAC detects LF or RF it asserts lf_received or rf_received

VLAN tag support:

- Up to four VLAN tags, where VLAN tags can occur in any order (any enabled TPID value can exist in any of the up to four VLAN tag locations and the same TPID value can exist in multiple VLAN tag locations)
- Native understanding of the standard Tag Protocol ID (TPID) values for C-tag (0x8100) and S-tag (0x88A8)
- Two configurable TPID values beyond the standard values

3.2.7.2 MAC Merge

The TX MAC Merge function implements the Frame Preemption Transmit Processing State Diagram of IEEE 802.3-2018.

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The RX MAC Merge function implements the Frame Preemption Receive Processing State Diagram of IEEE 802.3-2018. This block performs frame count & fragment count checks for proper reassembly. Note in LAN8042 the fragments are never actually reassembled into complete frames. In case of a fragment count mismatch or FCS error, it asserts an error indication (note a mismatched mCRC is not an error rather it indicates the CRC is actually an FCS).

The Verify Respond function implements the Verify and Respond State Diagrams of IEEE 802.3-2018.

3.2.7.3 Packet Interface Wrapper

The Packet Interface Wrapper handles the following functions:

- Provide a Packet Interface to MACsec and FC Buffer blocks. On this Packet Interface, frames are transported without Preamble, SFD/SMD, and CRC.
  - [MCH disabled] Preamble and SFD/SMD are stripped from frames toward the Packet Interface, and are added to frames received from the Packet Interface.
  - [MCH enabled] The MCH is sent as part of the packet toward the Packet Interface, and received as part of the packet from the Packet Interface.
  - For frames heading toward the Packet Interface, the CRC is already checked by the Rx MAC Kernel. The Wrapper strips the CRC and also passes along the CRC error indication from the Rx MAC Kernel to the Packet Interface.
  - For frames arriving from the Packet Interface, the Wrapper inserts a dummy CRC at the end of the frame and performs any padding if needed. The Tx MAC Kernel updates the dummy CRC. For frames requiring a corrupt CRC, Wrapper signals the Tx MAC Kernel to corrupt the CRC. Two different CRC corruptions schemes are supported, configurable in the Tx MAC Kernel:
    - CRC Inversion. The CRC is calculated and inverted.
    - CRC with Debug Code. The Packet Interface Wrapper provides a debug code to use instead of the CRC. Note there is a corner case if the CRC happens to match the debug code, the msb is inverted by the MAC Kernel so the CRC will still fail.
- [Host Packet IF Wrapper] Process the Egress Host Interface Format bytes as applicable toward the Rx MAC Packet Interface. Generate the Ingress Host Interface Format bytes as applicable toward the Tx MAC Kernel.
- If an error condition is detected, discard and count the errored frame.

3.2.7.4 Port Statistics

The following counters count the number of bytes or frames received or transmitted. The counters count continuously and are only cleared if the device is reset or the counter is written with 0 through the CPU interface. These counters wrap continuously, rolling over to 0 when the maximum value is reached.

Unless specified otherwise, each counter is 32 bits.

- RX_IN_BYTES_CNT (64 bits) counts the total bytes received including preamble
- RX_OK_BYTES_CNT (64 bits) counts the number of bytes received in valid frames
- RX_BAD_BYTES_CNT counts the number of bytes received in invalid frames
- TX_OUT_BYTES_CNT (64 bits) counts the total number of bytes transmitted including preamble
- TX_OK_BYTES_CNT (64 bits) counts the number of bytes in successfully transmitted frames

The following counters are based on the type of frame received or transmitted:

- RX_PAUSE_CNT counts the number of pause frames received
- RX_UNSUP_OPCODE_CNT counts the number of control frames received with unsupported opcodes
- RX_UC_CNT counts the number of unicast frames received
- RX_MC_CNT counts the number of multicast frames received
- RX_BC_CNT counts the number of broadcast frames received
- TX_PAUSE_CNT counts the number of pause frames transmitted
- TX_UC_CNT counts the number of unicast frames transmitted
- TX_MC_CNT counts the number of multicast frames transmitted
- TX_BC_CNT counts the number of broadcast frames transmitted

The following error counters are provided:

- RX_SYMBOL_ERR_CNT counts the number of symbol errors received
- RX_CRC_ERR_CNT counts the number of frames received with CRC errors

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- RX_UNDERSIZE_CNT counts the number of undersized frames received with valid CRC
- RX_FRAGMENTS_CNT counts the number of undersized frames received with invalid CRC
- RX_IN_RANGE_LENGTH_ERR_CNT counts the number of frames where the length field does not match the frame length
- RX_OUT_OF_RANGE_LENGTH_ERR_CNT counts the number of frames with an illegal length field
- RX_OVERSIZE_CNT counts the number of oversize frames with valid CRC
- RX_JABBERS_CNT counts the number of oversize frames with an invalid CRC
- RX_XGMII_PROT_ERR_CNT counts the number of XGMII protocol errors detected.

The following size histogram counters are provided for both transmit and receive directions:

- Frames with 64-byte payloads
- Frames with 65-byte to 127-byte payloads
- Frames with 128-byte to 255-byte payloads
- Frames with 256-byte to 511-byte payloads
- Frames with 512-byte to 1023-byte payloads
- Frames with 1024-byte to 1518-byte payloads
- Frames with 1519-byte to maximum size payloads

Frame size counters also count invalid frames, as long as they are not short frames, fragments, long frames, or jabber frames. Long frames are defined as those greater than MAX_LEN bytes. The above counters are all 32 bits unless otherwise noted, and all counters wrap.

3.2.8 FLOW CONTROL BUFFER

The Flow Control Buffer provides:

- Buffering from the Host and Pause generation toward the Host to accommodate MACsec frame expansion and receipt of Pause frames from the Line.
  - Pause frames received from the Line can result in flow control from the MACsec Line Part to here (see separate section on Flow Control). In this case the Line Port Pause timer function is implemented here.
  - Pause generation toward the Host is configurable based on XON/XOFF thresholds.
  - Cut-through operation
- Special handling of MAC Control Frames which must pass from Host to Line bypassing the FC Buffer.
  - Control frames are buffered in a dedicated queue which has strict priority scheduling over the normal data frame queue, and are not stopped due to receipt of Pause frames from the Line

The ingress_fc_buffer provides:

- Buffering toward the Host to allow Pause frame insertion toward the Host.
  - IFG shrink is available if enabled and if necessary to provide some speedup toward the Host to compensate for Pause frame insertion.
  - Cut-through operation

3.2.9 MACSEC

The LAN8042 includes a high-performance streaming MACsec frame processing engine that provides hardware acceleration for the complete MACsec frame transform along with frame classification and statistics counter updates. The following list includes some of the major features of the MACsec engine.

- Fully IEEE 802.1AE-2006, IEEE 802.1AEbn, and IEEE 802.1AEbw-2013 compliant.
- 64 secure associations (SA) per direction and 64 ingress consistency check rules.
- MACsec cipher suite GCM-AES-128 support.
- MACsec cipher suite GCM-AES-256 support.
- MACsec cipher suite GCM-AES-XPN-128/256 support.
- VLAN and Q-in-Q tag detection.
- MACsec tag detection and sub-classification (Untagged, Tagged, BadTag, KaY).
- Programmable “control” packet classification.
- 8-entry programmable non-match flow operation selection (drop, bypass), depending on MACsec tag sub-classification and control packet classification.
- Programmable confidentiality offset (0B – 127B).

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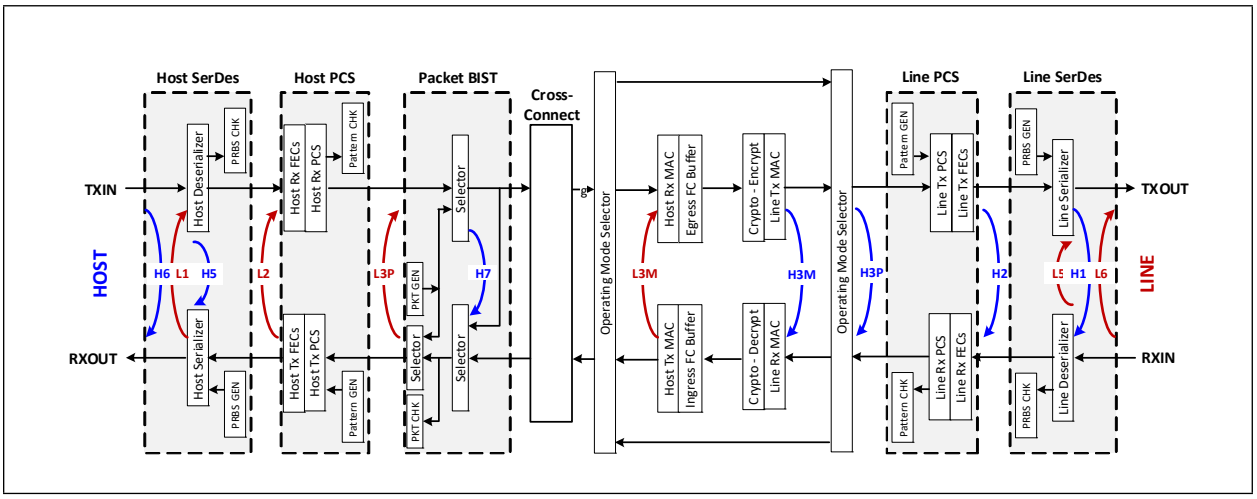
- SecTAG insertion and removal.
- Integrity Check Value (ICV) checking/removal and calculation/insertion.
- Packet number generation and checking.
- IEEE 802.1AE MACsec statistics counter support.
- Ingress path consistency checking (ICC)–64/16 entry programmable matching table with separate drop/transfer decisions.
- MTU checking and oversize dropping dependent on VLAN User priority for VLAN frames and at global level for non-VLAN frames.
- Advanced MACsec transformations–VLAN tag bypass and EoMPLS header bypass.
- Hardware offload for the nextPN and lowestPN update from the host(KaY).
- Support for AES-ECB, AES-CTR, and AES-GCM/GMAC transformation for FIPS certification of the crypto core.

3.2.10 LOOPBACKS AND PACKET BIST

LAN8042 supports loopbacks and data plane BIST as shown in Figure 3-8.

FIGURE 3-8: LOOPBACKS AND DATA PLANE BIST



3.2.10.1 Loopbacks

Loopback details are provided in Table 3-1.

TABLE 3-1: LOOPBACKS

LB Name	Description	Applicable Registers
H1/L1	H1: Line SerDes TXOUT to RXIN Serial LB L1: Host SerDes RXOUT to TXIN Serial LB	Set both LN_CFG_TX2RX_LP_EN=1 and LN_CFG_TXLB_EN=1 HOST_PMA_EXT : LANE_GRP_0:LANE_04.LN_CFG_TX2RX_LP_EN and HOST_PMA_EXT :LANE_GRP_0:LANE_19.LN_CFG_TXLB_EN
H2/L2	H2: Line PCS PMA-Side LB back toward XC L2: Host PCS PMA-Side LB back toward XC Loopback comes after all FEC functions Clock is looped, no Rate Adaptation performed H2/L2 Loopbacks also provide these options: • Forward packets to the SerDes • Block packet forwarding to the SerDes and instead send zeros to the SerDes • Block packet forwarding to the SerDes and instead send 00FF pattern to the SerDes	HOST_SLICE:HOST_P-MA_PCS_LPBK:L2_LPBK:L2_LPBK LINE_SLICE:LINE_P-MA_PCS_LPBK:H2_LPBK:H2_LPBK
H3P/L3P	H3P: Line PCS Core-Side LB back toward XC L3P: Host PCS Core-Side LB back toward XC Clock is looped, Rate Adaptation is performed H3P/L3P Loopbacks also provide these options: • Forward packets to the PCS • Block packet forwarding to the PCS and instead send XGMII Idles to the PCS	HOST_SLICE:HOST_P-MA_PCS_LPBK:L3P_LPBK:L3P_LPBK LINE_SLICE:LINE_P-MA_PCS_LPBK:H3P_LPBK:H3P_LPBK
H3M/L3M	H3M: Line MAC PCS-Side LB back toward XC L3M: Host MAC PCS-Side LB back toward Line	(H3M) LINE_MAC_LB_CFG:XGMII_HOST_LB_EN (L3M) HOST_MAC_LB_CFG:XGMII_HOST_LB_EN
H5/L5	H5: Host SerDes RXIN to TXOUT Serial LB L5: Line SerDes RXIN to TXOUT Serial LB	Set all LN_CFG_RX2TX_LP_EN=1, LN_CFG_RXL-B_EN=1, and LN_CFG_CDRCK_EN=1
H6/L6	H6: Host SerDes RXIN to TXOUT Serial LB L6: Line SerDes RXIN to TXOUT Serial LB	Set all LN_CFG_RX2TX_LP_EN=1, LN_CFG_RXL-B_EN=1, and LN_CFG_CDRCK_EN=0.
H7	H7: Packet BIST Core-Side LB toward Host L7: N/A - does not exist H7 supports both Packet BIST operations as well as Host PCS Core-Side LB back toward Host.	HOST_SLICE:PKTBIST_DATAPATH_CONTROL: IGR_XGMII_PG_SEL2

3.2.10.2 Data Plane BIST

LAN8042 supports the following data plane BIST:

- SD25G PRBS Generator and Checker.
- PCS1G Pattern Generator and Checker.
- PCS25G Pattern Generator and Checker.
- PKT_BIST Packet Generator and Checker, described below.

The Packet BIST consists of a Packet Generator, Packet Checker, and data path selectors. The data path selectors implement the LAN8042 H7 Loopback, which supports the Packet BIST functions but can also be used as a general-purpose data path loopback supporting all ports speeds.

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The **Packet Generator** generates configurable 25/X GMII Ethernet frames, either toward the Cross Connect or toward the Host PCS. The Packet Generator supports the following features:

- Standard Packet with some amount of programmable fields.
- Standard Ethernet frame with Preamble and FCS. Advanced features such as P-frames/fragments are not supported.
- Standard Packet payload is always PRBS31, packet length is configurable.
- When not sending Ethernet frames it sends Idles. It can also send a constant stream of Idles.
- Provides a count of Packets Sent
- Standard Packet Length, IPG, and lane alignment to 25/X GMII bus are all configurable

Table 3-2 shows the fixed and configurable fields for generating a Standard Packet.

TABLE 3-2: PACKET GENERATOR STANDARD PACKET

Field	Bits	Content
Preamble	64	0xFB555555555555D5[1]
Destination Address	48	Configurable
Source Address	48	Configurable
EtherType	16	Configurable
PRBS31	Variable	Continuous 2^31-1 pattern
FCS	32	Standard Ethernet CRC-32
Terminate	8	0xFD[2]

Note 1: The “FB” becomes a “55” when transmitted on the network.
2: The “Terminate” is an internal indication and is not transmitted on the network.

The Packet Checker monitors incoming 25/X GMII Ethernet frames arriving from one of three places:

- The Cross-Connect (LAN8042 ingress direction)
- The Host RX PCS (LAN8042 egress direction)
- The Packet Generator (mainly useful as a Packet BIST self-test)

The Packet Checker supports the following features:

- Counts Ethernet frames received with correct FCS
- Counts Ethernet frames received with incorrect FCS
- Counts PRBS31 bit errors
- Counts Ethernet frame fragments received
- Counts Local Fault (LF) ordered sets received in IPG

The Packet Generator and Checker provides basic test capabilities covering the following:

- PCS and SerDes: Runs at rate and covers all speeds, FECs, and datapaths (e.g. PCS Retimer and MAC Retimer).
  - No coverage of ANEG or KR Training
- Cross-Connect
- MACsec: Checks that basic MACsec is configured and running properly by encrypting toward the Line Port, looping, and decrypting from the Line Port.
  - Many encapsulations and advanced MACsec functions are not covered.
  - Ingress Host Format 0 and Egress Host Format 0 is directly covered
  - Other Egress Host Formats are not covered.
  - Other Ingress Host Formats can be generated but not checked by the Packet Checker

Frame Preemption cannot be tested. Only e-Frames can be generated or checked.

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3.3 Frame Preemption Verify/Respond System Operation

As described in 802.3, frame preemption is enabled in the transmit direction only if it is determined that the Link Partner supports the preemption capability. This is a two-step process:

1. Discovery. Link Partner preemption capability is advertised using the Additional Ethernet Capabilities TLV in an LLDPDU addressed to the Nearest Bridge group address (see IEEE Std 802.1Q).
2. Verification. Frame preemption capability is verified using the Verify/Respond protocol, executed by the MAC Merge functions at each end of the link. The MAC Merge function initiates verification by sending a verify mPacket, expecting receipt of a respond mPacket to confirm that the Link Partner supports frame preemption.

Without an intervening LAN8042, the MAC Merge function in the customer system Host MAC would communicate directly with the MAC Merge function in the Link Partner Line MAC to verify frame preemption capability.

With an intervening LAN8042 operating in MAC Retimer mode, two additional MAC Merge functions are introduced: one in the LAN8042 Host MAC and the other in the LAN8042 Line MAC.

LAN8042 supports two Frame Preemption Verify / Respond options toward the Line Port:

- Verify / Respond Line Side Mode
  The MAC Merge function in the LAN8042 Line MAC executes the Verify / Respond protocol for the system. The customer system must read the result from the LAN8042 Line MAC and configure its own Host MAC accordingly.
- Verify / Respond Transparent Mode
  The MAC Merge function in the customer system Host MAC executes the Verify / Respond protocol for the system. Verify and Respond mPackets are passed transparently through the LAN8042 in both directions. The customer system Host MAC and Link Partner Line MAC resolve the verification state, and must configure all MACs accordingly.

Once preemption verification is complete, operation is the same regardless of which Verify/Respond mode was used:

- If preemption is enabled in MAC Retimer mode fragments are passed through the LAN8042 in both directions, but are checked for proper formatting.
- If preemption is disabled in MAC Retimer mode the LAN8042 will filter fragments received from the Line. The LAN8042 will pass fragments received from the Host but they should not occur in a proper configuration.
- In PCS Retimer mode fragments are passed through the LAN8042 transparently in both directions.

Frame Preemption verification should not be performed between the Host and the LAN8042 Host MAC.

3.4 Link Fault Signaling System Operation

Link Fault Signaling (LFS) provides fault detection and reporting for 10G and 25G links per 802.3 clause 46.3.4. Two types of link fault are detected and reported by the Reconciliation Sublayer (RS), which is part of the MAC:

- Local Fault (LF): a receive fault which is between the link partner RS and the local RS
- Remote Fault (RF): a transmit fault which is between the local RS and the link partner RS

Without an intervening LAN8042, the RS function in the customer system Host MAC would communicate fault status directly with the RS function in the Link Partner Line MAC.

With an intervening LAN8042 operating in MAC Retimer mode, two additional RS functions are introduced: one in the LAN8042 Host MAC and the other in the LAN8042 Line MAC.

LAN8042 supports two LFS options toward the Line Port:

- LFS Line Side Mode
  The RS function in the LAN8042 Line MAC executes the LFS protocol for the system. LF/RF symbols from the Line Port are terminated in the Line MAC, LF/RF symbols from the Host Port are terminated in the Host MAC.
- LFS Transparent Mode
  The RS function in the customer system Host MAC executes the LFS protocol for the system. The LAN8042 transparently passes the LF and RF symbols between Line and Host Ports.

In PCS Retimer mode the LAN8042 passes the LF and RF symbols between Line and Host Ports.

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3.5 Flow Control System Operation

3.5.1 PAUSE HANDLING AND FLOW CONTROL

The LAN8042 supports all the following Flow Control capabilities in MAC Retimer mode:

- Options for handling Pause from Line MAC partner:
  - React at the Egress Flow Control Buffer output
  - React at the TX Line MAC
  - Do not react to Pause in LAN8042, pass the Pause frame to the Host
- Internal flow control to the Egress Flow Control Buffer from the TX Line MAC and MACsec blocks
- Forwarding Pause from the Host to the TX Line Port
  - LAN8042 never generates Pause to the Line Port
- Generating Pause toward the Host due to MACsec frame expansion or Pause received from Line MAC partner
  - This capability is used with MACsec Egress Host Formats 0 and 2 unless IFG Extend is used. See Section 3.7.5.1 for more details on the various Egress Host Formats.

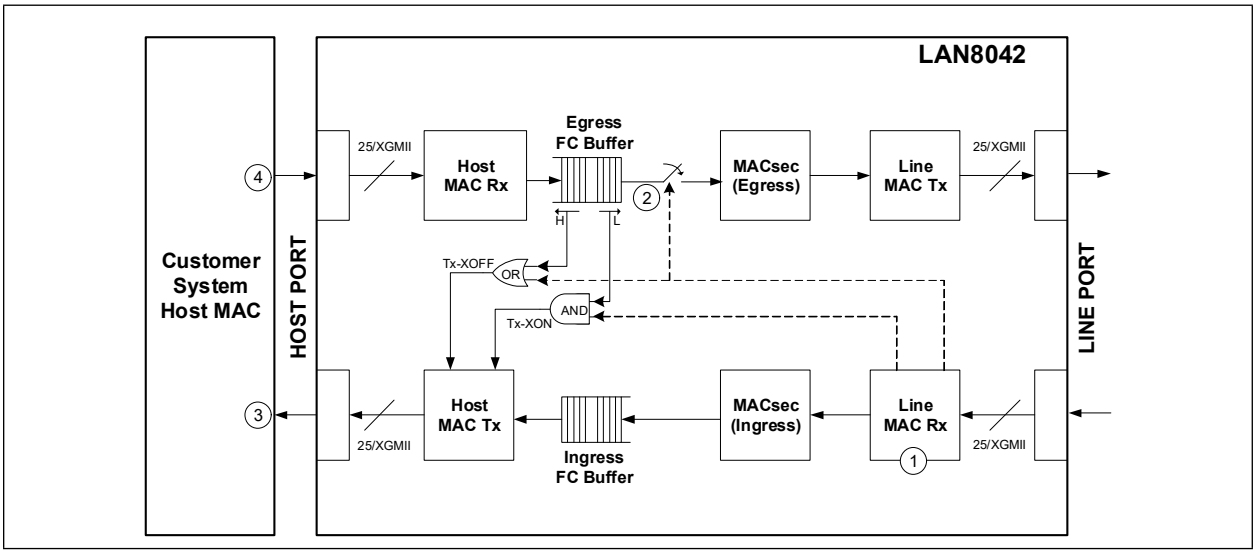
3.5.2 BASIC FLOW CONTROL HANDLING

"Basic Flow Control" in this section describes:

- Receiving Pause from the Line MAC partner and reacting to it at the Egress FC Buffer output
- Generating Pause toward the Host due to filling of the Egress FC Buffer.
- Forwarding Pause from the Host to the TX Line Port.

Figure 3-9 illustrates Basic Flow Control operation when a pause frame is received from the Line:

FIGURE 3-9: BASIC FLOW CONTROL, PAUSE FROM THE LINE



Follow the tags 1, 2, 3, 4 in the figure.

1. A pause frame (XOFF) is received by the LAN8042 Line MAC RX. This frame is internally consumed by the Line MAC. The Line MAC RX signals the Egress FC Buffer indicating Pause was received and providing the Pause quanta.
2. The Egress FC Buffer goes into the Pause state at the next TX frame boundary. The Pause Timer is maintained by the Egress FC Buffer and is started only after it goes into the Pause state. In the worst case, the Egress FC Buffer may immediately go into the Pause state. Hence, the Egress FC Buffer drain rate is 0 and the fill rate can be the full Host Port speed. The Egress FC buffer will signal XOFF to the Host MAC TX ASAP to schedule a pause transmission toward the Host. This signaling is shown via the optional "OR" gate.
   - Even when LAN8042 is not in the Pause state, the Egress FC Buffer may still signal XOFF / XON to the LAN8042 Host MAC TX (scheduling a pause transmission toward the Host) to manage frame expansion due to MACsec. This is done through XOFF / XON thresholds.

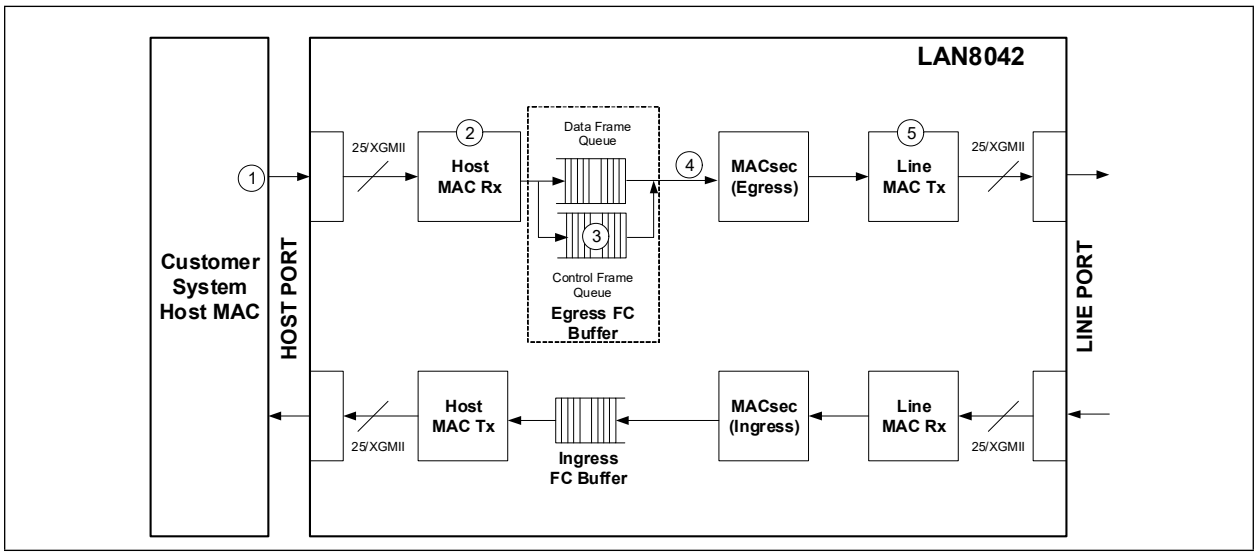
3. The LAN8042 Host MAC TX can schedule a pause frame for transmission toward the Host at the next RX frame boundary. In the worst case, the LAN8042 Host MAC TX has just started transmitting a jumbo frame toward the Host. During this time the Egress FC Buffer is continuing to receive frames from the Host. The Egress FC Buffer must have the capability to hold at least one Jumbo frame until the XOFF pause frame is received by the customer system Host MAC.
4. It is possible that the customer system Host MAC may have started transmitting a jumbo frame toward the Egress FC Buffer. So the Egress FC Buffer must also have the capability to hold a second Jumbo frame until the customer system Host MAC stops sending.
   - In addition to the two jumbo frames, there is also an 802.3-specified reaction time that the customer system Host MAC is expected to meet, during which the Egress Flow Control Buffer is continuing to receive frames from the Host.

The following Egress FC Buffer configuration settings control the handling of pause frames received from the Line in Basic Flow Control operation:

- PAUSE_REACT_ENA - Enables pause reaction and pause timer maintenance in the Egress FC Buffer. This should be set to 1.
- PAUSE_GEN_ENA - Enables XON and XOFF pause frame signaling to the LAN8042 Host MAC TX based on XON and XOFF thresholds. This should be set to 1.
- INCLUDE_PAUSE_RCVD_IN_PAUSE_GEN - Enables the optional “OR” and “AND” gates in the previous figure. Recommended to be set to 1. When disabled the LAN8042 Host MAC TX will only generate pause frames toward the Host based on Egress FC Buffer XOFF/XON thresholds.

Figure 3-10 illustrates Basic Flow Control operation when a pause frame is received from the Host:

FIGURE 3-10: BASIC FLOW CONTROL, PAUSE FROM THE HOST



Follow the tags 1, 2, 3, 4, 5 in the figure.

1. The Host experiences congestion in Ingress and sends a pause (XOFF) to the LAN8042 Host Port. Ultimately this pause frame should reach the LAN8042 Line MAC link partner and control it to stop sending frames to the LAN8042 and ultimately toward the Host.
2. The LAN8042 Host MAC RX receives this pause frame but it is not enabled to react on received pause frames. The pause frame is passed by the LAN8042 Host MAC RX to the Egress FC Buffer.
   - LAN8042 never pauses the ingress stream toward the Host since it is not designed with large Ingress FC Buffers.
3. The Egress FC Buffer maintains two logical queues, one for Data frames and one for MAC Control frames (such as a pause frame). MAC Control frames cut ahead of any Data frames or fragments. In case a data frame is already scheduled and in progress, the MAC Control frames are transmitted from the Egress FC Buffer at the next boundary irrespective of if there are other data frames in the Data frame queue. This is done to quickly relay MAC Control frames to the Line.
4. The Egress FC Buffer might be in the Pause state due to pause (XOFF) received from the Line. Irrespective of

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the Pause state, the Egress FC Buffer transmits any or all MAC Control frames from the Control frame queue.

5. The pause frame passes through the MACsec block and also through the Line MAC TX block to the Line.
6. Not shown, but when the pause frame reaches the Line MAC link partner, it is expected that the Line MAC link partner will react to the pause frame and stop sending frames toward the LAN8042.

The following Egress FC Buffer configuration settings control the handling of pause frames received from the Host in Basic Flow Control operation:

- TX_CTRL_QUEUE_ENA determines if the Control frame queue is enabled in the Egress FC Buffer. This should be set to 1 in Basic Flow Control mode.
- TX_CTRL_QUEUE_START/END and TX_DATA_QUEUE_START/END configure the partitioning of Egress FC Buffer physical memory between Data frame and Control frame queues.

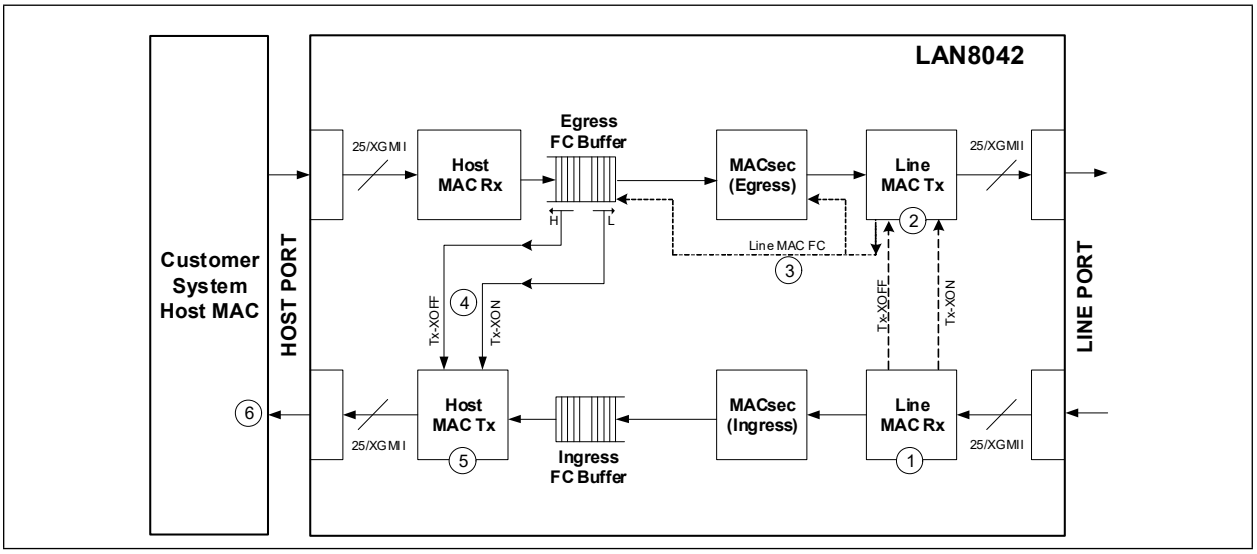
3.5.3 ADVANCED FLOW CONTROL HANDLING

"Advanced Flow Control" in this section describes:

- Receiving Pause from the LAN8042 Line MAC partner and reacting to it at the LAN8042 Line MAC TX.
- LAN8042 Line MAC TX flow-controlling the Egress FC Buffer.
- Generating Pause toward the Host due to filling of the Egress FC Buffer.
- Forwarding Pause from the Host to the TX Line Port while in this mode.

Figure 3-11 illustrates Advanced Flow Control operation when a pause frame is received from the Line:

FIGURE 3-11: ADVANCED FLOW CONTROL, PAUSE FROM THE LINE

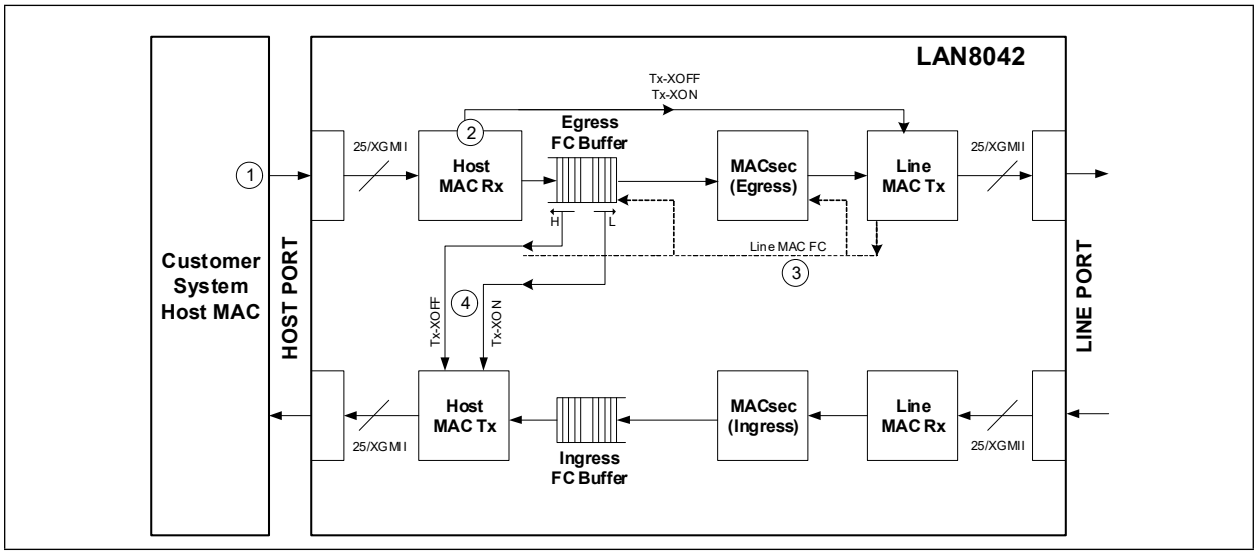


Follow the tags 1, 2, 3, 4, 5, 6 in the figure.

1. A pause frame (XOFF) is received by the LAN8042 Line MAC RX. This frame is internally consumed by the Line MAC.
2. The Line MAC RX signals the Line MAC TX indicating Pause was received and providing the Pause quanta. The Line MAC TX goes into the Pause state at the next TX frame boundary. The Pause Timer is maintained by the Line MAC TX and is started only after it goes into the Pause state.
3. The Line MAC TX issues Line MAC FC to stall the MACsec (Egress) and the Egress FC Buffer.
4. The Egress FC Buffer signals XOFF/XON to the LAN8042 Host MAC TX based on the XOFF/XON thresholds.
5. The LAN8042 Host MAC TX can schedule a pause frame for transmission toward the Host at the next RX frame boundary.
6. The customer system Host MAC receives the pause frame and stops transmitting toward the Egress FC Buffer.

Figure 3-12 illustrates Advanced Flow Control operation when a pause frame is received from the Host:

FIGURE 3-12: ADVANCED FLOW CONTROL, PAUSE FROM THE HOST



Follow the tags 1, 2, 3, 4, 5 in the figure.

1. The Host experiences congestion in Ingress and sends a pause (XOFF) to the LAN8042 Host Port.
2. The LAN8042 Host MAC RX receives and consumes this pause frame. The Pause timer is maintained in the LAN8042 Host MAC RX (instead of Line MAC TX) which generates XOFF / XON control to the LAN8042 Line MAC TX.
3. The LAN8042 Line MAC TX issues Line MAC FC to stall the MACsec (Egress) and the Egress FC Buffer in order to transmit a pause frame (either XOFF or XON) to the Line. This path will work irrespective of whether the LAN8042 Line MAC TX is in the Pause state.
4. The Egress FC Buffer is not expected to fill up due to Line MAC FC, but it can still signal XOFF/XON to the LAN8042 Host MAC TX based on the XOFF/XON thresholds

The following Egress FC Buffer configuration settings control Advanced Flow Control operation:

- PAUSE_GEN_ENA must be set to 1 to enable signaling to the LAN8042 Line MAC TX.

PAUSE_REACT_ENA, INCLUDE_PAUSE_RCVD_IN_PAUSE_GEN and TX_CTRL_QUEUE_ENA must all be set to 0.

3.6 Auto-negotiation and Training

The LAN8042 supports Auto-Negotiation per IEEE 802.3 clause 73 for the following link types:

- 1000BASE-KX (backplane)
- 10GBASE-KR (backplane)
- 10GBASE-CR (DAC)
- 25GBASE-KR/KR-S (backplane)
- 25GBASE-CR/CR-S (DAC)

Clause 73 auto-negotiation enables devices at both ends of a link segment to advertise abilities, acknowledge receipt, and discover the common modes of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

Clause 73 auto-negotiation also provides a parallel detection function to allow devices to connect to and inter-operate with devices which do not support Clause 73 auto-negotiation or have auto-negotiation disabled.

The LAN8042 also supports Auto-Negotiation per IEEE 802.3 clause 37 for the 1000BASE-LX and 1000BASE-SX (optical) link types. Auto-negotiation is supported for Pause and Remote Fault Signaling only, these link types are only supported at 1 Gbps and with full duplex.

The LAN8042 allows management to separately enable or disable clause 37 and clause 73 auto-negotiation, and to select a specific operational mode. Note there is no auto-negotiation support for 10G and 25G optical link types.

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The LAN8042 supports Link Training per IEEE 802.3 clause 72 for the following link types:

- 10GBASE-KR (backplane), follows Clause 72.6.10
- 10GBASE-CR (DAC), follows Clause 72.6.10
- 25GBASE-KR/KR-S (backplane), follows Clause 72.6.10 with minor 25G modifications specified by Clause 92.7.12 Lane 0
- 25GBASE-CR/CR-S (DAC), follows Clause 72.6.10 with minor 25G modifications specified by Clause 92.7.12 Lane 0

Clause 72 Link Training allows the devices at both ends of the link to dynamically select digital filter tap settings which optimize link performance.

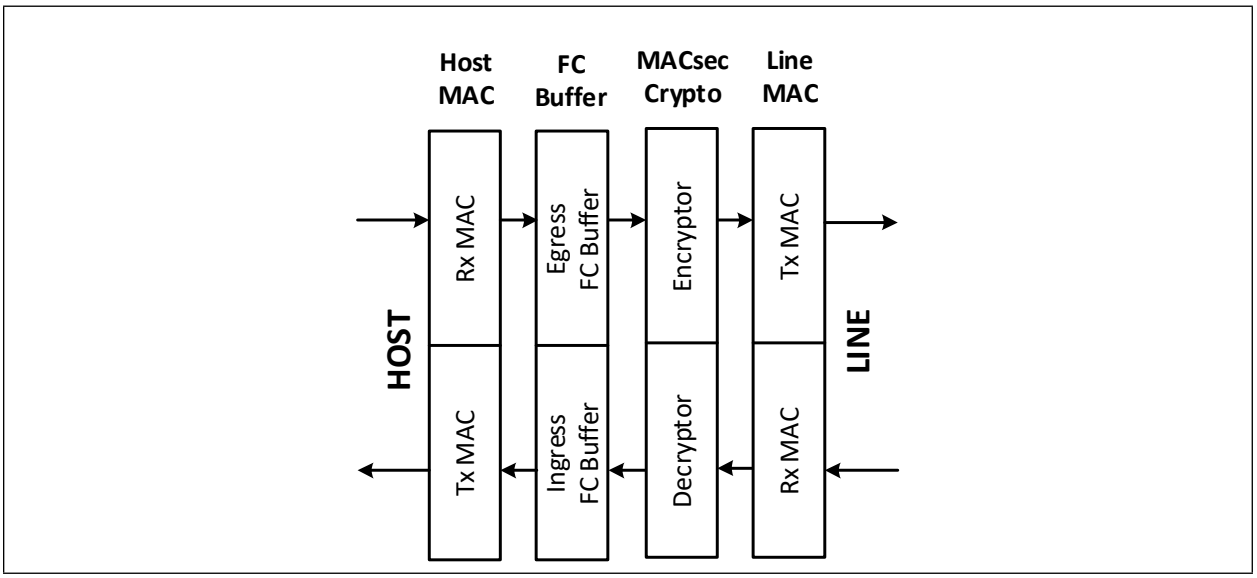
The LAN8042 allows management to disable dynamic link training and to statically configure the filter settings.

3.6.1 25G TECHNOLOGY ABILITY

There is some overlap between the pre-standard 25G Ethernet Consortium ("25G & 50G Specification") and IEEE 802.3. The LAN8042 supports ANEG for 25G and FEC as specified by IEEE by using the DME base page, as well as supporting ANEG for 25G and FEC using the Next Page for Extended Technologies as specified by the 25G Ethernet Consortium.

3.7 MACsec Operation

FIGURE 3-13: MACSEC ARCHITECTURE



The MACsec architecture is shown in Figure 3-13 and consists of:

- A Line-facing MAC (Line MAC) and a Host-facing MAC (Host MAC).
  - When MACsec is enabled, the MACs are required to terminate and convert the PHY-layer 25/X GMII bus into a packet bus for use by the MACsec Crypto. MAC operation is described in Section 3.2.7.
  - The Host MAC also generates the Ingress MACsec Host Formats (L2H direction) and processes the Egress MACsec Host Formats (H2L direction). MACsec Host Formats are described in Section 3.7.5 below.
- A MACsec Crypto providing MAC-layer security services toward the Line Port.
  - Line Port frames are secured by MACsec, Host Port frames are unsecured.
  - MACsec Crypto operation is described in Section 3.7.1 below.
- A Flow Control Buffer.
  - When enabled, the Egress FC Buffer absorbs the frame expansion created by the MACsec Crypto Engine inserting extra bytes, and uses XON/XOFF flow control toward the Host Port to maintain full bandwidth

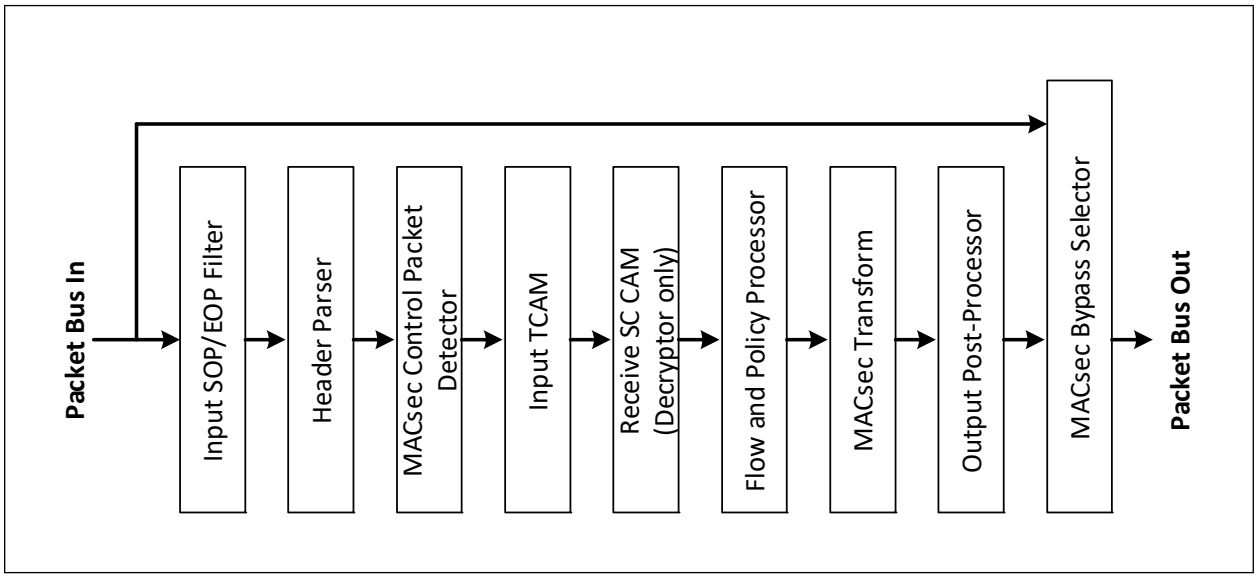
throughput toward the Line Port.

- The Ingress FC Buffer enables insertion of XON/XOFF PAUSE frames toward the Host Port. Interframe Gap (IFG) can be reduced toward the Host if needed to compensate for PAUSE frame insertion.
- FC Buffer operation is described in Section 3.2.8.

3.7.1 MACSEC CRYPTO

The MACsec Crypto is shown in Figure 3-14. It provides multi-stage processing as described below.

FIGURE 3-14: MACSEC CRYPTO



MACsec Encryptor (Egress / H2L) and Decryptor (Ingress / L2H) operations are identical except for a few situations mentioned in the following sections.

Note on MACsec padding and depadding operations:

If the unencrypted frame already contains Ethernet padding prior to MACsec Encryptor processing, the MACsec Encryptor is unaware of the padding and so this padding is encrypted/protected by MACsec and the ICV is appended after the padding.

When this frame is decrypted, the MACsec Decryptor is still unaware of this padding and the decrypted frame with padding will be output.

However if the unencrypted frame is shorter than the legal Ethernet frame size, the MACsec Encryptor will add padding and indicate the original frame size using the Short Length (SL) field in the SecTAG. In this case the ICV is appended to the short frame and any padding is appended AFTER the ICV.

When this frame is decrypted, the SL field is used by the Decryptor to locate the ICV. The Decryptor removes the padding and outputs the (short) decrypted frame. These short frames are padded to minimum size by the Host MAC.

These padding/depadding actions are only applicable to frames which are processed for MACsec, and do not apply to frames which bypass MACsec processing.

Note on MACsec drop/discard operations

Since the MACsec Crypto operates in cut-through mode, the first output data word of a frame typically leaves the MACsec Crypto before the last input data word of a frame enters, and errors such as ICV check verification or MTU checking may only be detected after the last byte of frame data has been processed. Consequently, dropping a frame is accomplished by corrupting the frame CRC.

The MACsec Crypto can also be programmed to drop frames completely (internal drop), but only if the decision to drop has been made by the flow lookup stage.

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3.7.1.1 Input SOP / EOP Filter

The Input SOP / EOP Filter stage ensures that only the valid sequence of SOP/EOP and in case of preemption (SOF/EOF) is passed to the rest of the MACsec Crypto. The filter tracks the sequence and in case of anomalies detected, it injects "dummy" words to complete unfinished sequences.

3.7.1.2 Header Parser

The Header Parser stage performs the following functions:

- Parses the arriving frame and extracts Ethernet, VLAN, MPLS, and SecTAG fields for classification.
  - MAC-DA, MAC-SA, and EtherType/Length are always extracted
  - Up to four VLAN tags can be identified based on the two standard TPIDs (S-tag and C-tag) and four configurable TPIDs
  - Up to five MPLS labels can be identified based on two standard MPLS EtherTypes and two configurable MPLS EtherTypes
  - MPLS parsing also accommodates Entropy Label Indicator (ELI), Entropy Label (EL), and Pseudowire Control Word (CW)
- SecTAG classification results in frames being categorized as one of:
  - Untagged. No SecTAG is found based on the standard SecTAG EtherType or the configurable SecTAG EtherType.
  - Bad Tag. An invalid SecTAG is found.
  - KaY Tag. The frame has a KaY tag, it will bypass MACsec processing.
  - Tagged. A valid non-KaY SecTAG was found.

3.7.1.3 MACsec Control Packet Detector

The MACsec Control Packet Detector stage consists of a configurable set of static match rules that can be enabled individually to the outer Ethernet header. Hitting any of these rules results in a frame to be considered as a MACsec Control Packet for all subsequent operations.

MACsec Control Packets can also be detected by the Input TCAM.

3.7.1.4 Input TCAM

The Input TCAM stage provides the vPort policy to use for the frame, as well as flags for forcing the frame to be dropped or considered a 'control' frame. The Secure Channel is also indicated, which can be overridden by the Receive SC CAM for cases with multiple SCs per vPort (Decryptor only).

If no entry in the input TCAM is hit, the frame is not matched to a vPort but is processed according to a set of non-match flows, which gives flexibility in configuring what to do with the frame. Typical system behavior would be to drop all frames that did not hit any entry in the input TCAM and did not hit any control packet matching rules.

3.7.1.5 Receive SC CAM

The Receive SC CAM stage only exists in the Decryptor, and is used for cases where multiple Rx Secure Channels map to the same vPort.

In the Encryptor, each vPort supports a single Tx Secure Channel. For the use case where multiple Tx Secure Channels map to the same SecY, a vPort per VLAN priority must be used.

3.7.1.6 Flow and Policy Processor

The Flow and Policy Processor is the final stage of the input classification module in which instructions for the frame transform are determined from all parsing and classification results collected so far. These instructions are given to the MACsec Transform stage.

3.7.1.7 MACsec Transform

The MACsec Transform stage carries out the actual frame transformation.

- For egress MACsec operations it inserts the SecTAG, optionally encrypts the payload data and appends the ICV.
- For ingress MACsec operations, it removes the SecTAG, optionally decrypts the payload data and removes (and validates) the ICV.

The MACsec Transform stage can detect several error conditions (like sequence number errors and authentication errors), which will cause the frame to be dropped by applying a flow-defined drop_action.

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3.7.1.8 Output Post-Processor

The Output Post-Processor is the final stage of the processing pipeline. It provides MTU checking (Encryptor only) and frame dropping due to error conditions detected by the MACsec Transform stage (such as sequence number rollover and authentication failure) and it updates all MACsec Statistics counters.

3.7.1.9 MACsec Bypass Selector

The MACsec Bypass Selector provides for a static bypass of the MACsec Crypto.

Note other bypass operations are configurable within the MACsec Crypto, such as for MACsec Control Packets.

3.7.1.10 MACsec Statistics

The MACsec Crypto implements several statistics counters groups. Statistics align with the 802.1AE-2018 standard unless otherwise noted.

- MACsec SA/SC statistics, counted per SA index
- MACsec SecY Global statistics counted per vPort index
- MACsec SecY Port statistics (counting MIB statistics for three MACsec ports of a SecY) counted per vPort index
- TCAM Hit counter per each TCAM entry
- MACsec Debug statistics

For SC statistics the host must accumulate SA counters.

TABLE 3-3: MACSEC SA/SC STATISTICS

Name	Direction	Scope	Comments
OutOctetsEncrypted/ OutOctetsProtected	Egress	Per-SA	Host to split the counters
OutPktsEncrypted/ OutPktsProtected.	Egress	Per-SA	Host to split the counters
OutPktsTooLong	Egress	Per-SA	Packets failing MTU check
OutPktSANotInUse	Egress	Per-SA	Packets with SA not in use (not a standard counter)
InOctetsDecrypted	Ingress	Per-SA	
InOctetsValidated	Ingress	Per-SA	
InPktsUnchecked	Ingress	Per-SA	
InPktsDelayed	Ingress	Per-SA	
InPktsLate	Ingress	Per-SA	
InPktsOk	Ingress	Per-SA	
InPktsInvalid	Ingress	Per-SA	
InPktsNotValid	Ingress	Per-SA	
InPktsNotUsingSA	Ingress	Per-SA	
InPktsUnusedSA	Ingress	Per-SA	

TABLE 3-4: MACSEC SECY GLOBAL STATISTICS

Name	Direction	Scope	Comments
TransformErrorPkts	Egress	SecY	
OutPktsCtrl	Egress	SecY	
OutPktsUntagged	Egress	SecY	
TransformErrorPkts	Ingress	SecY	
InPktsCtrl	Ingress	SecY	
InPktsUntagged	Ingress	SecY	
InPktsNoTag	Ingress	SecY	

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TABLE 3-4: MACSEC SECY GLOBAL STATISTICS (CONTINUED)

Name	Direction	Scope	Comments
InPktsBadTag	Ingress	SecY	
InPktsNoSCI	Ingress	SecY	
InPktsUnknownSCI	Ingress	SecY	
InPktsTaggedCtrl	Ingress	SecY	

TABLE 3-5: MACSEC SECY PORT STATISTICS

Name	Direction	Scope	Comments
ifOutOctetsCommon	Egress	SecY	
ifOutOctetsUncontrolled	Egress	SecY	
ifOutOctetsControlled	Egress	SecY	
ifOutUcastPktsUncontrolled	Egress	SecY	
ifOutMcastPktsUncontrolled	Egress	SecY	
ifOutBcastPktsUncontrolled	Egress	SecY	
ifOutUcastPktsControlled	Egress	SecY	
ifOutMcastPktsControlled	Egress	SecY	
ifOutBcastPktsControlled	Egress	SecY	
ifInOctetsUncontrolled	Ingress	SecY	
ifInOctetsControlled	Ingress	SecY	
ifInUcastPktsUncontrolled	Ingress	SecY	
ifInMcastPktsUncontrolled	Ingress	SecY	
ifInBcastPktsUncontrolled	Ingress	SecY	
ifInUcastPktsControlled	Ingress	SecY	
ifInMcastPktsControlled	Ingress	SecY	
ifInBcastPktsControlled	Ingress	SecY	

TABLE 3-6: TCAM HIT STATISTICS

Name	Direction	Scope	Comments
TCAMHit	Ingress/Egress	Per-Rule	Number of Input TCAM hits
RxCAMHit	Ingress	Per-Rules	Number of Rx SC CAM hits

TABLE 3-7: MACSEC DEBUG STATISTICS

Name	Direction	Scope	Comments
TCAMMiss	Ingress/Egress	Global	Number of frames that missed the TCAM
TCAMHitMultiple	Ingress/Egress	Global	Number of frames that hit multiple TCAM entries simultaneously
HeaderParserDroppedPkts	Ingress/Egress	Global	Frames dropped by header parser as invalid (e.g. # runt frames received

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3.7.2 MACSEC CAPTURE FIFO

A 512-Byte Capture FIFO is provided which can capture up to the first 504 bytes for packets failing any security check.

The security fail event can be used as a trigger. The FIFO can also be enabled to capture the first packet on any given SA. Multiple packets can also be captured in this FIFO.

H2L frames are captured after MACsec encryption. L2H frames are captured after MACsec decryption.

3.7.3 DEBUG FAULT CODE IN CRC

Each ingress or egress frame failing security check will have its CRC corrupted. As described in Section 3.2.7.3, two CRC corruption options are supported:

- CRC inversion
- CRC with Debug Code

This section describes the Debug Code, which uses 31 of the 32 available CRC bits. The 32nd CRC bit is reserved to make sure the CRC fails (to prevent the Debug Code from accidentally passing the CRC test).

The Debug Code is described in the following table:

TABLE 3-8: CRC TEST DEBUG CODES

CRC[31:0] bit	Egress / H2L Fault Code	Ingress / L2H Fault Code
31	Reserved to ensure the CRS fails	
30	1 = Valid SA hit	
29:23	the SA which was hit, valid when CRC[30]=1	
22	Unused=0	InPktsUnusedSA
21	Unused=0	InPktsNotUsingSA
20	Unused=0	InPktsNotValid
19	Unused=0	InPktsInvalid
18	Unused=0	InPktsOk
17	OutPktSANotInUse	InPktsLate
16	OutPktsTooLong	InPktsDelayed
15	OutPktsEncrypted	OutPktsProtected
14	Unused=0	InPktsTaggedCtrl
13	Unused=0	InPktsUnknownSCI
12	Unused=0	InPktsNoSCI
11	Unused=0	InPktsBadTag
10	OutPktsUntagged	InPktsNoTag InPktsUntagged
9	OutPktsCtrl	InPktsCtrl
8	TransformErrorPkts	TransformErrorPkts
7	IfOutPktsControlled	IfOutPktsControlled
6	IfOutPktsUncontrolled	IfOutPktsUncontrolled
5	HeaderParserDroppedPkts	HeaderParserDroppedPkts
4	TCAMHitMultiple	TCAMHitMultiple
3	TCAMMiss	TCAMMiss
2	pkt_tx_sec_fail	pkt_tx_sec_fail
1	pkt_tx_min_frag_err	pkt_tx_min_frag_err
0	Unused=0	pkt_tx_split_tag_sc_err

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3.7.4 MACSEC FRAME ENCAPSULATIONS AND TRANSFORMS

The left side of Table 3-9 lists the unencrypted frame encapsulations supported by the MACsec Crypto, and the right side of the table lists the set of possible transformations into encrypted / authenticated frames.

Specific Ingress and Egress Host Formats are described in the following sections.

TABLE 3-9: MACsec FORMATS AND TRANSFORMS

Unencrypted Frame Format Passed Across the Host Interface		Resulting Encrypted / Authenticated Frame Format(s) On the Line Interface	
Outer Encaps	**Inner Encaps**	**SecTAG Supported Locations**	**ICV Coverage**
Ethernet: 0 VLAN tags	N/A	After MAC-SA (standard)	MAC-DA to ICV
Ethernet: 1 VLAN tag	N/A	After MAC-SA (standard) After VLAN tag (1 tag bypass)	MAC-DA to ICV MAC-DA to ICV except bypassed tag
Ethernet: 2 VLAN tags	N/A	After MAC-SA (standard) After 1st VLAN tag (1 tag bypass) After 2nd VLAN tag (2 tag bypass)	MAC-DA to ICV MAC-DA to ICV except bypassed tag MAC-DA to ICV except bypassed tags
Ethernet: 3 VLAN tags	N/A	After MAC-SA (standard) After 1st VLAN tag (1 tag bypass) After 2nd VLAN tag (2 tag bypass) After 3rd VLAN tag (3 tag bypass)	MAC-DA to ICV MAC-DA to ICV except bypassed tag MAC-DA to ICV except bypassed tags MAC-DA to ICV except bypassed tags
Ethernet: 4 VLAN tags	N/A	After MAC-SA (standard) After 1st VLAN tag (1 tag bypass) After 2nd VLAN tag (2 tag bypass) After 3rd VLAN tag (3 tag bypass) After 4th VLAN tag (4 tag bypass)	MAC-DA to ICV MAC-DA to ICV except bypassed tag MAC-DA to ICV except bypassed tags MAC-DA to ICV except bypassed tags MAC-DA to ICV except bypassed tags

TABLE 3-9: MACsec FORMATS AND TRANSFORMS (CONTINUED)

Unencrypted Frame Format Passed Across the Host Interface		Resulting Encrypted / Authenticated Frame Format(s) On the Line Interface	
Outer Encaps	**Inner Encaps**	**SecTAG Supported Locations**	**ICV Coverage**
EoMPLS[1]: Between 1 and 5 MPLS Labels	Ethernet: 0 tags	After Outer MAC-SA (standard) After Inner MAC-SA (~standard[2])	Outer MAC-DA to ICV Inner MAC-DA to ICV
	Ethernet: 1 tag	After Outer MAC-SA (standard) After Inner MAC-SA (~standard[2]) After Inner 1st VLAN tag (1 inner tag bypass)	Outer MAC-DA to ICV Inner MAC-DA to ICV Inner MAC-DA to ICV except bypassed inner tag
	Ethernet: 2 tags	After Outer MAC-SA (standard) After Inner MAC-SA (~standard[2]) After Inner 1st VLAN tag (1 inner tag bypass) After Inner 2nd VLAN tag (2 inner tag bypass)	Outer MAC-DA to ICV Inner MAC-DA to ICV Inner MAC-DA to ICV except bypassed inner tag Inner MAC-DA to ICV except bypassed inner tags

1: Ethernet over MPLS: outer encapsulation is untagged Ethernet with the indicated number of MPLS labels, plus an optional Pseudowire control word.

2: This is not explicitly specified in the MACsec standard. But it is the result of transporting a standard MACsec-formatted Ethernet frame over a standard MPLS tunnel.

3.7.4.1 MACsec Line Formats

- Line Interface format options include:
- Location of SecTAG and ICV coverage is seen in Table 3-9.
- The maximum offset to the start of the SecTAG is 58 bytes, which is for the EoMPLS case with 5 MPLS labels, a pseudowire control word, and two inner VLAN tags being bypassed.
- Standard option to encrypt the frame payload beginning with the byte after SecTAG and ending with the byte before ICV.
- Confidentiality Offset option to encrypt the frame payload beginning N bytes after the SecTAG and ending with the byte before ICV. N can be up to 128. Confidentiality Offset allows for N bytes to be visible to the network (unencrypted) but still authenticated.
- Option to not encrypt any frame payload. Note if the frame is not encrypted it is not confidential / private (any outsider can read the contents), but it is still authenticated by the ICV (any outsider modification are detected and rejected by MACsec).
- Unfragmented E-frames, unfragmented P-frames and fragmented P-frames are all supported.

3.7.5 MACSEC HOST FORMATS

The LAN8042 supports a variety of formats on the Host Ports to simplify system MACsec operation. These formats provide:

- Multiple Egress / H2L approaches to handling the frame expansion introduced in the PHY due to MACsec adding SecTAG and ICV to departing frames. A range of options is provided from very simple (use of Pause to the Host) to options which do not disturb any time-critical TSN scheduling by the Host.
- Multiple Ingress / L2H approaches to handling frame preemption fragment reduction introduced in the PHY due to MACsec removing SecTAG and ICV from arriving frames. Again a range of options is provided depending on the

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needs of the Host.

3.7.5.1 MACsec Egress Host Formats

MACsec egress processing adds a SecTAG (8 bytes or 16 bytes) and an ICV (16 bytes) to every applicable Ethernet frame. Even though the Line Port TXOUT bandwidth can be maintained at 100%, this "bandwidth expansion" in the PHY means the Host Port TXIN bandwidth must be reduced by some amount to not overrun the PHY.

The LAN8042 provides three MACsec Egress Host Formats to provide options to the Host for managing this bandwidth expansion. All frames which will have MACsec applied must use the same Egress Host Format on a given Host Interface.

These formats are mostly independent of the unencrypted encapsulations shown in Table 3-9. Each Egress Host Format supports all unencrypted encapsulations in Table 3-9, noting that Egress Host Formats 1 and 2 require the complete SecTAG to exist in the first frame fragment which in some configurations might limit the maximum encapsulation depth.

1. Egress Host Format 0

   This is the legacy format where the unencrypted frame arrives at the LAN8042 across the Host Port with no special modifications for MACsec. To manage MACsec bandwidth expansion the Host must either:

   - Extend the InterFrame Gap ("IFG Extend") by at least the number of expansion bytes (24 bytes or 32 bytes depending on SecTAG size)
   - Make use of the Egress Flow Control Buffer feature and rely on LAN8042-generated Pause frames across the Host Port to regulate the bandwidth.

2. Egress Host Format 1

   This format requires the Host to insert Dummy SecTAG and Dummy ICV bytes of the same size and in the same location as the real SecTAG and ICV will appear on the Line Port. The MACsec Encryptor overwrites these Dummy bytes with real SecTAG and ICV, resulting in a TSN-friendly constant delay encryption process.

3. Egress Host Format 2

   This format allows the Host to insert a Dummy SecTAG in the front of the frame, and either use IFG Extend or Pause flow control to account for the 16 bytes of ICV expansion. This format exists to support Hosts which cannot easily add bytes to the end of a frame.

The three MACsec Egress Host Formats are summarized in Table 3-10, and described in more detail in the following sections.

TABLE 3-10: MACSEC EGRESS HOST FORMATS

Format	Dummy SecTAG	Dummy ICV	Frame Expansion due to MACsec SecTAG=8B/16B ICV=16B	Comments
0	No	No	24B/32B	Requires IFG Extend or Egress FC Buffer Pause.
1	Yes	Yes	0B	No Frame Expansion Host to Line
2	Yes	No	16B	Requires IFG Extend or Egress FC Buffer Pause.

3.7.5.1.1 MACsec Egress Host Format 0

Egress Host Format 0 with fragmentation disabled is the legacy format supported by previous Microchip MACsec PHYs. In this format, each MACsec-transformed frame grows in size by either 24 or 32 bytes.

Two methods exist to prevent dropping egress frames due to the frame size expansion:

1. The Egress FC Buffers will generate Pause toward the Host to throttle the rate down as it's filling. Note this creates a very large variable latency through the LAN8042, which may be undesirable for TSN operation.
2. If supported in the Host a better option is to extend the inter-frame gap (IFG) to accommodate the 24 or 32 bytes of frame expansion. This removes the variable latency and is more suitable for TSN operation, although it may also prevent the egress line from reaching 100% utilization depending on how precisely the Host can control IFG for non-MACsec frames and fragmented p-frames (if frame pre-emption is enabled).

With frame preemption enabled, LAN8042 provides two options for applying the frame growth to fragmented frames:

1. EOP-only growth option enabled: The EOP fragment size changes by the full 24 or 32 bytes, and all other fragment sizes are unchanged.

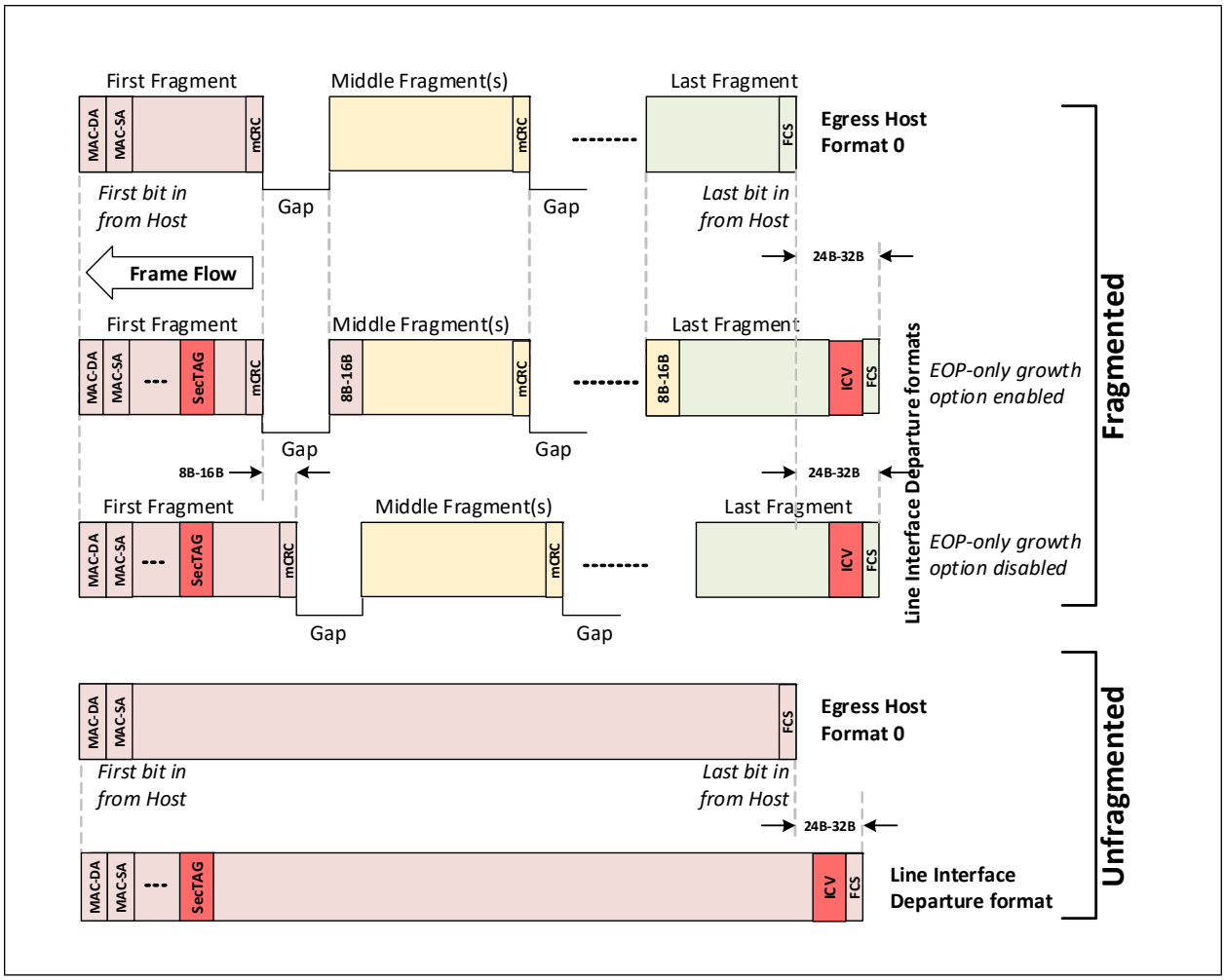
- Since non-final fragments are not expanded, there is no delay to any e-frames preempting this p-frame, although all subsequent frames are delayed by the frame size change.
- If decrypted by a MACsec PHY (e.g. LAN8042) or for a port loopback test, the post-decryption SOP and EOP fragment sizes will be different from the pre-encryption SOP and EOP fragment sizes. While this is legal and should be handled cleanly, the option to disable EOP-only growth exists in case this causes issues.

2. EOP-only growth option disabled: The SOP fragment size changes by 8 or 16 bytes due to SecTAG insertion, and the EOP fragment size changes by 16 bytes due to ICV insertion.
   - Any e-frames preempting this p-frame are delayed by the SecTAG insertion.
   - If decrypted by a MACsec PHY (e.g. LAN8042) or for a port loopback test, the post-decryption fragment sizes are identical to the pre-encryption fragment sizes.

Note in Egress Host Format 0 the SecTAG is allowed to span the first and second fragment of a fragmented frame, depending on first fragment size, encapsulation size, and SecTAG size. This can only occur for very deep EoMPLS encapsulations.

Figure 3-15 illustrates operation with Egress Host Format 0, showing both an unfragmented frame and also a fragmented frame.

FIGURE 3-15: MACSEC EGRESS HOST FORMAT 0



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3.7.5.1.2 MACsec Egress Host Formats 1 and 2

Egress Host Formats 1 and 2 require the Host to insert Dummy SecTAG and/or Dummy ICV bytes into the packet. These bytes are overwritten by the MACsec Encryptor so no frame expansion takes place where the dummy bytes are used.

Egress Host Format 1 is ideal if the Host can support it. There is no frame expansion at all, and IFG Extend is not required so the egress line can reach 100% utilization.

- Dummy SecTAG is always inserted immediately behind MAC-SA, Dummy ICV is always inserted immediately before FCS.

Egress Host Format 2 targets a Host which can only insert dummy bytes near the front of the frame. Note the frame expansion is less than in Egress Host Format 0, and also Egress Host Format 2 can be used in combination with a smaller value of IFG Extend than Egress Host Format 0.

- Dummy SecTAG is always inserted immediately behind MAC-SA.

Note in both Egress Host Formats 1 and 2 the SecTAG must be fully within the first fragment.

Figure 3-16 illustrates operation with Egress Host Format 1, showing both an unfragmented frame and also a fragmented frame.

FIGURE 3-16: MACSEC EGRESS HOST FORMAT 1

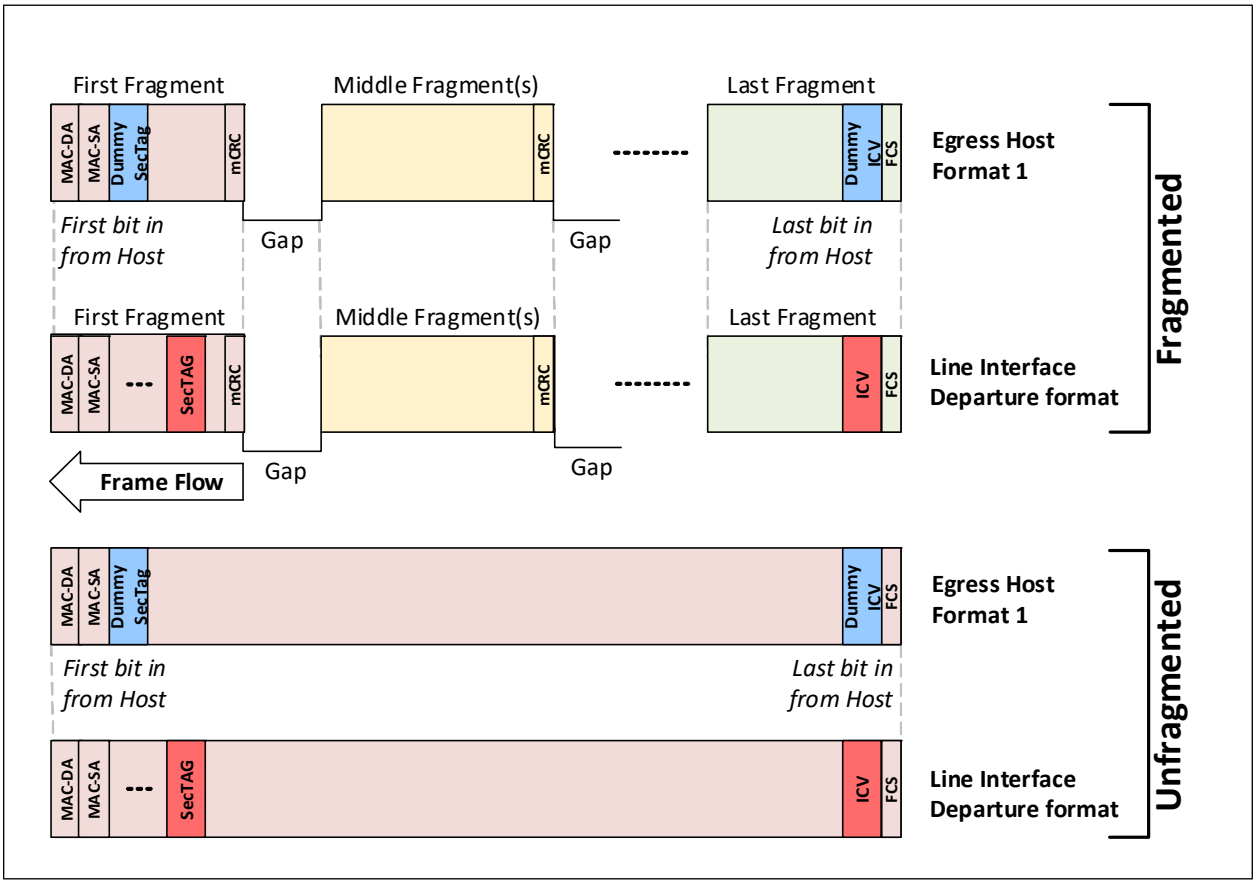
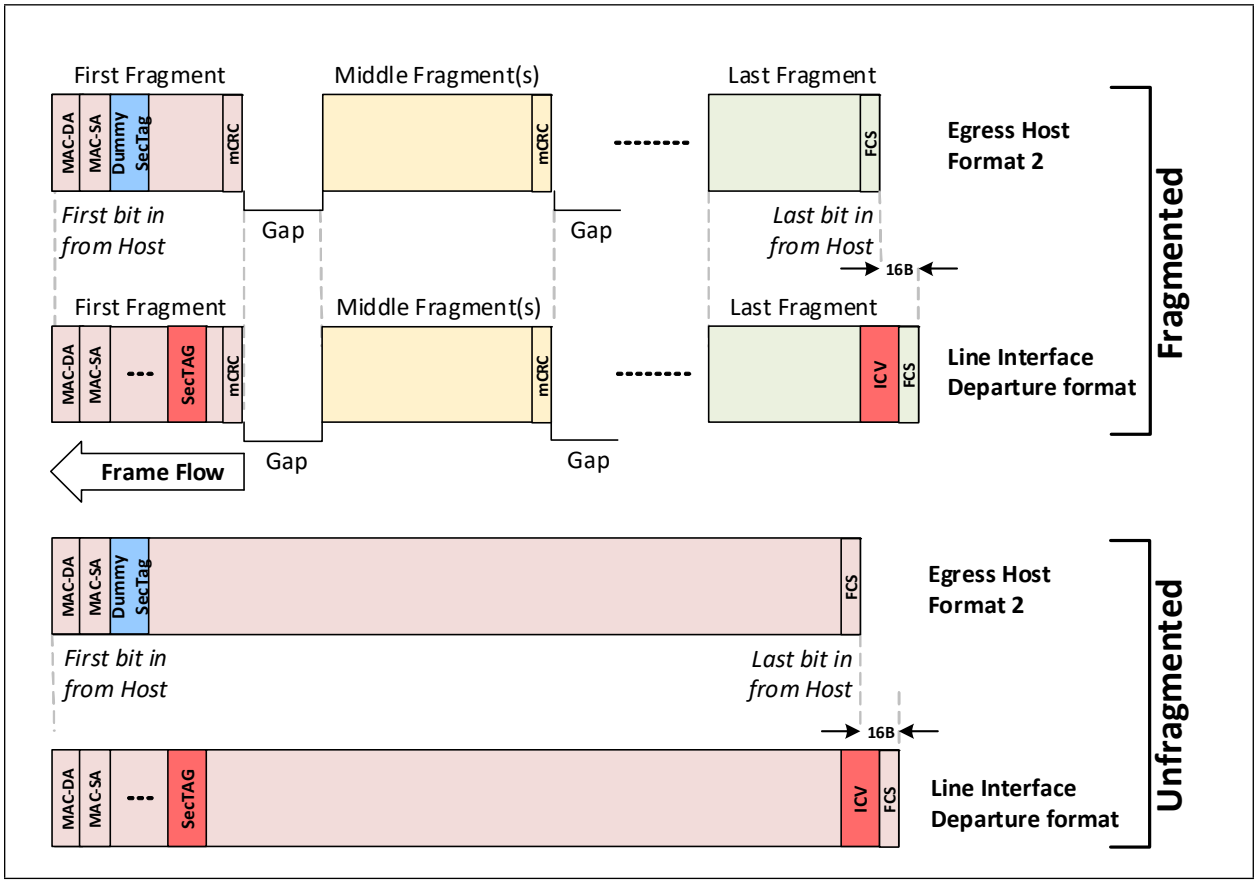


Figure 3-17 illustrates operation with Egress Host Format 2, showing both an unfragmented frame and also a fragmented frame.

FIGURE 3-17: MACSEC EGRESS HOST FORMAT 2



3.7.5.1.3 MACsec Ingress Host Formats

MACsec ingress processing removes a SecTAG (8 bytes or 16 bytes) and an ICV (16 bytes) from every applicable Ethernet frame. For unfragmented frames this is not an issue, but for fragmented frames this can create illegal (too small) fragments toward the Host MAC and Host Port.

The LAN8042 provides four MACsec Ingress Host Formats to provide options to the Host for managing small fragments. All frames which have had MACsec applied must use the same Ingress Host Format on a given Host Interface.

These formats are fully independent of the unencrypted encapsulations shown in Table 3-11. Each Ingress Host Format supports all unencrypted encapsulations in Table 3-11.

Ingress Host Format 0

This format provides the expected unencrypted frame (both SecTAG and ICV are removed) with no special format for MACsec. It is the recommended format when frame preemption is disabled.

This format is not recommended when frame preemption is enabled, due to possibility of creating illegal (too small) fragments when removing SecTAG and ICV.

Ingress Host Format 1

This format retains both SecTAG and ICV, so is able to be used when frame preemption is enabled or disabled. The Host must locate and remove the SecTAG and ICV when using this format.

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Ingress Host Format 2

This format replaces the SecTAG and ICV with user defined Dummy SecTAG and ICV bytes. Using a "byte rippling" approach, the Dummy SecTAG and ICV bytes are moved to a fixed position in the front of the frame to simplify Host removal of these bytes.

The frame size and fragment sizes are unchanged with this format, and it is able to be used when frame preemption is enabled or disabled. MACsec-related Host processing of ingress frames is simplified compared to Ingress Format 1.

Ingress Host Format 3

This format provides the expected unencrypted frame (both SecTAG and ICV are removed) with no special format for MACsec. In addition, it uses the "byte rippling" approach on fragmented frames. So long as non-final fragments are configured to be at least 128 bytes including mCRC (by setting addFragSize to any value greater than 0), the removal of SecTAG and ICV will not create illegal (too small) fragments.

This format is recommended when frame preemption is enabled and addFragSize is greater than 0, as there is no required MACsec-related Host processing of ingress frames.

The four MACsec Ingress Host Formats are summarized in Table 3-11, and described in more detail in the following sections.

TABLE 3-11: MACSEC INGRESS HOST FORMATS

Format	SecTAG and ICV Handling	Byte Rippling on Frame Fragments	Frame Reduction due to MACsec SecTAG=8B/16B ICV=16B	Comments
0	Remove both ICV and SecTAG	No	24B/32B	Not recommended when Frame Preemption is enabled
1	Retain both ICV and SecTAG	No	0B	
2	Replace both ICV and SecTAG with Dummy ICV and Dummy SecTAG	Yes	0B	
3	Remove both ICV and SecTAG	Yes	24B/32B	Recommended when Frame Preemption is enabled and addFragSize is greater than 0 (minimum non-final fragment size is at least 128 bytes)

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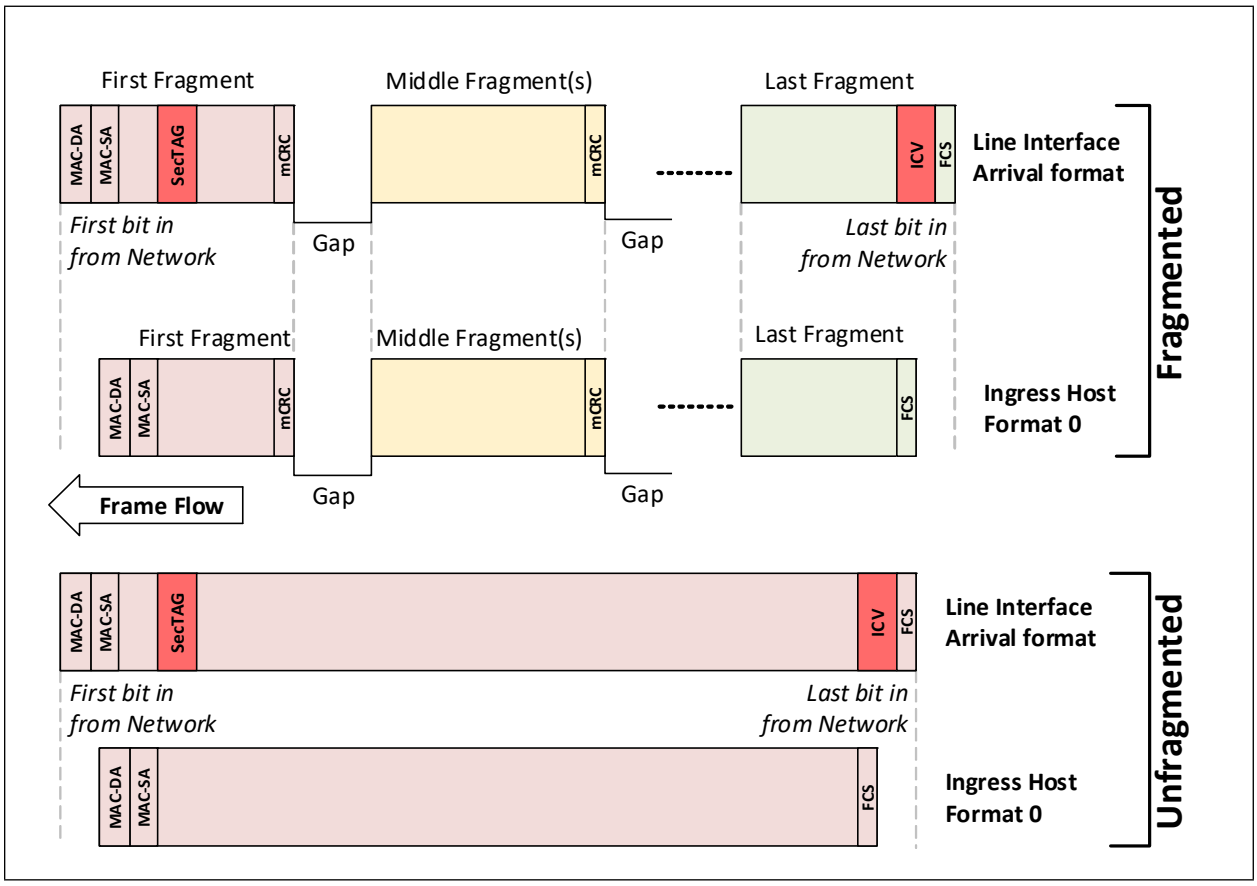
3.7.5.1.4 MACsec Ingress Host Format 0

Ingress Host Format 0 with fragmentation disabled is the first of two legacy formats supported by previous Microchip MACsec PHYs. In this format, each MACsec-transformed frame shrinks in size by either 24 or 32 bytes. Unfragmented frames are padded if necessary to get back to the minimum required 64 byte size, as per IEEE 802.3.

Ingress Host Format 0 should not be used with fragmentation enabled.

FIGURE 3-18: MACSEC INGRESS HOST FORMAT 0



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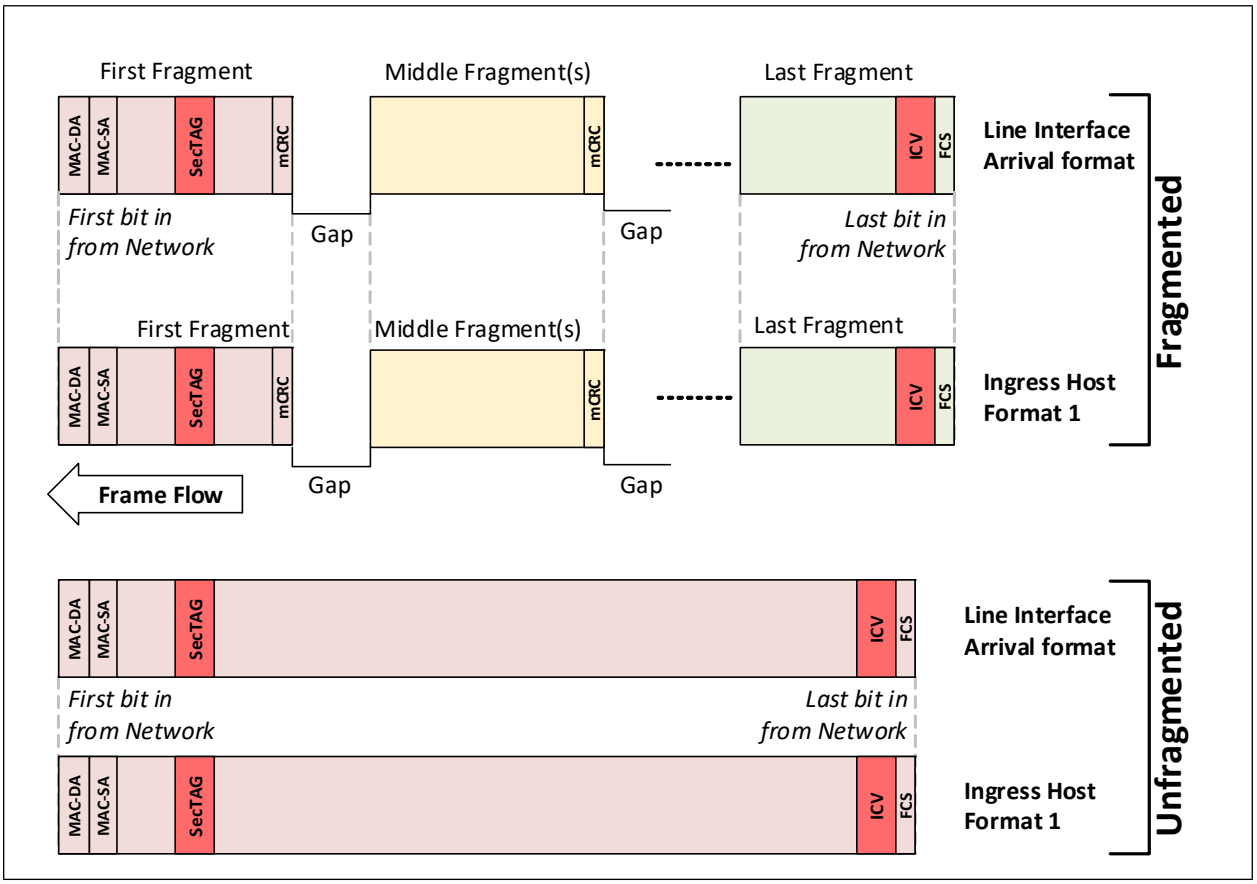
3.7.5.1.5 MACsec Ingress Host Format 1

Ingress Host Format 1 with fragmentation disabled is the second of two legacy formats supported by previous Microchip MACsec PHYs. In this format, there is no frame size change due to MACsec. Ingress Host Format 1 also works with fragmentation enabled or disabled.

Ingress Host Format 1 requires the Host to be capable of locating and removing both the SecTAG and ICV, which is not typically expected of Hosts. Note the MACsec Crypto can overwrite SecTAG in addition to retaining it.

FIGURE 3-19: MACSEC INGRESS HOST FORMAT 1



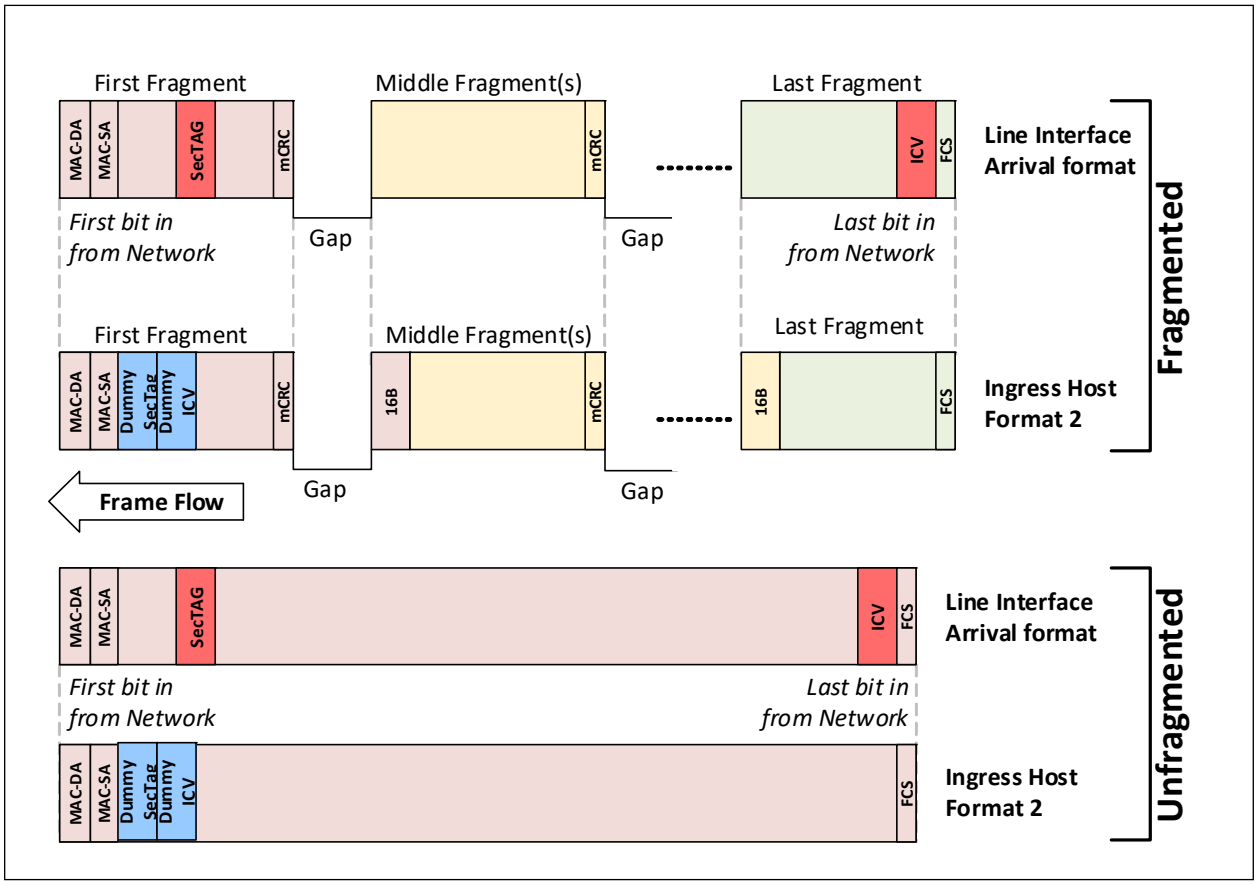
3.7.5.1.6 MACsec Ingress Host Format 2

Ingress Host Format 2 removes the SecTAG and ICV, then inserts a Dummy SecTAG and Dummy ICV. The Dummy SecTAG is located immediately after the MAC-SA and the Dummy ICV is located immediately after the Dummy SecTAG.

Byte Rippling is used to maintain the fragment sizes of the original frame as received on the Line Port. The result is that the Host only needs to remove bytes from the front of the frame, which is commonly supported in many Hosts. Note the overall frame size, and the size of all fragments, are all unchanged due to this operation.

Figure 3-20 shows frame arrival format from the Line Port on top, with Ingress Host Format 2 departure to the Host Port:

FIGURE 3-20: MACSEC INGRESS HOST FORMAT 2



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3.7.5.1.7 MACsec Ingress Host Format 3

Ingress Host Format 3 removes the SecTAG and ICV, but does not insert any Dummy SecTAG or Dummy ICV. Byte Rippling is used to maintain the fragment sizes of the original frame as received on the Line Port, except for the first fragment which will be smaller by the amount of SecTAG+ICV bytes. For unfragmented frames, the MAC may need to pad small frames to the minimum legal size of 64 bytes.

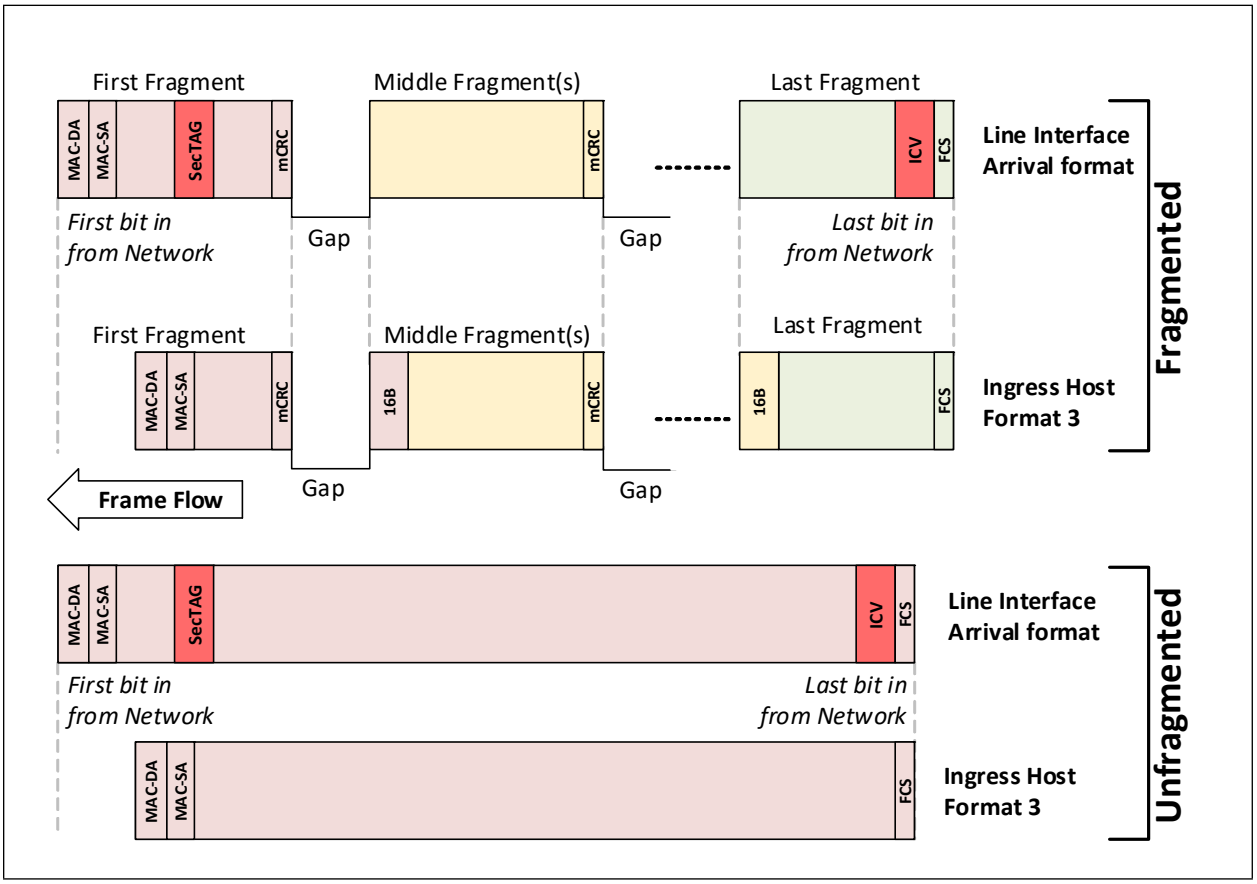
Ingress Host Format 3 cannot be used when the minimum non-final fragment size of 64 bytes is configured (addFrag-Size=0). It can be used with any larger minimum non-final fragment size (addFragSize greater than 0), noting that the first fragment size (internal between LAN8042 and Host) may be unexpectedly small but is legal.

The very significant advantage of Ingress Host Format 3 is the Host has no MACsec bytes to locate and remove.

Figure 3-21 shows frame arrival format from the Line Port on top, with Ingress Host Format 3 departure to the Host Port.

The overall frame size and first fragment size are reduced by 24 or 32 bytes, and all other fragment sizes do not change.

FIGURE 3-21: MACSEC INGRESS HOST FORMAT 3



3.8 Clocking

3.8.1 DATA PATH CLOCKING

Each slice data path Tx and Rx clocks are generated by that slice's SerDes CMU. Tx datapath clocks are generated from the 156.25 MHz SYSREFCK and are frequency synchronous across all slices. Rx datapath clocks are recovered from the Rx serial datastream and may be frequency asynchronous to other clocks.

Loop timing of a port (using the receive clock as the transmit clock) is not supported.

3.8.2 SYSTEM CLOCK GENERATION

The following internal chip clocks are generated by the System PLL which uses the 156.25 MHz SYSREFCK as reference:

- 300 MHz for SPI, MDIO, and internal CSR register logic

- 300 MHz for TWI Host

3.8.3 SYNCHRONOUS ETHERNET AND RECOVERED CLOCKS

The LAN8042 supports Synchronous Ethernet as specified by ITU-T G.8261 is supported in LAN8042 as described below. A system with LAN8042 may support Synchronous Ethernet only.

Table 3-12 illustrates a system using LAN8042 to support Synchronous Ethernet. Typical requirements include:

- Ability to select any Line Port recovered clock as the Primary timing reference. The LAN8042 RCKOUTA can be used for this purpose.
- Ability to select any Line Port recovered clock as the Secondary timing reference. The LAN8042 RCKOUTB can be used for this purpose.
- Ability to use a local high-quality oscillator as the Primary, Secondary or Hold-over timing reference. The OCXO provides this function in this example. OCXO specifics are out of scope for this example.
- The selected timing reference must be qualified and cleaned up by the DPLL, which also may perform timing failover and frequency conversion functions. DPLL specifics are out of scope for this example.
- All Line Ports will use the DPLL output as their reference timing. This becomes the 156.25MHz SYSREFCK input into the LAN8042.

The LAN8042 provides two Recovered Clock outputs supporting the following capabilities:

- Each output is selectable to provide the recovered clock from any LAN8042 Line Port
- Each output has a configurable divider which can provide frequencies per Table 3-12
- Each output has a Squelch function, where the output is disabled for Line Port fault conditions. Squelching the clock immediately in hardware can be used to achieve faster timing failover. Note that when squelched, the recovered clocks can stop either high or low. Clock Squelch can also be disabled.
  The applicable fault conditions are:
  - Link Down (condition can be ignored by setting PCS_LINK_STS_SQUELCH_ENA=0)
  - Loss of Signal (LOS) (condition can be ignored by setting SD_LOS_SQUELCH_ENA=0)
  - Link is in the Training state (condition is always applicable)

TABLE 3-12: RECOVERED CLOCK OUTPUT FREQUENCIES

Port Speed	Recovered Clock Frequency	Recovered Clock Output Divider	Recovered Clock Output Frequency
1G	125.00 MHz	1	125
		2	62.5
		4	31.25
		8	15.625
10G	257.8125 MHz	1	Not Available
		2	128.90625
		4	64.453125
		8	32.2265625
25G	644.53125 MHz	1	Not Available
		2	Not Available
		4	Not Available
		8	80.56640625

3.9 Device Management

3.9.1 SPI CLIENT INTERFACE

LAN8042 supports the SPI Client interface as a high bandwidth interface for MACsec key and classification updates. The SPI interface is also capable of accessing the entire status and configuration register space. The SPI Client interface consists of the SPI_CLIENT_SCK serial clock input, the SPI_CLIENT_MOSI data input, the SPI_CLIENT_MISO data output and the SPI_CLIENT_SSN input (active low).The SPI Client interface is implemented as a pipeline system,

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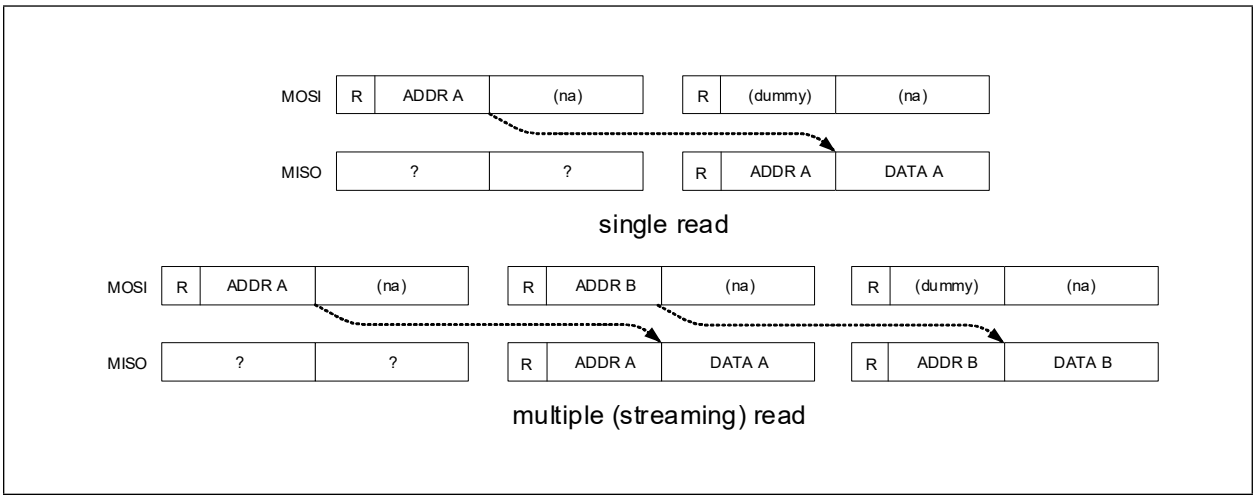
addressing the bandwidth requirement for writing MACsec keys as well as FIFO registers. As such, the data read back during any READ transaction is the value request from the previous transaction. To illustrate, single and multi-register reads would look like Figure 3-22.

FIGURE 3-22: SPI CLIENT PIPELINED READS



From a software perspective, a read of a single address would have to actually do two SPI reads. However, for streaming out many registers at once, the interface is using the full bandwidth while retaining random access.

SPI instruction consists of a 56-bit format as shown in Table 3-13:

TABLE 3-13: SPI CLIENT INSTRUCTION FORMAT

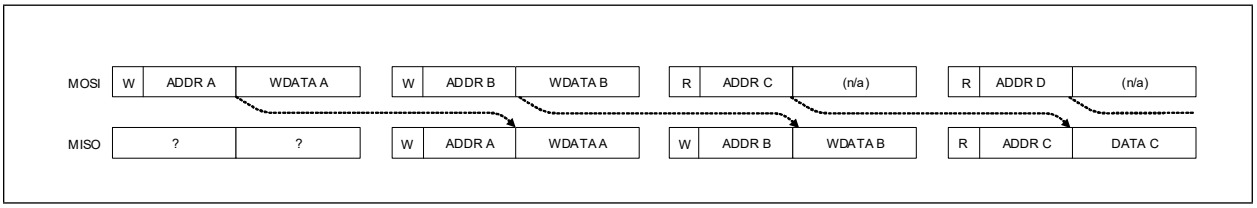
Bit	Name	Description
55	Read/Write	1 = Write, 0 = Read
54:53	Slice Number	0 = Slice 1 1 = Slice 2 2 = Slice 3 3 = Slice 4
52:48	Device Number	5 bits for devices 1 - 31
47:32	Address	16 bits Register access
31:0	Data	32 bits

APPLICATION NOTE: When accessing FIFOs or other change on read registers, either singly or streaming, care must be taken to not inadvertently perform an excess read during the second / final phase of the pipeline access. For example the dummy address should not access a FIFO or change on read register. A safe dummy address would be that of the Device_ID register in the GLOBAL target (device 0x1E).

Writes happen at the end of the command (they are not pipelined).

The read-back data of the transaction following a write is the last write parameters.

FIGURE 3-23: SPI CLIENT PIPELINED WRITES FOLLOWED BY READS



3.9.2 MANAGEMENT DATA INPUT/OUTPUT (MDIO) INTERFACE

LAN8042 supports the Management Data Input/Output (MDIO) Interface as a low to medium bandwidth interface for basic PHY management.

APPLICATION NOTE: Although the Management Data Input/Output (MDIO) Interface can access the entire status and configuration register space, due to its slow bandwidth and high latency, the Management Data Input/Output (MDIO) Interface is not recommended as the only interface to access the device.

LAN8042 supports the Management Data Input/Output (MDIO) Interface as defined clause 45 of the IEEE 802.3 Ethernet specification. The Management Data Input/Output (MDIO) Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC).

The base port address is determined by the PADDR inputs and can be any value from 0 to 28 for quad Slice devices. Each Slice is addressed at an offset from the base address. Slice 0 is at PADDR, Slice 1 at PADDR+1,etc.

If the base address is set too high, the offset of the higher Slices would wrap past zero. Do not to exceed a PHY base address of 28 (for quad Slice devices).

3.10 Fiber Modules and Management

3.10.1 TWO-WIRE INTERFACE

A serial Two Wire Interface (TWI) Host, enabled as GPIO Alternate Functions, is available for optical module management per Line Port.

The TWI Host must be configured before initiating any TWI instructions. The Client ID to be transmitted in the first byte of every instruction is selectable in the TWI_CLIENT_ID register (default value 0x50).

The interface's data rate is determined by the PRESCALE register. The TWI Host can operate from 916 Hz to 1 MHz. The logic is clocked at 300 MHz with the data rate controlled by the PRESCALE register using this formula:

- TWI SCL frequency = (300 MHz) / [5 * (PRESCALE+1)], where
  - PRESCALE is valid between 0x003B and 0xFFFF (0x003B = 1 MHz, default of 0x0095 = 400 kHz, 0x0257 = 100 kHz)

The TWI Host transmits instructions to the optical module with 8-bit data registers and 256 register addresses per Client ID. The TWI_BUS_STATUS.TWI_BUS_BUSY or TWI_READ_STATUS_DATA.TWI_BUS_BUSY register bit should be read to verify the previous instruction has finished prior to initiating a new instruction. Instructions initiated when the interface is busy will be ignored. Both registers report the same interface busy status purely for user convenience.

Read Instructions

A read instruction is initiated by the TWI Host when the TWI_READ_ADDR register is written. The value written to TWI_READ_ADDR.READ_ADDR field is the optical module register address to be read. Once the TWI_READ_STATUS_DATA.TWI_BUS_BUSY bit clears, indicating the read instruction completed, the returned data is available in the TWI_READ_STATUS_DATA.READ_DATA field.

The TWI Host does not support read-increment instructions.

Write Instructions

A write instruction is initiated by the TWI Host when the TWI_WRITE_CTRL register is written. The value written to TWI_WRITE_CTRL.WRITE_ADDR field is the optical module register address to be written while the value written to TWI_WRITE_CTRL.WRITE_DATA field is the optical module register data.

The TWI_BUS_STATUS register reports the status of the write instruction. TWI_BUS_STATUS.TWI_WRITE_ACK=1 indicates that the TWI Host received ACKs from the optical module at appropriate times. TWI_BUS_STATUS.TWI_WRITE_ACK is cleared each time a new instruction is issued. TWI_BUS_STATUS.TWI_WRITE_ACK=0 indicates the TWI Host did not receive ACKs from the optical module at appropriate times, meaning the interface is likely stuck in a state waiting for the ACK.

Clock Stretching

The optical module may hold the TWI_SCL signal low following the ACK cycle. This will cause the TWI Host to be wait-stated.

Bus clear

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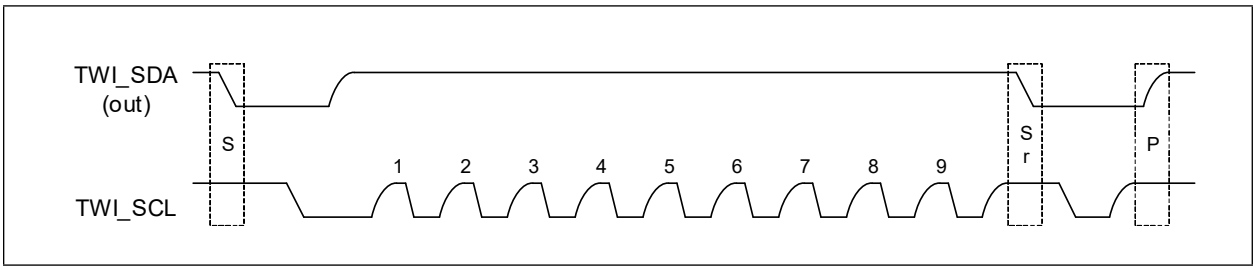
Writing a 1 to the BLOCK_LEVEL_RESET1.TWIM_RESET register bit will reset the TWI Host and release it from its stuck state. An external reset should be issued to the optical module as well.

The TWI Host and the optical module can become out-of-sync due to these resets and a bus clear sequence should be issued by writing any value to the TWI_RESET_SEQ register. This will put the optical module's two-wire interface back into a state that allows it to receive future two-wire serial instructions.

The following illustration shows a two-wire serial bus clear sequence. The bus clear sequence consists of a START symbol (S), nine SCK clock pulses while SDA is high, a repeated START symbol (Sr) and a STOP symbol (P).

FIGURE 3-24: TWI BUS CLEAR



3.10.2 FIBER MODULE SUPPORT

LAN8042 supports the following optical modules, with GPIO mappings as described. Signal polarity is generally consistent across module types (e.g. 0 on the MOD_ABS input indicates a module is present) but module-specific differences exist. In some modules dual-purpose signal (e.g. IntL/RxLOSL) behavior is configurable in the module using the TWI interface.

TABLE 3-14: OPTICAL MODULE INTERFACES

LAN8042 Pins	Optical Module Pins					
	SFP *INF-8074i*	**XFP** *INF-8077i*	**SFP+** *SFF8431*	**QSFP+** *SFF8436* *SFF8679*	**SFP28** *SFF8402*	**QSFP28** *SFF8665* *SFF8679*
RATESEL0 (output)	RATESELECT Full vs Reduced Rate Not often used	PDOWN/RST	RS0 / RS1 Full vs Reduced Rate Not often used	ResetL	Speci-fied to be same as SFP+	ResetL
MOD_ABS (input)	MOD-DEF0 0=module pres-ent	MOD_ABS 0=module present	MOD_ABS 0=module present	ModPrsL 0=module present		ModPrsL 0=module present
TWI_HST_SCL (output)	MOD-DEF1 =I2C SCL	SCL	SCL	SCL		SCL
TWI_HST_SDA (I/O)	MOD-DEF2 =I2C SDA	SDA	SDA	SDA		SDA
TX_DIS (output)	TXDISABLE	TX_DIS	TX_DISABLE	LPMode/TxDis		LPMode/ TxDis
TX_FAULT (input)	TXFAULT	MOD_NR				
RXLOS (input)[1]	LOS	RX_LOS	RX_LOS	IntL/RxLOSL		IntL/ RxLOSL
		MOD_DESEL Tie low		ModSelL Tie low		ModSelL Tie low

1: When enabled as an Alternate Function, RX_LOS is internally combined with the Line SerDes LOS into the applicable PCS to force an immediate Link Down condition when either the optical receive signal or SerDes receive signal is lost.

I^2C (TWI) is supported by a dedicated TWI Host in each LAN8042 slice.

3.11 LEDs

LAN8042 supports two LEDs per Line Port: Activity and Link Up, which operate as follows:

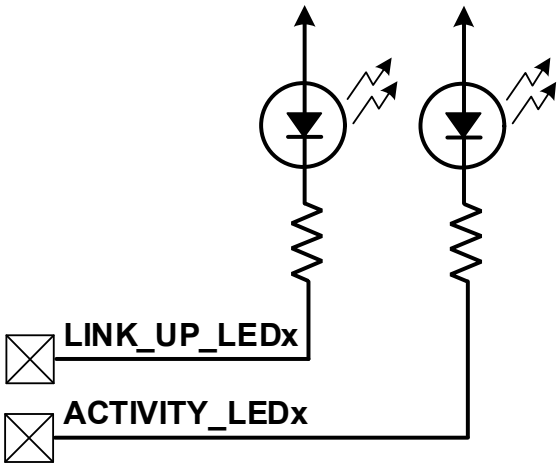
1. The Line Port Activity LED blinks at a configurable rate when either TX or RX Line Port activity is detected. The Line Port Activity LED is not lit and does not blink when the Line Port Link is down.
2. The Line Port Link Up LED is lit solid when the Line Port Link is up and is not be lit when the Line Port Link is down.
3. LEDs functions as above for all Line Port speeds and PCSs.
4. Each LED is active low (GPIO output = 0 turns the LED on).

APPLICATION NOTE: LEDs are internally active low, therefore the GPIO polarity should be non-inverted (GPIOOUT_INVx = 0) to achieve an active low pin.

APPLICATION NOTE: LEDs are typically set to open-drain operation by setting GPIOOUT_PPx = 0.

Blinking is configured via the ACTIVITY_LED_BLINK_TIME register.

FIGURE 3-25: LINE PORT LEDS



3.12 GPIOs

LAN8042 provides 40 GPIOs with the following functionality:

- Each pin can function as a normal GPIO which can operate as an Input, Output or I/O.
  - GPIOFUN_SELx must be set to a 1 for the GPIO mode.
  - There are is no explicit “GPIO output data bit” for software to control. GPIO output data is normally a 0 when the GPIO output is enabled. The GPIO output can be set to 1 by inverting the output (setting GPIOOUT_INVx = 1).
  - GPIO outputs are selectable push-pull or open drain. If configured as an open drain output or I/O pin, an external pull-up resistor is always required for proper operation.
  - Each GPIO pin can be configured to be an interrupt source.

  Note: Internal pull-ups are enabled by default but are only meant to prevent floating inputs.
- Alternately, each pin can be configured as an Alternate Function. Alternate Functions support one optical module interface per Line Port, two Aggregate Interrupts to an external Host CPU and two LEDs per Line port.
  - GPIOFUN_SELx must be set to a 0 for the Alternate Function to be selected.

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- GPIOOUT_ENx must be set to a 1 for the Alternate Function to be output.
- The GPIOOUT_INVx can be used to invert the Alternate Function.
- Alternate Function outputs are selectable push-pull or open drain.

• By default all pins default to GPIOs, have internal pull-up enabled, are output disabled, open-drain and non-inverted
• GPIOFUN_SELx = 1, GPIOOUT_ENx = 0, GPIOOUT_PPx = 0, GPIOOUT_INVx = 0).

Note: Some optical module interface signals are supported as standard GPIOs (i.e. no extra hardware) while some connect through an Alternate Function path.

Note: GPIO and interrupt source input paths continue to function while configured as an Alternate Function (thus allowing software and hardware to monitor pin states).

Note: For Alternate Functions (which have an input path) set as a GPIO, the Alternate Function input value is set inactive as stated in Table 3-16

For GPIOs which do not have an Alternate Function output, the Alternate Function output value is to be a ‘1’. Assuming GPIOOUT_INVx = 0, if the GPIOFUN_SELx is set for ‘Alternate Function’ the pin will not be driven.

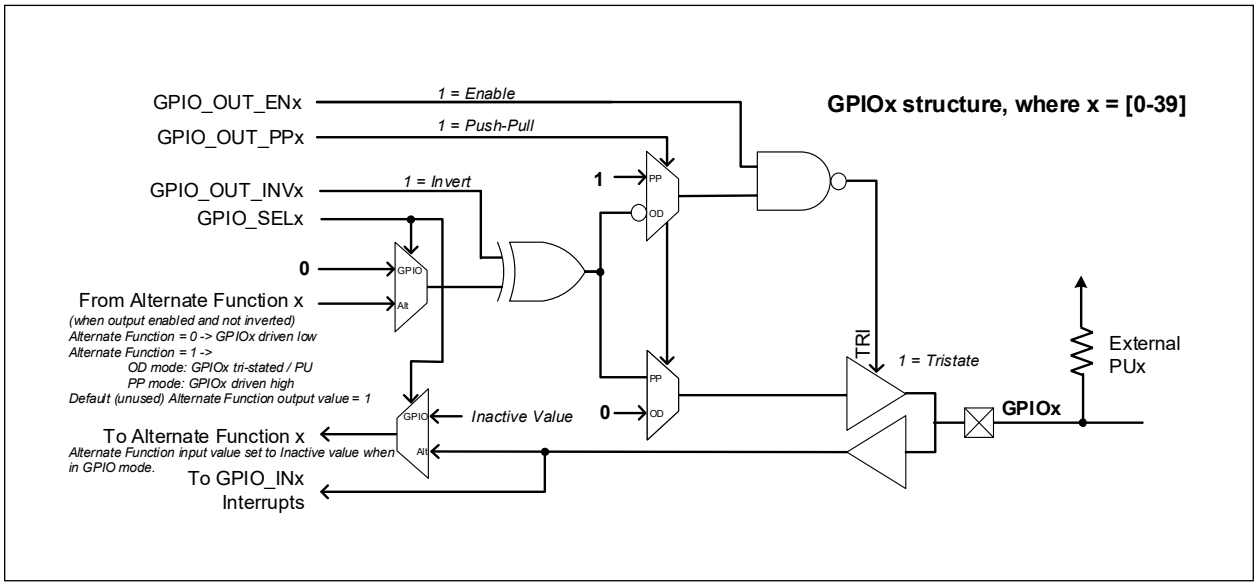
The GPIO output logic is as follows:

TABLE 3-15: GPIO OUTPUT TRUTH TABLE

GPIOOUT_ENx (0=disabled 1=enabled)	**GPIOFUN_SELx** (0=alternate 1=GPIO)	**GPIOOUT_PPx** (0=open-drain 1=push-pull)	**GPIOOUT_INVx** (0=non-inverted 1=inverted)	**Alt Function**	**GPIOx Output**
0	X	X	X	X	Hi-Z (PU)
1	1	0	0	X	0
			1	X	Hi-Z (PU)
		1	0	X	0
			1	X	1
	0	0	0	0	0
			0	1	Hi-Z (PU)
			1	0	Hi-Z (PU)
			1	1	0
		1	0	0	0
			0	1	1
			1	0	1
			1	1	0

Figure 3-26 shows a high-level view of a representative GPIO. This structure is repeated per GPIO.

FIGURE 3-26: GPIO STRUCTURE



LAN8042 GPIO functions are described in Table 3-16

TABLE 3-16: SUPPORTED GPIO FUNCTIONS

GPIO	Alternate Function	Internal Mapping	Setting	System Purpose	
GPIO0	-		GPIO (Output)	CH0_RATESEL0 / PDOWN / RST	Line Port 0 Module Interface
GPIO1	-		GPIO (Input)	CH0_MOD_ABS	
GPIO2	CH0_TWI_HST_SCL	CH0 TWI Host	Alt Fn (Output)	CH0_TWI_HST_SCL	
GPIO3	CH0_TWI_HST_SDA	CH0 TWI Host Inactive Value = 0	Alt Fn (I/O)	CH0_TWI_HST_SDA	
GPIO4	-		GPIO (Output)	CH0_TX_DIS	
GPIO5	-		GPIO (Input)	CH0_TX_FAULT	
GPIO6	CH0_Optical_LOS	CH0 PCS LOS logic Inactive Value = 0	Alt Fn (Input)	CH0_RXLOS	
	-	-		CH0_INTL	
GPIO7	CH0_RX_LED	CH0 LP LED logic	Alt Fn (Output)	CH0_LINK_LED	Line Port 0 Link LED
GPIO8	-		GPIO (Output)	CH1_RATESEL0 / PDOWN / RST	Line Port 1 Module Interface
GPIO9	-		GPIO (Input)	CH1_MOD_ABS	
GPIO10	CH1_TWI_HST_SCL	CH1 TWI Host	Alt Fn (Output)	CH1_TWI_HST_SCL	
GPIO11	CH1_TWI_HST_SDA	CH1 TWI Host Inactive Value = 0	Alt Fn (I/O)	CH1_TWI_HST_SDA	
GPIO12	-		GPIO (Output)	CH1_TX_DIS	
GPIO13	-		GPIO (Input)	CH1_TX_FAULT	
GPIO14	CH1_Optical_LOS	CH1 PCS LOS logic Inactive Value = 0	Alt Fn (Input)	CH1_RXLOS	
	-	-		CH1_INTL	
GPIO15	CH1_RX_LED	CH1 LP LED logic	Alt Fn (Output)	CH1_LINK_LED	Line Port 1 Link LED

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TABLE 3-16: SUPPORTED GPIO FUNCTIONS (CONTINUED)

GPIO	Alternate Function	Internal Mapping	Setting	System Purpose	
GPIO16	-		GPIO (Output)	CH2_RATESEL0 / PDOWN / RST	Line Port 2 Module Interface
GPIO17	-		GPIO (Input)	CH2_MOD_ABS	
GPIO18	CH2_TWI_HST_SCL	CH2 TWI Host	Alt Fn (Output)	CH2_TWI_HST_SCL	
GPIO19	CH2_TWI_HST_SDA	CH2 TWI Host Inactive Value = 0	Alt Fn (I/O)	CH2_TWI_HST_SDA	
GPIO20	-		GPIO (Output)	CH2_TX_DIS	
GPIO21	-		GPIO (Input)	CH2_TX_FAULT	
GPIO22	CH2_Optical_LOS	CH2 PCS LOS logic Inactive Value = 0	Alt Fn (Input)	CH2_RXLOS	
	-	-		CH2_INTL	
GPIO23	CH2_RX_LED	CH2 LP LED logic	Alt Fn (Output)	CH2_LINK_LED	Line Port 2 Link LED
GPIO24	-		GPIO (Output)	CH3_RATESEL0 / PDOWN / RST	Line Port 3 Module Interface
GPIO25	-		GPIO (Input)	CH3_MOD_ABS	
GPIO26	CH3_TWI_HST_SCL	CH3 TWI Host	Alt Fn (Output)	CH3_TWI_HST_SCL	
GPIO27	CH3_TWI_HST_SDA	CH3 TWI Host Inactive Value = 0	Alt Fn (I/O)	CH3_TWI_HST_SDA	
GPIO28	-		GPIO (Output)	CH3_TX_DIS	
GPIO29	-		GPIO (Input)	CH3_TX_FAULT	
GPIO30	CH3_Optical_LOS	CH3 PCS LOS logic Inactive Value = 0	Alt Fn (Input)	CH3_RXLOS	
	-	-		CH3_INTL	
GPIO31	CH3_RX_LED	CH3 LP LED logic	Alt Fn (Output)	CH3_LINK_LED	Line Port 3 Link LED
GPIO32	-	-	GPIO (Output)	GPIO32	Available GPIO
GPIO33	-	-	GPIO (Output)	GPIO33	Available GPIO
GPIO34	INTR_A	Aggregate Interrupt 0	Alt Fn (Output)	INTR_A	Host CPU Interrupts
GPIO35	INTR_B	Aggregate Interrupt 1	Alt Fn (Output)	INTR_B	
GPIO36	CH0_TX_LED	CH0 LP LED logic	Alt Fn (Output)	CH0_ACTIVITY_LED	Line Ports 0-3 Activity LEDs
GPIO37	CH1_TX_LED	CH1 LP LED logic	Alt Fn (Output)	CH1_ACTIVITY_LED	
GPIO38	CH2_TX_LED	CH2 LP LED logic	Alt Fn (Output)	CH2_ACTIVITY_LED	
GPIO39	CH3_TX_LED	CH3 LP LED logic	Alt Fn (Output)	CH3_ACTIVITY_LED	

3.12.1 GPIO INTERRUPTS

Each GPIO pin can be configured as an interrupt source. The pin must be configured as an input and will generate an input upon state change. The minimum pulse width that must be reliably detected is 100 ns. Any smaller pulse may or may not be detected.

APPLICATION NOTE: Following reset(s) a false GPIO interrupt might be indicated due to the settling of the change detect logic.

GPIOs are always enabled as inputs. Any pin change due to GPIO or Alternate Function output will cause a GPIO interrupt.

3.13 Resets and Power-On Self-Test

3.13.1 RESETS

LAN8042 supports the following resets.

- Global Hardware Reset
  - Global Hardware Reset is asserted by the RESET_N pin input which is required at power-up and available for the system to initiate a full chip reset without cycling power.
  - Global Hardware Reset resets all chip functions except PLLs and clocks.
- Global Software Reset
  - Global Software Reset is asserted by Software writing to the appropriate GLOBAL_FAST_RESET or BLOCK_LEVEL_SOFTWARE_RESET1 register bit. Global Fast reset bits are self-clearing.
  - The Global Software Reset resets all chip functions except PLLs, clocks, GPIOs, and certain Global functions.
- Global Software Block Resets
  - Global Software Block Resets are asserted by Software writing to the appropriate BLOCK_LEVEL_SOFTWARE_RESET1/2. Global Software Block reset bits are self-clearing.
- Host Slice and Line Slice Software Resets
  - Host Slice and Line Slice Software Resets are asserted by Software writing to the appropriate BLOCK_LEVEL_SOFTWARE_RESET1 or GLOBAL_FAST_RESET register bits. Global Fast reset bits are self-clearing.
  - Slice Software Resets reset the Slice logic, as well as the applicable Slice interface of the Cross-Connect.
- CSR Ring Software Resets
  CSR Ring Software Resets are asserted by Software writing to the appropriate GLOBAL_FAST_RESET register bit.

3.14 Host Interrupts

LAN8042 supports two Aggregate Interrupts to an external Host CPU, Aggregate Interrupt 0 and Aggregate Interrupt 1, each of which can be generated from any of the following interrupt sources:

- Any slice-level interrupt source
- Any chip-level interrupt source

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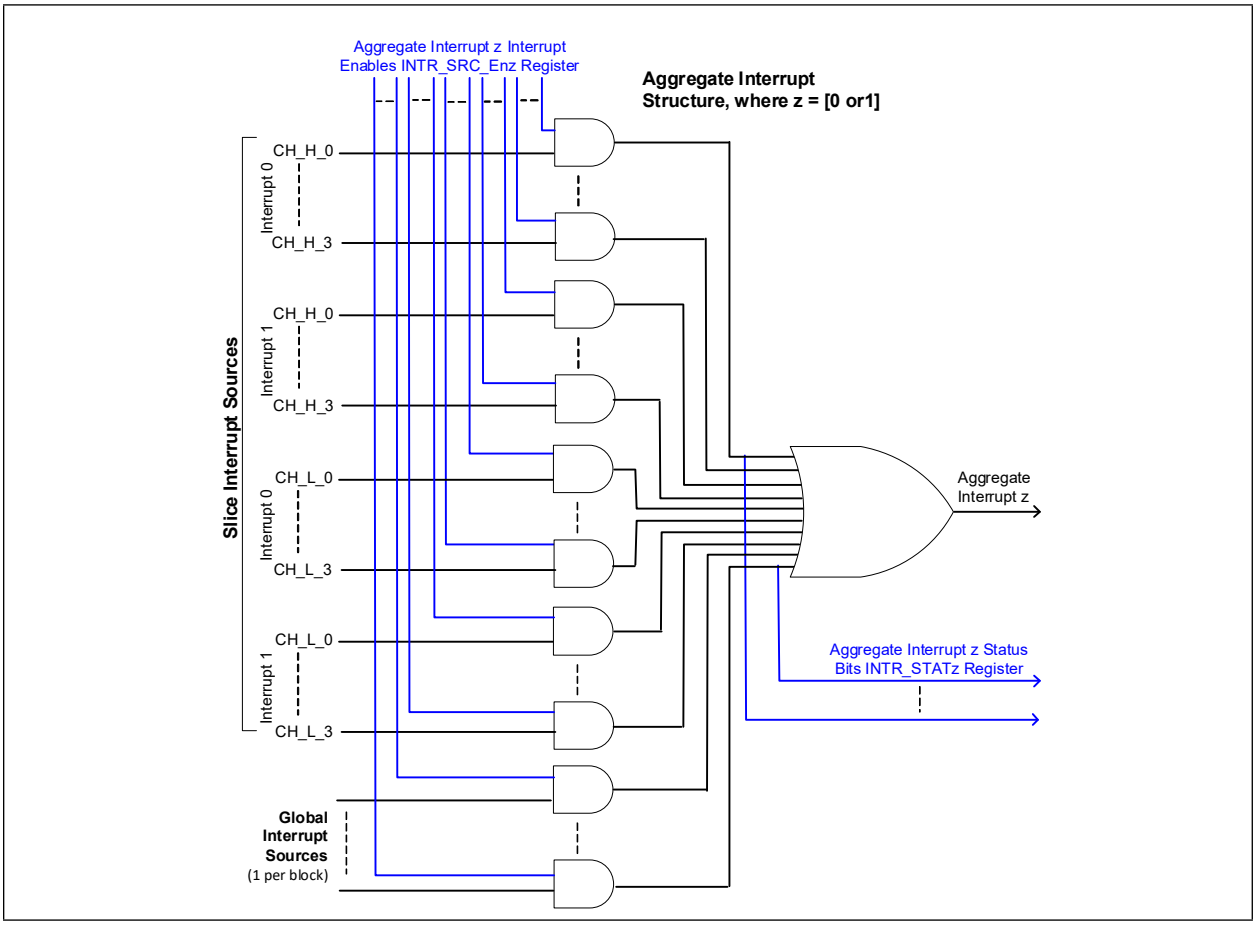
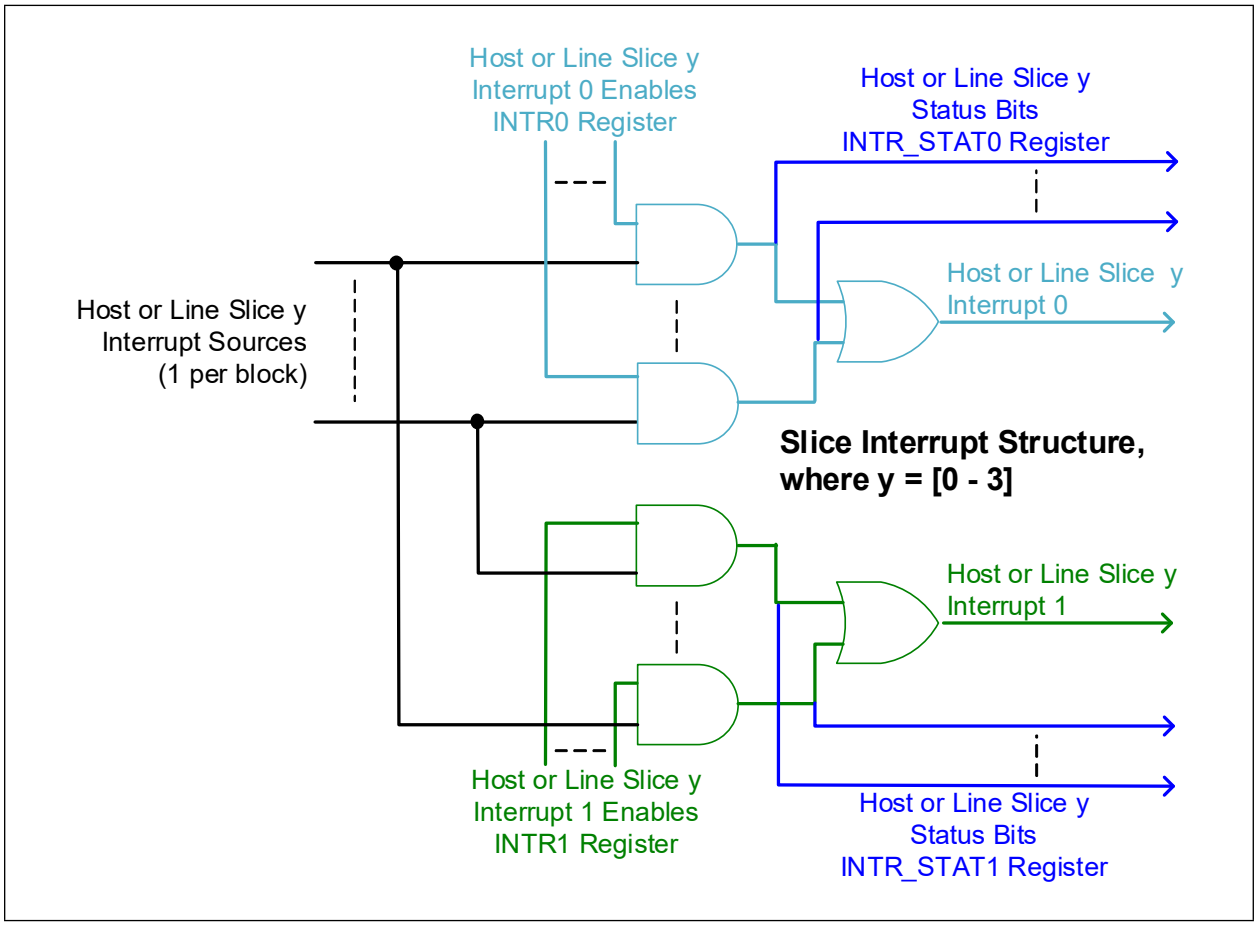
Figure 3-27 shows how interrupts are generated and is repeated for each of the two Aggregate Interrupts. Interrupts are active high by default but can be active low by inverting the GPIO pin.

FIGURE 3-27: GLOBAL AGGREGATE INTERRUPTS



Each of the four Host slices generates a CH_H_0 and a CH_H_1 interrupt and each of the four Line slices generates a CH_L_0 and a CH_L_1 interrupt. Each of the Host slice interrupts is identical as is each of the Line slice interrupts.

FIGURE 3-28: SLICE INTERRUPTS



Interrupt Masks (Enables) are organized as follows:

- Aggregate Interrupt 0: The global ISR INTR_SRC_EN0 register contains an enable bit for each chip-level block with interrupt capability, the eight Slice Interrupts 0 and the eight Slice Interrupts 1.
- Aggregate Interrupt 1: The global ISR INTR_SRC_EN1 register contains an enable bit for each chip-level block with interrupt capability, the eight Slice Interrupts 0 and the eight Slice Interrupts 1.
- Slice interrupts: Each Host slice and each Line slice has an INTR0 register for its Slice Interrupt 0 and an INTR1 register for its Slice Interrupt 1. In these registers is an interrupt enable bit for each slice-level block with interrupt capability.
- Each chip-level and slice-level block with interrupt capability contains a register with a mask or enable bit for each interrupt in the block.

Effectively slice-level interrupts have 3 levels of enable, one at the Aggregate level, one at the slice level and one at each block. Chip-level interrupts have 2 levels of enable, one at the Aggregate level and one at each block.

Interrupt Status is organized as follows:

- Aggregate Interrupt 0: The global INTR_STAT0 register contains a read-only, masked interrupt status bit for each chip-level block with interrupt capability, the eight Slice Interrupts 0 and the eight Slice Interrupts 1.
- Aggregate Interrupt 1: The global INTR_STAT1 register contains a read-only, masked interrupt status bit for each chip-level block with interrupt capability, the eight Slice Interrupts 0 and the eight Slice Interrupts 1.
- Slice interrupts: Each Host slice and each Line slice has an INTR_STAT0 register for its Slice Interrupt 0 and an INTR_STAT1 register for its Slice Interrupt 1. In these registers is a read-only, masked interrupt status bit for each slice-level block with interrupt capability.
- Each chip-level and slice-level block with interrupt capability contains one or more interrupt status registers with a

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status bit for each interrupt in the block. Interrupts are latched and cleared at this level.

Effectively slice-level interrupts have 3 levels of status, one at the Aggregate level, one at the slice level and one at each block. Chip-level interrupts have 2 levels of status, one at the Aggregate level and one at each block. Note the status at the Aggregate and slice levels return the masked interrupts while the status at the block level return the unmasked interrupts.

3.15 JTAG

The device includes an integrated JTAG test port. The interface consists of five standard pins (TDI, TDO, TCK, TMS and TRST). A sixth pin, JTAG_SEL, is used for test mode. The JTAG interface conforms to the IEEE Standard 1149.1 - 2001 Standard Test Access Port (TAP) and Boundary-Scan Architecture.

3.15.1 TEST TAP CONTROLLER

All input and output data is synchronous to the TCK test clock input. TAP input signals TMS and TDI are clocked into the test logic on the rising edge of TCK, while the output signal TDO is clocked on the falling edge.

The implemented IEEE 1149.1 instructions and their op codes are shown in the following table. The length of the instruction is 4 bits.

TABLE 3-17: IEEE 1149.1 OP CODES

Instruction	Op Code	Comment
BYPASS 0	all 0’s	Mandatory Instruction
BYPASS 1	all 1’s	Mandatory Instruction
SAMPLE	0101	Mandatory Instruction
EXTEST	0001	Mandatory Instruction
CLAMP	0000	Optional Instruction
ID_CODE	1000	Optional Instruction
HIGHZ	0110	Optional Instruction
INTEST	0100	Optional Instruction
EXTEST_PULSE	0010	Mandatory Instruction for 1149.6
EXTEST_TRAIN	0011	Mandatory Instruction for 1149.6
HOSTIJTAG 1	0111	Mandatory AccessLink Instruction for IEEE 1687 (iJTAG)

Access to device test mode registers are implemented with private instructions as listed in the LAN8042 Test Controller Specification.

3.15.1.1 JTAG Timing Requirements

The JTAG test tap must run at 25 MHz or better.

3.15.2 TEST MODES

Test modes are accessed via the JTAG interface when the JTAG_SEL pin is set low. Test modes are selected using internal user data registers. The functionality of the test controller is left to design.

At design discretion, RAM and ROM BIST maybe directly controlled by test registers or may be controlled using the BIST registers in the CSR Ring.

3.15.3 CSR RING ACCESS

JTAG test mode may access the CSR Ring registers.

JTAG test mode access to the CSR Ring registers will statically take over the CSR Ring Origins from the PHY management interface.

As opposed to using the channel number / MMD / register mapping scheme that is used by the SPI and MDIO accesses, JTAG access to the CSR Ring registers will directly specify the ring number, target ID and full register address.

3.15.4 BOUNDARY SCAN

Standard JTAG 1149.1 boundary scan is provided on the digital pins.

The SerDeses' TX and RX pairs support AC boundary scan (JTAG 1149.6). Some support logic is required.

3.16 Miscellaneous

3.16.1 POWER MANAGEMENT

LAN8042 supports the following Power Management capabilities:

SerDes

Each SerDes may be dynamically powered down to save power.

Data Path Clocks

Each SerDes CMU supports powering down its VCO and various clock drivers effectively providing clock gating to each slice's data path.

3.16.2 WARM RESTART

Hardware support for software based Warm Restart.

3.16.3 TEMPERATURE SENSOR

LAN8042 contains a Temperature Sensor with accuracy of ±1.5°C (to be finalized during characterization). It is read and controlled via registers in the GLOBAL target.

3.17 Configuration Straps

3.17.1 FUNCTION MODE STRAPS

Several pin based straps are available to select firmware, Host software or hardware implemented options.

Configuration straps are multi-function pins that are driven as outputs during normal operation. During a System Reset (**RESET_N**) these outputs are not driven. The externally pulled high or low state of the signal is latched following deassertion of **RESET_N** and is used to determine the value of the Strap_Read register and the default value of the Strap_Override register.

Note: Functional configuration straps include internal pull-down resistors.

Bit assignments are as follows.

Note: Firmware or Host software implemented assignments are non-hardware committed in that they can be redefined in the future.

TABLE 3-18: STRAP PIN ASSIGNMENTS

Bit	Description	Pin or logic level	Firmware**, Software or Hardware**
7	Test	TEST (Note 1)	Firmware
6	unused	'b0	n/a
5	unused	'b0	n/a
4	unused	'b0	n/a
3	BIST Bypass (BIST_BYPASS_STRAP)	FAILOVEROUT1	Software, Firmware, Hardware
2	Reserved Strap1	FAILOVEROUT0	n/a
1	RESERVED	0	
0	RESERVED	0	
1:	Not really a strap, but rather a the live pin value.		

Note: The system designer must guarantee that configuration straps meet the timing requirements. If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

Note: When externally pulling configuration straps high the strap should be tied to the VDDO associated with the shared pin.

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A 16-bit Strap_Override register allows for Host software determined reconfiguration as well as for extra option bits.

4.0 OPERATIONAL CHARACTERISTICS

4.1 Absolute Maximum Ratings*

Supply Voltage (**VDD**) (Note 4-1) ..... -0.3V to +0.99V

Supply Voltage (**VDDHS_N, VDDHS_S, VDDHV_N, VDDHV_S**) ..... -0.3V to +1.10V

Supply Voltage (**VDDH18_N, VDDH18_S, VDDO_18, VDDA_SYSPLL, VDDA_PLL**) ..... -0.3V to +1.96V

Variable Supply Voltage (**VDDO_A, VDDO_B**) ..... -0.3V to +3.465V

Positive voltage on input signal pins (referenced to **VDDO_A, VDDO_B**), with respect to ground ..... **VDDO_A/B** +0.5V

Negative voltage on input signal pins (referenced to **VDDO_A, VDDO_B**), with respect to ground ..... -0.5V

Positive voltage on input signal pins (referenced to **VDDO_18**), with respect to ground ..... +2.1V

Negative voltage on input signal pins (referenced to **VDDO_18**), with respect to ground ..... -0.5V

LVDS input signal pins voltage, with respect to ground ..... 0V to +2.4V

Storage Temperature ..... -55°C to +150°C

Lead Temperature Range ..... Refer to JEDEC Spec. J-STD-020

HBM ESD Performance (**RXIN[0:3]N/P, TXOUT[0:3]N/P, RXOUT[0:3]N/P, TXIN[0:3]N/P**) ..... +/-1 kV

HBM ESD Performance (all others) ..... +/-2 kV

CDM ESD Performance ..... +/-200V

Note 4-1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 4.2, Operating Conditions**, Section 4.5, DC Specifications, or any other applicable section of this specification is not implied.

4.2 Operating Conditions**

Supply Voltage (**VDD**) ..... (+/-5%) 0.855V to +0.945V

Supply Voltage @ 25 Gbps (**VDDHS_N, VDDHS_S, VDDHV_N, VDDHV_S**) ..... (+/-2.5%) 1.0V to +1.05V

Supply Voltage @ 1 Gbps / 10 Gbps (**VDDHS_N, VDDHS_S, VDDHV_N, VDDHV_S**) ..... (+/-5%) 0.95V to +1.05V

Supply Voltage (**VDDH18_N, VDDH18_S, VDDO_18, VDDA_SYSPLL, VDDA_PLL**) ..... (+/-5%) 1.71V to +1.89V

Variable Supply Voltage, @1.8V (**VDDO_A, VDDO_B**) ..... (+/-5%) 1.71V to +1.89V

Variable Supply Voltage, @3.3V (**VDDO_A, VDDO_B**) ..... (+/-5%) 3.135V to +3.465V

Positive voltage on input signal pins (referenced to **VDDO_A, VDDO_B**), with respect to ground ..... **VDDO_A/B** +0.5V

Negative voltage on input signal pins (referenced to **VDDO_A, VDDO_B**), with respect to ground ..... -0.5V

Positive voltage on input signal pins (referenced to **VDDO_18**), with respect to ground ..... +2.1V

Negative voltage on input signal pins (referenced to **VDDO_18**), with respect to ground ..... -0.5V

LVDS input signal pins voltage, with respect to ground ..... 0V to +2.4V

Operating Temperature ..... T_A= -40°C to T_J=110°C

**Proper operation of the device is guaranteed only within the ranges specified in this section.

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4.3 Package Thermal Specifications

4.3.1 256-BGA

TABLE 4-1: PACKAGE THERMAL PARAMETERS (256-BGA)

Symbol	Value	Units	Notes
Θ_{JA}	14.38	°C/W	0 Meters/second
	11.42	°C/W	1 Meters/second
	10.39	°C/W	2.5 Meters/second
Θ_{JB}	2.82	°C/W	
Θ_{JC}	0.70	°C/W	
Ψ_{JT}	0.25	°C/W	

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESDN51.

4.4 Power Consumption

This section details the power consumption of the device as measured during various modes of operation at various operating voltages. Power dissipation is impacted by temperature, supply voltage and external source/sink requirements.

Power dissipation is impacted by temperature, supply voltage and external source/sink requirements. All worst-case measurements were taken at the maximum temperature/voltages from the Operating Conditions. All typical measurements were taken at +25°C unless otherwise noted.

4.4.1 WORST CASE FOUR PORT OPERATION

All worst case measurements were taken at voltage +5% and maximum operating temperature unless otherwise noted.

TABLE 4-2: WORST CASE 25G FOUR PORT (0.9V, 1.0V, 1.0V, 1.8V, 1.8V, 3.3V)

Modes	0.9V VDD Total (mA)	1.0V VDDHV_N/S Total (mA)	1.0V VDDHS_N/S Total (mA)	1.8V VDDA_SYSPLL/ VDDA_PLL VDDO_18 Total (mA) (Note 4-2)	1.8V VDDH18_N/S Total (mA)	3.3V VDDO_A Total (mA)	3.3V VDDO_B Total (mA)	Total Power (mW)
4 ports Host/Line 25 Gbps 100% utilization	1965	75	2755	10	335	30	30	5707
4 ports Host/Line 25 Gbps, 100% utilization, MACsec enabled in MAC Retimer mode	2752	75	2755	10	335	30	30	6451
After Hardware Reset Deassertion	400	70	628	10	30	40	20	1413

Note 4-2 VDDO_18 is its own power rail and operates independently of VDDA_SYSPLL/VDDA_PLL.

TABLE 4-3: WORST CASE 10G FOUR PORT (0.9V, 1.0V, 1.0V, 1.8V, 1.8V, 3.3V)

Modes	0.9V VDD Total (mA)	1.0V VDDHV_N/S Total (mA)	1.0V VDDHS_N/S Total (mA)	1.8V VDDA_SYSPLL VDDA_PLL/ VDDO_18 Total (mA) (Note 4-3)	1.8V VDDH18_N/S Total (mA)	3.3V VDDO_A Total (mA)	3.3V VDDO_B Total (mA)	Total Power (mW)
4 ports Host/Line 10 Gbps, 100% utilization	1360	70	2040	10	305	30	30	4323

TABLE 4-3: WORST CASE 10G FOUR PORT (0.9V, 1.0V, 1.0V, 1.8V, 1.8V, 3.3V)

4 ports Host/Line 10 Gbps, 100% utilization, MACsec enabled in MAC Retimer mode	1735	70	2044	10	305	30	30	4681
After Hardware Reset Deassertion	400	70	628	10	30	40	20	1413

Note 4-3 VDDO_18 is its own power rail and operates independently of VDDA_SYSPLL/VDDA_PLL.

4.4.2 TYPICAL USAGE FOUR PORT OPERATION

All typical usage measurements were taken at +25°C unless otherwise noted.

TABLE 4-4: TYPICAL USAGE 25G FOUR PORT (0.9V, 1.0V, 1.0V, 1.8V, 1.8V, 3.3V)

Modes	0.9V VDD Total (mA)	1.0V VDDHV_N/S Total (mA)	1.0V VDDHS_N/S Total (mA)	1.8V VDDA_SYSPLL VDDA_PLL/ VDDO_18 Total (mA) (Note 4-4)	1.8V VDDH18_N/S Total (mA)	3.3V VDDO_A Total (mA)	3.3V VDDO_B Total (mA)	Total Power (mW)
4 ports Host/Line 25 Gbps, 100% utilization	1260	70	2550	10	325	30	30	4637
4 ports Host/Line 25 Gbps, 100% utilization, MACsec enabled in MAC Retimer mode	2205	70	2576	10	325	30	30	5514
After Hardware Reset Deassertion	226	70	650	10	30	20	30	1194

Note 4-4 VDDO_18 is its own power rail and operates independently of VDDA_SYSPLL/VDDA_PLL.

TABLE 4-5: TYPICAL USAGE 10G FOUR PORT (0.9V, 1.0V, 1.0V, 1.8V, 1.8V, 3.3V)

Modes	0.9V VDD Total (mA)	1.0V VDDHV_N/S Total (mA)	1.0V VDDHS_N/S Total (mA)	1.8V VDDA_SYSPLL VDDA_PLL/ VDDO_18 Total (mA) (Note 4-5)	1.8V VDDH18_N/S Total (mA)	3.3V VDDO_A Total (mA)	3.3V VDDO_B Total (mA)	Total Power (mW)
4 ports Host/Line 10 Gbps, 100% utilization	605	70	1862	10	300	20	30	3264
4 ports Host/Line 10 Gbps, 100% utilization, MACsec enabled in MAC Retimer mode	920	70	1862	10	300	20	30	3548
After Hardware Reset Deassertion	226	70	650	10	30	20	30	1194

Note 4-5 VDDO_18 is its own power rail and operates independently of VDDA_SYSPLL/VDDA_PLL.

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4.5 DC Specifications

TABLE 4-6: DC ELECTRICAL CHARACTERISTICS FOR 1.8V LVCMOS I/O

Parameter	Symbol	Min	Max	Units	Notes
Low Input Level	V_{IL}	-	0.693	V	Non-Schmitt mode
High Input Level	V_{IH}	1	-	V	Non-Schmitt mode
Schmitt Mode Falling Trip Point	V_{T-}	0.3*VDDO_18	0.6*VDDO_18	V	
Schmitt Mode Rising Trip Point	V_{T+}	0.4*VDDO_18	0.7*VDDO_18	V	
Schmitt Mode Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	0.1*VDDO_18	0.4*VDDO_18	V	
Input Leakage (V_{IN} = VSS or VDDO_18)	I_{IH}	-5	5	µA	Note 4-6
Pull-Up Resistance (V_{IN} = VSS)	R_{DPU}	10	-	kΩ	
Pull-Down Resistance (V_{IN} = VDDO_18)	R_{DPD}	10	-	kΩ	
Low Output Level	V_{OL}	-	0.4	V	I_{OL} = -4/8/16/20 mA
High Output Level	V_{OH}	VDDO_18 - 0.4	-	V	I_{OH} = 4/8/16/20 mA

Note 4-6 This specification applies to all inputs and three-stated bi-directional pins.

TABLE 4-7: DC ELECTRICAL CHARACTERISTICS FOR SELECTABLE 1.8V LVCMOS I/O

Parameter	Symbol	Min	Max	Units	Notes
1.8V Operation					
Low Input Level	V_{IL}	-0.3	0.693	V	Non-Schmitt mode
High Input Level	V_{IH}	1	2.28	V	Non-Schmitt mode
Schmitt Mode Low Input Level	V_{IL}	0.3*VDDO_A/B	0.6*VDDO_A/B	V	
Schmitt Mode High Input Level	V_{IH}	0.4*VDDO_A/B	0.7*VDDO_A/B	V	
Schmitt Mode Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	0.1*VDDO_A/B	-	V	
Input Leakage (V_{IN} = VSS or VDDO_A/B)	I_{IH}	-40	20	µA	Note 4-7
Pull-Up Resistance (V_{IN} = VSS)	R_{DPU}	10	-	kΩ	
Pull-Down Resistance (V_{IN} = VDDO_A/B)	R_{DPD}	10	-	kΩ	
Low Output Level	V_{OL}	-	0.4	V	I_{OL} = -4/8/16/20 mA Note 4-8
High Output Level	V_{OH}	VDDO_A/B - 0.4	-	V	I_{OH} = 4/8/16/20 mA Note 4-8
DC Sinking Current	I_{SINK}	-	10	mA	Note 4-9
DC Sourcing Current	I_{SOURCE}	-	10	mA	Note 4-9

Note 4-7 This specification applies to all inputs and three-stated bi-directional pins.

Note 4-8 The I_{OH}/I_{OL} values are NOT the actual DC currents supported for a lifetime of 10 years. The Electro-migration limit determines the maximum current supported under various modes of operation. The DC current supported for a lifetime of 10 years is defined as I_{SOURCE} and I_{SINK}.

Note 4-9 The max. DC current drive is obtained by setting drive strength to 20 mA. Under this mode the IO can sink 10 mA average current for 10 years within the limits of acceptable EM degradation.

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TABLE 4-8: DC ELECTRICAL CHARACTERISTICS FOR SELECTABLE 3.3V LVCMOS I/O

Parameter	Symbol	Min	Max	Units	Notes
3.3V Operation					
Low Input Level	V_{IL}	-0.3	1.22	V	Non-Schmitt mode
High Input Level	V_{IH}	1.93	**VDDO_A/B** + 0.3	V	Non-Schmitt mode
Schmitt Mode Low Input Level	V_{IL}	0.7	1.9	V	
Schmitt Mode High Input Level	V_{IH}	0.9	2.1	V	
Schmitt Mode Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	0.3	-	V	
Input Leakage (V_{IN} = **VSS** or **VDDO_A/B**)	I_{IH}	-40	20	µA	Note 4-10
Pull-Up Resistance (V_{IN} = **VSS**)	R_{DPU}	10	-	kΩ	
Pull-Down Resistance (V_{IN} = **VDDO_A/B**)	R_{DPD}	10	-	kΩ	
Low Output Level	V_{OL}	-	0.4	V	I_{OL} = -4/8/16/20 mA Note 4-11
High Output Level	V_{OH}	**VDDO_A/B** - 0.4	-	V	I_{OH} = 4/8/16/20 mA Note 4-11
DC Sinking Current	I_{SINK}	-	10	mA	Note 4-12
DC Sourcing Current	I_{SOURCE}	-	10	mA	Note 4-12

Note 4-10 This specification applies to all inputs and three-stated bi-directional pins.

Note 4-11 The I_{OH}/I_{OL} values are NOT the actual DC currents supported for a lifetime of 10 years. The Electromigration limit determines the maximum current supported under various modes of operation. The DC current supported for a lifetime of 10 years is defined as I_{SOURCE} and I_{SINK}.

Note 4-12 The max. DC current drive is obtained by setting drive strength to 20 mA. Under this mode the IO can sink 10 mA average current for 10 years within the limits of acceptable EM degradation.

4.5.1 SYSREFCK AND LREFCK CLOCK INPUTS DC ELECTRICAL CHARACTERISTICS

TABLE 4-9: SYSREFCK AND LREFCK DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Units
Clock source output DC Impedance	Z_{C-DC}	40	50	60	Ω Note 4-14
Input DC differential termination	R_I	80	-	100	Ω Note 4-15
Differential peak-to-peak input swing	$\|V_{ID}\|$	600	-	1600	mVppd Note 4-16
Input common-mode voltage	V_{CM}	-	900	-	mV

Note 4-13 Clock signal must be AC coupled.

Note 4-14 50 ohm DPLL Clock output termination used

Note 4-15 100ohm differential input termination used

Note 4-16 Covered 400mV and 800mV

4.5.2 SERDES DC ELECTRICAL CHARACTERISTICS

TABLE 4-10: SD25G TRANSMITTER

Parameter	Symbol	Min	Typical	Max	Units	Condition
Differential resistance	R_{DIFF}	80	100	120	Ω	-
Differential peak-to-peak output voltage Note 4-17	V_{O_DIFF}	400 Note 4-18	-	1200	mVppd	25GBASE-KR, 25G BASECR Note 4-19
Differential peak-to-peak output voltage	V_{O_DIFF}	-	-	900	mVppd	25GBASE-SR Note 4-19
Differential peak-to-peak output voltage with Tx disabled	V_{O_IDLE}	-	-	35	mVppd	25GBASE-SR Note 4-19
Differential peak-to-peak output voltage with Tx disabled	V_{OD_IDLE}	-	-	30	mVppd	25GBASE-KR, 25G BASECR Note 4-19

Note 4-17 Differential output swing is register configurable.

Note 4-18 The minimum drive level is the lowest guaranteed drive level achievable with the maximum amplitude configuration applied.

Note 4-19 Measured with 7 dB loss test channel at 12.89 GHz.

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TABLE 4-11: SD25G RECEIVER

Parameter	Symbol	Min	Typical	Max	Units	Condition
Differential peak-to-peak input voltage	V_{I_DIFF}	100	-	1200	mVppd	Clean eye sensitivity Note 4-20
AC-Coupling Note 4-21	-	-	-	100	nF	Note 4-22
Note 4-20 RX JTOL testing covered. Note 4-21 AC-coupling should be done at receiver. Note 4-22 100nf AC cap used for testing						

4.6 AC Specifications

4.6.1 POWER SEQUENCING

During power on and off, **VDDHS_S**, **VDDHS_N**, **VDDHV_S**, and **VDDHV_N** must never be more than 300 mV above **VDD**. The maximum rising slope of the **VDDHS_S, VDDHS_N, VDDHV_S, VDDHV_N**, **VDDH18_S,** and **VDDH18_N** supplies during power turn-on must be below 5 V/ms to limit the inrush current.

In summary, the following power up sequence should be followed: 0.9V before 1.0V before 1.8V before 3.3V. The **RESET_N** and **TRST** inputs must be held low until all power supply voltages have reached their recommended operating condition values.

4.6.2 SYSREFCK AND LREFCK CLOCK INPUTS AC ELECTRICAL CHARACTERISTICS

TABLE 4-12: SYSREFCK AND LREFCK AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Units	Condition
REFCLK frequency Note 4-23	f	-100 ppm	156.25	100 ppm	MHz	-
Clock duty cycle	-	40	-	60	%	Measured at 50% threshold
Rise time and fall time	t_R, t_F	-	-	0.5	ns	Within ±200 mV relative to common mode.
REFCLK input peak-to-peak jitter, bandwidth from 2.5 kHz to 10 MHz Note 4-24	-	-	-	30	ps	-
Note 4-23 SYSREFCK and LREFCK must be frequency synchronous. Note 4-24 Peak-to-peak values are typically higher than the RMS value by a factor of 10 to 14.						

4.6.3 SERDES AC ELECTRICAL CHARACTERISTICS

This section describes the AC specifications for the SerDes transceiver. The transceiver supports:

- SFP
- 1000BASE
- 10GBASE
- 25GBASE

Table 4-13 lists the AC characteristics for the SerDes transmitter.

TABLE 4-13: 1G SFP, 1000BASE-KX TRANSMITTER OUTPUT

Parameter	Symbol	Min	Max	Units	Condition
Data Rate	-	1.25 - 100 ppm	1.25 + 100 ppm	Gbps	SFP (SFP-MSA), 1000BASE-KX (IEEE 802.3, clause 70)
Rise time and fall time Note 4-25	t_R, t_F	35.6	320	ps	20% to 80%, 1000BASE-KX
Random jitter	R_J	-	0.15	UI_{PP}	At BER 10-12, 1000BASE-KX
Deterministic jitter	D_J	-	0.15	UI_{PP}	At BER 10-12, 1000BASE-KX
Total jitter	T_J	-	0.25	UI_{PP}	At BER 10-12, 1000BASE-KX
Eye mask	X1	-	0.125	UI	
Eye mask	X2	-	0.325	UI	
Eye mask	Y1	350	-	mV	
Eye mask	Y2	-	800	mV	

Note 4-25 Slew rate is programmable.

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Table 4-14 lists the AC characteristics for the SerDes transmitter.

TABLE 4-14: 1G SFP, 1000BASE-KX RECEIVER

Parameter	Symbol	Min	Max	Units	Condition
Data Rate	-	1.25 - 100 ppm	1.25 + 100 ppm	Gbps	SFP 1000BASE-KX
Differential input return loss	RLI_{SDD11}	-	-10	dB	50 MHz to 1289 MHz
Differential input return loss	RLI_{SDD11}	-	-10 + 13.275 x log (f/1289 MHz)	dB	1289 MHz to 3750 MHz
Common-mode input return loss	RLO_{SCC11}	- -	-7 + 13.275 x log (f/1250 MHz)	dB	100 MHz to 1250 MHz 1250 MHz to 3750 MHz
Jitter tolerance, total Note 4-26	TOL_{TJ}	600	-	ps	1G mode measured according to IEEE 802.3 Clause 38.6.8
Jitter tolerance, deterministic Note 4-26	TOL_{DJ}	370	-	ps	1G mode measured according to IEEE 802.3 Clause 38.6.8
Wideband SyncE jitter tolerance	WJT	312.5	-	UI_{P-P}	1G mode. 10 Hz to 12.1 Hz. Measured according to ITU-T G.8262, section 9.2
Wideband SyncE jitter tolerance	WJT	3750/f	-	UI_{P-P}	1G mode. 12.1 Hz to 2.5 kHz (f). Measured according to ITU-T G.8262, section 9.2
Wideband SyncE jitter tolerance	WJT	1.5	-	UI_{P-P}	1G mode. 2.5 kHz to 50 kHz. Measured according to ITU-T G.8262, section 9.2
Note 4-26	Jitter requirements represent high-frequency jitter (above 637 kHz) and not low-frequency jitter or wander.				

TABLE 4-15: 10G TRANSMITTER OUTPUT (SFI POINT B, HOST)

Parameter	Symbol	Min	Max	Units	Condition
Termination mismatch	ΔZ_M	-	5	%	-
AC common-mode voltage	V_{OCM_AC}	-	15	mV_{RMS}	Note 4-27
Total jitter Note 4-27	T_J	-	0.28	UI	Note 4-27
Data-dependent jitter	DDJ	-	0.1	UI	Note 4-27
Pulse shrinkage jitter	DDPWS	-	0.062	UI_{RMS}	Measured at point B, as specified in SFF-8431, revision 4.1. 6 dB channel loss (For 9 dB channel loss, worst case is 0.08 UI) Note 4-28
Uncorrelated jitter	UJ	-	0.023	UI_{RMS}	Note 4-27
Eye mask	X1	-	0.12	UI	Measured at 5e-5 mask hit ratio Note 4-27
Eye mask	X2	-	0.33	UI	Measured at 5e-5 mask hit ratio Note 4-27
Eye mask	Y1	95	-	mV	Measured at 5e-5 mask hit ratio Maximum SFI Channel loss of 3 dB Note 4-27
Eye mast	Y2	-	350	mV	Note 4-27

Note 4-27 With a jitter-free reference clock. Any **REFCLK** jitter with a frequency content below 7 MHz will add to the jitter generated at the 10G output.

Note 4-28 Measure at Point B as specified in SFF-8431, revision 4.1. A test channel of 5.5 dB insertion loss at 5.156 GHz was used.

TABLE 4-16: 10G RECEIVER INPUT (SFI POINT C AND C”, HOST)

Parameter	Symbol	Min	Max	Units	Condition
Pulse width shrinkage jitter	$DDPWS_{JIT_P\text{-}P}$	-	0.3	UI	Calibrated and measured at point C”, as specified in SFF-8431, revision 4.1
Eye mask X1	X1	-	0.35	UI	Calibrated and measured at point C”, as specified in SFF-8431, revision 4.1
Eye mask Y1	Y1	150	-	mV	Calibrated and measured at point C”, as specified in SFF-8431, revision 4.1
Eye mask Y2	Y2	-	425	mV	Calibrated and measured at point C”, as specified in SFF-8431, revision 4.1

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TABLE 4-17: 10GBASE-KR TRANSMITTER

Parameter	Symbol	Min	Max	Units	Condition
Data rate	-	10.3125 - 100 ppm	10.3125 + 100 ppm	Gbps	KR
Differential output return loss Note 4-29	RLO_{SDD22}	-	-9	dB	50 MHz to 2.5 GHz
Differential output return loss	RLO_{SDD22}	-	-9 + 12 x log (ƒ/2.5 GHz)	dB	2.5 GHz to 7.5 GHz
Common-mode output return loss	RLO_{SCC22}	-	-6	dB	50 MHz to 2.5 GHz
Common-mode output return loss	RLO_{SCC22}	-	-6 + 12 x log (ƒ/2.5 GHz)	dB	2.5 GHz to 7.5 GHz
Rise time and fall time	t_R, t_F	-	47	UI_{P-P}	-
Random jitter	R_J	-	0.15	UI_{P-P}	-
Deterministic jitter	D_J	-	0.15	UI_{P-P}	-
Duty cycle distortion (part of DJ)	DCD	-	0.035	UI_{P-P}	-
Total jitter Note 4-30	TJ	-	0.28	UI_{P-P}	-

Note 4-29 Informative, system related: maximum insertion loss is 15 dB @ 5 Ghz (10 Gbps) (vs ~25 dB based on the KR spec). This is to allow low cost interface implementation, while meeting system requirements.

Note 4-30 With a jitter-free reference clock. Any **REFCLK** jitter with a frequency content below 7 MHz will add to the jitter generated at the 10 Gbps output.

TABLE 4-18: 10GBASE-KR RECEIVER

Parameter	Symbol	Min	Max	Units	Condition
Data rate	-	10.3125 - 100 ppm	10.3125 + 100 ppm	Gbps	KR
Differential input return loss Note 4-31	RLI_{SDD11}	-	-9	dB	50 MHz to 2.5 GHz
Differential input return loss	RLI_{SDD11}	-	-9 + 12 x log (ƒ/2.5 GHz)	dB	2.5 GHz to 7.5 GHz

Note 4-31 Maximum insertion loss is 15 dB @ 5 GHz (10 Gbps) (vs ~25 dB based on the KR spec). This is to allow low cost interface implementation, while meeting system requirements.

TABLE 4-19: 25GBASE-KR/CR/SR/LR/ER TRANSMITTER

Parameter	Symbol	Min	Max	Units	Condition
Data rate	-	25.78125 - 100 ppm	25.78125 + 100 ppm	Gbps	-
Differential output return loss	RLO_{SDD22}	-	-12.05 + f	dB	50 MHz to 6 GHz
Differential output return loss	RLO_{SDD22}	-	-6.5 + 0.075f	dB	6 GHz to 19 GHz
Common-mode output return loss	RLO_{SCC22}	-	-9.05 + f	dB	50 MHz to 6 GHz
Common-mode output return loss	RLO_{SCC22}	-	-3.5 + 0.075f	dB	6 GHz to 19 GHz
Steady-state voltage	vf	0.4	0.6	V	25G BASE-KR
Steady-state voltage	vf	0.34	0.6	V	25G BASE-CR Note 4-32
Linear fit pulse peak	-	0.71 x vf	-	V	25G BASE-KR
Linear fit pulse peak	-	0.45 x vf		-	25G BASE-CR Note 4-32
Normalized coefficient step size	-	0.0083	0.05	-	-
Pre-cursor full-scale range	-	1.4	4	-	-
Signal-to-noise and distortion ratio	-	27	-	dB	25G BASE-KR
Signal-to-noise and distortion ratio	-	26	-	dB	25G BASE-CR Note 4-32
Even-odd jitter	$J_{even-odd}$	-	0.052	UI	Note 4-32
Effective bounded uncorrelated jitter	$J_{bounded-uncorr}$	-	0.1	UIP-P	Note 4-32
Effective Total uncorrelated jitter	$J_{total-uncorr}$	-	0.18	UIP-P	Note 4-32
Note 4-32 A test channel of 7 dB loss at 12.89 GHz was used.					

Note: Jitter specified with a jitter-free reference clock. Any **REFCLK** jitter with a frequency content below 7 MHz will add to the jitter generated at the 25 Gbps output.

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TABLE 4-20: 25GBASE-KR/CR/SR/LR/ER RECEIVER

Parameter	Symbol	Min	Max	Units	Condition
Data rate	-	25.78125 - 100 ppm	25.78125 + 100 ppm	Gbps	-
Differential intput return loss	RLI_{SDD11}	-	-12.05 + f	dB	50 MHz to 6 GHz
Differential input return loss	RLI_{SDD11}	-	-6.5 + 0.075f	dB	6 GHz to 19 GHz
Differential to common-mode return loss	RLI_{SCC11}	-	-25 + 1.44f	dB	50 MHz to 6.95 GHz
Differential to common-mode return loss	RLI_{SCC11}	-	-15	dB	6.95 GHz to 19 GHz
Jitter tolerance	J_{tol}	5	-	UI	190 kHz, RS-FEC error ratio < 10-4
Jitter tolerance	J_{tol}	1	-	UI	940 kHz, RS-FEC error ratio < 10-4

Note: Jitter specified with a jitter-free reference clock. Any **REFCLK** jitter with a frequency content below 7 MHz will add to the jitter generated at the 25 Gbps output.

4.6.4 TWI HOST TIMING

This section specifies the Twisted Wire Interface format and timing of the device.

FIGURE 4-1: TWI HOST TIMING

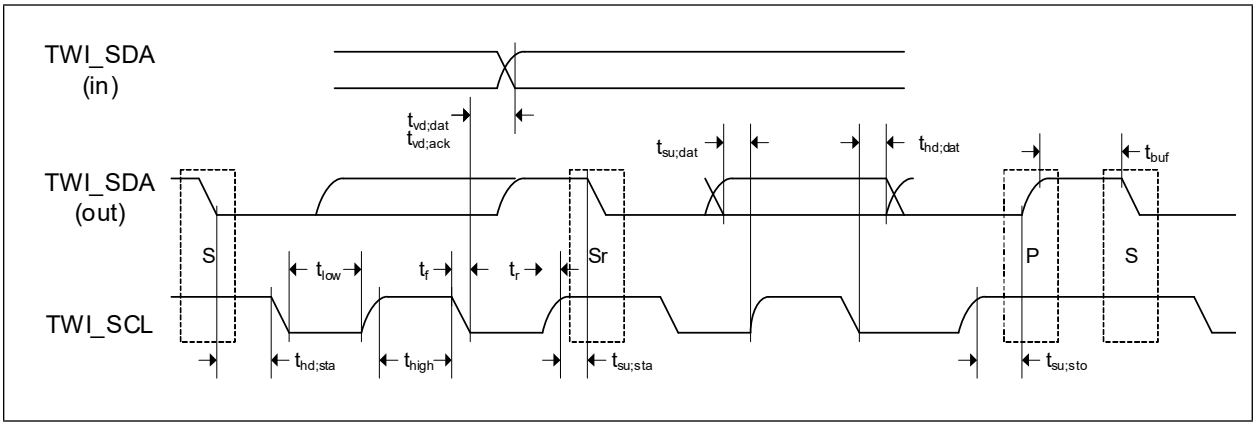

TABLE 4-21: TWI HOST TIMING VALUES

Symbol	Description	Standard Mode		Fast Mode		Fast Mode Plus		
		Min	Max	Min	Max	Min	Max	Units
f_{scl}	TWI_SCL clock frequency		100		400		1000	kHz
t_{high}	TWI_SCL high time (Note 4-33)	3.0		0.6		0.26		µs
t_{low}	TWI_SCL low time (Note 4-34)	4.7		1.2		0.48		µs
t_r	Rise time of TWI_SDA and TWI_SCL		1000		300		120	ns
t_f	Fall time of TWI_SDA and TWI_SCL		300		300		120	ns
$t_{su;sta}$	Setup time (provided to client) of TWI_SCL high before TWI_SDA output falling for repeated start condition (Note 4-35)	4.9		0.9		0.38		µs
$t_{hd;sta}$	Hold time (provided to client) of TWI_SCL after TWI_SDA output low for start or repeated start condition (Note 4-36)	4.5		0.9		0.38		µs
$t_{vd;dat}$	TWI_SDA data input valid (from client) after TWI_SCL low. (Note 4-37)		3400		850		400	ns
$t_{vd;ack}$	TWI_SDA acknowledge input valid (from client) after TWI_SCL low (Note 4-37)		3400		850		400	ns
$t_{su;dat}$	Setup time (provided to client) TWI_SDA output before TWI_SCL rising (Note 4-37)	300		150		100		ns
$t_{hd;dat}$	Hold time (provided to client) of TWI_SDA output after TWI_SCL falling (Note 4-37)	50	3400	50	850	50		ns
$t_{su;sto}$	Setup time (provided to client) of TWI_SCL high before TWI_SDA output rising for stop condition (Note 4-36)	4.5		0.9		0.38		µs
t_{buf}	Bus free time	4.7		1.3		0.5		µs
C_B	Capacitive load for TWI_SCL and TWI_SDA bus line		400		330			pF
R_P	External pull-up resistor (Note 4-38)	900	$8 \times 10^{-7}/C_B$	900	$3 \times 10^{-7}/C_B$			Ω

Note 4-33 Assumes worst case rise time and zero fall time. Nominally t_{high} is 40% of the period.

Note 4-34 Assumes worst case fall time and zero rise time. Nominally t_{low} is 60% of the period.

Note 4-35 These values provide 200, 300 and 120 (respectively) ns of margin compared to the I^2C specification.

Note 4-36 These values provide 500, 300 and 120 (respectively) ns of margin compared to the I^2C specification.

Note 4-37 These values provide 50 ns of margin compared to the I^2C specification.

Note 4-38 Minimum value is determined from IOL and internal reliability requirements. Maximum value is determined by load capacitance. Microchip recommends 10 kΩ for typical applications in which capacitance loads are below the specified minimums.

Note 4-39 Assumes a drive strength setting of 4 ma.

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4.6.5 MDC/MDIO CLIENT

This section specifies the MDC/MDIO format and timing of the device.

FIGURE 4-2: MDC/MDIO TIMING

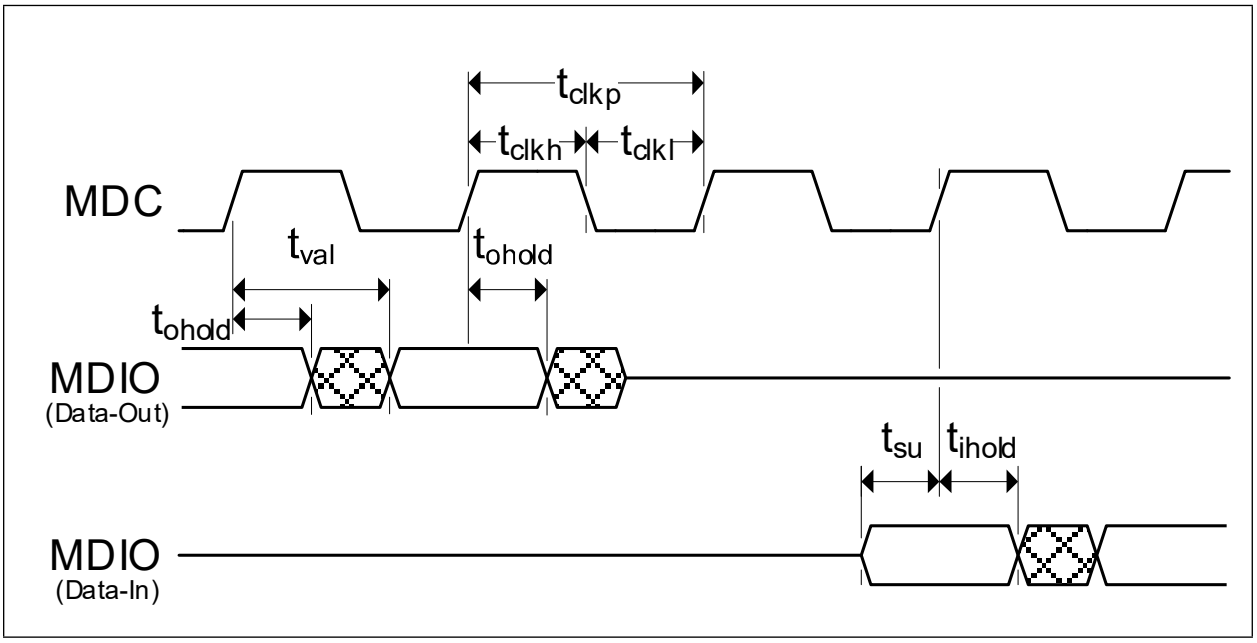

TABLE 4-22: MDC/MDIO TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{clkp}	**MDC** period	40	400	Note 4-40	ns
t_{clkh}	**MDC** high time	10			ns
t_{clkl}	**MDC** low time	10			ns
t_{val}	**MDIO** (read from PHY) output valid from rising edge of **MDC**	0		14	ns
t_{ohold}	**MDIO** (read from PHY) output hold from rising edge of **MDC**	0			ns
t_{su}	**MDIO** (write to PHY) input setup time to rising edge of **MDC**	8 Note 4-41			ns
t_{ihold}	**MDIO** (write to PHY) input hold time after rising edge of **MDC**	8 Note 4-41			ns

Note 4-40 As a client, the device can operate with MDC clock frequencies as low as in the range of 10s/100s of Hertz as could be generated by the host using bit banging techniques on its GPIO pins. There is no maximum clock period.

Note 4-41 These values provide 2 ns margin beyond the IEEE specification.

Note 4-42 Assumes PCB loading of 5 pf. Assumes a drive strength setting of 8 ma. Note that 8 ma is not the device default. Higher drive settings may achieve faster times especially at higher PCB loading.

4.6.6 SPI CLIENT

This section specifies the SPI format and timing of the device.t

FIGURE 4-3: SPI CLIENT NORMAL MODE

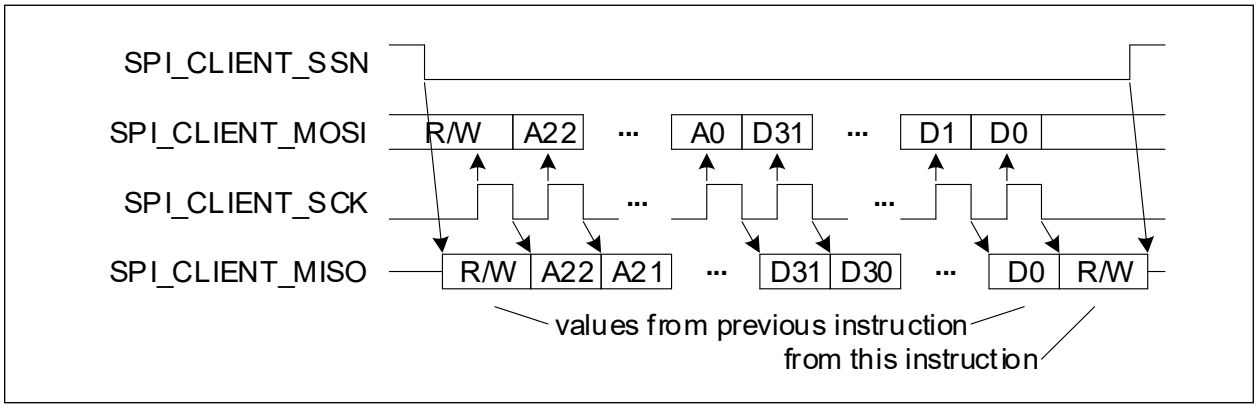

FIGURE 4-4: SPI CLIENT FAST MODE

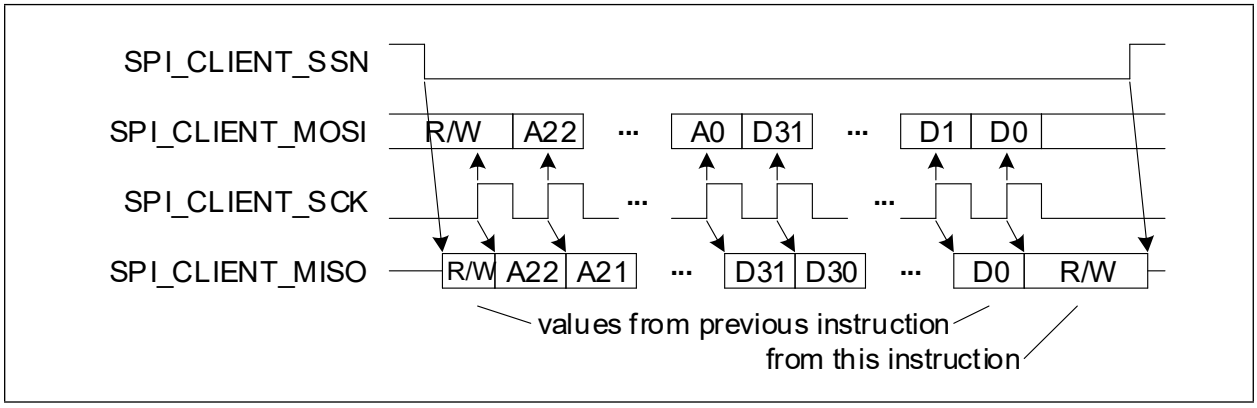

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FIGURE 4-5: SPI CLIENT TIMING

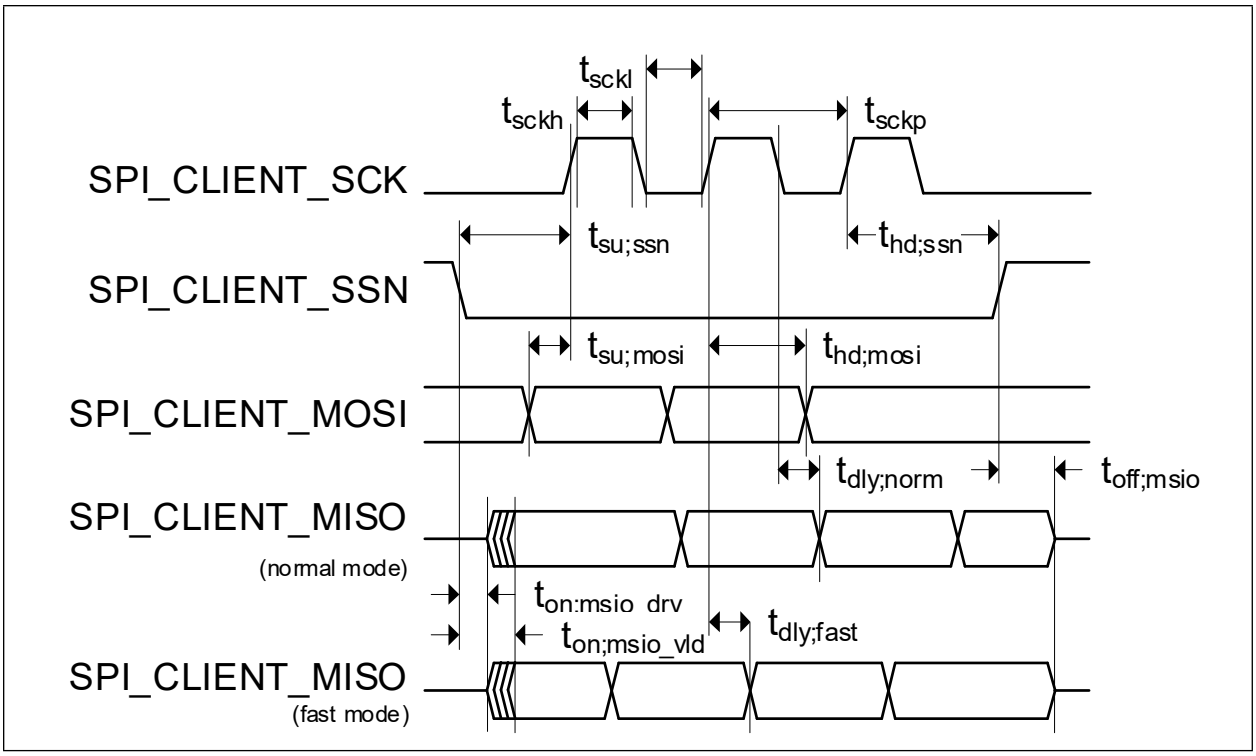

TABLE 4-23: SPI CLIENT TIMING VALUES

Symbol	Description	Min	Max	Units
t_{sckp}	**SPI_CLIENT_SCK** period - normal mode	50	Note 4-43	ns
	SPI_CLIENT_SCK period - fast mode	22	Note 4-43	ns
t_{sckh}	**SPI_CLIENT_SCK** high time - normal mode	22		ns
	SPI_CLIENT_SCK high time - fast mode	8		ns
t_{sckl}	**SPI_CLIENT_SCK** low time - normal mode	22		ns
	SPI_CLIENT_SCK low time - fast mode	8		ns
$t_{su;mosi}$	**SPI_CLIENT_MOSI** data setup time to **SPI_CLIENT_SCK** rising	8		ns
$t_{hd;mosi}$	**SPI_CLIENT_MOSI** data hold time from **SPI_CLIENT_SCK** rising	8		ns
$t_{su;ssn}$	**SPI_CLIENT_SSN** active setup time to **SPI_CLIENT_SCK** rising	12		ns
$t_{hd;ssn}$	**SPI_CLIENT_SSN** inactive hold time from **SPI_CLIENT_SCK** rising	SCK period + 12		ns
$t_{on;miso_drv}$	**SPI_CLIENT_SSN** transition low to **SPI_CLIENT_MISO** drive	0		ns

TABLE 4-23: SPI CLIENT TIMING VALUES (CONTINUED)

Symbol	Description	Min	Max	Units
$t_{on;miso_vld}$	**SPI_CLIENT_SSN** transition low to **SPI_CLIENT_MISO** valid		8 / 13 / 18 Note 4-45	ns
$t_{off;miso}$	**SPI_CLIENT_SSN** transition high to **SPI_CLIENT_MISO** high impedance		10	ns
$t_{dly;norm}$	Falling **SPI_CLIENT_SCK** to valid **SPI_CLIENT_MISO** data, normal mode	6 Note 4-44	16 / 20 / 25 Note 4-45	ns
$t_{dly;fast}$	Rising **SPI_CLIENT_SCK** to valid **SPI_CLIENT_MISO** data, fast mode	6 Note 4-44	16 / 20 / 25 Note 4-45	ns

Note 4-43 The device can operate with clock frequencies in the 10s/100s of Hertz.

Note 4-44 Guaranteed by design minimum of 2 system clock periods at 300 MHz.

Note 4-45 Assumes PCB loading of 5 pf, 50 pf and 100 pf respectively.
Assumes a drive strength setting of 8 ma. Note that 8 ma is not the device default. Higher drive settings may achieve faster times especially at higher PCB loading

Device input to output time only. Does not include PCB routing delay or host setup time.

The data output propagation delay may require delayed data sampling at the Host (i.e. data output is valid into the next clock cycle) or the use of a lower frequency.

4.6.7 RECOVERED CLOCK TIMING REQUIREMENTS

The recovered clock output duty cycle requirement is 40% minimum, 50% typical, 60% maximum.

TABLE 4-24: RECOVERED CLOCK RISE / FALL TIME

Symbol	Description	Condition	Min	Typ	Max	Units
t_{rise}	Rise time	8 ma drive, 10 pF load, 3.3V IO Supply	0.67	0.84	1.15	ns
		8 ma drive, 10 pF load, 1.8V IO Supply	0.71	0.85	0.90	ns
		8 ma drive, 25 pF load, 3.3V IO Supply	1.31	1.64	2.27	ns
		8 ma drive, 25 pF load, 1.8V IO Supply	1.30	1.58	1.68	ns
t_{fall}	Fall time	8 ma drive, 10 pF load, 3.3V IO Supply	0.61	0.73	0.98	ns
		8 ma drive, 10 pF load, 1.8V IO Supply	0.69	0.83	0.86	ns
		8 ma drive, 25 pF load, 3.3V IO Supply	1.15	1.39	1.50	ns
		8 ma drive, 25 pF load, 1.8V IO Supply	1.24	1.51	1.60	ns

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TABLE 4-25: RECOVERED CLOCK OUT FREQUENCIES

Operating Mode	Internal Recovered Clock Frequency (MHz)	N	Recovered Clock Out Frequency (MHz)
1G	125.00	1	125.00
		2	62.50
		4	31.25
		8	15.625
10G	257.8125	1	Reserved
		2	128.90625
		4	64.453125
		8	32.2265625
25G	644.53125	1	Reserved
		2	Reserved
		4	Reserved
		8	80.56640625

4.6.8 RESET PIN CONFIGURATION STRAP TIMING

Figure 4-6 illustrates the **RESET_N** timing requirements and its relation to the configuration straps. In addition to the specified power and clock stable minimum duration, **RESET_N** must be asserted for the minimum period specified.

FIGURE 4-6: RESET_N CONFIGURATION STRAP TIMING

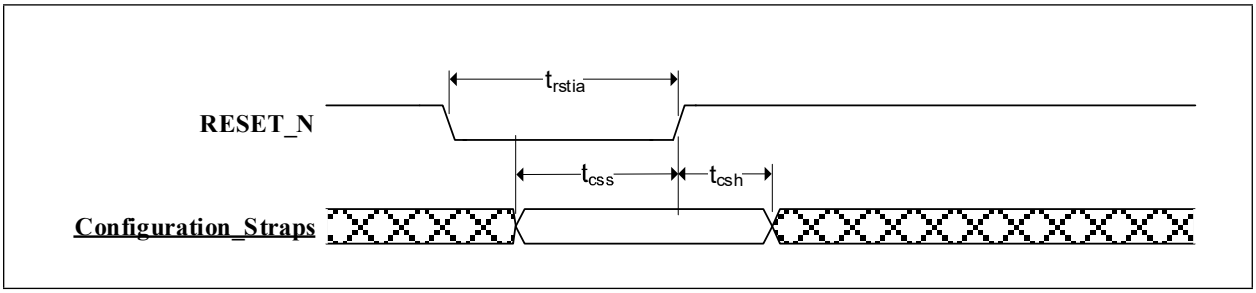

TABLE 4-26: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	Min	Max	Units
t_{rstia}	**RESET_N** input assertion time	1		µs
t_{css}	Configuration strap setup before **RESET_N** deassertion	10		ns
t_{csh}	Configuration strap hold after **RESET_N** deassertion	10		ns
t_{odad}	Output drive after **RESET_N** deassertion	150		ns

4.6.9 JTAG TIMING VALUES

4.6.9.1 JTAG Timing Requirements

The JTAG test tap must run at 25 MHz or better.

FIGURE 4-7: JTAG TIMING

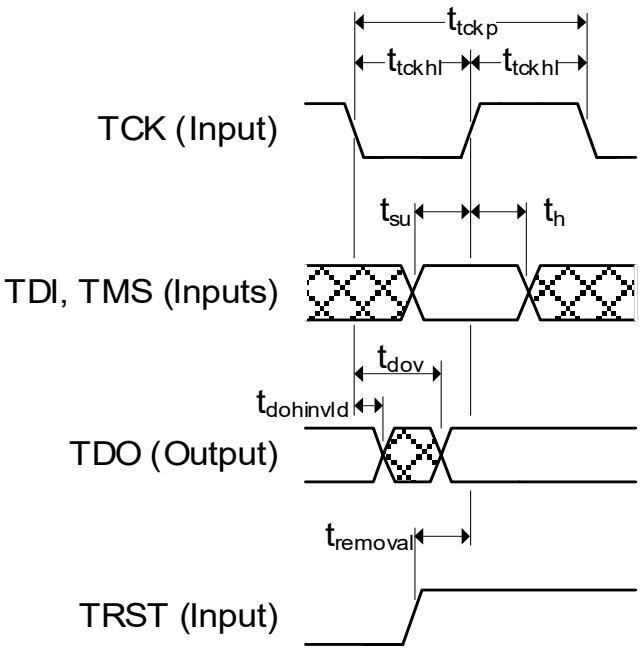

TABLE 4-27: JTAG TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{tckp}	**TCK** clock period	40		ns	ns
t_{tckhl}	**TCK** clock high/low time	t_{tckp}*0.4		t_{tckp}*0.6	ns
t_{su}	**TDI**, **TMS** setup to **TCK** rising edge	10			ns
t_h	**TDI**, **TMS** hold from **TCK** rising edge	10			ns
t_{dov}	**TDO** output valid from **TCK** falling edge			16	ns
$t_{doinvld}$	**TDO** output invalid from **TCK** falling edge	0			ns
$t_{removal}$	**TRST** release before **TCK** rising edge	10			ns

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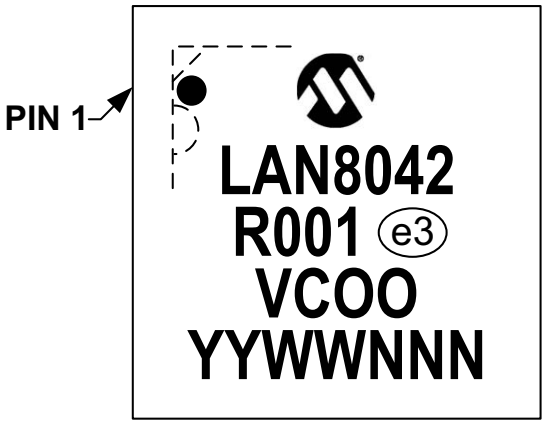
TABLE 4-27: JTAG TIMING VALUES (CONTINUED)

Symbol	Description	Min	Typ	Max	Units
Note:	Assumes PCB loading of 25 pf. Assumes a drive strength setting of 8 mA.				

5.0 PACKAGE INFORMATION

5.1 Top Marking



Legend:

R	Product revision
000	Internal code
e3	Pb-free JEDEC® designator for Matte Tin (Sn)
V	Plant of assembly
COO	Country of origin
YY	Year code (last two digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information

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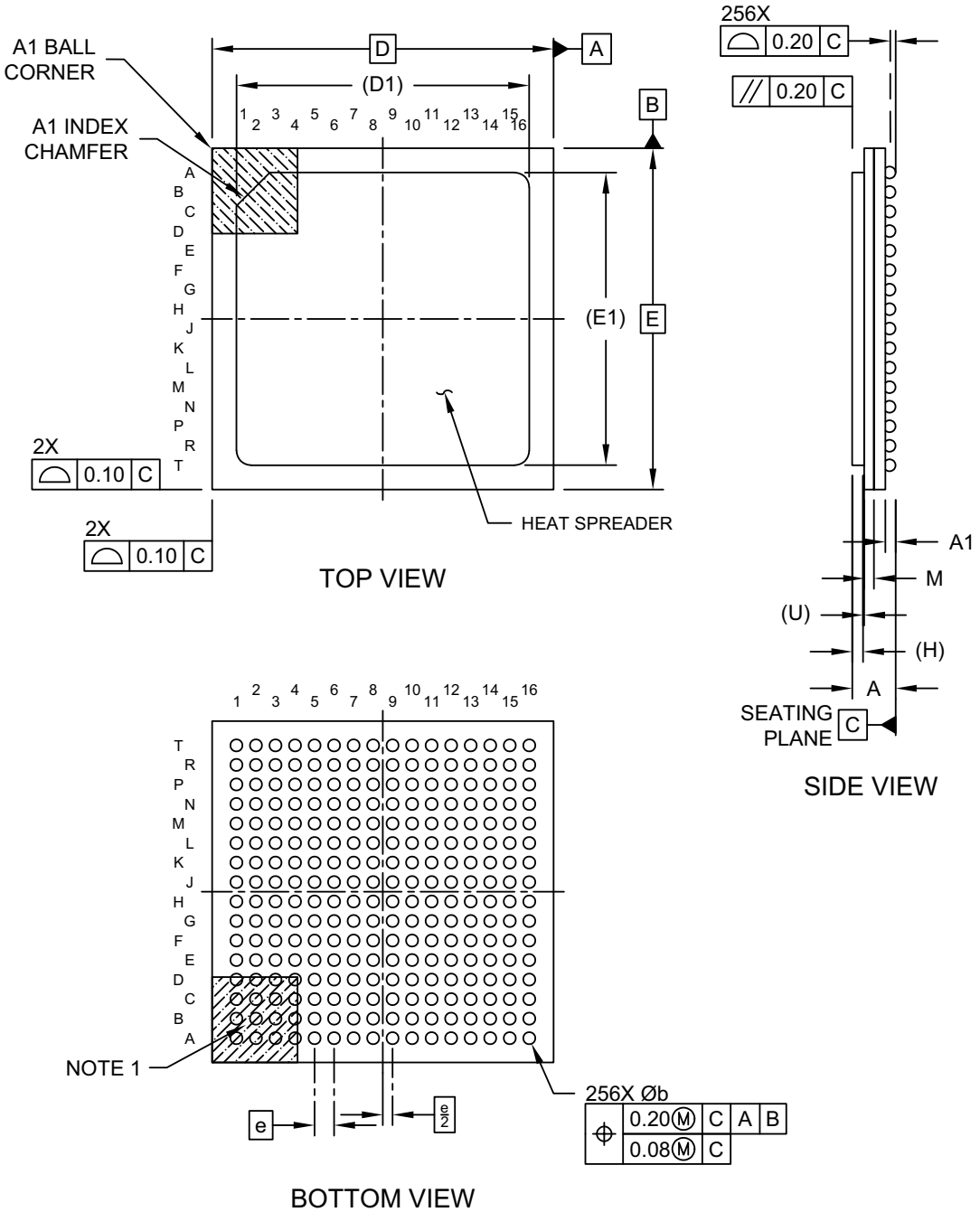
5.2 256-BGA

FIGURE 5-1: 256-BGA PACKAGE DRAWING

256-Ball FlipChip Chip Scale Package (3HW) - 14x14x1.78 mm Body [FCCSP] With Heat Spreader

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-563 Rev B Sheet 1 of 2

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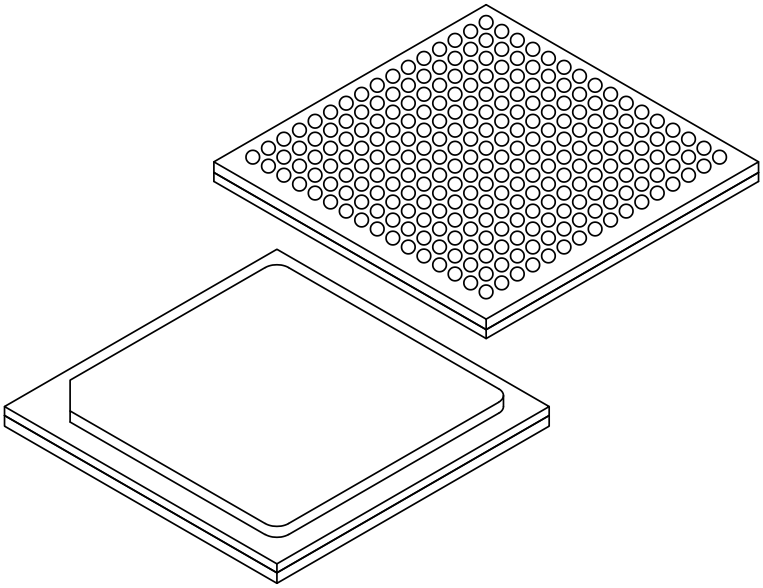
FIGURE 5-2: 256-BGA DIMENSIONS

256-Ball FlipChip Chip Scale Package (3HW) - 14x14x1.78 mm Body [FCCSP] With Heat Spreader

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	256		
Pitch	e	0.80 BSC		
Overall Height	A	1.48	1.63	1.78
Ball Height	A1	0.37	0.42	0.47
Mold Cap Thickness	M	0.35	0.40	0.45
Heat Seperator Epoxy Thickness	U	0.05 REF		
Heat Spreader Thickness	H	0.30 REF		
Overall Length	D	14.00 BSC		
Heat Spreader Length	D1	12.00 REF		
Overall Width	E	14.00 BSC		
Heat Spreader Width	E1	12.00 REF		
Ball Diameter	b	0.46	0.51	0.56

Notes:

1. Pin 1 visual index feature may vary but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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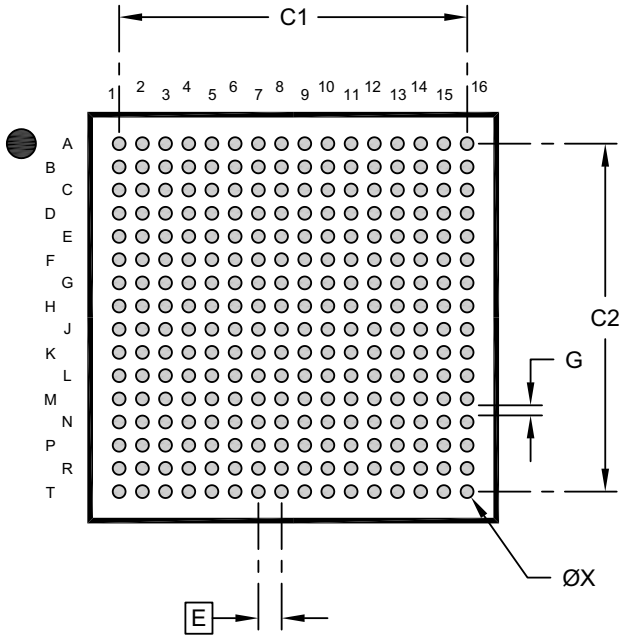
FIGURE 5-3: 256-BGA LAND PATTERN

256-Ball FlipChip Chip Scale Package (3HW) - 14x14x1.78 mm Body [FCCSP] With Heat Spreader

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		12.00	
Contact Pad Spacing	C2		12.00	
Contact Pad Diameter (X256)	X			0.45
Contact Pad to Contact Pad	G	0.35		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, please refer to current industry standard IPC-7093.

Microchip Technology Drawing C04-2563 Rev B

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APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005096E (11-03-25)		Removed confidential footer
DS00005096D (09-19-25)	Table 2-1, "256-BGA Ball Assignments", Table 2-2, "256-BGA BALL Assignments (9-16)"	Updated thermal diode pin assignments: • L13 was THERMD_Sp, now THERMD_Sn. • M13 was THERMD_Sn, now THERMD_Sp. • N13 was THERMD_Fp, now THERMD_Fn. • P13 was THERMD_Fn, now THERMD_Fp.
	Table 2-3, "Pin Descriptions", Table 2-4, "GPIO Alternate Functions / System Usage"	Updated GPIOs descriptions and notes to state that internal pull-ups are enabled by default.
	Table 2-6, "Buffer Type Descriptions"	Description change for buffer PU: “pull-downs” changed to “pull-ups”
	Section 2.3, Buffer Types	Added definition for Pull-ups (PU).
	Section 3.2.4, PCS25G	Added bullet regarding Local Fault Detection.
	Section 3.2.6.2.2, Hardware W/P Switch Failover	Added description for Connection Fault Detection filtering.
	Section 3.12, GPIOs	Added information on default setting of GPIO pull-up enable.
	Table 3-13, "SPI Client Instruction Format"	Added SPI Client instructions for register bit formatting.
	Table 4.3, "Package Thermal Specifications"	Updated Package Thermal values.
	Table 4.4, "Power Consumption"	Added Power consumption values.
	Table 5.0, "Package Information"	Update of Top Marking and 256-BGA Package figures.
DS00005096C (06-03-24)	Section 3.8.3, Synchronous Ethernet and Recovered Clocks	Added the following text to the 8th bullet point in this section: “Note that when squelched, the recovered clocks can stop either high or low.”
	Section 4.3, Package Thermal Specifications, Section 4.6, AC Specifications, Section 4.6.4, TWI Host Timing, Section 4.6.5, MDC/MDIO Client, Section 4.6.6, SPI Client, Section 4.6.8, Reset Pin Configuration Strap Timing, Section 4.6.9, JTAG Timing Values	New sections added.
	Section 5.2, 256-BGA	Added updated Package Drawing, Dimensions and Land Pattern.
DS00005096B (11-03-23)	Section 4.1, Absolute Maximum Ratings* and Section 4.2, Operating Conditions**	Updated positive and negative voltage numbers for **VDDO_A** and **VDDO_B**.
DS00005096A (10-27-23)	All	Initial Release

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-	X	/	XXX
Device		Temperature Range		Package

Device:	LAN8042	= Quad 1G/10G/25G PHY w/ MACsec
Temperature Range:	V	= -40°C (T_A) to +110°C (T_J) (Extended Temperature)
Package:	3HW	= 256-ball HFC-BGA

Example:

a) LAN8042-V/3HW
Tray, -40°C (T_A) to +110°C (T_J), 256-ball BGA

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