dsPIC33CDVL256MC506 Family Data Sheet

16-Bit Digital Signal Controllers with High-Speed PWM, CAN Flexible Data-Rate (CAN FD), MOSFET Gate Driver and LIN Transceiver

Operating Conditions

- 3.0V to 3.6V: -40°C to +125°C, DC to 100 MIPS
- 3.0V to 3.6V: -40°C to +150°C, DC to 70 MIPS

Host dsPIC DSC Features

- Based on dsPIC33CK256MC506
- 16-Bit Wide Data Path
- Code-Efficient (C and Assembly) Architecture
- 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle, Mixed-Sign Multiply:
  - 32-bit multiply support
- Fast Six-Cycle Divide
- Zero-Overhead Looping

High-Resolution PWM

- Four PWM Pairs
- Up to 2 ns PWM Resolution
- Dead Time for Rising and Falling Edges
- Dead-Time Compensation
- Clock Chopping for High-Frequency Operation
- PWM Support for:
  - DC/DC, AC/DC, inverters, PFC, lighting
  - BLDC, PMSM, ACIM, SRM motors
- Fault and Current Limit Inputs
- Flexible Trigger Configuration for ADC Triggering

High-Speed Analog-to-Digital Converter

- Up to 20 A/D Inputs
- 12-Bit Resolution
- One Shared SAR ADC Core
- Up to 3.5 Msps Conversion Rate per Core
- Dedicated Result Buffer for Each Analog Channel
- Flexible and Independent ADC Trigger Sources

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- Four Digital Comparators
- Four Oversampling Filters

Analog Features

- Two 15 ns Analog Comparators
- Three Op Amps:
  - 20 MHz GBW, 40 v/µs slew rate
- Two 12-Bit PDM DAC with Slope Compensation
  - One buffered DAC output

Microcontroller Features

- Up to 256 Kbytes Flash Memory:
  - Ten thousand erase/write cycle endurance
  - Twenty years minimum data retention
  - Self-programmable under software control
  - Programmable code protection
  - Error Code Correction (ECC)
  - Flash OTP by ICSP™ Write Inhibit
- Up to 32 Kbytes SRAM Memory:
  - SRAM Memory Built-In Self-Test (MBIST)
  - Multiple interrupt vectors with individually programmable priority
  - Four sets of interrupt context saving registers, which include accumulator and STATUS, for fast reserved interrupt handling
- Four External Interrupt Pins
- Watchdog Timer (WDT)
- Windowed Deadman Timer (DMT)
  - Fail-Safe Clock Monitor (FSCM) with dedicated oscillator
- Selectable Oscillator Options Including:
  - High-precision, 8 MHz internal Fast RC (FRC) oscillator
  - Primary high-speed, crystal/resonator oscillator or external clock
  - Primary PLL, which can be clocked from FRC or crystal oscillator
- Low-Power Management Modes (Sleep and Idle)
- Power-on Reset and Brown-out Reset
- On-Board Capacitorless Regulator
  - 384 bytes of One-Time-Programmable (OTP) memory
- High-Current I/O Sink/Source
  - Edge or level change notification interrupt on I/O pins
- Peripheral Pin Select (PPS) Remappable Pins

Debug Features

- Three Programming and Debugging Interfaces:
  - Two-wire ICSP™ interface with non-intrusive access and real-time data exchange with the application

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- Three Complex, Five Simple Breakpoints
  - IEEE Standard 1149.2 compatible (JTAG) boundary scan

Peripheral Features

- Two Four-Wire SPI modules:
  - 16-byte FIFO
  - Variable width
  - I2S mode
- One I^2C Host and Client w/Address Masking and IPMI Support
- Three Protocol UARTs with Automated Handling Support for:
  - LIN 2.2
  - DMX
  - Smart card (ISO 7816)
- One SENT module
- One CAN Flexible Data (FD) module
- Timers/Counters:
  - One dedicated 16-bit timer/counter
  - Four Single Output Capture/Compare/PWM/ Timer (SCCP) modules:
    - Flexible configuration as PWM, input capture, output compare or timers
    - Two 16-bit timers or one 32-bit timer in each module
    - PWM resolution down to 2.5 ns
    - Single PWM output
- One Quadrature Encoder Interface (QEI):
  - Four inputs: Phase A, Phase B, Home, Index
    - One 32-bit timer/counter (in QEI module, available if encoder is not used)
- Reference Clock Output (REFCLKO)
  - Four Configurable Logic Cells (CLC) with internal connections to select peripherals and PPS
- Four-Channel Hardware DMA
- 32-Bit CRC Calculation Module
- Peripheral Trigger Generator (PTG):
  - Sixteen possible trigger sources to other peripheral modules
  - CPU-independent state machine-based instruction sequencer
  - Two 16-bit general purpose timers

LIN Transceiver Module (Based on ATA663211 Device) (dsPIC33CDVLXXXMCX06 Only)

- LIN_BUS Voltage Up to 40V
- LIN_VDD Voltage = 5V to 28V
- Very Low Supply Current:
  - Sleep mode: typically 9 µA
  - Fail-Safe mode: typically 80 µA

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  - Normal mode: typically 250 µA
- Fully Compatible with 3.3V and 5V Devices
- LIN Physical Layer According to LIN 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2
  - Wake-up capability via LIN_BUS activity (100 µs dominant)
  - External wake-up via LIN_WKIN pin (100 µs low level)

Safety Features

- Backup Fast RC Oscillator (BFRC)
- Brown-out Reset (BOR)
- Capless Internal Voltage Regulator
- Clock Monitor System with Backup Oscillator
- CodeGuard™ Security
- Cyclic Redundancy Check (CRC)
- Dual Watchdog Timer (WDT)
- Fail-Safe Clock Monitoring (FSCM)
- Flash Error Correcting Code (ECC)
- Flash OTP by ICSP™ Write Inhibit
- RAM Memory Built-In Self-Test (MBIST)
- Two-Speed Start-up
- Virtual Pins for Redundancy and Monitoring
- Windowed Deadman Timer (DMT)

MOSFET Gate Driver Module (Based on MCP8021 Device)

- Three Half-Bridge Drivers Configured to Drive External High-Side NMOS and Low-Side NMOS MOSFETs:
  - Peak output current: 0.5A @ 12V
  - Shoot-through protection
  - Overcurrent and short-circuit protection
- Fixed Output Linear Regulator:
  - 3.3V @ 70 mA
  - True current foldback
- Protection Features:
  - Gate drive undervoltage lockout: 4.5V
    - Supply voltage undervoltage shutdown: 4.5V
    - Supply voltage undervoltage lockout (UVLO): 6.25V
  - Overvoltage lockout (OVLO): 32V
  - Transient (100 ms) voltage tolerance: 40V
  - Power module thermal shutdown

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Functional Safety Readiness – ISO 26262/ IEC 61508/IEC 60730

- To learn about the Functional Safety Readiness of this device family and the various Functional Safety standards an application can target using this device family, visit www.microchip.com/dsPIC33-Functional-Safety.

dsPIC33CDVL256MC506 Product Families

The features of the dsPIC33CDVL256MC506 family devices are listed in Table 1.

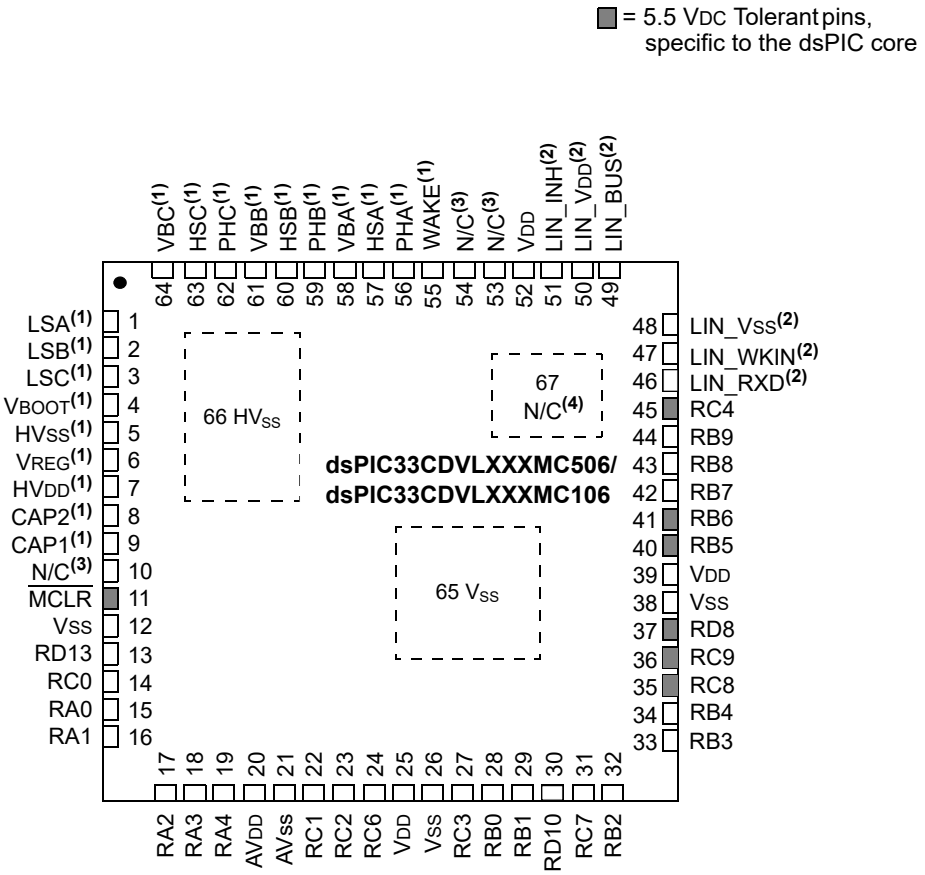
Table 1. dsPIC33CDVL256MC506 Family Device Features

Device	Pins	Flash (Kbytes)	SRAM (Kbytes)	DMA # of Ch	GPIO/PPS	LIN Transceiver	MOSFET Gate Driver	16-Bit Timer	SCCP	UART	SPI	I2C	SENT	CAN-FD	MC PWM	PWM Res (ns)	QEI	12-Bit ADC Module	ADC Channels	Op Amp	Analog Comp w/12-Bit DAC	PTG	CLC	REFO	CRC	WDT/DMT
dsPIC33CDVL128MC506	64	128	16	4	27/22	1	1	1	4	3	2	1	1	1	4x2	2	1	1	20	3	2	1	4	1	1	1/1
dsPIC33CDV128MC506	64	128	16	4	30/25	0	1	1	4	3	2	1	1	1	4x2	2	1	1	20	3	2	1	4	1	1	1/1
dsPIC33CDVL256MC506	64	256	32	4	27/22	1	1	1	4	3	2	1	1	1	4x2	2	1	1	20	3	2	1	4	1	1	1/1
dsPIC33CDV256MC506	64	256	32	4	30/25	0	1	1	4	3	2	1	1	1	4x2	2	1	1	20	3	2	1	4	1	1	1/1
dsPIC33CDVL128MC106	64	128	16	4	27/22	1	1	1	4	3	2	1	1	0	4x2	2	1	1	20	3	2	1	4	1	1	1/1
dsPIC33CDV128MC106	64	128	16	4	30/25	0	1	1	4	3	2	1	1	0	4x2	2	1	1	20	3	2	1	4	1	1	1/1
dsPIC33CDVL256MC106	64	256	32	4	27/22	1	1	1	4	3	2	1	1	0	4x2	2	1	1	20	3	2	1	4	1	1	1/1
dsPIC33CDV256MC106	64	256	32	4	30/25	0	1	1	4	3	2	1	1	0	4x2	2	1	1	20	3	2	1	4	1	1	1/1

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Pin Diagrams

64-Pin 9x9mm VGQFN (8QW)



Notes:

1. These pins are specific to the MOSFET gate driver module.
2. These pins are specific to the LIN transceiver module.
3. The pin is connected to a device interconnect.
4. The pin has no electrical connection to the device, but it is recommended to connect it to V_{SS}/LIN_V_{SS} in the PCB design to improve thermal dissipation.

Table 2. dsPIC33CDVLXXXMC506/dsPIC33CDVLXXXMC106 Complete Pin Functions

Pin	Function	Pin	Function
1	LSA	35	**RP56**/ASDA1/SCK2/RC8
2	LSB	36	**RP57**/ASCL1/SDI2/RC9
3	LSC	37	**RP72**/SDO2/PCI19/RD8
4	V_{BOOT}	38	V_{SS}
5	HV_{SS}	39	V_{DD}
6	V_{REG}	40	PGD3/**RP37**/RB5
7	HV_{DD}	41	PGC3/**RP38**/RB6
8	CAP2	42	AN2/**RP39**/RB7
9	CAP1	43	PGD1/AN10/**RP40**/SCL1/RB8

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Table 2. dsPIC33CDVLXXXMC506/dsPIC33CDVLXXXMC106 Complete Pin Functions (continued)

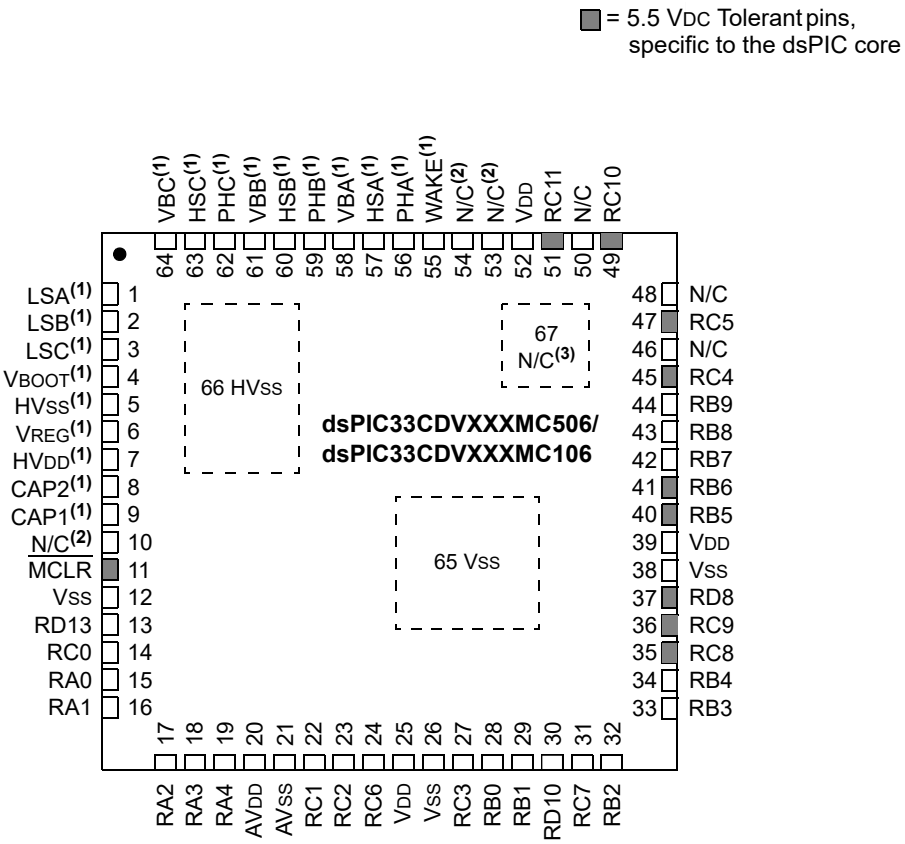
Pin	Function	Pin	Function
10	N/C(1)	44	PGC1/AN11/**RP41**/SDA1/RB9
11	$\overline{MCLR}$	45	**RP52**/RC4
12	V_{SS}	46	LIN_RXD
13	ANN0/**RP77**/RD13	47	LIN_WKIN
14	AN12/**RP48**/RC0	48	LIN_Vss
15	OA1OUT/AN0/CMP1A/IBIAS0/RA0	49	LIN_BUS
16	OA1IN-/AN16/RA1	50	LIN_VDD
17	OA1IN+/AN9/RA2	51	LIN_INH
18	DACOUT/AN3/CMP1C/RA3	52	V_{DD}
19	OA3OUT/AN4/IBIAS3/RA4	53	N/C(1)
20	AV_{DD}	54	N/C(1)
21	AV_{SS}	55	WAKE
22	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/RC1	56	PHA
23	OA3IN+/AN14/ISRC1/**RP50**/RC2	57	HSA
24	AN19/IBIAS1/**RP54**/RC6	58	VBA
25	V_{DD}	59	PHB
26	V_{SS}	60	HSB
27	AN15/CMP2A/IBIAS2/**RP51**/RC3	61	VBB
28	OSCI/CLKI/AN5/**RP32**/RB0	62	PHC
29	OSCO/CLKO/AN6/**RP33**/RB1	63	HSC
30	AN18/ISRC3/**RP74**/RD10	64	VBC
31	AN7/ISRC2/**RP55**/RC7	65	V_{SS}(2)
32	OA2OUT/AN1/CMP1D/CMP2D/**RP34**/INT0/RB2	66	HVss(2)
33	PGD2/OA2IN-/AN8/**RP35**/RB3	67	N/C(3)
34	PGC2/OA2IN+/AN17/**RP36**/RB4		

Legend: RPn represents remappable pins for the Peripheral Pin Select (PPS) function.
Notes:

1. Pin is connected to a device interconnect.
2. Pin is connected to a device exposed pad.
3. The pin has no electrical connection to the device, but it is recommended to connect it to V_{SS}/LIN_V_{SS} in the PCB design to improve thermal dissipation.

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64-Pin 9x9mm VGQFN (8QW)



Notes:

1. These pins are specific to the MOSFET gate driver module.
2. The pin is connected to a device interconnect.
3. The pin has no electrical connection to the device but is recommended to be connected to V_{SS} in the PCB design to improve thermal dissipation.

Table 3. dsPIC33CDVXXXMC506/dsPIC33CDVXXXMC106 Complete Pin Functions

Pin	Function	Pin	Function
1	LSA	35	**RP56**/ASDA1/SCK2/RC8
2	LSB	36	**RP57**/ASCL1/SDI2/RC9
3	LSC	37	**RP72**/SDO2/PCI19/RD8
4	V_{BOOT}	38	V_{SS}
5	HV_{SS}	39	V_{DD}
6	V_{REG}	40	PGD3/**RP37**/RB5
7	HV_{DD}	41	PGC3/**RP38**/RB6
8	CAP2	42	AN2/**RP39**/RB7
9	CAP1	43	PGD1/AN10/**RP40**/SCL1/RB8
10	N/C(1)	44	PGC1/AN11/**RP41**/SDA1/RB9
11	$\overline{MCLR}$	45	**RP52**/RC4
12	V_{SS}	46	N/C

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Table 3. dsPIC33CDVXXXMC506/dsPIC33CDVXXXMC106 Complete Pin Functions (continued)

Pin	Function	Pin	Function
13	ANN0/**RP77**/RD13	47	**RP53**/RC5
14	AN12/**RP48**/RC0	48	N/C
15	OA1OUT/AN0/CMP1A/IBIAS0/RA0	49	**RP58**/RC10
16	OA1IN-/AN16/RA1	50	N/C
17	OA1IN+/AN9/RA2	51	**RP59**/RC11
18	DACOUT/AN3/CMP1C/RA3	52	V_{DD}
19	OA3OUT/AN4/IBIAS3/RA4	53	N/C(1)
20	AVdd	54	N/C(1)
21	AV_{SS}	55	WAKE
22	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/RC1	56	PHA
23	OA3IN+/AN14/ISRC1/**RP50**/RC2	57	HSA
24	AN19/IBIAS1/**RP54**/RC6	58	VBA
25	V_{DD}	59	PHB
26	V_{SS}	60	HSB
27	AN15/CMP2A/IBIAS2/**RP51**/RC3	61	VBB
28	OSCI/CLKI/AN5/**RP32**/RB0	62	PHC
29	OSCO/CLKO/AN6/**RP33**/RB1	63	HSC
30	AN18/ISRC3/**RP74**/RD10	64	VBC
31	AN7/ISRC2/**RP55**/RC7	65	V_{SS}(2)
32	OA2OUT/AN1/CMP1D/CMP2D/**RP34**/INT0/RB2	66	HV_{SS}(2)
33	PGD2/OA2IN-/AN8/**RP35**/RB3	67	N/C(3)
34	PGC2/OA2IN+/AN17/**RP36**/RB4		

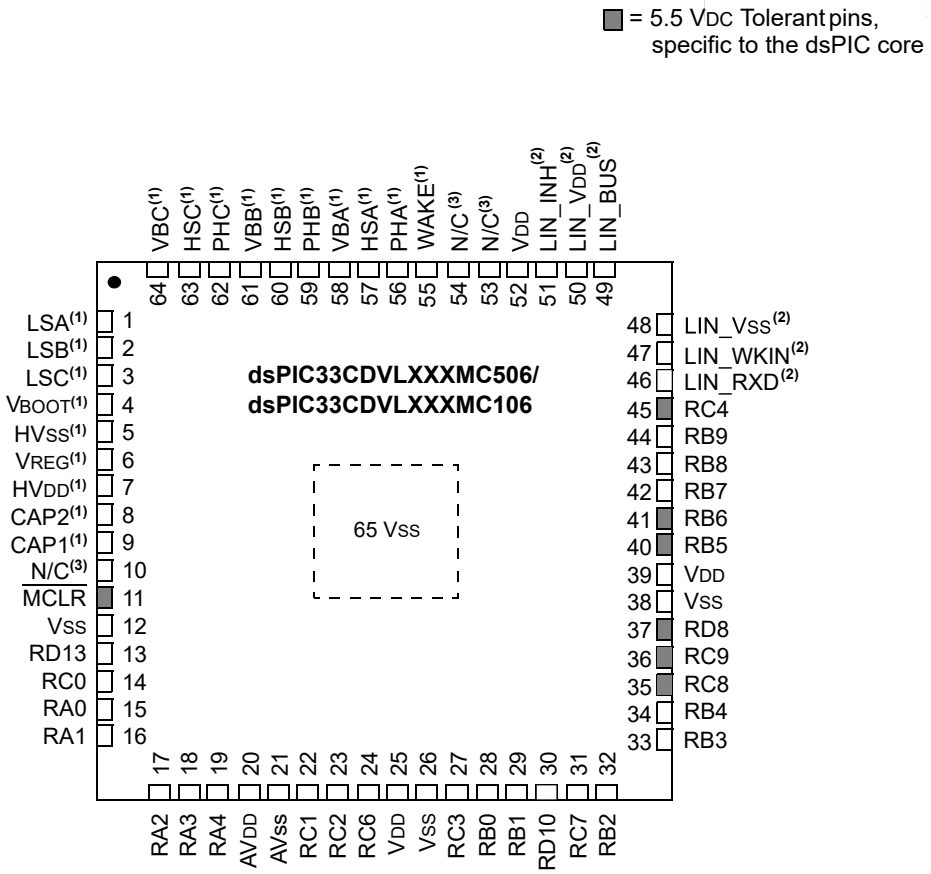
Legend: RPn represents remappable pins for the Peripheral Pin Select (PPS) function.

Notes:

1. Pin is connected to a device interconnect.
2. Pin is connected to a device exposed pad.
3. Pin has no electrical connection to the device but is recommended to be connected to V_{SS}/HV_{SS} in the PCB design to improve thermal dissipation.

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64-Pin 8x8mm VQFN (8PW)



Notes:

1. These pins are specific to the MOSFET gate driver module.
2. These pins are specific to the LIN transceiver module.
3. The pin is connected to a device interconnect.

Table 4. dsPIC33CDVLXXXMC506/dsPIC33CDVLXXXMC106 Complete Pin Functions

Pin	Function	Pin	Function
1	LSA	34	PGC2/OA2IN+/AN17/**RP36**/RB4
2	LSB	35	**RP56**/ASDA1/SCK2/RC8
3	LSC	36	**RP57**/ASCL1/SDI2/RC9
4	V_{BOOT}	37	**RP72**/SDO2/PCI19/RD8
5	HV_{SS}	38	V_{SS}
6	V_{REG}	39	V_{DD}
7	HV_{DD}	40	PGD3/**RP37**/RB5
8	CAP2	41	PGC3/**RP38**/RB6
9	CAP1	42	AN2/**RP39**/RB7
10	N/C(1)	43	PGD1/AN10/**RP40**/SCL1/RB8
11	$\overline{MCLR}$	44	PGC1/AN11/**RP41**/SDA1/RB9
12	V_{SS}	45	**RP52**/RC4

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Table 4. dsPIC33CDVLXXXMC506/dsPIC33CDVLXXXMC106 Complete Pin Functions (continued)

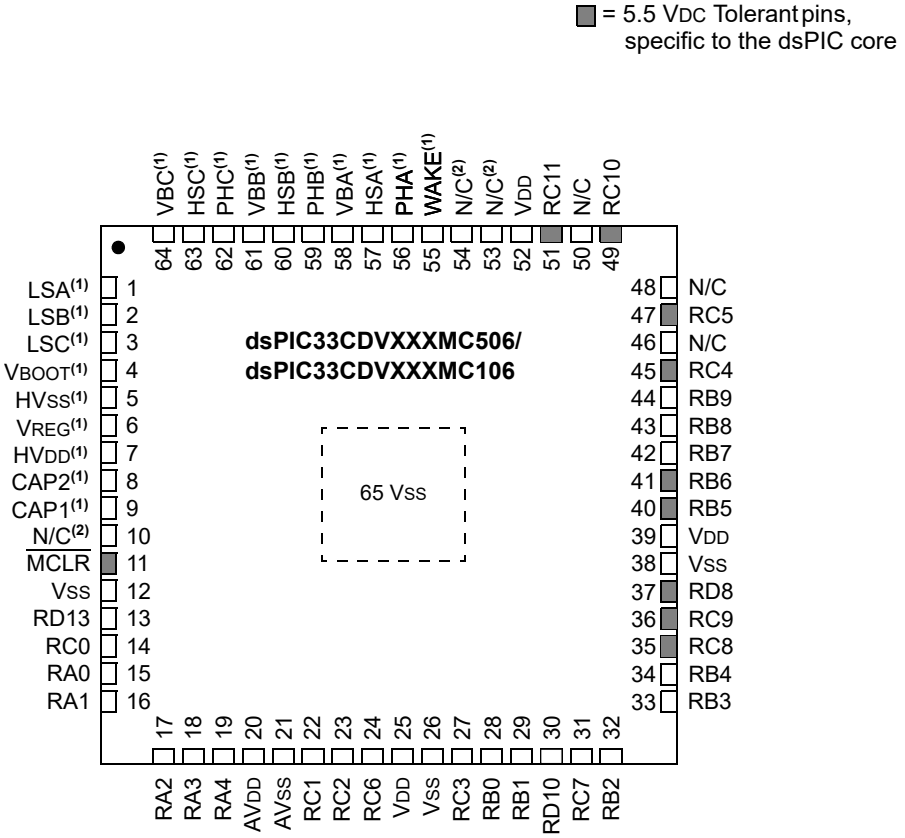
Pin	Function	Pin	Function
13	ANN0/**RP77**/RD13	46	LIN_RXD
14	AN12/**RP48**/RC0	47	LIN_WKIN
15	OA1OUT/AN0/CMP1A/IBIAS0/RA0	48	LIN_V_{SS}
16	OA1IN-/AN16/RA1	49	LIN_BUS
17	OA1IN+/AN9/RA2	50	LIN_V_{DD}
18	DACOUT/AN3/CMP1C/RA3	51	LIN_INH
19	OA3OUT/AN4/IBIAS3/RA4	52	V_{DD}
20	AVdd	53	N/C(1)
21	AV_{SS}	54	N/C(1)
22	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/RC1	55	WAKE
23	OA3IN+/AN14/ISRC1/**RP50**/RC2	56	PHA
24	AN19/IBIAS1/**RP54**/RC6	57	HSA
25	V_{DD}	58	VBA
26	V_{SS}	59	PHB
27	AN15/CMP2A/IBIAS2/**RP51**/RC3	60	HSB
28	OSCI/CLKI/AN5/**RP32**/RB0	61	VBB
29	OSCO/CLKO/AN6/**RP33**/RB1	62	PHC
30	AN18/ISRC3/**RP74**/RD10	63	HSC
31	AN7/ISRC2/**RP55**/RC7	64	VBC
32	OA2OUT/AN1/CMP1D/CMP2D/**RP34**/INT0/RB2	65	V_{SS}(2)
33	PGD2/OA2IN-/AN8/**RP35**/RB3		

Legend: RPn represents remappable pins for the Peripheral Pin Select (PPS) function.
Notes:

1. Pin is connected to a device interconnect.
2. Pin is connected to a device exposed pad.

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64-Pin 8x8mm VQFN (8PW)



Notes:

1. These pins are specific to the MOSFET gate driver module.
2. The pin is connected to a device interconnect.

Table 5. dsPIC33CDVXXXMC506/dsPIC33CDVXXXMC106 Complete Pin Functions

Pin	Function	Pin	Function
1	LSA	34	PGC2/OA2IN+/AN17/**RP36**/RB4
2	LSB	35	**RP56**/ASDA1/SCK2/RC8
3	LSC	36	**RP57**/ASCL1/SDI2/RC9
4	V_{BOOT}	37	**RP72**/SDO2/PCI19/RD8
5	HV_{SS}	38	V_{SS}
6	V_{REG}	39	V_{DD}
7	HV_{DD}	40	PGD3/**RP37**/RB5
8	CAP2	41	PGC3/**RP38**/RB6
9	CAP1	42	AN2/**RP39**/RB7
10	N/C(1)	43	PGD1/AN10/**RP40**/SCL1/RB8
11	$\overline{MCLR}$	44	PGC1/AN11/**RP41**/SDA1/RB9
12	V_{SS}	45	**RP52**/RC4
13	ANN0/**RP77**/RD13	46	N/C
14	AN12/**RP48**/RC0	47	**RP53**/RC5

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Table 5. dsPIC33CDVXXXMC506/dsPIC33CDVXXXMC106 Complete Pin Functions (continued)

Pin	Function	Pin	Function
15	OA1OUT/AN0/CMP1A/IBIAS0/RA0	48	N/C
16	OA1IN-/AN16/RA1	49	**RP58**/RC10
17	OA1IN+/AN9/RA2	50	N/C
18	DACOUT/AN3/CMP1C/RA3	51	**RP59**/RC11
19	OA3OUT/AN4/IBIAS3/RA4	52	V_{DD}
20	AVdd	53	N/C(1)
21	AV_{SS}	54	N/C(1)
22	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/RC1	55	WAKE
23	OA3IN+/AN14/ISRC1/**RP50**/RC2	56	PHA
24	AN19/IBIAS1/**RP54**/RC6	57	HSA
25	V_{DD}	58	VBA
26	V_{SS}	59	PHB
27	AN15/CMP2A/IBIAS2/**RP51**/RC3	60	HSB
28	OSCI/CLKI/AN5/**RP32**/RB0	61	VBB
29	OSCO/CLKO/AN6/**RP33**/RB1	62	PHC
30	AN18/ISRC3/**RP74**/RD10	63	HSC
31	AN7/ISRC2/**RP55**/RC7	64	VBC
32	OA2OUT/AN1/CMP1D/CMP2D/**RP34**/INT0/RB2	65	V_{SS}(2)
33	PGD2/OA2IN-/AN8/**RP35**/RB3		

Legend: RPn represents remappable pins for the Peripheral Pin Select (PPS) function.
Notes:

1. Pin is connected to a device interconnect.
2. Pin is connected to a device exposed pad.

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Table of Contents

Operating Conditions....1
Host dsPIC DSC Features....1
High-Resolution PWM....1
High-Speed Analog-to-Digital Converter....1
Analog Features....2
Microcontroller Features....2
Debug Features....2
Peripheral Features....3
LIN Transceiver Module (Based on ATA663211 Device) (dsPIC33CDVLXXXMCX06 Only)....3
Safety Features....4
MOSFET Gate Driver Module (Based on MCP8021 Device)....4
Functional Safety Readiness – ISO 26262/ IEC 61508/IEC 60730....5
dsPIC33CDVL256MC506 Product Families....5
Pin Diagrams....6
64-Pin 9x9mm VGQFN (8QW)....6
64-Pin 9x9mm VGQFN (8QW)....8
64-Pin 8x8mm VQFN (8PW)....10
64-Pin 8x8mm VQFN (8PW)....12
1. Device Overview....20
2. Guidelines for Getting Started with 16-Bit Digital Signal Controllers....27
2.1. Basic Connection Requirements....27
2.2. Decoupling Capacitors....27
2.3. Master Clear (MCLR) Pin....28
2.4. ICSP Pins....29
2.5. External Oscillator Pins....29
2.6. External Oscillator Layout Guidance....30
2.7. Oscillator Value Conditions on Device Start-up....30
2.8. Unused I/Os....31
2.9. Bulk Capacitors....31
3. CPU....32
3.1. Registers....32
3.2. Instruction Set....32
3.3. Data Space Addressing....32
3.4. Addressing Modes....33
3.5. CPU Control/Status Registers....38
3.6. Arithmetic Logic Unit (ALU)....73

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3.7. DSP Engine....74

4. Memory Organization....76
4.1. Program Address Space....76
4.2. Data Address Space....78
4.3. BIST Overview....82
4.4. Memory Resources....84
4.5. Bit-Reversed Addressing....97
4.6. Interfacing Program and Data Memory Spaces....99

5. Flash Program Memory....102
5.1. Table Instructions and Flash Programming....102
5.2. RTSP Operation....103
5.3. Error Correcting Code (ECC)....105
5.4. ECC Fault Injection....106
5.5. Flash OTP by ICSP™ Write Inhibit....106
5.6. Program Flash Memory Control Registers....108
5.7. ECC Control Registers....117

6. Resets....124
6.1. Reset Resources....125
6.2. Reset Control Register....126
6.3. Key Resources....127

7. Interrupt Controller....128
7.1. Interrupt Vector Table....128
7.2. Alternate Interrupt Vector Table....129
7.3. Reset Sequence....131
7.4. Interrupt Resources....137
7.5. Interrupt Control and Status Registers....137
7.6. INTCON1 through INTCON4....137
7.7. Status/Control Registers....139
7.8. Key Resources....239

8. I/O Ports....240
8.1. Parallel I/O (PIO) Ports....240
8.2. Configuring Analog and Digital Port Pins....241
8.3. Input Change Notification (ICN)....292
8.4. Peripheral Pin Select (PPS)....293
8.5. Considerations for Peripheral Pin Selection....294
8.6. Input Mapping....294
8.7. Virtual Connections....298
8.8. Output Mapping....299
8.9. Mapping Limitations....299
8.10. I/O Helpful Tips....302
8.11. I/O Ports Resources....304

9. Oscillator with High-Frequency PLL....366
9.1. Primary PLL....368
9.2. CPU Clocking....369

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9.3. Primary Oscillator (POSC)....370
9.4. Internal Fast RC (FRC) Oscillator....371
9.5. Low-Power RC (LPRC) Oscillator....371
9.6. Internal Backup Fast RC (BFRC) Oscillator....371
9.7. Reference Clock Output....371
9.8. Oscillator Configuration....372
9.9. OSCCON Unlock Sequence....373
9.10. Oscillator Control Registers....374

10. Direct Memory Access (DMA) Controller....387
10.1. Summary of DMA Operations....388
10.2. Typical Setup....391

11. Controller Area Network Flexible Data-Rate (CAN FD) Modules....405
11.1. Features....405
11.2. CAN Control/Status Registers....408

12. High-Speed PWM....479
12.1. Features....479
12.2. Architecture Overview....479
12.3. Lock and Write Restrictions....480
12.4. PWM4H/L Output on Peripheral Pin Select....480
12.5. PWM Control/Status Registers....481
12.6. Control Registers....482

13. MOSFET Gate Driver Module....542
13.1. Communications Port (DE2 Interconnect)....544
13.2. Low-Side PWM Inputs (PWMAL, PWMBL, PWMCL)....544
13.3. High-Side PWM Inputs (PWMAH, PWMBH, PWMCH)....545
13.4. Output Enable (OE) Input....545
13.5. Fault Output ($\overline{\text{FAULT}}$)....545
13.6. Wake Input (WAKE)....545
13.7. Motor Phase Inputs (PHA, PHB, PHC)....545
13.8. High-Side N-MOSFET Gate Driver Outputs (HSA, HSB, HSC)....545
13.9. Bootstrap Inputs (VBA, VBB, VBC)....546
13.10. Low-Side N-MOSFET Gate Driver Outputs (LSA, LSB, LSC)....546
13.11. Bootstrap Supply (V_{BOOT})....546
13.12. +3.3V (VREG)....546
13.13. Power Supply Input (HV_{DD})....546
13.14. Charge Pump Flying Capacitor (CAP1, CAP2)....547
13.15. State Diagram....547
13.16. Bias Generator....548
13.17. Supervisor....550
13.18. Output Enable (OE)....551
13.19. Faults....552
13.20. Motor Control Unit....554
13.21. Motor Control....556
13.22. DE2 Communication Port....558
13.23. MOSFET Gate Driver Registers....565
13.24. Application Information....570

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13.25. Device Protection ... 572

14. High-Speed, 12-Bit Analog-to-Digital Converter ... 577
14.1. ADC Features Overview ... 577
14.2. Analog-to-Digital Converter Resources ... 579
14.3. ADC Control Registers ... 581

15. High-Speed Analog Comparator with Slope Compensation DAC ... 643
15.1. Overview ... 643
15.2. Features Overview ... 644
15.3. DAC Control Registers ... 645
15.4. DAC Control Registers ... 646

16. Quadrature Encoder Interface (QEI) ... 660
16.1. QEI Control/Status Registers ... 663

17. Universal Asynchronous Receiver Transmitter (UART) ... 692
17.1. Architectural Overview ... 692
17.2. Character Frame ... 693
17.3. Data Buffers ... 693
17.4. Protocol Extensions ... 693
17.5. UART Control/Status Registers ... 694

18. LIN Transceiver Module ... 720
18.1. Pin Description ... 721
18.2. Functional Description ... 723
18.3. Wake-up Scenarios from Sleep Mode ... 725
18.4. Behavior Under Low Supply Voltage Condition ... 727
18.5. Application Circuit ... 728

19. Serial Peripheral Interface (SPI) ... 729
19.1. SPI Control/Status Registers ... 736

20. Inter-Integrated Circuit (I^2C) ... 754
20.1. Communicating as a Host in a Single Host Environment ... 754
20.2. Setting Baud Rate When Operating as a Bus Main ... 755
20.3. Secondary Address Masking ... 756
20.4. SMBus Support ... 757
20.5. I2C Control/Status Registers ... 758

21. Single-Edge Nibble Transmission (SENT) ... 771
21.1. Transmit Mode ... 772
21.2. Receive Mode ... 773
21.3. SENT Control/Status Registers ... 775

22. Timer1 ... 785
22.1. Timer1 Control Registers ... 786

23. Capture/Compare/PWM/Timer Modules (SCCP) ... 791
23.1. Time Base Generator ... 792
23.2. General Purpose Timer ... 793

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23.3. Output Compare Mode....794
23.4. Input Capture Mode....795
23.5. Auxiliary Output....796
23.6. SCCP Control/Status Registers....798

24. Configurable Logic Cell (CLC)....820
24.1. Control Registers....822
24.2. CLC Control Registers....824

25. Peripheral Trigger Generator (PTG)....834
25.1. Features....834
25.2. PTG Registers....837
25.3. PTG Step Commands....869

26. 32-Bit Programmable Cyclic Redundancy Check (CRC) Generator....873
26.1. CRC Control Registers....874

27. Current Bias Generator (CBG)....884
27.1. Current Bias Generator Control Registers....886

28. Operational Amplifier....892
28.1. Operational Amplifier Control Registers....893

29. Deadman Timer (DMT)....896
29.1. Deadman Timer Control/Status Registers....897

30. Power-Saving Features....909
30.1. Clock Frequency and Clock Switching....909
30.2. Instruction-Based Power-Saving Modes....909
30.3. Interrupts Coincident with Power Save Instructions....911
30.4. Doze Mode....911
30.5. Peripheral Module Disable....911
30.6. Power-Saving Control Registers....912
30.7. Power-Saving Resources....922

31. Special Features....923
31.1. Configuration Bits....923
31.2. Configuration Registers....925
31.3. Device Calibration and Identification....946
31.4. User OTP Memory....948
31.5. On-Chip Voltage Regulator....948
31.6. Brown-out Reset (BOR)....950
31.7. Dual Watchdog Timer (WDT)....951
31.8. JTAG Interface....955
31.9. In-Circuit Serial Programming™ (ICSP™)....955
31.10. In-Circuit Debugger....955
31.11. Code Protection and CodeGuard™ Security....956

32. Instruction Set Summary....957

33. Development Support....971

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34. Electrical Characteristics 972
34.1. DC Characteristics 973
34.2. AC Characteristics and Timing Parameters 982
35. High-Temperature Electrical Characteristics 998
35.1. DC Characteristics 998
36. MOSFET Gate Driver Electrical Characteristics 1005
37. LIN Transceiver Electrical Characteristics 1013
38. Packaging Information 1020
38.1. Package Marking Information 1020
38.2. Package Details 1021
39. Revision History 1027
40. Product Identification System 1028
Microchip Information 1029
Trademarks 1029
Legal Notice 1029
Microchip Devices Code Protection Feature 1029

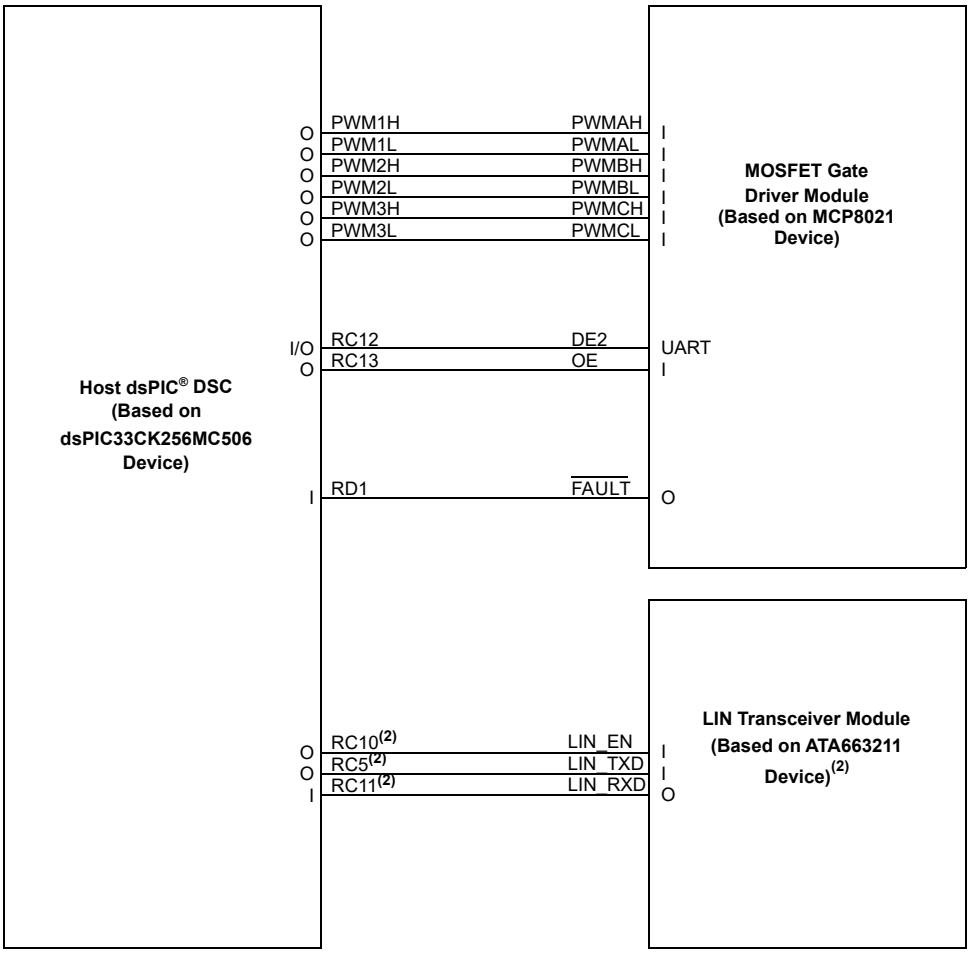
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1. Device Overview

This document contains device-specific information for the dsPIC33CDVL256MC506 Digital Signal Controller (DSC) devices.

dsPIC33CDVL256MC506 devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1. dsPIC33CDVL256MC506



Note:

1. Device Interconnections are shown in Table 1-1.

   Only applies to devices with the LIN transceiver module. Please see dsPIC33CDVL256MC506 Product Families for more information

Table 1-1. dsPIC33CDVL256MC506 Family Interconnections

Host Connection	Module Connection	Pin
dsPIC® DSC Connection	**MOSFET Gate Driver Connection**	**External Pin**
RB14/PWM1H	PWMAH	10
RB15/PWM1L	PWMAL	No
RB12/PWM2H	PWMBH	54
RB13/PWM2L	PWMBL	No
RB10/PWM3H	PWMCH	53

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Table 1-1. dsPIC33CDVL256MC506 Family Interconnections (continued)

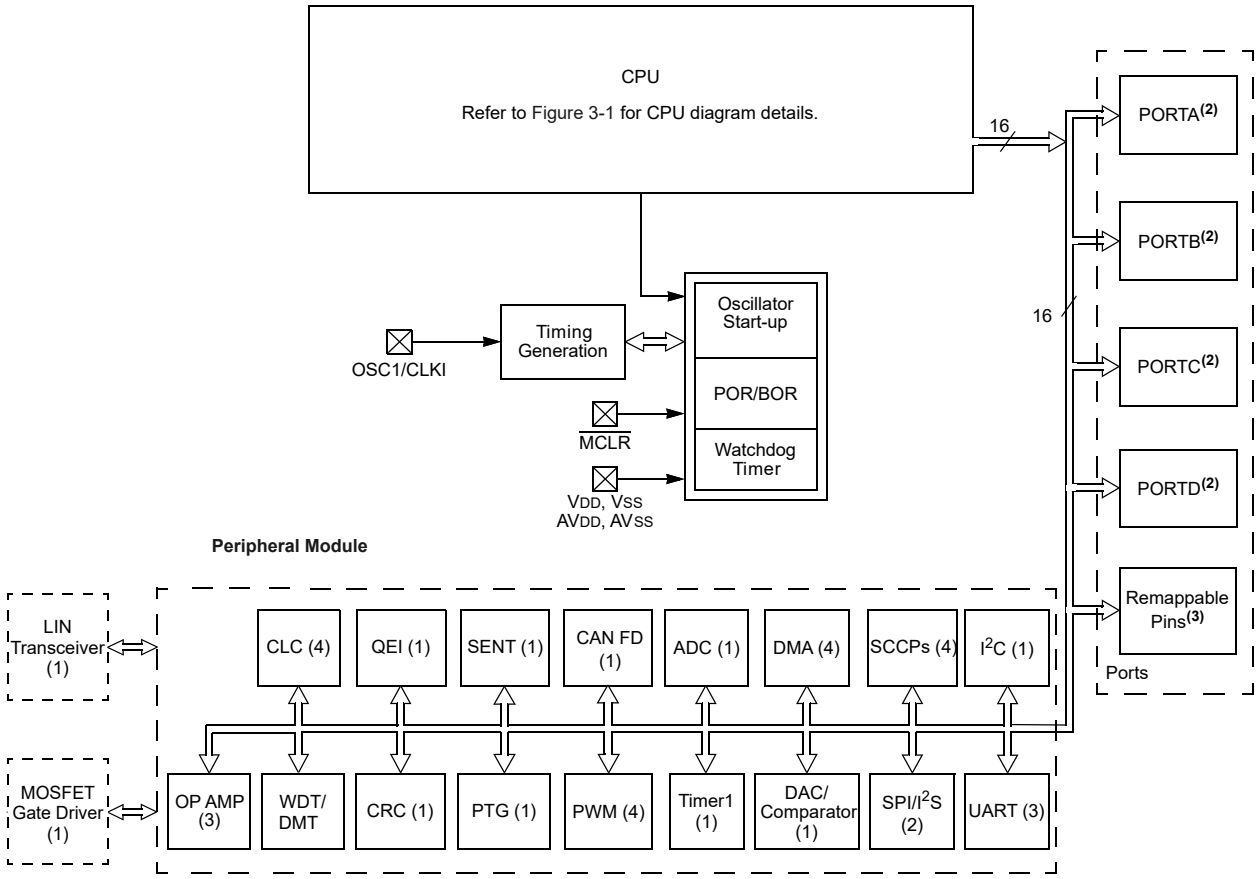
Host Connection	Module Connection	Pin
RB11/PWM3L	PWMCL	No
RD1	FAULT	No
RC12/RP60	DE2	No
RC13	OE	No
dsPIC DSC Connection	**LIN Transceiver Connection(2)**	**External Pin**
RC10	LIN_EN	No
RC5/RP53	LIN_TXD	No
RC11/RP59	LIN_RXD	No

Notes:

1. Interconnect is also bonded to an external device pin.
2. Only applies to devices with LIN Transceiver module.

Figure 1-2 shows a general block diagram of the core and peripheral modules of the dsPIC33CDVL256MC506 family.

Figure 1-2. dsPIC33CDVL256MC506 Family Block Diagram(1)



Notes:

1. The numbers in the parentheses are the number of instantiations of the module indicated.
2. Not all I/O pins or features are implemented on all device pinout configurations. See Table 1-2 for specific implementations by pin count.
3. Some peripheral I/Os are only accessible through Peripheral Pin Select (PPS).

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Table 1-2. Pinout I/O Descriptions

Pin Name(1)	Pin Type	Buffer Type	PPS	Description
AN0-AN19	I	Analog	No	Analog input channels
ANN0	I	Analog	No	Analog negative input
ADCTRG	I	ST	Yes	ADC Trigger Input 31
CAN1RX	I	ST	Yes	CAN1 receive input
CAN1TX	O	—	Yes	CAN1 transmit output
CLKI	I	ST/CMOS	No	External Clock (EC) source input. Always associated with OSCI pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to the crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSCO pin function.
OSCI	I	ST/CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSCO	I/O	—	No	Oscillator crystal output. Connects to the crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKI	I	ST	Yes	Reference clock input
REFCLKO	O	—	Yes	Reference clock output
INT0	I	ST	No	External Interrupt 0
INT1	I	ST	Yes	External Interrupt 1
INT2	I	ST	Yes	External Interrupt 2
INT3	I	ST	Yes	External Interrupt 3
IOCA[4:0]	I	ST	No	Interrupt-on-Change input for PORTA
IOCB[15:0]	I	ST	No	Interrupt-on-Change input for PORTB
IOCC[15:0]	I	ST	No	Interrupt-on-Change input for PORTC
IOCD[15:0]	I	ST	No	Interrupt-on-Change input for PORTD

Legend:

- CMOS = CMOS compatible input or output
- Analog = Analog input
- P = Power
- ST = Schmitt Trigger input with CMOS levels
- O = Output
- I = Input
- PPS = Peripheral Pin Select
- TTL = TTL input buffer

Notes:

1. Not all pins are available in all package variants. See the Pin Diagrams section for pin availability.
2. PWM4L and PWM4H pins are available on PPS.

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Table 1-2. Pinout I/O Descriptions (continued)

Pin Name(1)	Pin Type	Buffer Type	PPS	Description
QEIA1	I	ST	Yes	QEI Input A
QEIB1	I	ST	Yes	QEI Input B
QEINDX1	I	ST	Yes	QEI Index 1 input
QEIHOM1	I	ST	Yes	QEI Home 1 input
QEICMP	O	—	Yes	QEI comparator output
RA0-RA4	I/O	ST	No	PORTA is a bidirectional I/O port
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port
RC0-RC15	I/O	ST	No	PORTC is a bidirectional I/O port
RD0-RD15	I/O	ST	No	PORTD is a bidirectional I/O port
T1CK	I	ST	Yes	Timer1 external clock input
$\overline{U1CTS}$	I	ST	Yes	UART1 Clear-to-Send
$\overline{U1RTS}$	O	—	Yes	UART1 Request-to-Send
U1RX	I	ST	Yes	UART1 receive
U1TX	O	—	Yes	UART1 transmit
$\overline{U1DSR}$	I	ST	Yes	UART1 Data-Set-Ready
U1DTR	O	—	Yes	UART1 Data-Terminal-Ready
$\overline{U2CTS}$	I	ST	Yes	UART2 Clear-to-Send
$\overline{U2RTS}$	O	—	Yes	UART2 Request-to-Send
U2RX	I	ST	Yes	UART2 receive
U2TX	O	—	Yes	UART2 transmit
$\overline{U2DSR}$	I	ST	Yes	UART2 Data-Set-Ready
U2DTR	O	—	Yes	UART2 Data-Terminal-Ready
$\overline{U3CTS}$	I	ST	Yes	UART3 Clear-to-Send
$\overline{U3RTS}$	O	—	Yes	UART3 Request-to-Send
U3RX	I	ST	Yes	UART3 receive
U3TX	O	—	Yes	UART3 transmit
$\overline{U3DSR}$	I	ST	Yes	UART3 Data-Set-Ready
U3DTR	O	—	Yes	UART3 Data-Terminal-Ready

Legend:

- CMOS = CMOS compatible input or output
- Analog = Analog input
- P = Power
- ST = Schmitt Trigger input with CMOS levels
- O = Output
- I = Input
- PPS = Peripheral Pin Select
- TTL = TTL input buffer

Notes:

1. Not all pins are available in all package variants. See the Pin Diagrams section for pin availability.
2. PWM4L and PWM4H pins are available on PPS.

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Table 1-2. Pinout I/O Descriptions (continued)

Pin Name[1]	Pin Type	Buffer Type	PPS	Description
SENT1	I	ST	Yes	SENT1 input
SENT1OUT	O	—	Yes	SENT1 output
PTGTRG24	O	—	Yes	PTG Trigger Output 24
PTGTRG25	O	—	Yes	PTG Trigger Output 25
TCKI1-TCKI4	I	ST	Yes	SCCP Timer Inputs 1 through 4
ICM1-ICM4	I	ST	Yes	SCCP Capture Inputs 1 through 4
OCFA-OCFB	I	ST	Yes	SCCP Fault Inputs A through B
OCM1-OCM4	O	—	Yes	SCCP Compare Outputs 1 through 4
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1
SDI1	I	ST	Yes	SPI1 data in
SDO1	O	—	Yes	SPI1 data out
$\overline{SS1}$	I/O	ST	Yes	SPI1 Slave synchronization or frame pulse I/O
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2
SDI2	I	ST	Yes	SPI2 data in
SDO2	O	—	Yes	SPI2 data out
$\overline{SS2}$	I/O	ST	Yes	SPI2 Slave synchronization or frame pulse I/O
SCL1	I/O	ST	No	Synchronous serial clock I/O for I2C1
SDA1	I/O	ST	No	Synchronous serial data I/O for I2C1
ASCL1	I/O	ST	No	Alternate synchronous serial clock I/O for I2C1
ASDA1	I/O	ST	No	Alternate synchronous serial data I/O for I2C1
TMS	I	ST	No	JTAG Test mode select pin
TCK	I	ST	No	JTAG test clock input pin
TDI	I	ST	No	JTAG test data input pin
TDO	O	—	No	JTAG test data output pin
PCI8-PCI22	I	ST	Yes	PWM Inputs 8 through 22
PWMEA-PWMED	O	—	Yes	PWM Event Outputs A through D
PWM1L-PWM4L[2]	O	—	No	PWM Low Outputs 1 through 4
PWM1H-PWM4H[2]	O	—	No	PWM High Outputs 1 through 4

Legend:

- CMOS = CMOS compatible input or output
- Analog = Analog input
- P = Power
- ST = Schmitt Trigger input with CMOS levels
- O = Output
- I = Input
- PPS = Peripheral Pin Select
- TTL = TTL input buffer

Notes:

1. Not all pins are available in all package variants. See the Pin Diagrams section for pin availability.
2. PWM4L and PWM4H pins are available on PPS.

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Table 1-2. Pinout I/O Descriptions (continued)

Pin Name[1]	Pin Type	Buffer Type	PPS	Description
CLCINA-CLCIND	I	ST	Yes	CLC Inputs A through D
CLC1OUT-CLC4OUT	O	—	Yes	CLC Outputs 1 through 4
CMP1	O	—	Yes	Comparator 1 output
CMP1A	I	Analog	No	Comparator Channel 1A input
CMP1B	I	Analog	No	Comparator Channel 1B input
CMP1C	I	Analog	No	Comparator Channel 1C input
CMP1D	I	Analog	No	Comparator Channels 1D input
CMP2	O	—	Yes	Comparator 2 output
CMP2A	I	Analog	No	Comparator Channel 2A input
CMP2B	I	Analog	No	Comparator Channel 2B input
CMP2C	I	Analog	No	Comparator Channel 2C input
CMP2D	I	Analog	No	Comparator Channels 2D input
DACOUT1	O	—	No	DAC output voltage
IBIAS0-IBIAS3	O	Analog	No	50 µA Constant-Current Outputs 0 through 3
ISRC0-ISRC3	O	Analog	No	10 µA Constant-Current Outputs 0 through 3
OA1IN+	I	—	No	Op Amp 1+ input
OA1IN-	I	—	No	Op Amp 1- input
OA1OUT	O	—	No	Op Amp 1 output
OA2IN+	I	—	No	Op Amp 2+ input
OA2IN-	I	—	No	Op Amp 2- input
OA2OUT	O	—	No	Op Amp 2 output
OA3IN+[3]	I	—	No	Op Amp 3+ input
OA3IN-[3]	I	—	No	Op Amp 3- input
OA3OUT[3]	O	—	No	Op Amp 3 output

Legend:

- CMOS = CMOS compatible input or output
- Analog = Analog input
- P = Power
- ST = Schmitt Trigger input with CMOS levels
- O = Output
- I = Input
- PPS = Peripheral Pin Select
- TTL = TTL input buffer

Notes:

1. Not all pins are available in all package variants. See the Pin Diagrams section for pin availability.
2. PWM4L and PWM4H pins are available on PPS.

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Table 1-2. Pinout I/O Descriptions (continued)

Pin Name(1)	Pin Type	Buffer Type	PPS	Description
PGD1	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 1
PGC1	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 1
PGD2	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 2
PGC2	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 2
PGD3	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 3
PGC3	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 3
$\overline{MCLR}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AV_{DD}	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AV_{SS}	P	P	No	Ground reference for analog modules. This pin must be connected at all times.
V_{DD}	P	—	No	Positive supply for peripheral logic and I/O pins. This pin must be connected at all times.
V_{SS}	P	—	No	Ground reference for logic and I/O pins. This pin must be connected at all times.

Legend:

- CMOS = CMOS compatible input or output
- Analog = Analog input
- P = Power
- ST = Schmitt Trigger input with CMOS levels
- O = Output
- I = Input
- PPS = Peripheral Pin Select
- TTL = TTL input buffer

Notes:

1. Not all pins are available in all package variants. See the Pin Diagrams section for pin availability.
2. PWM4L and PWM4H pins are available on PPS.

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2. Guidelines for Getting Started with 16-Bit Digital Signal Controllers

2.1. Basic Connection Requirements

Getting started with the family devices of the dsPIC33CDVL256MC506 requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names which must always be connected:

- All V_{DD} and V_{SS} pins
  (see Decoupling Capacitors)
- All AV_{DD} and AV_{SS} pins
  regardless if the ADC module is not used (see Electrical Characteristics)
- $\overline{MCLR}$ pin
  (see Master Clear (MCLR) Pin)
- PGCx/PGDx pins
  used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see ICSP Pins)
- OSCI and OSCO pins
  when an external oscillator source is used (see External Oscillator Pins)

2.2. Decoupling Capacitors

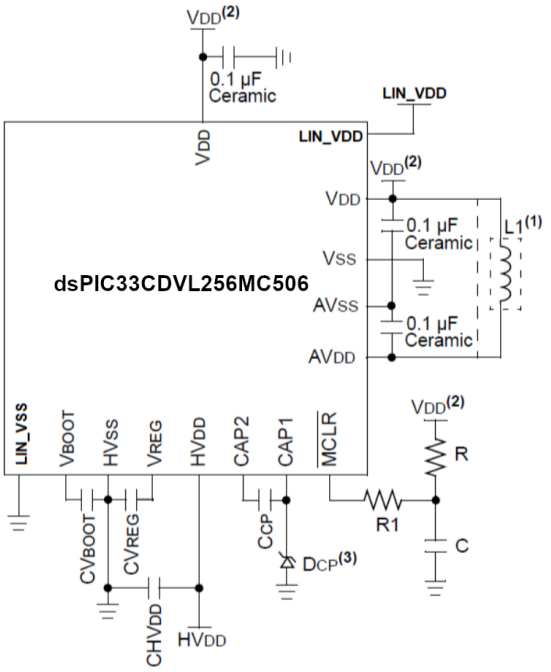
The use of decoupling capacitors on every pair of power supply pins, such as V_{DD}, V_{SS}, AV_{DD} and AV_{SS}, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the Printed Circuit Board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

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Figure 2-1. Recommended Minimum Connection



Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

2: VDD/AVDD pins may be powered by either an external power supply or by the 3.3V VREG output.

3: A Schottky diode between the CAP1 pin and HVSS is recommended to ensure that the CAP1 pin absolute minimum voltage specification of -0.3V is maintained.

Where:

$$f = \frac{FCNV}{2}$$ (i.e., ADC conversion rate/2)

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.3. Master Clear ($\overline{\text{MCLR}}$) Pin

The $\overline{\text{MCLR}}$ pin provides two specific device functions:

- Device Reset
- Device Programming and Debugging.

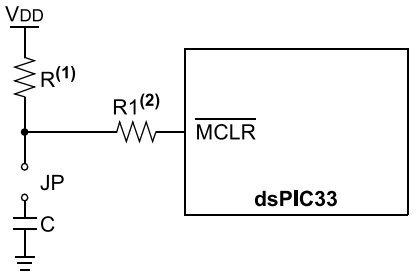
During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, the specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations.

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Place the components, as shown in Figure 2-2, within one-quarter inch (6 mm) of the $\overline{MCLR}$ pin.

Figure 2-2. Example of $\overline{MCLR}$ Pin Connections



Notes:

1. R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met.
2. R1 ≤ 470Ω will limit any current flowing into $\overline{MCLR}$ from the external capacitor, C, in the event of $\overline{MCLR}$ pin breakdown due to electrostatic discharge (ESD) or electrical overstress (EOS). Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met.

2.4. ICSP Pins

The PGCx and PGDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGCx and PGDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the Communication Channel Select (i.e., PGCx/PGDx pins) programmed into the device matches the physical connections for the ICSP to the emulator.

For more information on emulator connection requirements, as well as which Microchip development tools support programming and debugging of this device, refer to the documentation that is available on the Microchip website.

2.5. External Oscillator Pins

When the Primary Oscillator (POSC) circuit is used to connect a crystal oscillator, special care and consideration are needed to ensure proper operation. The POSC circuit should be tested across the environmental conditions that the end product is intended to be used. The load capacitors specified in the crystal oscillator data sheet can be used as a starting point, however, the parasitic capacitance from the PCB traces can affect the circuit, and the values may need to be altered to ensure proper start-up and operation. Excessive trace length and other physical interaction can lead to poor signal quality. Poorly tuned oscillator circuits can have reduced amplitude, incorrect frequency (runt pulses), distorted waveforms and long start-up times that may result in unpredictable application behavior, such as instruction misexecution, illegal opcode fetch, etc. Ensure that the crystal oscillator circuit is at full amplitude and the correct frequency before the system begins to execute code. In planning the application's routing and I/O assignments, ensure that adjacent port pins and other

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signals in close proximity to the oscillator do not have high frequencies, short rise and fall times and other similar noise. For further information on the Primary Oscillator, see Primary Oscillator (POSC).

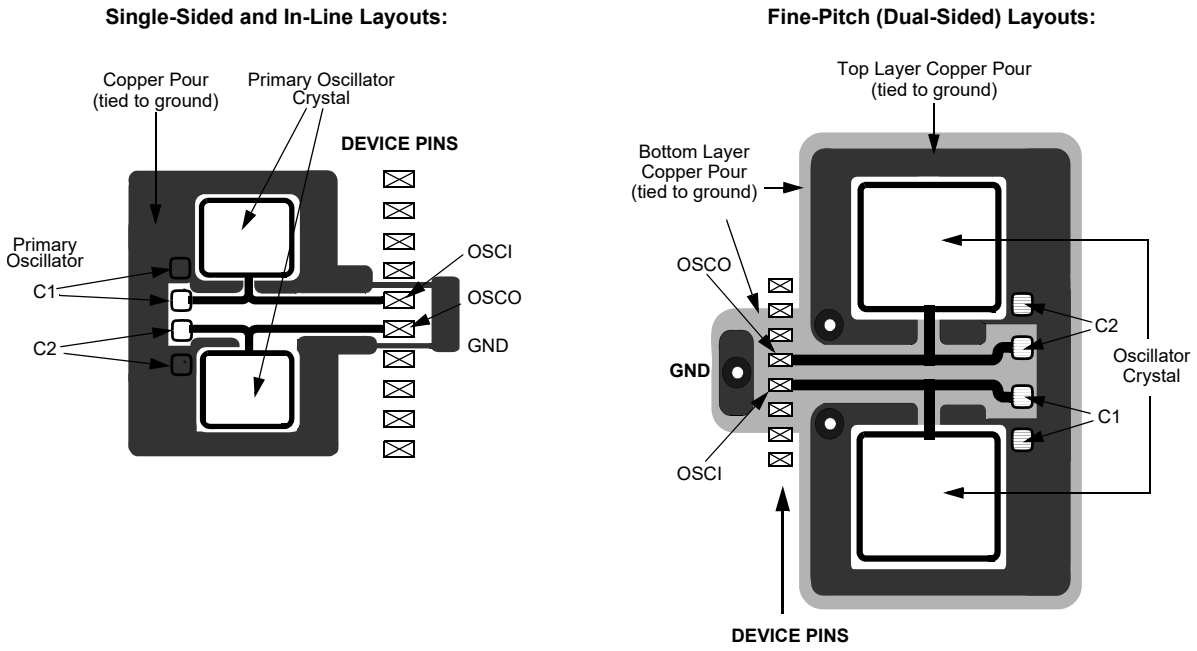
2.6. External Oscillator Layout Guidance

Use best practices during PCB layout to ensure robust start-up and operation. The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. If using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. Suggested layouts are shown in Figure 2-3. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the Microchip website (www.microchip.com):

- AN943, "Practical PICmicro® Oscillator Analysis and Design"
- AN949, "Making Your Oscillator Work"

Figure 2-3. Suggested Placement of the Oscillator Circuit



2.7. Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to a certain frequency (see Oscillator with High-Frequency PLL) to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside of this range, the application must start up in FRC mode first. The default PLL settings after a POR, with an oscillator frequency outside of this range, will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

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2.8. Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between V_{SS} and unused pins, and drive the output to logic low.

2.9. Bulk Capacitors

On boards with power traces running longer than six inches in length, it is suggested to use a bulk capacitor for integrated circuits, including DSCs, to supply a local power source. The value of the bulk capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the bulk capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

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3. CPU

This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Enhanced CPU"** (www.microchip.com/DS70005158) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The dsPIC33CDVL256MC506 family CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for Digital Signal Processing (DSP). The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

3.1. Registers

The dsPIC33CDVL256MC506 devices have sixteen 16-bit Working registers in the programmer's model. Each of the Working registers can act as a Data, Address or Address Offset register. The 16th Working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

In addition, the dsPIC33CDVL256MC506 devices include four Alternate Working register sets, which consist of W0 through W14. The Alternate Working registers can be made persistent to help reduce the saving and restoring of register content during Interrupt Service Routines (ISRs). The Alternate Working registers can be assigned to a specific Interrupt Priority Level (IPL1 through IPL6) by configuring the CTXTx[2:0] bits in the FALTREG Configuration register. The Alternate Working registers can also be accessed manually by using the `CTXTSWP` instruction. The CCTXI[2:0] and MCTXI[2:0] bits in the CTXTSTAT register can be used to identify the current and most recent manually selected Working register sets.

3.2. Instruction Set

The instruction set for dsPIC33CDVL256MC506 devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3. Data Space Addressing

The base Data Space can be addressed as up to 4K words or 8 Kbytes, and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which split the data address space into two parts. The X and Y Data Space boundary is device-specific.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 16K program word boundary. The program-to-Data-Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Refer to **"Data Memory"** (www.microchip.com/DS70000595) in the *"dsPIC33/PIC24 Family Reference Manual"* for more details on PSV and table accesses.

On dsPIC33CDVL256MC506 family devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms.

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3.4. Addressing Modes

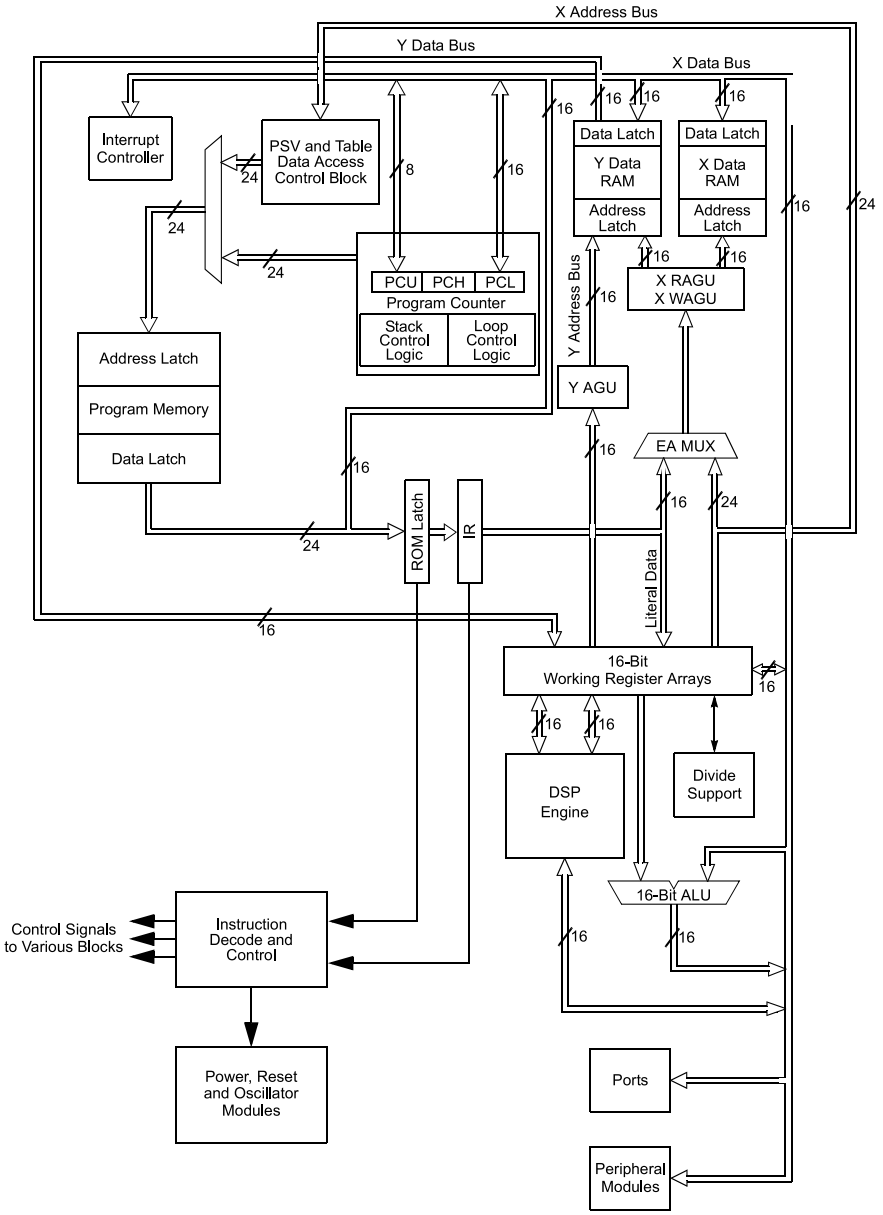
The CPU supports the following addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending on its functional requirements. Up to six addressing modes are supported for each instruction.

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Figure 3-1. dsPIC33CDVL256MC506 Family CPU Block Diagram



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3.4.1. Programmer's Model

The programmer's model for the dsPIC33CDVL256MC506 family is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 3-1 provides a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33CDVL256MC506 devices include control registers for Modulo Addressing, Bit-Reversed Addressing and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in Figure 3-2.

Table 3-1. Programmer's Model Register Descriptions

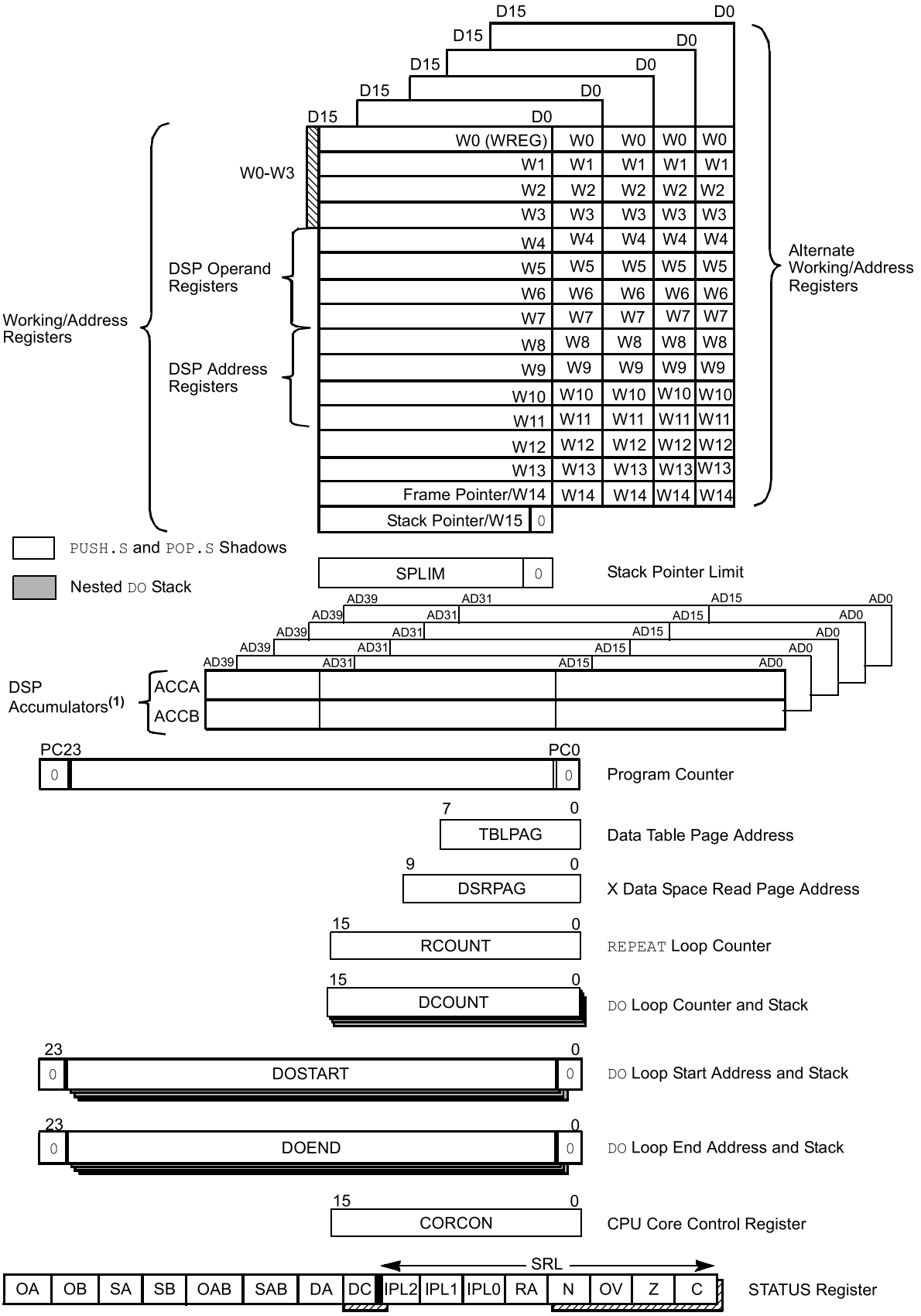
Register(s) Name	Description
W0 through W15(1)	Working Register Array
W0 through W14(1)	Alternate Working Register Array 1
W0 through W14(1)	Alternate Working Register Array 2
W0 through W14(1)	Alternate Working Register Array 3
W0 through W14(1)	Alternate Working Register Array 4
ACCA, ACCB	40-bit DSP Accumulators (Additional Four Alternate Accumulators)
PC	23-bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	16-bit Stack Pointer Limit Value Register
TBLPAG	8-bit Table Memory Page Address Register
DSRPAG	10-bit Extended Data Space (EDS) Read Page Register
RCOUNT	16-bit REPEAT Loop Counter Register
DCOUNT	16-bit DO Loop Counter Register
DOSTARTL(2)	15-bit DO Loop Start Address Register (bit 0 = 0) (Low)
DOSTARTH(2)	7-bit DO Loop Start Address Register (High)
DOENDL	15-bit DO Loop End Address Register (bit 0 = 0) (Low)
DOENDH	7-bit DO Loop End Address Register (High)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

Notes:

1. Memory-mapped W0 through W14 represent the values of the registers in the currently active CPU context.
2. The DOSTARTH and DOSTARTL registers are read-only.

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Figure 3-2. Programmer's Model



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3.4.2. CPU Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page contains the latest updates and additional information.

3.4.2.1. Key Resources

- **"Enhanced CPU"** (www.microchip.com/DS70005158) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33/PIC24 Family Reference Manual"* sections
- Development Tools

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3.5. CPU Control/Status Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	WREG0	15:8	WREG0[15:8]							
		7:0	WREG0[7:0]							
0x02	WREG1	15:8	WREG1[15:8]							
		7:0	WREG1[7:0]							
0x04	WREG2	15:8	WREG2[15:8]							
		7:0	WREG2[7:0]							
0x06	WREG3	15:8	WREG3[15:8]							
		7:0	WREG3[7:0]							
0x08	WREG4	15:8	WREG4[15:8]							
		7:0	WREG4[7:0]							
0x0A	WREG5	15:8	WREG5[15:8]							
		7:0	WREG5[7:0]							
0x0C	WREG6	15:8	WREG6[15:8]							
		7:0	WREG6[7:0]							
0x0E	WREG7	15:8	WREG7[15:8]							
		7:0	WREG7[7:0]							
0x10	WREG8	15:8	WREG8[15:8]							
		7:0	WREG8[7:0]							
0x12	WREG9	15:8	WREG9[15:8]							
		7:0	WREG9[7:0]							
0x14	WREG10	15:8	WREG10[15:8]							
		7:0	WREG10[7:0]							
0x16	WREG11	15:8	WREG11[15:8]							
		7:0	WREG11[7:0]							
0x18	WREG12	15:8	WREG12[15:8]							
		7:0	WREG12[7:0]							
0x1A	WREG13	15:8	WREG13[15:8]							
		7:0	WREG13[7:0]							
0x1C	WREG14	15:8	WREG14[15:8]							
		7:0	WREG14[7:0]							
0x1E	WREG15	15:8	WREG15[15:8]							
		7:0	WREG15[7:0]							
0x20	SPLIM	15:8	SPLIM[15:8]							
		7:0	SPLIM[7:0]							
0x22	ACCAL	15:8	ACCAL[15:8]							
		7:0	ACCAL[7:0]							
0x24	ACCAH	15:8	ACCAH[15:8]							
		7:0	ACCAH[7:0]							
0x26	ACCAU	15:8	ACCA39[7:0]							
		7:0	ACCAU[7:0]							
0x28	ACCBL	15:8	ACCBL[15:8]							
		7:0	ACCBL[7:0]							
0x2A	ACCBH	15:8	ACCBH[15:8]							
		7:0	ACCBH[7:0]							
0x2C	ACCBU	15:8	ACCB39[7:0]							
		7:0	ACCBU[7:0]							
0x2E	PCL	15:8	PCL[15:8]							
		7:0	PCL[7:0]							
0x30	PCH	15:8								
		7:0	PCH[7:0]							
0x32	DSRPAG	15:8							DSRPAG[9:8]	
		7:0	DSRPAG[7:0]							
0x34	DSWPAG	15:8								DSWPAG[8]
		7:0	DSWPAG[7:0]							
0x36	RCOUNT	15:8	RCOUNT[15:8]							
		7:0	RCOUNT[7:0]							
0x38	DCOUNT	15:8	DCOUNT[15:8]							
		7:0	DCOUNT[7:0]							

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CPU Control/Status Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x3A	DOSTARTL	15:8	DOSTARTL[15:8]							
		7:0	DOSTARTL[7:0]							
0x3C	DOSTARTH	15:8								
		7:0		DOSTARTH[6:0]						
0x3E	DOENDL	15:8	DOENDL[15:8]							
		7:0	DOENDL[7:0]							
0x40	DOENDH	15:8								
		7:0		DOENDH[6:0]						
0x42	SR	15:8	OA	OB	SA	SB	OAB	SAB	DA	DC
		7:0	IPL[2:0]			RA	N	OV	Z	C
0x44	CORCON	15:8	VAR		US[1:0]		EDT	DL[2:0]		
		7:0	SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF
0x46	MODCON	15:8	XMODEN	YMODEN			BWM[3:0]			
		7:0	YWM[3:0]				XWM[3:0]			
0x48	XMODSRT	15:8	XS[15:8]							
		7:0	XS[7:0]							
0x4A	XMODEND	15:8	XE[15:8]							
		7:0	XE[7:0]							
0x4C	YMODSRT	15:8	YS[15:8]							
		7:0	YS[7:0]							
0x4E	YMODEND	15:8	YE[15:8]							
		7:0	YE[7:0]							
0x50	XBREV	15:8	BREN	XB[14:8]						
		7:0	XB[7:0]							
0x52	DISICNT	15:8			DISICNT[13:8]					
		7:0	DISICNT[7:0]							
0x54	TBLPAG	15:8								
		7:0	TBLPAG[7:0]							
0x56	YPAG	15:8								
		7:0	YPAG[7:0]							
0x58	MSTRPR	15:8								
		7:0			DMAPR	CANPR				NVMPR
0x5A	CTXTSTAT	15:8						CCTXI[2:0]		
		7:0						MCTXI[2:0]		

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3.5.1. Working Register x

Name: WREGx
Offset: 0x00, 0x02, 0x04, 0x06, 0x08, 0x0A, 0x0C, 0x0E, 0x10, 0x12, 0x14, 0x16, 0x18, 0x1A, 0x1C, 0x1E

Bit	15	14	13	12	11	10	9	8
	WREGx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREGx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREGx[15:0] Data bits

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3.5.2. Stack Pointer Limit Value Register

Name: SPLIM
Offset: 0x20

Bit	15	14	13	12	11	10	9	8
	SPLIM[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SPLIM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SPLIM[15:0] Stack Limit Address bits

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3.5.3. Accumulator A Low Register

Name: ACCAL
Offset: 0x22

Bit	15	14	13	12	11	10	9	8
	ACCAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ACCAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ACCAL[15:0] Accumulator A Low Register bits

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3.5.4. Accumulator A High Register

Name: ACCAH
Offset: 0x24

Bit	15	14	13	12	11	10	9	8
	ACCAH[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ACCAH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ACCAH[15:0] Accumulator A High Register bits

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3.5.5. Accumulator A Upper Register

Name: ACCAU
Offset: 0x26

Bit	15	14	13	12	11	10	9	8
	ACCA39[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ACCAU[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – ACCA39[7:0] Accumulator A bits

Bits 7:0 – ACCAU[7:0] Accumulator A bits

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3.5.6. Accumulator B Low Register

Name: ACCBL
Offset: 0x28
Property: R/W

Bit	15	14	13	12	11	10	9	8
	ACCBL[15:8]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ACCBL[7:0]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ACCBL[15:0] Accumulator B Low Register bits

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3.5.7. Accumulator B High Register

Name: ACCBH
Offset: 0x2A
Property: R/W

Bit	15	14	13	12	11	10	9	8
	ACCBH[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ACCBH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ACCBH[15:0] Accumulator B High Register bits

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3.5.8. Accumulator B Upper Address Register

Name: ACCBU
Offset: 0x2C

Bit	15	14	13	12	11	10	9	8
	ACCB39[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ACCBU[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – ACCB39[7:0] Accumulator B bits

Bits 7:0 – ACCBU[7:0] Accumulator B bits

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3.5.9. Program Counter Low Register

Name: PCL
Offset: 0x2E

Bit	15	14	13	12	11	10	9	8
	PCL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PCL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PCL[15:0] Program Counter Low Value bits

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3.5.10. Program Counter High Register

Name: PCH
Offset: 0x30

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PCH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PCH[7:0] Program Counter High Value bits

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3.5.11. Data Space Read Page Register

Name: DSRPAG
Offset: 0x32

Bit	15	14	13	12	11	10	9	8
							DSRPAG[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	DSRPAG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – DSRPAG[9:0] Data Space Read Page Value bits

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3.5.12. Data Space Write Page Register

Name: DSWPAG
Offset: 0x34

Bit	15	14	13	12	11	10	9	8
								DSWPAG[8]
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
	DSWPAG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 8:0 – DSWPAG[8:0] Data Space Write Page Value bits

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3.5.13. `REPEAT` Loop Counter Register

Name: RCOUNT
Offset: 0x36

Bit	15	14	13	12	11	10	9	8
	RCOUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RCOUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RCOUNT[15:0] Current Loop Counter Value for `REPEAT` Instruction bits

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3.5.14. DO Loop Iteration Count Register

Name: DCOUNT
Offset: 0x38

Bit	15	14	13	12	11	10	9	8
	DCOUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DCOUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DCOUNT[15:0] DO Loop Iteration Count Register bits

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3.5.15. DO Loop Start Address Register Low

Name: DOSTARTL
Offset: 0x3A

Bit	15	14	13	12	11	10	9	8
	DOSTARTL[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DOSTARTL[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DOSTARTL[15:0] Current DO Loop Start Address bits
Note: DOSTARTL[0] always reads as '0'; DOSTARTL is a read-only register.

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3.5.16. DO Loop Start Address Register High

Name: DOSTARTH
Offset: 0x3C

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		DOSTARTH[6:0]						
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bits 6:0 – DOSTARTH[6:0] Current DO Loop Start Address bits
Note: DOSTARTH[0] always reads as '0'; DOSTARTH is a read-only register.

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3.5.17. DO Loop End Address Register Low

Name: DOENDL
Offset: 0x3E

Bit	15	14	13	12	11	10	9	8
	DOENDL[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DOENDL[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DOENDL[15:0] Current DO Loop End Address bits
Note: DOENDL[0] always reads as '0'.

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3.5.18. DO Loop End Address Register High

Name: DOENDH
Offset: 0x40

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		DOENDH[6:0]						
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bits 6:0 – DOENDH[6:0] Current DO Loop End Address bits
Note: DOENDH[0] always reads as '0'.

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3.5.19. CPU STATUS Register

Name: SR
Offset: 0x42

Notes:

1. The IPL[2:0] bits are concatenated with the IPL[3] bit (CORCON[3]) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL[3] = 1. User interrupts are disabled when IPL[3] = 1.
2. The IPL[2:0] Status bits are read-only when the NSTDIS bit (INTCON1[15]) = 1.
3. A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

Legend: C = Clearable bit

Bit	15	14	13	12	11	10	9	8
	OA	OB	SA	SB	OAB	SAB	DA	DC
Access	R/W	R/W	R/W	R/W	R/C	R/C	R	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IPL[2:0]			RA	N	OV	Z	C
Access	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OA Accumulator A Overflow Status bit

Value	Description
1	Accumulator A has overflowed
0	Accumulator A has not overflowed

Bit 14 – OB Accumulator B Overflow Status bit

Value	Description
1	Accumulator B has overflowed.
0	Accumulator B has not overflowed.

Bit 13 – SA Accumulator A Saturation 'Sticky' Status bit(3)

Value	Description
1	Accumulator A is saturated or has been saturated at some time.
0	Accumulator A is not saturated.

Bit 12 – SB Accumulator B Saturation 'Sticky' Status bit(3)

Value	Description
1	Accumulator B is saturated or has been saturated at some time.
0	Accumulator B is not saturated.

Bit 11 – OAB OA || OB Combined Accumulator Overflow Status bit

Value	Description
1	Accumulator A or B has overflowed.
0	Neither Accumulator A or B has overflowed.

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Bit 10 – SAB SA || SB Combined Accumulator 'Sticky' Status bit

Value	Description
1	Accumulator A or B is saturated or has been saturated at some time.
0	Neither Accumulator A or B is saturated.

Bit 9 – DA DO Loop Active bit

Value	Description
1	DO loop is in progress.
0	DO loop is not in progress.

Bit 8 – DC MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit

Value	Description
1	A carry-out from the fourth low-order bit (for byte-sized data) or eighth low-order bit (for word-sized data) of the result occurred.
0	No carry-out from the fourth low-order bit (for byte-sized data) or eighth low-order bit (for word-sized data) of the result occurred.

Bits 7:5 – IPL[2:0] CPU Interrupt Priority Level Status bits(1,2)

Value	Description
111	CPU Interrupt Priority Level is 7 (15); user interrupts are disabled.
110	CPU Interrupt Priority Level is 6 (14).
101	CPU Interrupt Priority Level is 5 (13).
100	CPU Interrupt Priority Level is 4 (12).
011	CPU Interrupt Priority Level is 3 (11).
010	CPU Interrupt Priority Level is 2 (10).
001	CPU Interrupt Priority Level is 1 (9).
000	CPU Interrupt Priority Level is 0 (8).

Bit 4 – RA REPEAT Loop Active bit

Value	Description
1	REPEAT loop is in progress.
0	REPEAT loop is not in progress.

Bit 3 – N MCU ALU Negative bit

Value	Description
1	Result was negative.
0	Result was non-negative (zero or positive).

Bit 2 – OV MCU ALU Overflow bit

This bit is used for signed arithmetic (two's complement). It indicates an overflow of the magnitude that causes the sign bit to change state.

Value	Description
1	Overflow occurred for signed arithmetic (in this arithmetic operation).
0	No overflow occurred.

Bit 1 – Z MCU ALU Zero bit

Value	Description
1	An operation that affects the Z bit has set it at some time in the past.
0	The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result).

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Bit 0 – C MCU ALU Carry/$\overline{\text{Borrow}}$ bit

Value	Description
1	A carry-out from the Most Significant bit of the result occurred.
0	No carry-out from the Most Significant bit of the result occurred.

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3.5.20. Core Control Register

Name: CORCON
Offset: 0x44

Notes:

1. This bit is always read as '0'.
2. The IPL3 bit is concatenated with the IPL[2:0] bits (SR[7:5]) to form the CPU Interrupt Priority Level.

Legend: C = Clearable bit

Bit	15	14	13	12	11	10	9	8
	VAR		US[1:0]		EDT	DL[2:0]		
Access	R/W		R/W	R/W	R/W	R	R	R
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF
Access	R/W	R/W	R/W	R/W	R/C	R	R/W	R/W
Reset	0	0	1	0	0	0	0	0

Bit 15 – VAR Variable Exception Processing Latency Control bit

Value	Description
1	Variable exception processing is enabled.
0	Fixed exception processing is enabled.

Bits 13:12 – US[1:0] DSP Multiply Unsigned/Signed Control bits

Value	Description
11	Reserved
10	DSP engine multiplies are mixed sign.
01	DSP engine multiplies are unsigned.
00	DSP engine multiplies are signed.

Bit 11 – EDT Early DO Loop Termination Control bit(1)

Value	Description
1	Terminates executing DO loop at the end of the current loop iteration.
0	No effect

Bits 10:8 – DL[2:0] DO Loop Nesting Level Status bits

Value	Description
111	Seven DO loops are active.
. . .	
001	One DO loop is active.
000	Zero DO loops are active.

Bit 7 – SATA ACCA Saturation Enable bit

Value	Description
1	Accumulator A saturation is enabled.
0	Accumulator A saturation is disabled.

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Bit 6 – SATB ACCB Saturation Enable bit

Value	Description
1	Accumulator B saturation is enabled.
0	Accumulator B saturation is disabled.

Bit 5 – SATDW Data Space Write from DSP Engine Saturation Enable bit

Value	Description
1	Data Space write saturation is enabled.
0	Data Space write saturation is disabled.

Bit 4 – ACCSAT Accumulator Saturation Mode Select bit

Value	Description
1	9.31 saturation (super saturation)
0	1.31 saturation (normal saturation)

Bit 3 – IPL3 CPU Interrupt Priority Level Status 3 bit (2)

Value	Description
1	CPU Interrupt Priority Level is greater than 7.
0	CPU Interrupt Priority Level is 7 or less.

Bit 2 – SFA Stack Frame Active Status bit

Value	Description
1	Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG.
0	Stack frame is not active; W14 and W15 address the base Data Space.

Bit 1 – RND Rounding Mode Select bit

Value	Description
1	Biased (conventional) rounding is enabled.
0	Unbiased (convergent) rounding is enabled.

Bit 0 – IF Integer or Fractional Multiplier Mode Select bit

Value	Description
1	Integer mode is enabled for DSP multiply.
0	Fractional mode is enabled for DSP multiply.

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3.5.21. Modulo and Bit-Reversed Addressing Control Register

Name: MODCON
Offset: 0x46

Bit	15	14	13	12	11	10	9	8
	XMODEN	YMODEN			BWM[3:0]			
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	7	6	5	4	3	2	1	0
	YWM[3:0]				XWM[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – XMODEN X RAGU and X WAGU Modulus Addressing Enable bit

Value	Description
1	X AGU Modulus Addressing enabled.
0	X AGU Modulus Addressing disabled.

Bit 14 – YMODEN Y AGU Modulus Addressing Enable bit

Value	Description
1	Y AGU Modulus Addressing enabled.
0	Y AGU Modulus Addressing disabled.

Bits 11:8 – BWM[3:0] X WAGU Register Select for Bit-Reversed Addressing bits

Value	Description
1111	W15 Bit-Reversed Addressing disabled.
1110	W14 selected for Bit-Reversed Addressing.
0000	W0 selected for Bit-Reversed Addressing.

Bits 7:4 – YWM[3:0] Y AGU W Register Select for Modulo Addressing bits

Value	Description
1111	W15 Bit-Reversed Addressing disabled.
1110	W14 selected for Bit-Reversed Addressing.
0000	W0 selected for Bit-Reversed Addressing.

Bits 3:0 – XWM[3:0] X RAGU and X WAGU W Register Select for Modulo Addressing bits

Value	Description
1111	W15 Bit-Reversed Addressing disabled.
1110	W14 selected for Bit-Reversed Addressing.
0000	W0 selected for Bit-Reversed Addressing.

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3.5.22. X AGU Modulo Addressing Start Register

Name: XMODSRT
Offset: 0x48

Bit	15	14	13	12	11	10	9	8
	XS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	XS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – XS[15:0] X RAGU and X WAGU Modulo Addressing Start Address bits

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3.5.23. X AGU Modulo Addressing End Register

Name: XMODEND
Offset: 0x4A

Bit	15	14	13	12	11	10	9	8
	XE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	XE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – XE[15:0] X RAGU and X WAGU Modulo Addressing End Address bits

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3.5.24. Y AGU Modulo Addressing Start Register

Name: YMODSRT
Offset: 0x4C

Bit	15	14	13	12	11	10	9	8
	YS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	YS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – YS[15:0] Y AGU Modulo Addressing Start Address bits

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3.5.25. Y AGU Modulo Addressing End Register

Name: YMODEND
Offset: 0x4E

Bit	15	14	13	12	11	10	9	8
	YE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	YE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – YE[15:0] X AGU Modulo Addressing End Address bits

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3.5.26. X AGU Bit-Reversed Addressing Control Register

Name: XBREV
Offset: 0x50

Bit	15	14	13	12	11	10	9	8
	BREN	XB[14:8]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	XB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bit 15 – BREN Bit-Reversed Addressing (X AGU) Enable bit

Value	Description
1	Bit-Reversed Addressing enabled.
0	Bit-Reversed Addressing disabled.

Bits 14:0 – XB[14:0] X AGU Bit-Reversed Modifier bits

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3.5.27. Disable Interrupt Count Register

Name: DISICNT
Offset: 0x52

Bit	15	14	13	12	11	10	9	8
			DISICNT[13:8]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DISICNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 13:0 – DISICNT[13:0] Current Counter Value for `DISI` Instruction bits

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3.5.28. Table Memory Page Address Register

Name: TBLPAG
Offset: 0x54

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	TBLPAG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TBLPAG[7:0] Table Memory Page Value bits

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3.5.29. Y Page Register

Name: YPAG
Offset: 0x56

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	YPAG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – YPAG[7:0] Y Page bits
Note: When implemented, YPAG is a R/W SFR register which resets to 0x0001. When not implemented, YPAG is a read-only SFR register which will always return the fixed Y RAM page value, 0x0001.

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3.5.30. EDS Bus Master Priority Control Register

Name: MSTRPR
Offset: 0x58

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			DMAPR	CANPR				NVMPR
Access			R/W	R/W				R/W
Reset			0	0				0

Bit 5 – DMAPR Modify DMA Controller Bus Main Priority Relative to CPU bit

Value	Description
1	Raises the DMA Controller bus main priority above that of the CPU.
0	No change to the DMA Controller bus main priority.

Bit 4 – CANPR Modify CAN1 Bus Main Priority Relative to CPU bit

Value	Description
1	Raises the CAN1 bus main priority above that of the CPU.
0	No change to the CAN1 bus main priority.

Bit 0 – NVMPR Modify NVM Controller Bus Main Priority Relative to CPU bit

Value	Description
1	Raises the NVM Controller bus main priority above that of the CPU.
0	No change to the NVM Controller bus main priority.

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3.5.31. CPU W Register Context Status Register

Name: CTXTSTAT
Offset: 0x5A

Bit	15	14	13	12	11	10	9	8
						CCTXI[2:0]		
Access						R	R	R
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
						MCTXI[2:0]		
Access						R	R	R
Reset						0	0	0

Bits 10:8 – CCTXI[2:0] Current (W Register) Context Identifier bits

Value	Description
111	Reserved
. . .	
100	Alternate Working Register Set 4 is currently in use.
011	Alternate Working Register Set 3 is currently in use.
010	Alternate Working Register Set 2 is currently in use.
001	Alternate Working Register Set 1 is currently in use.
000	Default register set is currently in use.

Bits 2:0 – MCTXI[2:0] Manual (W Register) Context Identifier bits

Value	Description
111	Reserved
. . .	
100	Alternate Working Register Set 4 was most recently manually selected.
011	Alternate Working Register Set 3 was most recently manually selected.
010	Alternate Working Register Set 2 was most recently manually selected.
001	Alternate Working Register Set 1 was most recently manually selected.
000	Default register set was most recently manually selected.

3.6. Arithmetic Logic Unit (ALU)

The dsPIC33CDVL256MC506 family ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the **"16-Bit MCU and DSC Programmer's Reference Manual"** (www.microchip.com/DS70000157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

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3.6.1. Multiplier

Using the high-speed, 17-bit x 17-bit multiplier, the ALU supports unsigned, signed or mixed-sign operation in several MCU Multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.6.2. Divider

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute. There are additional instructions: `DIV2` and `DIVF2`. Divide instructions will complete in six cycles.

3.7. DSP Engine

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are `ADD`, `SUB`, `NEG`, `MIN`, and `MAX`.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- Signed, unsigned or mixed-sign DSP multiply (USx)
- Conventional or convergent rounding (RND)
- Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

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Table 3-2. DSP Instructions Summary

Instruction	Algebraic Operation	ACC Write-Back
CLR	$A = 0$	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	$A = A + (x \cdot y)$	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	$A = x \cdot y$	No
MPY	$A = x^2$	No
MPY.N	$A = -x \cdot y$	No
MSC	$A = A - x \cdot y$	Yes

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4. Memory Organization

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"dsPIC33/PIC24 Program Memory"** (www.microchip.com/DS70000613) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The dsPIC33CDVL256MC506 family architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

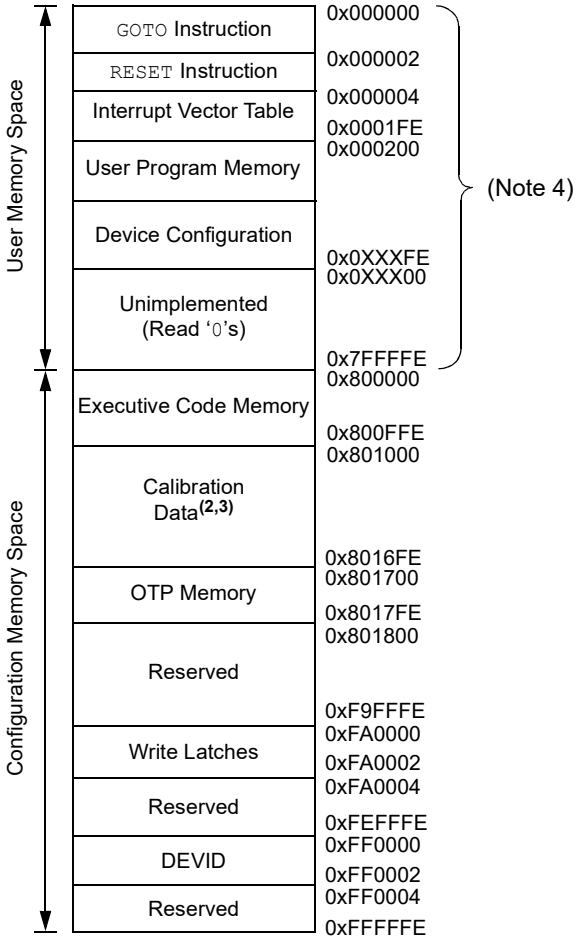
4.1. Program Address Space

The program address memory space of the dsPIC33CDVL256MC506 family devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in Interfacing Program and Data Memory Spaces.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of `TBLRD` operations, which use TBLPAG[7] to permit access to calibration data and Device ID sections of the configuration memory space.

The program memory maps for the dsPIC33CDVL256MC506 family are shown in Figure 4-1 through Figure 4-3.

Figure 4-1. Program Memory Map for dsPIC33CDVLXXXMC506/106 and dsPIC33CDVXXXMC506/106 Devices(1)



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Notes:

1. Memory areas are not shown to scale.
2. Calibration data area must be maintained during programming.
3. Calibration data area includes UDID, ICSP™ Write Inhibit and FBOOT registers' locations.
4. See Figure 4-2 and Figure 4-3 for details.

Figure 4-2. Program Memory Map for dsPIC33CDVL256MC506/106 and dsPIC33CDV256MC506/106 Devices

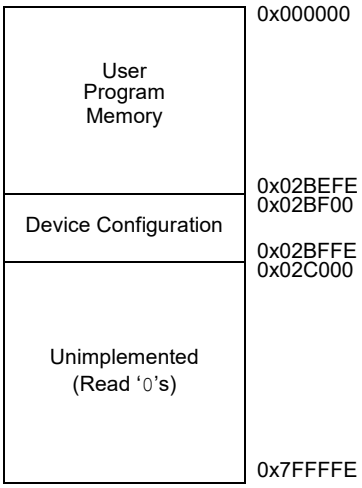
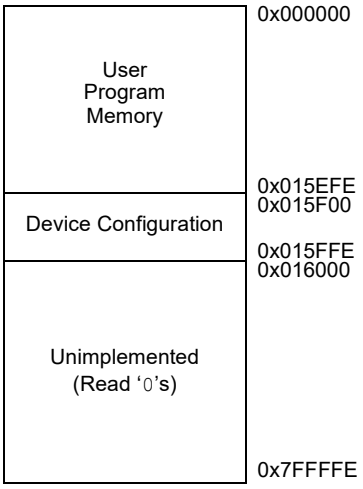


Figure 4-3. Program Memory Map for dsPIC33CDVL128MC506/106 and dsPIC33CDV128MC506/106 Devices



4.1.1. Program Memory Organization

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address in program memory as consisting of a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Interrupt and Trap Vectors).

Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented by two during code execution. This arrangement provides compatibility with Data Memory Space Addressing and makes data in the program memory space accessible.

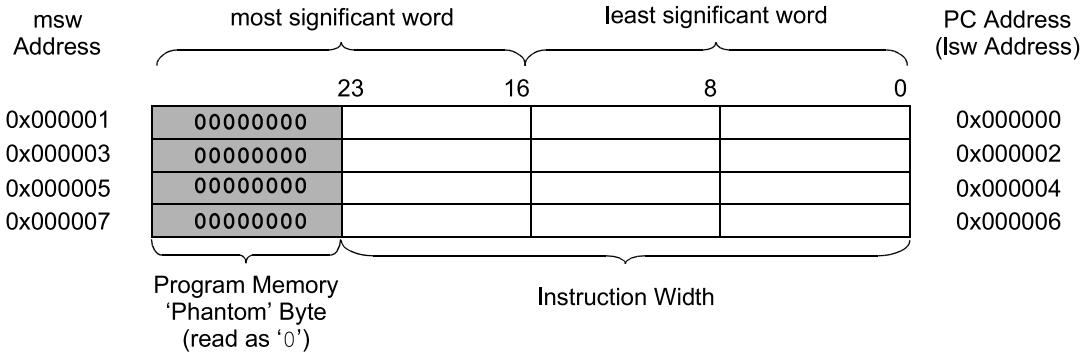
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4.1.2. Interrupt and Trap Vectors

All dsPIC33CDVL256MC506 family devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A `GOTO` instruction is programmed by the user application at address 0x000000 of Flash memory, with the actual address for the start of code at address 0x000002 of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in the Interrupt Controller section.

Figure 4-4. Program Memory Organization



4.1.2.1. Unique Device Identifier (UDID)

All dsPIC33CDVL256MC506 family devices are individually encoded during final manufacturing with a Unique Device Identifier or UDID. The UDID cannot be erased by a bulk erase command or any other user-accessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a requirement. It may also be used by the application manufacturer for any number of things that may require unique identification, such as:

- Tracking the device
- Unique serial number
- Unique security key

The UDID comprises five 24-bit program words. When taken together, these fields form a unique 120-bit identifier.

The UDID is stored in five read-only locations, located between 0x801200 and 0x801208 in the device configuration space. Table 4-1 lists the addresses of the identifier words and shows their contents.

Table 4-1. UDID Addresses

UDID	Address	Description
UDID1	0x801200	UDID Word 1
UDID2	0x801202	UDID Word 2
UDID3	0x801204	UDID Word 3
UDID4	0x801206	UDID Word 4
UDID5	0x801208	UDID Word 5

4.2. Data Address Space

The dsPIC33CDVL256MC506 family CPU has a separate 16-bit wide data memory space. The Data Space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory map is shown in Near Data Space.

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All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This arrangement gives a base Data Space address range of 64 Kbytes or 32K words.

The lower half of the data memory space (i.e., when EA[15] = 0) is used for implemented memory addresses, while the upper half (EA[15] = 1) is reserved for the Program Space Visibility (PSV).

The dsPIC33CDVL256MC506 family devices implement up to 48 Kbytes of data memory. If an EA points to a location outside of this area, an all-zero word or byte is returned.

4.2.1. Data Space Width

The data memory space is organized in byte-addressable, 16-bit wide blocks. Data are aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

4.2.2. Data Memory Organization and Alignment

To maintain backward compatibility with PIC® MCU devices and improve Data Space memory usage efficiency, the dsPIC33CDVL256MC506 family instruction set supports both word and byte operations. As a consequence of byte accessibility, all effective address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB; the MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

4.2.3. SFR Space

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, are primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33CDVL256MC506 family core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

Note: The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

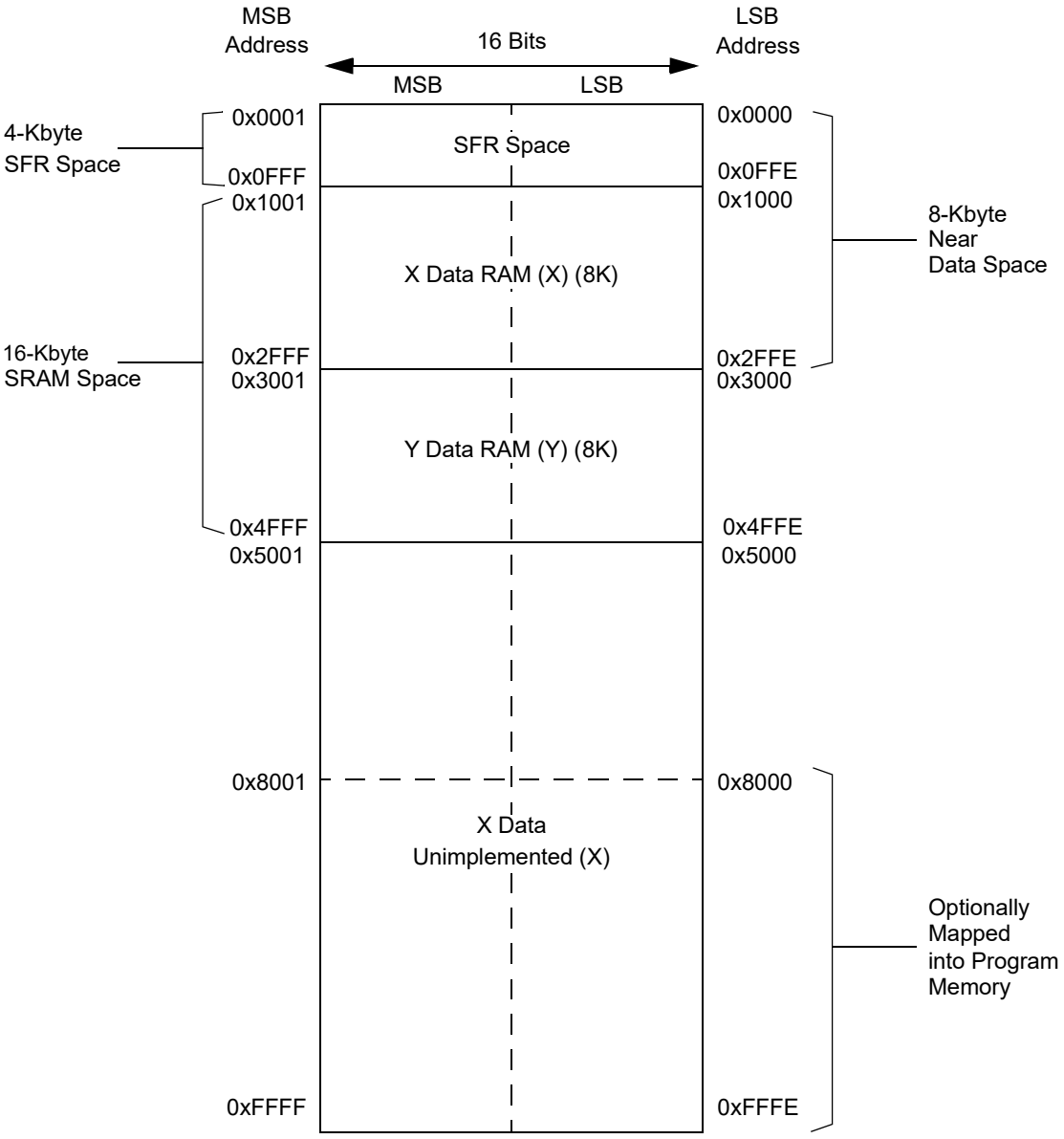
4.2.4. Near Data Space

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole Data Space is addressable using MOV instructions, which

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support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a Working register as an address pointer.

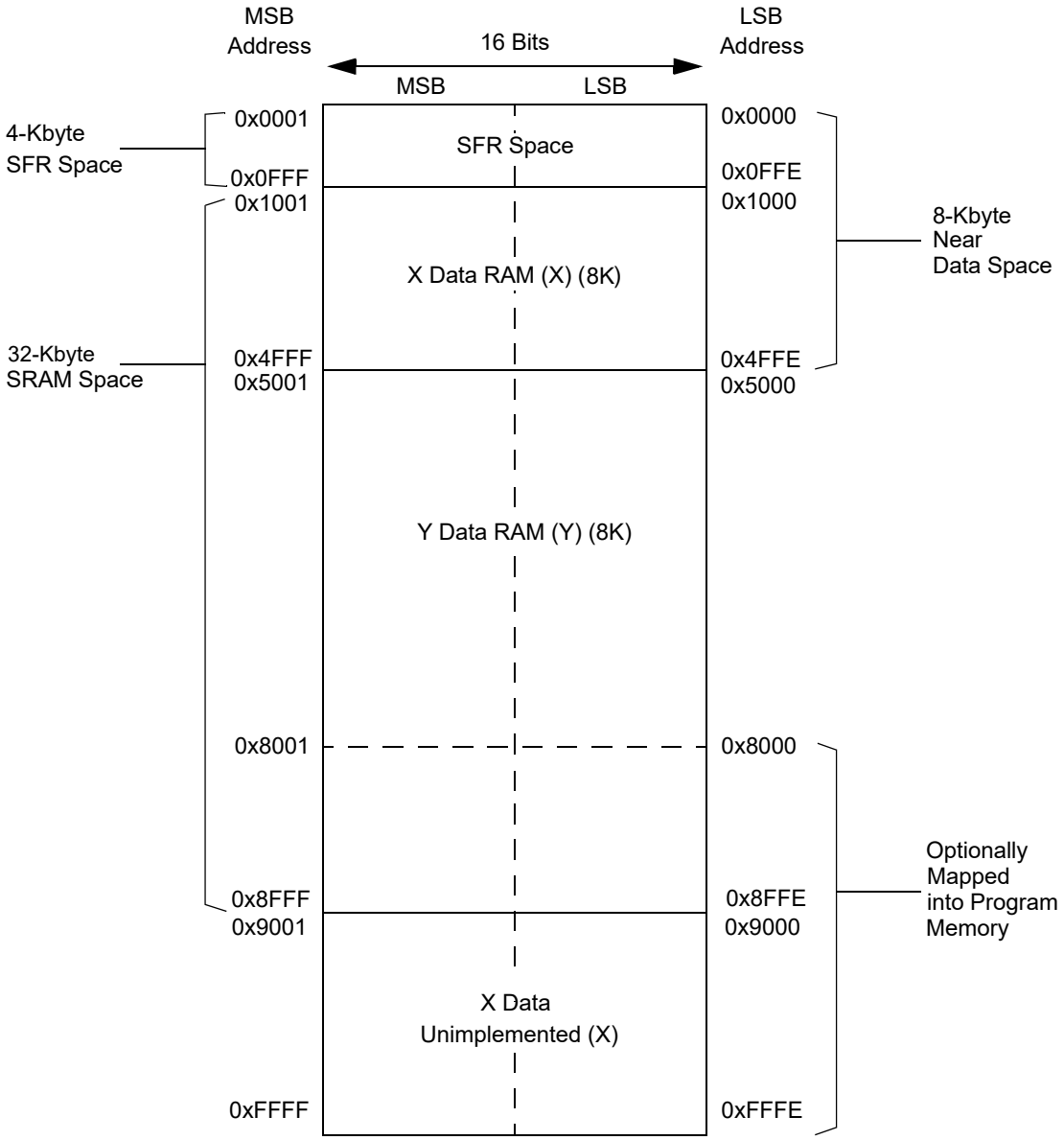
Figure 4-5. Data Memory Map for dsPIC33CDVL128MC106 Devices



Note: Memory areas are not shown to scale.

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Figure 4-6. Data Memory Map for dsPIC33CDVL256MC506 Devices



Note: Memory areas are not shown to scale.

4.2.5. X and Y Data Spaces

The dsPIC33CDVL256MC506 family core has two Data Spaces, X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X Data Space is used by all instructions and supports all addressing modes. X Data Space has separate read and write data buses. The X read data bus is the read data path for all instructions

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that view Data Space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y Data Space is used in concert with the X Data Space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X Data Space.

All data memory writes, including in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

4.3. BIST Overview

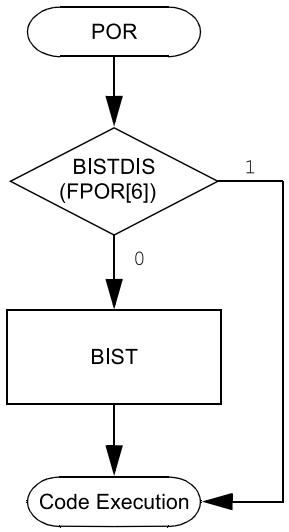
The dsPIC33CDVL256MC506 family features a data memory Built-In Self-Test (BIST) that has the option to be run at start-up or run time. The memory test checks that all memory locations are functional and provides a pass/fail status of the RAM that can be used by software to take action if needed. If a failure is reported, the specific location(s) are not identified. The BIST feature operates with a clock of FRC+PLL with PLL settings, forced by hardware to result in a 125 MHz clock rate, at both start-up and run time.

The MBISTCON register (MBISTCON) contains control and status bits for BIST operation. The MBISTDONE bit (MBISTCON[7]) indicates if a BIST was run since the last Reset, and the MBISTSTAT bit (MBISTCON[4]) provides the pass/fail result.

4.3.1. BIST at Start-up

The BIST can be configured to automatically run on a POR-type Reset, as shown in Figure 4-7. By default, when BISTDIS (FPOR[6]) = 1, the BIST is disabled and will not be part of device start-up. If the BISTDIS bit is cleared during device programming, the BIST will run after all Configuration registers have been loaded and before code execution begins.

Figure 4-7. BIST Flowchart



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4.3.2. BIST at Run Time

The BIST can also be run at any time during code execution. Note that a BIST will corrupt all of the RAM contents, including the stack pointer, and requires a subsequent Reset. The system should be prepared for a Reset before a BIST is performed. The BIST is invoked by setting the MBISTEN bit (MBISTCON[0]). The MBISTCON register is protected against accidental writes and requires an unlock sequence prior to writing. Only one bit can be set per unlock sequence. The procedure for a run-time BIST is as follows:

1. Execute the unlock sequence by consecutively writing 0x55 and 0xAA to the NVMKEY register.
2. Write 0x0001 to the MBISTCON SFR.
3. Execute a software `RESET` command.
4. Verify a Software Reset has occurred by reading SWR (RCON[6]) (optional).
5. Verify that the MBISTDONE bit is set.
6. Take action depending on test result indicated by MBISTSTAT.

4.3.2.1. Fault Simulation

A mechanism is available to simulate a BIST failure to allow testing of Fault handling software. When the FLTINJ bit is set during a run-time BIST, the MBISTSTAT bit will be set regardless of the test result. The procedure for a BIST Fault simulation is as follows:

1. Execute the unlock sequence by consecutively writing 0x55 and 0xAA to the NVMKEY register.
2. Set the MBISTEN bit (MBISTCON[0]).
3. Execute 2nd unlock sequence by consecutively writing 0x55 and 0xAA to the NVMKEY register.
4. Set the FLTINJ bit (MBISTCON[8]).
5. Execute a software `RESET` command.
6. Verify the MBISTDONE, MBSITSTAT and FLTINJ bits are all set.

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4.3.3. MBIST Control Register

Name: MBISTCON
Offset: 0xEFC

Notes:

1. Resets only on a true POR Reset.
2. This bit will self-clear when the MBIST test is complete.

Legend: HS = Hardware Settable bit; HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
								FLTINJ
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
	MBISTDONE			MBISTSTAT				MBISTEN
Access	R/W/HS			R				R/W/HC-0
Reset	0			0				0

Bit 8 – FLTINJ MBIST Fault Inject Control bit(1)

Value	Description
1	The MBIST test will complete and sets MBISTSTAT = 1, simulating an SRAM test failure.
0	The MBIST test will execute normally.

Bit 7 – MBISTDONE MBIST Done Status bit

Value	Description
1	An MBIST operation has been executed.
0	No MBIST operation has occurred on the last Reset sequence.

Bit 4 – MBISTSTAT MBIST Status bit

Value	Description
1	The last MBIST failed.
0	The last MBIST passed.

Bit 0 – MBISTEN MBIST Enable bit(2)

Value	Description
1	MBIST test is armed; an MBIST test will execute at the next device Reset.
0	MBIST test is disarmed.

4.4. Memory Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page contains the latest updates and additional information.

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4.4.1. Key Resources

- **"dsPIC33/PIC24 Program Memory"** (www.microchip.com/DS70000613) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

4.4.2. Paged Memory Scheme

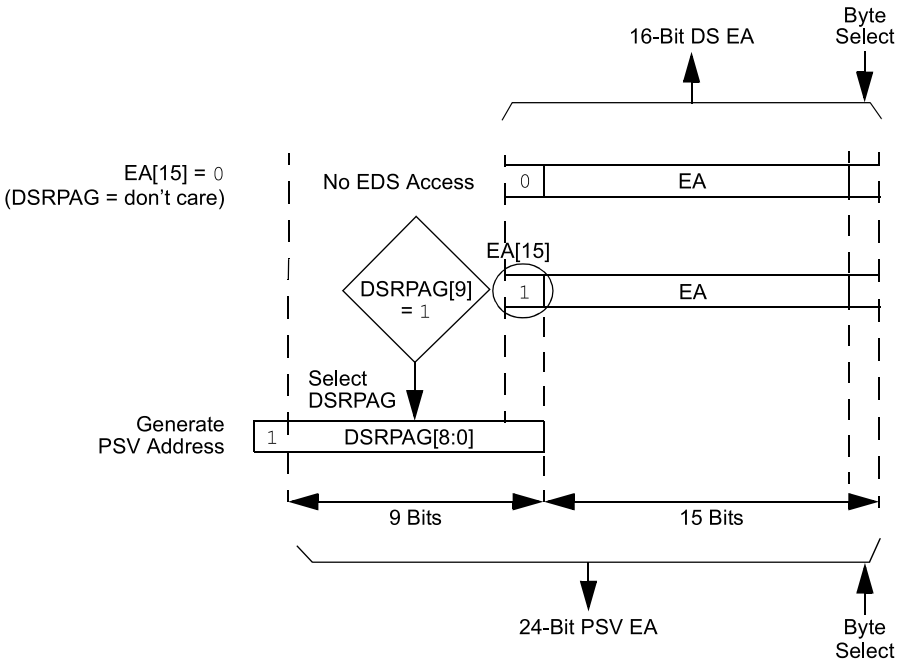
The dsPIC33CDVL256MC506 architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using `MOV` instructions in a linear fashion for pre- and post-modified Effective Addresses (EAs). The upper half of the base Data Space address is used in conjunction with the Data Space Read Page (DSRPAG) register to form the Program Space Visibility (PSV) address.

The Data Space Read Page (DSRPAG) register is located in the SFR space. When DSRPAG[9] = `1` and the base address bit, EA[15] = `1`, the DSRPAG[8:0] bits are concatenated onto EA[14:0] to form the 24-bit PSV read address.

The paged memory scheme provides access to multiple 32-Kbyte windows in the PSV memory. The Data Space Read Page (DSRPAG) register, in combination with the upper half of the Data Space address, can provide up to 8 Mbytes of PSV address space. The paged data memory space is shown in Figure 4-8.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG.

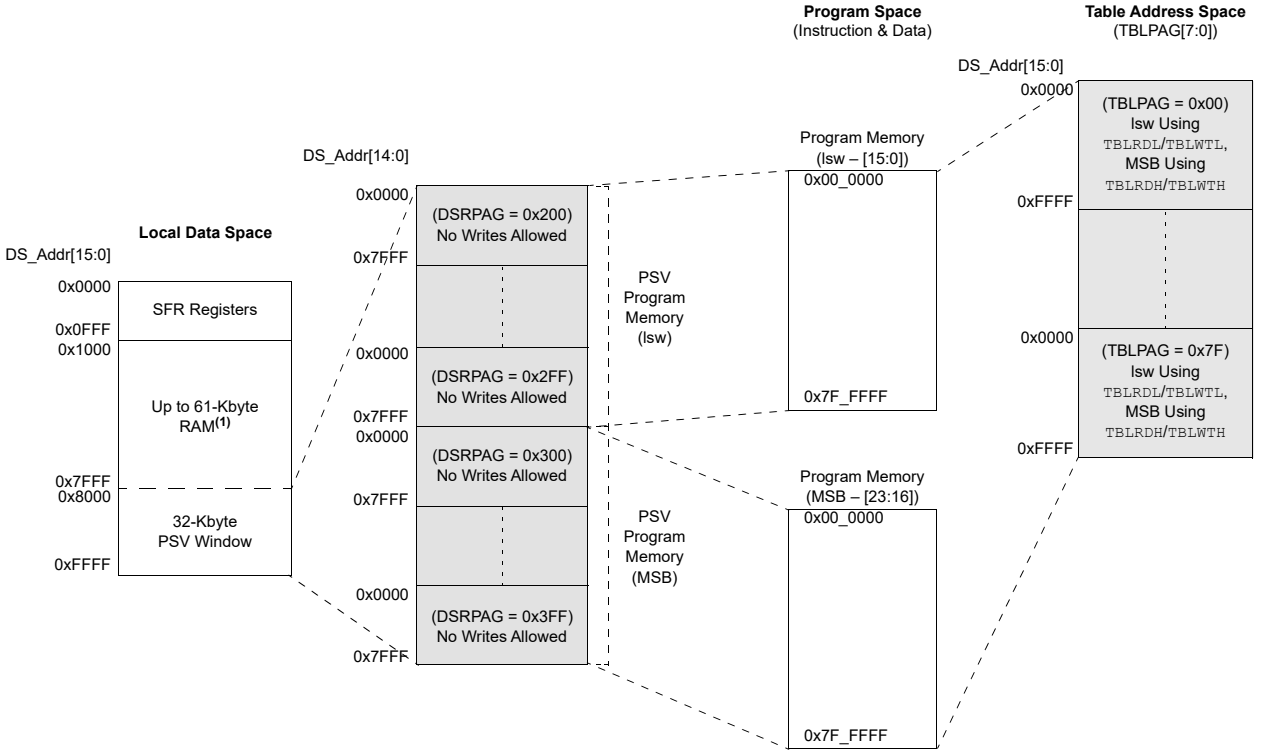
Figure 4-8. Program Space Visibility (PSV) Read Address Generation



Note: DS read access when DSRPAG = 0x000 will force an address error trap.

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Figure 4-9. Paged Data Memory Space



When a PSV page overflow or underflow occurs, EA[15] is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the PSV pages can occur at the page boundaries when:

- The initial address, prior to modification, addresses the PSV page.
- The EA calculation uses Pre- or Post-Modified Register Indirect Addressing; however, this does not include Register Offset Addressing.

In general, when an overflow is detected, the DSRPAG register is incremented and the EA[15] bit is set to keep the base address within the PSV window. When an underflow is detected, the DSRPAG register is decremented and the EA[15] bit is set to keep the base address within the PSV window. This creates a linear PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0 and PSV spaces. Table 4-2 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA[15] bit is set and the DSRPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

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Table 4-2. Overflow and Underflow Scenarios at Page 0 and PSV Space Boundaries(2,3,4)

O/U, R/W	Operation	Before			After		
		DSRPAG	DS EA[15]	Page Description	DSRPAG	DS EA[15]	Page Description
O, Read	[++Wn] or [Wn++]	DSRPAG = 0x2FF	1	PSV: Last lsw page	DSRPAG = 0x300	1	PSV: First MSB page
O, Read		DSRPAG = 0x3FF	1	PSV: Last MSB page	DSRPAG = 0x3FF	0	See **Note 1**
U, Read	[--Wn] or [Wn--]	DSRPAG = 0x001	1	PSV page	DSRPAG = 0x001	0	See **Note 1**
U, Read		DSRPAG = 0x200	1	PSV: First lsw page	DSRPAG = 0x200	0	See **Note 1**
U, Read		DSRPAG = 0x300	1	PSV: First MSB page	DSRPAG = 0x2FF	1	PSV: Last lsw page

Legend: O = Overflow, U = Underflow

Notes:

1. The Register Indirect Addressing now addresses a location in the base Data Space (0x0000-0x8000).
2. An EDS access, with DSRPAG = 0x000, will generate an address error trap.
3. Only reads from PS are supported using DSRPAG.
4. Pseudolinear Addressing is not supported for large offsets.

4.4.2.1. Extended X Data Space

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible, regardless of the contents of the Data Space Read Page register. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA[15] = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF of base Data Space, in combination with DSRPAG = 0x00. Consequently, DSRPAG is initialized to 0x001 at Reset.

Notes:

1. DSRPAG should not be used to access Page 0. An EDS access with DSRPAG set to 0x000 will generate an address error trap.
2. Clearing the DSRPAG in software has no effect.

The remaining PSV pages are only accessible using the DSRPAG register in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where the base address bit, EA[15] = 1.

4.4.2.2. Software Stack

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating the stack pointer (for example, creating stack frames).

Note: To protect against misaligned stack accesses, W15[0] is fixed to '0' by the hardware.

W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33CDVL256MC506 devices and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within the Data Space.

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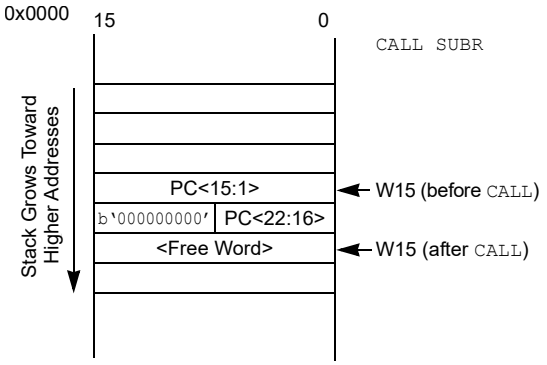
The Software Stack Pointer always points to the first available free word and fills the software stack, working from lower toward higher addresses. Figure 4-10 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC[15:0] are pushed onto the first available stack word, then PC[22:16] are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-10. During exception processing, the MSB of the PC is concatenated with the lower eight bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

Notes:

1. To maintain system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging and is, therefore, restricted to an address range of 0x0000 to 0xFFFF. The same applies to W14 when used as a Stack Frame Pointer (SFA = 1).
2. As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment.

Figure 4-10. CALL Stack Frame



4.4.3. Instruction Addressing Modes

The addressing modes shown in Table 4-3 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

Table 4-3. Fundamental Addressing Modes Supported

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

4.4.3.1. File Registration Instructions

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a

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register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.4.3.2. MCU Instructions

The three-operand MCU instructions are of the form:

```
Operand 3 = Operand 1 [function] Operand 2
```

where Operand 1 is always a Working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

4.4.3.3. Move and Accumulator Instructions

Move instructions, and the DSP accumulator class of instructions, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.4.3.4. MAC Instructions

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the data pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The effective addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

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Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.4.3.5. Other Instructions

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

4.4.4. Modulo Addressing

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the data pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a Bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

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4.4.4.1. Modulo and Bit-Reversed Addressing Control Register

Name: MODCON
Offset: 0x46

Bit	15	14	13	12	11	10	9	8
	XMODEN	YMODEN			BWM[3:0]			
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	7	6	5	4	3	2	1	0
	YWM[3:0]				XWM[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – XMODEN X RAGU and X WAGU Modulus Addressing Enable bit

Value	Description
1	X AGU Modulus Addressing enabled.
0	X AGU Modulus Addressing disabled.

Bit 14 – YMODEN Y AGU Modulus Addressing Enable bit

Value	Description
1	Y AGU Modulus Addressing enabled.
0	Y AGU Modulus Addressing disabled.

Bits 11:8 – BWM[3:0] X WAGU Register Select for Bit-Reversed Addressing bits

Value	Description
1111	W15 Bit-Reversed Addressing disabled.
1110	W14 selected for Bit-Reversed Addressing.
0000	W0 selected for Bit-Reversed Addressing.

Bits 7:4 – YWM[3:0] Y AGU W Register Select for Modulo Addressing bits

Value	Description
1111	W15 Bit-Reversed Addressing disabled.
1110	W14 selected for Bit-Reversed Addressing.
0000	W0 selected for Bit-Reversed Addressing.

Bits 3:0 – XWM[3:0] X RAGU and X WAGU W Register Select for Modulo Addressing bits

Value	Description
1111	W15 Bit-Reversed Addressing disabled.
1110	W14 selected for Bit-Reversed Addressing.
0000	W0 selected for Bit-Reversed Addressing.

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4.4.4.2. X AGU Modulo Addressing Start Register

Name: XMODSRT
Offset: 0x48

Bit	15	14	13	12	11	10	9	8
	XS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	XS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – XS[15:0] X RAGU and X WAGU Modulo Addressing Start Address bits

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4.4.4.3. X AGU Modulo Addressing End Register

Name: XMODEND
Offset: 0x4A

Bit	15	14	13	12	11	10	9	8
	XE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	XE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – XE[15:0] X RAGU and X WAGU Modulo Addressing End Address bits

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4.4.4.4. Y AGU Modulo Addressing Start Register

Name: YMODSRT
Offset: 0x4C

Bit	15	14	13	12	11	10	9	8
	YS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	YS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – YS[15:0] Y AGU Modulo Addressing Start Address bits

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4.4.4.5. Y AGU Modulo Addressing End Register

Name: YMODEND
Offset: 0x4E

Bit	15	14	13	12	11	10	9	8
	YE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	YE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – YE[15:0] X AGU Modulo Addressing End Address bits

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4.4.4.6. X AGU Bit-Reversed Addressing Control Register

Name: XBREV
Offset: 0x50

Bit	15	14	13	12	11	10	9	8
	BREN	XB[14:8]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	XB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bit 15 – BREN Bit-Reversed Addressing (X AGU) Enable bit

Value	Description
1	Bit-Reversed Addressing enabled.
0	Bit-Reversed Addressing disabled.

Bits 14:0 – XB[14:0] X AGU Bit-Reversed Modifier bits

4.4.4.7. Start and End Address

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND.

Note: Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.4.4.8. W Address Register Selection

The Modulo and Bit-Reversed Addressing Control register, MODCON, contains enable flags, as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

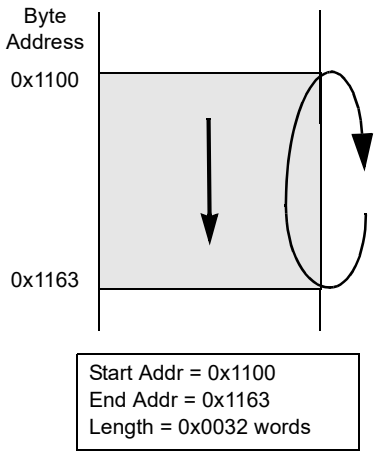
- If XWM = `1111`, X RAGU and X WAGU Modulo Addressing is disabled.
- If YWM = `1111`, Y AGU Modulo Addressing is disabled.

The X Address Space Pointer W (XWM) register, to which Modulo Addressing is to be applied, is stored in MODCON[3:0]. Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '`1111`' and the XMODEN bit (MODCON[15]) is set.

The Y Address Space Pointer W (YWM) register, to which Modulo Addressing is to be applied, is stored in MODCON[7:4]. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '`1111`' and the YMODEN bit (MODCON[14]) is set.

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Figure 4-11. Modulo Addressing Operation Example




```
MOV     #0x1100, W0
MOV     W0, XMODSRT     ;set modulo start address
MOV     #0x1163, W0
MOV     W0, MODEND      ;set modulo end address
MOV     #0x8001, W0
MOV     W0, MODCON      ;enable W1, X AGU for modulo

MOV     #0x0000, W0     ;W0 holds buffer fill value

MOV     #0x1110, W1     ;point W1 to buffer

DO      AGAIN, #0x31    ;fill the 50 buffer locations
MOV     W0, [W1++]      ;fill the next location
AGAIN:  INC W0, W0      ;increment the fill value
```

4.4.4.9. Modulo Addressing Applicability

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note: The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed, but the contents of the register remain unchanged.

4.5. Bit-Reversed Addressing

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.5.1. Bit-Reversed Addressing Implementation

Bit-Reversed Addressing mode is enabled in any of these situations:

- BWMx bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing).
- The BREN bit is set in the XBREV register.
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment.

If the length of a bit-reversed buffer is M = 2^N bytes, the last 'N' bits of the data buffer start address must be zeros.

XB[14:0] are the Bit-Reversed Addressing modifier, or pivot point, which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

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Note: All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data are a requirement, the LSb of the EA is ignored (and always clear).

Note: Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV[15]) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

Figure 4-12. Bit-Reversed Addressing Example

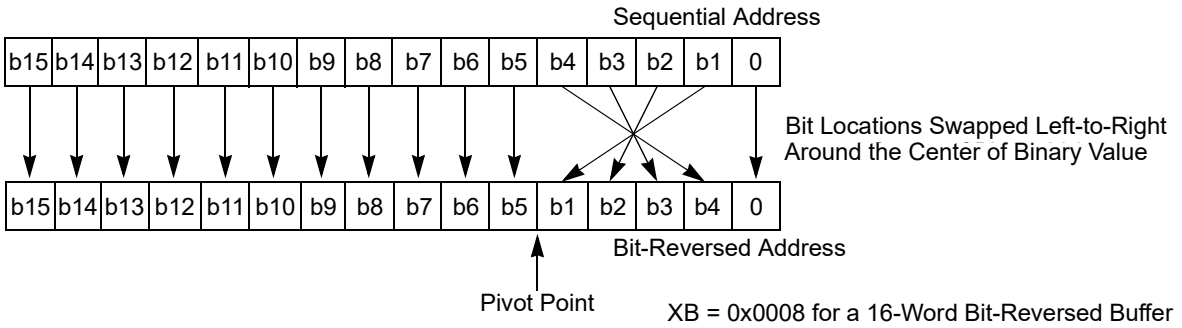


Table 4-4. Bit-Reversed Addressing Sequence (16-Entry)

Normal Address					Bit-Reversed Address				
A3	**A2**	**A1**	**A0**	**Decimal**	**A3**	**A2**	**A1**	**A0**	**Decimal**
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

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4.6. Interfacing Program and Data Memory Spaces

The dsPIC33CDVL256MC506 family architecture uses a 24-bit wide Program Space and a 16-bit wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use these data successfully, they must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33CDVL256MC506 family devices provides two methods by which Program Space can be accessed during operation:

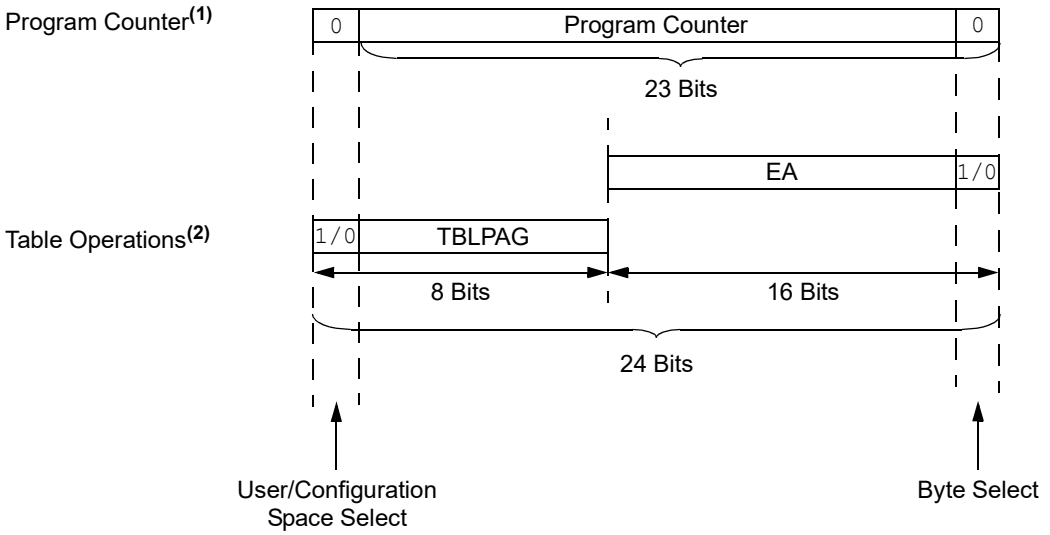
- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for lookups from a large table of static data. The application can only access the least significant word of the program word.

Table 4-5. Program Space Address Construction

Access Type	Access Space	Program Space Address				
		[23]	[22:16]	[15]	[14:1]	[0]
Instruction Access (Code Execution)	User	0	PC[22:1]			0
		0xxx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG[7:0]		Data EA[15:0]		
		0xxx xxxx xxxx xxxx xxxx xxxx				
	Configuration	TBLPAG[7:0]		Data EA[15:0]		
		1xxx xxxx xxxx xxxx xxxx xxxx				

Figure 4-13. Data Access from Program Space Address Generation



Note 1: The Least Significant bit (LSb) of Program Space addresses is always fixed as '0' to maintain word alignment of data in the Program and Data Spaces.

2: Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.

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4.6.1. Data Access from Program Memory Using Table Instructions

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper eight bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

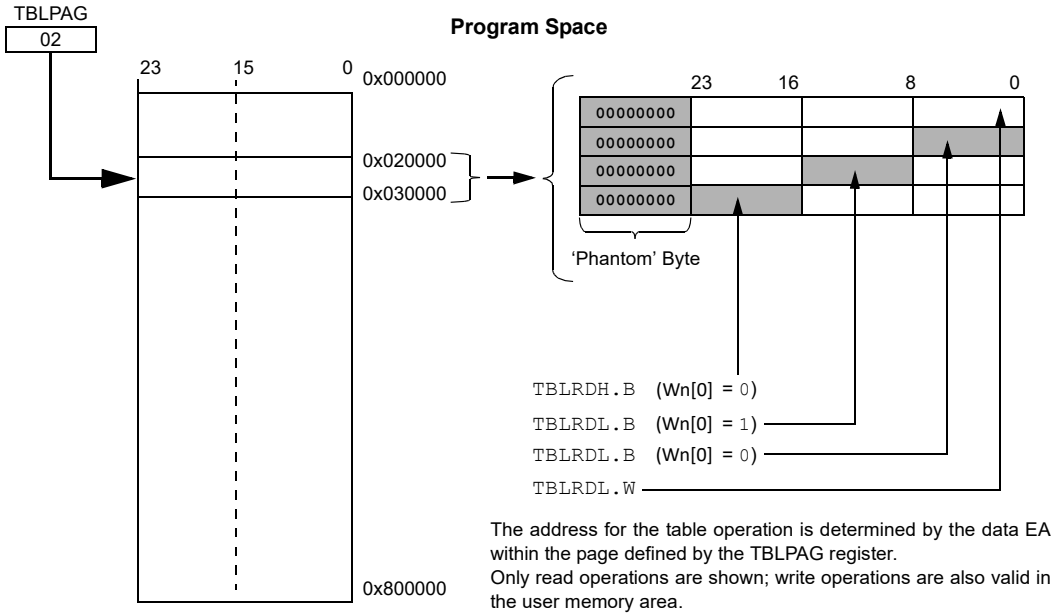
- TBLRDL (Table Read Low):
  - In Word mode, this instruction maps the lower word of the Program Space location (P[15:0]) to a data address (D[15:0])
  - In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.
- TBLRDH (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address (P[23:16]) to a data address. The 'phantom' byte (D[15:8]) is always '0'.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to D[7:0] of the data address in the TBLRDL instruction. The data is always '0' when the upper phantom byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in Flash Program Memory.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG[7] = 0, the table page is located in the user memory space. When TBLPAG[7] = 1, the page is located in the configuration space.

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Figure 4-14. Accessing Program Memory with Table Instructions



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5. Flash Program Memory

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Flash Programming"** (www.microchip.com/DS70000609) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The dsPIC33CDVL256MC506 family devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire V_{DD} range.

Flash memory can be programmed in three ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)
- Run-Time Self-Programming (RTSP)

ICSP allows for a dsPIC33CDVL256MC506 family device to be serially programmed while in the end application circuit. This is done with a Programming Clock and Programming Data (PGCx/PGDx) line and three other lines for power (V_{DD}), ground (V_{SS}) and Master Clear ($\overline{MCLR}$). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

Enhanced In-Circuit Serial Programming uses an on-board bootloader, known as the Programming Executive, to manage the programming process. Using an SPI data frame format, the Programming Executive can erase, program and verify program memory. For more information on Enhanced ICSP, see the device programming specification.

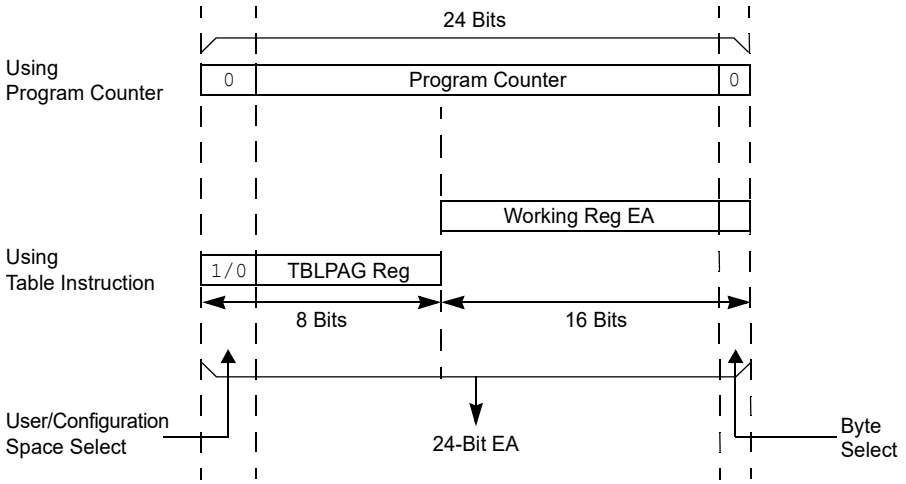
RTSP is accomplished using `TBLRD` (Table Read) and `TBLWT` (Table Write) instructions. With RTSP, the user application can write program memory data by double program memory words or by blocks (rows) of 128 instructions (256 addressable bytes). RTSP can erase program memory in blocks (pages) of 1024 instructions (2048 addressable bytes) at a time.

5.1. Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the table read and table write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in Normal Operating mode. The 24-bit target address in the program memory is formed using bits[7:0] of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instructions, as shown in Figure 5-1. The `TBLRDL` and `TBLWTL` instructions are used to read or write to bits[15:0] of program memory. `TBLRDL` and `TBLWTL` can access program memory in both Word and Byte modes. The `TBLRDH` and `TBLWTH` instructions are used to read or write to bits[23:16] of program memory. `TBLRDH` and `TBLWTH` can also access program memory in Word or Byte mode.

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Figure 5-1. Addressing for Table Registers



5.2. RTSP Operation

RTSP allows the user application to program one double instruction word or one row at a time. The double instruction word write blocks and single row write blocks are edge-aligned, from the beginning of program memory, on boundaries of one double instruction word and 64 double instruction words, respectively.

The basic sequence for RTSP programming is to first load two 24-bit instructions into the NVM write latches found in configuration memory space. Refer to Table 4-1 through Table 4-3 for write latch addresses. Then, the WR bit in the NVMCON register is set to initiate the write process. The processor stalls (waits) until the programming operation is finished. The WR bit is automatically cleared when the operation is finished.

Double instruction word writes are performed by manually loading both write latches, using `TBLWTL` and `TBLWTH` instructions, and then initiating the NVM write while the NVMOPx bits are set to '0x1'. The program space destination address is defined by the NVMADR/U registers.

Row programming is performed by first loading 128 instructions into data RAM and then loading the address of the first instruction in that row into the NVMSRCADRL/H registers. Once the write has been initiated, the device will automatically load two instructions into the write latches and write them to the program space destination address defined by the NVMADR/U registers.

The operation will increment the NVMSRCADRL/H and the NVMADR/U registers until all double instruction words have been programmed.

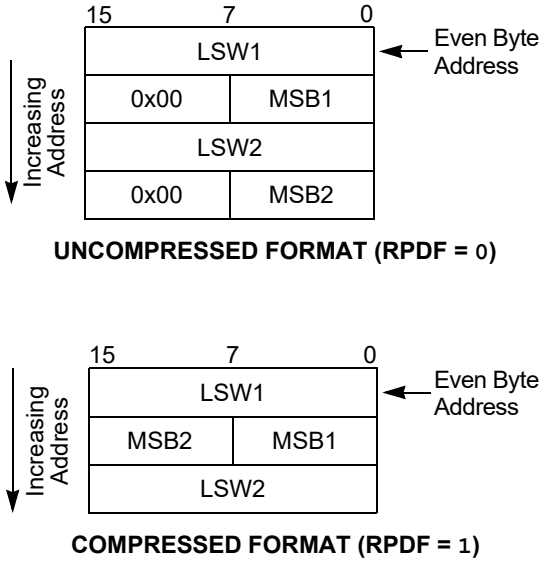
The RPDF bit (NVMCON[9]) selects the format of the stored data in RAM to be either compressed or uncompressed. See Figure 5-2 for data formatting.

Compressed data help to reduce the amount of required RAM by using the upper byte of the second word for the MSB of the second instruction.

All erase and program operations may optionally use the NVM interrupt to signal the successful completion of the operation.

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Figure 5-2. Uncompressed/Compressed Format



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Example 5-1. Flash Write/Read

```
/////////Flash write ////////////////////////
//Sample code for writing 0x123456 to address locations 0x10000 / 10002
NVMCON = 0x4001;
TBLPAG = 0xFA;                 // write latch upper address
NVMADR = 0x0000;               // set target write address of general segment
NVMADRU = 0x0001;
__builtin_tblwtl(0, 0x3456);   // load write latches
__builtin_tblwth (0,0x12);
__builtin_tblwtl(2, 0x3456);   // load write latches
__builtin_tblwth (2,0x12);
asm volatile ("disi #5");
__builtin_write_NVM();
while(_WR == 1 ) ;

////////////Flash Read///////////////
//Sample code to read the Flash content of address 0x10000
// readDataL/ readDataH variables need to defined
TBLPAG = 0x0001;
readDataL = __builtin_tblrdl(0x0000);
readDataH = __builtin_tblrdh(0x0000);
```

5.3. Error Correcting Code (ECC)

In order to improve program memory performance and durability, the devices include Error Correcting Code functionality (ECC) as an integral part of the Flash memory controller. ECC can determine the presence of single-bit errors in program data, including which bit is in error, and correct the data automatically without user intervention. ECC cannot be disabled.

When data are written to program memory, ECC generates a 7-bit Hamming code parity value for every two (24-bit) instruction words. The data are stored in blocks of 48 data bits and seven parity bits; parity data are not memory-mapped and are inaccessible. When the data are read back, the ECC calculates the parity on them and compares it to the previously stored parity value. If a parity mismatch occurs, there are two possible outcomes:

- A single-bit error has occurred and has been automatically corrected on read back.
- A double-bit error has occurred and the read data are not changed.

Single-bit error occurrence can be identified by the state of the ECCSBEIF (IFS0[13]) bit. An interrupt can be generated when the corresponding interrupt enable bit, ECCSBEIE (IEC0[13]), is set. The ECCSTATL register contains the parity information for single-bit errors. The SECOUT[7:0] bit field contains the expected calculated SEC parity, and the SECIN[7:0] bits contain the actual value from a Flash read operation. The SECSYNDx bits (ECCSTATH[7:0]) indicate the bit position of the single-bit error within the 48-bit pair of instruction words. When no error is present, SECINx equals SECOUTx and SECSYNDx is zero. The ECCSTATL and ECCSTATH registers will only update and be valid when an error has occurred, or when including Fault injection is enabled and an ECCADDR match occurs.

Double-bit errors result in a generic hard trap. The ECCDBE bit (INTCON4[1]) will be set to identify the source of the hard trap. If no Interrupt Service Routine is implemented for the hard trap, a device Reset will also occur. The ECCSTATH register contains double-bit error status information. The DEDOUT bit is the expected calculated DED parity and DEDIN is the actual value from a Flash read operation. When no error is present, DEDIN equals DEDOUT.

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5.4. ECC Fault Injection

To test Fault handling, an EEC error can be generated. Both single and double-bit errors can be generated in both the read and write data paths. Read path Fault injection first reads the Flash data and then modifies them prior to entering the ECC logic. Write path Fault injection modifies the actual data prior to them being written into the target Flash and will cause an EEC error on a subsequent Flash read. The following procedure is used to inject a Fault:

1. Load Flash target address into the ECCADDR register.
2. Select the first Fault bit determined by FLT1PTRx (ECCCONH[7:0]). The target bit is inverted to create the Fault.
3. If a double Fault is desired, select the second Fault bit determined by FLT2PTRx (ECCCONH[15:8]); otherwise, set to all '1's.
4. Write the NVMKEY unlock sequence.
5. Enable the ECC Fault injection logic by setting the FLTINJ bit (ECCCONL[0]).
6. Perform a read or write to the Flash target address.

5.5. Flash OTP by ICSP™ Write Inhibit

ICSP Write Inhibit is an access restriction feature that, when activated, restricts all Flash memory. Once activated, ICSP Write Inhibit permanently prevents ICSP Flash programming and erase operations and cannot be deactivated. This feature is intended to prevent alteration of Flash memory contents, with behavior similar to One-Time-Programmable (OTP) devices.

RTSP, including erase and programming operations, is not restricted when ICSP Write Inhibit is activated; however, code to perform these actions must be programmed into the device before ICSP Write Inhibit is activated. This allows for a bootloader-type application to alter Flash contents with ICSP Write Inhibit activated.

Entry into ICSP and Enhanced ICSP modes is not affected by ICSP Write Inhibit. In these modes, it will continue to be possible to read configuration memory space and any user memory space regions that are not code-protected. With ICSP writes inhibited, an attempt to set WR (NVMCON[15]) = 1 will maintain WR = 0, and instead, set WRERR (NVMCON[13]) = 1. All Enhanced ICSP erase and programming commands will have no effect, with self-checked programming commands returning a FAIL response opcode (PASS if the destination already exactly matched the requested programming data).

Once ICSP Write Inhibit is activated, it is not possible for a device executing in Debug mode to erase/write Flash, nor can a debug tool switch the device to Production mode. ICSP Write Inhibit should, therefore, only be activated on devices programmed for production.

5.5.1. Activating Flash OTP by ISCP Write Inhibit

Note: It is not possible to deactivate ICSP Write Inhibit.

ICSP Write Inhibit is activated by executing a pair of NVMCON double-word programming commands to save two 16-bit activation values in the configuration memory space. The target NVM addresses and values required for activation are shown in Table 5-1. Once both addresses contain their activation values, ICSP Write Inhibit will take permanent effect on the next device Reset.

Only the lower 16 data bits stored at the activation addresses are evaluated; the upper eight bits and second 24-bit word written by the double-word programming should be written as '0's. The addresses can be programmed in any order and also during separate ICSP/Enhanced ICSP/RTSP sessions, but any attempt to program an incorrect 16-bit value or use a row programming operation to program the values will be aborted without altering the existing data.

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Table 5-1. ICSP™ Write Inhibit Activation Addresses and Data

	Configuration Memory Address	ICSP™ Write Inhibit Activation Value
Write Lock 1	0x801028	0x006D63
Write Lock 2	0x80102C	0x006870

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5.6. Program Flash Memory Control Registers

Six SFRs are used to write and erase the Program Flash Memory: NVMCON, NVMKEY, NVMADR/U and NVMSRCADRL/H.

The NVMCON register selects the operation to be performed (page erase, word/row program) and initiates the program or erase cycle.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register. There are two NVM Address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word/row for programming operations, or the selected page for erase operations. The NVMADRU register is used to hold the upper eight bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

For row programming operation, data to be written to Program Flash Memory are written into data memory space (RAM) at an address defined by the NVMSRCADRL/H register pair (location of first element in row programming data).

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5.6.1. NVM Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x08D0	NVMCON	15:8	WR	WREN	WRERR	NVMSIDL			RPDF	URERR
		7:0					NVMOP[3:0]			
0x08D2	NVMADR	15:8	NVMADR[15:8]							
		7:0	NVMADR[7:0]							
0x08D4	NVMADRU	15:8								
		7:0	NVMADRU[23:16]							
0x08D6	NVMKEY	15:8								
		7:0	NVMKEY[7:0]							
0x08D8	NVMSRCADRL	15:8	NVMSRCADR[15:8]							
		7:0	NVMSRCADR[7:0]							
0x08DA	NVMSRCADRH	15:8								
		7:0	NVMSRCADR[23:16]							

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5.6.1.1. Nonvolatile Memory (NVM) Control Register

Name: NVMCON
Offset: 0x8D0

Notes:

1. These bits can only be reset on a POR.
2. If this bit is set, there will be minimal power savings (I_{IDLE}), and upon exiting Idle mode, there is a delay (T_{VREG}) before Flash memory becomes operational.
3. All other combinations of NVMOP[3:0] are unimplemented.
4. Execution of the `PWRSAV` instruction is ignored while any of the NVM operations are in progress.
5. Two adjacent words on a 4-word boundary are programmed during execution of this operation.

Legend: C = Clearable bit; SO = Settable Only bit

Bit	15	14	13	12	11	10	9	8
	WR	WREN	WRERR	NVMSIDL			RPDF	URERR
Access	R/SO	R/W	R/C	R/W			R/W	R/C
Reset	0	0	0	0			0	0

Bit	7	6	5	4	3	2	1	0
					NVMOP[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – WR Write Control bit(1)

Value	Description
1	Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete.
0	Program or erase operation is complete and inactive.

Bit 14 – WREN Write Enable bit(1)

Value	Description
1	Enables Flash program/erase operations
0	Inhibits Flash program/erase operations

Bit 13 – WRERR Write Sequence Error Flag bit(1)

Value	Description
1	An improper program or erase sequence attempt, or termination has occurred (bit is set automatically on any set attempt of the WR bit).
0	The program or erase operation completed normally.

Bit 12 – NVMSIDL NVM Stop in Idle Control bit(2)

Value	Description
1	Flash voltage regulator goes into Standby mode during Idle mode.
0	Flash voltage regulator is active during Idle mode.

Bit 9 – RPDF Row Programming Data Format bit

Value	Description
1	Row data to be stored in RAM are in a compressed format.
0	Row data to be stored in RAM are in an uncompressed format.

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Bit 8 – URERR Row Programming Data Underrun Error bit

Value	Description
1	Indicates row programming operation has been terminated.
0	No data underrun error is detected.

Bits 3:0 – NVMOP[3:0] NVM Operation Select bits(1,3,4)

Value	Description
1111	Reserved
1110	User memory bulk erase operation
1101	Reserved
1100	Reserved
1011	Reserved
1010	Reserved
1001	Reserved
1000	Reserved
0111	Reserved
0101	Reserved
0100	Reserved
0011	Memory page erase operation
0010	Memory row program operation
0001	Memory double-word operation(5)
0000	Reserved

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5.6.1.2. Nonvolatile Memory Lower Address Register

Name: NVMADR
Offset: 0x8D2

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
	NVMADR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	NVMADR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 15:0 – NVMADR[15:0] Nonvolatile Memory Lower Write Address bits
Selects the lower 16 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

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5.6.1.3. Nonvolatile Memory Upper Address Register

Name: NVMADRU
Offset: 0x8D4

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	NVMADRU[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – NVMADRU[23:16] Nonvolatile Memory Upper Write Address bits
Selects the upper 8 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

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5.6.1.4. Nonvolatile Memory Key Register

Name: NVMKEY
Offset: 0x8D6

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	NVMKEY[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – NVMKEY[7:0] NVM Key Register bits (write-only)

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5.6.1.5. NVM Source Data Address Register Low

Name: NVMSRCADRL
Offset: 0x8D8

Bit	15	14	13	12	11	10	9	8
	NVMSRCADR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NVMSRCADR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – NVMSRCADR[15:0] NVM Source Data Address bits
The RAM address of the data to be programmed into Flash when the NVMOP[3:0] bits are set to row programming.

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5.6.1.6. NVM Source Data Address Register High

Name: NVMSRCADRH
Offset: 0x8DA

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	NVMSRCADR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – NVMSRCADR[23:16] NVM Source Data Address bits
The RAM address of the data to be programmed into Flash when the NVMOP[3:0] bits are set to row programming.

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5.7. ECC Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xF0	ECCCONL	15:8								
		7:0								FLTINJ
0xF2	ECCCONH	15:8	FLT2PTR[7:0]							
		7:0	FLT1PTR[7:0]							
0xF4	ECCADDRL	15:8	ECCADDRL[15:8]							
		7:0	ECCADDRL[7:0]							
0xF6	ECCADDRH	15:8								
		7:0	ECCADDRH[23:16]							
0xF8	ECCSTATL	15:8	SECOUT[7:0]							
		7:0	SECIN[7:0]							
0xFA	ECCSTATH	15:8							DEDOUT	DEDIN
		7:0	SYND[7:0]							

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5.7.1. ECC Fault Injection Configuration Register Low

Name: ECCCONL
Offset: 0x0F0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								FLTINJ
Access								R/W
Reset								0

Bit 0 – FLTINJ Fault Injection Sequence Enable bit

Value	Description
1	Enabled
0	Disabled

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5.7.2. ECC Fault Injection Configuration Register High

Name: ECCCONH
Offset: 0x0F2

Bit	15	14	13	12	11	10	9	8
	FLT2PTR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FLT1PTR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – FLT2PTR[7:0] ECC Fault Injection Bit Pointer 2 bits

Value	Description
11111111-00111000	No Fault injection occurs.
00110111	Fault injection (bit inversion) occurs on bit 55 of ECC bit order.
. . .	
00000001	Fault injection (bit inversion) occurs on bit 1 of ECC bit order.
00000000	Fault injection (bit inversion) occurs on bit 0 of ECC bit order.

Bits 7:0 – FLT1PTR[7:0] ECC Fault Injection Bit Pointer 1 bits

Value	Description
11111111-00111000	No Fault injection occurs.
00110111	Fault injection occurs on bit 55 of ECC bit order.
. . .	
00000001	Fault injection occurs on bit 1 of ECC bit order.
00000000	Fault injection occurs on bit 0 of ECC bit order.

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5.7.3. ECC Fault Inject Address Compare Register Low

Name: ECCADDRL
Offset: 0x0F4

Bit	15	14	13	12	11	10	9	8
	ECCADDRL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ECCADDRL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ECCADDRL[15:0] ECC Fault Injection NVM Address Match Compare bits

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5.7.4. ECC Fault Inject Address Compare Register High

Name: ECCADDRH
Offset: 0x0F6

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	ECCADDRH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ECCADDRH[23:16] ECC Fault Injection NVM Address Match Compare bits

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5.7.5. ECC System Status Display Register Low

Name: ECCSTATL
Offset: 0x0F8

Bit	15	14	13	12	11	10	9	8
	SECOUT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SECIN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – SECOUT[7:0] Calculated Single Error Correction Parity Value bits

Bits 7:0 – SECIN[7:0] Read Single Error Correction Parity Value bits
SECIN[7:0] bits are the actual parity value of a Flash read operation.

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5.7.6. ECC System Status Display Register High

Name: ECCSTATH
Offset: 0x0FA

Bit	15	14	13	12	11	10	9	8
							DEDOUT	DEDIN
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	SYND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 9 – DEDOUT Calculated Dual Bit Error Detection Parity bit

Bit 8 – DEDIN Read Dual Bit Error Detection Parity bit
DEDIN is the actual parity value of a Flash read operation.

Bits 7:0 – SYND[7:0] Calculated ECC Syndrome Value bits
Indicates the bit location that contains the error.

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6. Resets

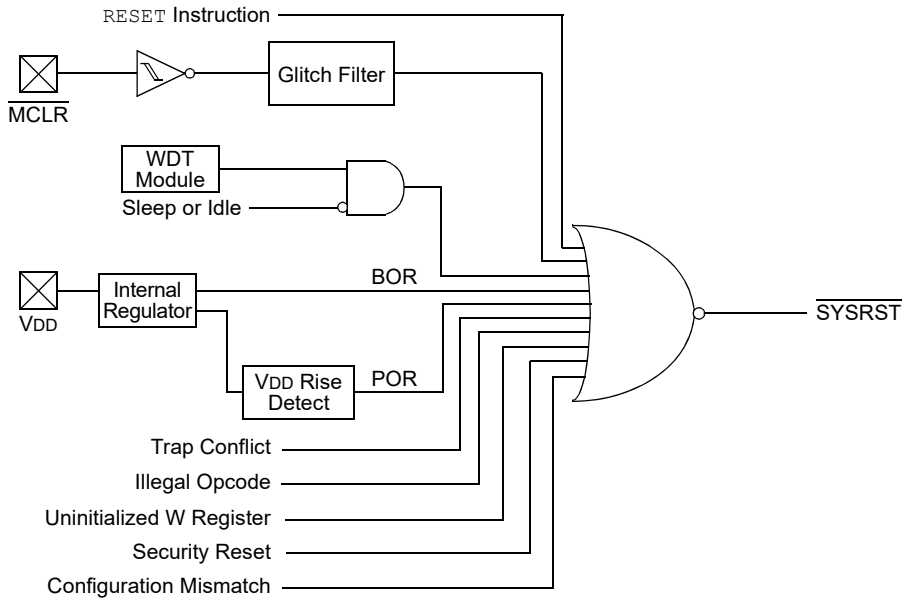
Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Reset"** (www.microchip.com/DS70000602) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- $\overline{\text{MCLR}}$: Master Clear Pin Reset
- SWR: `RESET` Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
  - Illegal Opcode Reset
  - Uninitialized W Register Reset
  - Security Reset

A simplified block diagram of the Reset module is shown in Figure 6-1

Figure 6-1. Master Reset System Block Diagram



Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state, and some are unaffected.

Note: Refer to the specific peripheral section or Memory Organization of this data sheet for register Reset states.

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All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset.

A POR clears all the bits, except for the BOR and POR bits (RCON[1:0]) that are set. The user application can set or clear any bit, at any time, during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

For all Resets, the default clock source is determined by the FNOSC[2:0] bits in the FOSCSEL Configuration register. The value of the FNOSCx bits is loaded into the NOSC[2:0] (OSCCON[10:8]) bits on Reset, which in turn, initializes the system clock.

6.1. Reset Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page contains the latest updates and additional information.

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6.2. Reset Control Register

Name: RCON(1)
Offset: 0xF80

Note:

1. All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

Bit	15	14	13	12	11	10	9	8
	TRAPR	IOPUWR					CM	VREGS
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0

Bit	7	6	5	4	3	2	1	0
	EXTR	SWR		WDTO	SLEEP	IDLE	BOR	POR
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	1	1

Bit 15 – TRAPR Trap Reset Flag bit

Value	Description
1	A Trap Conflict Reset has occurred.
0	A Trap Conflict Reset has not occurred.

Bit 14 – IOPUWR Illegal Opcode or Uninitialized W Register Access Reset Flag bit

Value	Description
1	An Illegal Opcode, an Illegal Address mode or Uninitialized W Register used as an Address Pointer caused a Reset.
0	An Illegal Opcode or Uninitialized W Register Reset has not occurred.

Bit 9 – CM Configuration Mismatch Flag bit

Value	Description
1	A Configuration Mismatch Reset has occurred.
0	A Configuration Mismatch Reset has not occurred.

Bit 8 – VREGS Voltage Regulator Standby During Sleep bit

Value	Description
1	Voltage regulator is active during Sleep.
0	Voltage regulator goes into Standby mode during Sleep.

Bit 7 – EXTR External Reset ($\overline{\text{MCLR}}$) Pin bit

Value	Description
1	A Master Clear (pin) Reset has occurred.
0	A Master Clear (pin) Reset has not occurred.

Bit 6 – SWR Software `RESET` (Instruction) Flag bit

Value	Description
1	A `RESET` instruction has been executed.
0	A `RESET` instruction has not been executed.

Bit 4 – WDTO Watchdog Timer Time-out Flag bit

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Value	Description
1	WDT time-out has occurred.
0	WDT time-out has not occurred.

Bit 3 – SLEEP Wake-up from Sleep Flag bit

Value	Description
1	Device has been in Sleep mode.
0	Device has not been in Sleep mode.

Bit 2 – IDLE Wake-up from Idle Flag bit

Value	Description
1	Device has been in Idle mode.
0	Device has not been in Idle mode.

Bit 1 – BOR Brown-out Reset Flag bit

Value	Description
1	A Brown-out Reset has occurred.
0	A Brown-out Reset has not occurred.

Bit 0 – POR Power-on Reset Flag bit

Value	Description
1	A Power-on Reset has occurred.
0	A Power-on Reset has not occurred.

6.3. Key Resources

- **"Reset"** (www.microchip.com/DS70000602) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* sections
- Development Tools

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7. Interrupt Controller

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (www.microchip.com/DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The dsPIC33CDVL256MC506 family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33CDVL256MC506 family CPU.

The interrupt controller has the following features:

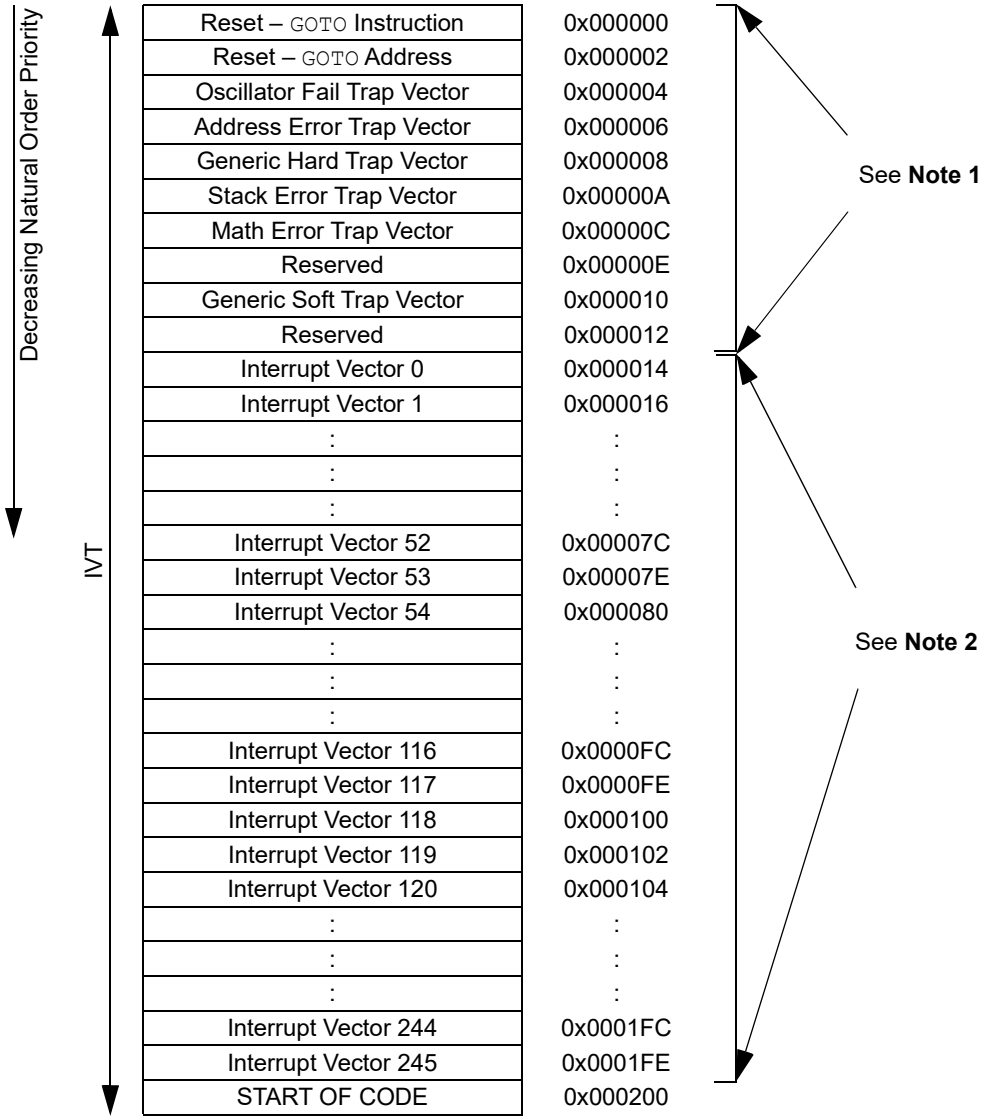
- Six Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Fixed Interrupt Entry and Return Latencies
- Alternate Interrupt Vector Table (AIVT) for Debug Support

7.1. Interrupt Vector Table

The dsPIC33CDVL256MC506 family Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory, starting at location, 000004h. The IVT contains six non-maskable trap vectors and up to 246 sources of interrupts. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

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Figure 7-1. dsPIC33CDVL256MC506 Family Interrupt Vector Table



Notes:

1. See Table 7-1.
2. See Table 7-2.

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

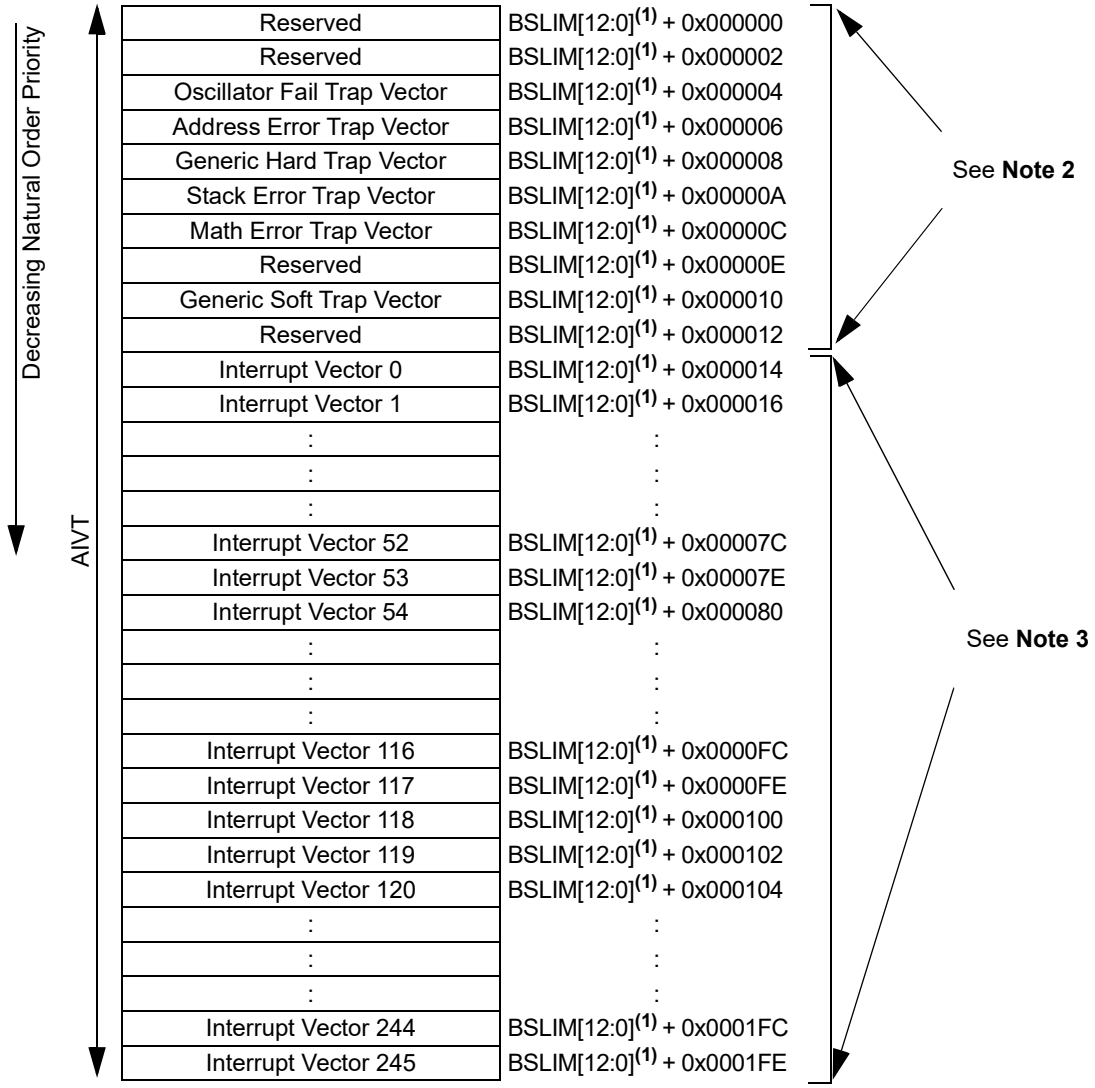
7.2. Alternate Interrupt Vector Table

The Alternate Interrupt Vector Table (AIVT), shown in Figure 7-2, is available only when the Boot Segment (BS) is defined and the AIVT has been enabled. To enable the Alternate Interrupt Vector Table, the Configuration bit, AIVTDIS in the FSEC register, must be programmed and the AIVTEN bit must be set (INTCON2[8] = 1). When the AIVT is enabled, all interrupt and exception processes use the alternate vectors instead of the default vectors. The AIVT begins at the start of the last page of the Boot Segment, defined by BSLIM[12:0]. The second half of the page is no longer usable space. The Boot Segment must be at least two pages to enable the AIVT.

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Note: Although the Boot Segment must be enabled in order to enable the AIVT, application code does not need to be present inside of the Boot Segment. The AIVT (and IVT) will inherit the Boot Segment code protection.

Figure 7-2. dsPIC33CDVL256MC506 Alternate Interrupt Vector Table



Notes:

1. The address depends on the size of the Boot Segment defined by BSLIM[12:0]: [(BSLIM[12:0] – 1) x 0x800] + Offset.
2. See Table 7-1.
3. See Table 7-2.

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7.3. Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33CDVL256MC506 family devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A `GOTO` instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a `RESET` instruction.

Table 7-1. Trap Vector Details

Trap Description	MPLAB® XC16 Trap ISR Name	IVT Address	Trap Bit Location			Priority
			Interrupt Flag	Type	Enable	
Oscillator Failure	_OscillatorFail	0x000004	INTCON1[1]	—	—	15
Address Error	_AddressError	0x000006	INTCON1[3]	—	—	14
ECC Double-Bit Error	_HardTrapError	0x000008	INTCON4[1]	—	—	13
Software Generated Trap	_HardTrapError	0x000008	INTCON4[0]	—	INTCON2[13]	13
Stack Error	_StackError	0x00000A	INTCON1[2]	—	—	12
Overflow Accumulator A	_MathError	0x00000C	INTCON1[4]	INTCON1[14]	INTCON1[10]	11
Overflow Accumulator B	_MathError	0x00000C	INTCON1[4]	INTCON1[13]	INTCON1[9]	11
Catastrophic Overflow Accumulator A	_MathError	0x00000C	INTCON1[4]	INTCON1[12]	INTCON1[8]	11
Catastrophic Overflow Accumulator B	_MathError	0x00000C	INTCON1[4]	INTCON1[11]	INTCON1[8]	11
Shift Accumulator Error	_MathError	0x00000C	INTCON1[4]	INTCON1[7]	INTCON1[8]	11
Divide-by-Zero Error	_MathError	0x00000C	INTCON1[4]	INTCON1[6]	INTCON1[8]	11
Reserved	_Reserved	0x00000E	—	—	—	—
CAN Address Error	_SoftTrapError	0x000010	INTCON3[9]	—	—	9
NVM Address Error	_SoftTrapError	0x000010	INTCON3[8]	—	—	9
`DO` Stack Overflow	_SoftTrapError	0x000010	INTCON3[4]	—	—	9
Reserved	Reserved	0x000012	—	—	—	—

Table 7-2. Interrupt Vector Details

Interrupt Source	MPLAB® XC16 ISR Name	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
					Flag	Enable	Priority
External Interrupt 0	_INT0Interrupt	8	0	0x000014	IFS0[0]	IEC0[0]	IPC0[2:0]

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Table 7-2. Interrupt Vector Details (continued)

Interrupt Source	MPLAB® XC16 ISR Name	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
					Flag	Enable	Priority
Timer1	_T1Interrupt	9	1	0x000016	IFS0[1]	IEC0[1]	IPC0[6:4]
Change Notice Interrupt A	_CNAInterrupt	10	2	0x000018	IFS0[2]	IEC0[2]	IPC0[10:8]
Change Notice Interrupt B	_CNBInterrupt	11	3	0x00001A	IFS0[3]	IEC0[3]	IPC0[14:12]
DMA Channel 0	_DMA0Interrupt	12	4	0x00001C	IFS0[4]	IEC0[4]	IPC1[2:0]
Reserved	Reserved	13	5	0x00001E	—	—	—
Input Capture/ Output Compare 1	_CCP1Interrupt	14	6	0x000020	IFS0[6]	IEC0[6]	IPC1[10:8]
CCP1 Timer	_CCT1Interrupt	15	7	0x000022	IFS0[7]	IEC0[7]	IPC1[14:12]
DMA Channel 1	_DMA1Interrupt	16	8	0x000024	IFS0[8]	IEC0[8]	IPC2[2:0]
SPI1 Receiver	_SPI1RXInterrupt	17	9	0x000026	IFS0[9]	IEC0[9]	IPC2[6:4]
SPI1 Transmitter	_SPI1TXInterrupt	18	10	0x000028	IFS0[10]	IEC0[10]	IPC2[10:8]
UART1 Receiver	_U1RXInterrupt	19	11	0x00002A	IFS0[11]	IEC0[11]	IPC2[14:12]
UART1 Transmitter	_U1TXInterrupt	20	12	0x00002C	IFS0[12]	IEC0[12]	IPC3[2:0]
ECC Single Bit Error	_ECCSBEInterrupt	21	13	0x00002E	IFS0[13]	IEC0[13]	IPC3[6:4]
NVM Write Complete	_NVMInterrupt	22	14	0x000030	IFS0[14]	IEC0[14]	IPC3[10:8]
External Interrupt 1	_INT1Interrupt	23	15	0x000032	IFS0[15]	IEC0[15]	IPC3[14:12]
I2C1 Slave Event	_SI2C1Interrupt	24	16	0x000034	IFS1[0]	IEC1[0]	IPC4[2:0]
I2C1 Master Event	_MI2C1Interrupt	25	17	0x000036	IFS1[1]	IEC1[1]	IPC4[6:4]
DMA Channel 2	_DMA2Interrupt	26	18	0x000038	IFS1[2]	IEC1[2]	IPC4[10:8]
Change Notice Interrupt C(1)	_CNCInterrupt	27	19	0x00003A	IFS1[3]	IEC1[3]	IPC4[14:12]
External Interrupt 2	_INT2Interrupt	28	20	0x00003C	IFS1[4]	IEC1[4]	IPC5[2:0]
DMA Channel 3	_DMA3Interrupt	29	21	0x00003E	IFS1[5]	IEC1[5]	IPC5[6:4]
Reserved	Reserved	30	22	0x000040	—	—	—
Input Capture/ Output Compare 2	_CCP2Interrupt	31	23	0x000042	IFS1[7]	IEC1[7]	IPC5[14:12]
CCP2 Timer	_CCT2Interrupt	32	24	0x000044	IFS1[8]	IEC1[8]	IPC6[2:0]

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Table 7-2. Interrupt Vector Details (continued)

Interrupt Source	MPLAB® XC16 ISR Name	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
					Flag	Enable	Priority
CAN1 Combined Error(2)	_CANInterrupt	33	25	0x000046	IFS1[9]	IEC1[9]	IPC6[6:4]
External Interrupt 3	_INT3Interrupt	34	26	0x000048	IFS1[10]	IEC1[10]	IPC6[10:8]
U2RX – UART2 Receiver	_U2RXInterrupt	35	27	0x00004A	IFS1[11]	IEC1[11]	IPC6[14:12]
U2TX – UART2 Transmitter	_U2TXInterrupt	36	28	0x00004C	IFS1[12]	IEC1[12]	IPC7[2:0]
SPI2 Receiver	_SPI2RXInterrupt	37	29	0x00004E	IFS1[13]	IEC1[13]	IPC7[6:4]
SPI2 Transmitter	_SPI2TXInterrupt	38	30	0x000050	IFS1[14]	IEC1[14]	IPC7[10:8]
CAN1 RX Data Ready(2)	_C1RXInterrupt	39	31	0x000052	IFS1[15]	IEC1[15]	IPC7[14:12]
Reserved	Reserved	40-42	32-34	0x000054-0x000058	—	—	—
Input Capture/ Output Compare 3	_CCP3Interrupt	43	35	0x00005A	IFS2[3]	IEC2[3]	IPC8[14:12]
CCP3 Timer	_CCT3Interrupt	44	36	0x00005C	IFS2[4]	IEC2[4]	IPC9[2:0]
Reserved	Reserved	45-47	37-39	0x00005E-0x000062	—	—	—
Input Capture/ Output Compare 4	_CCP4Interrupt	48	40	0x000064	IFS2[8]	IEC2[8]	IPC10[2:0]
CCP4 Timer	_CCT4Interrupt	49	41	0x000066	IFS2[9]	IEC2[9]	IPC10[6:4]
Reserved	Reserved	50-52	42-44	0x000068-0x00006C	—	—	—
Deadman Timer	_DMTInterrupt	53	45	0x00006E	IFS2[13]	IEC2[13]	IPC11[6:4]
Reserved	Reserved	54-55	46-47	0x000070-0x000072	—	—	—
QEI Position Counter Compare	_QEI1Interrupt	56	48	0x000074	IFS3[0]	IEC3[0]	IPC12[2:0]
UART1 Error	_U1EInterrupt	57	49	0x000076	IFS3[1]	IEC3[1]	IPC12[6:4]
UART2 Error	_U2EInterrupt	58	50	0x000078	IFS3[2]	IEC3[2]	IPC12[10:8]
CRC Generator	_CRCInterrupt	59	51	0x00007A	IFS3[3]	IEC3[3]	IPC12[14:12]
CAN1 TX Data Request(2)	_C1TXInterrupt	60	52	0x00007C	IFS3[4]	IEC3[4]	IPC13[2:0]
Reserved	Reserved	61-63	53-55	0x00007E-0x000082	—	—	—
UART3 Error	_U3EInterrupt	64	56	0x000084	IFS3[8]	IEC3[8]	IPC14[2:0]
UART3 Receiver	_U3RXInterrupt	65	57	0x000086	IFS3[9]	IEC3[9]	IPC14[6:4]

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Table 7-2. Interrupt Vector Details (continued)

Interrupt Source	MPLAB® XC16 ISR Name	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
					Flag	Enable	Priority
UART3 Transmitter	_U3TXInterrupt	66	58	0x000088	IFS3[10]	IEC3[10]	IPC14[10:8]
Reserved	Reserved	67-68	59-60	0x00008A-0x00008C	—	—	—
In-Circuit Debugger	_ICDInterrupt	69	61	0x00008E	IFS3[13]	IEC3[13]	IPC15[6:4]
Reserved	Reserved	70	62	0x000090	—	—	—
PTG Step	_PTGSTEPInterrupt	71	63	0x000092	IFS3[15]	IEC3[15]	IPC15[14:12]
I2C1 Bus Collision	_I2C1BCInterrupt	72	64	0x000094	IFS4[0]	IEC4[0]	IPC16[2:0]
Reserved	Reserved	73-74	65-66	0x000096-0x000098	—	—	—
PWM Generator 1	_PWM1Interrupt	75	67	0x00009A	IFS4[3]	IEC4[3]	IPC16[14:12]
PWM Generator 2	_PWM2Interrupt	76	68	0x00009C	IFS4[4]	IEC4[4]	IPC17[2:0]
PWM Generator 3	_PWM3Interrupt	77	69	0x00009E	IFS4[5]	IEC4[5]	IPC17[6:4]
PWM Generator 4	_PWM4Interrupt	78	70	0x0000A0	IFS4[6]	IEC4[6]	IPC17[10:8]
Reserved	Reserved	79-82	71-74	0x0000A2-0x0000A8	—	—	—
Change Notice D(1)	_CNDInterrupt	83	75	0x0000AA	IFS4[11]	IEC4[11]	IPC18[14:12]
Reserved	Reserved	84	76	0x0000AC	—	—	—
Comparator 1	_CMP1Interrupt	85	77	0x0000AE	IFS4[13]	IEC4[13]	IPC19[6:4]
Comparator 2	_CMP2Interrupt	86	78	0x0000B0	IFS4[14]	IEC4[14]	IPC19[10:8]
Reserved	Reserved	87-88	79-80	0x0000B2-0x0000B4	—	—	—
PTG Watchdog Timer Time-out	_PTGWDTInterrupt	89	81	0x0000B6	IFS5[1]	IEC5[1]	IPC20[6:4]
PTG Trigger 0	_PTG0Interrupt	90	82	0x0000B8	IFS5[2]	IEC5[2]	IPC20[10:8]
PTG Trigger 1	_PTG1Interrupt	91	83	0x0000BA	IFS5[3]	IEC5[3]	IPC20[14:12]
PTG Trigger 2	_PTG2Interrupt	92	84	0x0000BC	IFS5[4]	IEC5[4]	IPC21[2:0]
PTG Trigger 3	_PTG3Interrupt	93	85	0x0000BE	IFS5[5]	IEC5[6]	IPC21[6:4]
SENT1 TX/RX	_SENT1Interrupt	94	86	0x0000C0	IFS5[6]	IEC5[6]	IPC21[10:8]
SENT1 Error	_SENT1EInterrupt	95	87	0x0000C2	IFS5[7]	IEC5[7]	IPC21[14:12]
Reserved	Reserved	96-97	88-89	0x0000C4-0x0000C6	—	—	—
ADC Global Interrupt	_ADCInterrupt	98	90	0x0000C8	IFS5[10]	IEC5[10]	IPC22[10:8]
ADC AN0 Interrupt	_ADCAN0Interrupt	99	91	0x0000CA	IFS5[11]	IEC5[11]	IPC22[14:12]
ADC AN1 Interrupt	_ADCAN1Interrupt	100	92	0x0000CC	IFS5[12]	IEC5[12]	IPC23[2:0]

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Table 7-2. Interrupt Vector Details (continued)

Interrupt Source	MPLAB® XC16 ISR Name	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
					Flag	Enable	Priority
ADC AN2 Interrupt	_ADCAN2Interrupt	101	93	0x0000CE	IFS5[13]	IEC5[13]	IPC23[6:4]
ADC AN3 Interrupt	_ADCAN3Interrupt	102	94	0x0000D0	IFS5[14]	IEC5[14]	IPC23[10:8]
ADC AN4 Interrupt	_ADCAN4Interrupt	103	95	0x0000D2	IFS5[15]	IEC5[15]	IPC23[14:12]
ADC AN5 Interrupt	_ADCAN5Interrupt	104	96	0x0000D4	IFS6[0]	IEC6[0]	IPC24[2:0]
ADC AN6 Interrupt	_ADCAN6Interrupt	105	97	0x0000D6	IFS6[1]	IEC6[1]	IPC24[6:4]
ADC AN7 Interrupt(3)	_ADCAN7Interrupt	106	98	0x0000D8	IFS6[2]	IEC6[2]	IPC24[10:8]
ADC AN8 Interrupt	_ADCAN8Interrupt	107	99	0x0000DA	IFS6[3]	IEC6[3]	IPC24[14:12]
ADC AN9 Interrupt	_ADCAN9Interrupt	108	100	0x0000DC	IFS6[4]	IEC6[4]	IPC25[2:0]
ADC AN10 Interrupt	_ADCAN10Interrupt	109	101	0x0000DE	IFS6[5]	IEC6[5]	IPC25[6:4]
ADC AN11 Interrupt	_ADCAN11Interrupt	110	102	0x0000E0	IFS6[6]	IEC6[6]	IPC25[10:8]
ADC AN12 Interrupt(3)	_ADCAN12Interrupt	111	103	0x0000E2	IFS6[7]	IEC6[7]	IPC25[14:12]
ADC AN13 Interrupt(3)	_ADCAN13Interrupt	112	104	0x0000E4	IFS6[8]	IEC6[8]	IPC26[2:0]
ADC AN14 Interrupt(3)	_ADCAN14Interrupt	113	105	0x0000E6	IFS6[9]	IEC6[9]	IPC26[6:4]
ADC AN15 Interrupt(3)	_ADCAN15Interrupt	114	106	0x0000E8	IFS6[10]	IEC6[10]	IPC26[10:8]
ADC AN16 Interrupt	_ADCAN16Interrupt	115	107	0x0000EA	IFS6[11]	IEC6[11]	IPC26[14:12]
ADC AN17 Interrupt	_ADCAN17Interrupt	116	108	0x0000EC	IFS6[12]	IEC6[12]	IPC27[2:0]
ADC AN18 Interrupt(3)	_ADCAN18Interrupt	117	109	0x0000EE	IFS6[13]	IEC6[13]	IPC27[6:4]
ADC AN19 Interrupt(3)	_ADCAN19Interrupt	118	110	0x0000F0	IFS6[14]	IEC6[14]	IPC27[10:8]
ADC AN20 Interrupt	_ADCAN20Interrupt	119	111	0x0000F2	IFS6[15]	IEC6[15]	IPC27[14:12]
ADC AN21 Interrupt	_ADCAN21Interrupt	120	112	0x0000F4	IFS7[0]	IEC7[0]	IPC28[2:0]
Reserved	Reserved	121-123	113-115	0x0000F6-0x000FA	—	—	—
ADC Digital Comparator 0	_ADCMP0Interrupt	124	116	0x0000FC	IFS7[4]	IEC7[4]	IPC29[2:0]
ADC Digital Comparator 1	_ADCMP1Interrupt	125	117	0x0000FE	IFS7[5]	IEC7[5]	IPC29[6:4]
ADC Digital Comparator 2	_ADCMP2Interrupt	126	118	0x000100	IFS7[6]	IEC7[6]	IPC29[10:8]

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Table 7-2. Interrupt Vector Details (continued)

Interrupt Source	MPLAB® XC16 ISR Name	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
					Flag	Enable	Priority
ADC Digital Comparator 3	_ADCMP3Interrupt	127	119	0x000102	IFS7[7]	IEC7[7]	IPC29[14:12]
ADC Oversample Filter 0	_ADFLTR0Interrupt	128	120	0x000104	IFS7[8]	IEC7[8]	IPC30[2:0]
ADC Oversample Filter 1	_ADFLTR1Interrupt	129	121	0x000106	IFS7[9]	IEC7[9]	IPC30[6:4]
ADC Oversample Filter 2	_ADFLTR2Interrupt	130	122	0x000108	IFS7[10]	IEC7[10]	IPC30[10:8]
ADC Oversample Filter 3	_ADFLTR3Interrupt	131	123	0x00010A	IFS7[11]	IEC7[11]	IPC30[14:12]
CLC1 Positive Edge	_CLC1PInterrupt	132	124	0x00010C	IFS7[12]	IEC7[12]	IPC31[2:0]
CLC2 Positive Edge	_CLC2PInterrupt	133	125	0x00010E	IFS7[13]	IEC7[13]	IPC31[6:4]
SPI1 Error	_SPI1Interrupt	134	126	0x000110	IFS7[14]	IEC7[14]	IPC31[10:8]
SPI2 Error	_SPI2Interrupt	135	127	0x000112	IFS7[15]	IEC7[15]	IPC31[14:12]
Reserved	Reserved	136-176	128-168	0x000114-0x000164	—	—	—
PWM Event A	_PEVTAInterrupt	177	169	0x000166	IFS10[9]	IEC10[9]	IPC42[6:4]
PWM Event B	_PEVTBInterrupt	178	170	0x000168	IFS10[10]	IEC10[10]	IPC42[10:8]
PWM Event C	_PEVTCInterrupt	179	171	0x00016A	IFS10[11]	IEC10[11]	IPC42[14:12]
PWM Event D	_PEVTDInterrupt	180	172	0x00016C	IFS10[12]	IEC10[12]	IPC43[2:0]
PWM Event E	_PEVTEInterrupt	181	173	0x00016E	IFS10[13]	IEC10[13]	IPC43[6:4]
PWM Event F	_PEVTFInterrupt	182	174	0x000170	IFS10[14]	IEC10[14]	IPC43[10:8]
CLC3 Positive Edge	_CLC3PInterrupt	183	175	0x000172	IFS10[15]	IEC10[15]	IPC43[14:12]
CLC4 Positive Edge	_CLC4PInterrupt	184	176	0x000174	IFS11[0]	IEC11[0]	IPC44[2:0]
CLC1 Negative Edge	_CLC1NInterrupt	185	177	0x000176	IFS11[1]	IEC11[1]	IPC44[6:4]
CLC2 Negative Edge	_CLC2NInterrupt	186	178	0x000178	IFS11[2]	IEC11[2]	IPC44[10:8]
CLC3 Negative Edge	_CLC3NInterrupt	187	179	0x00017A	IFS11[3]	IEC11[3]	IPC44[14:]12]
CLC4 Negative Edge	_CLC4NInterrupt	188	180	0x00017C	IFS11[4]	IEC11[4]	IPC45[2:0]
Reserved	Reserved	189-196	181-188	0x0017E-0x0018C	—	—	—
UART1 Event	_U1EVTInterrupt	197	189	0x00018E	IFS11[13]	IF2C11[13]	IPC47[6:4]
UART2 Event	_U2EVTInterrupt	198	190	0x000190	IFS11[14]	IF2C11[14]	IPC47[12:8]
UART3 Event	_U3EVTInterrupt	199	191	0x000192	IFS11[15]	IF2C11[15]	IPC47[14:12]

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Table 7-2. Interrupt Vector Details (continued)

Interrupt Source	MPLAB® XC16 ISR Name	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
					Flag	Enable	Priority
Reserved	Reserved	200-255	192-247	0x000194-0x0001FE	—	—	—

Note:

1. Availability dependent on supported I/O ports. Refer to Table 8-2 for availability on device variants.
2. Availability dependent on supported peripherals, refer to Table 1.
3. Availability dependent on number of supported ADC channels. Refer to Table 1 for ADC channel availability on device variants.

7.4. Interrupt Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page contains the latest updates and additional information.

7.4.1. Key Resources

- **"Interrupts"** (www.microchip.com/DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

7.5. Interrupt Control and Status Registers

The dsPIC33CDVL256MC506 family devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- INTTREG

7.6. INTCON1 through INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS), as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior, contains the Global Interrupt Enable bit (GIE) and the Alternate Interrupt Vector Table Enable bit (AIVTEN).

INTCON3 contains the status flags for the Auxiliary PLL and DO stack overflow status trap sources.

The INTCON4 register contains the Software Generated Hard Trap Status bit (SGHT).

7.6.1. IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

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7.6.2. IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.6.3. IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of seven priority levels.

7.6.4. INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number (VECNUM[7:0]) and Interrupt Level bits (ILR[3:0]) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 7-2. For example, INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0[0], the INT0IE bit in IEC0[0] and the INT0IP[2:0] bits in the first position of IPC0 (IPC0[2:0]).

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7.7. Status/Control Registers

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers, refer to **"Enhanced CPU"** (www.microchip.com/DS70005158) in the *"dsPIC33/PIC24 Family Reference Manual"*.

- The CPU STATUS Register, SR, contains the IPL[2:0] bits (SR[7:5]). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit, which together with IPL[2:0], also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0800	IFS0	15:8	INT1IF	NVMIF	ECCSBEIF	U1TXIF	U1RXIF	SPI1TXIF	SPI1RXIF	DMA1IF
		7:0	CCT1IF	CCP1IF		DMA0IF	CNBIF	CNAIF	T1IF	INT0IF
0x0802	IFS1	15:8	C1RXIF	SPI2TXIF	SPI2RXIF	U2TXIF	U2RXIF	INT3IF	C1IF	CCP2IF
		7:0	CCP2IF		DMA3IF	INT2IF	CNCIF	DMA2IF	MI2C1IF	SI2C1IF
0x0804	IFS2	15:8			DMTIF				CCT4IF	CCP4IF
		7:0				CCT3IF	CCP3IF			
0x0806	IFS3	15:8	PTGSTEPIF		ICDIF			U3TXIF	U3RXIF	U3EIF
		7:0				C1TXIF	CRCIF	U2EIF	U1EIF	QEI1IF
0x0808	IFS4	15:8		CMP2IF	CMP1IF		CNDIF			
		7:0		PWM4IF	PWM3IF	PWM2IF	PWM1IF			I2C1BCIF
0x080A	IFS5	15:8	AD1AN4IF	AD1AN3IF	AD1AN2IF	AD1AN1IF	AD1AN0IF	ADCIF		
		7:0	SENT1EIF	SENT1IF	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	
0x080C	IFS6	15:8	AD1AN20IF	AD1AN19IF	AD1AN18IF	AD1AN17IF	AD1AN16IF	AD1AN15IF	AD1AN14IF	AD1AN13IF
		7:0	AD1AN12IF	AD1AN11IF	AD1AN10IF	AD1AN9IF	AD1AN8IF	AD1AN7IF	AD1AN6IF	AD1AN5IF
0x080E	IFS7	15:8	SPI2IF	SPI1IF	CLC2PIF	CLC1PIF	ADFLTR3IF	ADFLTR2IF	ADFLTR1IF	ADFLTR0F
		7:0	ADCMP3IF	ADCMP2IF	ADCMP1IF	ADCMP0IF	ADFLTIF			AD1AN21IF
0x0810 ... 0x0813	Reserved									
0x0814	IFS10	15:8	CLC3PIF	PEVTFIF	PEVTEIF	PEVTDIF	PEVTCIF	PEVTBIF	PEVTAIF	
		7:0								
0x0816	IFS11	15:8	U3EVTIF	U2EVTIF	U1EVTIF					
		7:0				CLC4NIF	CLC3NIF	CLC2NIF	CLC1NIF	CLC4PIF
0x0818 ... 0x081F	Reserved									
0x0820	IEC0	15:8	INT1IE	NVMIE	ECCSBEIE	U1TXIE	U1RXIE	SPI1TXIE	SPI1RXIE	DMA1IE
		7:0	CCT1IE	CCP1IE		DMA0IE	CNBIE	CNAIE	T1IE	INT0IE
0x0822	IEC1	15:8	C1RXIE	SPI2TXIE	SPI2RXIE	U2TXIE	U2RXIE	INT3IE	C1IE	CCT2IE
		7:0	CCP2IE		DMA3IE	INT2IE	CNCIE	DMA2IE	MI2C1IE	SI2C1IE
0x0824	IEC2	15:8			DMTIE				CCT4IE	CCP4IE
		7:0				CCT3IE	CCP3IE			
0x0826	IEC3	15:8	PTGSTEPIE		ICDIE			U3TXIE	U3RXIE	U3EIE
		7:0				C1TXIE	CRCIE	U2EIE	U1EIE	QEI1IE
0x0828	IEC4	15:8		CMP2IE	CMP1IE		CNDIE			
		7:0		PWM4IE	PWM3IE	PWM2IE	PWM1IE			I2C1BCIE
0x082A	IEC5	15:8	AD1AN4IE	AD1AN3IE	AD1AN2IE	AD1AN1IE	AD1AN0IE	ADCIE		
		7:0	SENT1EIE	SENT1IE	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	
0x082C	IEC6	15:8	AD1AN20IE	AD1AN19IE	AD1AN18IE	AD1AN17IE	AD1AN16IE	AD1AN15IE	AD1AN14IE	AD1AN13IE
		7:0	AD1AN12IE	AD1AN11IE	AD1AN10IE	AD1AN9IE	AD1AN8IE	AD1AN7IE	AD1AN6IE	AD1AN5IE
0x082E	IEC7	15:8	SPI2GIE	SPI1GIE	CLC2PIE	CLC1PIE	ADFLTR3IE	ADFLTR2IE	ADFLTR1IE	ADFLTR0IE
		7:0	ADCMP3IE	ADCMP2IE	ADCMP1IE	ADCMP0IE	ADFLTIE			AD1AN21IE
0x0830 ... 0x0833	Reserved									

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Status/Control Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0834	IEC10	15:8	CLC3PIE	PEVTFIE	PEVTEIE	PEVTDIE	PEVTCIE	PEVTBIE	PEVTAIE	
		7:0								
0x0836	IEC11	15:8	U3ENTIE	U2ENTIE	U1ENTIE					
		7:0				CLC4NIE	CLC3NIE	CLC2NIE	CLC1NIE	CLC4PIE
0x0838 ... 0x083F	Reserved									
0x0840	IPC0	15:8		CNBIP[2:0]				CNAIP[2:0]		
		7:0		T1IP[2:0]				INT0IP[2:0]		
0x0842	IPC1	15:8		CCT1IP[2:0]				CCP1IP[2:0]		
		7:0						DMA0IP[2:0]		
0x0844	IPC2	15:8		U1RXIP[2:0]				SPI1TXIP[2:0]		
		7:0		SPI1RXIP[2:0]				DMA1IP[2:0]		
0x0846	IPC3	15:8		INT1IP[2:0]				NVMIP[2:0]		
		7:0		ECCSBIP[2:0]				U1TXIP[2:0]		
0x0848	IPC4	15:8		CNCIP[2:0]				DMA2IP[2:0]		
		7:0		MI2C1IP[2:0]				SI2C1IP[2:0]		
0x084A	IPC5	15:8		CCP2IP[2:0]						
		7:0		DMA3IP[6:4]				INT2IP[2:0]		
0x084C	IPC6	15:8		U2RXIP[2:0]				INT3IP[2:0]		
		7:0						CCT2IP[2:0]		
0x084E	IPC7	15:8		C1RXIP[2:0]				SPI2TXIP[2:0]		
		7:0		SPI2RXIP[2:0]				U2TXIP[2:0]		
0x0850	IPC8	15:8		CCP3IP[2:0]						
		7:0								
0x0852	IPC9	15:8								
		7:0						CCT3IP[2:0]		
0x0854	IPC10	15:8								
		7:0		CCT4IP[2:0]				CCP4IP[2:0]		
0x0856	IPC11	15:8								
		7:0		DMTIP[2:0]						
0x0858	IPC12	15:8		CRCIP[2:0]				U2EIP[2:0]		
		7:0		U1EIP[2:0]				QEI1IP[2:0]		
0x085A	IPC13	15:8								
		7:0						C1TXIP[2:0]		
0x085C	IPC14	15:8						U3TXIP[2:0]		
		7:0		U3RXIP[2:0]				U3EIP[2:0]		
0x085E	IPC15	15:8		PTGSTEPIP[2:0]						
		7:0		ICDIP[2:0]						
0x0860	IPC16	15:8		PWM1IP[2:0]						
		7:0						I2C1BCIP[2:0]		
0x0862	IPC17	15:8						PWM4IP[2:0]		
		7:0		PWM3IP[2:0]				PWM2IP[2:0]		
0x0864	IPC18	15:8		CNDIP[2:0]						
		7:0								
0x0866	IPC19	15:8						CMP2IP[2:0]		
		7:0		CMP1IP[2:0]						
0x0868	IPC20	15:8		PTG1IP[2:0]				PTG0IP[2:0]		
		7:0		PTGWDTIP[2:0]						
0x086A	IPC21	15:8		SENT1EIP[2:0]				SENT1IP[2:0]		
		7:0		PTG3IP[2:0]				PTG2IP[2:0]		
0x086C	IPC22	15:8		AD1AN0IP[2:0]				ADCIP[2:0]		
		7:0								
0x086E	IPC23	15:8		AD1AN4IP[2:0]				AD1AN3IP[2:0]		
		7:0		AD1AN2IP[2:0]				ADCAN1IP[2:0]		
0x0870	IPC24	15:8		AD1AN8IP[2:0]				AD1AN7IP[2:0]		
		7:0		AD1AN6IP[2:0]				AD1AN5IP[2:0]		
0x0872	IPC25	15:8		AD1AN12IP[2:0]				AD1AN11IP[2:0]		
		7:0		AD1AN10IP[2:0]				AD1AN9IP[2:0]		

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Status/Control Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0874	IPC26	15:8		AD1AN16IP[2:0]				AD1AN15IP[2:0]		
		7:0		AD1AN14IP[2:0]				AD1AN13IP[2:0]		
0x0876	IPC27	15:8		AD1AN20IP[2:0]				AD1AN19IP[2:0]		
		7:0		AD1AN18IP[2:0]				AD1AN17IP[2:0]		
0x0878	IPC28	15:8								
		7:0						AD1AN21IP[2:0]		
0x087A	IPC29	15:8		ADCMP3IP[2:0]				ADCMP2IP[2:0]		
		7:0		ADCMP1IP[2:0]				ADCMP0IP[2:0]		
0x087C	IPC30	15:8		ADFLTR3IP[2:0]				ADFLTR2IP[2:0]		
		7:0		ADFLTR1IP[2:0]				ADFLTR0IP[2:0]		
0x087E	IPC31	15:8		SPI2IP[2:0]				SPI1IP[2:0]		
		7:0		CLC2PIP[2:0]				CLC1PIP[2:0]		
0x0880 ... 0x0893	Reserved									
0x0894	IPC42	15:8		PEVTCIP[2:0]				PEVTBIP[2:0]		
		7:0		PEVTAIP[2:0]						
0x0896	IPC43	15:8		CLC3PEIP[2:0]				PEVTFIP[2:0]		
		7:0		PEVTEIP[2:0]				PEVTDIP[2:0]		
0x0898	IPC44	15:8		CLC3NEIP[2:0]				CLC2NEIP[2:0]		
		7:0		CLC1NEIP[2:0]				CLC4PEIP[2:0]		
0x089A	IPC45	15:8								
		7:0						CLC4NEIP[2:0]		
0x089C ... 0x089D	Reserved									
0x089E	IPC47	15:8		U3EVTIP[2:0]				U2EVTIP[2:0]		
		7:0		U1EVTIP[2:0]						
0x08A0 ... 0x08BF	Reserved									
0x08C0	INTCON1	15:8	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
		7:0	SFTACERR	DIV0ERR		MATHERR	ADDRERR	STKERR	OSCFAIL	
0x08C2	INTCON2	15:8	GIE	DISI	SWTRAP					AIVTEN
		7:0					INT3EP	INT2EP	INT1EP	INT0EP
0x08C4	INTCON3	15:8							CAN	NAE
		7:0			DAE	DOOVR				
0x08C6	INTCON4	15:8								
		7:0							ECCDBE	SGHT
0x08C8	INTTREG	15:8			VHOLD		ILR[3:0]			
		7:0	VECNUM[7:0]							

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7.7.1. Interrupt Request Flags Register 0

Name: IFS0
Offset: 0x800

Bit	15	14	13	12	11	10	9	8
	INT1IF	NVMIF	ECCSBEIF	U1TXIF	U1RXIF	SPI1TXIF	SPI1RXIF	DMA1IF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CCT1IF	CCP1IF		DMA0IF	CNBIF	CNAIF	T1IF	INT0IF
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 15 – INT1IF External Interrupt 1 bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 14 – NVMIF Nonvolatile Memory Write Complete Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 13 – ECCSBEIF ECC Single bit Error Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 12 – U1TXIF UART1 Transmitter Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 11 – U1RXIF UART1 Receiver Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 10 – SPI1TXIF SPI1 Transfer Done Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 9 – SPI1RXIF SPI1 Receive Done Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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Bit 8 – DMA1IF Direct Memory Access 1 Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 7 – CCT1IF SCCP1 Timer Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 6 – CCP1IF Input Capture/Output Compare 1 Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 4 – DMA0IF Direct Memory Access 0 Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 3 – CNBIF Change Notice Interrupt B bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 2 – CNAIF Change Notice Interrupt A bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 1 – T1IF Timer1 Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 0 – INT0IF External Interrupt 0 bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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7.7.2. Interrupt Request Flags Register 1

Name: IFS1
Offset: 0x802

Bit	15	14	13	12	11	10	9	8
	C1RXIF	SPI2TXIF	SPI2RXIF	U2TXIF	U2RXIF	INT3IF	C1IF	CCP2IF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CCP2IF		DMA3IF	INT2IF	CNCIF	DMA2IF	MI2C1IF	SI2C1IF
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 15 – C1RXIF CAN1 RX Data Ready Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 14 – SPI2TXIF SPI2 Transfer Done Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 13 – SPI2RXIF SPI2 Receiver Done Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 12 – U2TXIF UART2 Transmitter Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 11 – U2RXIF UART2 Receiver Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 10 – INT3IF External Interrupt 3 bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 9 – C1IF CAN1 Combined Error Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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Bit 8 – CCP2IF SCCP2 Timer Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 7 – CCP2IF Input Capture/Output Compare 2 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 5 – DMA3IF Direct Memory Access 3 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 4 – INT2IF External Interrupt 2 bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 3 – CNCIF Change Notice Interrupt C bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 2 – DMA2IF Direct Memory Access 2 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 1 – MI2C1IF I2C1 Host Events Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 0 – SI2C1IF I2C1 Client Events Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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7.7.3. Interrupt Request Flags Register 2

Name: IFS2
Offset: 0x804

Bit	15	14	13	12	11	10	9	8
			DMTIF				CCT4IF	CCP4IF
Access			R/W				R/W	R/W
Reset			0				0	0

Bit	7	6	5	4	3	2	1	0
				CCT3IF	CCP3IF			
Access				R/W	R/W			
Reset				0	0			

Bit 13 – DMTIF Deadman Timer Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 9 – CCT4IF SCCP4 Timer Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 8 – CCP4IF Input Capture/Output Compare 4 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 4 – CCT3IF SCCP3 Timer Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 3 – CCP3IF Capture/Output Compare 3 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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7.7.4. Interrupt Request Flags Register 3

Name: IFS3
Offset: 0x806

Bit	15	14	13	12	11	10	9	8
	PTGSTEPIF		ICDIF			U3TXIF	U3RXIF	U3EIF
Access	R/W		R/W			R/W	R/W	R/W
Reset	0		0			0	0	0

Bit	7	6	5	4	3	2	1	0
				C1TXIF	CRCIF	U2EIF	U1EIF	QEI1IF
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 15 – PTGSTEPIF PTG Step Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 13 – ICDIF In-Circuit Debugger Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 10 – U3TXIF UART3 Transmitter Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 9 – U3RXIF UART3 Receiver Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 8 – U3EIF UART3 Error Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 4 – C1TXIF CAN1 TX Data Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 3 – CRCIF Cyclic Redundancy Check Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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Bit 2 – U2EIF UART2 Error Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 1 – U1EIF UART1 Error Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 0 – QEI1IF QEI1 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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7.7.5. Interrupt Request Flags Register 4

Name: IFS4
Offset: 0x808

Bit	15	14	13	12	11	10	9	8
		CMP2IF	CMP1IF		CNDIF			
Access		R/W	R/W		R/W			
Reset		0	0		0			

Bit	7	6	5	4	3	2	1	0
		PWM4IF	PWM3IF	PWM2IF	PWM1IF			I2C1BCIF
Access		R/W	R/W	R/W	R/W			R/W
Reset		0	0	0	0			0

Bit 14 – CMP2IF Comparator 2 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 13 – CMP1IF Comparator 1 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 11 – CNDIF Change Notification D Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 6 – PWM4IF PWM Channel 4 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 5 – PWM3IF PWM Channel 3 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 4 – PWM2IF PWM Channel 2 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 3 – PWM1IF PWM Channel 1 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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Bit 0 – I2C1BCIF I2C1 Bus Collision Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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7.7.6. Interrupt Request Flags Register 5

Name: IFS5
Offset: 0x80A

Bit	15	14	13	12	11	10	9	8
	AD1AN4IF	AD1AN3IF	AD1AN2IF	AD1AN1IF	AD1AN0IF	ADCIF		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
	SENT1EIF	SENT1IF	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 15 – AD1AN4IF ADC AN4 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 14 – AD1AN3IF ADC AN3 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 13 – AD1AN2IF ADC AN2 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 12 – AD1AN1IF ADC AN1 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 11 – AD1AN0IF ADC AN0 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 10 – ADCIF ADC Global Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 7 – SENT1EIF SENT1 External Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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Bit 6 – SENT1IF SENT1 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 5 – PTG3IF PTG3 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 4 – PTG2IF PTG2 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 3 – PTG1IF PTG1 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 2 – PTG0IF PTG0 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 1 – PTGWDTIF PTG Watchdog Timer Time-out Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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7.7.7. Interrupt Request Flags Register 6

Name: IFS6
Offset: 0x80C

Bit	15	14	13	12	11	10	9	8
	AD1AN20IF	AD1AN19IF	AD1AN18IF	AD1AN17IF	AD1AN16IF	AD1AN15IF	AD1AN14IF	AD1AN13IF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	AD1AN12IF	AD1AN11IF	AD1AN10IF	AD1AN9IF	AD1AN8IF	AD1AN7IF	AD1AN6IF	AD1AN5IF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – AD1AN20IF ADC AN20 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 14 – AD1AN19IF ADC AN19 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 13 – AD1AN18IF ADC AN18 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 12 – AD1AN17IF ADC AN17 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 11 – AD1AN16IF ADC AN16 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 10 – AD1AN15IF ADC AN15 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 9 – AD1AN14IF ADC AN14 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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Bit 8 – AD1AN13IF ADC AN13 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 7 – AD1AN12IF ADC AN12 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 6 – AD1AN11IF ADC AN11 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 5 – AD1AN10IF ADC AN10 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 4 – AD1AN9IF ADC AN9 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 3 – AD1AN8IF ADC AN8 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 2 – AD1AN7IF ADC AN7 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 1 – AD1AN6IF ADC AN6 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 0 – AD1AN5IF ADC AN5 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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7.7.8. Interrupt Request Flags Register 7

Name: IFS7
Offset: 0x80E

Bit	15	14	13	12	11	10	9	8
	SPI2IF	SPI1IF	CLC2PIF	CLC1PIF	ADFLTR3IF	ADFLTR2IF	ADFLTR1IF	ADFLTR0F
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADCMP3IF	ADCMP2IF	ADCMP1IF	ADCMP0IF	ADFLTIF			AD1AN21IF
Access	R/W	R/W	R/W	R/W	R/W			R/W
Reset	0	0	0	0	0			0

Bit 15 – SPI2IF SPI2 General Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 14 – SPI1IF SPI1 General Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 13 – CLC2PIF CLC2 Positive Edge Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 12 – CLC1PIF CLC1 Positive Edge Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 11 – ADFLTR3IF ADC Oversample Filter 3 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 10 – ADFLTR2IF ADC Oversample Filter 2 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 9 – ADFLTR1IF ADC Oversample Filter 1 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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Bit 8 – ADFLTR0F ADC Oversample Filter 0 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 7 – ADCMP3IF ADC Digital Comparator 3 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 6 – ADCMP2IF ADC Digital Comparator 2 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 5 – ADCMP1IF ADC Digital Comparator 1 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 4 – ADCMP0IF ADC Digital Comparator 0 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 3 – ADFLTIF ADC Fault Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 0 – AD1AN21IF ADC AN21 Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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7.7.9. Interrupt Request Flags Register 10

Name: IFS10
Offset: 0x814

Bit	15	14	13	12	11	10	9	8
	CLC3PIF	PEVTFIF	PEVTEIF	PEVTDIF	PEVTCIF	PEVTBIF	PEVTAIF	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – CLC3PIF CLC3 Positive Edge Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 14 – PEVTFIF PWM Event F Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 13 – PEVTEIF PWM Event E Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 12 – PEVTDIF PWM Event D Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 11 – PEVTCIF PWM Event C Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 10 – PEVTBIF PWM Event B Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 9 – PEVTAIF PWM Event A Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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7.7.10. Interrupt Request Flags Register 11

Name: IFS11
Offset: 0x816

Bit	15	14	13	12	11	10	9	8
	U3EVTIF	U2EVTIF	U1EVTIF					
Access	R/W	R/W	R/W					
Reset	0	0	0					

Bit	7	6	5	4	3	2	1	0
				CLC4NIF	CLC3NIF	CLC2NIF	CLC1NIF	CLC4PIF
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 15 – U3EVTIF UART3 Event Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 14 – U2EVTIF UART2 Event Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 13 – U1EVTIF UART1 Event Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 4 – CLC4NIF CLC4 Negative Edge Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 3 – CLC3NIF CLC3 Negative Edge Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 2 – CLC2NIF CLC2 Negative Edge Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

Bit 1 – CLC1NIF CLC1 Negative Edge Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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Bit 0 – CLC4PIF CLC4 Positive Edge Interrupt bit

Value	Description
1	Interrupt has occurred.
0	Interrupt has not occurred.

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7.7.11. Interrupt Enable Register 0

Name: IEC0
Offset: 0x820

Bit	15	14	13	12	11	10	9	8
	INT1IE	NVMIE	ECCSBEIE	U1TXIE	U1RXIE	SPI1TXIE	SPI1RXIE	DMA1IE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CCT1IE	CCP1IE		DMA0IE	CNBIE	CNAIE	T1IE	INT0IE
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 15 – INT1IE External Interrupt 1 Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 14 – NVMIE NVM Program/Erase Complete Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 13 – ECCSBEIE ECC Single Bit Error Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 12 – U1TXIE UART1 Transmitter Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 11 – U1RXIE UART1 Receiver Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 10 – SPI1TXIE SPI1 Transfer Done Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 9 – SPI1RXIE SPI1 Receive Done Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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Bit 8 – DMA1IE Direct Memory Access 1 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 7 – CCT1IE SCCP1 Timer Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 6 – CCP1IE Input Capture/Output Compare 1 Interrupt

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 4 – DMA0IE Direct Memory Access 0 Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 3 – CNBIE Change Notice B Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 2 – CNAIE Change Notice A Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 1 – T1IE Timer1 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 0 – INT0IE External Interrupt 0 Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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7.7.12. Interrupt Enable Register 1

Name: IEC1
Offset: 0x822

Bit	15	14	13	12	11	10	9	8
	C1RXIE	SPI2TXIE	SPI2RXIE	U2TXIE	U2RXIE	INT3IE	C1IE	CCT2IE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CCP2IE		DMA3IE	INT2IE	CNCIE	DMA2IE	MI2C1IE	SI2C1IE
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 15 – C1RXIE CAN1 RX Data Ready Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 14 – SPI2TXIE SPI2 Transmitter Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 13 – SPI2RXIE SPI2 Receiver Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 12 – U2TXIE UART2 Transmitter Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 11 – U2RXIE UART2 Receiver Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 10 – INT3IE External Interrupt 3 Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 9 – C1IE CAN1 Combined Error Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

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Bit 8 – CCT2IE SCCP2 Timer Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 7 – CCP2IE Input Capture/Output Compare 2 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 5 – DMA3IE Direct Memory Access 3 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 4 – INT2IE External Interrupt 2 Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 3 – CNCIE Change Notice C Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 2 – DMA2IE Direct Memory Access 2 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 1 – MI2C1IE I2C1 Host Events Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 0 – SI2C1IE I2C1 Client Events Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

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7.7.13. Interrupt Enable Register 2

Name: IEC2
Offset: 0x824

Bit	15	14	13	12	11	10	9	8
			DMTIE				CCT4IE	CCP4IE
Access			R/W				R/W	R/W
Reset			0				0	0

Bit	7	6	5	4	3	2	1	0
				CCT3IE	CCP3IE			
Access				R/W	R/W			
Reset				0	0			

Bit 13 – DMTIE Deadman Timer Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 9 – CCT4IE SCCP4 Timer Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 8 – CCP4IE Input Capture/Output Compare 4 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 4 – CCT3IE SCCP3 Timer Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 3 – CCP3IE Input Capture/Output Compare 3 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

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7.7.14. Interrupt Enable Register 3

Name: IEC3
Offset: 0x826

Bit	15	14	13	12	11	10	9	8
	PTGSTEPIE		ICDIE			U3TXIE	U3RXIE	U3EIE
Access	R/W		R/W			R/W	R/W	R/W
Reset	0		0			0	0	0

Bit	7	6	5	4	3	2	1	0
				C1TXIE	CRCIE	U2EIE	U1EIE	QEI1IE
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 15 – PTGSTEPIE PTG Step Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 13 – ICDIE ICD Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 10 – U3TXIE UART3 Transmitter Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 9 – U3RXIE UART3 Receiver Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 8 – U3EIE UART3 Error Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 4 – C1TXIE CAN1 TX Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 3 – CRCIE CRC Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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Bit 2 – U2EIE UART2 Error Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 1 – U1EIE UART1 Error Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 0 – QEI1IE QEI1 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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7.7.15. Interrupt Enable Register 4

Name: IEC4
Offset: 0x828

Bit	15	14	13	12	11	10	9	8
		CMP2IE	CMP1IE		CNDIE			
Access		R/W	R/W		R/W			
Reset		0	0		0			

Bit	7	6	5	4	3	2	1	0
		PWM4IE	PWM3IE	PWM2IE	PWM1IE			I2C1BCIE
Access		R/W	R/W	R/W	R/W			R/W
Reset		0	0	0	0			0

Bit 14 – CMP2IE Comparator 2 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 13 – CMP1IE Comparator 1 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 11 – CNDIE Change Notice D Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 6 – PWM4IE PWM Generator 4 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 5 – PWM3IE PWM Generator 3 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 4 – PWM2IE PWM Generator 2 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 3 – PWM1IE PWM Generator 1 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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Bit 0 – I2C1BCIE I2C1 Bus Collision Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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7.7.16. Interrupt Enable Register 5

Name: IEC5
Offset: 0x82A

Bit	15	14	13	12	11	10	9	8
	AD1AN4IE	AD1AN3IE	AD1AN2IE	AD1AN1IE	AD1AN0IE	ADCIE		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
	SENT1EIE	SENT1IE	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 15 – AD1AN4IE ADC AN4 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 14 – AD1AN3IE ADC AN3 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 13 – AD1AN2IE ADC AN2 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 12 – AD1AN1IE ADC AN1 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 11 – AD1AN0IE ADC AN0 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 10 – ADCIE ADC Global Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 7 – SENT1EIE SENT1 External Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

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Bit 6 – SENT1IE SENT1 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 5 – PTG3IE PTG3 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 4 – PTG2IE PTG2 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 3 – PTG1IE PTG1 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 2 – PTG0IE PTG0 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 1 – PTGWDTIE PTG Watchdog Timer Time-out Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

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7.7.17. Interrupt Enable Register 6

Name: IEC6
Offset: 0x82C

Bit	15	14	13	12	11	10	9	8
	AD1AN20IE	AD1AN19IE	AD1AN18IE	AD1AN17IE	AD1AN16IE	AD1AN15IE	AD1AN14IE	AD1AN13IE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	AD1AN12IE	AD1AN11IE	AD1AN10IE	AD1AN9IE	AD1AN8IE	AD1AN7IE	AD1AN6IE	AD1AN5IE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – AD1AN20IE ADC AN20 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 14 – AD1AN19IE ADC AN19 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 13 – AD1AN18IE ADC AN18 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 12 – AD1AN17IE ADC AN17 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 11 – AD1AN16IE ADC AN16 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 10 – AD1AN15IE ADC AN15 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 9 – AD1AN14IE ADC AN14 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

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Bit 8 – AD1AN13IE ADC AN13 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 7 – AD1AN12IE ADC AN12 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 6 – AD1AN11IE ADC AN11 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 5 – AD1AN10IE ADC AN10 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 4 – AD1AN9IE ADC AN9 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 3 – AD1AN8IE ADC AN8 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 2 – AD1AN7IE ADC AN7 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 1 – AD1AN6IE ADC AN6 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 0 – AD1AN5IE ADC AN5 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

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7.7.18. Interrupt Enable Register 7

Name: IEC7
Offset: 0x82E

Bit	15	14	13	12	11	10	9	8
	SPI2GIE	SPI1GIE	CLC2PIE	CLC1PIE	ADFLTR3IE	ADFLTR2IE	ADFLTR1IE	ADFLTR0IE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADCMP3IE	ADCMP2IE	ADCMP1IE	ADCMP0IE	ADFLTIE			AD1AN21IE
Access	R/W	R/W	R/W	R/W	R/W			R/W
Reset	0	0	0	0	0			0

Bit 15 – SPI2GIE SPI2 Error Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 14 – SPI1GIE SPI1 Error Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 13 – CLC2PIE CLC2 Positive Edge Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 12 – CLC1PIE CLC1 Positive Edge Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 11 – ADFLTR3IE ADC Oversample Filter 3 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 10 – ADFLTR2IE ADC Oversample Filter 2 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 9 – ADFLTR1IE ADC Oversample Filter 1 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

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Bit 8 – ADFLTR0IE ADC Oversample Filter 0 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 7 – ADCMP3IE ADC Digital Comparator 3 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 6 – ADCMP2IE ADC Digital Comparator 2 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 5 – ADCMP1IE ADC Digital Comparator 1 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 4 – ADCMP0IE ADC Digital Comparator 0 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 3 – ADFLTIE ADC Fault Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 0 – AD1AN21IE ADC AN21 Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

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7.7.19. Interrupt Enable Register 10

Name: IEC10
Offset: 0x834

Bit	15	14	13	12	11	10	9	8
	CLC3PIE	PEVTFIE	PEVTEIE	PEVTDIE	PEVTCIE	PEVTBIE	PEVTAIE	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – CLC3PIE CLC3 Positive Edge Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 14 – PEVTFIE PWM Event F Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 13 – PEVTEIE PWM Event E Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 12 – PEVTDIE PWM Event D Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 11 – PEVTCIE PWM Event C Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 10 – PEVTBIE PWM Event B Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 9 – PEVTAIE PWM Event A Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

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7.7.20. Interrupt Enable Register 11

Name: IEC11
Offset: 0x836

Bit	15	14	13	12	11	10	9	8
	U3ENTIE	U2ENTIE	U1ENTIE					
Access	R/W	R/W	R/W					
Reset	0	0	0					

Bit	7	6	5	4	3	2	1	0
				CLC4NIE	CLC3NIE	CLC2NIE	CLC1NIE	CLC4PIE
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 15 – U3ENTIE UART3 Event Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 14 – U2ENTIE UART2 Event Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 13 – U1ENTIE UART1 Event Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 4 – CLC4NIE CLC4 Negative Edge Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 3 – CLC3NIE CLC3 Negative Edge Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 2 – CLC2NIE CLC2 Negative Edge Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

Bit 1 – CLC1NIE CLC1 Negative Edge Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

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Bit 0 – CLC4PIE CLC4 Positive Edge Interrupt Enable bit

Value	Description
1	Interrupt enabled.
0	Interrupt not enabled.

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7.7.21. Interrupt Priority Register 0

Name: IPC0
Offset: 0x840

Bit	15	14	13	12	11	10	9	8
		CNBIP[2:0]				CNAIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		T1IP[2:0]				INT0IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – CNBIP[2:0] Change Notice B Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – CNAIP[2:0] Change Notice A Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – T1IP[2:0] Timer1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – INT0IP[2:0] External Interrupt 0 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.22. Interrupt Priority Register 1

Name: IPC1
Offset: 0x842

Bit	15	14	13	12	11	10	9	8
		CCT1IP[2:0]				CCP1IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
						DMA0IP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bits 14:12 – CCT1IP[2:0] SCCP1 Timer Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – CCP1IP[2:0] Input Capture/Output Compare 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – DMA0IP[2:0] Direct Memory Access 0 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.23. Interrupt Priority Register 2

Name: IPC2
Offset: 0x844

Bit	15	14	13	12	11	10	9	8
		U1RXIP[2:0]				SPI1TXIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		SPI1RXIP[2:0]				DMA1IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – U1RXIP[2:0] UART1 Receiver Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – SPI1TXIP[2:0] SPI1 Transfer Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – SPI1RXIP[2:0] SPI1 Receiver Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – DMA1IP[2:0] Direct Memory Access 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.24. Interrupt Priority Register 3

Name: IPC3
Offset: 0x846

Bit	15	14	13	12	11	10	9	8
		INT1IP[2:0]				NVMIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		ECCSBIP[2:0]				U1TXIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – INT1IP[2:0] External Interrupt 1 Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – NVMIP[2:0] NVM Program/Erase Complete Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – ECCSBIP[2:0] Error Correcting Code Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – U1TXIP[2:0] UART1 Transmitter Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.25. Interrupt Priority Register 4

Name: IPC4
Offset: 0x848

Bit	15	14	13	12	11	10	9	8
		CNCIP[2:0]				DMA2IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		MI2C1IP[2:0]				SI2C1IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – CNCIP[2:0] Change Notification C Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – DMA2IP[2:0] Direct Memory Access 2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – MI2C1IP[2:0] I2C1 Host Events Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – SI2C1IP[2:0] I2C1 Client Events Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.26. Interrupt Priority Register 5

Name: IPC5
Offset: 0x84A

Bit	15	14	13	12	11	10	9	8
		CCP2IP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bit	7	6	5	4	3	2	1	0
		DMA3IP[6:4]				INT2IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – CCP2IP[2:0] Interrupt-on-Change 2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – DMA3IP[6:4] Direct Memory Access 3 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – INT2IP[2:0] External Interrupt 2 Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.27. Interrupt Priority Register 6

Name: IPC6
Offset: 0x84C

Bit	15	14	13	12	11	10	9	8
		U2RXIP[2:0]				INT3IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
						CCT2IP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bits 14:12 – U2RXIP[2:0] UART2 Receiver Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – INT3IP[2:0] External Interrupt 3 Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – CCT2IP[2:0] SCCP2 Timer Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.28. Interrupt Priority Register 7

Name: IPC7
Offset: 0x84E

Bit	15	14	13	12	11	10	9	8
		C1RXIP[2:0]				SPI2TXIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		SPI2RXIP[2:0]				U2TXIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – C1RXIP[2:0] CAN1 RX Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – SPI2TXIP[2:0] SPI2 Transmitter Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – SPI2RXIP[2:0] SPI2 Receiver Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – U2TXIP[2:0] UART 2 Transmitter Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.29. Interrupt Priority Register 8

Name: IPC8
Offset: 0x850

Bit	15	14	13	12	11	10	9	8
		CCP3IP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 14:12 – CCP3IP[2:0] Input Capture/Output Compare 3 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.30. Interrupt Priority Register 9

Name: IPC9
Offset: 0x852

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						CCT3IP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bits 2:0 – CCT3IP[2:0] SCCP3 Timer Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.31. Interrupt Priority Register 10

Name: IPC10
Offset: 0x854

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		CCT4IP[2:0]				CCP4IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 6:4 – CCT4IP[2:0] SCCP4 Timer Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – CCP4IP[2:0] Input Capture/Output Compare 4 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.32. Interrupt Priority Register 11

Name: IPC11
Offset: 0x856

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		DMTIP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bits 6:4 – DMTIP[2:0] Deadman Timer Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.33. Interrupt Priority Register 12

Name: IPC12
Offset: 0x858

Bit	15	14	13	12	11	10	9	8
		CRCIP[2:0]				U2EIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		U1EIP[2:0]				QEI1IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – CRCIP[2:0] Cyclic Redundancy Check Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – U2EIP[2:0] UART2 Error Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – U1EIP[2:0] UART1 Error Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – QEI1IP[2:0] QEI1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.34. Interrupt Priority Register 13

Name: IPC13
Offset: 0x85A

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						C1TXIP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bits 2:0 – C1TXIP[2:0] CAN1 TX Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.35. Interrupt Priority Register 14

Name: IPC14
Offset: 0x85C

Bit	15	14	13	12	11	10	9	8
						U3TXIP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bit	7	6	5	4	3	2	1	0
		U3RXIP[2:0]				U3EIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 10:8 – U3TXIP[2:0] UART3 Transmitter Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – U3RXIP[2:0] UART3 Receiver Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – U3EIP[2:0] UART3 External Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.36. Interrupt Priority Register 15

Name: IPC15
Offset: 0x85E

Bit	15	14	13	12	11	10	9	8
		PTGSTEPIP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bit	7	6	5	4	3	2	1	0
		ICDIP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bits 14:12 – PTGSTEPIP[2:0] PTG Step Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – ICDIP[2:0] ICD Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.37. Interrupt Priority Register 16

Name: IPC16
Offset: 0x860

Bit	15	14	13	12	11	10	9	8
		PWM1IP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bit	7	6	5	4	3	2	1	0
						I2C1BCIP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bits 14:12 – PWM1IP[2:0] PWM Generator 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – I2C1BCIP[2:0] I2C1 Bus Collision Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.38. Interrupt Priority Register 17

Name: IPC17
Offset: 0x862

Bit	15	14	13	12	11	10	9	8
						PWM4IP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bit	7	6	5	4	3	2	1	0
		PWM3IP[2:0]				PWM2IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 10:8 – PWM4IP[2:0] PWM Generator 4 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – PWM3IP[2:0] PWM Generator 3 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – PWM2IP[2:0] PWM Generator 2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.39. Interrupt Priority Register 18

Name: IPC18
Offset: 0x864

Bit	15	14	13	12	11	10	9	8
		CNDIP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 14:12 – CNDIP[2:0] Change Notice D Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.40. Interrupt Priority Register 19

Name: IPC19
Offset: 0x866

Bit	15	14	13	12	11	10	9	8
						CMP2IP[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
		CMP1IP[2:0]						
Access		R/W	R/W	R/W				
Reset		0	0	0				

Bits 10:8 – CMP2IP[2:0] Comparator 2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – CMP1IP[2:0] Comparator 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.41. Interrupt Priority Register 20

Name: IPC20
Offset: 0x868

Bit	15	14	13	12	11	10	9	8
		PTG1IP[2:0]				PTG0IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		PTGWDTIP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bits 14:12 – PTG1IP[2:0] Peripheral Trigger Generator 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – PTG0IP[2:0] Peripheral Trigger Generator 0 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – PTGWDTIP[2:0] PTG Watchdog Timer Time-out Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.42. Interrupt Priority Register 21

Name: IPC21
Offset: 0x86A

Bit	15	14	13	12	11	10	9	8
		SENT1EIP[2:0]				SENT1IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		PTG3IP[2:0]				PTG2IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – SENT1EIP[2:0] SENT1 External Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – SENT1IP[2:0] SENT1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – PTG3IP[2:0] Peripheral Trigger Generator 3 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – PTG2IP[2:0] Peripheral Trigger Generator 2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.43. Interrupt Priority Register 22

Name: IPC22
Offset: 0x86C

Bit	15	14	13	12	11	10	9	8
		AD1AN0IP[2:0]				ADCIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 14:12 – AD1AN0IP[2:0] ADC AN0 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – ADCIP[2:0] ADC Global Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.44. Interrupt Priority Register 23

Name: IPC23
Offset: 0x86E

Bit	15	14	13	12	11	10	9	8
		AD1AN4IP[2:0]				AD1AN3IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		AD1AN2IP[2:0]				ADCAN1IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – AD1AN4IP[2:0] ADC AN4 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – AD1AN3IP[2:0] ADC AN3 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – AD1AN2IP[2:0] ADC AN2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – ADCAN1IP[2:0] ADC CAN1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.45. Interrupt Priority Register 24

Name: IPC24
Offset: 0x870

Bit	15	14	13	12	11	10	9	8
		AD1AN8IP[2:0]				AD1AN7IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		AD1AN6IP[2:0]				AD1AN5IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – AD1AN8IP[2:0] ADC AN8 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – AD1AN7IP[2:0] ADC AN7 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – AD1AN6IP[2:0] ADC AN6 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – AD1AN5IP[2:0] ADC AN5 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.46. Interrupt Priority Register 25

Name: IPC25
Offset: 0x872

Bit	15	14	13	12	11	10	9	8
		AD1AN12IP[2:0]				AD1AN11IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		AD1AN10IP[2:0]				AD1AN9IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – AD1AN12IP[2:0] ADC AN12 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – AD1AN11IP[2:0] ADC AN11 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – AD1AN10IP[2:0] ADC AN10 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – AD1AN9IP[2:0] ADC AN9 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.47. Interrupt Priority Register 26

Name: IPC26
Offset: 0x874

Bit	15	14	13	12	11	10	9	8
		AD1AN16IP[2:0]				AD1AN15IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		AD1AN14IP[2:0]				AD1AN13IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – AD1AN16IP[2:0] ADC AN16 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – AD1AN15IP[2:0] ADC AN15 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – AD1AN14IP[2:0] ADC AN14 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – AD1AN13IP[2:0] ADC AN13 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.48. Interrupt Priority Register 27

Name: IPC27
Offset: 0x876

Bit	15	14	13	12	11	10	9	8
		AD1AN20IP[2:0]				AD1AN19IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		AD1AN18IP[2:0]				AD1AN17IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – AD1AN20IP[2:0] ADC AN20 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – AD1AN19IP[2:0] ADC AN19 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – AD1AN18IP[2:0] ADC AN18 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – AD1AN17IP[2:0] ADC AN17 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.49. Interrupt Priority Register 28

Name: IPC28
Offset: 0x878

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						AD1AN21IP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bits 2:0 – AD1AN21IP[2:0] ADC AN21 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.50. Interrupt Priority Register 29

Name: IPC29
Offset: 0x87A

Bit	15	14	13	12	11	10	9	8
		ADCMP3IP[2:0]				ADCMP2IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		ADCMP1IP[2:0]				ADCMP0IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – ADCMP3IP[2:0] ADC Digital Comparator 3 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – ADCMP2IP[2:0] ADC Digital Comparator 2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – ADCMP1IP[2:0] ADC Digital Comparator 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – ADCMP0IP[2:0] ADC Digital Comparator 0 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.51. Interrupt Priority Register 30

Name: IPC30
Offset: 0x87C

Bit	15	14	13	12	11	10	9	8
		ADFLTR3IP[2:0]				ADFLTR2IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		ADFLTR1IP[2:0]				ADFLTR0IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – ADFLTR3IP[2:0] ADC Oversample Filter 3 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – ADFLTR2IP[2:0] ADC Oversample Filter 2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – ADFLTR1IP[2:0] ADC Oversample Filter 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – ADFLTR0IP[2:0] ADC Oversample Filter 0 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.52. Interrupt Priority Register 31

Name: IPC31
Offset: 0x87E

Bit	15	14	13	12	11	10	9	8
		SPI2IP[2:0]				SPI1IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		CLC2PIP[2:0]				CLC1PIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – SPI2IP[2:0] SPI2 Error Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – SPI1IP[2:0] SPI1 Error Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – CLC2PIP[2:0] CLC2 Positive Edge Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – CLC1PIP[2:0] CLC1 Positive Edge Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.53. Interrupt Priority Register 42

Name: IPC42
Offset: 0x894

Bit	15	14	13	12	11	10	9	8
		PEVTCIP[2:0]				PEVTBIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		PEVTAIP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bits 14:12 – PEVTCIP[2:0] PWM Event C Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – PEVTBIP[2:0] PWM Event B Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – PEVTAIP[2:0] PWM Event A Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.54. Interrupt Priority Register 43

Name: IPC43
Offset: 0x896

Bit	15	14	13	12	11	10	9	8
		CLC3PEIP[2:0]				PEVTFIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		PEVTEIP[2:0]				PEVTDIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – CLC3PEIP[2:0] CLC3 Positive Edge Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – PEVTFIP[2:0] PWM Event F Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – PEVTEIP[2:0] PWM Event E Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – PEVTDIP[2:0] PWM Event D Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.55. Interrupt Priority Register 44

Name: IPC44
Offset: 0x898

Bit	15	14	13	12	11	10	9	8
		CLC3NEIP[2:0]				CLC2NEIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		CLC1NEIP[2:0]				CLC4PEIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – CLC3NEIP[2:0] CLC3 Negative Edge Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – CLC2NEIP[2:0] CLC2 Negative Edge Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – CLC1NEIP[2:0] CLC1 Negative Edge Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – CLC4PEIP[2:0] CLC4 Positive Edge Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)

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Value	Description
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.56. Interrupt Priority Register 45

Name: IPC45
Offset: 0x89A

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						CLC4NEIP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bits 2:0 – CLC4NEIP[2:0] CLC4 Negative Edge Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.57. Interrupt Priority Register 47

Name: IPC47
Offset: 0x89E

Bit	15	14	13	12	11	10	9	8
		U3EVTIP[2:0]				U2EVTIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		U1EVTIP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bits 14:12 – U3EVTIP[2:0] UART3 Event Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – U2EVTIP[2:0] UART2 Event Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – U1EVTIP[2:0] UART1 Event Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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7.7.58. Interrupt Control Register 1

Name: INTCON1
Offset: 0x8C0

Bit	15	14	13	12	11	10	9	8
	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SFTACERR	DIV0ERR		MATHERR	ADDRERR	STKERR	OSCFAIL	
Access	R/W	R/W		R/W	R/W	R/W	R/W	
Reset	0	0		0	0	0	0	

Bit 15 – NSTDIS Interrupt Nesting Disable bit

Value	Description
1	Interrupt nesting is disabled.
0	Interrupt nesting is enabled.

Bit 14 – OVAERR Accumulator A Overflow Trap Flag bit

Value	Description
1	Trap was caused by overflow of Accumulator A.
0	Trap was not caused by overflow of Accumulator A.

Bit 13 – OVBERR Accumulator B Overflow Trap Flag bit

Value	Description
1	Trap was caused by overflow of Accumulator B.
0	Trap was not caused by overflow of Accumulator B.

Bit 12 – COVAERR Accumulator A Catastrophic Overflow Trap Flag bit

Value	Description
1	Trap was caused by catastrophic overflow of Accumulator A.
0	Trap was not caused by catastrophic overflow of Accumulator A.

Bit 11 – COVBERR Accumulator B Catastrophic Overflow Trap Flag bit

Value	Description
1	Trap was caused by catastrophic overflow of Accumulator B.
0	Trap was not caused by catastrophic overflow of Accumulator B.

Bit 10 – OVATE Accumulator A Overflow Trap Enable bit

Value	Description
1	Trap overflow of Accumulator A.
0	Trap is disabled.

Bit 9 – OVBTE Accumulator B Overflow Trap Enable bit

Value	Description
1	Trap overflow of Accumulator B.
0	Trap is disabled.

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Bit 8 – COVTE Catastrophic Overflow Trap Enable bit

Value	Description
1	Trap on catastrophic overflow of Accumulator A or B is enabled.
0	Trap is disabled.

Bit 7 – SFTACERR Shift Accumulator Error Status bit

Value	Description
1	Math error trap was caused by an invalid accumulator shift.
0	Math error trap was not caused by an invalid accumulator shift.

Bit 6 – DIV0ERR Divide-by-Zero Error Status bit

Value	Description
1	Math error trap was caused by a divide-by-zero.
0	Math error trap was not caused by a divide-by-zero.

Bit 4 – MATHERR Math Error Status bit

Value	Description
1	Math error trap has occurred.
0	Math error trap has not occurred.

Bit 3 – ADDRERR Address Error Trap Status bit

Value	Description
1	Address error trap has occurred.
0	Address error trap has not occurred.

Bit 2 – STKERR Stack Error Trap Status bit

Value	Description
1	Stack error trap has occurred.
0	Stack error trap has not occurred.

Bit 1 – OSCFAIL Oscillator Failure Trap Status bit

Value	Description
1	Oscillator failure trap has occurred.
0	Oscillator failure trap has not occurred.

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7.7.59. Interrupt Control Register 2

Name: INTCON2
Offset: 0x8C2

Bit	15	14	13	12	11	10	9	8
	GIE	DISI	SWTRAP					AIVTEN
Access	R/W	R/W	R/W					R/W
Reset	1	0	0					0

Bit	7	6	5	4	3	2	1	0
					INT3EP	INT2EP	INT1EP	INT0EP
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – GIE Global Interrupt Enable bit

Value	Description
1	Interrupts and associated IE bits are enabled.
0	Interrupts are disabled, but traps are still enabled.

Bit 14 – DISI `DISI` Instruction Status bit

Value	Description
1	`DISI` instruction is active.
0	`DISI` instruction is not active.

Bit 13 – SWTRAP Software Trap Status bit

Value	Description
1	Software trap is enabled.
0	Software trap is disabled.

Bit 8 – AIVTEN Alternate Interrupt Vector Table Enable bit

Value	Description
1	Uses Alternate Interrupt Vector Table
0	Uses standard Interrupt Vector Table

Bit 3 – INT3EP External Interrupt 3 Edge Detect Polarity Select bit

Value	Description
1	Interrupt on negative edge
0	Interrupt on positive edge

Bit 2 – INT2EP External Interrupt 2 Edge Detect Polarity Select bit

Value	Description
1	Interrupt on negative edge
0	Interrupt on positive edge

Bit 1 – INT1EP External Interrupt 1 Edge Detect Polarity Select bit

Value	Description
1	Interrupt on negative edge
0	Interrupt on positive edge

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Bit 0 – INT0EP External Interrupt 0 Edge Detect Polarity Select bit

Value	Description
1	Interrupt on negative edge
0	Interrupt on positive edge

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7.7.60. Interrupt Control Register 3

Name: INTCON3
Offset: 0x8C4

Bit	15	14	13	12	11	10	9	8
							CAN	NAE
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
			DAE	DOOVR				
Access			R/W	R/W				
Reset			0	0				

Bit 9 – CAN CAN Address Error Soft Trap Status bit

Value	Description
1	CAN address error soft trap has occurred.
0	CAN address error soft trap has not occurred.

Bit 8 – NAE NVM Address Error Soft Trap Status bit

Value	Description
1	NVM address error soft trap has occurred.
0	NVM address error soft trap has not occurred.

Bit 5 – DAE DAE DMA Address Error Soft Trap Status bit

Value	Description
1	DMA address error trap has occurred.
0	DMA address error trap has not occurred.

Bit 4 – DOOVR DO Stack Overflow Soft Trap Status bit

Value	Description
1	DO stack overflow soft trap has occurred.
0	DO stack overflow soft trap has not occurred.

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7.7.61. Interrupt Control Register 4

Name: INTCON4
Offset: 0x8C6

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							ECCDBE	SGHT
Access							R/W	R/W
Reset							0	0

Bit 1 – ECCDBE ECC Double-Bit Error Trap bit

Value	Description
1	ECC double-bit error trap has occurred.
0	ECC double-bit error trap has not occurred.

Bit 0 – SGHT Software Generated Hard Trap Status bit

Value	Description
1	Software generated hard trap has occurred.
0	Software generated hard trap has not occurred.

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7.7.62. Interrupt Control and Status Register

Name: INTTREG
Offset: 0x8C8

Bit	15	14	13	12	11	10	9	8
			VHOLD		ILR[3:0]			
Access			R/W		R	R	R	R
Reset			0		0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VECNUM[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 13 – VHOLD Vector Number Capture Enable bit

Value	Description
1	VECNUM[7:0] bits read current value of vector number encoding tree (i.e., highest priority pending interrupt).
0	Vector number latched into VECNUM[7:0] at interrupt Acknowledge and retained until next IACK.

Bits 11:8 – ILR[3:0] New CPU Interrupt Priority Level bits

Value	Description
1111	CPU Interrupt Priority Level is 15
. . .	
0001	CPU Interrupt Priority Level is 1
0000	CPU Interrupt Priority Level is 0

Bits 7:0 – VECNUM[7:0] Vector Number of Pending Interrupt bits

Value	Description
11111111	255, Reserved; do not use
. . .	
00001001	9, IC1 – Input Capture 1
00001000	8, INT0 – External Interrupt 0
00000111	7, Reserved; do not use
00000110	6, Generic soft error trap
00000101	5, Reserved; do not use
00000100	4, Math error trap
00000011	3, Stack error trap
00000010	2, Generic hard trap
00000001	1, Address error trap
00000000	0, Oscillator fail trap

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7.8. Key Resources

- **"Interrupts"** (www.microchip.com/DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

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8. I/O Ports

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"I/O Ports with Edge Detect"** (www.microchip.com/DS70005322) in the *"dsPIC33/PIC24 Family Reference Manual"*.

Many of the device pins are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

Some of the key features of the I/O ports are:

- Individual Output Pin Open-Drain Enable/Disable
- Individual Input Pin Weak Pull-up and Pull-Down
- Monitor Selective Inputs and Generate Interrupt when a Change in Pin State is Detected
- Operation during Sleep and Idle Modes

8.1. Parallel I/O (PIO) Ports

All port pins have 12 registers directly associated with their operation as digital I/Os. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input.

All port pins are defined as inputs after a Reset.

Table 8-1.

Pin	Function
Reads from the latch (LATx)	Read the latch
Writes to the latch	Write the latch
Reads from the port (PORTx)	Read the port pins
Writes to the port pins	Write the latch

Any bit and its associated data and control registers that are not valid for a particular device are disabled. This means the corresponding LATx and TRISx registers, as well as the port pin, are read as zeros.

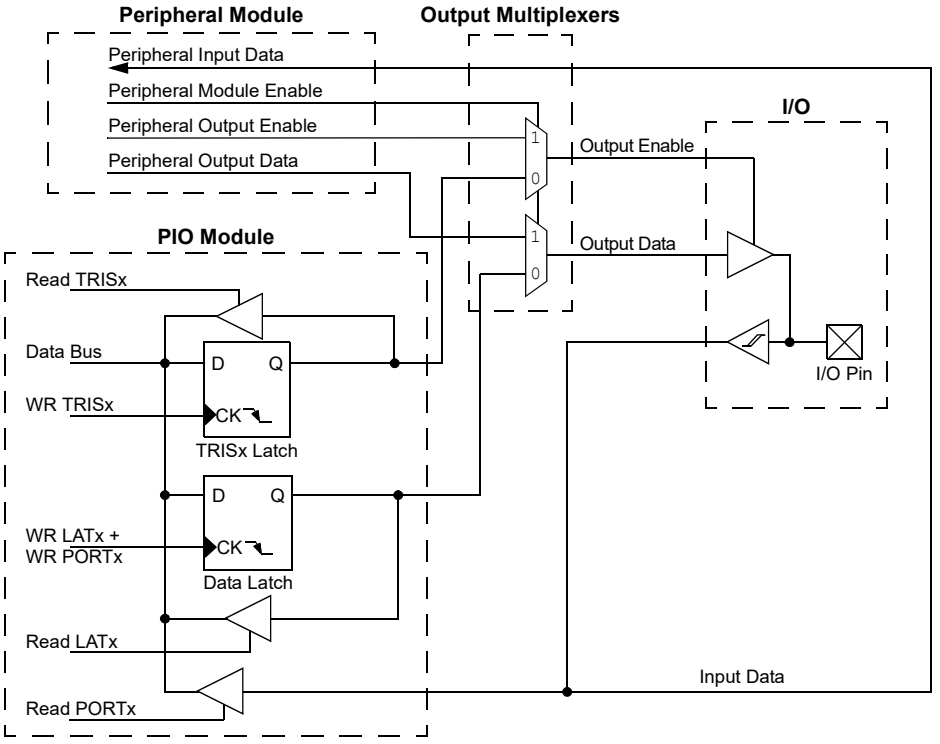
When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs. Table 8-2 shows the pin availability. Figure 8-1 shows the 5V input tolerant pins across this device.

Table 8-2. Pin and ANSELx Availability

Device	Rx15	Rx14	Rx13	Rx12	Rx11	Rx10	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Rx1	Rx0
PORTA																
dsPIC33CDV(L)XXXMC506/106	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X
ANSELA	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X
PORTB																
dsPIC33CDV(L)XXXMC506/106	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ANSELB	—	—	—	—	—	—	X	X	X	—	—	X	X	X	X	X
PORTC																
dsPIC33CDV(L)XXXMC506/106	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ANSELC	—	—	—	—	—	—	—	—	X	X	—	—	X	X	X	X
PORTD																
dsPIC33CDV(L)XXXMC506/106	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ANSELD	—	—	X	—	—	X	—	—	—	—	—	—	—	—	—	—

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Figure 8-1. Block Diagram of a Typical Shared Port Structure



8.1.1. Open-Drain Configuration

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Enable for PORTx register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs, other than V_{DD}, by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum V_{IH} specification for that particular pin.

8.2. Configuring Analog and Digital Port Pins

The ANSELx registers control the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules (such as timers, UARTs, etc.), the corresponding ANSELx bit must be cleared.

The ANSELx registers have a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-2).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (V_{OH} or V_{OL}) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin, defined as a digital input (including the ANx pins), can cause the input buffer to consume current that exceeds the device specifications.

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8.2.1. I/O Port Write/Read Timing

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a `NOP`.

The following registers are in the PORT module:

- ANSELx (one per port)
- TRISx (one per port)
- PORTx (one per port)
- LATx (one per port)
- ODCx (one per port)
- CNPUx (one per port)
- CNPDx (one per port)
- CNCONx (one per port – optional)
- CNEN0x (one per port)
- CNSTATx (one per port – optional)
- CNEN1x (one per port)
- CNFx (one per port)

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8.2.2. Port Controls/Status Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0E00	ANSELA	15:8								
		7:0				ANSEL[4:0]				
0x0E02	TRISA	15:8								
		7:0				TRISA[4:0]				
0x0E04	PORTA	15:8								
		7:0				RA[4:0]				
0x0E06	LATA	15:8								
		7:0				LATA[4:0]				
0x0E08	ODCA	15:8								
		7:0				ODCA[4:0]				
0x0E0A	CNPUA	15:8								
		7:0				CNPUA[4:0]				
0x0E0C	CNPDA	15:8								
		7:0				CNPDA[4:0]				
0x0E0E	CNCONA	15:8	ON				CNSTYLE			
		7:0								
0x0E10	CNEN0A	15:8								
		7:0				CNEN0A[4:0]				
0x0E12	CNSTATA	15:8								
		7:0				CNSTATA[4:0]				
0x0E14	CNEN1A	15:8								
		7:0				CNEN1A[4:0]				
0x0E16	CNFA	15:8								
		7:0				CNFA[4:0]				
0x0E18 ... 0x0E1B	Reserved									
0x0E1C	ANSELB	15:8							ANSELB[9:7]	
		7:0	ANSELB[9:7]			ANSELB[4:0]				
0x0E1E	TRISB	15:8	TRISB[15:8]							
		7:0	TRISB[7:0]							
0x0E20	PORTB	15:8	RB[15:8]							
		7:0	RB[7:0]							
0x0E22	LATB	15:8	LATB[15:8]							
		7:0	LATB[7:0]							
0x0E24	ODCB	15:8	ODCB[15:8]							
		7:0	ODCB[7:0]							
0x0E26	CNPUB	15:8	CNPUB[15:8]							
		7:0	CNPUB[7:0]							
0x0E28	CNPDB	15:8	CNPDB[15:8]							
		7:0	CNPDB[7:0]							
0x0E2A	CNCONB	15:8	ON				CNSTYLE			
		7:0								
0x0E2C	CNEN0B	15:8	CNEN0B[15:8]							
		7:0	CNEN0B[7:0]							
0x0E2E	CNSTATB	15:8	CNSTATB[15:8]							
		7:0	CNSTATB[7:0]							
0x0E30	CNEN1B	15:8	CNEN1B[15:8]							
		7:0	CNEN1B[7:0]							
0x0E32	CNFB	15:8	CNFB[15:8]							
		7:0	CNFB[7:0]							
0x0E34 ... 0x0E37	Reserved									
0x0E38	ANSELC	15:8								
		7:0	ANSELC[7:6]				ANSELC[3:0]			
0x0E3A	TRISC	15:8	TRISC[15:8]							
		7:0	TRISC[7:0]							

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Port Controls/Status Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0E3C	PORTC	15:8	RC[15:8]							
		7:0	RC[7:0]							
0x0E3E	LATC	15:8	LATC[15:8]							
		7:0	LATC[7:0]							
0x0E40	ODCC	15:8	ODCC[15:8]							
		7:0	ODCC[7:0]							
0x0E42	CNPUC	15:8	CNPUC[15:8]							
		7:0	CNPUC[7:0]							
0x0E44	CNPDC	15:8	CNPDC[15:8]							
		7:0	CNPDC[7:0]							
0x0E46	CNCONC	15:8	ON				CNSTYLE			
		7:0								
0x0E48	CNEN0C	15:8	CNEN0C[15:8]							
		7:0	CNEN0C[7:0]							
0x0E4A	CNSTATC	15:8	CNSTATC[15:8]							
		7:0	CNSTATC[7:0]							
0x0E4C	CNEN1C	15:8	CNEN1C[15:8]							
		7:0	CNEN1C[7:0]							
0x0E4E	CNFC	15:8	CNFC[15:8]							
		7:0	CNFC[7:0]							
0x0E50 ... 0x0E53	Reserved									
0x0E54	ANSELD	15:8			ANSELD13		ANSELD[11:10]			
		7:0								
0x0E56	TRISD	15:8	TRISD[15:8]							
		7:0	TRISD[7:0]							
0x0E58	PORTD	15:8	RD[15:8]							
		7:0	RD[7:0]							
0x0E5A	LATD	15:8	LATD[15:8]							
		7:0	LATD[7:0]							
0x0E5C	ODCD	15:8	ODCD[15:8]							
		7:0	ODCD[7:0]							
0x0E5E	CNPUD	15:8	CNPUD[15:8]							
		7:0	CNPUD[7:0]							
0x0E60	CNPDD	15:8	CNPDD[15:8]							
		7:0	CNPDD[7:0]							
0x0E62	CNCOND	15:8	ON				CNSTYLE			
		7:0								
0x0E64	CNEN0D	15:8	CNEN0D[15:8]							
		7:0	CNEN0D[7:0]							
0x0E66	CNSTATD	15:8	CNSTATD[15:8]							
		7:0	CNSTATD[7:0]							
0x0E68	CNEN1D	15:8	CNEN1D[15:8]							
		7:0	CNEN1D[7:0]							
0x0E6A	CNFD	15:8	CNFD[15:8]							
		7:0	CNFD[7:0]							

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8.2.2.1. Analog Select for PORTA Register

Name: ANSELA
Offset: 0xE00

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				ANSEL[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				1	1	1	1	1

Bits 4:0 – ANSEL[4:0] Analog Select for PORTx bits

Value	Description
1	Analog input is enabled and digital input is disabled on the PORTx[n] pin.
0	Analog input is disabled and digital input is enabled on the PORTx[n] pin.

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8.2.2.2. Output Enable for PORTA Register

Name: TRISA
Offset: 0xE02

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				TRISA[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	1

Bits 4:0 – TRISA[4:0] Output Enable for PORTx bits

Value	Description
1	LATx[n] is not driven on the PORTx[n] pin.
0	LATx[n] is driven on the PORTx[n] pin.

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8.2.2.3. Input Data for PORTA Register

Name: PORTA
Offset: 0xE04

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				RA[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	1

Bits 4:0 – RA[4:0] PORTA Data Input Value bits

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8.2.2.4. Output Data for PORTA Register

Name: LATA
Offset: 0xE06

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				LATA[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				x	x	x	x	0

Bits 4:0 – LATA[4:0] PORTA Data Output Value bits

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8.2.2.5. Open-Drain Enable for PORTA Register

Name: ODCA
Offset: 0xE08

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				ODCA[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – ODCA[4:0] PORTA Open-Drain Enable bits

Value	Description
1	Open-drain is enabled on the PORTA pin.
0	Open-drain is disabled on the PORTA pin.

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8.2.2.6. Change Notification Pull-up Enable for PORTA Register

Name: CNPUA
Offset: 0xE0A

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				CNPUA[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – CNPUA[4:0] Change Notification Pull-up Enable for PORTA bits

Value	Description
1	The pull-up for PORTx[n] is enabled – takes precedence over the pull-down selection.
0	The pull-up for PORTx[n] is disabled.

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8.2.2.7. Change Notification Pull-Down Enable for PORTA Register

Name: CNPDA
Offset: 0xE0C

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				CNPDA[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – CNPDA[4:0] Change Notification Pull-Down Enable for PORTA bits

Value	Description
1	The pull-down for PORTx[n] is enabled (if the pull-up for PORTx[n] is not enabled).
0	The pull-down for PORTx[n] is disabled.

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8.2.2.8. Change Notification Control for PORTA Register

Name: CNCONA
Offset: 0xE0E

Bit	15	14	13	12	11	10	9	8
	ON				CNSTYLE			
Access	R/W				R/W			
Reset	0				0			

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – ON Change Notification (CN) Control for PORTA On bit

Value	Description
1	CN is enabled.
0	CN is disabled.

Bit 11 – CNSTYLE Change Notification Style Selection bit

Value	Description
1	Edge style (detects edge transitions, CNFx[15:0] bits are used for a Change Notification event).
0	Mismatch style (detects change from the last port read, CNSTATx[15:0] bits are used for a Change Notification event).

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8.2.2.9. Interrupt Change Notification Enable for PORTA Register

Name: CNEN0A
Offset: 0xE10

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				CNEN0A[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – CNEN0A[4:0] Interrupt Change Notification Enable for PORTA bits

Value	Description
1	Interrupt-on-change (from the last read value) is enabled for PORTx[n].
0	Interrupt-on-change is disabled for PORTx[n].

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8.2.2.10. Interrupt Change Notification Status for PORTA Register

Name: CNSTATA
Offset: 0xE12

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				CNSTATA[4:0]				
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bits 4:0 – CNSTATA[4:0] Interrupt Change Notification Status for PORTA bits
When CNSTYLE (CNCONx[11]) = 0:

Value	Description
1	Change occurred on PORTx[n] since last read of PORTx[n].
0	Change did not occur on PORTx[n] since last read of PORTx[n].

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8.2.2.11. Interrupt Change Notification Edge Select for PORTA Register

Name: CNEN1A
Offset: 0xE14

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				CNEN1A[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – CNEN1A[4:0] Interrupt Change Notification Edge Select for PORTA bits

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8.2.2.12. Interrupt Change Notification Flag for PORTA Register

Name: CNFA
Offset: 0xE16

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				CNFA[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – CNFA[4:0] Interrupt Change Notification Flag for PORTA bits
When CNSTYLE (CNCONx[11]) = 1:

Value	Description
1	An enabled edge event occurred on the PORTx[n] pin.
0	An enabled edge event did not occur on the PORTx[n] pin.

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8.2.2.13. Analog Select for PORTB Register

Name: ANSELB
Offset: 0xE1C

Bit	15	14	13	12	11	10	9	8
							ANSELB[9:7]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	ANSELB[9:7]			ANSELB[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	1			1	1	1	1	1

Bits 9:7 – ANSELB[9:7] Analog Select for PORTx bits

Value	Description
1	Analog input is enabled and digital input is disabled on the PORTx[n] pin.
0	Analog input is disabled and digital input is enabled on the PORTx[n] pin.

Bits 4:0 – ANSELB[4:0] Analog Select for PORTx bits

Value	Description
1	Analog input is enabled and digital input is disabled on the PORTx[n] pin.
0	Analog input is disabled and digital input is enabled on the PORTx[n] pin.

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8.2.2.14. Output Enable for PORTB Register

Name: TRISB
Offset: 0xE1E

Bit	15	14	13	12	11	10	9	8
	TRISB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRISB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 15:0 – TRISB[15:0] Output Enable for PORTB bits

Value	Description
1	LATx[n] is not driven on the PORTx[n] pin.
0	LATx[n] is driven on the PORTx[n] pin.

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8.2.2.15. Input Data for PORTB Register

Name: PORTB
Offset: 0xE20

Bit	15	14	13	12	11	10	9	8
	RB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 15:0 – RB[15:0] PORTB Data Input Value bits

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8.2.2.16. Output Data for PORTB Register

Name: LATB
Offset: 0xE22

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
	LATB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LATB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – LATB[15:0] PORTB Data Output Value bits

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8.2.2.17. Open-Drain Enable for PORTB Register

Name: ODCB
Offset: 0xE24

Bit	15	14	13	12	11	10	9	8
	ODCB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ODCB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ODCB[15:0] PORTB Open-Drain Enable bits

Value	Description
1	Open-drain is enabled on the PORTB pin.
0	Open-drain is disabled on the PORTB pin.

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8.2.2.18. Change Notification Pull-up Enable for PORTB Register

Name: CNPUB
Offset: 0xE26

Bit	15	14	13	12	11	10	9	8
	CNPUB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNPUB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNPUB[15:0] Change Notification Pull-up Enable for PORTB bits

Value	Description
1	The pull-up for PORTx[n] is enabled – takes precedence over the pull-down selection.
0	The pull-up for PORTx[n] is disabled.

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8.2.2.19. Change Notification Pull-Down Enable for PORTB Register

Name: CNPDB
Offset: 0xE28

Bit	15	14	13	12	11	10	9	8
	CNPDB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNPDB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNPDB[15:0] Change Notification Pull-Down Enable for PORTB bits

Value	Description
1	The pull-down for PORTx[n] is enabled (if the pull-up for PORTx[n] is not enabled).
0	The pull-down for PORTx[n] is disabled.

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8.2.2.20. Change Notification Control for PORTB Register

Name: CNCONB
Offset: 0xE2A

Bit	15	14	13	12	11	10	9	8
	ON				CNSTYLE			
Access	R/W				R/W			
Reset	0				0			

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – ON Change Notification (CN) Control for PORTB On bit

Value	Description
1	CN is enabled.
0	CN is disabled.

Bit 11 – CNSTYLE Change Notification Style Selection bit

Value	Description
1	Edge style (detects edge transitions, CNFx[15:0] bits are used for a Change Notification event).
0	Mismatch style (detects change from last port read, CNSTATx[15:0] bits are used for a Change Notification event).

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8.2.2.21. Interrupt Change Notification Enable for PORTB Register

Name: CNEN0B
Offset: 0xE2C

Bit	15	14	13	12	11	10	9	8
	CNEN0B[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNEN0B[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNEN0B[15:0] Interrupt Change Notification Enable for PORTB bits

Value	Description
1	Interrupt-on-change (from the last read value) is enabled for PORTx[n].
0	Interrupt-on-change is disabled for PORTx[n].

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8.2.2.22. Interrupt Change Notification Status for PORTB Register

Name: CNSTATB
Offset: 0xE2E

Bit	15	14	13	12	11	10	9	8
	CNSTATB[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNSTATB[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNSTATB[15:0] Interrupt Change Notification Status for PORTB bits
When CNSTYLE (CNCONx[11]) = 0:

Value	Description
1	Change occurred on PORTx[n] since last read of PORTx[n].
0	Change did not occur on PORTx[n] since last read of PORTx[n].

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8.2.2.23. Interrupt Change Notification Edge Select for PORTB Register

Name: CNEN1B
Offset: 0xE30

Bit	15	14	13	12	11	10	9	8
	CNEN1B[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNEN1B[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNEN1B[15:0] Interrupt Change Notification Edge Select for PORTB bits

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8.2.2.24. Interrupt Change Notification Flag for PORTB Register

Name: CNFB
Offset: 0xE32

Bit	15	14	13	12	11	10	9	8
	CNFB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNFB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

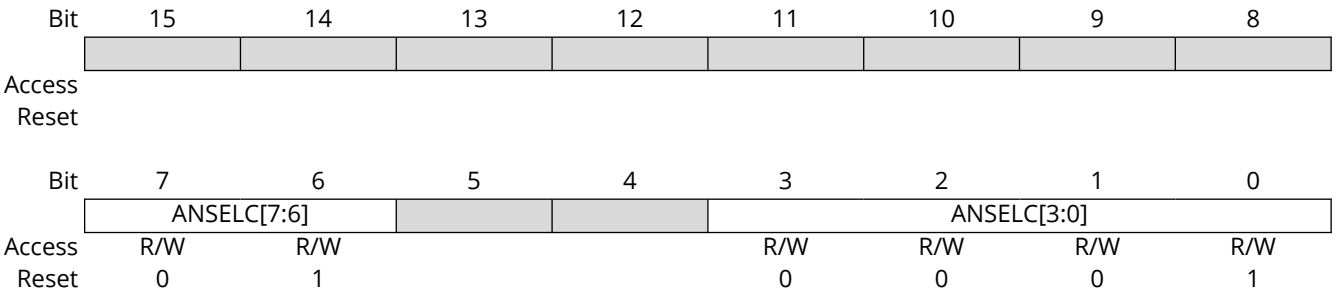
Bits 15:0 – CNFB[15:0] Interrupt Change Notification Flag for PORTB bits
When CNSTYLE (CNCONx[11]) = 1:

Value	Description
1	An enabled edge event occurred on the PORTx[n] pin.
0	An enabled edge event did not occur on the PORTx[n] pin.

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8.2.2.25. Analog Select for PORTC Register

Name: ANSELC
Offset: 0xE38



Bits 7:6 – ANSELC[7:6] Analog Select for PORTC bits

Value	Description
1	Analog input is enabled and digital input is disabled on the PORTx[n] pin.
0	Analog input is disabled and digital input is enabled on the PORTx[n] pin.

Bits 3:0 – ANSELC[3:0] Analog Select for PORTC bits

Value	Description
1	Analog input is enabled and digital input is disabled on the PORTx[n] pin.
0	Analog input is disabled and digital input is enabled on the PORTx[n] pin.

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8.2.2.26. Output Enable for PORTC Register

Name: TRISC
Offset: 0xE3A

Bit	15	14	13	12	11	10	9	8
	TRISC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRISC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 15:0 – TRISC[15:0] Output Enable for PORTC bits

Value	Description
1	LATx[n] is not driven on the PORTx[n] pin.
0	LATx[n] is driven on the PORTx[n] pin.

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8.2.2.27. Input Data for PORTC Register

Name: PORTC(1)
Offset: 0xE3C

Notes:

1. PORTC is not available on 28-pin devices.
2. 36-pin devices only have pins RC0 to RC5.
3. 48-pin devices only have pins RC0 to RC13.

Bit	15	14	13	12	11	10	9	8
	RC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 15:0 – RC[15:0] PORTC Data Input Value bits(2,3)

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8.2.2.28. Output Data for PORTC Register

Name: LATC
Offset: 0xE3E

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
	LATC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LATC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – LATC[15:0] PORTC Data Output Value bits

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8.2.2.29. Open-Drain Enable for PORTC Register

Name: ODCC
Offset: 0xE40

Bit	15	14	13	12	11	10	9	8
	ODCC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ODCC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ODCC[15:0] PORTC Open-Drain Enable bits

Value	Description
1	Open-drain is enabled on the PORTC pin.
0	Open-drain is disabled on the PORTC pin.

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8.2.2.30. Change Notification Pull-up Enable for PORTC Register

Name: CNPUC
Offset: 0xE42

Bit	15	14	13	12	11	10	9	8
	CNPUC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNPUC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNPUC[15:0] Change Notification Pull-up Enable for PORTC bits

Value	Description
1	The pull-up for PORTx[n] is enabled – takes precedence over the pull-down selection.
0	The pull-up for PORTx[n] is disabled.

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8.2.2.31. Change Notification Pull-Down Enable for PORTC Register

Name: CNPDC
Offset: 0xE44

Bit	15	14	13	12	11	10	9	8
	CNPDC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNPDC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNPDC[15:0] Change Notification Pull-Down Enable for PORTC bits

Value	Description
1	The pull-down for PORTx[n] is enabled (if the pull-up for PORTx[n] is not enabled).
0	The pull-down for PORTx[n] is disabled.

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8.2.2.32. Change Notification Control for PORTC Register

Name: CNCONC
Offset: 0xE46

Bit	15	14	13	12	11	10	9	8
	ON				CNSTYLE			
Access	R/W				R/W			
Reset	0				0			

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – ON Change Notification (CN) Control for PORTC On bit

Value	Description
1	CN is enabled.
0	CN is disabled.

Bit 11 – CNSTYLE Change Notification Style Selection bit

Value	Description
1	Edge style (detects edge transitions, CNFx[15:0] bits are used for a Change Notification event).
0	Mismatch style (detects change from last port read, CNSTATx[15:0] bits are used for a Change Notification event).

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8.2.2.33. Interrupt Change Notification Enable for PORTC Register

Name: CNEN0C
Offset: 0xE48

Bit	15	14	13	12	11	10	9	8
	CNEN0C[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNEN0C[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNEN0C[15:0] Interrupt Change Notification Enable for PORTC bits

Value	Description
1	Interrupt-on-change (from the last read value) is enabled for PORTx[n].
0	Interrupt-on-change is disabled for PORTx[n].

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8.2.2.34. Interrupt Change Notification Status for PORTC Register

Name: CNSTATC
Offset: 0xE4A

Bit	15	14	13	12	11	10	9	8
	CNSTATC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNSTATC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNSTATC[15:0] Interrupt Change Notification Status for PORTC bits
When CNSTYLE (CNCONx[11]) = 0:

Value	Description
1	Change occurred on PORTx[n] since last read of PORTx[n].
0	Change did not occur on PORTx[n] since last read of PORTx[n].

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8.2.2.35. Interrupt Change Notification Edge Select for PORTC Register

Name: CNEN1C
Offset: 0xE4C

Bit	15	14	13	12	11	10	9	8
	CNEN1C[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNEN1C[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNEN1C[15:0] Interrupt Change Notification Edge Select for PORTC bits

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8.2.2.36. Interrupt Change Notification Flag for PORTC Register

Name: CNFC
Offset: 0xE4E

Bit	15	14	13	12	11	10	9	8
	CNFC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNFC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNFC[15:0] Interrupt Change Notification Flag for PORTC bits
When CNSTYLE (CNCONx[11]) = 1:

Value	Description
1	An enabled edge event occurred on the PORTx[n] pin.
0	An enabled edge event did not occur on the PORTx[n] pin.

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8.2.2.37. Analog Select for PORTD Register

Name: ANSELD
Offset: 0xE54

Bit	15	14	13	12	11	10	9	8
			ANSELD13		ANSELD[11:10]			
Access			R/W		R/W	R/W		
Reset			1		0	1		

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 13 – ANSELD13 Analog Select for PORTD bit

Value	Description
1	Analog input is enabled and digital input is disabled on the PORTx[n] pin.
0	Analog input is disabled and digital input is enabled on the PORTx[n] pin.

Bits 11:10 – ANSELD[11:10] Analog Select for PORTD bits

Value	Description
1	Analog input is enabled and digital input is disabled on the PORTx[n] pin.
0	Analog input is disabled and digital input is enabled on the PORTx[n] pin.

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8.2.2.38. Output Enable for PORTD Register

Name: TRISD
Offset: 0xE56

Bit	15	14	13	12	11	10	9	8
	TRISD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRISD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 15:0 – TRISD[15:0] Output Enable for PORTD bits

Value	Description
1	LATx[n] is not driven on the PORTx[n] pin.
0	LATx[n] is driven on the PORTx[n] pin.

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8.2.2.39. Input Data for PORTD Register

Name: PORTD(1)
Offset: 0xE58

Notes:

1. PORTD is not available on 28 and 36-pin devices.
2. 48-pin devices only have RD0, RD8, RD10 and RD13.

Bit	15	14	13	12	11	10	9	8
	RD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 15:0 – RD[15:0] PORTD Data Input Value bits(2)

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8.2.2.40. Output Data for PORTD Register

Name: LATD
Offset: 0xE5A

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
	LATD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	LATD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 15:0 – LATD[15:0] PORTD Data Output Value bits

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8.2.2.41. Open-Drain Enable for PORTD Register

Name: ODCD
Offset: 0xE5C

Bit	15	14	13	12	11	10	9	8
	ODCD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ODCD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ODCD[15:0] PORTD Open-Drain Enable bits

Value	Description
1	Open-drain is enabled on the PORTD pin.
0	Open-drain is disabled on the PORTD pin.

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8.2.2.42. Change Notification Pull-up Enable for PORTD Register

Name: CNPUD
Offset: 0xE5E

Bit	15	14	13	12	11	10	9	8
	CNPUD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNPUD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNPUD[15:0] Change Notification Pull-up Enable for PORTD bits

Value	Description
1	The pull-up for PORTx[n] is enabled – takes precedence over the pull-down selection.
0	The pull-up for PORTx[n] is disabled.

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8.2.2.43. Change Notification Pull-Down Enable for PORTD Register

Name: CNPDD
Offset: 0xE60

Bit	15	14	13	12	11	10	9	8
	CNPDD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNPDD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNPDD[15:0] Change Notification Pull-Down Enable for PORTD bits

Value	Description
1	The pull-down for PORTx[n] is enabled (if the pull-up for PORTx[n] is not enabled).
0	The pull-down for PORTx[n] is disabled.

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8.2.2.44. Change Notification Control for PORTD Register

Name: CNCOND
Offset: 0xE62

Bit	15	14	13	12	11	10	9	8
	ON				CNSTYLE			
Access	R/W				R/W			
Reset	0				0			

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – ON Change Notification (CN) Control for PORTD On bit

Value	Description
1	CN is enabled.
0	CN is disabled.

Bit 11 – CNSTYLE Change Notification Style Selection bit

Value	Description
1	Edge style (detects edge transitions, CNFx[15:0] bits are used for a Change Notification event).
0	Mismatch style (detects change from last port read, CNSTATx[15:0] bits are used for a Change Notification event).

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8.2.2.45. Interrupt Change Notification Enable for PORTD Register

Name: CNEN0D
Offset: 0xE64

Bit	15	14	13	12	11	10	9	8
	CNEN0D[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNEN0D[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNEN0D[15:0] Interrupt Change Notification Enable for PORTD bits

Value	Description
1	Interrupt-on-change (from the last read value) is enabled for PORTx[n].
0	Interrupt-on-change is disabled for PORTx[n].

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8.2.2.46. Interrupt Change Notification Status for PORTD Register

Name: CNSTATD
Offset: 0xE66

Bit	15	14	13	12	11	10	9	8
	CNSTATD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNSTATD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNSTATD[15:0] Interrupt Change Notification Status for PORTD bits
When CNSTYLE (CNCONx[11]) = 0:

Value	Description
1	Change occurred on PORTx[n] since last read of PORTx[n].
0	Change did not occur on PORTx[n] since last read of PORTx[n].

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8.2.2.47. Interrupt Change Notification Edge Select for PORTD Register

Name: CNEN1D
Offset: 0xE68

Bit	15	14	13	12	11	10	9	8
	CNEN1D[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNEN1D[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNEN1D[15:0] Interrupt Change Notification Edge Select for PORTD bits

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8.2.2.48. Interrupt Change Notification Flag for PORTD Register

Name: CNFD
Offset: 0xE6A

Bit	15	14	13	12	11	10	9	8
	CNFD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNFD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNFD[15:0] Interrupt Change Notification Flag for PORTD bits
When CNSTYLE (CNCONx[11]) = 1:

Value	Description
1	An enabled edge event occurred on the PORTx[n] pin.
0	An enabled edge event did not occur on the PORTx[n] pin.

8.3. Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows the dsPIC33CDVL256MC506 family devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States, even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State. Five control registers are associated with the Change Notification (CN) functionality of each I/O port. To enable the Change Notification feature for the port, the ON bit (CNCONx[15]) must be set.

The CNEN0x and CNEN1x registers contain the CN interrupt enable control bits for each of the input pins. The setting of these bits enables a CN interrupt for the corresponding pins. Also, these bits—in combination with the CNSTYLE bit (CNCONx[11])—define the type of transition when the interrupt is generated. Possible CN event options are listed in Table 8-3.

Table 8-3. Change Notification Event Options

CNSTYLE Bit (CNCONx[11])	CNEN1x Bit	CNEN0x Bit	Change Notification Event Description
0	Does not matter	0	Disabled
0	Does not matter	1	Detects a mismatch between the last read state and the current state of the pin.
1	0	0	Disabled
1	0	1	Detects a positive transition only (from '0' to '1').
1	1	0	Detects a negative transition only (from '1' to '0').
1	1	1	Detects both positive and negative transitions.

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The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit. In addition to the CNSTATx register, the CNFx register is implemented for each port. This register contains flags for Change Notification events. These flags are set if the valid transition edge (selected in the CNEN0x and CNEN1x registers) is detected. CNFx stores the occurrence of the event. CNFx bits must be cleared in software to get the next Change Notification interrupt. The CN interrupt is generated only for the I/Os configured as inputs (corresponding TRISx bits must be set).

Note: Pull-ups and pull-downs on Input Change Notification pins should always be disabled when the port pin is configured as a digital output.

8.4. Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features, while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

8.4.1. Available Pins

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, “RPn”, in their full pin designation, where “n” is the remappable pin number. “RP” is used to designate pins that support both remappable input and output functions.

8.4.2. Available Peripherals

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general-purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. One example includes I^2C modules. A similar requirement excludes all modules with analog inputs, such as the A/D Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/Os and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

8.4.3. Controlling Configuration Changes

Because peripheral mapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. The dsPIC33CDVL256MC506 devices implement a control register lock sequence.

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8.4.3.1. Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes will appear to execute normally, but the contents of the registers will remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (RPCON[11]). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, the NVMKEY unlock sequence must be executed:

1. Write 0x55 to NVMKEY.
2. Write 0xAA to NVMKEY.
3. Clear (or set) IOLOCK as a single operation.

IOLOCK remains in one state until changed. This allows all of the Peripheral Pin Selects to be configured with a single unlock sequence, followed by an update to all of the control registers. Then, IOLOCK can be set with a second lock sequence.

Note: MPLAB® XC16 provides a built-in C language function for unlocking and modifying the RPCON register:

```
__builtin_write_RPCON(value);
```

For more information, see the MPLAB® XC16 Help files.

8.5. Considerations for Peripheral Pin Selection

The ability to control Peripheral Pin Selection introduces several considerations into application design that most users would never think of otherwise. This is particularly true for several common peripherals, which are only available as remappable peripherals.

The main consideration is that the Peripheral Pin Selects are not available on default pins in the device's default (Reset) state. More specifically, because all RPINRx registers reset to '1's and RPORx registers reset to '0's, this means all PPS inputs are tied to V_{SS}, while all PPS outputs are disconnected. This means that before any other application code is executed, the user must initialize the device with the proper peripheral configuration. Because the IOLOCK bit resets in the unlocked state, it is not necessary to execute the unlock sequence after the device has come out of Reset. For application safety, however, it is always better to set IOLOCK and lock the configuration after writing to the control registers.

The NVMKEY unlock sequence must be executed as an Assembly language routine. If the bulk of the application is written in C, or another high-level language, the unlock sequence should be performed by writing in-line assembly or by using the `__builtin_write_RPCON(value)` function provided by the compiler.

Choosing the configuration requires a review of all Peripheral Pin Selects and their pin assignments, particularly those that will not be used in the application. In all cases, unused pin-selectable peripherals should be disabled completely. Unused peripherals should have their inputs assigned to an unused RPn pin function. I/O pins with unused RPn functions should be configured with the null peripheral output.

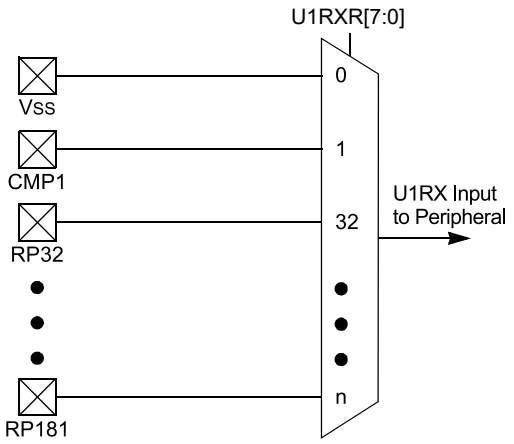
8.6. Input Mapping

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping. Each register contains sets of 8-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 8-bit index value maps the RPn pin with the corresponding value, or internal signal, to that peripheral. See Table 8-4 for a list of available inputs.

For example, Figure 8-2 illustrates remappable pin selection for the U1RX input.

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Figure 8-2. Remappable Input for U1RX



Example 8-1 provides a configuration for bidirectional communication with flow control using UART1. The following input and output functions are used:

- Input Functions: U1RX, $\overline{U1CTS}$
- Output Functions: U1TX, $\overline{U1RTS}$

Table 8-4. Remappable Pin Inputs

RPINRx[15:8] or RPINRx[7:0]	Function	Available on Ports
0	V_{SS}	Internal
1	Comparator 1	Internal
2	Comparator 2	Internal
3-5	RP3-RP5	Reserved
6	PTG Trigger 26	Internal
7	PTG Trigger 27	Internal
8-10	RP8-RP10	Reserved
11	PWM Event Out C	Internal
12	PWM Event Out D	Internal
13	PWM Event Out E	Internal
14-31	RP14-RP31	Reserved
32	RP32	Port Pin RB0
33	RP33	Port Pin RB1
34	RP34	Port Pin RB2
35	RP35	Port Pin RB3
36	RP36	Port Pin RB4
37	RP37	Port Pin RB5
38	RP38	Port Pin RB6
39	RP39	Port Pin RB7
40	RP40	Port Pin RB8
41	RP41	Port Pin RB9
42	RP42	Port Pin RB10
43	RP43	Port Pin RB11
44	RP44	Port Pin RB12
45	RP45	Port Pin RB13

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Table 8-4. Remappable Pin Inputs (continued)

RPINRx[15:8] or RPINRx[7:0]	Function	Available on Ports
46	RP46	Port Pin RB14
47	RP47	Port Pin RB15
48	RP48	Port Pin RC0
49	RP49	Port Pin RC1
50	RP50	Port Pin RC2
51	RP51	Port Pin RC3
52	RP52	Port Pin RC4
53	RP53	Port Pin RC5
54	RP54	Port Pin RC6
55	RP55	Port Pin RC7
56	RP56	Port Pin RC8
57	RP57	Port Pin RC9
58	RP58	Port Pin RC10
59	RP59	Port Pin RC11
60	RP60	Port Pin RC12
61	RP61	Port Pin RC13
62	RP62	Port Pin RC14
63	RP63	Port Pin RC15
64	RP64	Port Pin RD0
65	RP65	Port Pin RD1
66	RP66	Port Pin RD2
67	RP67	Port Pin RD3
68	RP68	Port Pin RD4
69	RP69	Port Pin RD5
70	RP70	Port Pin RD6
71	RP71	Port Pin RD7
72	RP72	Port Pin RD8
73	RP73	Port Pin RD9
74	RP74	Port Pin RD10
75	RP75	Port Pin RD11
76	RP76	Port Pin RD12
77	RP77	Port Pin RD13
78	RP78	Port Pin RD14
79	RP79	Port Pin RD15
80-165	RP80-RP165	Reserved
166	DAC2 pwm_req_on	Internal
167	DAC2 pwm_req_off	Internal
168	DAC1 pwm_req_on	Internal
169	DAC1 pwm_req_off	Internal
170-175	RP170-RP175	Reserved
176	RP176	Virtual RPV0
177	RP177	Virtual RPV1
178	RP178	Virtual RPV2
179	RP179	Virtual RPV3
180	RP180	Virtual RPV4

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Table 8-4. Remappable Pin Inputs (continued)

RPINRx[15:8] or RPINRx[7:0]	Function	Available on Ports
181	RP181	Virtual RPV5

Table 8-5. Selectable Input Sources (Maps Input to Function)

Input Name(1)	Function Name	Register	Register Bits
External Interrupt 1	INT1	RPINR0	INT1R[7:0]
External Interrupt 2	INT2	RPINR1	INT2R[7:0]
External Interrupt 3	INT3	RPINR1	INT3R[7:0]
Timer1 External Clock	T1CK	RPINR2	T1CK[7:0]
SCCP Timer1	TCKI1	RPINR3	TCKI1R[7:0]
SCCP Capture 1	ICM1	RPINR3	ICM1R[7:0]
SCCP Timer2	TCKI2	RPINR4	TCKI2R[7:0]
SCCP Capture 2	ICM2	RPINR4	ICM2R[7:0]
SCCP Timer3	TCKI3	RPINR5	TCKI3R[7:0]
SCCP Capture 3	ICM3	RPINR5	ICM3R[7:0]
SCCP Timer4	TCKI4	RPINR6	TCKI4R[7:0]
SCCP Capture 4	ICM4	RPINR6	ICM4R[7:0]
SCCP Fault A	OCFA	RPINR11	OCFAR[7:0]
SCCP Fault B	OCFB	RPINR11	OCFBR[7:0]
PWM PCI Input 8	PCI8	RPINR12	PCI8R[7:0]
PWM PCI Input 9	PCI9	RPINR12	PCI9R[7:0]
PWM PCI Input 10	PCI10	RPINR13	PCI10R[7:0]
PWM PCI Input 11	PCI11	RPINR13	PCI11R[7:0]
QEI1 Input A	QEIA1	RPINR14	QEIA1R[7:0]
QEI1 Input B	QEIB1	RPINR14	QEIB1R[7:0]
QEI1 Index 1 Input	QEINDX1	RPINR15	QEINDX1R[7:0]
QEI1 Home 1 Input	QEIHOM1	RPINR15	QEIHOM1R[7:0]
UART1 Receive	U1RX	RPINR18	U1RXR[7:0]
UART1 Data-Set-Ready	$\overline{\text{U1DSR}}$	RPINR18	U1DSRR[7:0]
UART2 Receive	U2RX	RPINR19	U2RXR[7:0]
UART2 Data-Set-Ready	U2DSR	RPINR19	U2DSRR[7:0]
SPI1 Data Input	SDI1	RPINR20	SDI1R[7:0]
SPI1 Clock Input	SCK1IN	RPINR20	SCK1R[7:0]
SPI1 Client Select	$\overline{\text{SS1}}$	RPINR21	SS1R[7:0]
Reference Clock Input	REFCLKI	RPINR21	REFOIR[7:0]
SPI2 Data Input	SDI2	RPINR22	SDI2R[7:0]
SPI2 Clock Input	SCK2IN	RPINR22	SCK2R[7:0]
SPI2 Client Select	$\overline{\text{SS2}}$	RPINR23	SS2R[7:0]
CAN1 Input (CAN1RX)	CAN1RX	RPINR26	CAN1RXR[7:0]
UART3 Receive	U3RX	RPINR27	U3RXR[7:0]
UART3 Data-Set-Ready	$\overline{\text{U3DSR}}$	RPINR27	U3DSRR[7:0]
SCCP Fault C	OCFC	RPINR37	OCFCR[7:0]
PWM PCI Input 17	PCI17	RPINR37	PCI17R[7:0]
PWM PCI Input 18	PCI18	RPINR38	PCI18R[7:0]
PWM PCI Input 12	PCI12	RPINR42	PCI12R[7:0]
PWM PCI Input 13	PCI13	RPINR42	PCI13R[7:0]

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Table 8-5. Selectable Input Sources (Maps Input to Function) (continued)

Input Name[1]	Function Name	Register	Register Bits
PWM PCI Input 14	PCI14	RPINR43	PCI14R[7:0]
PWM PCI Input 15	PCI15	RPINR43	PCI15R[7:0]
PWM PCI Input 16	PCI16	RPINR44	PCI16R[7:0]
SENT1 Input	SENT1	RPINR44	SENT1R[7:0]
CLC Input A	CLCINA	RPINR45	CLCINAR[7:0]
CLC Input B	CLCINB	RPINR46	CLCINBR[7:0]
CLC Input C	CLCINC	RPINR46	CLCINCR[7:0]
CLC Input D	CLCIND	RPINR47	CLCINDR[7:0]
ADC Trigger Input (ADTRIG31)	ADCTRG	RPINR47	ADCTRGR[7:0]
SCCP Fault D	OCFD	RPINR48	OCFDR[7:0]
UART1 Clear-to-Send	$\overline{\text{U1CTS}}$	RPINR48	U1CTSR[7:0]
UART2 Clear-to-Send	$\overline{\text{U2CTS}}$	RPINR49	U2CTSR[7:0]
UART3 Clear-to-Send	$\overline{\text{U3CTS}}$	RPINR49	U3CTSR[7:0]

Note:

1. Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

Example 8-1. Configuring UART1 Input and Output Functions

```
//
*****************************************
// Unlock Registers
//*****************************************
__builtin_write_RPCON(0x0000);
//*****************************************
// Configure Input Functions (See Table 3-32)
// Assign U1Rx To Pin RP35
//***************************
_U1RXR = 35;
// Assign U1CTS To Pin RP36
//***************************
_U1CTSR = 36;
//*****************************************
// Configure Output Functions (See Table 3-34)
//*****************************************
// Assign U1Tx To Pin RP37
//***************************
_RP37R = 1;
//***************************
// Assign U1RTS To Pin RP38
//***************************
_RP38R = 2;
//*****************************************
// Lock Registers
//*****************************************
__builtin_write_RPCON(0x0800);
```

8.7. Virtual Connections

The dsPIC33CDVL256MC506 devices support six virtual RPn pins (RP176-RP181), which are identical in functionality to all other RPn pins, with the exception of pinouts. These six pins are internal to the devices and are not connected to a physical device pin.

These pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example, the output of the analog comparator can be connected to RP176 and the PWM Fault input can be configured for RP176 as well. This configuration allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

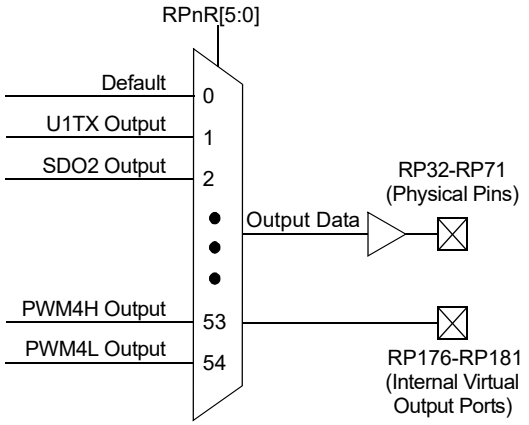
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8.8. Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Each register contains sets of 6-bit fields, with each set associated with one RPn pin (see RPINR0 through RPINR49). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 8-6 and Figure 8-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

Figure 8-3. Multiplexing Remappable Outputs for RPn



Note: There are six virtual output ports which are not connected to any I/O ports (RP176-RP181). These virtual ports can be accessed by RPOR20, RPOR21 and RPOR22.

8.9. Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally, any combination of peripheral mappings, across any or all of the RPn pins, is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs, and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view (see Table 8-6).

Table 8-6. Remappable Output Pin Registers(1)

Register	RPn Pin	I/O Port
RPOR0[5:0]	RP32	Port Pin RB0
RPOR0[13:8]	RP33	Port Pin RB1
RPOR1[5:0]	RP34	Port Pin RB2
RPOR1[13:8]	RP35	Port Pin RB3
RPOR2[5:0]	RP36	Port Pin RB4
RPOR2[13:8]	RP37	Port Pin RB5
RPOR3[5:0]	RP38	Port Pin RB6
RPOR3[13:8]	RP39	Port Pin RB7
RPOR4[5:0]	RP40	Port Pin RB8

Notes:

1. Not all RPn pins are available on all packages. Make sure the selected device variant has the feature available on the device.
2. Availability is dependent on supported I/O ports. Refer to Table 8-2 for availability on device variants.

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Table 8-6. Remappable Output Pin Registers[1] (continued)

Register	RPn Pin	I/O Port
RPOR4[13:8]	RP41	Port Pin RB9
RPOR5[5:0]	RP42	Port Pin RB10
RPOR5[13:8]	RP43	Port Pin RB11
RPOR6[5:0]	RP44	Port Pin RB12
RPOR6[13:8]	RP45	Port Pin RB13
RPOR7[5:0]	RP46	Port Pin RB14
RPOR7[13:8]	RP47	Port Pin RB15
RPOR8[5:0][2]	RP48	Port Pin RC0
RPOR8[13:8][2]	RP49	Port Pin RC1
RPOR9[5:0][2]	RP50	Port Pin RC2
RPOR9[13:8][2]	RP51	Port Pin RC3
RPOR10[5:0][2]	RP52	Port Pin RC4
RPOR10[13:8][2]	RP53	Port Pin RC5
RPOR11[5:0][2]	RP54	Port Pin RC6
RPOR11[13:8][2]	RP55	Port Pin RC7
RPOR12[5:0][2]	RP56	Port Pin RC8
RPOR12[13:8][2]	RP57	Port Pin RC9
RPOR13[5:0][2]	RP58	Port Pin RC10
RPOR13[13:8][2]	RP59	Port Pin RC11
RPOR14[5:0][2]	RP60	Port Pin RC12
RPOR14[13:8][2]	RP61	Port Pin RC13
RPOR15[5:0][2]	RP62	Port Pin RC14
RPOR15[13:8][2]	RP63	Port Pin RC15
RPOR16[5:0][2]	RP64	Port Pin RD0
RPOR16[13:8][2]	RP65	Port Pin RD1
RPOR17[5:0][2]	RP66	Port Pin RD2
RPOR17[13:8][2]	RP67	Port Pin RD3
RPOR18[5:0][2]	RP68	Port Pin RD4
RPOR18[13:8][2]	RP69	Port Pin RD5
RPOR19[5:0][2]	RP70	Port Pin RD6
RPOR19[13:8][2]	RP71	Port Pin RD7
RPOR20[5:0][2]	RP72	Port Pin RD8
RPOR20[13:8][2]	RP73	Port Pin RD9
RPOR21[5:0][2]	RP74	Port Pin RD10
RPOR21[13:8][2]	RP75	Port Pin RD11
RPOR22[5:0][2]	RP76	Port Pin RD12
RPOR22[13:8][2]	RP77	Port Pin RD13
RPOR23[5:0][2]	RP78	Port Pin RD14
RPOR23[13:8][2]	RP79	Port Pin RD15
RPOR24[5:0]	RP176	Virtual pin RPV0
RPOR24[13:8]	RP177	Virtual pin RPV1

Notes:

1. Not all RPn pins are available on all packages. Make sure the selected device variant has the feature available on the device.
2. Availability is dependent on supported I/O ports. Refer to Table 8-2 for availability on device variants.

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Table 8-6. Remappable Output Pin Registers[1] (continued)

Register	RPn Pin	I/O Port
RPOR25[5:0]	RP178	Virtual pin RPV2
RPOR25[13:8]	RP179	Virtual pin RPV3
RPOR26[5:0]	RP180	Virtual pin RPV4
RPOR26[13:8]	RP181	Virtual pin RPV5

Notes:

1. Not all RPn pins are available on all packages. Make sure the selected device variant has the feature available on the device.
2. Availability is dependent on supported I/O ports. Refer to Table 8-2 for availability on device variants.

Table 8-7. Output Selection for Remappable Pins (RPn)[1]

Function	RPnR[5:0]	Output Name
Default PORT	0	RPn tied to Default Pin
U1TX	1	RPn tied to UART1 Transmit
$\overline{\text{U1RTS}}$	2	RPn tied to UART1 Request-to-Send
U2TX	3	RPn tied to UART2 Transmit
$\overline{\text{U2RTS}}$	4	RPn tied to UART2 Request-to-Send
SDO1	5	RPn tied to SPI1 Data Output
SCK1	6	RPn tied to SPI1 Clock Output
$\overline{\text{SS1}}$	7	RPn tied to SPI1 Slave Select
SDO2	8	RPn tied to SPI2 Data Output
SCK2	9	RPn tied to SPI2 Clock Output
$\overline{\text{SS2}}$	10	RPn tied to SPI2 Slave Select
REFCLKO	14	RPn tied to Reference Clock Output
OCM1	15	RPn tied to SCCP1 Output
OCM2	16	RPn tied to SCCP2 Output
OCM3	17	RPn tied to SCCP3 Output
OCM4	18	RPn tied to SCCP4 Output
CAN1TX	21	RPn tied to CAN1 Output
CMP1	23	RPn tied to Comparator 1 Output
CMP2	24	RPn tied to Comparator 2 Output
U3TX	27	RPn tied to UART3 Transmit
$\overline{\text{U3RTS}}$	28	RPn tied to UART3 Request-to-Send
PWM4H	34	RPn tied to PWM4H Output
PWM4L	35	RPn tied to PWM4L Output
PWMEA	36	RPn tied to PWM Event A Output
PWMEB	37	RPn tied to PWM Event B Output
QEICMP	38	RPn tied to QEI Comparator Output
CLC1OUT	40	RPn tied to CLC1 Output
CLC2OUT	41	RPn tied to CLC2 Output
PWMEC	44	RPn tied to PWM Event C Output
PWMED	45	RPn tied to PWM Event D Output
PTGTRG24	46	PTG Trigger Output 24
PTGTRG25	47	PTG Trigger Output 25

Note:

1. Not all RPn pins are available on all packages. Make sure the selected device variant has the feature available on the device.

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Table 8-7. Output Selection for Remappable Pins (RPn)[1] (continued)

Function	RPnR[5:0]	Output Name
SENT1OUT	48	RPn tied to SENT1 Output
CLC3OUT	59	RPn tied to CLC3 Output
CLC4OUT	60	RPn tied to CLC4 Output
U1DTR	61	Data Terminal Ready Output 1
U2DTR	62	Data Terminal Ready Output 2
U3DTR	63	RPn tied to UART3 DTR

Note:

1. Not all RPn pins are available on all packages. Make sure the selected device variant has the feature available on the device.

8.10. I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 34-16 under “Injection Current”, have internal protection diodes to V_{DD} and V_{SS}. The term, “Injection Current”, is also referred to as “Clamp Current”. On designated pins with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or lesser than the data sheet absolute maximum ratings with respect to the V_{SS} and V_{DD} supplies. Note that when the user application forward biases either of the high or low-side internal input clamp diodes, that the resulting current being injected into the device that is clamped internally by the V_{DD} and V_{SS} power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins, by default, after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a ‘0’, regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Select for PORTx registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a ‘0’.
   Note: Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.
3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name, from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1; this indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(V_{DD} – 0.8), not V_{DD}. This value is still above the minimum V_{IH} of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the V_{OH}/I_{OH} and V_{OL}/I_{OL} DC characteristics specification. The respective I_{OH} and I_{OL} current rating only applies to maintaining the corresponding output at or above the V_{OH}, and at or below the V_{OL} levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum V_{IH}/V_{IL} levels. An I/O pin output can safely sink or source any current less than that listed in the Absolute Maximum Ratings in Electrical Characteristics of this data sheet. For example:
   V_{OH} = 2.4v @ I_{OH} = -8 mA and V_{DD} = 3.3V

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The maximum output current sourced by any 8 mA I/O pin = 12 mA.

LED source current < 12 mA is technically permitted.

6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
   a. Only one “output” function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
   b. It is possible to assign a “remappable output” function to multiple pins and externally short or tie them together for increased current drive.
   c. If any “dedicated output” function is enabled on a pin, it will take precedence over any remappable “output” function.
   d. If any “dedicated digital” (input or output) function is enabled on a pin, any number of “input” remappable functions can be mapped to the same pin.
   e. If any “dedicated analog” function(s) are enabled on a given pin, “digital input(s)” of any kind will all be disabled, although a single “digital output”, at the user’s cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input, provided there is no external analog input, such as for a Built-In Self-Test.
   f. Any number of “input” remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable “output”.
   g. The TRISx registers control only the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRISx setting. The TRISx register does not control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRISx settings, which means that the TRISx bit must be set to input for pins with only remappable input function(s) assigned.
   h. All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin has been disabled. Only the Analog Select for PORTx (ANSELx) registers control the digital input buffer, not the TRISx register. The user must disable the analog function on a pin using the Analog Select for PORTx registers in order to use any “digital input(s)” on a corresponding pin, no exceptions.

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8.11. I/O Ports Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page contains the latest updates and additional information.

8.11.1. Key Resources

- **"I/O Ports with Edge Detect"** (www.microchip.com/DS70005322) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* sections
- Development Tools

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8.11.2. Peripheral Pin Select Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0D00	RPCON	15:8					IOLOCK			
		7:0								
0x0D02 ... 0x0D03	Reserved									
0x0D04	RPINR0	15:8	INT1R[7:0]							
		7:0								
0x0D06	RPINR1	15:8	INT3R[7:0]							
		7:0	INT2R[7:0]							
0x0D08	RPINR2	15:8	T1CKR[7:0]							
		7:0								
0x0D0A	RPINR3	15:8	ICM1R[7:0]							
		7:0	TCKI1[7:0]							
0x0D0C	RPINR4	15:8	ICM2R[7:0]							
		7:0	TCKI2R[7:0]							
0x0D0E	RPINR5	15:8	ICM3R[7:0]							
		7:0	TCKI3R[7:0]							
0x0D10	RPINR6	15:8	ICM4R[7:0]							
		7:0	TCKI4R[7:0]							
0x0D12 ... 0x0D19	Reserved									
0x0D1A	RPINR11	15:8	OCFBR[7:0]							
		7:0	OCFAR[7:0]							
0x0D1C	RPINR12	15:8	PCI9R[7:0]							
		7:0	PCI8R[7:0]							
0x0D1E	RPINR13	15:8	PCI11R[7:0]							
		7:0	PCI10R[7:0]							
0x0D20	RPINR14	15:8	QEIB1R[7:0]							
		7:0	QEIA1R[7:0]							
0x0D22	RPINR15	15:8	QEIHOM1R[7:0]							
		7:0	QEINDX1R[7:0]							
0x0D24 ... 0x0D27	Reserved									
0x0D28	RPINR18	15:8	U1DSRR[7:0]							
		7:0	U1RXR[7:0]							
0x0D2A	RPINR19	15:8	U2DSRR[7:0]							
		7:0	U2RXR[7:0]							
0x0D2C	RPINR20	15:8	SCK1R[7:0]							
		7:0	SDI1R[7:0]							
0x0D2E	RPINR21	15:8	REFOIR[7:0]							
		7:0	SS1R[7:0]							
0x0D30	RPINR22	15:8	SCK2R[7:0]							
		7:0	SDI2R[7:0]							
0x0D32	RPINR23	15:8								
		7:0	SS2R[7:0]							
0x0D34 ... 0x0D37	Reserved									
0x0D38	RPINR26	15:8								
		7:0	CAN1RXR[7:0]							
0x0D3A	RPINR27	15:8	U3DSRR[7:0]							
		7:0	U3RXR[7:0]							
0x0D3C ... 0x0D4D	Reserved									
0x0D4E	RPINR37	15:8	PCI17R[7:0]							
		7:0	OCFCR[7:0]							

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Peripheral Pin Select Control Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0D50	RPINR38	15:8								
		7:0	PCI18R[7:0]							
0x0D52 ... 0x0D57	Reserved									
0x0D58	RPINR42	15:8	PCI13R[7:0]							
		7:0	PCI12R[7:0]							
0x0D5A	RPINR43	15:8	PCI15R[7:0]							
		7:0	PCI14R[7:0]							
0x0D5C	RPINR44	15:8	SENT1R[7:0]							
		7:0	PCI16[7:0]							
0x0D5E	RPINR45	15:8	CLCINAR[7:0]							
		7:0								
0x0D60	RPINR46	15:8	CLCINCR[7:0]							
		7:0	CLCINBR[7:0]							
0x0D62	RPINR47	15:8	ADCTRGR[7:0]							
		7:0	CLCINDR[7:0]							
0x0D64	RPINR48	15:8	U1CTSR[7:0]							
		7:0	OCFDR[7:0]							
0x0D66	RPINR49	15:8	U3CTSR[7:0]							
		7:0	U2CTSR[7:0]							
0x0D68 ... 0x0D7F	Reserved									
0x0D80	RPOR0	15:8			RP33R[5:0]					
		7:0			RP32R[5:0]					
0x0D82	RPOR1	15:8			RP35R[5:0]					
		7:0			RP34R[5:0]					
0x0D84	RPOR2	15:8			RP37R[5:0]					
		7:0			RP36R[5:0]					
0x0D86	RPOR3	15:8			RP39R[5:0]					
		7:0			RP38R[5:0]					
0x0D88	RPOR4	15:8			RP41R[5:0]					
		7:0			RP40R[5:0]					
0x0D8A	RPOR5	15:8			RP43R[5:0]					
		7:0			RP42R[5:0]					
0x0D8C	RPOR6	15:8			RP45R[5:0]					
		7:0			RP44R[5:0]					
0x0D8E	RPOR7	15:8			RP47R[5:0]					
		7:0			RP46R[5:0]					
0x0D90	RPOR8	15:8			RP49R[5:0]					
		7:0			RP48R[5:0]					
0x0D92	RPOR9	15:8			RP51R[5:0]					
		7:0			RP50R[5:0]					
0x0D94	RPOR10	15:8			RP53R[5:0]					
		7:0			RP52R[5:0]					
0x0D96	RPOR11	15:8			RP55R[5:0]					
		7:0			RP54R[5:0]					
0x0D98	RPOR12	15:8			RP57R[5:0]					
		7:0			RP56R[5:0]					
0x0D9A	RPOR13	15:8			RP59R[5:0]					
		7:0			RP58R[5:0]					
0x0D9C	RPOR14	15:8			RP61R[5:0]					
		7:0			RP60R[5:0]					
0x0D9E	RPOR15	15:8			RP63R[5:0]					
		7:0			RP62R[5:0]					
0x0DA0	RPOR16	15:8			RP65R[5:0]					
		7:0			RP64R[5:0]					
0x0DA2	RPOR17	15:8			RP67R[5:0]					
		7:0			RP66R[5:0]					

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Peripheral Pin Select Control Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0DA4	RPOR18	15:8			RP69R[5:0]					
		7:0			RP68R[5:0]					
0x0DA6	RPOR19	15:8			RP71R[5:0]					
		7:0			RP70R[5:0]					
0x0DA8	RPOR20	15:8			RP73R[5:0]					
		7:0			RP72R[5:0]					
0x0DAA	RPOR21	15:8			RP75R[5:0]					
		7:0			RP74R[5:0]					
0x0DAC	RPOR22	15:8			RP77R[5:0]					
		7:0			RP76R[5:0]					
0x0DAE	RPOR23	15:8			RP79R[5:0]					
		7:0			RP78R[5:0]					
0x0DB0	RPOR24	15:8			RPV1[5:0]					
		7:0			RPV0[5:0]					
0x0DB2	RPOR25	15:8			RPV3[5:0]					
		7:0			RPV2[5:0]					
0x0DB4	RPOR26	15:8			RPV5[5:0]					
		7:0			RPV4[5:0]					

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8.11.2.1. Peripheral Remapping Configuration Register

Name: RPCON(1)
Offset: 0xD00

Note:

1. Writing to this register requires an unlock sequence.

Bit	15	14	13	12	11	10	9	8
					IOLOCK			
Access					R/W			
Reset					0			

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 11 – IOLOCK Peripheral Remapping Register Lock bit

Value	Description
1	All Peripheral Remapping registers are locked and cannot be written.
0	All Peripheral Remapping registers are unlocked and can be written.

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8.11.2.2. Peripheral Pin Select Input Register 0

Name: RPINR0
Offset: 0xD04

Bit	15	14	13	12	11	10	9	8
	INT1R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 15:8 – INT1R[7:0] Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits

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8.11.2.3. Peripheral Pin Select Input Register 1

Name: RPINR1
Offset: 0xD06

Bit	15	14	13	12	11	10	9	8
	INT3R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INT2R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – INT3R[7:0] Assign External Interrupt 3 (INT3) to the Corresponding RPn Pin bits

Bits 7:0 – INT2R[7:0] Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits

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8.11.2.4. Peripheral Pin Select Input Register 2

Name: RPINR2
Offset: 0xD08

Bit	15	14	13	12	11	10	9	8
	T1CKR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 15:8 – T1CKR[7:0] Assign Timer1 External Clock (T1CK) to the Corresponding RPn Pin bits

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8.11.2.5. Peripheral Pin Select Input Register 3

Name: RPINR3
Offset: 0xD0A

Bit	15	14	13	12	11	10	9	8
	ICM1R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TCKI1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – ICM1R[7:0] Assign SCCP Capture 1 (ICM1) Input to the Corresponding RPn Pin bits

Bits 7:0 – TCKI1[7:0] Assign SCCP Timer1 (TCKI1) Input to the Corresponding RPn Pin bits

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8.11.2.6. Peripheral Pin Select Input Register 4

Name: RPINR4
Offset: 0xD0C

Bit	15	14	13	12	11	10	9	8
	ICM2R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TCKI2R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – ICM2R[7:0] Assign SCCP Capture 2 (ICM2) Input to the Corresponding RPn Pin bits

Bits 7:0 – TCKI2R[7:0] Assign SCCP Timer2 (TCKI2) Input to the Corresponding RPn Pin bits

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8.11.2.7. Peripheral Pin Select Input Register 5

Name: RPINR5
Offset: 0xD0E

Bit	15	14	13	12	11	10	9	8
	ICM3R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TCKI3R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – ICM3R[7:0] Assign SCCP Capture 3 (ICM3) Input to the Corresponding RPn Pin bits

Bits 7:0 – TCKI3R[7:0] Assign SCCP Timer3 (TCKI3) Input to the Corresponding RPn Pin bits

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8.11.2.8. Peripheral Pin Select Input Register 6

Name: RPINR6
Offset: 0xD10

Bit	15	14	13	12	11	10	9	8
	ICM4R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TCKI4R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – ICM4R[7:0] Assign SCCP Capture 4 (ICM4) Input to the Corresponding RPn Pin bits

Bits 7:0 – TCKI4R[7:0] Assign SCCP Timer4 (TCKI4) Input to the Corresponding RPn Pin bits

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8.11.2.9. Peripheral Pin Select Input Register 11

Name: RPINR11
Offset: 0xD1A

Bit	15	14	13	12	11	10	9	8
	OCFBR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OCFAR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – OCFBR[7:0] Assign SCCP Fault B (OCFB) Input to the Corresponding RPn Pin bits

Bits 7:0 – OCFAR[7:0] Assign SCCP Fault A (OCFA) Input to the Corresponding RPn Pin bits

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8.11.2.10. Peripheral Pin Select Input Register 12

Name: RPINR12
Offset: 0xD1C

Bit	15	14	13	12	11	10	9	8
	PCI9R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PCI8R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PCI9R[7:0] Assign PWM Input 9 (PCI9) to the Corresponding RPn Pin bits

Bits 7:0 – PCI8R[7:0] Assign PWM Input 8 (PCI8) to the Corresponding RPn Pin bits

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8.11.2.11. Peripheral Pin Select Input Register 13

Name: RPINR13
Offset: 0xD1E

Bit	15	14	13	12	11	10	9	8
	PCI11R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PCI10R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PCI11R[7:0] Assign PWM Input 11 (PCI11) to the Corresponding RPn Pin bits

Bits 7:0 – PCI10R[7:0] Assign PWM Input 10 (PCI10) to the Corresponding RPn Pin bits

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8.11.2.12. Peripheral Pin Select Input Register 14

Name: RPINR14
Offset: 0xD20

Bit	15	14	13	12	11	10	9	8
	QEIB1R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	QEIA1R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – QEIB1R[7:0] Assign QEI Input B (QEIB1) to the Corresponding RPn Pin bits

Bits 7:0 – QEIA1R[7:0] Assign QEI Input A (QEIA1) to the Corresponding RPn Pin bits

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8.11.2.13. Peripheral Pin Select Input Register 15

Name: RPINR15
Offset: 0xD22

Bit	15	14	13	12	11	10	9	8
	QEIHOM1R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	QEINDX1R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – QEIHOM1R[7:0] Assign QEI Home 1 Input (QEIHOM1) to the Corresponding RPn Pin bits

Bits 7:0 – QEINDX1R[7:0] Assign QEI Index 1 Input (QEINDX1) to the Corresponding RPn Pin bits

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8.11.2.14. Peripheral Pin Select Input Register 18

Name: RPINR18
Offset: 0xD28

Bit	15	14	13	12	11	10	9	8
	U1DSRR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	U1RXR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – U1DSRR[7:0] Assign UART1 Data-Set-Ready ($\overline{U1DSR}$) to the Corresponding RPn Pin bits

Bits 7:0 – U1RXR[7:0] Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits

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8.11.2.15. Peripheral Pin Select Input Register 19

Name: RPINR19
Offset: 0xD2A

Bit	15	14	13	12	11	10	9	8
	U2DSRR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	U2RXR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – U2DSRR[7:0] Assign UART2 Data-Set-Ready ($\overline{\text{U2DSR}}$) to the Corresponding RPn Pin bits

Bits 7:0 – U2RXR[7:0] Assign UART2 Receive (U2RX) to the Corresponding RPn Pin bits

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8.11.2.16. Peripheral Pin Select Input Register 20

Name: RPINR20
Offset: 0xD2C

Bit	15	14	13	12	11	10	9	8
	SCK1R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SDI1R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – SCK1R[7:0] Assign SPI1 Clock Input (SCK1IN) to the Corresponding RPn Pin bits

Bits 7:0 – SDI1R[7:0] Assign SPI1 Data Input (SDI1) to the Corresponding RPn Pin bits

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8.11.2.17. Peripheral Pin Select Input Register 21

Name: RPINR21
Offset: 0xD2E

Bit	15	14	13	12	11	10	9	8
	REFOIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SS1R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – REFOIR[7:0] Assign Reference Clock Input (REFOI) to the Corresponding RPn Pin bits

Bits 7:0 – SS1R[7:0] Assign SPI1 Client Select ($\overline{SS1}$) to the Corresponding RPn Pin bits

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8.11.2.18. Peripheral Pin Select Input Register 22

Name: RPINR22
Offset: 0xD30

Bit	15	14	13	12	11	10	9	8
	SCK2R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SDI2R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – SCK2R[7:0] Assign SPI2 Clock Input (SCK2IN) to the Corresponding RPn Pin bits

Bits 7:0 – SDI2R[7:0] Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits

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8.11.2.19. Peripheral Pin Select Input Register 23

Name: RPINR23
Offset: 0xD32

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	SS2R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – SS2R[7:0] Assign SPI2 Client Select ($\overline{SS2}$) to the Corresponding RPn Pin bits

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8.11.2.20. Peripheral Pin Select Input Register 26

Name: RPINR26
Offset: 0xD38

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	CAN1RXR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CAN1RXR[7:0] Assign CAN1 Input (CAN1RX) to the Corresponding RPn Pin bits

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8.11.2.21. Peripheral Pin Select Input Register 27

Name: RPINR27
Offset: 0xD3A

Bit	15	14	13	12	11	10	9	8
	U3DSRR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	U3RXR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – U3DSRR[7:0] Assign UART3 Data-Set-Ready ($\overline{\text{U3DSR}}$) to the Corresponding RPn Pin bits

Bits 7:0 – U3RXR[7:0] Assign UART3 Receive (U3RX) to the Corresponding RPn Pin bits

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8.11.2.22. Peripheral Pin Select Input Register 37

Name: RPINR37
Offset: 0xD4E

Bit	15	14	13	12	11	10	9	8
	PCI17R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OCFCR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PCI17R[7:0] Assign PWM Input 17 (PCI17) to the Corresponding RPn Pin bits

Bits 7:0 – OCFCR[7:0] Assign SCCP Fault C (OCFC) Input to the Corresponding RPn Pin bits

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8.11.2.23. Peripheral Pin Select Input Register 38

Name: RPINR38
Offset: 0xD50

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PCI18R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PCI18R[7:0] Assign PWM Input 18 (PCI18) to the Corresponding RPn Pin bits

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8.11.2.24. Peripheral Pin Select Input Register 42

Name: RPINR42
Offset: 0xD58

Bit	15	14	13	12	11	10	9	8
	PCI13R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PCI12R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PCI13R[7:0] Assign PWM Input 13 (PCI13) to the Corresponding RPn Pin bits

Bits 7:0 – PCI12R[7:0] Assign PWM Input 12 (PCI12) to the Corresponding RPn Pin bits

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8.11.2.25. Peripheral Pin Select Input Register 43

Name: RPINR43
Offset: 0xD5A

Bit	15	14	13	12	11	10	9	8
	PCI15R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PCI14R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PCI15R[7:0] Assign PWM Input 15 (PCI15) to the Corresponding RPn Pin bits

Bits 7:0 – PCI14R[7:0] Assign PWM Input 14 (PCI14) to the Corresponding RPn Pin bits

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8.11.2.26. Peripheral Pin Select Input Register 44

Name: RPINR44
Offset: 0xD5C

Bit	15	14	13	12	11	10	9	8
	SENT1R[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PCI16[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – SENT1R[7:0] Assign SENT1 Input (SENT1) to the Corresponding RPn Pin bits

Bits 7:0 – PCI16[7:0] Assign PWM Input 16 (PCI16) to the Corresponding RPn Pin bits

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8.11.2.27. Peripheral Pin Select Input Register 45

Name: RPINR45
Offset: 0xD5E

Bit	15	14	13	12	11	10	9	8
	CLCINAR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 15:8 – CLCINAR[7:0] Assign CLC Input A (CLCINA) to the Corresponding RPn Pin bits

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8.11.2.28. Peripheral Pin Select Input Register 46

Name: RPINR46
Offset: 0xD60

Bit	15	14	13	12	11	10	9	8
	CLCINCR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CLCINBR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – CLCINCR[7:0] Assign CLC Input C (CLCINC) to the Corresponding RPn Pin bits

Bits 7:0 – CLCINBR[7:0] Assign CLC Input B (CLCINB) to the Corresponding RPn Pin bits

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8.11.2.29. Peripheral Pin Select Input Register 47

Name: RPINR47
Offset: 0xD62

Bit	15	14	13	12	11	10	9	8
	ADCTRGR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CLCINDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – ADCTRGR[7:0] Assign ADC Trigger Input (ADCTRG) to the Corresponding RPn Pin bits

Bits 7:0 – CLCINDR[7:0] Assign CLC Input D (CLCIND) to the Corresponding RPn Pin bits

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8.11.2.30. Peripheral Pin Select Input Register 48

Name: RPINR48
Offset: 0xD64

Bit	15	14	13	12	11	10	9	8
	U1CTSR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OCFDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – U1CTSR[7:0] Assign UART1 Clear-to-Send ($\overline{U1CTS}$) to the Corresponding RPn Pin bits

Bits 7:0 – OCFDR[7:0] Assign xCCP Fault D (OCFD) to the Corresponding RPn Pin bits

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8.11.2.31. Peripheral Pin Select Input Register 49

Name: RPINR49
Offset: 0xD66

Bit	15	14	13	12	11	10	9	8
	U3CTSR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	U2CTSR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – U3CTSR[7:0] Assign UART3 Clear-to-Send ($\overline{U3CTS}$) to the Corresponding RPn Pin bits

Bits 7:0 – U2CTSR[7:0] Assign UART2 Clear-to-Send ($\overline{U2CTS}$) to the Corresponding RPn Pin bits

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8.11.2.32. Peripheral Pin Select Output Register 0

Name: RPOR0
Offset: 0xD80

Bit	15	14	13	12	11	10	9	8
			RP33R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP32R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP33R[5:0] Peripheral Output Function is Assigned to RP33 Output Pin bits

Bits 5:0 – RP32R[5:0] Peripheral Output Function is Assigned to RP32 Output Pin bits

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8.11.2.33. Peripheral Pin Select Output Register 1

Name: RPOR1
Offset: 0xD82

Bit	15	14	13	12	11	10	9	8
			RP35R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP34R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP35R[5:0] Peripheral Output Function is Assigned to RP35 Output Pin bits

Bits 5:0 – RP34R[5:0] Peripheral Output Function is Assigned to RP34 Output Pin bits

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8.11.2.34. Peripheral Pin Select Output Register 2

Name: RPOR2
Offset: 0xD84

Bit	15	14	13	12	11	10	9	8
			RP37R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP36R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP37R[5:0] Peripheral Output Function is Assigned to RP37 Output Pin bits

Bits 5:0 – RP36R[5:0] Peripheral Output Function is Assigned to RP36 Output Pin bits

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8.11.2.35. Peripheral Pin Select Output Register 3

Name: RPOR3
Offset: 0xD86

Bit	15	14	13	12	11	10	9	8
			RP39R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP38R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP39R[5:0] Peripheral Output Function is Assigned to RP39 Output Pin bits

Bits 5:0 – RP38R[5:0] Peripheral Output Function is Assigned to RP38 Output Pin bits

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8.11.2.36. Peripheral Pin Select Output Register 4

Name: RPOR4
Offset: 0xD88

Bit	15	14	13	12	11	10	9	8
			RP41R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP40R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP41R[5:0] Peripheral Output Function is Assigned to RP41 Output Pin bits

Bits 5:0 – RP40R[5:0] Peripheral Output Function is Assigned to RP40 Output Pin bits

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8.11.2.37. Peripheral Pin Select Output Register 5

Name: RPOR5
Offset: 0xD8A

Bit	15	14	13	12	11	10	9	8
			RP43R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP42R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP43R[5:0] Peripheral Output Function is Assigned to RP43 Output Pin bits

Bits 5:0 – RP42R[5:0] Peripheral Output Function is Assigned to RP42 Output Pin bits

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8.11.2.38. Peripheral Pin Select Output Register 6

Name: RPOR6
Offset: 0xD8C

Bit	15	14	13	12	11	10	9	8
			RP45R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP44R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP45R[5:0] Peripheral Output Function is Assigned to RP45 Output Pin bits

Bits 5:0 – RP44R[5:0] Peripheral Output Function is Assigned to RP44 Output Pin bits

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8.11.2.39. Peripheral Pin Select Output Register 7

Name: RPOR7
Offset: 0xD8E

Bit	15	14	13	12	11	10	9	8
			RP47R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP46R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP47R[5:0] Peripheral Output Function is Assigned to RP47 Output Pin bits

Bits 5:0 – RP46R[5:0] Peripheral Output Function is Assigned to RP46 Output Pin bits

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8.11.2.40. Peripheral Pin Select Output Register 8

Name: RPOR8
Offset: 0xD90

Bit	15	14	13	12	11	10	9	8
			RP49R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP48R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP49R[5:0] Peripheral Output Function is Assigned to RP49 Output Pin bits

Bits 5:0 – RP48R[5:0] Peripheral Output Function is Assigned to RP48 Output Pin bits

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8.11.2.41. Peripheral Pin Select Output Register 9

Name: RPOR9
Offset: 0xD92

Bit	15	14	13	12	11	10	9	8
			RP51R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP50R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP51R[5:0] Peripheral Output Function is Assigned to RP51 Output Pin bits

Bits 5:0 – RP50R[5:0] Peripheral Output Function is Assigned to RP50 Output Pin bits

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8.11.2.42. Peripheral Pin Select Output Register 10

Name: RPOR10
Offset: 0xD94

Bit	15	14	13	12	11	10	9	8
			RP53R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP52R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP53R[5:0] Peripheral Output Function is Assigned to RP53 Output Pin bits

Bits 5:0 – RP52R[5:0] Peripheral Output Function is Assigned to RP52 Output Pin bits

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8.11.2.43. Peripheral Pin Select Output Register 11

Name: RPOR11
Offset: 0xD96

Bit	15	14	13	12	11	10	9	8
			RP55R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP54R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP55R[5:0] Peripheral Output Function is Assigned to RP55 Output Pin bits

Bits 5:0 – RP54R[5:0] Peripheral Output Function is Assigned to RP54 Output Pin bits

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8.11.2.44. Peripheral Pin Select Output Register 12

Name: RPOR12
Offset: 0xD98

Bit	15	14	13	12	11	10	9	8
			RP57R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP56R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP57R[5:0] Peripheral Output Function is Assigned to RP57 Output Pin bits

Bits 5:0 – RP56R[5:0] Peripheral Output Function is Assigned to RP56 Output Pin bits

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8.11.2.45. Peripheral Pin Select Output Register 13

Name: RPOR13
Offset: 0xD9A

Bit	15	14	13	12	11	10	9	8
			RP59R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP58R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP59R[5:0] Peripheral Output Function is Assigned to RP59 Output Pin bits

Bits 5:0 – RP58R[5:0] Peripheral Output Function is Assigned to RP58 Output Pin bits

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8.11.2.46. Peripheral Pin Select Output Register 14

Name: RPOR14
Offset: 0xD9C

Bit	15	14	13	12	11	10	9	8
			RP61R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP60R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP61R[5:0] Peripheral Output Function is Assigned to RP61 Output Pin bits

Bits 5:0 – RP60R[5:0] Peripheral Output Function is Assigned to RP60 Output Pin bits

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8.11.2.47. Peripheral Pin Select Output Register 15

Name: RPOR15
Offset: 0xD9E

Bit	15	14	13	12	11	10	9	8
			RP63R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP62R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP63R[5:0] Peripheral Output Function is Assigned to RP63 Output Pin bits

Bits 5:0 – RP62R[5:0] Peripheral Output Function is Assigned to RP62 Output Pin bits

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8.11.2.48. Peripheral Pin Select Output Register 16

Name: RPOR16
Offset: 0xDA0

Bit	15	14	13	12	11	10	9	8
			RP65R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP64R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP65R[5:0] Peripheral Output Function is Assigned to RP65 Output Pin bits

Bits 5:0 – RP64R[5:0] Peripheral Output Function is Assigned to RP64 Output Pin bits

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8.11.2.49. Peripheral Pin Select Output Register 17

Name: RPOR17
Offset: 0xDA2

Bit	15	14	13	12	11	10	9	8
			RP67R[5:0]					
Access			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP66R[5:0]					
Access			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0

Bits 13:8 – RP67R[5:0] Peripheral Output Function is Assigned to RP67 Output Pin bits

Bits 5:0 – RP66R[5:0] Peripheral Output Function is Assigned to RP66 Output Pin bits

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8.11.2.50. Peripheral Pin Select Output Register 18

Name: RPOR18
Offset: 0xDA4

Bit	15	14	13	12	11	10	9	8
			RP69R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP68R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP69R[5:0] Peripheral Output Function is Assigned to RP69 Output Pin bits

Bits 5:0 – RP68R[5:0] Peripheral Output Function is Assigned to RP68 Output Pin bits

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8.11.2.51. Peripheral Pin Select Output Register 19

Name: RPOR19
Offset: 0xDA6

Bit	15	14	13	12	11	10	9	8
			RP71R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP70R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP71R[5:0] Peripheral Output Function is Assigned to RP71 Output Pin bits

Bits 5:0 – RP70R[5:0] Peripheral Output Function is Assigned to RP70 Output Pin bits

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8.11.2.52. Peripheral Pin Select Output Register 20

Name: RPOR20
Offset: 0xDA8

Bit	15	14	13	12	11	10	9	8
			RP73R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP72R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP73R[5:0] Peripheral Output Function is Assigned to RP73 Output Pin bits

Bits 5:0 – RP72R[5:0] Peripheral Output Function is Assigned to RP72 Output Pin bits

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8.11.2.53. Peripheral Pin Select Output Register 21

Name: RPOR21
Offset: 0xDAA

Bit	15	14	13	12	11	10	9	8
			RP75R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP74R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP75R[5:0] Peripheral Output Function is Assigned to RP75 Output Pin bits

Bits 5:0 – RP74R[5:0] Peripheral Output Function is Assigned to RP74 Output Pin bits

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8.11.2.54. Peripheral Pin Select Output Register 22

Name: RPOR22
Offset: 0xDAC

Bit	15	14	13	12	11	10	9	8
			RP77R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP76R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP77R[5:0] Peripheral Output Function is Assigned to RP77 Output Pin bits

Bits 5:0 – RP76R[5:0] Peripheral Output Function is Assigned to RP76 Output Pin bits

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8.11.2.55. Peripheral Pin Select Output Register 23

Name: RPOR23
Offset: 0xDAE

Bit	15	14	13	12	11	10	9	8
			RP79R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RP78R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RP79R[5:0] Peripheral Output Function is Assigned to RP79 Output Pin bits

Bits 5:0 – RP78R[5:0] Peripheral Output Function is Assigned to RP78 Output Pin bits

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8.11.2.56. Peripheral Pin Select Output Register 24

Name: RPOR24
Offset: 0xDB0

Note:
1. These are virtual output ports.

Bit	15	14	13	12	11	10	9	8
			RPV1[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RPV0[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RPV1[5:0] Peripheral Output Function is Assigned to RPV1 Output Pin bits(1)

Bits 5:0 – RPV0[5:0] Peripheral Output Function is Assigned to RPV0 Output Pin bits(1)

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8.11.2.57. Peripheral Pin Select Output Register 25

Name: RPOR25
Offset: 0xDB2

Note:

1. These are virtual output ports.

Bit	15	14	13	12	11	10	9	8
			RPV3[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RPV2[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RPV3[5:0] Peripheral Output Function is Assigned to RPV3 Output Pin bits(1)

Bits 5:0 – RPV2[5:0] Peripheral Output Function is Assigned to RPV2 Output Pin bits(1)

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8.11.2.58. Peripheral Pin Select Output Register 26

Name: RPOR26
Offset: 0xDB4

Note:

1. These are virtual output ports.

Bit	15	14	13	12	11	10	9	8
			RPV5[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			RPV4[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – RPV5[5:0] Peripheral Output Function is Assigned to RPV5 Output Pin bits(1)

Bits 5:0 – RPV4[5:0] Peripheral Output Function is Assigned to RPV4 Output Pin bits(1)

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9. Oscillator with High-Frequency PLL

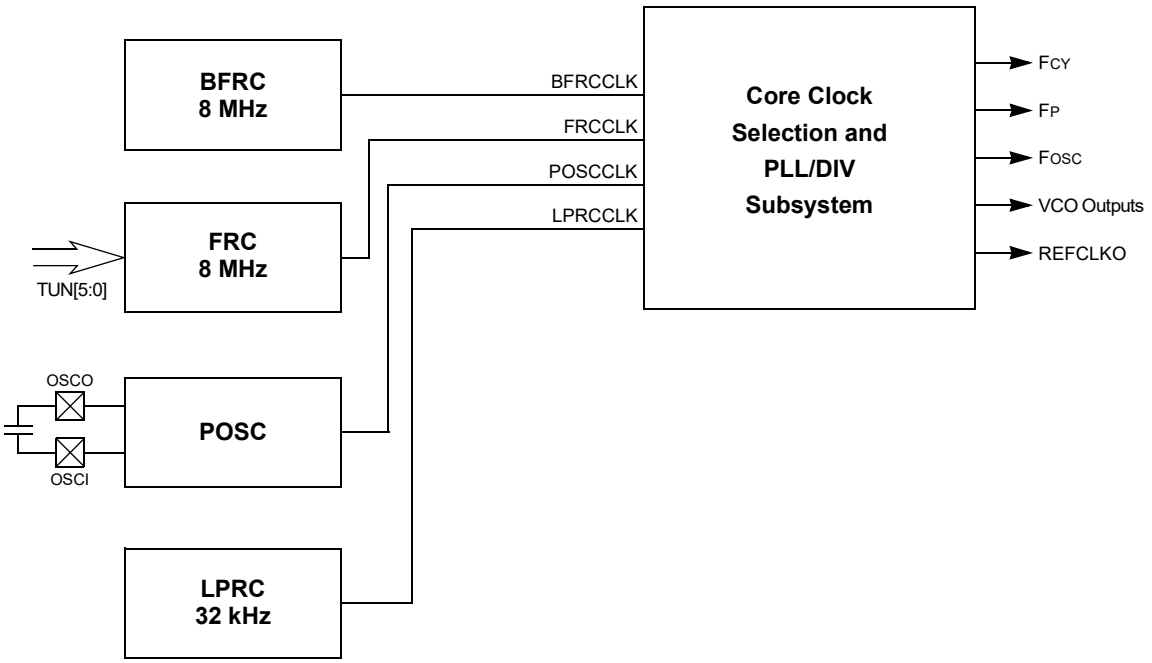
Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Oscillator Module with High-Speed PLL"** (www.microchip.com/DS70005255) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The dsPIC33CDVL256MC506 family oscillator with high-frequency PLL includes these characteristics:

- On-Chip Phase-Locked Loop (PLL) to Boost Internal Operating Frequency on Select Internal and External Oscillator Sources
- Doze mode for System Power Savings
- Scalable Reference Clock Output (REFCLKO)
- On-the-Fly Clock Switching between Various Clock Sources
- Fail-Safe Clock Monitoring (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown

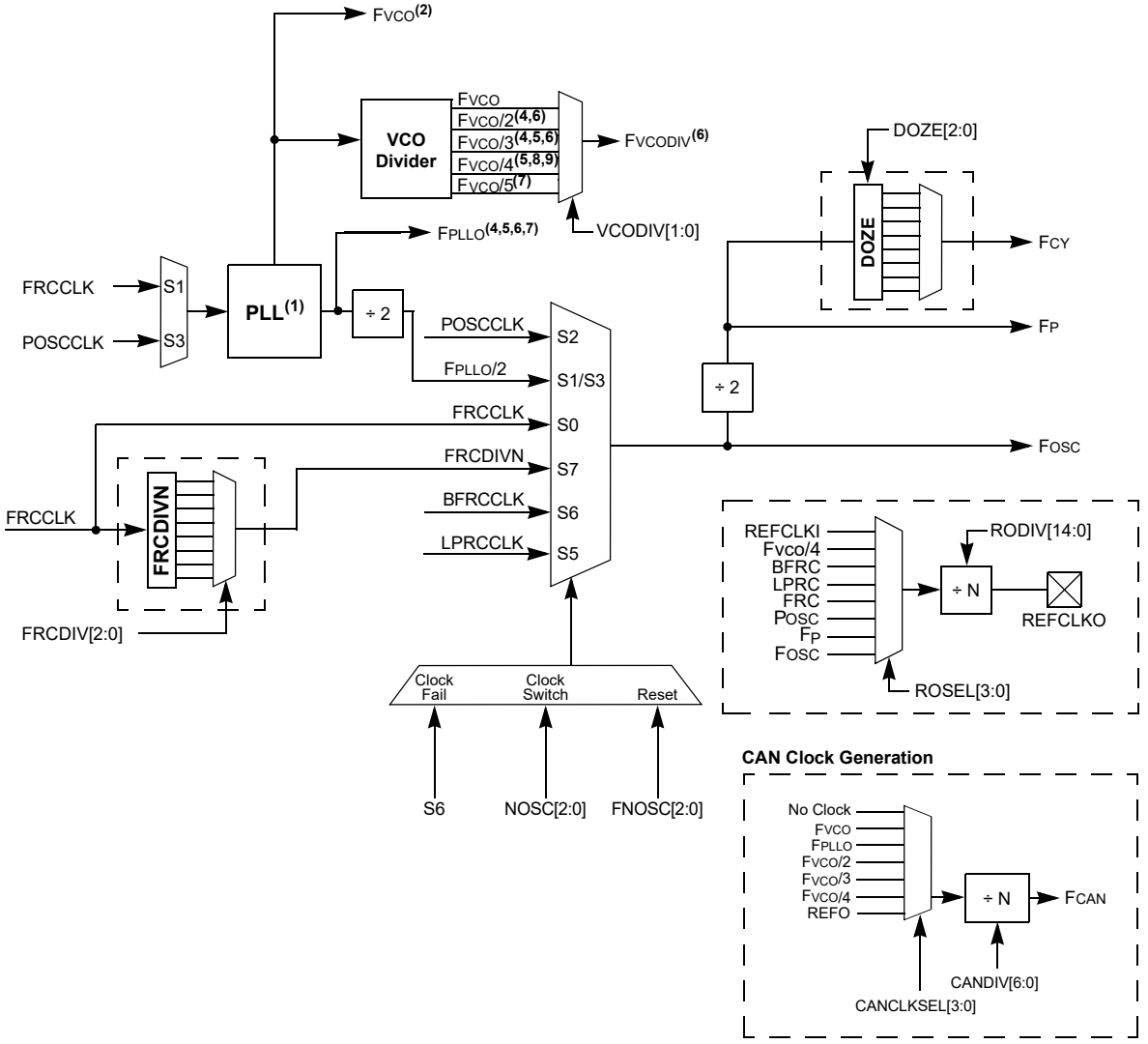
A block diagram of the dsPIC33CDVL256MC506 oscillator system is shown in Figure 9-1.

Figure 9-1. dsPIC33CDVL256MC506 Core Clock Sources Block Diagram



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Figure 9-2. dsPIC33CDVL256MC506 Oscillator Subsystem



Notes:

1. See Figure 9-3 for details of the PLL module.
2. See Figure 9-3 for the source of F_{VCO}.
3. XTPLL, HSPLL, ECPLL, FRCPLL.
4. Clock option for PWM.
5. Clock option for ADC.
6. Clock option for DAC.
7. Clock option for UART.
8. Clock option for REFO.
9. Clock option for PTG.

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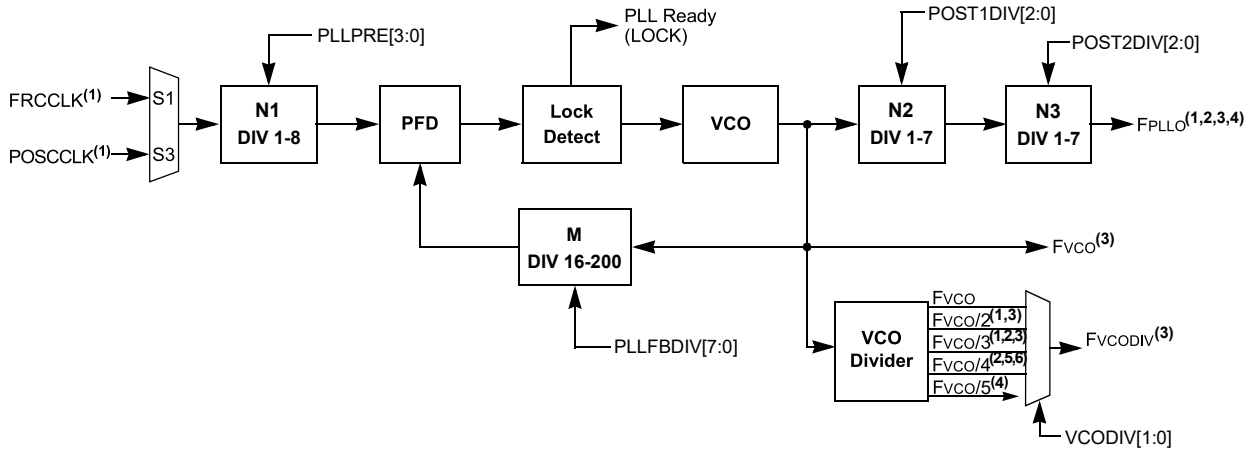
9.1. Primary PLL

The Primary Oscillator and internal FRC Oscillator sources can optionally use an on-chip PLL to obtain higher operating speeds. Figure 9-3 illustrates a block diagram of the Primary PLL module.

For PLL operation, the following requirements must be met at all times without exception:

- The PLL Input Frequency (F_{PLLI}) must be in the range of 8 MHz to 64 MHz.
- The PFD Input Frequency (F_{PFD}) must be in the range of 8 MHz to (F_{VCO}/16) MHz.
- The VCO Output Frequency (F_{VCO}) must be in the range of 400 MHz to 1600 MHz.

Figure 9-3. Primary Core PLL and VCO Detail



Notes:

1. Clock option for PWM.
2. Clock option for ADC.
3. Clock option for DAC.
4. Clock option for UART.
5. Clock option for REFO.
6. Clock option for PTG.

Equation 9-1 provides the relationship between the PLL Input Frequency (F_{PLLI}) and the VCO Output Frequency (F_{VCO}).

Equation 9-1. Primary Core F_{VCO} Calculation

$$FVCO = FPLLI \times \left(\frac{M}{N1}\right) = FPLLI \times \left(\frac{PLLFBDIV\,[7:0]}{PLLPRE\,[3:0]}\right)$$

Equation 9-2 provides the relationship between the PLL Input Frequency (F_{PLLI}) and PLL Output Frequency (F_{PLLO}).

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Equation 9-2. Primary Core F_{PLLO} Calculation

$$FPLLO = FPLLI \times \left(\frac{M}{N1 \times N2 \times N3}\right) = FPLLI \times \left(\frac{PLLFBDIV[7:0]}{PLLPRE[3:0] \times POST1DIV[2:0] \times POST2DIV[2:0]}\right)$$

Where:

$M = PLLFBDIV[7:0]$
$N1 = PLLPRE[3:0]$
$N2 = POST1DIV[2:0]$
$N3 = POST2DIV[2:0]$

Note: The PLL Phase Detector Input Divider Select (PLLPREx) bits and the PLL Feedback Divider (PLLFBDIVx) bits should not be changed when operating in PLL mode. Therefore, the user must start with either a non-PLL source or clock switch to a non-PLL source (e.g., internal FRC Oscillator) to make any necessary changes and then clock switch to the desired PLL source.
Using Two-Speed Start-up (IESO (FOSCSEL[7])) with a PLL source will start the device on the FRC while preparing the PLL. Once the PLL is ready, the device will switch automatically to the new source. This mode should not be used if changes are needed to the PLLPREx and PLLFBDIVx bits because the PLL may be running before user code execution begins.

It is not permitted to directly switch the clock from one PLL clock source to a different PLL clock source. The user would need to transition between PLL clock sources with a clock switch to a non-PLL clock source.

Example 9-1. Code Example for Using Primary PLL with 8 MHz Internal FRC

```
//code example for 50 MIPS system clock using 8MHz FRC
// Select Internal FRC at POR
_FOSCSEL(FNOSC_FRC & IESO_OFF);
// Enable Clock Switching
_FOSC(FCKSM_CSECMD);
int main()
{
// Configure PLL prescaler, both PLL postscalers, and PLL feedback divider
CLKDIVbits.PLLPRE = 1;          // N1=1
PLLFBDbits.PLLFBDIV = 125;      // M = 125
PLLDIVbits.POST1DIV = 5;        // N2=5
PLLDIVbits.POST2DIV = 1;        // N3=1
// Initiate Clock Switch to FRC with PLL (NOSC=0b001)
__builtin_write_OSCCONH(0x01);
__builtin_write_OSCCONL(OSCCON | 0x01);
// Wait for Clock switch to occur
while (OSCCONbits.OSWEN!= 0);
}
```

Note: $F_{PLLO} = F_{PLLI} * M/(N1 * N2 * N3)$; $F_{PLLI} = 8$; M = 125; N1 = 1; N2 = 5; N3 = 1; so $F_{PLLO} = 8 * 125/(1 * 5 * 1) = 200$ MHz or 50 MIPS.

9.2. CPU Clocking

The dsPIC33CDVL256MC506 devices can be configured to use any of the following clock configurations:

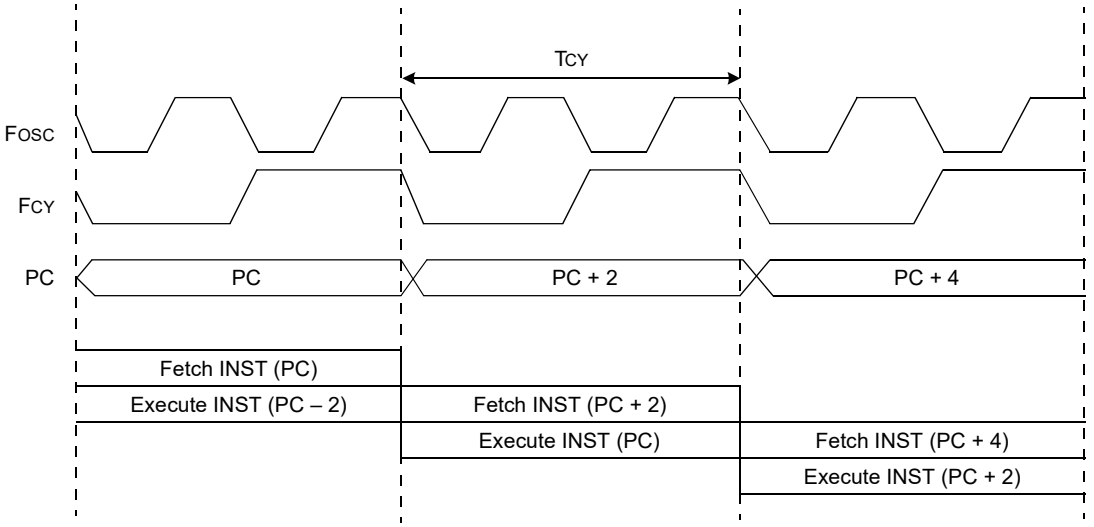
- Primary Oscillator (POSC) on the OSCI and OSCO pins
- Internal Fast RC Oscillator (FRC) with optional clock divider
- Internal Low-Power RC Oscillator (LPRC)
- Primary Oscillator with PLL (ECPLL, HSPLL, XTPLL)
- Internal Fast RC Oscillator with PLL (FRCPLL)
- Backup Internal Fast RC Oscillator (BFRC)

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The system clock source is divided by two to produce the internal instruction cycle clock. In this document, the instruction cycle clock is denoted by F_{CY}. The timing diagram in Figure 9-4 illustrates the relationship between the system clock (F_{OSC}), the instruction cycle clock (F_{CY}) and the Program Counter (PC).

The internal instruction cycle clock (F_{CY}) can be output on the OSCO I/O pin if the Primary Oscillator mode (POSCMD[1:0]) is not configured as HS/XT. For more information, see Oscillator with High-Frequency PLL.

Figure 9-4. Clock and Instruction Cycle Timing



9.3. Primary Oscillator (POSC)

The dsPIC33CDVL256MC506 family devices contain one instance of the Primary Oscillator (POSC). The Primary Oscillator is available on the OSCI and OSCO pins of the dsPIC33C devices. This connection enables an external crystal (or ceramic resonator) to provide the clock to the device. The Primary Oscillator provides three modes of operation:

- Medium Speed Oscillator (XT Mode): The XT mode is a Medium Gain, Medium Frequency mode used to work with crystal frequencies of 3.5 MHz to 10 MHz.
- High-Speed Oscillator (HS Mode): The HS mode is a High-Gain, High-Frequency mode used to work with crystal frequencies of 10 MHz to 32 MHz.
- External Clock Source Operation (EC Mode): If the on-chip oscillator is not used, the EC mode allows the internal oscillator to be bypassed. The device clocks are generated from an external source (0 MHz to up to 64 MHz) and input on the OSCI pin.

9.3.1. Primary Oscillator Pin Functionality

The Primary Oscillator pins (OSCI and OSCO) can be used for other functions when the Primary Oscillator is not being used. The POSCMD[1:0] Configuration bits in the Oscillator Configuration register (FOSC[1:0]) determine the oscillator pin function. The OSCIOFNC bit (FOSC[2]) determines the OSCO/CLKO pin function. By default, the CLKO function is active, and the pin will output a clock frequency of F_{CY}. A clock signal is present on the OSCO/CLKO pin when the device is unprogrammed or during the programming sequence. Care should be taken when the OSCO/CLKO pin is used to drive other circuitry.

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9.4. Internal Fast RC (FRC) Oscillator

The dsPIC33CDVL256MC506 family devices contain one instance of the internal Fast RC (FRC) Oscillator. The FRC Oscillator provides a nominal 8 MHz clock without requiring an external crystal or ceramic resonator, which results in system cost savings for applications that do not require a precise clock reference.

The application software can tune the frequency of the oscillator using the FRC Oscillator Tuning bits (TUN[5:0]) in the FRC Oscillator Tuning register (OSCTUN[5:0]).

9.5. Low-Power RC (LPRC) Oscillator

The dsPIC33CDVL256MC506 family devices contain one instance of the Low-Power RC (LPRC) Oscillator, which provides a nominal clock frequency of 32.768 kHz. The dsPIC33CDVL256MC506 family devices implement the LPRC function with the BFRC and post-divider to yield a 50% duty cycle output.

The LPRC is the clock source for the Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM) circuits in the clock subsystem. The LPRC Oscillator is shut off in Sleep mode. The LPRC Oscillator remains enabled under these conditions:

- The FSCM is enabled.
- The WDT is enabled.
- The LPRC Oscillator is selected as the system clock.

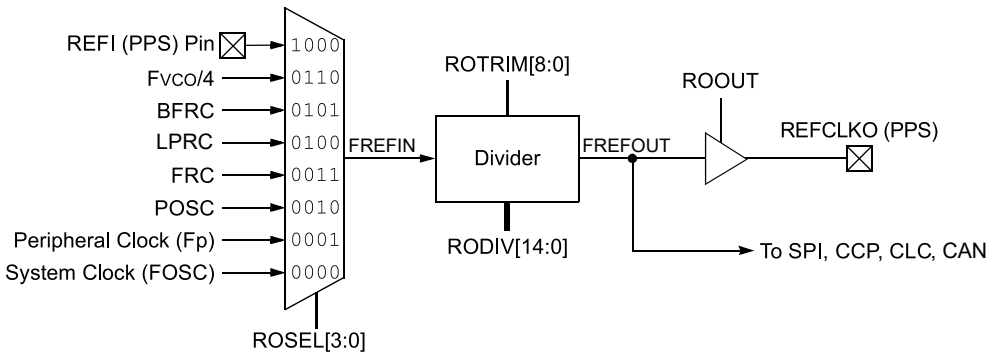
9.6. Internal Backup Fast RC (BFRC) Oscillator

The oscillator block provides a stable reference clock source for the Fail-Safe Clock Monitor (FSCM). When FSCM is enabled in the FCKSM[1:0] Configuration bits (FOSC[7:6]), it constantly monitors the main clock source against a reference signal from the 8 MHz Internal Backup Fast RC (BFRC) Oscillator. In case of a clock failure, the Fail-Safe Clock Monitor switches the clock to the BFRC Oscillator, allowing for continued low-speed operation or a safe application shutdown.

9.7. Reference Clock Output

In addition to the CLKO output ($F_{OSC}/2$), the dsPIC33CDVL256MC506 family devices can be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application. CLKO is enabled by the Configuration bit (OSCIOFNC) and is independent of the REFCLKO reference clock. REFCLKO is mappable to any I/O pin that has mapped output capability. The reference clock output module block diagram is shown in Figure 9-5.

Figure 9-5. Reference Clock Generator



This reference clock output is controlled by the REFOCONL and REFOCONH registers. Setting the ROEN bit (REFOCONL[15]) makes the clock signal available on the REFCLKO pin. The RODIV[14:0] bits (REFOCONH[14:0]) and ROTRIM[8:0] bits (REFOTRIM[15:7]) enable the selection of different clock divider options. The formula for determining the final frequency output is shown in Equation 9-3.

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The ROSWEN bit (REFOCONL[9]) indicates that the clock divider has been successfully switched. In order to switch the REFCLKO divider, the user should ensure that this bit reads as '0'. Write the updated values to the RODIV[14:0] or ROTRIM[8:0] bits, set the ROSWEN bit, and then wait until it is cleared before assuming that the REFCLKO clock is valid.

Equation 9-3. Calculating Frequency Output

$$FREFOUT = \frac{FREFIN}{2 \bullet (RODIV[14:0] + ROTRIM[8:0]/512)}$$

Where: $FREFOUT$ = Output Frequency
$FREFIN$ = Input Frequency
When $RODIV[14:0] = 0$, the output clock is the same as the input clock.

The ROSEL[3:0] bits (REFOCONL[3:0]) determine which clock source is used for the reference clock output. The ROSLP bit (REFOCONL[11]) determines if the reference source is available on REFCLKO when the device is in Sleep mode.

To use the reference clock output in Sleep mode, both the ROSLP bit must be set and the clock selected by the ROSEL[3:0] bits must be enabled for operation during Sleep mode, if possible. Clearing the ROSEL[3:0] bits allows the reference output frequency to change, as the system clock changes during any clock switches. The ROOUT bit enables/disables the reference clock output on the REFCLKO pin.

The ROACTIV bit (REFOCONL[8]) indicates that the module is active; it can be cleared by disabling the module (setting ROEN to '0'). The user must not change the reference clock source or adjust the divider when the ROACTIV bit indicates that the module is active. To avoid glitches, the user should not disable the module until the ROACTIV bit is '1'.

9.8. Oscillator Configuration

The oscillator system has both Configuration registers and SFRs to configure, control and monitor the system. The FOSCSEL and FOSC Configuration registers (FOSCSEL and FOSC, respectively) are used for initial setup.

Table 9-1 lists the configuration settings that select the device's oscillator source and operating mode at a Power-on Reset (POR).

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Table 9-1. Configuration Bit Values for Clock Selection

Oscillator Source	Oscillator Mode	FNOSC[2:0] Value	POSCMD[1:0] Value
S0	Fast RC Oscillator (FRC)(1)	000	xx
S1	Fast RC Oscillator with PLL (FRCPLL)(1)	001	xx
S2	Primary Oscillator (EC)(1)	010	00
S2	Primary Oscillator (XT)	010	01
S2	Primary Oscillator (HS)	010	10
S3	Primary Oscillator with PLL (ECPLL)(1)	011	00
S3	Primary Oscillator with PLL (XTPLL)	011	01
S3	Primary Oscillator with PLL (HSPLL)	011	10
S4	Reserved	100	xx
S5	Low-Power RC Oscillator (LPRC)(1)	101	xx
S6	Backup FRC (BFRC)(1)	110	xx
S7	Fast RC Oscillator with ÷ N Divider (FRCDIVN)(1,2)	111	xx

Notes:
1. The OSCO pin function is determined by the OSCIOFNC Configuration bit.
2. This is the default oscillator mode for an unprogrammed (erased) device.

9.9. OSCCON Unlock Sequence

The OSCCON register is protected against unintended writes through a lock mechanism. The upper and lower bytes of OSCCON have their own unlock sequence, and both must be used when writing to both bytes of the register.

Before OSCCON can be written to, the following unlock sequence must be used:

1. Execute the unlock sequence for the OSCCON high byte.
   In two back-to-back instructions:
   - Write 0x78 to OSCCON[15:8]
   - Write 0x9A to OSCCON[15:8]
2. In the instruction immediately following the unlock sequence, the OSCCON[15:8] bits can be modified.
3. Execute the unlock sequence for the OSCCON low byte.
   In two back-to-back instructions:
   - Write 0x46 to OSCCON[7:0]
   - Write 0x57 to OSCCON[7:0]
4. In the instruction immediately following the unlock sequence, the OSCCON[7:0] bits can be modified.

Note: MPLAB® XC16 provides a built-in C language function, including the unlocking sequence to modify high and low bytes in the OSCCON register:

```
__builtin_write_OSCCONH(value)
__builtin_write_OSCCONL(value)
```


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9.10. Oscillator Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0F84	OSCCON	15:8			COSC[2:0]				NOSC[2:0]	
		7:0	CLKLOCK		LOCK		CF			OSWEN
0x0F86	CLKDIV	15:8	ROI		DOZE[2:0]		DOZEN		FRCDIV[2:0]	
		7:0			Reserved[1:0]			PLLPRE[3:0]		
0x0F88	PLLFBD	15:8						Reserved[3:0]		
		7:0				PLLFBDIV[7:0]				
0x0F8A	PLLDIV	15:8								VCODIV[1:0]
		7:0			POST1DIV[2:0]				POST2DIV[2:0]	
0x0F8C	OSCTUN	15:8								
		7:0				TUN[5:0]				
0x0F8E ... 0x0F99	Reserved									
0x0F9A	CANCLKCON	15:8	CANCLKEN					CANCLKSEL[3:0]		
		7:0				CANCLKDIV[6:0]				
0x0F9C ... 0x0FB7	Reserved									
0x0FB8	REFOCONL	15:8	ROEN		ROSIDL	ROOUT	ROSLP		ROSWEN	ROACTIV
		7:0					ROSEL[3:0]			
0x0FBA	REFOCONH	15:8				RODIV[14:8]				
		7:0				RODIV[7:0]				
0x0FBC ... 0x0FBD	Reserved									
0x0FBE	REFOTRIMH	15:8				ROTRIM[8:0]				
		7:0	ROTRIM[8:0]							

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9.10.1. Oscillator Control Register

Name: OSCCON(1)
Offset: 0xF84

Notes:

1. Writes to this register require an unlock sequence.
2. Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.
3. This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and will trigger an oscillator failure trap.

Legend: y = Value set from Configuration bits on POR

Bit	15	14	13	12	11	10	9	8
		COSC[2:0]				NOSC[2:0]		
Access		R	R	R		R/W	R/W	R/W
Reset		0	0	0		y	y	y

Bit	7	6	5	4	3	2	1	0
	CLKLOCK		LOCK		CF			OSWEN
Access	R/W		R		R			R/W
Reset	0		0		0			0

Bits 14:12 – COSC[2:0] Current Oscillator Selection bits (read-only)

Value	Description
111	Fast RC Oscillator (FRC) with Divide-by-n (FRCDIVN)
110	Backup FRC (BFRC)
101	Low-Power RC Oscillator (LPRC)
100	Reserved – default to FRC
011	Primary Oscillator (XT, HS, EC) with PLL (XTPLL, HSPLL, ECPLL)
010	Primary Oscillator (XT, HS, EC)
001	Fast RC Oscillator (FRC) with PLL (FRCPLL)
000	Fast RC Oscillator (FRC)

Bits 10:8 – NOSC[2:0] New Oscillator Selection bits(2)

Value	Description
111	Fast RC Oscillator (FRC) with Divide-by-n (FRCDIVN)
110	Backup FRC (BFRC)
101	Low-Power RC Oscillator (LPRC)
100	Reserved – default to FRC
011	Primary Oscillator (XT, HS, EC) with PLL (XTPLL, HSPLL, ECPLL)
010	Primary Oscillator (XT, HS, EC)
001	Fast RC Oscillator (FRC) with PLL (FRCPLL)
000	Fast RC Oscillator (FRC)

Bit 7 – CLKLOCK Clock Lock Enable bit

Value	Description
1	If (FCKSM0 = 1), then clock and PLL configurations are locked; if (FCKSM0 = 0), then clock and PLL configurations may be modified
0	Clock and PLL selections are not locked, configurations may be modified

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Bit 5 – LOCK PLL Lock Status bit (read-only)

Value	Description
1	Indicates that PLL is in lock or PLL start-up timer is satisfied
0	Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

Bit 3 – CF Clock Fail Detect bit(3)

Value	Description
1	FSCM has detected a clock failure
0	FSCM has not detected a clock failure

Bit 0 – OSWEN Oscillator Switch Enable bit

Value	Description
1	Requests oscillator switch to the selection specified by the NOSC[2:0] bits
0	Oscillator switch is complete

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9.10.2. Clock Divider Register

Name: CLKDIV
Offset: 0xF86

Notes:

1. The DOZE[2:0] bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE[2:0] are ignored.
2. This bit is cleared when the ROI bit is set and an interrupt occurs.
3. The DOZEN bit cannot be set if DOZE[2:0] = 000. If DOZE[2:0] = 000, any attempt by user software to set the DOZEN bit is ignored.
4. PLLPRE[3:0] may be updated while the PLL is operating, but the VCO may overshoot.

Legend: r = Reserved bit

Bit	15	14	13	12	11	10	9	8
	ROI	DOZE[2:0]			DOZEN	FRCDIV[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			Reserved[1:0]		PLLPRE[3:0]			
Access			r	r	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	1

Bit 15 – ROI Recover on Interrupt bit

Value	Description
1	Interrupts will clear the DOZEN bit, and the processor clock and the peripheral clock ratio is set to 1:1.
0	Interrupts have no effect on the DOZEN bit.

Bits 14:12 – DOZE[2:0] Processor Clock Reduction Select bits(1)

Value	Description
111	F_{OSC} divided by 128
110	F_{OSC} divided by 64
101	F_{OSC} divided by 32
100	F_{OSC} divided by 16
011	F_{OSC} divided by 8 (default)
010	F_{OSC} divided by 4
001	F_{OSC} divided by 2
000	F_{OSC} divided by 1

Bit 11 – DOZEN Doze Mode Enable bit(2,3)

Value	Description
1	DOZE[2:0] field specifies the ratio between the peripheral clocks and the processor clocks.
0	Processor clock and peripheral clock ratio is forced to 1:1.

Bits 10:8 – FRCDIV[2:0] Internal Fast RC Oscillator Postscaler bits

Value	Description
111	FRC divided by 256
110	FRC divided by 64
101	FRC divided by 32

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Value	Description
100	FRC divided by 16
011	FRC divided by 8
010	FRC divided by 4
001	FRC divided by 2
000	FRC divided by 1 (default)

Bits 5:4 – Reserved[1:0] Read as '0'

Bits 3:0 – PLLPRE[3:0] PLL Phase Detector Input Divider Select bits(4)
(also denoted as 'N1', PLL prescaler)

Value	Description
1111	Reserved
. . .	
1001	Reserved
1000	Input divided by 8
0111	Input divided by 7
0110	Input divided by 6
0101	Input divided by 5
0100	Input divided by 4
0011	Input divided by 3
0010	Input divided by 2
0001	Input divided by 1 (power-on default selection)
0000	Reserved

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9.10.3. PLL Feedback Divider Register

Name: PLLFBD
Offset: 0xF88

Note:

1. The allowed range is 16-200 (decimal). The rest of the values are reserved and should be avoided. The power on the default feedback divider is 150 (decimal) with an 8 MHz FRC input clock. The VCO frequency is 1.2 GHz.

Legend: r = Reserved bit

Bit	15	14	13	12	11	10	9	8
					Reserved[3:0]			
Access					r	r	r	r
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PLLFBDIV[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	1	0	1	1	0

Bits 11:8 – Reserved[3:0] Maintain as '0'

Bits 7:0 – PLLFBDIV[7:0] PLL Feedback Divider bits (also denoted as 'M', PLL multiplier)(1)

Value	Description
11111111	Reserved
...	
11001001	Reserved
11001000	Maximum (200 decimal)
...	
10010110	150 (default)
...	
00010000	Minimum (16 decimal)
00001111	Reserved
...	
00000000	Reserved

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9.10.4. PLL Output Divider Register

Name: PLLDIV
Offset: 0xF8A

Notes:

1. The POST1DIVx and POST2DIVx divider values must not be changed while the PLL is operating.
2. The default values for POST1DIVx and POST2DIVx are 4 and 1, respectively, yielding a 150 MHz system source clock.

Bit	15	14	13	12	11	10	9	8
							VCODIV[1:0]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
		POST1DIV[2:0]				POST2DIV[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bits 9:8 – VCODIV[1:0] PLL VCO Output Divider Select bits

Value	Description
11	F_{VCO}
10	$F_{VCO}/2$
01	$F_{VCO}/3$
00	$F_{VCO}/4$

Bits 6:4 – POST1DIV[2:0] PLL Output Divider #1 Ratio bits(1,2)
POST1DIV[2:0] can have a valid value, from 1 to 7 (POST1DIVx value should be greater than or equal to the POST2DIVx value). The POST1DIVx divider is designed to operate at higher clock rates than the POST2DIVx divider.

Bits 2:0 – POST2DIV[2:0] PLL Output Divider #2 Ratio bits(1,2)
POST2DIV[2:0] can have a valid value, from 1 to 7 (POST1DIVx value should be greater than or equal to the POST2DIVx value). The POST1DIVx divider is designed to operate at higher clock rates than the POST2DIVx divider.

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9.10.5. FRC Oscillator Tuning Register

Name: OSCTUN
Offset: 0xF8C

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			TUN[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – TUN[5:0] FRC Oscillator Tuning bits

Value	Description
011111	Maximum frequency deviation of 1.45% (MHz)
011110	Center frequency + 1.40% (MHz)
. . .	
000001	Center frequency + 0.047% (MHz)
000000	Center frequency (8.00 MHz nominal)
111111	Center frequency – 0.047% (MHz)
. . .	
100001	Center frequency – 1.45% (MHz)
100000	Minimum frequency deviation of -1.50% (MHz)

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9.10.6. CAN Clock Control Register

Name: CANCLKCON
Offset: 0xF9A

Notes:

1. The user must ensure the input clock source is 640 MHz or less. Operation with an input reference frequency above 640 MHz will result in unpredictable behavior.
2. The CANCLKDIVx divider value must not be changed during CAN module operation.
3. The user must ensure the maximum clock output frequency of the divider is 80 MHz or less.

Bit	15	14	13	12	11	10	9	8
	CANCLKEN				CANCLKSEL[3:0]			
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit	7	6	5	4	3	2	1	0
		CANCLKDIV[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit 15 – CANCLKEN CAN Clock Generator Enable bit

Value	Description
1	CAN clock generation circuitry is enabled.
0	CAN clock generation circuitry is disabled.

Bits 11:8 – CANCLKSEL[3:0] CAN Clock Source Select bits(1)

Value	Description
0110-1111	Reserved (no clock selected)
0101	$F_{VCO}/4$
0100	$F_{VCO}/3$
0011	$F_{VCO}/2$
0010	F_{PLLO}
0001	F_{VCO}
0000	0 (no clock selected)

Bits 6:0 – CANCLKDIV[6:0] CAN Clock Divider Select bits(2,3)

Value	Description
1111111	Divide-by-128
. . .	
0000010	Divide-by-3
0000001	Divide-by-2
0000000	Divide-by-1

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9.10.7. Reference Clock Control Low Register

Name: REFOCONL
Offset: 0xFB8

Legend: HC = Hardware Clearable bit; HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
	ROEN		ROSIDL	ROOUT	ROSLP		ROSWEN	ROACTIV
Access	R/W		R/W	R/W	R/W		R/W/HC	R/HSC
Reset	0		0	0	0		0	0

Bit	7	6	5	4	3	2	1	0
					ROSEL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – ROEN Reference Clock Enable bit

Value	Description
1	Reference oscillator is enabled on the REFCLKO pin.
0	Reference oscillator is disabled.

Bit 13 – ROSIDL Reference Clock Stop in Idle bit

Value	Description
1	Reference oscillator continues to run in Idle mode.
0	Reference oscillator is disabled in Idle mode.

Bit 12 – ROOUT Reference Clock Output Enable bit

Value	Description
1	Reference clock external output is enabled and available on the REFCLKO pin.
0	Reference clock external output is disabled.

Bit 11 – ROSLP Reference Clock Stop in Sleep bit

Value	Description
1	Reference oscillator continues to run in Sleep modes.
0	Reference oscillator is disabled in Sleep modes.

Bit 9 – ROSWEN Reference Clock Output Enable bit

Value	Description
1	Clock divider change (requested by changes to RODIVx) is requested or is in progress (set in software, cleared by hardware upon completion).
0	Clock divider change has been completed or is not pending.

Bit 8 – ROACTIV Reference Clock Status bit

Value	Description
1	Reference clock is active; do not change the clock source.
0	Reference clock is stopped; the clock source and configuration may be safely changed.

Bits 3:0 – ROSEL[3:0] Reference Clock Source Select bits

Value	Description
1111-1000	Reserved

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Value	Description
0111	REFCLKI pin
0110	$F_{VCO}/4$
0101	BFRC
0100	LPRC
0011	FRC
0010	Primary Oscillator
0001	Peripheral clock (F_P)
0000	System clock (F_{OSC})

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9.10.8. Reference Clock Control High Register

Name: REFOCONH
Offset: 0xFBA

Bit	15	14	13	12	11	10	9	8
		RODIV[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RODIV[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 14:0 – RODIV[14:0] Reference Clock Integer Divider Select bits
Divider for the selected input clock source is two times the selected value.

Value	Description
111 1111 1111 1111	Base clock value divided by 65,534 (2 * 7FFFh)
111 1111 1111 1110	Base clock value divided by 65,532 (2 * 7FFEh)
111 1111 1111 1101	Base clock value divided by 65,530 (2 * 7FFDh)
. . .	
000 0000 0000 0010	Base clock value divided by 4 (2 * 2)
000 0000 0000 0001	Base clock value divided by 2 (2 * 1)
000 0000 0000 0000	Base clock value

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9.10.9. Reference Clock Trim Register

Name: REFOTRIMH
Offset: 0xFBE

Bit	15	14	13	12	11	10	9	8
	ROTRIM[8:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ROTRIM[8:0]							
Access	R/W							
Reset	0							

Bits 15:7 – ROTRIM[8:0] REFO Trim bits
These bits provide a fractional additive to the RODIV[14:0] value for the 1/2 period of the REFO clock.

Value	Description
111111111	511/512 (0.998046875 divisor added to the RODIV[14:0] value)
111111110	510/512 (0.99609375 divisor added to the RODIV[14:0] value)
. . .	
100000000	256/512 (0.5000 divisor added to the RODIV[14:0] value)
. . .	
000000010	2/512 (0.00390625 divisor added to the RODIV[14:0] value)
000000001	1/512 (0.001953125 divisor added to the RODIV[14:0] value)
000000000	0/512 (0.0 divisor added to the RODIV[14:0] value)

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10. Direct Memory Access (DMA) Controller

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Direct Memory Access Controller (DMA)"** (www.microchip.com/DS30009742) in the "*dsPIC33/PIC24 Family Reference Manual*".

The Direct Memory Access (DMA) Controller is designed to service high data throughput peripherals operating on the SFR bus, allowing them to access data memory directly and alleviating the need for CPU-intensive management. By allowing these data-intensive peripherals to share their own data path, the main data bus is also deloaded, resulting in additional power savings.

The DMA Controller functions both as a peripheral and a direct extension of the CPU. It is located on the microcontroller data bus, between the CPU and DMA-enabled peripherals, with direct access to SRAM. This partitions the SFR bus into two buses, allowing the DMA Controller access to the DMA-capable peripherals located on the new DMA SFR bus. The controller serves as an Initiator device on the DMA SFR bus, controlling data flow from DMA-capable peripherals.

The controller also monitors CPU instruction processing directly, allowing it to be aware of when the CPU requires access to peripherals on the DMA bus and automatically relinquishes control to the CPU as needed. This increases the effective bandwidth for handling data without DMA operations, causing a processor stall. This makes the controller essentially transparent to the user.

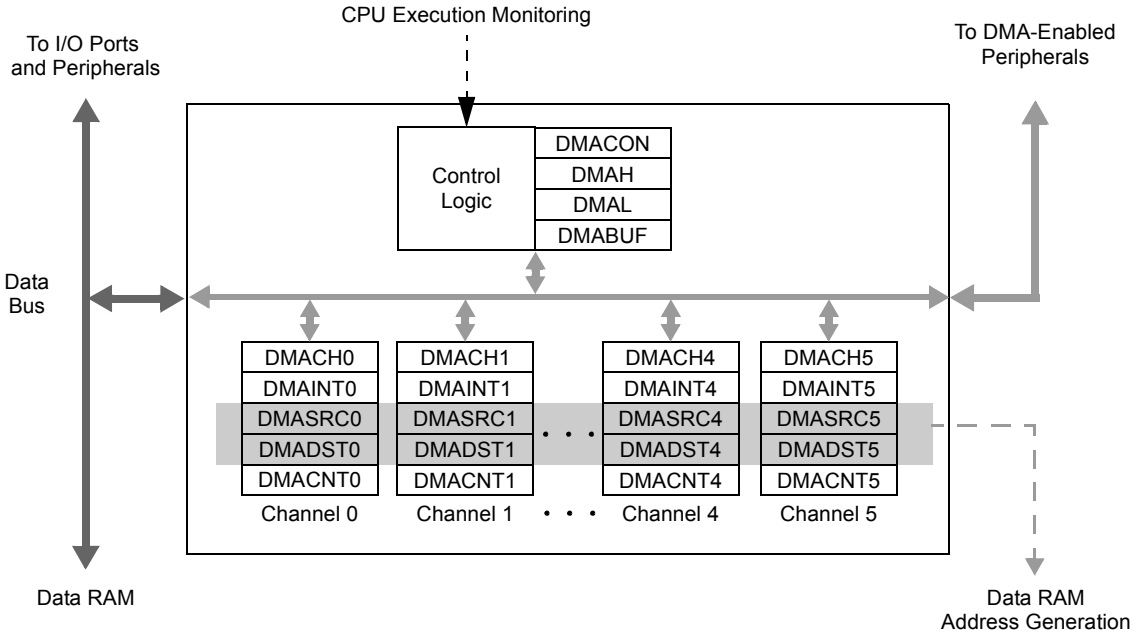
The DMA Controller has these features:

- A Total of Four Independently Programmable Channels
- Concurrent Operation with the CPU (no DMA Caused Wait States)
- DMA Bus Arbitration
- Five Programmable Address Modes
- Four Programmable Transfer Modes
- Four Flexible Internal Data Transfer Modes
- Byte or Word Support for Data Transfer
- 16-Bit Source and Destination Address Register for Each Channel, Dynamically Updated and Reloadable
- 16-Bit Transaction Count Register, Dynamically Updated and Reloadable
- Upper and Lower Address Limit Registers
- Counter Half-Full Level Interrupt
- Software Triggered Transfer
- Null Write Mode for Symmetric Buffer Operations

A simplified block diagram of the DMA Controller is shown in Figure 10-1.

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Figure 10-1. DMA Functional Block Diagram



10.1. Summary of DMA Operations

The DMA Controller is capable of moving data between addresses according to a number of different parameters. Each of these parameters can be independently configured for any transaction. In addition, any or all of the DMA channels can independently perform a different transaction at the same time. Transactions are classified by these parameters:

- Source and destination (SFRs and data RAM)
- Data size (byte or word)
- Trigger source
- Transfer mode (One-Shot, Repeated or Continuous)
- Addressing modes (Fixed Address or Address Blocks with or without Address Increment/Decrement)

In addition, the DMA Controller provides channel priority arbitration for all channels.

10.1.1. Source and Destination

Using the DMA Controller, data may be moved between any two addresses in the Data Space. The SFR space (0000h to 0FFFh), or the data RAM space (5000h to 9000h), can serve as either the source or the destination. Data can be moved between these areas in either direction or between addresses in either area. The four different combinations are shown in Addressing Modes.

If it is necessary to protect areas of data RAM, the DMA Controller allows the user to set upper and lower address boundaries for operations in the Data Space above the SFR space. The boundaries are set by the DMAH and DMAL Limit registers. If a DMA channel attempts an operation outside of the address boundaries, the transaction is terminated and an interrupt is generated.

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10.1.2. Data Size

The DMA Controller can handle both 8-bit and 16-bit transactions. Size is user-selectable using the SIZE bit (DMACHn[1]). By default, each channel is configured for word-size transactions. When byte-size transactions are chosen, the LSB of the source and/or destination address determines if the data represent the upper or lower byte of the data RAM location.

10.1.3. Trigger Source

The DMA Controller can use 82 of the device's interrupt sources to initiate a transaction. The DMA trigger sources occur in reverse order from their natural interrupt priority and are shown in Addressing Modes.

Since the source and destination addresses for any transaction can be programmed independently of the trigger source, the DMA Controller can use any trigger to perform an operation on any peripheral. This also allows DMA channels to be cascaded to perform more complex transfer operations.

10.1.4. Transfer Mode

The DMA Controller supports four types of data transfers based on the volume of data to be moved for each trigger.

- One-Shot: A single transaction occurs for each trigger.
- Continuous: A series of back-to-back transactions occur for each trigger; the number of transactions is determined by the DMACNTn transaction counter.
- Repeated One-Shot: A single transaction is performed repeatedly, once per trigger, until the DMA channel is disabled.
- Repeated Continuous: A series of transactions are performed repeatedly, one cycle per trigger, until the DMA channel is disabled.

All transfer modes allow the option to have the source and destination addresses and counter value automatically reloaded after the completion of a transaction.

10.1.5. Addressing Modes

The DMA Controller also supports transfers between single addresses or address ranges. The four basic options are:

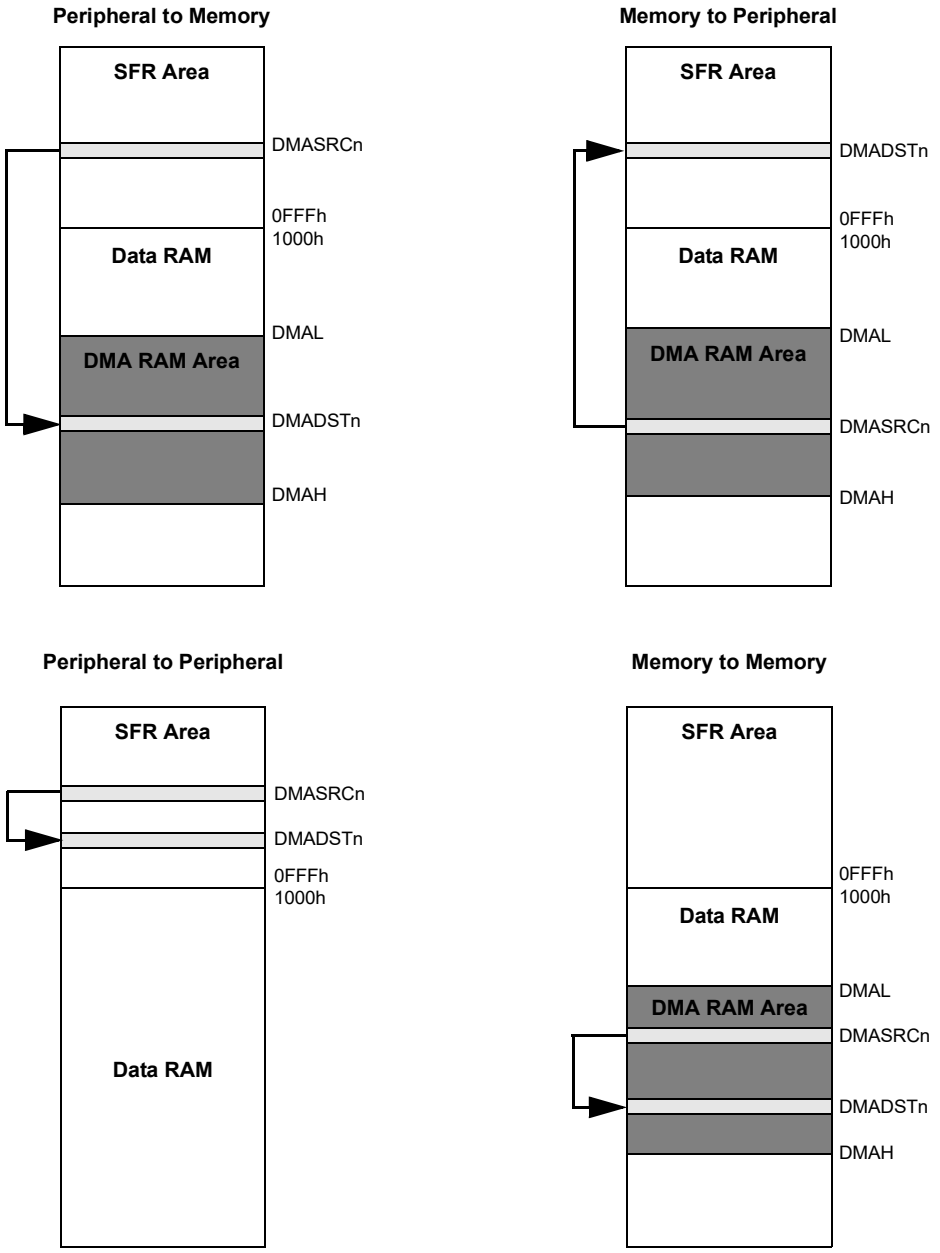
- Fixed-to-Fixed: Between two constant addresses
- Fixed-to-Block: From a constant source address to a range of destination addresses
- Block-to-Fixed: From a range of source addresses to a single, constant destination address
- Block-to-Block: From a range of source addresses to a range of destination addresses

The option to select auto-increment or auto-decrement of source and/or destination addresses is available for Block Addressing modes.

In addition to the four basic modes, the DMA Controller also supports Peripheral Indirect Addressing (PIA) mode, where the source or destination address is generated jointly by the DMA Controller and a PIA-capable peripheral. When enabled, the DMA channel provides a base source and/or destination address, while the peripheral provides a fixed range offset address.

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Figure 10-2. Types of DMA Data Transfers



Note: Relative sizes of memory areas are not shown to scale.

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10.1.6. Channel Priority

Each DMA channel functions independently of the others but also competes with the others for access to the data and DMA buses. When access collisions occur, the DMA Controller arbitrates between the channels using a user-selectable priority scheme. Two schemes are available:

- Round Robin: When two or more channels collide, the lower-numbered channel receives priority on the first collision. On subsequent collisions, the higher-numbered channels each receive priority based on their channel number.
- Fixed: When two or more channels collide, the lowest numbered channel always receives priority, regardless of past history; however, any channel being actively processed is not available for an immediate retrigger. If a higher priority channel is continually requesting service, it will be scheduled for service after the next lower priority channel with a pending request.

10.2. Typical Setup

To set up a DMA channel for a basic data transfer:

1. Enable the DMA Controller (DMAEN = 1) and select an appropriate channel priority scheme by setting or clearing PRSSEL.
2. Program DMAH and DMAL with appropriate upper and lower address boundaries for data RAM operations.
3. Select the DMA channel to be used and disable its operation (CHEN = 0).
4. Program the appropriate source and destination addresses for the transaction into the channel's DMASRCn and DMADSTn registers. For PIA Mode Addressing, use the base address value.
5. Program the DMACNTn register for the number of triggers per transfer (One-Shot or Continuous modes) or the number of words (bytes) to be transferred (Repeated modes).
6. Set or clear the SIZE bit to select the data size.
7. Program the TRMODE[1:0] bits to select the Data Transfer mode.
8. Program the SAMODE[1:0] and DAMODE[1:0] bits to select the addressing mode.
9. Enable the DMA channel by setting CHEN.
10. Enable the trigger source interrupt.

10.2.1. Peripheral Module Disable

The channels of the DMA Controller can be individually powered down using the Peripheral Module Disable (PMD) registers.

10.2.2. DMA Registers

The DMA Controller uses a number of registers to control its operation. The number of registers depends on the number of channels implemented for a particular device.

There are always four module-level registers (one control and three buffer/address):

- DMACON: DMA Engine Control Register
- DMAH and DMAL: DMA High and Low Address Limit Registers
- DMABUF: DMA Transfer Data Buffer

Each of the DMA channels implements five registers (two control and three buffer/address):

- DMACHn: DMA Channel n Control Register
- DMAINTn: DMA Channel n Interrupt Register
- DMASRCn: DMA Data Source Address Pointer for Channel n Register
- DMADSTn: DMA Data Destination Source for Channel n Register

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- DMACNTn: DMA Transaction Counter for Channel n Register

For devices, there are a total of 34 registers.

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10.2.3. DMA Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0ABC	DMACON	15:8	DMAEN		DMASIDL					
		7:0								PRSSEL
0x0ABE	DMABUF	15:8	DMABUF[15:8]							
		7:0	DMABUF[7:0]							
0x0AC0	DMAL	15:8	LADDR[15:8]							
		7:0	LADDR[7:0]							
0x0AC2	DMAH	15:8	HADDR[15:8]							
		7:0	HADDR[7:0]							
0x0AC4	DMACH0	15:8				Reserved		NULLW	RELOAD	CHREQ
		7:0	SAMODE[1:0]		DAMODE[1:0]		TRMODE[1:0]		SIZE	CHEN
0x0AC6	DMAINT0	15:8	DBUFWF	CHSEL[6:0]						
		7:0	HIGHIF	LOWIF	DONEIF	HALFIF	OVRUNIF			HALFEN
0x0AC8	DMASRCn	15:8	SADDR[15:8]							
		7:0	SADDR[7:0]							
0x0ACA	DMADSTn	15:8	DADDR[15:8]							
		7:0	DADDR[7:0]							
0x0ACC	DMACNTn	15:8	CNT[15:8]							
		7:0	CNT[7:0]							
0x0ACE	DMACH1	15:8				Reserved		NULLW	RELOAD	CHREQ
		7:0	SAMODE[1:0]		DAMODE[1:0]		TRMODE[1:0]		SIZE	CHEN
0x0AD0	DMAINT1	15:8	DBUFWF	CHSEL[6:0]						
		7:0	HIGHIF	LOWIF	DONEIF	HALFIF	OVRUNIF			HALFEN
0x0AD2	DMASRCn	15:8	SADDR[15:8]							
		7:0	SADDR[7:0]							
0x0AD4	DMADSTn	15:8	DADDR[15:8]							
		7:0	DADDR[7:0]							
0x0AD6	DMACNTn	15:8	CNT[15:8]							
		7:0	CNT[7:0]							
0x0AD8	DMACH2	15:8				Reserved		NULLW	RELOAD	CHREQ
		7:0	SAMODE[1:0]		DAMODE[1:0]		TRMODE[1:0]		SIZE	CHEN
0x0ADA	DMAINT2	15:8	DBUFWF	CHSEL[6:0]						
		7:0	HIGHIF	LOWIF	DONEIF	HALFIF	OVRUNIF			HALFEN
0x0ADC	DMASRCn	15:8	SADDR[15:8]							
		7:0	SADDR[7:0]							
0x0ADE	DMADSTn	15:8	DADDR[15:8]							
		7:0	DADDR[7:0]							
0x0AE0	DMACNTn	15:8	CNT[15:8]							
		7:0	CNT[7:0]							
0x0AE2	DMACH3	15:8				Reserved		NULLW	RELOAD	CHREQ
		7:0	SAMODE[1:0]		DAMODE[1:0]		TRMODE[1:0]		SIZE	CHEN
0x0AE4	DMAINT3	15:8	DBUFWF	CHSEL[6:0]						
		7:0	HIGHIF	LOWIF	DONEIF	HALFIF	OVRUNIF			HALFEN
0x0AE6	DMASRCn	15:8	SADDR[15:8]							
		7:0	SADDR[7:0]							
0x0AE8	DMADSTn	15:8	DADDR[15:8]							
		7:0	DADDR[7:0]							
0x0AEA	DMACNTn	15:8	CNT[15:8]							
		7:0	CNT[7:0]							

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10.2.3.1. DMA Engine Control Register

Name: DMACON
Offset: 0xABC

Bit	15	14	13	12	11	10	9	8
	DMAEN		DMASIDL					
Access	R/W		R/W					
Reset	0		0					

Bit	7	6	5	4	3	2	1	0
								PRSSEL
Access								R/W
Reset								0

Bit 15 – DMAEN DMA Module Enable bit

Value	Description
1	Enables module.
0	Disables module and terminates all active DMA operation(s).

Bit 13 – DMASIDL DMA Stop in Idle bit

Value	Description
1	DMA continues to run in Idle mode.
0	DMA is disabled in Idle mode.

Bit 0 – PRSSEL Channel Priority Scheme Selection bit

Value	Description
1	Round robin scheme
0	Fixed priority scheme

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10.2.3.2. DMA Buffer Register

Name: DMABUF
Offset: 0xABE

Bit	15	14	13	12	11	10	9	8
	DMABUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DMABUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DMABUF[15:0] DMA Buffer bits

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10.2.3.3. DMA Low Address Limit Register

Name: DMAL
Offset: 0xAC0

Bit	15	14	13	12	11	10	9	8
	LADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – LADDR[15:0] DMA Low Address Limit bits

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10.2.3.4. DMA High Address Limit Register

Name: DMAH
Offset: 0xAC2

Bit	15	14	13	12	11	10	9	8
	HADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – HADDR[15:0] DMA High Address Limit bits

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10.2.3.5. DMA Channel n Control Register

Name: DMACHn
Offset: 0xAC4, 0xACE, 0xAD8, 0xAE2

Notes:

1. Only the original DMACNTn is required to be stored to recover the original DMASRCn and DMADSTn values.
2. DMACNTn will always be reloaded in repeated mode transfers, regardless of the state of the RELOAD bit.
3. The number of transfers executed while CHREQ is set depends on the configuration of TRMODE[1:0].

Legend: r = Reserved bit

Bit	15	14	13	12	11	10	9	8
				Reserved		NULLW	RELOAD	CHREQ
Access				r		R/W	R/W	R/W
Reset				0		0	0	0

Bit	7	6	5	4	3	2	1	0
	SAMODE[1:0]		DAMODE[1:0]		TRMODE[1:0]		SIZE	CHEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 12 – Reserved Maintain as '0'

Bit 10 – NULLW Null Write Mode bit

Value	Description
1	A dummy write is initiated to DMASRCn for every write to DMADSTn.
0	No dummy write is initiated.

Bit 9 – RELOAD Address and Count Reload bit(1)

Value	Description
1	DMASRCn, DMADSTn and DMACNTn registers are reloaded to their previous values upon the start of the next operation.
0	DMASRCn, DMADSTn and DMACNTn are not reloaded on the start of the next operation(2).

Bit 8 – CHREQ DMA Channel Software Request bit(3)

Value	Description
1	A DMA request is initiated by software and is automatically cleared upon completion of a DMA transfer.
0	No DMA request is pending.

Bits 7:6 – SAMODE[1:0] Source Address Mode Selection bits

Value	Description
11	DMASRCn is used in Peripheral Indirect Addressing and remains unchanged.
10	DMASRCn is decremented based on the SIZE bit after a transfer completion.
01	DMASRCn is incremented based on the SIZE bit after a transfer completion.
00	DMASRCn remains unchanged after a transfer completion.

Bits 5:4 – DAMODE[1:0] Destination Address Mode Selection bits

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Value	Description
11	DMADSTn is used in Peripheral Indirect Addressing and remains unchanged.
10	DMADSTn is decremented based on the SIZE bit after transfer completion.
01	DMADSTn is incremented based on the SIZE bit after the transfer is complete.
00	DMADSTn remains unchanged after the transfer is completed.

Bits 3:2 – TRMODE[1:0] Transfer Mode Selection bits

Value	Description
11	Repeated Continuous
10	Continuous
01	Repeated One-Shot
00	One-Shot

Bit 1 – SIZE Data Size Selection bit

Value	Description
1	Byte (8-bit)
0	Word (16-bit)

Bit 0 – CHEN DMA Channel Enable bit

Value	Description
1	The corresponding channel is enabled.
0	The corresponding channel is disabled.

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10.2.3.6. DMA Channel n Interrupt Register

Name: DMAINTn
Offset: 0xAC6, 0xAD0, 0xADA, 0xAE4

Notes:

1. Setting these flags in software does not generate an interrupt.
2. Testing for address limit violations (DMASRCn or DMADSTn is either greater than DMAH or less than DMAL) is NOT done before the actual access.

Bit	15	14	13	12	11	10	9	8
	DBUFWF	CHSEL[6:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HIGHIF	LOWIF	DONEIF	HALFIF	OVRUNIF			HALFEN
Access	R/W	R/W	R/W	R/W	R/W			R/W
Reset	0	0	0	0	0			0

Bit 15 – DBUFWF DMA Buffered Data Write Flag bit(1)

Value	Description
1	The content of the DMA buffer has not been written to the location specified in DMADSTn or DMASRCn in Null Write mode.
0	The content of the DMA buffer has been written to the location specified in DMADSTn or DMASRCn in Null Write mode.

Bits 14:8 – CHSEL[6:0] DMA Channel Trigger Selection bits (see Table 10-1)

Bit 7 – HIGHIF DMA High Address Limit Interrupt Flag bit(1,2)

Value	Description
1	The DMA channel has attempted to access an address higher than DMAH or the upper limit of the data RAM space.
0	The DMA channel has not invoked the high address limit interrupt.

Bit 6 – LOWIF DMA Low Address Limit Interrupt Flag bit(1,2)

Value	Description
1	The DMA channel has attempted to access the DMA SFR address lower than DMAL, but above the SFR range (07FFh).
0	The DMA channel has not invoked the low address limit interrupt.

Bit 5 – DONEIF DMA Complete Operation Interrupt Flag bit(1)

Value	Description
1	The previous DMA session has ended with completion.
0	The current DMA session has not yet completed.
	If CHEN = 0:
1	The previous DMA session has ended with completion.
0	The previous DMA session has ended without completion.

Bit 4 – HALFIF DMA 50% Watermark Level Interrupt Flag bit(1)

Value	Description
1	DMACNTn has reached the halfway point to 0000h.

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Value	Description
0	DMACNTn has not reached the halfway point.

Bit 3 – OVRUNIF DMA Channel Overrun Flag bit(1)

Value	Description
1	The DMA channel is triggered while it is still completing the operation based on the previous trigger.
0	The overrun condition has not occurred.

Bit 0 – HALFEN Halfway Completion Watermark bit

Value	Description
1	Interrupts are invoked when DMACNTn reaches its halfway point and upon completion.
0	An interrupt is invoked only upon the completion of the transfer.

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10.2.3.7. DMA Data Source Address Pointer Channel n Register

Name: DMASRCn
Offset: 0xAC8, 0xAD2, 0xADC, 0xAE6

Bit	15	14	13	12	11	10	9	8
	SADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SADDR[15:0] DMA Data Source Address Pointer bits

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10.2.3.8. DMA Data Source Address Pointer Channel n Register

Name: DMADSTn
Offset: 0xACA, 0xAD4, 0xADE, 0xAE8

Bit	15	14	13	12	11	10	9	8
	DADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DADDR[15:0] DMA Data Destination Address Pointer bits

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10.2.3.9. DMA Transaction Counter Channel n Register

Name: DMACNTn
Offset: 0xACC, 0xAD6, 0xAE0, 0xAEA

Bit	15	14	13	12	11	10	9	8
	CNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNT[15:0] DMA Transaction Counter bits

10.2.4. DMA Trigger Sources

Table 10-1. DMA Channel Trigger Sources

CHSEL[6:0]	Trigger (Interrupt)	CHSEL[6:0]	Trigger (Interrupt)	CHSEL[6:0]	Trigger (Interrupt)
00h	INT0 – External Interrupt 0	1Ch	PWM Generator 1	39h	ADC Done AN17
01h	SCCP1 IC/OC	1Dh	PWM Generator 2	3Ah	ADC Done AN18
02h	SPI1 Receiver	1Eh	PWM Generator 3	3Bh	ADC Done AN19
03h	SPI1 Transmitter	1Fh	PWM Generator 4	3Ch	ADC Done AN20
04h	UART1 Receiver	20h-23h	(Reserved, do not use)	3Dh	ADC Done AN21
05h	UART1 Transmitter	24h	PWM Event C	3Eh-3Fh	(Reserved, do not use)
06h	ECC Single Bit Error	25h	SENT1 TX/RX	40h	AD1FLTR1 – Oversample Filter 1
07h	NVM Write Complete	26h	(Reserved, do not use)	41h	AD1FLTR2 – Oversample Filter 2
08h	INT1 – External Interrupt 1	27h	ADC1 Group Convert Done	42h	AD1FLTR3 – Oversample Filter 3
09h	SI2C1 – I2C1 Client Event	28h	ADC Done AN0	43h	AD1FLTR4 – Oversample Filter 4
0Ah	MI2C1 – I2C1 Host Event	29h	ADC Done AN1	44h	CLC1 Positive Edge Interrupt
0Bh	INT2 – External Interrupt 2	2Ah	ADC Done AN2	45h	CLC2 Positive Edge Interrupt
0Ch	SCCP2 IC/OC	2Bh	ADC Done AN3	46h	SPI1 – Fault Interrupt
0Dh	INT3 – External Interrupt 3	2Ch	ADC Done AN4	47h	SPI2 – Fault Interrupt
0Eh	UART2 Receiver	2Dh	ADC Done AN5	48h-56h	(Reserved, do not use)
0Fh	UART2 Transmitter	2Eh	ADC Done AN6	57h	PWM Event D
10h	SPI2 Receiver	2Fh	ADC Done AN7	58h	PWM Event E
11h	SPI2 Transmitter	30h	ADC Done AN8	59h	PWM Event F
12h	SCCP3 IC/OC	31h	ADC Done AN9	5Ah-5Fh	(Reserved, do not use)
13h-14h	(Reserved, do not use)	32h	ADC Done AN10	60h	CLC3 Positive Edge Interrupt
15h	SCCP4 IC/OC	33h	ADC Done AN11	61h	CLC4 Positive Edge Interrupt
16h-17h	(Reserved, do not use)	34h	ADC Done AN12	62h-67h	(Reserved, do not use)
18h	CRC Generator Interrupt	35h	ADC Done AN13	68h	UART3 Receiver
19h	PWM Event A	36h	ADC Done AN14	69h	UART3 Transmitter
1Ah	(Reserved, do not use)	37h	ADC Done AN15	6Ah-7Fh	(Reserved, do not use)
1Bh	PWM Event B	38h	ADC Done AN16		

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11. Controller Area Network Flexible Data-Rate (CAN FD) Modules

Notes:

1. This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"CAN Flexible Data-Rate (FD) Protocol Module"** (www.microchip.com/DS70005340) in the *"dsPIC33/PIC24 Family Reference Manual"*.
2. Not all device variants include the CAN FD peripheral. Refer to Table 1 for availability.

11.1. Features

The CAN FD modules have the following features:

General

- Nominal (Arbitration) Bit Rate up to 1 Mbps
- Data Bit Rate up to 8 Mbps
- CAN FD Controller Modes:
  - Mixed CAN 2.0B and CAN FD mode
  - CAN 2.0B mode
- Conforms to ISO 11898-1:2015

Message FIFOs

- Seven FIFOs, Configurable as Transmit or Receive FIFOs
- One Transmit Queue (TXQ)
- Transmit Event FIFO (TEF) with 32-Bit Timestamp

Message Transmission

- Message Transmission Prioritization:
  - Based on priority bit field, and/or
  - Message with the lowest ID gets transmitted first using the TXQ
- Programmable Automatic Retransmission Attempts: Unlimited, Three Attempts or Disabled

Message Reception

- 16 Flexible Filter and Mask Objects.
- Each Object can be Configured to Filter Either:
  - Standard ID + first 18 data bits
  - Extended ID
- 32-Bit Timestamp
- The CAN FD Bit Stream Processor (BSP) implements the Medium Access Control of the CAN FD Protocol described in ISO 11898-1:2015. It serializes and deserializes the bit stream, encodes and decodes the CAN FD frames, manages the medium access, acknowledges frames, and detects and signals errors.
- The TX Handler prioritizes the messages that are requested for transmission by the Transmit FIFOs. It uses the RAM interface to fetch the transmit data from RAM and provides it to the BSP for transmission.
- The BSP provides received messages to the RX handler. The RX handler uses acceptance filters to filter out messages that shall be stored in the receive FIFOs. It uses the RAM interface to store received data into RAM.

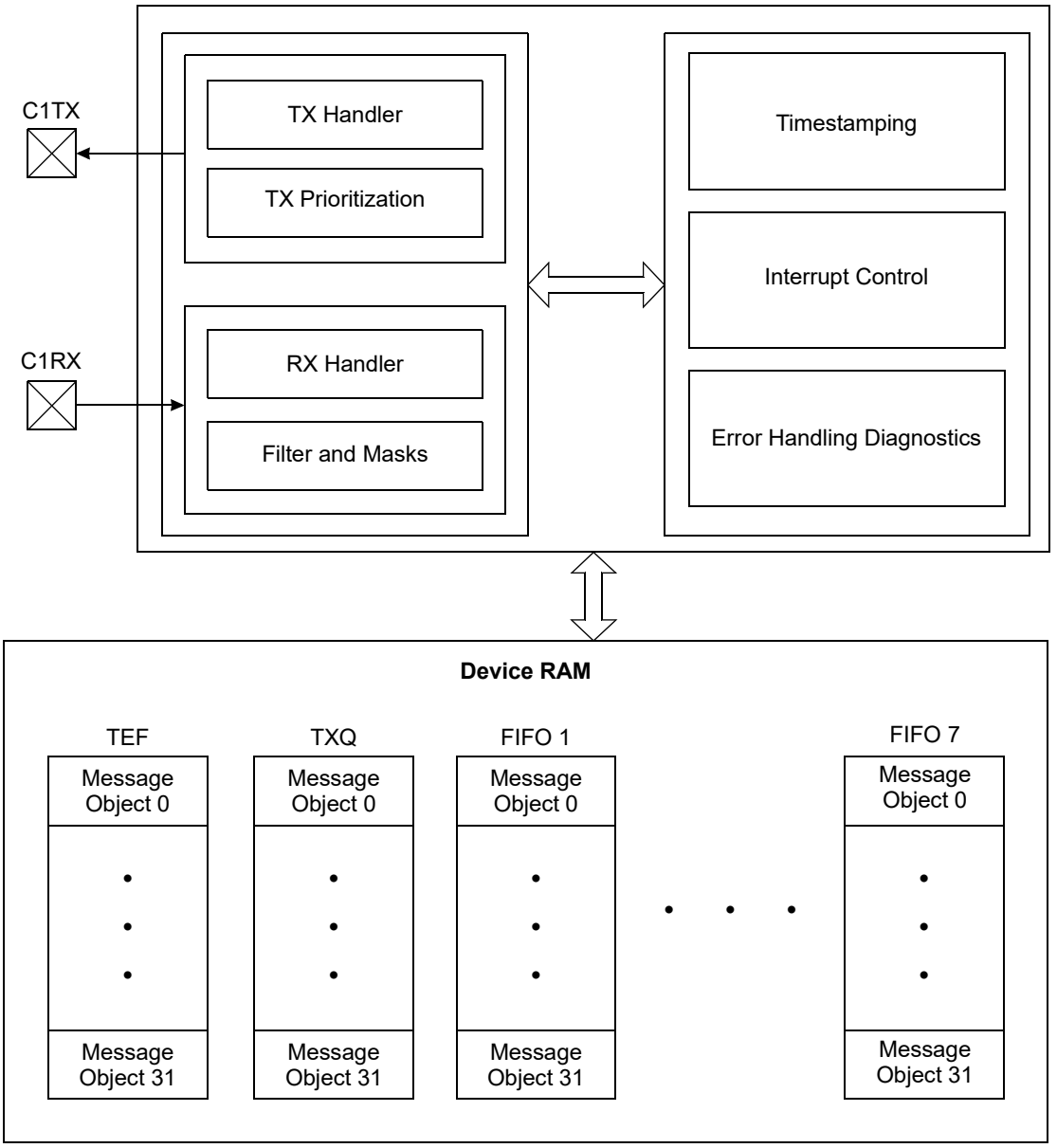
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- Each FIFO can be configured either as a Transmit or Receive FIFO. The FIFO control keeps track of the FIFO head and tail and calculates the user address. In a TX FIFO, the user address points to the address in RAM where the data for the next transmit message shall be stored. In an RX FIFO, the user address points to the address in RAM where the data of the next receive message shall be read. The user notifies the FIFO that a message was written to or read from RAM by incrementing the head/tail of the FIFO.
- The Transmit Queue (TXQ) is a special transmit FIFO that transmits the messages based on the ID of the messages stored in the queue.
- The Transmit Event FIFO (TEF) stores the Message IDs of the transmitted messages.
- A Free-Running Time Base Counter is used to timestamp received messages. Messages in the TEF can also be timestamped.
- The CAN FD Controller Modules generate interrupts when new messages are received or when messages are transmitted successfully.

Figure 11-1 shows the CAN FD system block diagram.

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Figure 11-1. CAN FD Module Block Diagram



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11.2. CAN Control/Status Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x05C0	C1CONL	15:8	CON		SIDL	BRSDIS	BUSY	WFT[1:0]		WAKFIL
		7:0	CLKSEL	PXEDIS	ISOCRCEN			DNCNT[4:0]		
0x05C2	C1CONH	15:8	TXBWS[3:0]				ABAT	REQOP[2:0]		
		7:0	OPMOD[2:0]			TXQEN	STEF	SERRLOM	ESIGM	RTXAT
0x05C4 ... 0x05C5	Reserved									
0x05C6	C1NBTCFGL	15:8		TSEG2[6:0]						
		7:0		SJW[6:0]						
0x05C6	C1NBTCFGH	15:8	BRP[7:0]							
		7:0	TSEG1[7:0]							
0x05C8	C1DBTCFGL	15:8					TSEG2[3:0]			
		7:0					SJW[3:0]			
0x05CA	C1DBTCFGH	15:8	BRP[7:0]							
		7:0				TSEG1[4:0]				
0x05CC	C1TDCL	15:8		TDCO[6:0]						
		7:0			TDCV[5:0]					
0x05CE	C1TDCH	15:8							EDGFLTEN	SID11EN
		7:0							TDCMOD[1:0]	
0x05D0	C1TBCL	15:8	TBC[15:8]							
		7:0	TBC[7:0]							
0x05D2	C1TBCH	15:8	TBC[31:24]							
		7:0	TBC[23:16]							
0x05D4	C1TSCONL	15:8							TBCPRE[9:8]	
		7:0	TBCPRE[7:0]							
0x05D6	C1TSCONH	15:8								
		7:0						TSRES	TSEOF	TBCEN
0x05D8	C1VECL	15:8				FILHIT[4:0]				
		7:0		ICODE[6:0]						
0x05DA	C1VECH	15:8		RXCODE[6:0]						
		7:0		TXCODE[6:0]						
0x05DC	C1INTL	15:8	IVMIF	WAKIF	CERRIF	SERRIF	RXOVIF	TXATIF		
		7:0				TEFIF	MODIF	TBCIF	RXIF	TXIF
0x05DE	C1INTH	15:8	IVMIE	WAKIE	CERRIE	SERRIE	RXOVIE	TXATIE		
		7:0				TEFIE	MODIE	TBCIE	RXIE	TXIE
0x05E0	C1RXIFL	15:8	RFIF[15:8]							
		7:0	RFIF[7:1]							
0x05E2	C1RXIFH	15:8	RFIF[31:24]							
		7:0	RFIF[23:16]							
0x05E4	C1TXIFL	15:8	TFIF[7:0]							
		7:0	TFIF[7:0]							
0x05E6	C1TXIFH	15:8	TFIF[31:24]							
		7:0	TFIF[23:16]							
0x05E8	C1RXOVIFL	15:8	RFOVIF[15:8]							
		7:0	RFOVIF[7:1]							
0x05EA	C1RXOVIFH	15:8	RFOVIF[31:16]							
		7:0								
0x05EC	C1TXATIFL	15:8	TFATIF[15:8]							
		7:0	TFATIF[7:0]							
0x05EE	C1TXATIFH	15:8	TFATIF[31:24]							
		7:0	TFATIF[23:16]							
0x05F0	C1TXREQL	15:8	TXREQ[15:8]							
		7:0	TXREQ[7:1]							TXREQ0
0x05F2	C1TXREQH	15:8	TXREQ[31:24]							
		7:0	TXREQ[23:16]							
0x05F4	C1TRECL	15:8	TERRCNT[7:0]							
		7:0	RERRCNT[7:0]							
0x05F6	C1TRECH	15:8								
		7:0			TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN

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CAN Control/Status Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x05F8	C1BDIAG0L	15:8	NTERRCNT[7:0]							
		7:0	NRERRCNT[7:0]							
0x05FA	C1BDIAG0H	15:8	DTERRCNT[7:0]							
		7:0	DRERRCNT[7:0]							
0x05FC	C1BDIAG1L	15:8	EFMSGCNT[15:8]							
		7:0	EFMSGCNT[7:0]							
0x05FE	C1BDIAG1H	15:8	DLCMM	ESI	DCRCERR	DSTUFERR	DFORMERR		DBIT1ERR	DBIT0ERR
		7:0	TXBOERR		NCRCERR	NSTUFERR	NFORMERR	NACKERR	NBIT1ERR	NBIT0ERR
0x0600	C1TEFCONL	15:8						FRESET		UINC
		7:0			TEFTSEN		TEFOVIE	TEFFIE	TEFHIE	TEFNEIE
0x0602	C1TEFCONH	15:8				FSIZE[4:0]				
		7:0								
0x0604	C1TEFSTA	15:8								
		7:0					TEFOVIF	TEFFIF	TEFHIF	TEFNEIF
0x0606 ... 0x0607	Reserved									
0x0608	C1TEFUAL	15:8	TEFUA[15:8]							
		7:0	TEFUA[7:0]							
0x060A	C1TEFUAH	15:8	TEFUA[31:24]							
		7:0	TEFUA[23:16]							
0x060C	C1FIFOBAL	15:8	FIFOBA[15:8]							
		7:0	FIFOBA[7:0]							
0x060E	C1FIFOBAH	15:8	FIFOBA[31:24]							
		7:0	FIFOBA[23:16]							
0x0610	C1TXQCONL	15:8						FRESET	TXREQ	UINC
		7:0	TXEN			TXATIE		TXQEIE		TXQNIE
0x0612	C1TXQCONH	15:8	PLSIZE[2:0]			FSIZE[4:0]				
		7:0		TXAT[1:0]		TXPRI[4:0]				
0x0614	C1TXQSTA	15:8				TXQCI[4:0]				
		7:0	TXABT	TXLARB	TXERR	TXATIF		TXQEIF		TXQNIF
0x0616 ... 0x0617	Reserved									
0x0618	C1TXQUAL	15:8	TXQUA[15:8]							
		7:0	TXQUA[7:0]							
0x061A	C1TXQUAH	15:8	TXQUA[31:24]							
		7:0	TXQUA[23:16]							
0x061C	C1FIFOCON1L	15:8						FRESET	TXREQ	UINC
		7:0	TXEN	RTREN	RXTSEN	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
0x061E	C1FIFOCON1H	15:8	PLSIZE[2:0]			FSIZE[4:0]				
		7:0		TXAT[1:0]		TXPRI[4:0]				
0x0620	C1FIFOSTA1	15:8				FIFOCI[4:0]				
		7:0	TXABT	TXLARB	TXERR	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
0x0622 ... 0x0623	Reserved									
0x0624	C1FIFOUA1L	15:8	FIFOUA[15:8]							
		7:0	FIFOUA[7:0]							
0x0626	C1FIFOUA1H	15:8	FIFOUA[31:24]							
		7:0	FIFOUA[23:16]							
0x0628	C1FIFOCON2L	15:8						FRESET	TXREQ	UINC
		7:0	TXEN	RTREN	RXTSEN	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
0x062A	C1FIFOCON2H	15:8	PLSIZE[2:0]			FSIZE[4:0]				
		7:0		TXAT[1:0]		TXPRI[4:0]				
0x062C	C1FIFOSTA2	15:8				FIFOCI[4:0]				
		7:0	TXABT	TXLARB	TXERR	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
0x062E ... 0x062F	Reserved									

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CAN Control/Status Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0630	C1FIFOUA2L	15:8	FIFOUA[15:8]							
		7:0	FIFOUA[7:0]							
0x0632	C1FIFOUA2H	15:8	FIFOUA[31:24]							
		7:0	FIFOUA[23:16]							
0x0634	C1FIFOCON3L	15:8						FRESET	TXREQ	UINC
		7:0	TXEN	RTREN	RXTSEN	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
0x0636	C1FIFOCON3H	15:8	PLSIZE[2:0]			FSIZE[4:0]				
		7:0		TXAT[1:0]		TXPRI[4:0]				
0x0638	C1FIFOSTA3	15:8				FIFOCI[4:0]				
		7:0	TXABT	TXLARB	TXERR	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
0x063A ... 0x063B	Reserved									
0x063C	C1FIFOUA3L	15:8	FIFOUA[15:8]							
		7:0	FIFOUA[7:0]							
0x063E	C1FIFOUA3H	15:8	FIFOUA[31:24]							
		7:0	FIFOUA[23:16]							
0x0640	C1FIFOCON4L	15:8						FRESET	TXREQ	UINC
		7:0	TXEN	RTREN	RXTSEN	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
0x0642	C1FIFOCON4H	15:8	PLSIZE[2:0]			FSIZE[4:0]				
		7:0		TXAT[1:0]		TXPRI[4:0]				
0x0644	C1FIFOSTA4	15:8				FIFOCI[4:0]				
		7:0	TXABT	TXLARB	TXERR	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
0x0646 ... 0x0647	Reserved									
0x0648	C1FIFOUA4L	15:8	FIFOUA[15:8]							
		7:0	FIFOUA[7:0]							
0x064A	C1FIFOUA4H	15:8	FIFOUA[31:24]							
		7:0	FIFOUA[23:16]							
0x064C	C1FIFOCON5L	15:8						FRESET	TXREQ	UINC
		7:0	TXEN	RTREN	RXTSEN	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
0x064E	C1FIFOCON5H	15:8	PLSIZE[2:0]			FSIZE[4:0]				
		7:0		TXAT[1:0]		TXPRI[4:0]				
0x0650	C1FIFOSTA5	15:8				FIFOCI[4:0]				
		7:0	TXABT	TXLARB	TXERR	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
0x0652 ... 0x0653	Reserved									
0x0654	C1FIFOUA5L	15:8	FIFOUA[15:8]							
		7:0	FIFOUA[7:0]							
0x0656	C1FIFOUA5H	15:8	FIFOUA[31:24]							
		7:0	FIFOUA[23:16]							
0x0658	C1FIFOCON6L	15:8						FRESET	TXREQ	UINC
		7:0	TXEN	RTREN	RXTSEN	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
0x065A	C1FIFOCON6 H	15:8	PLSIZE[2:0]			FSIZE[4:0]				
		7:0		TXAT[1:0]		TXPRI[4:0]				
0x065C	C1FIFOSTA6	15:8				FIFOCI[4:0]				
		7:0	TXABT	TXLARB	TXERR	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
0x065E ... 0x065F	Reserved									
0x0660	C1FIFOUA6 L	15:8	FIFOUA[15:8]							
		7:0	FIFOUA[7:0]							
0x0662	C1FIFOUA6H	15:8	FIFOUA[31:24]							
		7:0	FIFOUA[23:16]							
0x0664	C1FIFOCON7L	15:8						FRESET	TXREQ	UINC
		7:0	TXEN	RTREN	RXTSEN	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
0x0666	C1FIFOCON7H	15:8	PLSIZE[2:0]			FSIZE[4:0]				
		7:0		TXAT[1:0]		TXPRI[4:0]				

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CAN Control/Status Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0668	C1FIFOSTA7	15:8				FIFOCI[4:0]				
		7:0	TXABT	TXLARB	TXERR	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
0x066A ... 0x066B	Reserved									
0x066C	C1FIFOUA7L	15:8	FIFOUA[15:8]							
		7:0	FIFOUA[7:0]							
0x066E	C1FIFOUA7H	15:8	FIFOUA[31:24]							
		7:0	FIFOUA[23:16]							
0x0670	C1FIFOCON8L	15:8						FRESET	TXREQ	UINC
		7:0	TXEN	RTREN	RXTSEN	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
0x0672	C1FIFOCON8H	15:8	PLSIZE[2:0]			FSIZE[4:0]				
		7:0		TXAT[1:0]		TXPRI[4:0]				
0x0674	C1FIFOSTA8	15:8				FIFOCI[4:0]				
		7:0	TXABT	TXLARB	TXERR	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
0x0676 ... 0x0677	Reserved									
0x0678	C1FIFOUA8L	15:8	FIFOUA[15:8]							
		7:0	FIFOUA[7:0]							
0x067A	C1FIFOUA8H	15:8	FIFOUA[31:24]							
		7:0	FIFOUA[23:16]							
0x067C	C1FLTCON0L	15:8	FLTENb			FbBP[4:0]				
		7:0	FLTENa			FaBP[4:0]				
0x067E	C1FLTCON0H	15:8	FLTENd			FdBP[4:0]				
		7:0	FLTENc			FcBP[4:0]				
0x0680	C1FLTCON1L	15:8	FLTENb			FbBP[4:0]				
		7:0	FLTENa			FaBP[4:0]				
0x0682	C1FLTCON1H	15:8	FLTENd			FdBP[4:0]				
		7:0	FLTENc			FcBP[4:0]				
0x0684	C1FLTCON2L	15:8	FLTENb			FbBP[4:0]				
		7:0	FLTENa			FaBP[4:0]				
0x0686	C1FLTCON2H	15:8	FLTENd			FdBP[4:0]				
		7:0	FLTENc			FcBP[4:0]				
0x0688	C1FLTCON3L	15:8	FLTENb			FbBP[4:0]				
		7:0	FLTENa			FaBP[4:0]				
0x068A	C1FLTCON3H	15:8	FLTENd			FdBP[4:0]				
		7:0	FLTENc			FcBP[4:0]				
0x068C	C1FLTOBJ0L	15:8	EID[4:0]					SID[10:8]		
		7:0	SID[7:0]							
0x068E	C1FLTOBJ0H	15:8		EXIDE	SID11	EID[17:13]				
		7:0	EID[12:5]							
0x0690	C1MASK0L	15:8	MEID[4:0]					MSID[10:8]		
		7:0	MSID[7:0]							
0x0692	C1MASK1H	15:8		MIDE	MSID11	MEID[17:13]				
		7:0	MEID[12:5]							
0x0694	C1FLTOBJ1L	15:8	EID[4:0]					SID[10:8]		
		7:0	SID[7:0]							
0x0696	C1FLTOBJ1H	15:8		EXIDE	SID11	EID[17:13]				
		7:0	EID[12:5]							
0x0698	C1MASK1L	15:8	MEID[4:0]					MSID[10:8]		
		7:0	MSID[7:0]							
0x069A	C1MASK2H	15:8		MIDE	MSID11	MEID[17:13]				
		7:0	MEID[12:5]							
0x069C	C1FLTOBJ2L	15:8	EID[4:0]					SID[10:8]		
		7:0	SID[7:0]							
0x069E	C1FLTOBJ2H	15:8		EXIDE	SID11	EID[17:13]				
		7:0	EID[12:5]							
0x06A0	C1MASK2L	15:8	MEID[4:0]					MSID[10:8]		
		7:0	MSID[7:0]							

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CAN Control/Status Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x06A2	C1MASK3H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x06A4	C1FLTOBJ3L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				
0x06A6	C1FLTOBJ3H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x06A8	C1MASK3L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x06AA	C1MASK4H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x06AC	C1FLTOBJ4L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				
0x06AE	C1FLTOBJ4H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x06B0	C1MASK4L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x06B2	C1MASK5H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x06B4	C1FLTOBJ5L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				
0x06B6	C1FLTOBJ5H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x06B8	C1MASK5L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x06BA	C1MASK6H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x06BC	C1FLTOBJ6L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				
0x06BE	C1FLTOBJ6H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x06C0	C1MASK6L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x06C2	C1MASK7H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x06C4	C1FLTOBJ7L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				
0x06C6	C1FLTOBJ7H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x06C8	C1MASK7L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x06CA	C1MASK8H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x06CC	C1FLTOBJ8L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				
0x06CE	C1FLTOBJ8H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x06D0	C1MASK8L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x06D2	C1MASK9H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x06D4	C1FLTOBJ9L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				
0x06D6	C1FLTOBJ9H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x06D8	C1MASK9L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x06DA	C1MASK10H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x06DC	C1FLTOBJ10L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				

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CAN Control/Status Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x06DE	C1FLTOBJ10H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x06E0	C1MASK10L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x06E2	C1MASK11H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x06E4	C1FLTOBJ11L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				
0x06E6	C1FLTOBJ11H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x06E8	C1MASK11L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x06EA	C1MASK13H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x06EC	C1FLTOBJ13L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				
0x06EE	C1FLTOBJ13H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x06F0	C1MASK13L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x06F2	C1MASK14H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x06F4	C1FLTOBJ14L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				
0x06F6	C1FLTOBJ14H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x06F8	C1MASK14L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x06FA	C1MASK15H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x06FC	C1FLTOBJ15L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				
0x06FE	C1FLTOBJ15H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x0700	C1MASK15L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x0702	C1MASK16H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				
0x0704	C1FLTOBJ15L	15:8				EID[4:0]			SID[10:8]	
		7:0				SID[7:0]				
0x0706	C1FLTOBJ15H	15:8		EXIDE	SID11			EID[17:13]		
		7:0				EID[12:5]				
0x0708	C1MASK15L	15:8				MEID[4:0]			MSID[10:8]	
		7:0				MSID[7:0]				
0x070A	C1MASK15H	15:8		MIDE	MSID11			MEID[17:13]		
		7:0				MEID[12:5]				

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11.2.1. CAN Control Register Low

Name: C1CONL
Offset: 0x5C0

Note:
1. These bits can only be modified in Configuration mode (OPMOD[2:0] = 100).

Bit	15	14	13	12	11	10	9	8
	CON		SIDL	BRSDIS	BUSY	WFT[1:0]		WAKFIL
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	1	1	1

Bit	7	6	5	4	3	2	1	0
	CLKSEL	PXEDIS	ISOCRCEN	DNCNT[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	0	0	0	0	0

Bit 15 – CON CAN Enable bit

Value	Description
1	CAN module is enabled.
0	CAN module is disabled.

Bit 13 – SIDL CAN Stop in Idle Control bit

Value	Description
1	Stops module operation in Idle mode.
0	Does not stop module operation in Idle mode.

Bit 12 – BRSDIS Bit Rate Switching (BRS) Disable bit

Value	Description
1	Bit rate switching is disabled, regardless of BRS in the transmit message object.
0	Bit rate switching depends on BRS in the transmit message object.

Bit 11 – BUSY CAN Module is Busy bit

Value	Description
1	The CAN module is active.
0	The CAN module is inactive.

Bits 10:9 – WFT[1:0] Selectable Wake-up Filter Time bits

Value	Description
11	$T11_{FILTER}$
10	$T10_{FILTER}$
01	$T01_{FILTER}$
00	$T00_{FILTER}$

Bit 8 – WAKFIL Enable CAN Bus Line Wake-up Filter bit(1)

Value	Description
1	Uses CAN bus line filter for wake-up.
0	CAN bus line filter is not used for wake-up.

Bit 7 – CLKSEL Module Clock Source Select bit(1)

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Value	Description
1	REFO clock is used as the clock source to the CAN module.
0	Clock from the CAN clock generator is used as the clock source to the CAN module.

Bit 6 – PXEDIS Protocol Exception Event Detection Disabled bit(1)

A recessive "reserved bit" following a recessive FDF bit is called a Protocol Exception.

Value	Description
1	Protocol Exception is treated as a form error.
0	If a Protocol Exception is detected, CAN will enter the bus integrating state.

Bit 5 – ISOCRCEN Enable ISO CRC in CAN FD Frames bit(1)

Value	Description
1	Includes stuff bit count in CRC field and uses non-zero CRC initialization vector.
0	Does not include stuff bit count in CRC field and uses CRC initialization vector with all zeros.

Bits 4:0 – DNCNT[4:0] DeviceNet™ Filter Bit Number bits

Value	Description
10011-11111	Invalid selection (compares up to 18 bits of data with EID).
10010	Compares up to Data Byte 2, bit 6 with EID17.
. . .	
00001	Compares up to Data Byte 0, bit 7 with EID0.
00000	Does not compare data bytes.

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11.2.2. CAN Control Register High

Name: C1CONH
Offset: 0x5C2

Note:

1. These bits can only be modified in Configuration mode (OPMOD[2:0] = 100).

Legend: S = Settable bit; HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
	TXBWS[3:0]				ABAT	REQOP[2:0]		
Access	R/W	R/W	R/W	R/W	S/HC	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	0

Bit	7	6	5	4	3	2	1	0
	OPMOD[2:0]			TXQEN	STEF	SERRLOM	ESIGM	RTXAT
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	1	1	0	0	0

Bits 15:12 – TXBWS[3:0] Transmit Bandwidth Sharing bits

Value	Description
1111-1100	4096
1011	2048
1010	1024
1001	512
1000	256
0111	128
0110	64
0101	32
0100	16
0011	8
0010	4
0001	2
0000	No delay

Bit 11 – ABAT Abort All Pending Transmissions bit

Value	Description
1	Signals all transmit buffers to abort transmission.
0	Module will clear this bit when all transmissions are aborted.

Bits 10:8 – REQOP[2:0] Request Operation Mode bits

Value	Description
111	Sets Restricted Operation mode.
110	Sets Normal CAN 2.0 mode; error frames on CAN FD frames.
101	Sets External Loopback mode.
100	Sets Configuration mode.
011	Sets Listen Only mode.
010	Sets Internal Loopback mode.
001	Sets Disable mode.
000	Sets Normal CAN FD mode; supports mixing of full CAN FD and classic CAN 2.0 frames.

Bits 7:5 – OPMOD[2:0] Operation Mode Status bits

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Value	Description
111	Module is in Restricted Operation mode.
110	Module is in Normal CAN 2.0 mode; error frames on CAN FD frames.
101	Module is in External Loopback mode.
100	Module is in Configuration mode.
011	Module is in Listen Only mode.
010	Module is in Internal Loopback mode.
001	Module is in Disable mode.
000	Module is in Normal CAN FD mode; supports mixing of full CAN FD and classic CAN 2.0 frames.

Bit 4 – TXQEN Enable Transmit Queue bit(1)

Value	Description
1	Enables Transmit Message Queue (TXQ) and reserves space in RAM.
0	Does not reserve space in RAM for TXQ.

Bit 3 – STEF Store in Transmit Event FIFO bit(1)

Value	Description
1	Saves transmitted messages in TEF.
0	Does not save transmitted messages in TEF.

Bit 2 – SERRLOM Transition to Listen Only Mode on System Error bit(1)

Value	Description
1	Transitions to Listen Only mode.
0	Transitions to Restricted Operation mode.

Bit 1 – ESIGM Transmit ESI in Gateway Mode bit(1)

Value	Description
1	ESI is transmitted as recessive when ESI of the message is high or CAN controller is error passive.
0	ESI reflects error status of CAN controller.

Bit 0 – RTXAT Restrict Retransmission Attempts bit(1)

Value	Description
1	Restricted retransmission attempts, uses TXAT[1:0] bits (C1TXQCONH[6:5]).
0	Unlimited number of retransmission attempts, TXAT[1:0] bits will be ignored.

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11.2.3. CAN Nominal Bit Time Configuration Register Low

Name: C1NBTCFGL(1)
Offset: 0x5C6

Note:
1. This register can only be modified in Configuration mode (OPMOD[2:0] = 100).

Bit	15	14	13	12	11	10	9	8
		TSEG2[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	1	1	1	1

Bit	7	6	5	4	3	2	1	0
		SJW[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	1	1	1	1

Bits 14:8 – TSEG2[6:0] Time Segment 2 bits (Phase Segment 2)

Value	Description
111 1111	Length is 128 x T_Q
. . .	
000 0000	Length is 1 x T_Q

Bits 6:0 – SJW[6:0] Synchronization Jump Width bits

Value	Description
111 1111	Length is 128 x T_Q
. . .	
000 0000	Length is 1 x T_Q

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11.2.4. CAN Nominal Bit Time Configuration Register High

Name: C1NBTCFGH(1)
Offset: 0x5C6

Note:
1. This register can only be modified in Configuration mode (OPMOD[2:0] = 100).

Bit	15	14	13	12	11	10	9	8
	BRP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TSEG1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	1	1	0	0

Bits 15:8 – BRP[7:0] Baud Rate Prescaler bits

Value	Description
1111 1111	$T_Q = 256/F_{SYS}$
. . .	
0000 0000	$T_Q = 1/F_{SYS}$

Bits 7:0 – TSEG1[7:0] Time Segment 1 bits (Propagation Segment + Phase Segment 1)

Value	Description
1111 1111	Length is 256 x T_Q
. . .	
0000 0000	Length is 1 x T_Q

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11.2.5. CAN Data Bit Time Configuration Register Low

Name: C1DBTCFGL(1)
Offset: 0x5C8

Note:
1. This register can only be modified in Configuration mode (OPMOD[2:0] = 100).

Bit	15	14	13	12	11	10	9	8
					TSEG2[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	1	1

Bit	7	6	5	4	3	2	1	0
					SJW[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	1	1

Bits 11:8 – TSEG2[3:0] Time Segment 2 bits (Phase Segment 2)

Value	Description
1111	Length is 16 x T_Q
. . .	
0000	Length is 1 x T_Q

Bits 3:0 – SJW[3:0] Synchronization Jump Width bits

Value	Description
1111	Length is 16 x T_Q
. . .	
0000	Length is 1 x T_Q

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11.2.6. CAN Data Bit Time Configuration Register High

Name: C1DBTCFGH(1)
Offset: 0x5CA

Note:
1. This register can only be modified in Configuration mode (OPMOD[2:0] = 100).

Bit	15	14	13	12	11	10	9	8
	BRP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				TSEG1[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	1	1	1	0

Bits 15:8 – BRP[7:0] Baud Rate Prescaler bits

Value	Description
1111 1111	$T_Q = 256/F_{SYS}$
. . .	
0000 0000	$T_Q = 1/F_{SYS}$

Bits 4:0 – TSEG1[4:0] Time Segment 1 bits (Propagation Segment + Phase Segment 1)

Value	Description
1 1111	Length is 32 x T_Q
. . .	
0 0000	Length is 1 x T_Q

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11.2.7. CAN Transmitter Delay Compensation Register Low

Name: C1TDCL(1)
Offset: 0x5CC

Notes:
1. This register can only be modified in Configuration mode (OPMOD[2:0] = 100).
2. $T_{CAN} = 1/F_{CAN}$. F_{CAN} is the clock that comes out of the CAN clock generator.

Bit	15	14	13	12	11	10	9	8
		TDCO[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	1	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			TDCV[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 14:8 – TDCO[6:0] Transmitter Delay Compensation Offset bits (Secondary Sample Point (SSP))

Value	Description
111 1111	-64 x T_{CAN}
. . .	
011 1111	63 x T_{CAN}
. . .	
000 0000	0 x T_{CAN}

Bits 5:0 – TDCV[5:0] Transmitter Delay Compensation Value bits (Secondary Sample Point (SSP))

Value	Description
11 1111	63 x T_{CAN}
. . .	
00 0000	0 x T_{CAN}

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11.2.8. CAN Transmitter Delay Compensation Register High

Name: C1TDCH(1)
Offset: 0x5CE

Note:
1. This register can only be modified in Configuration mode (OPMOD[2:0] = 100).

Bit	15	14	13	12	11	10	9	8
							EDGFLTEN	SID11EN
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
							TDCMOD[1:0]	
Access							R/W	R/W
Reset							1	0

Bit 9 – EDGFLTEN Enable Edge Filtering During Bus Integration State bit

Value	Description
1	Edge filtering is enabled according to ISO 11898-1:2015.
0	Edge filtering is disabled.

Bit 8 – SID11EN Enable 12-Bit SID in CAN FD Base Format Messages bit

Value	Description
1	RRS is used as SID11 in CAN FD base format messages: SID[11:0] = {SID[10:0], SID11}.
0	Does not use RRS; SID[10:0].

Bits 1:0 – TDCMOD[1:0] Transmitter Delay Compensation Mode bits (Secondary Sample Point (SSP))

Value	Description
10-11	Auto: Measures delay and adds TDCO[6:0]
01	Manual: Does not measure, uses TDCV[5:0] + TDCO[6:0] from register
00	Disabled

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11.2.9. CAN Time Base Counter Register Low

Name: C1TBCL(1,2)
Offset: 0x5D0

Notes:

1. The Time Base Counter (TBC) will be stopped and reset when TBCEN = 0 to save power.
2. The TBC prescaler count will be reset on any write to C1TBCH/L (TBCPREx will be unaffected).

Bit	15	14	13	12	11	10	9	8
	TBC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TBC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TBC[15:0] CAN Time Base Counter bits
This is a free-running timer that increments every TBCPREx clock when TBCEN is set.

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11.2.10. CAN Time Base Counter Register High

Name: C1TBCH(1,2)
Offset: 0x5D2

Notes:

1. The Time Base Counter (TBC) will be stopped and reset when TBCEN = 0 to save power.
2. The TBC prescaler count will be reset on any write to C1TBCH/L (TBCPREx will be unaffected).

Bit	15	14	13	12	11	10	9	8
	TBC[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TBC[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TBC[31:16] CAN Time Base Counter bits
This is a free-running timer that increments every TBCPREx clock when TBCEN is set.

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11.2.11. CAN Timestamp Control Register Low

Name: C1TSCONL
Offset: 0x5D4

Bit	15	14	13	12	11	10	9	8
							TBCPRE[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	TBCPRE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – TBCPRE[9:0] CAN Time Base Counter Prescaler bits

Value	Description
1023	TBC increments every 1024 clocks
. . .	
0	TBC increments every 1 clock

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11.2.12. CAN Timestamp Control Register High

Name: C1TSCONH
Offset: 0x5D6

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						TSRES	TSEOF	TBCEN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – TSRES Timestamp Reset bit (CAN FD frames only)

Value	Description
1	At sample point of the bit following the FDF bit
0	At sample point of Start-of-Frame (SOF)

Bit 1 – TSEOF Timestamp End-of-Frame (EOF) bit

Value	Description
1	Timestamp when frame is taken valid (11898-1 10.7): • RX no error until last, but one bit of EOF • TX no error until the end of EOF
0	Timestamp at “beginning” of frame: • Classical Frame: At sample point of SOF • FD Frame: See TSRES bit

Bit 0 – TBCEN Time Base Counter Enable bit

Value	Description
1	Enables TBC
0	Stops and resets TBC

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11.2.13. CAN Interrupt Code Register Low

Name: C1VECL
Offset: 0x5D8

Bit	15	14	13	12	11	10	9	8
				FILHIT[4:0]				
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		ICODE[6:0]						
Access		R	R	R	R	R	R	R
Reset		1	0	0	0	0	0	0

Bits 12:8 – FILHIT[4:0] Filter Hit Number bits

Value	Description
01111	Filter 15
01110	Filter 14
. . .	
00001	Filter 1
00000	Filter 0

Bits 6:0 – ICODE[6:0] Interrupt Flag Code bits

Value	Description
1001011-1111111	Reserved
1001010	Transmit attempt interrupt (any bit in C1TXATIF is set)
1001001	Transmit event FIFO interrupt (any bit in C1TEFSTA is set)
1001000	Invalid message occurred (IVMIF/IE)
1000111	CAN module mode change occurred (MODIF/IE)
1000110	CAN timer overflow (TBCIF/IE)
1000101	RX/TX MAB overflow/underflow (RX: Message received before previous message was saved to memory; TX: Can't feed TX MAB fast enough to transmit consistent data)
1000100	Address error interrupt (illegal FIFO address presented to system)
1000011	Receive FIFO overflow interrupt (any bit in C1RXOVIF is set)
1000010	Wake-up interrupt (WAKIF/WAKIE)
1000001	Error interrupt (CERRIF/IE)
1000000	No interrupt
0001000-0111111	Reserved
0000111	FIFO 7 interrupt (TFIF7 or RFIF7 is set)
. . .	
0000001	FIFO 1 interrupt (TFIF1 or RFIF1 is set)
0000000	FIFO 0 interrupt (TFIF0 is set)

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11.2.14. CAN Interrupt Code Register High

Name: C1VECH
Offset: 0x5DA

Bit	15	14	13	12	11	10	9	8
		RXCODE[6:0]						
Access		R	R	R	R	R	R	R
Reset		1	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		TXCODE[6:0]						
Access		R	R	R	R	R	R	R
Reset		1	0	0	0	0	0	0

Bits 14:8 – RXCODE[6:0] Receive Interrupt Flag Code bits

Value	Description
1000001-1111111	Reserved
1000000	No interrupt
0001000-0111111	Reserved
0000111	FIFO 7 interrupt (RFIF7 is set)
. . .	
0000010	FIFO 2 interrupt (RFIF2 is set)
0000001	FIFO 1 interrupt (RFIF1 is set)
0000000	Reserved; FIFO 0 cannot receive

Bits 6:0 – TXCODE[6:0] Transmit Interrupt Flag Code bits

Value	Description
1000001-1111111	Reserved
1000000	No interrupt
0001000-0111111	Reserved
0000111	FIFO 7 interrupt (TFIF7 is set)
. . .	
0000001	FIFO 1 interrupt (TFIF1 is set)
0000000	FIFO 0 interrupt (TFIF0 is set)

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11.2.15. CAN Interrupt Register Low

Name: C1INTL
Offset: 0x5DC

Note:

1. C1INTL: Flags are set by hardware and cleared by application.

Legend: C = Clearable bit; HS = Hardware Settable bit

Bit	15	14	13	12	11	10	9	8
	IVMIF	WAKIF	CERRIF	SERRIF	RXOVIF	TXATIF		
Access	HS/C	HS/C	HS/C	HS/C	R	R		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
				TEFIF	MODIF	TBCIF	RXIF	TXIF
Access				R	HS/C	HS/C	R	R
Reset				0	0	0	0	0

Bit 15 – IVMIF Invalid Message Interrupt Flag bit(1)

Value	Description
1	Invalid message interrupt occurred.
0	No invalid message interrupt.

Bit 14 – WAKIF Bus Wake-up Activity Interrupt Flag bit(1)

Value	Description
1	Wake-up activity interrupt occurred.
0	No wake-up activity interrupt.

Bit 13 – CERRIF CAN Bus Error Interrupt Flag bit(1)

Value	Description
1	CAN bus error interrupt occurred.
0	No CAN bus error interrupt.

Bit 12 – SERRIF System Error Interrupt Flag bit(1)

Value	Description
1	System error interrupt occurred.
0	No system error interrupt.

Bit 11 – RXOVIF Receive Buffer Overflow Interrupt Flag bit

Value	Description
1	Receive buffer overflow interrupt occurred.
0	No receive buffer overflow interrupt.

Bit 10 – TXATIF Transmit Attempt Interrupt Flag bit

Value	Description
1	Transmit attempt interrupt occurred.
0	No transmit attempt interrupt.

Bit 4 – TEFIF Transmit Event FIFO Interrupt Flag bit

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Value	Description
1	Transmit event FIFO interrupt occurred.
0	No transmit event FIFO interrupt.

Bit 3 – MODIF CAN Mode Change Interrupt Flag bit(1)

Value	Description
1	CAN module mode change occurred (OPMOD[2:0] has changed to reflect REQOP[2:0]).
0	No mode change occurred.

Bit 2 – TBCIF CAN Timer Overflow Interrupt Flag bit(1)

Value	Description
1	TBC has overflowed.
0	TBC has not overflowed.

Bit 1 – RXIF Receive Object Interrupt Flag bit

Value	Description
1	Receive object interrupt is pending.
0	No receive object interrupts are pending.

Bit 0 – TXIF Transmit Object Interrupt Flag bit

Value	Description
1	Transmit object interrupt is pending.
0	No transmit object interrupts are pending.

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11.2.16. CAN Interrupt Register High

Name: C1INTH
Offset: 0x5DE

Bit	15	14	13	12	11	10	9	8
	IVMIE	WAKIE	CERRIE	SERRIE	RXOVIE	TXATIE		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
				TEFIE	MODIE	TBCIE	RXIE	TXIE
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 15 – IVMIE Invalid Message Interrupt Enable bit

Value	Description
1	Invalid message interrupt is enabled.
0	Invalid message interrupt is disabled.

Bit 14 – WAKIE Bus Wake-up Activity Interrupt Enable bit

Value	Description
1	Wake-up activity interrupt is enabled.
0	Wake-up Activity Interrupt is disabled.

Bit 13 – CERRIE CAN Bus Error Interrupt Enable bit

Value	Description
1	CAN bus error interrupt is enabled.
0	CAN bus error interrupt is disabled.

Bit 12 – SERRIE System Error Interrupt Enable bit

Value	Description
1	System error interrupt is enabled.
0	System error interrupt is disabled.

Bit 11 – RXOVIE Receive Buffer Overflow Interrupt Enable bit

Value	Description
1	Receive buffer overflow interrupt is enabled.
0	Receive buffer overflow interrupt is disabled.

Bit 10 – TXATIE Transmit Attempt Interrupt Enable bit

Value	Description
1	Transmit attempt interrupt is enabled.
0	Transmit attempt interrupt is disabled.

Bit 4 – TEFIE Transmit Event FIFO Interrupt Enable bit

Value	Description
1	Transmit event FIFO interrupt is enabled.
0	Transmit event FIFO interrupt is disabled.

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Bit 3 – MODIE Mode Change Interrupt Enable bit

Value	Description
1	Mode change interrupt is enabled.
0	Mode change interrupt is disabled.

Bit 2 – TBCIE CAN Timer Interrupt Enable bit

Value	Description
1	CAN timer interrupt is enabled.
0	CAN timer interrupt is disabled.

Bit 1 – RXIE Receive Object Interrupt Enable bit

Value	Description
1	Receive object interrupt is enabled.
0	Receive object interrupt is disabled.

Bit 0 – TXIE Transmit Object Interrupt Enable bit

Value	Description
1	Transmit object interrupt is enabled.
0	Transmit object interrupt is disabled.

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11.2.17. CAN Receive Interrupt Status Register Low

Name: C1RXIFL(1)
Offset: 0x5E0

Note:

1. C1RXIFL: FIFO: RFIFx = 'or' of enabled RX FIFO flags (flags need to be cleared in the FIFO register).

Bit	15	14	13	12	11	10	9	8
	RFIF[15:8]							
Access	U	U	U	U	U	U	U	U
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RFIF[7:1]							
Access	R	R	R	R	R	R	R	
Reset	0	0	0	0	0	0	0	

Bits 15:8 – RFIF[15:8] Unimplemented

Bits 7:1 – RFIF[7:1] Receive FIFO Interrupt Pending bits

Value	Description
1	One or more enabled receive FIFO interrupts are pending.
0	No enabled receive FIFO interrupts are pending.

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11.2.18. CAN Receive Interrupt Status Register High

Name: C1RXIFH(1)
Offset: 0x5E2

Note:

1. C1RXIFH: FIFO: RFIFx = 'or' of enabled RX FIFO flags (flags need to be cleared in the FIFO register).

Bit	15	14	13	12	11	10	9	8
	RFIF[31:24]							
Access	U	U	U	U	U	U	U	U
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RFIF[23:16]							
Access	U	U	U	U	U	U	U	U
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RFIF[31:16] Unimplemented

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11.2.19. CAN Transmit Interrupt Status Register

Name: C1TXIFL(1)
Offset: 0x5E4

Note:

1. C1TXIFL: FIFO: TFIFx = 'or' of the enabled TX FIFO flags (flags need to be cleared in the FIFO register).
2. TFIF is for the Transmit Queue.

Bit	15	14	13	12	11	10	9	8
	TFIF[7:0]							
Access	U	U	U	U	U	U	U	U
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TFIF[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – TFIF[7:0] Unimplemented

Bits 7:0 – TFIF[7:0] Transmit FIFO/TXQ Interrupt Pending bits(2)

Value	Description
1	One or more enabled transmit FIFO/TXQ interrupts are pending.
0	No enabled transmit FIFO/TXQ interrupts are pending.

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11.2.20. CAN Transmit Interrupt Status Register High

Name: C1TXIFH(1)
Offset: 0x5E6

Note:

1. C1TXIFH: FIFO: TFIFx = 'or' of the enabled TX FIFO flags (flags need to be cleared in the FIFO register).

Bit	15	14	13	12	11	10	9	8
	TFIF[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TFIF[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TFIF[31:16] Unimplemented

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11.2.21. CAN Receive Overflow Interrupt Status Register Low

Name: C1RXOVIFL(1)
Offset: 0x5E8

Note:

1. C1RXOVIFL: FIFO: RFOVIFx (flag needs to be cleared in the FIFO register).

Bit	15	14	13	12	11	10	9	8
	RFOVIF[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RFOVIF[7:1]							
Access	R	R	R	R	R	R	R	
Reset	0	0	0	0	0	0	0	

Bits 15:8 – RFOVIF[15:8] Unimplemented

Bits 7:1 – RFOVIF[7:1] Receive FIFO Overflow Interrupt Pending bits

Value	Description
1	Interrupt is pending.
0	Interrupt is not pending.

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11.2.22. CAN Receive Overflow Interrupt Status Register High

Name: C1RXOVIFH(1)
Offset: 0x5EA

Note:

1. C1RXOVIFH: FIFO: RFOVIFx (flag needs to be cleared in the FIFO register).

Bit	15	14	13	12	11	10	9	8
	RFOVIF[31:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 15:8 – RFOVIF[31:16] Unimplemented

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11.2.23. CAN Transmit Attempt Interrupt Status Register Low

Name: C1TXATIFL(1)
Offset: 0x5EC

Notes:
1. C1TXATIFL: FIFO: TFATIFx (flag needs to be cleared in the FIFO register).
2. TFATIF0 is for the Transmit Queue.

Bit	15	14	13	12	11	10	9	8
	TFATIF[15:8]							
Access	U	U	U	U	U	U	U	U
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TFATIF[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – TFATIF[15:8] Unimplemented

Bits 7:0 – TFATIF[7:0] Transmit FIFO/TXQ Attempt Interrupt Pending bits(2)

Value	Description
1	Interrupt is pending.
0	Interrupt is not pending.

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11.2.24. CAN Transmit Attempt Interrupt Status Register High

Name: C1TXATIFH(1)
Offset: 0x5EE

Note:

1. C1TXATIFH: FIFO: TFATIFx (flag needs to be cleared in the FIFO register).

Bit	15	14	13	12	11	10	9	8
	TFATIF[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TFATIF[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TFATIF[31:16] Unimplemented

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11.2.25. CAN Transmit Request Register Low

Name: C1TXREQL
Offset: 0x5F0

Legend: S = Settable bit; HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
	TXREQ[15:8]							
Access	U	U	U	U	U	U	U	U
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXREQ[7:1]							TXREQ0
Access	S/HC	S/HC	S/HC	S/HC	S/HC	S/HC	S/HC	S/HC
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – TXREQ[15:8] Unimplemented

Bits 7:1 – TXREQ[7:1] Message Send Request bits
TXEN = 1 (object configured as a transmit object):
Setting this bit to '1' requests sending a message. The bit will automatically clear when the message(s) queued in the object is (are) successfully sent. This bit can NOT be used for aborting a transmission.
TXEN = 0 (object configured as a receive object):
This bit has no effect.

Bit 0 – TXREQ0 Transmit Queue Message Send Request bit
Setting this bit to '1' requests sending a message. The bit will automatically clear when the message(s) queued in the object is (are) successfully sent. This bit can NOT be used for aborting a transmission.

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11.2.26. CAN Transmit Request Register High

Name: C1TXREQH
Offset: 0x5F2

Bit	15	14	13	12	11	10	9	8
	TXREQ[31:24]							
Access	U	U	U	U	U	U	U	U
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXREQ[23:16]							
Access	U	U	U	U	U	U	U	U
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TXREQ[31:16] Unimplemented

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11.2.27. CAN Transmit/Receive Error Count Register Low

Name: C1TRECL
Offset: 0x5F4

Bit	15	14	13	12	11	10	9	8
	TERRCNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RERRCNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – TERRCNT[7:0] Transmit Error Counter bits

Bits 7:0 – RERRCNT[7:0] Receive Error Counter bits

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11.2.28. CAN Transmit/receive Error Count Register High

Name: C1TRECH
Offset: 0x5F6

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
Access			R	R	R	R	R	R
Reset			1	0	0	0	0	0

Bit 5 – TXBO Transmitter in Bus Off Error State bit (TERRCNT[7:0] > 255)
In Configuration mode, TXBO is set since the module is not on the bus.

Bit 4 – TXBP Transmitter in Bus Passive Error State bit (TERRCNT[7:0] > 127)

Bit 3 – RXBP Receiver in Bus Passive Error State bit (RERRCNT[7:0] > 127)

Bit 2 – TXWARN Transmitter in Warning State bit (128 > TERRCNT[7:0] > 95)

Bit 1 – RXWARN Receiver in Warning State bit (128 > RERRCNT[7:0] > 95)

Bit 0 – EWARN Transmitter or Receiver in Warning State bit

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11.2.29. CAN Bus Diagnostics Register 0 Low

Name: C1BDIAG0L
Offset: 0x5F8

Bit	15	14	13	12	11	10	9	8
	NTERRCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NRERRCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – NTERRCNT[7:0] Nominal Bit Rate Transmit Error Counter bits

Bits 7:0 – NRERRCNT[7:0] Nominal Bit Rate Receive Error Counter bits

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11.2.30. CAN Bus Diagnostics Register 0 High

Name: C1BDIAG0H
Offset: 0x5FA

Bit	15	14	13	12	11	10	9	8
	DTERRCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DRERRCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – DTERRCNT[7:0] Data Bit Rate Transmit Error Counter bits

Bits 7:0 – DRERRCNT[7:0] Data Bit Rate Receive Error Counter bits

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11.2.31. CAN Bus Diagnostics Register 1 Low

Name: C1BDIAG1L
Offset: 0x5FC

Bit	15	14	13	12	11	10	9	8
	EFMSGCNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	EFMSGCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – EFMSGCNT[15:0] Error-Free Message Counter bits

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11.2.32. CAN Bus Diagnostics Register 1 High

Name: C1BDIAG1H
Offset: 0x5FE

Bit	15	14	13	12	11	10	9	8
	DLCMM	ESI	DCRCERR	DSTUFERR	DFORMERR		DBIT1ERR	DBIT0ERR
Access	R/W	R/W	R/W	R/W	R/W		R/W	R/W
Reset	0	0	0	0	0		0	0

Bit	7	6	5	4	3	2	1	0
	TXBOERR		NCRCERR	NSTUFERR	NFORMERR	NACKERR	NBIT1ERR	NBIT0ERR
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 15 – DLCMM DLC Mismatch bit
During a transmission or reception, the specified DLC is larger than the PLSIZE[2:0] of the FIFO element.

Bit 14 – ESI ESI Flag of a Received CAN FD Message Set bit

Bit 13 – DCRCERR Same as for nominal bit rate

Bit 12 – DSTUFERR Same as for nominal bit rate

Bit 11 – DFORMERR Same as for nominal bit rate

Bit 9 – DBIT1ERR Same as for nominal bit rate

Bit 8 – DBIT0ERR Same as for nominal bit rate

Bit 7 – TXBOERR Device Went to Bus Off bit (and auto-recovered)

Bit 5 – NCRCERR Received Message with CRC Incorrect Checksum bit
The CRC checksum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data.

Bit 4 – NSTUFERR Received Message with Illegal Sequence bit
More than five equal bits in a sequence have occurred in a part of a received message where this is not allowed.

Bit 3 – NFORMERR Received Frame Fixed Format bit
A fixed format part of a received frame has the wrong format.

Bit 2 – NACKERR Transmitted Message Not Acknowledged bit
Transmitted message was not Acknowledged.

Bit 1 – NBIT1ERR Transmitted Message Recessive Level bit
During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant.

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Bit 0 – NBIT0ERR Transmitted Message Dominant Level bit

During the transmission of a message (or Acknowledge bit, active error flag or overload flag), the device wanted to send a dominant level (data or identifier bit of logical value '0'), but the monitored bus value was recessive. During bus off recovery, this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the bus off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed).

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11.2.33. CAN Transmit Event FIFO Control Register Low

Name: C1TEFCONL
Offset: 0x600

Legend: S = Settable bit; HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
						FRESET		UINC
Access						S/HC		S/HC
Reset						1		0

Bit	7	6	5	4	3	2	1	0
			TEFTSEN		TEFOVIE	TEFFIE	TEFHIE	TEFNEIE
Access			R/W		R/W	R/W	R/W	R/W
Reset			0		0	0	0	0

Bit 10 – FRESET FIFO Reset bit

Value	Description
1	FIFO will be reset when the bit is set and cleared by hardware when the FIFO is reset; the user should poll whether this bit is clear before taking any action.
0	No effect.

Bit 8 – UINC Increment Tail bit

Value	Description
1	When this bit is set, the FIFO tail will increment by a single message.
0	FIFO tail will not increment.

Bit 5 – TEFTSEN Transmit Event FIFO Timestamp Enable bit

Value	Description
1	Timestamp elements in TEF.
0	Does not timestamp elements in TEF.

Bit 3 – TEFOVIE Transmit Event FIFO Overflow Interrupt Enable bit

Value	Description
1	Interrupt is enabled for overflow event.
0	Interrupt is disabled for overflow event.

Bit 2 – TEFFIE Transmit Event FIFO Full Interrupt Enable bit

Value	Description
1	Interrupt is enabled for FIFO full.
0	Interrupt is disabled for FIFO full.

Bit 1 – TEFHIE Transmit Event FIFO Half Full Interrupt Enable bit

Value	Description
1	Interrupt is enabled for FIFO half full.
0	Interrupt is disabled for FIFO half full.

Bit 0 – TEFNEIE Transmit Event FIFO Not Empty Interrupt Enable bit

Value	Description
1	Interrupt is enabled for FIFO not empty.

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Value	Description
0	Interrupt is disabled for FIFO not empty.

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11.2.34. CAN Transmit Event FIFO Control Register High

Name: C1TEFCONH
Offset: 0x602

Note:

1. These bits can only be modified in Configuration mode (OPMOD[2:0] = 100).

Bit	15	14	13	12	11	10	9	8
				FSIZE[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 12:8 – FSIZE[4:0] FIFO Size bits(1)

Value	Description
11111	FIFO is 32 messages deep
...	
00010	FIFO is 3 messages deep
00001	FIFO is 2 messages deep
00000	FIFO is 1 message deep

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11.2.35. CAN Transmit Event FIFO Status Register

Name: C1TEFSTA
Offset: 0x604

Note:

1. These bits are read-only and reflect the status of the FIFO.

Legend: HC = Hardware Clearable bit; S = Settable bit can Set by '1'

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					TEFOVIF	TEFFIF	TEFHIF	TEFNEIF
Access					S/HC	R	R	R
Reset					0	0	0	0

Bit 3 – TEFOVIF Transmit Event FIFO Overflow Interrupt Flag bit

Value	Description
1	Overflow event has occurred.
0	No overflow event has occurred.

Bit 2 – TEFFIF Transmit Event FIFO Full Interrupt Flag bit(1)

Value	Description
1	FIFO is full.
0	FIFO is not full.

Bit 1 – TEFHIF Transmit Event FIFO Half Full Interrupt Flag bit(1)

Value	Description
1	FIFO is ≥ half full.
0	FIFO is < half full.

Bit 0 – TEFNEIF Transmit Event FIFO Not Empty Interrupt Flag bit(1)

Value	Description
1	FIFO is not empty.
0	FIFO is empty.

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11.2.36. CAN Transmit Event FIFO User Address Register Low

Name: C1TEFUAL(1)
Offset: 0x608

Note:

1. This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
	TEFUA[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	TEFUA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 15:0 – TEFUA[15:0] Transmit Event FIFO User Address bits
A read of this register will return the address where the next event is to be read (FIFO tail).

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11.2.37. CAN Transmit Event FIFO User Address Register High

Name: C1TEFUAH(1)
Offset: 0x60A

Note:

1. This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
	TEFUA[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	TEFUA[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 15:0 – TEFUA[31:16] Transmit Event FIFO User Address bits
A read of this register will return the address where the next event is to be read (FIFO tail).

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11.2.38. CAN Message Memory Base Address Register Low

Name: C1FIFOBAL
Offset: 0x60C

Bit	15	14	13	12	11	10	9	8
	FIFOBA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FIFOBA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – FIFOBA[15:0] Message Memory Base Address bits
Defines the base address for the transmit event FIFO followed by the message objects.

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11.2.39. CAN Message Memory Base Address Register High

Name: C1FIFOBAH
Offset: 0x60E

Bit	15	14	13	12	11	10	9	8
	FIFOBA[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FIFOBA[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – FIFOBA[31:16] Message Memory Base Address bits
Defines the base address for the transmit event FIFO followed by the message objects.

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11.2.40. CAN Transmit Queue Control Register Low

Name: C1TXQCONL
Offset: 0x610

Legend: HS = Hardware Settable bit; C = Clearable bit

Bit	15	14	13	12	11	10	9	8
						FRESET	TXREQ	UINC
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
	TXEN			TXATIE		TXQEIE		TXQNIE
Access	R			HS/C		R/W		R/W
Reset	0			0		0		0

Bit 10 – FRESET FIFO Reset bit

Value	Description
1	FIFO will be reset when bit is set, cleared by hardware when FIFO is reset; user should poll whether this bit is clear before taking any action.
0	No effect.

Bit 9 – TXREQ Message Send Request bit

Value	Description
1	Requests sending a message; the bit will automatically clear when all the messages queued in the TXQ are successfully sent.
0	Clearing the bit to '0' while set ('1') will request a message abort.

Bit 8 – UINC Increment Head/Tail bit
When this bit is set, the FIFO head will increment by a single message.

Bit 7 – TXEN TX Enable bit

Bit 4 – TXATIE Transmit Attempts Exhausted Interrupt Enable bit

Value	Description
1	Enables interrupt.
0	Disables interrupt.

Bit 2 – TXQEIE Transmit Queue Empty Interrupt Enable bit

Value	Description
1	Interrupt is enabled for TXQ empty.
0	Interrupt is disabled for TXQ empty.

Bit 0 – TXQNIE Transmit Queue Not Full Interrupt Enable bit

Value	Description
1	Interrupt is enabled for TXQ not full.
0	Interrupt is disabled for TXQ not full.

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11.2.41. CAN Transmit Queue Control Register High

Name: C1TXQCONH
Offset: 0x612

Note:
1. These bits can only be modified in Configuration mode (OPMOD[2:0] = 100).

Bit	15	14	13	12	11	10	9	8
	PLSIZE[2:0]			FSIZE[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		TXAT[1:0]		TXPRI[4:0]				
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	1	0	0	0	0	0

Bits 15:13 – PLSIZE[2:0] Payload Size bits(1)

Value	Description
111	64 data bytes
110	48 data bytes
101	32 data bytes
100	24 data bytes
011	20 data bytes
010	16 data bytes
001	12 data bytes
000	8 data bytes

Bits 12:8 – FSIZE[4:0] FIFO Size bits(1)

Value	Description
11111	FIFO is 32 messages deep.
. . .	
00010	FIFO is 3 messages deep.
00001	FIFO is 2 messages deep.
00000	FIFO is 1 message deep.

Bits 6:5 – TXAT[1:0] Retransmission Attempts bits
This feature is enabled when RTXAT (C1CONH[0]) is set.

Value	Description
11	Unlimited number of retransmission attempts.
10	Unlimited number of retransmission attempts
01	Three retransmission attempts.
00	Disables retransmission attempts.

Bits 4:0 – TXPRI[4:0] Message Transmit Priority bits

Value	Description
11111	Highest message priority.
. . .	
00000	Lowest message priority.

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11.2.42. CAN Transmit Queue Status Register

Name: C1TXQSTA
Offset: 0x614

Notes:

1. The TXQCI[4:0] bits give a zero-indexed value to the message in the TXQ. If the TXQ is four messages deep (FSIZE[4:0] = 3), TXQCIx will take on a value of 0 to 3, depending on the state of the TXQ.
2. This bit is updated when a message completes (or aborts) or when the TXQ is reset.

Legend: HS = Hardware Settable bit; C = Clearable bit

Bit	15	14	13	12	11	10	9	8
				TXQCI[4:0]				
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXABT	TXLARB	TXERR	TXATIF		TXQEIF		TXQNIF
Access	R	R	R	HS/C		R		R
Reset	0	0	0	0		1		1

Bits 12:8 – TXQCI[4:0] Transmit Message Queue Index bits(1)
A read of this register will return an index to the message that the FIFO will next attempt to transmit.

Bit 7 – TXABT Message Aborted Status bit(2)

Value	Description
1	Message was aborted.
0	Message completed successfully.

Bit 6 – TXLARB Message Lost Arbitration Status bit

Value	Description
1	Message lost arbitration while being sent.
0	Message did not lose arbitration while being sent.

Bit 5 – TXERR Error Detected During Transmission bit

Value	Description
1	A bus error occurred while the message was being sent.
0	A bus error did not occur while the message was being sent.

Bit 4 – TXATIF Transmit Attempts Exhausted Interrupt Pending bit

Value	Description
1	Interrupt is pending.
0	Interrupt is not pending.

Bit 2 – TXQEIF Transmit Queue Empty Interrupt Flag bit

Value	Description
1	TXQ is empty.
0	TXQ is not empty, at least one message is queued to be transmitted.

Bit 0 – TXQNIF Transmit Queue Not Full Interrupt Flag bit

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Value	Description
1	TXQ is not full.
0	TXQ is full.

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11.2.43. CAN Transmit Queue User Address Register Low

Name: C1TXQUAL(1)
Offset: 0x618

Note:

1. This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
	TXQUA[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	TXQUA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 15:0 – TXQUA[15:0] TXQ User Address bits
A read of this register will return the address where the next message is to be written (TXQ head).

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11.2.44. CAN Transmit Queue User Address Register High

Name: C1TXQUAH(1)
Offset: 0x61A

Note:

1. This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
	TXQUA[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	TXQUA[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 15:0 – TXQUA[31:16] TXQ User Address bits
A read of this register will return the address where the next message is to be written (TXQ head).

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11.2.45. CAN FIFO Control Register x Low (x = 1 to 8)

Name: C1FIFOCONxL
Offset: 0x61C, 0x628, 0x634, 0x640, 0x64C, 0x658, 0x664, 0x670

Note:
1. This bit can only be modified in Configuration mode (OPMOD[2:0] = 100).

Legend: S = Settable bit; HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
						FRESET	TXREQ	UINC
Access						S/HC	R/W/HC	S/HC
Reset						1	0	0

Bit	7	6	5	4	3	2	1	0
	TXEN	RTREN	RXTSEN	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 10 – FRESET FIFO Reset bit

Value	Description
1	FIFO will be reset when the bit is set and cleared by hardware when the FIFO is reset; the user should poll whether this bit is clear before taking any action.
0	No effect.

Bit 9 – TXREQ Message Send Request bit

TXEN = 0 (FIFO configured as a receive FIFO):
This bit has no effect.
TXEN = 1 (FIFO configured as a transmit FIFO):

Value	Description
1	Requests sending a message; the bit will automatically clear when all the messages queued in the FIFO are successfully sent.
0	Clearing the bit to '0' while set ('1') will request a message abort.

Bit 8 – UINC Increment Head/Tail bit

TXEN = 1 (FIFO configured as a transmit FIFO):
When this bit is set, the FIFO head will increment by a single message.
TXEN = 0 (FIFO configured as a receive FIFO):
When this bit is set, the FIFO tail will increment by a single message.

Bit 7 – TXEN TX/RX Buffer Selection bit

Value	Description
1	Transmits message object.
0	Receives message object.

Bit 6 – RTREN Auto-Remote Transmit (RTR) Enable bit

Value	Description
1	When a Remote Transmit is received, TXREQ will be set.
0	When a Remote Transmit is received, TXREQ will be unaffected.

Bit 5 – RXTSEN Received Message Timestamp Enable bit(1)

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Value	Description
1	Captures the timestamp in the received message object in RAM.
0	Does not capture the timestamp.

Bit 4 – TXATIE Transmit Attempts Exhausted Interrupt Enable bit

Value	Description
1	Enables interrupt.
0	Disables interrupt.

Bit 3 – RXOVIE Overflow Interrupt Enable bit

Value	Description
1	Interrupt is enabled for overflow event.
0	Interrupt is disabled for overflow event.

Bit 2 – TFERFFIE Transmit/Receive FIFO Empty/Full Interrupt Enable bit

TXEN = 1 (FIFO configured as a transmit FIFO):
Transmit FIFO Empty Interrupt Enable.

Value	Description
1	Interrupt is enabled for FIFO empty.
0	Interrupt is disabled for FIFO empty.

TXEN = 0 (FIFO configured as a receive FIFO):
Receive FIFO Full Interrupt Enable.

Value	Description
1	Interrupt is enabled for FIFO full.
0	Interrupt is disabled for FIFO full.

Bit 1 – TFHRFHIE Transmit/Receive FIFO Half Empty/Half Full Interrupt Enable bit

TXEN = 1 (FIFO configured as a transmit FIFO):
Transmit FIFO Half Empty Interrupt Enable.

Value	Description
1	Interrupt is enabled for FIFO half empty.
0	Interrupt is disabled for FIFO half empty.

TXEN = 0 (FIFO configured as a receive FIFO):
Receive FIFO Half Full Interrupt Enable.

Value	Description
1	Interrupt is enabled for FIFO half full.
0	Interrupt is disabled for FIFO half full.

Bit 0 – TFNRFNIE Transmit/Receive FIFO Not Full/Not Empty Interrupt Enable bit

TXEN = 1 (FIFO configured as a transmit FIFO):
Transmit FIFO Not Full Interrupt Enable.

Value	Description
1	Interrupt is enabled for FIFO not full.
0	Interrupt is disabled for FIFO not full.

TXEN = 0 (FIFO configured as a receive FIFO):
Receive FIFO Not Empty Interrupt Enable.

Value	Description
1	Interrupt is enabled for FIFO not empty.

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TFNRFNIE (continued)

Value	Description
0	Interrupt is disabled for FIFO not empty.

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11.2.46. CAN FIFO Control Register x High (x = 1 to 8)

Name: C1FIFOCONxH
Offset: 0x61E, 0x62A, 0x636, 0x642, 0x64E, 0x65A, 0x666, 0x672

Note:
1. These bits can only be modified in Configuration mode (OPMOD[2:0] = 100).

Bit	15	14	13	12	11	10	9	8
	PLSIZE[2:0]			FSIZE[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		TXAT[1:0]		TXPRI[4:0]				
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	1	0	0	0	0	0

Bits 15:13 – PLSIZE[2:0] Payload Size bits(1)

Value	Description
111	64 data bytes
110	48 data bytes
101	32 data bytes
100	24 data bytes
011	20 data bytes
010	16 data bytes
001	12 data bytes
000	8 data bytes

Bits 12:8 – FSIZE[4:0] FIFO Size bits(1)

Value	Description
11111	FIFO is 32 messages deep
. . .	
00010	FIFO is 3 messages deep
00001	FIFO is 2 messages deep
00000	FIFO is 1 message deep

Bits 6:5 – TXAT[1:0] Retransmission Attempts bits
This feature is enabled when RTXAT (C1CONH[0]) is set.

Value	Description
11	Unlimited number of retransmission attempts
10	Unlimited number of retransmission attempts
01	Three retransmission attempts
00	Disables retransmission attempts

Bits 4:0 – TXPRI[4:0] Message Transmit Priority bits

Value	Description
11111	Highest message priority
. . .	
00000	Lowest message priority

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11.2.47. CAN FIFO Status Register x (x = 1 to 8)

Name: C1FIFOSTAx
Offset: 0x620, 0x62C, 0x638, 0x644, 0x650, 0x65C, 0x668, 0x674

Notes:

1. The FIFOCI[4:0] bits provide a zero-indexed value to the message in the FIFO. If the FIFO is four messages deep (FSIZE[4:0] = 3), FIFOCIx will take on a value from 0 to 3, depending on the state of the FIFO.
2. These bits are updated when a message completes (or aborts) or when the FIFO is reset.
3. This bit is reset on any read of this register or when the TXQ is reset. The bits are cleared when TXREQ is set or by using an SPI write.

Legend: HS = Hardware Settable bit; C = Clearable bit

Bit	15	14	13	12	11	10	9	8
				FIFOCI[4:0]				
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXABT	TXLARB	TXERR	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
Access	R	R	R	HS/C	HS/C	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 12:8 – FIFOCI[4:0] FIFO Message Index bits(1)

TXEN = 1 (FIFO configured as a transmit buffer):
A read of this register will return an index to the message that the FIFO will next attempt to transmit.
TXEN = 0 (FIFO configured as a receive buffer):
A read of this register will return an index to the message that the FIFO will use to save the next message.

Bit 7 – TXABT Message Aborted Status bit(3)

Value	Description
1	Message was aborted.
0	Message completed successfully.

Bit 6 – TXLARB Message Lost Arbitration Status bit(2)

Value	Description
1	Message lost arbitration while being sent.
0	Message did not lose arbitration while being sent.

Bit 5 – TXERR Error Detected During Transmission bit(2)

Value	Description
1	A bus error occurred while the message was being sent.
0	A bus error did not occur while the message was being sent.

Bit 4 – TXATIF Transmit Attempts Exhausted Interrupt Pending bit

TXEN = 0 (FIFO configured as a receive buffer):
Unused, read as '0'.
TXEN = 1 (FIFO configured as a transmit buffer):

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Value	Description
1	Interrupt is pending.
0	Interrupt is not pending.

Bit 3 – RXOVIF Receive FIFO Overflow Interrupt Flag bit
TXEN = 1 (FIFO configured as a transmit buffer):
Unused, read as '0'.
TXEN = 0 (FIFO configured as a receive buffer):

Value	Description
1	Overflow event has occurred.
0	No overflow event has occurred.

Bit 2 – TFERFFIF Transmit/Receive FIFO Empty/Full Interrupt Flag bit
TXEN = 1 (FIFO configured as a transmit FIFO):
Transmit FIFO Empty Interrupt Flag.

Value	Description
1	FIFO is empty.
0	FIFO is not empty, at least one message is queued to be transmitted.

TXEN = 0 (FIFO configured as a receive FIFO):
Receive FIFO Full Interrupt Flag.

Value	Description
1	FIFO is full.
0	FIFO is not full.

Bit 1 – TFHRFHIF Transmit/Receive FIFO Half Empty/Half Full Interrupt Flag bit
TXEN = 1 (FIFO configured as a transmit FIFO):
Transmit FIFO Half Empty Interrupt Flag.

Value	Description
1	FIFO is ≤ half full.
0	FIFO is > half full.

TXEN = 0 (FIFO configured as a receive FIFO):
Receive FIFO Half Full Interrupt Flag.

Value	Description
1	FIFO is ≥ half full.
0	FIFO is < half full.

Bit 0 – TFNRFNIF Transmit/Receive FIFO Not Full/Not Empty Interrupt Flag bit
TXEN = 1 (FIFO configured as a transmit FIFO):
Transmit FIFO Not Full Interrupt Flag.

Value	Description
1	FIFO is not full.
0	FIFO is full.

TXEN = 0 (FIFO configured as a receive FIFO):
Receive FIFO Not Empty Interrupt Flag.

Value	Description
1	FIFO is not empty, has at least 1 message.
0	FIFO is empty.

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11.2.48. CAN FIFO User Address Register x Low (x = 1 to 8)

Name: C1FIFOUAxL(1)
Offset: 0x624, 0x630, 0x63C, 0x648, 0x654, 0x660, 0x66C, 0x678

Note:

1. This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
	FIFOUA[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	FIFOUA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 15:0 – FIFOUA[15:0] FIFO User Address bits

TXEN = 1 (FIFO configured as a transmit buffer):
A read of this register will return the address where the next message is to be written (FIFO head).
TXEN = 0 (FIFO configured as a receive buffer):
A read of this register will return the address where the next message is to be read (FIFO tail).

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11.2.49. CAN FIFO User Address Register x High (x = 1 to 8)

Name: C1FIFOUAxH(1)
Offset: 0x626, 0x632, 0x063E, 0x64A, 0x656, 0x662, 0x66E, 0x67A

Note:

1. This register is not ensured to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
	FIFOUA[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	FIFOUA[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 15:0 – FIFOUA[31:16] FIFO User Address bits

TXEN = 1 (FIFO configured as a transmit buffer):
A read of this register will return the address where the next message is to be written (FIFO head).
TXEN = 0 (FIFO configured as a receive buffer):
A read of this register will return the address where the next message is to be read (FIFO tail).

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11.2.50. CAN Filter Control Register x Low (x = 0 to 3)

Name: C1FLTCONxL
Offset: 0x67C, 0x680, 0x684, 0x688

Bit	15	14	13	12	11	10	9	8
	FLTENb			FbBP[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FLTENa			FaBP[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 15 – FLTENb Enable Filter b to Accept Messages bit

Value	Description
1	Filter is enabled.
0	Filter is disabled.

Bits 12:8 – FbBP[4:0] Pointer to Object When Filter b Hits bits

Value	Description
11111-11000	Reserved
00111	Message matching filter is stored in Object 7.
00110	Message matching filter is stored in Object 6.
. . .	
00010	Message matching filter is stored in Object 2.
00001	Message matching filter is stored in Object 1.
00000	Reserved; Object 0 is the TX Queue and can't receive messages.

Bit 7 – FLTENa Enable Filter a to Accept Messages bit

Value	Description
1	Filter is enabled.
0	Filter is disabled.

Bits 4:0 – FaBP[4:0] Pointer to Object When Filter a Hits bits

Value	Description
11111-11000	Reserved
00111	Message matching filter is stored in Object 7.
00110	Message matching filter is stored in Object 6.
. . .	
00010	Message matching filter is stored in Object 2.
00001	Message matching filter is stored in Object 1.
00000	Reserved; Object 0 is the TX Queue and can't receive messages.

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11.2.51. CAN Filter Control Register x High (x = 0 to 3)

Name: C1FLTCONxH
Offset: 0x67E, 0x682, 0x686, 0x68A

Bit	15	14	13	12	11	10	9	8
	FLTENd			FdBP[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FLTENc			FcBP[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 15 – FLTENd Enable Filter d to Accept Messages bit

Value	Description
1	Filter is enabled.
0	Filter is disabled.

Bits 12:8 – FdBP[4:0] Pointer to Object When Filter d Hits bits

Value	Description
11111-11000	Reserved
00111	Message matching filter is stored in Object 7.
00110	Message matching filter is stored in Object 6.
. . .	
00010	Message matching filter is stored in Object 2.
00001	Message matching filter is stored in Object 1.
00000	Reserved; Object 0 is the TX Queue and can't receive messages.

Bit 7 – FLTENc Enable Filter c to Accept Messages bit

Value	Description
1	Filter is enabled.
0	Filter is disabled.

Bits 4:0 – FcBP[4:0] Pointer to Object When Filter c Hits bits

Value	Description
11111-11000	Reserved
00111	Message matching filter is stored in Object 7.
00110	Message matching filter is stored in Object 6.
. . .	
00010	Message matching filter is stored in Object 2.
00001	Message matching filter is stored in Object 1.
00000	Reserved; Object 0 is the TX Queue and can't receive messages.

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11.2.52. CAN Filter Object Register x Low (x = 0 to 15)

Name: C1FLTOBJxL
Offset: 0x68C, 0x694, 0x69C, 0x6A4, 0x6AC, 0x6B4, 0x6BC, 0x6C4, 0x6CC, 0x6D4, 0x6DC, 0x6E4, 0x6EC, 0x6F4, 0x6FC, 0x704

Bit	15	14	13	12	11	10	9	8
	EID[4:0]					SID[10:8]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:11 – EID[4:0] Extended Identifier Filter bits
In DeviceNet™ mode, these are the filter bits for the first two data bytes.

Bits 10:0 – SID[10:0] Standard Identifier Filter bits

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11.2.53. CAN Filter Object Register x High (x = 0 to 15)

Name: C1FLTOBJxH
Offset: 0x68E, 0x696, 0x69E,0x6A6, 0x6AE, 0x6B6, 0x6BE, 0x6C6, 0x6CE, 0x6D6, 0x6DE, 0x6E6, 0x6EE,0x6F6, 0x6FE, 0x706

Bit	15	14	13	12	11	10	9	8
		EXIDE	SID11	EID[17:13]				
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	EID[12:5]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 14 – EXIDE Extended Identifier Enable bit
If MIDE = 1:

Value	Description
1	Matches only messages with Extended Identifier addresses.
0	Matches only messages with Standard Identifier addresses.

Bit 13 – SID11 Standard Identifier Filter bit

Bits 12:8 – EID[17:13] Extended Identifier Filter bits
In DeviceNet™ mode, these are the filter bits for the first two data bytes.

Bits 7:0 – EID[12:5] Extended Identifier Filter bits

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11.2.54. CAN Mask Register x Low (x = 0 to 15)

Name: C1MASKxL
Offset: 0x690, 0x698, 0x6A0, 0x6A8, 0x6B0, 0x6B8, 0x6C0, 0x6C8, 0x6D0, 0x6D8, 0x6E0, 0x6E8, 0x6F0, 0x6F8, 0x700, 0x708

Bit	15	14	13	12	11	10	9	8
	MEID[4:0]					MSID[10:8]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MSID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:11 – MEID[4:0] Extended Identifier Mask bits
In DeviceNet™ mode, these are the mask bits for the first two data bytes.

Bits 10:0 – MSID[10:0] Standard Identifier Mask bits

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11.2.55. CAN Mask Register x High (x = 0 to 15)

Name: C1MASKxH
Offset: 0x692, 0x69A, 0x6A2, 0x06AA, 0x06B2, 0x06BA, 0x06C2, 0x06CA, 0x06D2, 0x06DA, 0x06E2, 0x06EA, 0x06F2, 0x06FA, 0x0702, 0x70A

Bit	15	14	13	12	11	10	9	8
		MIDE	MSID11	MEID[17:13]				
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MEID[12:5]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 14 – MIDE Identifier Receive Mode bit

Value	Description
1	Matches only message types (standard or extended address) that correspond to the EXIDE bit in the filter.
0	Matches either standard or extended address message if filters match (i.e., if (Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID)).

Bit 13 – MSID11 Standard Identifier Mask bit

Bits 12:0 – MEID[17:5] Extended Identifier Mask bits
In DeviceNet™ mode, these are the mask bits for the first two data bytes.

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12. High-Speed PWM

The High-Speed PWM (HSPWM) module is a Pulse-Width Modulated (PWM) module to support both motor control and power supply applications. This flexible module provides features to support many types of Motor Control (MC) and Power Control (PC) applications, including:

- AC-to-DC Converters
- DC-to-DC Converters
- AC and DC Motors: BLDC, PMSM, ACIM, SRM, etc.
- Inverters
- Battery Chargers
- Digital Lighting
- Power Factor Correction (PFC)

Note: The Fine Edge Placement feature is not available in this family of devices.

12.1. Features

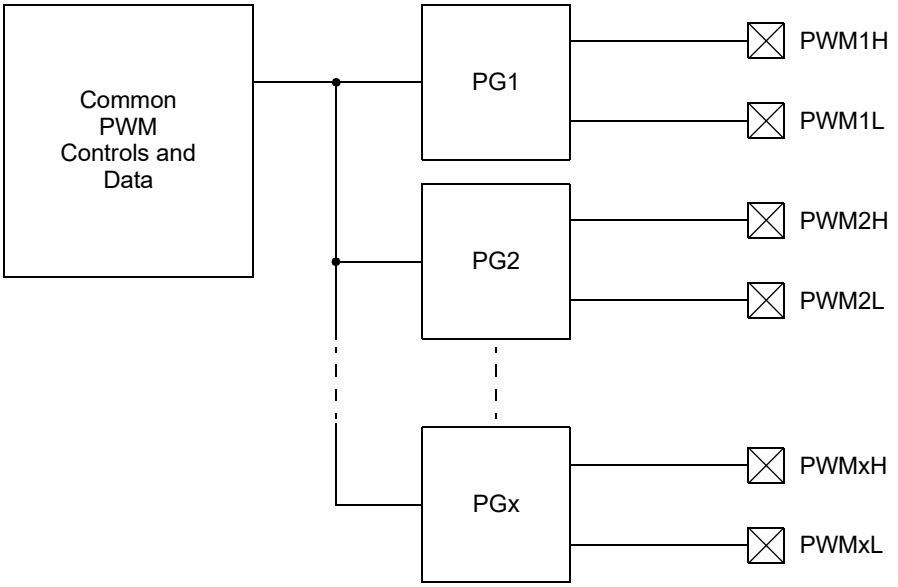
- Four Independent PWM Generators, each with Dual Outputs
- Operating Modes:
  - Independent Edge mode
  - Variable Phase PWM mode
  - Center-Aligned mode
  - Double Update Center-Aligned mode
  - Dual Edge Center-Aligned mode
  - Dual PWM mode
- Output Modes:
  - Complementary
  - Independent
  - Push-Pull
- Dead-Time Generator
- Leading-Edge Blanking (LEB)
- Output Override for Fault Handling
- Flexible Period/Duty Cycle Updating Options
- Programmable Control Inputs (PCI)
- Advanced Triggering Options
- Six Combinatorial Logic Outputs
- Six PWM Event Outputs

12.2. Architecture Overview

The PWM module consists of a common set of controls and features, and multiple instantiations of PWM Generators (PGs). Each PWM Generator can be independently configured, or multiple PWM Generators can be used to achieve complex multiphase systems. PWM Generators can also be used to implement sophisticated triggering, protection and logic functions. A high-level block diagram is shown in Figure 12-1.

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Figure 12-1. PWM High-Level Block Diagram



12.3. Lock and Write Restrictions

The LOCK bit (PCLKCON[8]) may be set in software to block writes to certain registers. For more information, refer to **"HRPWM with Fine Edge Placement"** (www.microchip.com/DS70005320) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The following lock/unlock sequence is required to set or clear the LOCK bit.

1. Write 0x55 to NVMKEY.
2. Write 0xAA to NVMKEY.
3. Clear (or set) the LOCK bit (PCLKCON[8]) as a single operation.

In general, modifications to configuration controls should not be done while the module is running, as indicated by the ON bit (PGxCONL[15]) being set.

12.4. PWM4H/L Output on Peripheral Pin Select

All devices support the capability to output PWM4H and PWM4L signals via Peripheral Pin Select (PPS) on to any "RPn" pin. This feature is intended for lower pin count devices that do not have PWM4H/L on dedicated pins.

Configuration bit, DUPWM (FDEVOPT[12]), provides the option to disable the fixed pin PWM4L/H functions when using the PPS. Clearing the DUPPWM bit will disable PWM4 function and allow the pin to be used for another purpose. Leaving the DUPPWM set (default) will output PWM4 on both fixed pin and PPS outputs. The output port enable bits, PENH and PENL (PGxIOCONH[3:2]), control output function for both dedicated and PPS pins outputs.

If PWM4H/L PPS output functions are used on devices that also have fixed PWM4H/L pins, the output signal will be present on both dedicated and "RPn" pins. The Output Port Enable bits, PENH and PENL (PGxIOCONH[3:2]), control both dedicated and PPS pins together; it is not possible to disable the dedicated pins and use only PPS.

Given the natural priority of the "RPn" functions above that of the PWM, it is possible to use the PPS output functions on the dedicated PWM4H/L pins, while the PWM4 signals are routed to other pins via PPS. Any of the peripheral outputs listed in Mapping Limitations, with the exception of 'Default Port', can be used. Input functions, including the ports and peripherals listed in Virtual Connections, cannot be used through the "RPn" function on dedicated PWM4H/L pins when PWM4 is active.

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12.5. PWM Control/Status Registers

There are two categories of Special Function Registers (SFRs) used to control the operation of the PWM module:

- Common, shared by all PWM Generators
- PWM Generator-specific

An ‘x’ in the register name denotes an instance of a PWM Generator.

A ‘y’ in the register name denotes an instance of the common function.

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12.6. Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0300	PCLKCON	15:8								LOCK
		7:0			DIVSEL[1:0]				MCLKSEL[1:0]	
0x0302	FSCL	15:8	FSCL[15:8]							
		7:0	FSCL[7:0]							
0x0304	FSMINPER	15:8	FSMINPER[15:8]							
		7:0	FSMINPER[7:0]							
0x0306	MPHASE	15:8	MPHASE[15:8]							
		7:0	MPHASE[7:0]							
0x0308	MDC	15:8	MDC[15:8]							
		7:0	MDC[7:0]							
0x030A	MPER	15:8	MPER[15:8]							
		7:0	MPER[7:0]							
0x030C	LFSR	15:8		LFSR[14:8]						
		7:0	LFSR[7:0]							
0x030E	CMBTRIGL	15:8								
		7:0					CTA4EN	CTA3EN	CTA2EN	CTA1EN
0x0310	CMBTRIGH	15:8								
		7:0					CTB4EN	CTB3EN	CTB2EN	CTB1EN
0x0312	LOGCONA	15:8	PWMS1A[3:0]				PWMS2A[3:0]			
		7:0	S1APOL	S2APOL	PWMLFA[1:0]			PWMLFAD[2:0]		
0x0314	LOGCONB	15:8	PWMS1B[3:0]				PWMS2B[3:0]			
		7:0	S1BPOL	S2BPOL	PWMLFB[1:0]			PWMLFBD[2:0]		
0x0316	LOGCONC	15:8	PWMS1C[3:0]				PWMS2C[3:0]			
		7:0	S1CPOL	S2CPOL	PWMLFC[1:0]			PWMLFCD[2:0]		
0x0318	LOGCOND	15:8	PWMS1D[3:0]				PWMS2D[3:0]			
		7:0	S1DPOL	S2DPOL	PWMLFD[1:0]			PWMLFDD[2:0]		
0x031A	LOGCONE	15:8	PWMS1E[3:0]				PWMS2E[3:0]			
		7:0	S1EPOL	S2EPOL	PWMLFE[1:0]			PWMLFED[2:0]		
0x031C	LOGCONF	15:8	PWMS1F[3:0]				PWMS2F[3:0]			
		7:0	S1FPOL	S2FPOL	PWMLFF[1:0]			PWMLFFD[2:0]		
0x031E	PWMEVTA	15:8	EVTAOEN	EVTAPOL	EVTASTRD	EVTASYNC				
		7:0	EVTASEL[3:0]					EVTAPGS[2:0]		
0x0320	PWMEVTB	15:8	EVTBOEN	EVTBPOL	EVTBSTRD	EVTBSYNC				
		7:0	EVTBSEL[3:0]					EVTBPGS[2:0]		
0x0322	PWMEVTC	15:8	EVTCOEN	EVTCPOL	EVTCSTRD	EVTCSYNC				
		7:0	EVTCSEL[3:0]					EVTCPGS[2:0]		
0x0324	PWMEVTD	15:8	EVTDOEN	EVTDPOL	EVTDSTRD	EVTDSYNC				
		7:0	EVTDSEL[3:0]					EVTDPGS[2:0]		
0x0326	PWMEVTE	15:8	EVTEOEN	EVTEPOL	EVTESTRD	EVTESYNC				
		7:0	EVTESEL[3:0]					EVTEPGS[2:0]		
0x0328	PWMEVTF	15:8	EVTFOEN	EVTFPOL	EVTFSTRD	EVTFSYNC				
		7:0	EVTFSEL[3:0]					EVTFPGS[2:0]		
0x032A	PG1CONL	15:8	ON	FRZ				TRGCNT[2:0]		
		7:0				CLKSEL[1:0]		MODSEL[2:0]		
0x032C	PG1CONH	15:8	MDCSEL	MPERSEL	MPHSEL		MSTEN	UPMOD[2:0]		
		7:0	Reserved	TRGMOD			SOCS[3:0]			
0x032E	PG1STAT	15:8	SEVT	FLTEVT	CLEVT	FFEVT	SACT	FLTACT	CLACT	FFACT
		7:0	TRSET	TRCLR	CAP	UPDATE	UPDREQ	STEER	CAHALF	TRIG
0x0330	PG1IOCONL	15:8	CLMOD	SWAP	OVRENH	OVRENL	OVRDAT[1:0]		OSYNC[1:0]	
		7:0	FLTDAT[1:0]		CLDAT[1:0]		FFDAT[1:0]		DBDAT[1:0]	
0x0332	PG1IOCONH	15:8		CAPSRC[2:0]						DTCMPSEL
		7:0			PMOD[1:0]		PENH	PENL	POLH	POLL
0x0334	PG1EVTL	15:8	ADTR1PS[4:0]					ADTR1EN3	ADTR1EN2	ADTR1EN1
		7:0				UPDTRG[1:0]		PGTRGSEL[2:0]		
0x0336	PG1EVTH	15:8	FLTIEN	CLIEN	FFIEN	SIEN			IEVTSEL[1:0]	
		7:0	ADTR2EN3	ADTR2EN2	ADTR2EN1	ADTR1OFS[4:0]				
0x0338	PG1FPCIL	15:8	TSYNCDIS	TERM[2:0]			AQPS	AQSS[2:0]		
		7:0	SWTERM	PSYNC	PPS	PSS[4:0]				

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Control Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x033A	PG1FPCIH	15:8	BPEN		BPSEL[2:0]				ACP[2:0]	
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS		TQSS[2:0]	
0x033C	PG1CLPCIL	15:8	TSYNCDIS		TERM[2:0]		AQPS		AQSS[2:0]	
		7:0	SWTERM	PSYNC	PPS			PSS[4:0]		
0x033E	PG1CLPCIH	15:8	BPEN		BPSEL[2:0]				ACP[2:0]	
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS		TQSS[2:0]	
0x0340	PG1FFPCIL	15:8	TSYNCDIS		TERM[2:0]		AQPS		AQSS[2:0]	
		7:0	SWTERM	PSYNC	PPS			PSS[4:0]		
0x0342	PG1FFPCIH	15:8	BPEN		BPSEL[2:0]				ACP[2:0]	
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS		TQSS[2:0]	
0x0344	PG1SPCIL	15:8	TSYNCDIS		TERM[2:0]		AQPS		AQSS[2:0]	
		7:0	SWTERM	PSYNC	PPS			PSS[4:0]		
0x0346	PG1SPCIH	15:8	BPEN		BPSEL[2:0]				ACP[2:0]	
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS		TQSS[2:0]	
0x0348	PG1LEBL	15:8	LEB[12:5]							
		7:0	LEB[4:0]							
0x034A	PG1LEBH	15:8						PWMPCI[2:0]		
		7:0					PHR	PHF	PLR	PLF
0x034C	PG1PHASE	15:8	PG1PHASE[15:8]							
		7:0	PG1PHASE[7:0]							
0x034E	PG1DC	15:8	PG1DC[15:8]							
		7:0	PG1DC[7:0]							
0x0350	PG1DCA	15:8								
		7:0	PG1DCA[7:0]							
0x0352	PG1PER	15:8	PG1PER[15:8]							
		7:0	PG1PER[7:0]							
0x0354	PG1TRIGA	15:8	PG1TRIGA[15:8]							
		7:0	PG1TRIGA[7:0]							
0x0356	PG1TRIGB	15:8	PG1TRIGB[15:8]							
		7:0	PG1TRIGB[7:0]							
0x0358	PG1TRIGC	15:8	PG1TRIGC[15:8]							
		7:0	PG1TRIGC[7:0]							
0x035A	PG1DTL	15:8						DTL[10:8]		
		7:0	DTL[7:0]							
0x035C	PG1DTH	15:8						DTH[10:8]		
		7:0	DTH[7:0]							
0x035E	PG1CAP	15:8	PG1CAP[15:8]							
		7:0	PG1CAP[7:0]							
0x0360	PG2CONL	15:8	ON	FRZ				TRGCNT[2:0]		
		7:0				CLKSEL[1:0]		MODSEL[2:0]		
0x0362	PG2CONH	15:8	MDCSEL	MPERSEL	MPHSEL		MSTEN	UPMOD[2:0]		
		7:0	Reserved	TRGMOD			SOCS[3:0]			
0x0364	PG2STAT	15:8	SEVT	FLTEVT	CLEVT	FFEVT	SACT	FLTACT	CLACT	FFACT
		7:0	TRSET	TRCLR	CAP	UPDATE	UPDREQ	STEER	CAHALF	TRIG
0x0366	PG2IOCONL	15:8	CLMOD	SWAP	OVRENH	OVRENL	OVRDAT[1:0]		OSYNC[1:0]	
		7:0	FLTDAT[1:0]		CLDAT[1:0]		FFDAT[1:0]		DBDAT[1:0]	
0x0368	PG2IOCONH	15:8		CAPSRC[2:0]						DTCMPSEL
		7:0			PMOD[1:0]		PENH	PENL	POLH	POLL
0x036A	PG2EVTL	15:8	ADTR1PS[4:0]					ADTR1EN3	ADTR1EN2	ADTR1EN1
		7:0				UPDTRG[1:0]		PGTRGSEL[2:0]		
0x036C	PG2EVTH	15:8	FLTIEN	CLIEN	FFIEN	SIEN			IEVTSEL[1:0]	
		7:0	ADTR2EN3	ADTR2EN2	ADTR2EN1	ADTR1OFS[4:0]				
0x036E	PG2FPCIL	15:8	TSYNCDIS		TERM[2:0]		AQPS		AQSS[2:0]	
		7:0	SWTERM	PSYNC	PPS			PSS[4:0]		
0x0370	PG2FPCIH	15:8	BPEN		BPSEL[2:0]				ACP[2:0]	
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS		TQSS[2:0]	
0x0372	PG2CLPCIL	15:8	TSYNCDIS		TERM[2:0]		AQPS		AQSS[2:0]	
		7:0	SWTERM	PSYNC	PPS			PSS[4:0]		
0x0374	PG2CLPCIH	15:8	BPEN		BPSEL[2:0]				ACP[2:0]	
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS		TQSS[2:0]	

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Control Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0376	PG2FFPCIL	15:8	TSYNCDIS		TERM[2:0]		AQPS		AQSS[2:0]	
		7:0	SWTERM	PSYNC	PPS			PSS[4:0]		
0x0378	PG2FFPCIH	15:8	BPEN		BPSEL[2:0]				ACP[2:0]	
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS		TQSS[2:0]	
0x037A	PG2SPCIL	15:8	TSYNCDIS		TERM[2:0]		AQPS		AQSS[2:0]	
		7:0	SWTERM	PSYNC	PPS			PSS[4:0]		
0x037C	PG2SPCIH	15:8	BPEN		BPSEL[2:0]				ACP[2:0]	
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS		TQSS[2:0]	
0x037E	PG2LEBL	15:8	LEB[12:5]							
		7:0	LEB[4:0]							
0x0380	PG2LEBH	15:8						PWMPCI[2:0]		
		7:0					PHR	PHF	PLR	PLF
0x0382	PG2PHASE	15:8	PG2PHASE[15:8]							
		7:0	PG2PHASE[7:0]							
0x0384	PG2DC	15:8	PG2DC[15:8]							
		7:0	PG2DC[7:0]							
0x0386	PG2DCA	15:8								
		7:0	PG2DCA[7:0]							
0x0388	PG2PER	15:8	PG2PER[15:8]							
		7:0	PG2PER[7:0]							
0x038A	PG2TRIGA	15:8	PG2TRIGA[15:8]							
		7:0	PG2TRIGA[7:0]							
0x038C	PG2TRIGB	15:8	PG2TRIGB[15:8]							
		7:0	PG2TRIGB[7:0]							
0x038E	PG2TRIGC	15:8	PG2TRIGC[15:8]							
		7:0	PG2TRIGC[7:0]							
0x0390	PG2DTL	15:8						DTL[10:8]		
		7:0	DTL[7:0]							
0x0392	PG2DTH	15:8						DTH[10:8]		
		7:0	DTH[7:0]							
0x0394	PG2CAP	15:8	PG2CAP[15:8]							
		7:0	PG2CAP[7:0]							
0x0396	PG3CONL	15:8	ON	FRZ				TRGCNT[2:0]		
		7:0				CLKSEL[1:0]		MODSEL[2:0]		
0x0398	PG3CONH	15:8	MDCSEL	MPERSEL	MPHSEL		MSTEN	UPMOD[2:0]		
		7:0	Reserved	TRGMOD			SOCS[3:0]			
0x039A	PG3STAT	15:8	SEVT	FLTEVT	CLEVT	FFEVT	SACT	FLTACT	CLACT	FFACT
		7:0	TRSET	TRCLR	CAP	UPDATE	UPDREQ	STEER	CAHALF	TRIG
0x039C	PG3IOCONL	15:8	CLMOD	SWAP	OVRENH	OVRENL	OVRDAT[1:0]		OSYNC[1:0]	
		7:0	FLTDAT[1:0]		CLDAT[1:0]		FFDAT[1:0]		DBDAT[1:0]	
0x039E	PG3IOCONH	15:8		CAPSRC[2:0]						DTCMPSEL
		7:0			PMOD[1:0]		PENH	PENL	POLH	POLL
0x03A0	PG3EVTL	15:8	ADTR1PS[4:0]					ADTR1EN3	ADTR1EN2	ADTR1EN1
		7:0				UPDTRG[1:0]		PGTRGSEL[2:0]		
0x03A2	PG3EVTH	15:8	FLTIEN	CLIEN	FFIEN	SIEN			IEVTSEL[1:0]	
		7:0	ADTR2EN3	ADTR2EN2	ADTR2EN1		ADTR1OFS[4:0]			
0x03A4	PG3FPCIL	15:8	TSYNCDIS		TERM[2:0]		AQPS		AQSS[2:0]	
		7:0	SWTERM	PSYNC	PPS			PSS[4:0]		
0x03A6	PG3FPCIH	15:8	BPEN		BPSEL[2:0]				ACP[2:0]	
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS		TQSS[2:0]	
0x03A8	PG3CLPCIL	15:8	TSYNCDIS		TERM[2:0]		AQPS		AQSS[2:0]	
		7:0	SWTERM	PSYNC	PPS			PSS[4:0]		
0x03AA	PG3CLPCIH	15:8	BPEN		BPSEL[2:0]				ACP[2:0]	
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS		TQSS[2:0]	
0x03AC	PG3FFPCIL	15:8	TSYNCDIS		TERM[2:0]		AQPS		AQSS[2:0]	
		7:0	SWTERM	PSYNC	PPS			PSS[4:0]		
0x03AE	PG3FFPCIH	15:8	BPEN		BPSEL[2:0]				ACP[2:0]	
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS		TQSS[2:0]	
0x03B0	PG3SPCIL	15:8	TSYNCDIS		TERM[2:0]		AQPS		AQSS[2:0]	
		7:0	SWTERM	PSYNC	PPS			PSS[4:0]		

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Control Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x03B2	PG3SPCIH	15:8	BPEN	BPSEL[2:0]				ACP[2:0]		
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS	TQSS[2:0]		
0x03B4	PG3LEBL	15:8	LEB[12:5]							
		7:0	LEB[4:0]							
0x03B6	PG3LEBH	15:8						PWMPCI[2:0]		
		7:0					PHR	PHF	PLR	PLF
0x03B8	PG3PHASE	15:8	PG3PHASE[15:8]							
		7:0	PG3PHASE[7:0]							
0x03BA	PG3DC	15:8	PG3DC[15:8]							
		7:0	PG3DC[7:0]							
0x03BC	PG3DCA	15:8								
		7:0	PG3DCA[7:0]							
0x03BE	PG3PER	15:8	PG3PER[15:8]							
		7:0	PG3PER[7:0]							
0x03C0	PG3TRIGA	15:8	PG3TRIGA[15:8]							
		7:0	PG3TRIGA[7:0]							
0x03C2	PG3TRIGB	15:8	PG3TRIGB[15:8]							
		7:0	PG3TRIGB[7:0]							
0x03C4	PG3TRIGC	15:8	PG3TRIGC[15:8]							
		7:0	PG3TRIGC[7:0]							
0x03C6	PG3DTL	15:8						DTL[10:8]		
		7:0	DTL[7:0]							
0x03C8	PG3DTH	15:8						DTH[10:8]		
		7:0	DTH[7:0]							
0x03CA	PG3CAP	15:8	PG3CAP[15:8]							
		7:0	PG3CAP[7:0]							
0x03CC	PG4CONL	15:8	ON	FRZ				TRGCNT[2:0]		
		7:0				CLKSEL[1:0]		MODSEL[2:0]		
0x03CE	PG4CONH	15:8	MDCSEL	MPERSEL	MPHSEL		MSTEN	UPMOD[2:0]		
		7:0	Reserved	TRGMOD			SOCS[3:0]			
0x03D0	PG4STAT	15:8	SEVT	FLTEVT	CLEVT	FFEVT	SACT	FLTACT	CLACT	FFACT
		7:0	TRSET	TRCLR	CAP	UPDATE	UPDREQ	STEER	CAHALF	TRIG
0x03D2	PG4IOCONL	15:8	CLMOD	SWAP	OVRENH	OVRENL	OVRDAT[1:0]		OSYNC[1:0]	
		7:0	FLTDAT[1:0]		CLDAT[1:0]		FFDAT[1:0]		DBDAT[1:0]	
0x03D4	PG4IOCONH	15:8		CAPSRC[2:0]						DTCMPSEL
		7:0			PMOD[1:0]		PENH	PENL	POLH	POLL
0x03D6	PG4EVTL	15:8	ADTR1PS[4:0]					ADTR1EN3	ADTR1EN2	ADTR1EN1
		7:0				UPDTRG[1:0]		PGTRGSEL[2:0]		
0x03D8	PG4EVTH	15:8	FLTIEN	CLIEN	FFIEN	SIEN			IEVTSEL[1:0]	
		7:0	ADTR2EN3	ADTR2EN2	ADTR2EN1	ADTR1OFS[4:0]				
0x03DA	PG4FPCIL	15:8	TSYNCDIS	TERM[2:0]			AQPS	AQSS[2:0]		
		7:0	SWTERM	PSYNC	PPS	PSS[4:0]				
0x03DC	PG4FPCIH	15:8	BPEN	BPSEL[2:0]				ACP[2:0]		
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS	TQSS[2:0]		
0x03DE	PG4CLPCIL	15:8	TSYNCDIS	TERM[2:0]			AQPS	AQSS[2:0]		
		7:0	SWTERM	PSYNC	PPS	PSS[4:0]				
0x03E0	PG4CLPCIH	15:8	BPEN	BPSEL[2:0]				ACP[2:0]		
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS	TQSS[2:0]		
0x03E2	PG4FFPCIL	15:8	TSYNCDIS	TERM[2:0]			AQPS	AQSS[2:0]		
		7:0	SWTERM	PSYNC	PPS	PSS[4:0]				
0x03E4	PG4FFPCIH	15:8	BPEN	BPSEL[2:0]				ACP[2:0]		
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS	TQSS[2:0]		
0x03E6	PG4SPCIL	15:8	TSYNCDIS	TERM[2:0]			AQPS	AQSS[2:0]		
		7:0	SWTERM	PSYNC	PPS	PSS[4:0]				
0x03E8	PG4SPCIH	15:8	BPEN	BPSEL[2:0]				ACP[2:0]		
		7:0	SWPCI	SWPCIM[1:0]		LATMOD	TQPS	TQSS[2:0]		
0x03EA	PG4LEBL	15:8	LEB[12:5]							
		7:0	LEB[4:0]							
0x03EC	PG4LEBH	15:8						PWMPCI[2:0]		
		7:0					PHR	PHF	PLR	PLF

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Control Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x03EE	PG4PHASE	15:8	PG4PHASE[15:8]							
		7:0	PG4PHASE[7:0]							
0x03F0	PG4DC	15:8	PG4DC[15:8]							
		7:0	PG4DC[7:0]							
0x03F2	PG4DCA	15:8								
		7:0	PG4DCA[7:0]							
0x03F4	PG4PER	15:8	PG4PER[15:8]							
		7:0	PG4PER[7:0]							
0x03F6	PG4TRIGA	15:8	PG4TRIGA[15:8]							
		7:0	PG4TRIGA[7:0]							
0x03F8	PG4TRIGB	15:8	PG4TRIGB[15:8]							
		7:0	PG4TRIGB[7:0]							
0x03FA	PG4TRIGC	15:8	PG4TRIGC[15:8]							
		7:0	PG4TRIGC[7:0]							
0x03FC	PG4DTL	15:8						DTL[10:8]		
		7:0	DTL[7:0]							
0x03FE	PG4DTH	15:8						DTH[10:8]		
		7:0	DTH[7:0]							
0x0400	PG4CAP	15:8	PG4CAP[15:8]							
		7:0	PG4CAP[7:0]							

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12.6.1. PWM Clock Control Register

Name: PCLKCON
Offset: 0x300

Notes:
1. A device-specific unlock sequence must be performed before this bit can be cleared.
2. Changing the MCLKSEL[1:0] bits while ON (PGxCONL[15]) = 1 is not recommended.

Bit	15	14	13	12	11	10	9	8
								LOCK
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
			DIVSEL[1:0]				MCLKSEL[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit 8 – LOCK Lock bit(1)

Value	Description
1	Write-protected registers and bits are locked.
0	Write-protected registers and bits are unlocked.

Bits 5:4 – DIVSEL[1:0] PWM Clock Divider Selection bits

Value	Description
11	Divide ratio is 1:16
10	Divide ratio is 1:8
01	Divide ratio is 1:4
00	Divide ratio is 1:2

Bits 1:0 – MCLKSEL[1:0] PWM Master Clock Selection bits(2)

Value	Description
11	$F_{VCO}/3$
10	F_{PLLO}
01	$F_{VCO}/2$
00	F_{OSC}

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12.6.2. Frequency Scale Register

Name: FSCL
Offset: 0x302

Bit	15	14	13	12	11	10	9	8
	FSCL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FSCL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – FSCL[15:0] Frequency Scale Register bits
The value in this register is added to the frequency scaling accumulator at each pwm_master_clk. When the accumulated value exceeds the value of FSMINPER, a clock pulse is produced.

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12.6.3. Frequency Scaling Minimum Period Register

Name: FSMINPER
Offset: 0x304

Bit	15	14	13	12	11	10	9	8
	FSMINPER[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FSMINPER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – FSMINPER[15:0] Frequency Scaling Minimum Period Register bits
This register holds the minimum clock period (maximum clock frequency) that can be produced by the frequency scaling circuit.

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12.6.4. Master Phase Register

Name: MPHASE
Offset: 0x306

Bit	15	14	13	12	11	10	9	8
	MPHASE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MPHASE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – MPHASE[15:0] Master Phase Register bits

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12.6.5. Master Duty Cycle Register

Name: MDC
Offset: 0x308

Bit	15	14	13	12	11	10	9	8
	MDC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MDC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – MDC[15:0] Master Duty Cycle Register bits

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12.6.6. Master Period Register

Name: MPER
Offset: 0x30A

Note:

1. Period values less than '0x0010' should not be selected.

Bit	15	14	13	12	11	10	9	8
	MPER[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MPER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – MPER[15:0] Master Period Register bits(1)

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12.6.7. Linear Feedback Shift Register

Name: LFSR
Offset: 0x30C

Bit	15	14	13	12	11	10	9	8
		LFSR[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LFSR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 14:0 – LFSR[14:0] Linear Feedback Shift Register bits
A read of this register will provide a 15-bit pseudorandom value.

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12.6.8. Combinatorial Trigger Register Low

Name: CMBTRIGL
Offset: 0x30E

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					CTA4EN	CTA3EN	CTA2EN	CTA1EN
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – CTA4EN Enable Trigger Output from PWM Generator #4 as Source for Combinatorial Trigger A bit

Value	Description
1	Enables specified trigger signal to be OR'd into the Combinatorial Trigger A signal.
0	Disabled

Bit 2 – CTA3EN Enable Trigger Output from PWM Generator #3 as Source for Combinatorial Trigger A bit

Value	Description
1	Enables specified trigger signal to be OR'd into the Combinatorial Trigger A signal.
0	Disabled

Bit 1 – CTA2EN Enable Trigger Output from PWM Generator #2 as Source for Combinatorial Trigger A bit

Value	Description
1	Enables specified trigger signal to be OR'd into the Combinatorial Trigger A signal.
0	Disabled

Bit 0 – CTA1EN Enable Trigger Output from PWM Generator #1 as Source for Combinatorial Trigger A bit

Value	Description
1	Enables specified trigger signal to be OR'd into the Combinatorial Trigger A signal.
0	Disabled

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12.6.9. Combinatorial Trigger Register High

Name: CMBTRIGH
Offset: 0x310

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					CTB4EN	CTB3EN	CTB2EN	CTB1EN
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – CTB4EN Enable Trigger Output from PWM Generator #4 as Source for Combinatorial Trigger B bit

Value	Description
1	Enables specified trigger signal to be OR'd into the Combinatorial Trigger B signal.
0	Disabled

Bit 2 – CTB3EN Enable Trigger Output from PWM Generator #3 as Source for Combinatorial Trigger B bit

Value	Description
1	Enables specified trigger signal to be OR'd into the Combinatorial Trigger B signal.
0	Disabled

Bit 1 – CTB2EN Enable Trigger Output from PWM Generator #2 as Source for Combinatorial Trigger B bit

Value	Description
1	Enables specified trigger signal to be OR'd into the Combinatorial Trigger B signal.
0	Disabled

Bit 0 – CTB1EN Enable Trigger Output from PWM Generator #1 as Source for Combinatorial Trigger B bit

Value	Description
1	Enables specified trigger signal to be OR'd into the Combinatorial Trigger B signal.
0	Disabled

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12.6.10. Combinatorial PWM Logic Control Register y

Name: LOGCONy
Offset: 0x312, 0x314, 0x316, 0x318, 0x31A, 0x31C

Note:
1. Logic function input will be connected to '0' if the PWM channel is not present.

Bit	15	14	13	12	11	10	9	8
	PWMS1y[3:0]				PWMS2y[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	S1yPOL	S2yPOL	PWMLFy[1:0]			PWMLFyD[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bits 15:12 – PWMS1y[3:0] Combinatorial PWM Logic Source #1 Selection bits(1)

Value	Description
1111-1000	Reserved
0111	PWM4L
0110	PWM4H
0101	PWM3L
0100	PWM3H
0011	PWM2L
0010	PWM2H
0001	PWM1L
0000	PWM1H

Bits 11:8 – PWMS2y[3:0] Combinatorial PWM Logic Source #2 Selection bits(1)

Value	Description
1111-1000	Reserved
0111	PWM4L
0110	PWM4H
0101	PWM3L
0100	PWM3H
0011	PWM2L
0010	PWM2H
0001	PWM1L
0000	PWM1H

Bit 7 – S1yPOL Combinatorial PWM Logic Source #1 Polarity bit

Value	Description
1	Input is inverted.
0	Input is positive logic.

Bit 6 – S2yPOL Combinatorial PWM Logic Source #2 Polarity bit

Value	Description
1	Input is inverted.
0	Input is positive logic.

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Bits 5:4 – PWMLFy[1:0] Combinatorial PWM Logic Function Selection bits

Value	Description
11	Reserved
10	PWMS1 ^ PWMS2 (XOR)
01	PWMS1 & PWMS2 (AND)
00	PWMS1 | PWMS2 (OR)

Bits 2:0 – PWMLFyD[2:0] Combinatorial PWM Logic Destination Selection bits

Value	Description
111–100	Reserved
011	Logic function is assigned to the PWM4H or PWM4L pin.
010	Logic function is assigned to the PWM3H or PWM3L pin.
001	Logic function is assigned to the PWM2H or PWM2L pin.
000	No assignment, combinatorial PWM logic function is disabled.

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12.6.11. PWM Event Output Control Register y

Name: PWMEVTy
Offset: 0x31E, 0x320, 0x322, 0x324, 0x326, 0x328

Notes:

1. The event signal is stretched using the peripheral clock because different PGs may be operating from different clock sources. The leading edge of the event pulse is produced in the clock domain of the PWM Generator. The trailing edge of the stretched event pulse is produced in the peripheral clock domain.
2. No event will be produced if the selected PWM Generator is not present.
3. This is the PWM Generator output signal prior to Output mode logic and any output override logic.
4. This signal should be the PGx_clk domain signal prior to any synchronization into the system clock domain.

Bit	15	14	13	12	11	10	9	8
	EVTyOEN	EVTyPOL	EVTySTRD	EVTySYNC				
Access	R/W	R/W	R/W	R/W				
Reset	0	0	0	0				

Bit	7	6	5	4	3	2	1	0
	EVTySEL[3:0]					EVTyPGS[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit 15 – EVTyOEN PWM Event Output Enable bit

Value	Description
1	Event output signal is output on the PWMEVTy pin.
0	Event output signal is internal only.

Bit 14 – EVTyPOL PWM Event Output Polarity bit

Value	Description
1	Event output signal is active-low.
0	Event output signal is active-high.

Bit 13 – EVTySTRD PWM Event Output Stretch Disable bit

Value	Description
1	Event output signal pulse width is not stretched.
0	Event output signal is stretched to eight PWM clock cycles minimum(1).

Bit 12 – EVTySYNC PWM Event Output Sync bit
Event output signal pulse will be two system clocks when this bit is set and EVTySTRD = 1.

Value	Description
1	Event output signal is synchronized to the system clock.
0	Event output is not synchronized to the system clock.

Bits 7:4 – EVTySEL[3:0] PWM Event Selection bits

Value	Description
1111-1010	Reserved

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Value	Description
1001	ADC Trigger 2 signal
1000	ADC Trigger 1 signal
0111	STEER signal (available in Push-Pull Output modes only)(4).
0110	CAHALF signal (available in Center-Aligned modes only)(4).
0101	PCI Fault active output signal
0100	PCI current-limit active output signal
0011	PCI feed-forward active output signal
0010	PCI Sync active output signal
0001	PWM Generator output signal(3)
0000	Source is selected by the PGTRGSEL[2:0] bits

Bits 2:0 – EVTyPGS[2:0] PWM Event Source Selection bits(2)

Value	Description
111-100	Reserved
011	PWM Generator 4
010	PWM Generator 3
001	PWM Generator 2
000	PWM Generator 1

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12.6.12. PWM Generator x Control Register Low

Name: PGxCONL
Offset: 0x32A, 0x360, 0x396, 0x3CC

Note:

1. The PWM Generator time base operates from the frequency scaling circuit clock, effectively scaling the duty cycle and period of the PWM Generator output.

Bit	15	14	13	12	11	10	9	8
	ON	FRZ				TRGCNT[2:0]		
Access	R/W	R/W				R/W	R/W	R/W
Reset	0	0				0	0	0

Bit	7	6	5	4	3	2	1	0
				CLKSEL[1:0]		MODSEL[2:0]		
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 15 – ON Enable bit

Value	Description
1	PWM Generator is enabled.
0	PWM Generator is not enabled.

Bit 14 – FRZ PGx Freeze bit

Value	Description
1	PGx stops operation in Debug mode.
0	PGx continues operation in Debug mode.

Bits 10:8 – TRGCNT[2:0] Trigger Count Select bits

Value	Description
111	PWM Generator produces eight PWM cycles after being triggered.
110	PWM Generator produces seven PWM cycles after being triggered.
101	PWM Generator produces six PWM cycles after being triggered.
100	PWM Generator produces five PWM cycles after being triggered.
011	PWM Generator produces four PWM cycles after being triggered.
010	PWM Generator produces three PWM cycles after being triggered.
001	PWM Generator produces two PWM cycles after being triggered.
000	PWM Generator produces one PWM cycle after being triggered.

Bits 4:3 – CLKSEL[1:0] Clock Selection bits

Value	Description
11	PWM Generator uses the Master clock scaled by frequency scaling circuit(1).
10	PWM Generator uses the Master clock divided by clock divider circuit(1).
01	PWM Generator uses the Master clock selected by the MCLKSEL[1:0] (PCLKCON[1:0]) control bits.
00	No clock selected, PWM Generator is in the lowest power state (default).

Bits 2:0 – MODSEL[2:0] Mode Selection bits

Value	Description
111	Dual Edge Center-Aligned PWM mode (interrupt/register update twice per cycle)
110	Dual Edge Center-Aligned PWM mode (interrupt/register update once per cycle)

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Value	Description
101	Double-Update Center-Aligned PWM mode
100	Center-Aligned PWM mode
011	Reserved
010	Independent Edge PWM mode, dual output
001	Variable Phase PWM mode
000	Independent Edge PWM mode

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12.6.13. PWM Generator x Control Register High

Name: PGxCONH
Offset: 0x32C, 0x362, 0x398, 0x3CE

Notes:

1. The PCI-selected Sync signal is always available to be OR'd with the selected SOC signal per the SOCS[3:0] bits if the PCI Sync function is enabled.
2. The source selected by the SOCS[3:0] bits MUST operate from the same clock source as the local PWM Generator. If not, the source must be routed through the PCI Sync logic so that the trigger signal may be synchronized to the PWM Generator clock domain.
3. PWM Generators are grouped into groups of four: PG1-PG4 and PG5-PG8, if available. Any generator within a group of four may be used to trigger another generator within the same group.

Legend: r = Reserved bit

Bit	15	14	13	12	11	10	9	8
	MDCSEL	MPERSEL	MPHSEL		MSTEN	UPMOD[2:0]		
Access	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0	0	0		0	0	0	0

Bit	7	6	5	4	3	2	1	0
	Reserved	TRGMOD			SOCS[3:0]			
Access	r	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit 15 – MDCSEL Master Duty Cycle Register Select bit

Value	Description
1	PWM Generator uses the MDC register.
0	PWM Generator uses the PGxDC register.

Bit 14 – MPERSEL Master Period Register Select bit

Value	Description
1	PWM Generator uses the MPER register.
0	PWM Generator uses the PGxPER register.

Bit 13 – MPHSEL Master Phase Register Select bit

Value	Description
1	PWM Generator uses the MPHASE register.
0	PWM Generator uses the PGxPHASE register.

Bit 11 – MSTEN Master Update Enable bit

Value	Description
1	PWM Generator broadcasts the software set/clear of the UPDATE status bit and EOC signal to other PWM Generators.
0	PWM Generator does not broadcast the UPDATE status bit state or EOC signal.

Bits 10:8 – UPMOD[2:0] PWM Buffer Update Mode Selection bits

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Value	Description
011	Client Immediate Update: Updates data registers immediately, or as soon as possible, when a Master update request is received. A Master update request will be transmitted if MSTEN = 1 and UPDREQ = 1 for the requesting PWM Generator.
010	Client SOC Update: Updates data registers at start of next cycle if a Master update request is received. A Master update request will be transmitted if MSTEN = 1 and UPDREQ = 1 for the requesting PWM Generator.
001	Immediate Update: Updates data registers immediately, or as soon as possible, if UPDREQ = 1. The UPDATE status bit will be cleared automatically after the update occurs.
000	SOC Update: Updates data registers at start of next PWM cycle if UPDREQ = 1. The UPDATE status bit will be cleared automatically after the update occurs.(1)

Bit 7 – Reserved Maintain as '0'

Bit 6 – TRGMOD PWM Generator Trigger Mode Selection bit

Value	Description
1	PWM Generator operates in Retriggerable mode.
0	PWM Generator operates in Single Trigger mode.

Bits 3:0 – SOCS[3:0] Start-of-Cycle Selection bits(1,2,3)

Value	Description
1111	TRIG bit or PCI Sync function only (no hardware trigger source is selected).
1110-0101	Reserved
0100	PWM4 trigger output selected by PGTRGSEL[2:0] (PGxEVT[2:0]).
0011	PWM3 trigger output selected by PGTRGSEL[2:0] (PGxEVT[2:0]).
0010	PWM2 trigger output selected by PGTRGSEL[2:0] (PGxEVT[2:0]).
0001	PWM1 trigger output selected by PGTRGSEL[2:0] (PGxEVT[2:0]).
0000	Local EOC – PWM Generator is self-triggered.

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12.6.14. PWM Generator x Status Register

Name: PGxSTAT
Offset: 0x32E, 0x364, 0x39A, 0x3D0

Note:

1. User software may write a '1' to CAP as a request to initiate a software capture. The CAP status bit will be set when the capture event has occurred. No further captures will occur until CAP is cleared by the software.

Legend: C = Clearable bit; HS = Hardware Settable bit

Bit	15	14	13	12	11	10	9	8
	SEVT	FLTEVT	CLEVT	FFEVT	SACT	FLTACT	CLACT	FFACT
Access	HS/C	HS/C	HS/C	HS/C	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRSET	TRCLR	CAP	UPDATE	UPDREQ	STEER	CAHALF	TRIG
Access	W	W	R/W/HS	R	W	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 15 – SEVT PCI Sync Event bit

Value	Description
1	A PCI Sync event has occurred (rising edge on PCI Sync output or PCI Sync output is high when module is enabled).
0	No PCI Sync event has occurred.

Bit 14 – FLTEVT PCI Fault Active Status bit

Value	Description
1	A Fault event has occurred (rising edge on PCI Fault output or PCI Fault output is high when module is enabled).
0	No Fault event has occurred.

Bit 13 – CLEVT PCI Current-Limit Status bit

Value	Description
1	A PCI current-limit event has occurred (rising edge on PCI current-limit output or PCI current-limit output is high when module is enabled).
0	No PCI current-limit event has occurred.

Bit 12 – FFEVT PCI Feed-Forward Active Status bit

Value	Description
1	A PCI feed-forward event has occurred (rising edge on PCI feed-forward output or PCI feed-forward output is high when module is enabled).
0	No PCI feed-forward event has occurred.

Bit 11 – SACT PCI Sync Status bit

Value	Description
1	PCI Sync output is active.
0	PCI Sync output is inactive.

Bit 10 – FLTACT PCI Fault Active Status bit

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Value	Description
1	PCI Fault output is active.
0	PCI Fault output is inactive.

Bit 9 – CLACT PCI Current-Limit Status bit

Value	Description
1	PCI current-limit output is active.
0	PCI current-limit output is inactive.

Bit 8 – FFACT PCI Feed-Forward Active Status bit

Value	Description
1	PCI feed-forward output is active.
0	PCI feed-forward output is inactive.

Bit 7 – TRSET PWM Generator Software Trigger Set bit
User software writes a '1' to this bit location to trigger a PWM Generator cycle. The bit location always reads as '0'. The TRIG bit will indicate '1' when the PWM Generator is triggered.

Bit 6 – TRCLR PWM Generator Software Trigger Clear bit
User software writes a '1' to this bit location to stop a PWM Generator cycle. The bit location always reads as '0'. The TRIG bit will indicate '0' when the PWM Generator is not triggered.

Bit 5 – CAP Capture Status bit(1)

Value	Description
1	PWM Generator time base value has been captured in PGxCAP.
0	No capture has occurred.

Bit 4 – UPDATE PWM Data Register Update Status/Control bit

Value	Description
1	PWM data register update is pending – user data registers are not writable.
0	No PWM data register update is pending.

Bit 3 – UPDREQ PWM Data Register Update Request bit
User software writes a '1' to this bit location to request a PWM Data register update. The bit location always reads as '0'. The UPDATE status bit will indicate '1' when an update is pending.

Bit 2 – STEER Output Steering Status bit (Push-Pull Output mode only)

Value	Description
1	PWM Generator is in second cycle of Push-Pull mode.
0	PWM Generator is in first cycle of Push-Pull mode.

Bit 1 – CAHALF Half Cycle Status bit (Center-Aligned modes only)

Value	Description
1	PWM Generator is in second half of time base cycle.
0	PWM Generator is in first half of time base cycle.

Bit 0 – TRIG PWM Trigger Status bit

Value	Description
1	PWM Generator is triggered and PWM cycle is in progress.
0	No PWM cycle is in progress.

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12.6.15. PWM Generator x I/O Control Register Low

Name: PGxIOCONL
Offset: 0x330, 0x366, 0x39C, 0x3D2

Bit	15	14	13	12	11	10	9	8
	CLMOD	SWAP	OVRENH	OVRENL	OVRDAT[1:0]		OSYNC[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FLTDAT[1:0]		CLDAT[1:0]		FFDAT[1:0]		DBDAT[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – CLMOD Current-Limit Mode Select bit

Value	Description
1	If the PCI current limit is active, then the PWMxH and PWMxL output signals are inverted (bit flipping), and the CLDAT[1:0] bits are not used.
0	If the PCI current limit is active, then the CLDAT[1:0] bits define the PWM output levels.

Bit 14 – SWAP Swap PWM Signals to PWMxH and PWMxL Device Pins bit

Value	Description
1	PWMxH signal is connected to the PWMxL pin, and the PWMxL signal is connected to the PWMxH pin.
0	PWMxH/L signals are mapped to their respective pins.

Bit 13 – OVRENH User Override Enable for PWMxH Pin bit

Value	Description
1	OVRDAT1 provides data for output on the PWMxH pin.
0	PWM Generator provides data for the PWMxH pin.

Bit 12 – OVRENL User Override Enable for PWMxL Pin bit

Value	Description
1	OVRDAT0 provides data for output on the PWMxL pin.
0	PWM Generator provides data for the PWMxL pin.

Bits 11:10 – OVRDAT[1:0] Data for PWMxH/PWMxL Pins if Override is Enabled bits
If OVERENH = 1, then OVRDAT1 provides data for PWMxH.
If OVERENL = 1, then OVRDAT0 provides data for PWMxL.

Bits 9:8 – OSYNC[1:0] User Output Override Synchronization Control bits

Value	Description
11	Reserved
10	User output overrides via the OVRENH/L and OVRDAT[1:0] bits occur when specified by the UPDMOD[2:0] bits in the PGxCONH register.
01	User output overrides via the OVRENH/L and OVRDAT[1:0] bits occur immediately (as soon as possible).
00	User output overrides via the OVRENH/L and OVRDAT[1:0] bits are synchronized to the local PWM time base (next Start-of-Cycle).

Bits 7:6 – FLTDAT[1:0] Data for PWMxH/PWMxL Pins if Fault Event is Active bits
If Fault is active, then FLTDAT1 provides data for PWMxH.

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If Fault is active, then FLTDAT0 provides data for PWMxL.

Bits 5:4 – CLDAT[1:0] Data for PWMxH/PWMxL Pins if Current-Limit Event is Active bits
If current limit is active, then CLDAT1 provides data for PWMxH.
If current limit is active, then CLDAT0 provides data for PWMxL.

Bits 3:2 – FFDAT[1:0] Data for PWMxH/PWMxL Pins if Feed-Forward Event is Active bits
If feed-forward is active, then FFDAT1 provides data for PWMxH.
If feed-forward is active, then FFDAT0 provides data for PWMxL.

Bits 1:0 – DBDAT[1:0] Data for PWMxH/PWMxL Pins if Debug Mode is Active and PTFRZ = 1 bits
If Debug mode is active and PTFRZ = 1, then DBDAT1 provides data for PWMxH.
If Debug mode is active and PTFRZ = 1, then DBDAT0 provides data for PWMxL.

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12.6.16. PWM Generator x I/O Control Register High

Name: PGxIOCONH
Offset: 0x332, 0x368, 0x39E, 0x3D4

Note:
1. A capture may be initiated in software at any time by writing a '1' to CAP (PGxSTAT[5]).

Bit	15	14	13	12	11	10	9	8
		CAPSRC[2:0]						DTCMPSEL
Access		R/W	R/W	R/W				R/W
Reset		0	0	0				0

Bit	7	6	5	4	3	2	1	0
			PMOD[1:0]		PENH	PENL	POLH	POLL
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 14:12 – CAPSRC[2:0] Time Base Capture Source Selection bits(1)

Value	Description
111	Reserved
110	Reserved
101	Reserved
100	Capture time base value at the assertion of the selected PCI Fault signal.
011	Capture time base value at the assertion of the selected PCI current-limit signal.
010	Capture the time base value at the assertion of the selected PCI feed-forward signal.
001	Capture time base value at the assertion of the selected PCI Sync signal.
000	No hardware source selected for time base capture – software only.

Bit 8 – DTCMPSEL Dead-Time Compensation Select bit

Value	Description
1	Dead-time compensation is controlled by PCI feed-forward limit logic.
0	Dead-time compensation is controlled by PCI Sync logic.

Bits 5:4 – PMOD[1:0] PWM Generator Output Mode Selection bits

Value	Description
11	Reserved
10	PWM Generator outputs operate in Push-Pull mode.
01	PWM Generator outputs operate in Independent mode.
00	PWM Generator outputs operate in Complementary mode.

Bit 3 – PENH PWMxH Output Port Enable bit

Value	Description
1	PWM Generator controls the PWMxH output pin.
0	PWM Generator does not control the PWMxH output pin.

Bit 2 – PENL PWMxL Output Port Enable bit

Value	Description
1	PWM Generator controls the PWMxL output pin.
0	PWM Generator does not control the PWMxL output pin.

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Bit 1 – POLH PWMxH Output Polarity bit

Value	Description
1	Output pin is active-low.
0	Output pin is active-high.

Bit 0 – POLL PWMxL Output Polarity bit

Value	Description
1	Output pin is active-low.
0	Output pin is active-high.

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12.6.17. PWM Generator x Event Register Low

Name: PGxEVTL
Offset: 0x334, 0x36A, 0x3A0, 0x3D6

Note:
1. These events are derived from the internal PWM Generator time-base comparison events.

Bit	15	14	13	12	11	10	9	8
	ADTR1PS[4:0]					ADTR1EN3	ADTR1EN2	ADTR1EN1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				UPDTRG[1:0]		PGTRGSEL[2:0]		
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 15:11 – ADTR1PS[4:0] ADC Trigger 1 Postscaler Selection bits

Value	Description
11111	1:32
. . .	
00010	1:3
00001	1:2
00000	1:1

Bit 10 – ADTR1EN3 ADC Trigger 1 Source is PGxTRIGC Compare Event Enable bit

Value	Description
1	PGxTRIGC register compare event is enabled as a trigger source for ADC Trigger 1.
0	PGxTRIGC register compare event is disabled as a trigger source for ADC Trigger 1.

Bit 9 – ADTR1EN2 ADC Trigger 1 Source is PGxTRIGB Compare Event Enable bit

Value	Description
1	PGxTRIGB register compare event is enabled as a trigger source for ADC Trigger 1.
0	PGxTRIGB register compare event is disabled as a trigger source for ADC Trigger 1.

Bit 8 – ADTR1EN1 ADC Trigger 1 Source is PGxTRIGA Compare Event Enable bit

Value	Description
1	PGxTRIGA register compare event is enabled as a trigger source for ADC Trigger 1.
0	PGxTRIGA register compare event is disabled as a trigger source for ADC Trigger 1.

Bits 4:3 – UPDTRG[1:0] Update Trigger Select bits

Value	Description
11	A write to the PGxTRIGA register automatically sets the UPDATE bit.
10	A write to the PGxPHASE register automatically sets the UPDATE bit.
01	A write to the PGxDC register automatically sets the UPDATE bit.
00	User must set the UPDATE bit (PGxSTAT[4]) manually.

Bits 2:0 – PGTRGSEL[2:0] PWM Generator Trigger Output Selection bits(1)

Value	Description
111	Reserved

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Value	Description
110	Reserved
101	Reserved
100	Reserved
011	PGxTRIGC compare event is the PWM Generator trigger.
010	PGxTRIGB compare event is the PWM Generator trigger.
001	PGxTRIGA compare event is the PWM Generator trigger.
000	EOC event is the PWM Generator trigger.

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12.6.18. PWM Generator x Event Register High

Name: PGxEVTH
Offset: 0x336, 0x36C, 0x3A2, 0x3D8

Notes:

1. An interrupt is only generated on the rising edge of the PCI Fault active signal.
2. An interrupt is only generated on the rising edge of the PCI current-limit active signal.
3. An interrupt is only generated on the rising edge of the PCI feed-forward active signal.
4. An interrupt is only generated on the rising edge of the PCI Sync active signal.

Bit	15	14	13	12	11	10	9	8
	FLTIEN	CLIEN	FFIEN	SIEN			IEVTSEL[1:0]	
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	0	0			0	0

Bit	7	6	5	4	3	2	1	0
	ADTR2EN3	ADTR2EN2	ADTR2EN1	ADTR1OFS[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – FLTIEN PCI Fault Interrupt Enable bit(1)

Value	Description
1	Fault interrupt is enabled.
0	Fault interrupt is disabled.

Bit 14 – CLIEN PCI Current-Limit Interrupt Enable bit(2)

Value	Description
1	Current-limit interrupt is enabled.
0	Current-limit interrupt is disabled.

Bit 13 – FFIEN PCI Feed-Forward Interrupt Enable bit(3)

Value	Description
1	Feed-forward interrupt is enabled.
0	Feed-forward interrupt is disabled.

Bit 12 – SIEN PCI Sync Interrupt Enable bit(4)

Value	Description
1	Sync interrupt is enabled.
0	Sync interrupt is disabled.

Bits 9:8 – IEVTSEL[1:0] Interrupt Event Selection bits

Value	Description
11	Time base interrupts are disabled (Sync, Fault, current-limit, and feed-forward events can be independently enabled).
10	Interrupts CPU at ADC Trigger 1 event
01	Interrupts CPU at TRIGA compare event
00	Interrupts CPU at EOC

Bit 7 – ADTR2EN3 ADC Trigger 2 Source is PGxTRIGC Compare Event Enable bit

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Value	Description
1	PGxTRIGC register compare event is enabled as a trigger source for ADC Trigger 2.
0	PGxTRIGC register compare event is disabled as a trigger source for ADC Trigger 2.

Bit 6 – ADTR2EN2 ADC Trigger 2 Source is PGxTRIGB Compare Event Enable bit

Value	Description
1	PGxTRIGB register compare event is enabled as a trigger source for ADC Trigger 2.
0	PGxTRIGB register compare event is disabled as a trigger source for ADC Trigger 2.

Bit 5 – ADTR2EN1 ADC Trigger 2 Source is PGxTRIGA Compare Event Enable bit

Value	Description
1	PGxTRIGA register compare event is enabled as a trigger source for ADC Trigger 2.
0	PGxTRIGA register compare event is disabled as a trigger source for ADC Trigger 2.

Bits 4:0 – ADTR1OFS[4:0] ADC Trigger 1 Offset Selection bits

Value	Description
11111	Offset by 31 trigger events
. . .	
00010	Offset by 2 trigger events
00001	Offset by 1 trigger event
00000	No offset

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12.6.19. PWM Generator x PCI Register Low

Name: PGxCLPCIL
Offset: 0x33C, 0x0372, 0x3A8, 0x3DE

Bit	15	14	13	12	11	10	9	8
	TSYNCDIS	TERM[2:0]			AQPS	AQSS[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SWTERM	PSYNC	PPS	PSS[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – TSYNCDIS Termination Synchronization Disable bit

Value	Description
1	Termination of latched PCI occurs immediately.
0	Termination of latched PCI occurs at PWM EOC.

Bits 14:12 – TERM[2:0] Termination Event Selection bits

Value	Description
111	Selects PCI Source #9
110	Selects PCI Source #8
101	Selects PCI Source #1 (PWM Generator output selected by the PWMPCI[2:0] bits).
100	PGxTRIGC trigger event
011	PGxTRIGB trigger event
010	PGxTRIGA trigger event
001	Auto-Terminate: Terminates when PCI source transitions from active to inactive.
000	Manual Terminate: Terminates on a write of '1' to the SWTERM bit location.

Bit 11 – AQPS Acceptance Qualifier Polarity Select bit

Value	Description
1	Inverted
0	Not inverted

Bits 10:8 – AQSS[2:0] Acceptance Qualifier Source Selection bits

Value	Description
111	SWPCI control bit only (qualifier forced to '0')
110	Selects PCI Source #9
101	Selects PCI Source #8
100	Selects PCI Source #1 (PWM Generator output selected by the PWMPCI[2:0] bits).
011	PWM Generator is triggered.
010	LEB is active.
001	Duty cycle is active (base PWM Generator signal).
000	No acceptance qualifier is used (qualifier forced to '1').

Bit 7 – SWTERM PCI Software Termination bit
A write of '1' to this location will produce a termination event. This bit location always reads as '0'.

Bit 6 – PSYNC PCI Synchronization Control bit

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Value	Description
1	PCI source is synchronized to PWM EOC.
0	PCI source is not synchronized to PWM EOC.

Bit 5 – PPS PCI Polarity Select bit

Value	Description
1	Inverted
0	Not inverted

Bits 4:0 – PSS[4:0] PCI Source Selection bits

Value	Description
11111	CLC1
11110-11101	Reserved
11100	Comparator 2 output
11011	Comparator 1 output
11010	PWM Event D
11001	PWM Event C
11000	PWM Event B
10111	PWM Event A
10110	Device pin, PCI[22]
10101	Device pin, PCI[21]
10100	Device pin, PCI[20]
10011	Device pin, PCI[19]
10010	RPn input, PCI18R
10001	RPn input, PCI17R
10000	RPn input, PCI16R
01111	RPn input, PCI15R
01110	RPn input, PCI14R
01101	RPn input, PCI13R
01100	RPn input, PCI12R
01011	RPn input, PCI11R
01010	RPn input, PCI10R
01001	RPn input, PCI9R
01000	RPn input, PCI8R
00111	Reserved
00110	Reserved
00101	Reserved
00100	Reserved
00011	Internally connected to Combo Trigger B
00010	Internally connected to Combo Trigger A
00001	Internally connected to the output of PWMPCI[2:0] MUX
00000	Tied to '0'

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12.6.20. PWM Generator x PCI Register High

Name: PGxCLPCIH
Offset: 0x33E, 0x374, 0x3AA, 0x3E0

Note:
1. Selects '0' if selected PWM Generator is not present.

Bit	15	14	13	12	11	10	9	8
	BPEN	BPSEL[2:0]				ACP[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	SWPCI	SWPCIM[1:0]		LATMOD	TQPS	TQSS[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – BPEN PCI Bypass Enable bit

Value	Description
1	PCI function is enabled, and local PCI logic is bypassed; the PWM Generator will be controlled by the PCI function in the PWM Generator selected by the BPSEL[2:0] bits.
0	PCI function is not bypassed.

Bits 14:12 – BPSEL[2:0] PCI Bypass Source Selection bits(1)

Value	Description
111-100	Reserved
011	PCI control is sourced from PWM Generator 4 PCI logic when BPEN = 1.
010	PCI control is sourced from PWM Generator 3 PCI logic when BPEN = 1.
001	PCI control is sourced from PWM Generator 2 PCI logic when BPEN = 1.
000	PCI control is sourced from PWM Generator 1 PCI logic when BPEN = 1.

Bits 10:8 – ACP[2:0] PCI Acceptance Criteria Selection bits

Value	Description
111	Reserved
110	Reserved
101	Latched any edge
100	Latched rising edge
011	Latched
010	Any edge
001	Rising edge
000	Level-sensitive

Bit 7 – SWPCI Software PCI Control bit

Value	Description
1	Drives a '1' to PCI logic assigned to by the SWPCIM[1:0] control bits.
0	Drives a '0' to PCI logic assigned to by the SWPCIM[1:0] control bits.

Bits 6:5 – SWPCIM[1:0] Software PCI Control Mode bits

Value	Description
11	Reserved

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Value	Description
10	SWPCI bit is assigned to termination qualifier logic.
01	SWPCI bit is assigned to acceptance qualifier logic.
00	SWPCI bit is assigned to PCI acceptance logic.

Bit 4 – LATMOD PCI SR Latch Mode bit

Value	Description
1	SR latch is Reset-dominant in Latched Acceptance modes.
0	SR latch is Set-dominant in Latched Acceptance modes.

Bit 3 – TQPS Termination Qualifier Polarity Select bit

Value	Description
1	Inverted
0	Not inverted

Bits 2:0 – TQSS[2:0] Termination Qualifier Source Selection bits

Value	Description
111	SWPCI control bit only (qualifier forced to '0').
110	Selects PCI Source #9
101	Selects PCI Source #8
100	Selects PCI Source #1 (PWM Generator output selected by the PWMPCI[2:0] bits).
011	PWM Generator is triggered
010	LEB is active
001	Duty cycle is active (base PWM Generator signal).
000	No termination qualifier used (qualifier forced to '1').

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12.6.21. PWM Generator x PCI Register Low

Name: PGxFPCIL
Offset: 0x338, 0x36E, 0x3A4, 0x3DA

Bit	15	14	13	12	11	10	9	8
	TSYNCDIS	TERM[2:0]			AQPS	AQSS[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SWTERM	PSYNC	PPS	PSS[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – TSYNCDIS Termination Synchronization Disable bit

Value	Description
1	Termination of latched PCI occurs immediately.
0	Termination of latched PCI occurs at PWM EOC.

Bits 14:12 – TERM[2:0] Termination Event Selection bits

Value	Description
111	Selects PCI Source #9
110	Selects PCI Source #8
101	Selects PCI Source #1 (PWM Generator output selected by the PWMPCI[2:0] bits).
100	PGxTRIGC trigger event
011	PGxTRIGB trigger event
010	PGxTRIGA trigger event
001	Auto-Terminate: Terminates when PCI source transitions from active to inactive.
000	Manual Terminate: Terminates on a write of '1' to the SWTERM bit location.

Bit 11 – AQPS Acceptance Qualifier Polarity Select bit

Value	Description
1	Inverted
0	Not inverted

Bits 10:8 – AQSS[2:0] Acceptance Qualifier Source Selection bits

Value	Description
111	SWPCI control bit only (qualifier forced to '0')
110	Selects PCI Source #9
101	Selects PCI Source #8
100	Selects PCI Source #1 (PWM Generator output selected by the PWMPCI[2:0] bits).
011	PWM Generator is triggered.
010	LEB is active
001	Duty cycle is active (base PWM Generator signal).
000	No acceptance qualifier is used (qualifier forced to '1').

Bit 7 – SWTERM PCI Software Termination bit
A write of '1' to this location will produce a termination event. This bit location always reads as '0'.

Bit 6 – PSYNC PCI Synchronization Control bit

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Value	Description
1	PCI source is synchronized to PWM EOC.
0	PCI source is not synchronized to PWM EOC.

Bit 5 – PPS PCI Polarity Select bit

Value	Description
1	Inverted
0	Not inverted

Bits 4:0 – PSS[4:0] PCI Source Selection bits

Value	Description
11111	CLC1
11110-11101	Reserved
11100	Comparator 2 output
11011	Comparator 1 output
11010	PWM Event D
11001	PWM Event C
11000	PWM Event B
10111	PWM Event A
10110	Device pin, PCI[22]
10101	Device pin, PCI[21]
10100	Device pin, PCI[20]
10011	Device pin, PCI[19]
10010	RPn input, PCI18R
10001	RPn input, PCI17R
10000	RPn input, PCI16R
01111	RPn input, PCI15R
01110	RPn input, PCI14R
01101	RPn input, PCI13R
01100	RPn input, PCI12R
01011	RPn input, PCI11R
01010	RPn input, PCI10R
01001	RPn input, PCI9R
01000	RPn input, PCI8R
00111	Reserved
00110	Reserved
00101	Reserved
00100	Reserved
00011	Internally connected to Combo Trigger B.
00010	Internally connected to Combo Trigger A.
00001	Internally connected to the output of PWMPCI[2:0] MUX.
00000	Tied to '0'

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12.6.22. PWM Generator x PCI Register High

Name: PGxFPCIH
Offset: 0x33A, 0x370, 0x3A6, 0x3DC

Note:
1. Selects '0' if selected PWM Generator is not present.

Bit	15	14	13	12	11	10	9	8
	BPEN	BPSEL[2:0]				ACP[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	SWPCI	SWPCIM[1:0]		LATMOD	TQPS	TQSS[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – BPEN PCI Bypass Enable bit

Value	Description
1	PCI function is enabled, and local PCI logic is bypassed; the PWM Generator will be controlled by the PCI function in the PWM Generator selected by the BPSEL[2:0] bits.
0	PCI function is not bypassed.

Bits 14:12 – BPSEL[2:0] PCI Bypass Source Selection bits(1)

Value	Description
111-100	Reserved
011	PCI control is sourced from PWM Generator 4 PCI logic when BPEN = 1.
010	PCI control is sourced from PWM Generator 3 PCI logic when BPEN = 1.
001	PCI control is sourced from PWM Generator 2 PCI logic when BPEN = 1.
000	PCI control is sourced from PWM Generator 1 PCI logic when BPEN = 1.

Bits 10:8 – ACP[2:0] PCI Acceptance Criteria Selection bits

Value	Description
111	Reserved
110	Reserved
101	Latched any edge
100	Latched rising edge
011	Latched
010	Any edge
001	Rising edge
000	Level-sensitive

Bit 7 – SWPCI Software PCI Control bit

Value	Description
1	Drives a '1' to PCI logic assigned to by the SWPCIM[1:0] control bits.
0	Drives a '0' to PCI logic assigned to by the SWPCIM[1:0] control bits.

Bits 6:5 – SWPCIM[1:0] Software PCI Control Mode bits

Value	Description
11	Reserved

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Value	Description
10	SWPCI bit is assigned to termination qualifier logic.
01	SWPCI bit is assigned to acceptance qualifier logic.
00	SWPCI bit is assigned to PCI acceptance logic.

Bit 4 – LATMOD PCI SR Latch Mode bit

Value	Description
1	SR latch is Reset-dominant in Latched Acceptance modes.
0	SR latch is Set-dominant in Latched Acceptance modes.

Bit 3 – TQPS Termination Qualifier Polarity Select bit

Value	Description
1	Inverted
0	Not inverted

Bits 2:0 – TQSS[2:0] Termination Qualifier Source Selection bits

Value	Description
111	SWPCI control bit only (qualifier forced to '0')
110	Selects PCI Source #9
101	Selects PCI Source #8
100	Selects PCI Source #1 (PWM Generator output selected by the PWMPCI[2:0] bits).
011	PWM Generator is triggered.
010	LEB is active.
001	Duty cycle is active (base PWM Generator signal).
000	No termination qualifier used (qualifier forced to '1').

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12.6.23. PWM Generator x Leading-Edge Blanking Register Low

Name: PGxLEBL
Offset: 0x348, 0x37E, 0x3B4, 0x3EA

Note:

1. Bits[2:0] are read-only and always remain as '0'.

Bit	15	14	13	12	11	10	9	8
	LEB[12:5]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LEB[4:0]							
Access	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0			

Bits 15:3 – LEB[12:0] Leading-Edge Blanking Period bits(1)
Leading-Edge Blanking period. The three LSBs of the blanking time are not used, providing a blanking resolution of eight clock periods. The minimum blanking period is eight clock periods, which occurs when LEB[15:3] = 0.

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12.6.24. PWM Generator x Leading-Edge Blanking Register High

Name: PGxLEBH
Offset: 0x34A, 0x380, 0x3B6, 0x3EC

Note:

1. The selected PWM Generator source does not affect the LEB counter. This source can be optionally used as a PCI input, PCI qualifier, PCI terminator, or PCI terminator qualifier (see the description in PGxCLPCIL and PGxCLPCIH for more information).

Bit	15	14	13	12	11	10	9	8
						PWMPCI[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
					PHR	PHF	PLR	PLF
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 10:8 – PWMPCI[2:0] PWM Source for PCI Selection bits(1)

Value	Description
111–100	Reserved
011	PWM Generator #4 output is made available to PCI logic.
010	PWM Generator #3 output is made available to PCI logic.
001	PWM Generator #2 output is made available to PCI logic.
000	PWM Generator #1 output is made available to PCI logic.

Bit 3 – PHR PWMxH Rising bit

Value	Description
1	Rising edge of PWMxH will trigger the LEB duration counter.
0	LEB ignores the rising edge of PWMxH.

Bit 2 – PHF PWMxH Falling bit

Value	Description
1	Falling edge of PWMxH will trigger the LEB duration counter.
0	LEB ignores the falling edge of PWMxH.

Bit 1 – PLR PWMxL Rising bit

Value	Description
1	Rising edge of PWMxL will trigger the LEB duration counter.
0	LEB ignores the rising edge of PWMxL.

Bit 0 – PLF PWMxL Falling bit

Value	Description
1	Falling edge of PWMxL will trigger the LEB duration counter.
0	LEB ignores the falling edge of PWMxL.

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12.6.25. PWM Generator x PCI Register Low

Name: PGxFFPCIL
Offset: 0x340, 0x376, 0x3AC, 0x3E2

Bit	15	14	13	12	11	10	9	8
	TSYNCDIS	TERM[2:0]			AQPS	AQSS[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SWTERM	PSYNC	PPS	PSS[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – TSYNCDIS Termination Synchronization Disable bit

Value	Description
1	Termination of latched PCI occurs immediately.
0	Termination of latched PCI occurs at PWM EOC.

Bits 14:12 – TERM[2:0] Termination Event Selection bits

Value	Description
111	Selects PCI Source #9
110	Selects PCI Source #8
101	Selects PCI Source #1 (PWM Generator output selected by the PWMPCI[2:0] bits).
100	PGxTRIGC trigger event
011	PGxTRIGB trigger event
010	PGxTRIGA trigger event
001	Auto-Terminate: Terminates when PCI source transitions from active to inactive.
000	Manual Terminate: Terminates on a write of '1' to the SWTERM bit location.

Bit 11 – AQPS Acceptance Qualifier Polarity Select bit

Value	Description
1	Inverted
0	Not inverted

Bits 10:8 – AQSS[2:0] Acceptance Qualifier Source Selection bits

Value	Description
111	SWPCI control bit only (qualifier forced to '0').
110	Selects PCI Source #9
101	Selects PCI Source #8
100	Selects PCI Source #1 (PWM Generator output selected by the PWMPCI[2:0] bits).
011	PWM Generator is triggered.
010	LEB is active.
001	Duty cycle is active (base PWM Generator signal).
000	No acceptance qualifier is used (qualifier forced to '1').

Bit 7 – SWTERM PCI Software Termination bit
A write of '1' to this location will produce a termination event. This bit location always reads as '0'.

Bit 6 – PSYNC PCI Synchronization Control bit

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Value	Description
1	PCI source is synchronized to PWM EOC.
0	PCI source is not synchronized to PWM EOC.

Bit 5 – PPS PCI Polarity Select bit

Value	Description
1	Inverted
0	Not inverted

Bits 4:0 – PSS[4:0] PCI Source Selection bits

Value	Description
11111	CLC1
11110	Reserved
11101	Comparator 3 output
11100	Comparator 2 output
11011	Comparator 1 output
11010	PWM Event D
11001	PWM Event C
11000	PWM Event B
10111	PWM Event A
10110	Device pin, PCI[22]
10101	Device pin, PCI[21]
10100	Device pin, PCI[20]
10011	Device pin, PCI[19]
10010	RPn input, PCI18R
10001	RPn input, PCI17R
10000	RPn input, PCI16R
01111	RPn input, PCI15R
01110	RPn input, PCI14R
01101	RPn input, PCI13R
01100	RPn input, PCI12R
01011	RPn input, PCI11R
01010	RPn input, PCI10R
01001	RPn input, PCI9R
01000	RPn input, PCI8R
00111	Reserved
00110	Reserved
00101	Reserved
00100	Reserved
00011	Internally connected to Combo Trigger B.
00010	Internally connected to Combo Trigger A.
00001	Internally connected to the output of PWMPCI[2:0] MUX.
00000	Tied to '0'.

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12.6.26. PWM Generator x PCI Register High

Name: PGxFFPCIH
Offset: 0x342, 0x378, 0x3AE, 0x3E4

Note:
1. Selects '0' if selected PWM Generator is not present.

Bit	15	14	13	12	11	10	9	8
	BPEN	BPSEL[2:0]				ACP[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	SWPCI	SWPCIM[1:0]		LATMOD	TQPS	TQSS[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – BPEN PCI Bypass Enable bit

Value	Description
1	PCI function is enabled, and the local PCI logic is bypassed; the PWM Generator will be controlled by the PCI function in the PWM Generator selected by the BPSEL[2:0] bits.
0	PCI function is not bypassed.

Bits 14:12 – BPSEL[2:0] PCI Bypass Source Selection bits(1)

Value	Description
111	PCI control is sourced from PWM Generator 8 PCI logic when BPEN = 1.
110	PCI control is sourced from PWM Generator 7 PCI logic when BPEN = 1.
101	PCI control is sourced from PWM Generator 6 PCI logic when BPEN = 1.
100	PCI control is sourced from PWM Generator 5 PCI logic when BPEN = 1.
011	PCI control is sourced from PWM Generator 4 PCI logic when BPEN = 1.
010	PCI control is sourced from PWM Generator 3 PCI logic when BPEN = 1.
001	PCI control is sourced from PWM Generator 2 PCI logic when BPEN = 1.
000	PCI control is sourced from PWM Generator 1 PCI logic when BPEN = 1.

Bits 10:8 – ACP[2:0] PCI Acceptance Criteria Selection bits

Value	Description
111	Reserved
110	Reserved
101	Latched any edge
100	Latched rising edge
011	Latched
010	Any edge
001	Rising edge
000	Level-sensitive

Bit 7 – SWPCI Software PCI Control bit

Value	Description
1	Drives a '1' to PCI logic assigned by the SWPCIM[1:0] control bits.
0	Drives a '0' to PCI logic assigned by the SWPCIM[1:0] control bits.

Bits 6:5 – SWPCIM[1:0] Software PCI Control Mode bits

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Value	Description
11	Reserved
10	SWPCI bit is assigned to termination qualifier logic.
01	SWPCI bit is assigned to acceptance qualifier logic.
00	SWPCI bit is assigned to PCI acceptance logic.

Bit 4 – LATMOD PCI SR Latch Mode bit

Value	Description
1	SR latch is Reset-dominant in Latched Acceptance modes.
0	SR latch is Set-dominant in Latched Acceptance modes.

Bit 3 – TQPS Termination Qualifier Polarity Select bit

Value	Description
1	Inverted
0	Not inverted

Bits 2:0 – TQSS[2:0] Termination Qualifier Source Selection bits

Value	Description
111	SWPCI control bit only (qualifier forced to '0').
110	Selects PCI Source #9
101	Selects PCI Source #8
100	Selects PCI Source #1 (PWM Generator output selected by the PWMPCI[2:0] bits).
011	PWM Generator is triggered.
010	LEB is active.
001	Duty cycle is active (base PWM Generator signal).
000	No termination qualifier used (qualifier forced to '1').

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12.6.27. PWM Generator x Select PCI Register Low

Name: PGxSPCIL
Offset: 0x344, 0x37A, 0x3B0, 0x3E6

Bit	15	14	13	12	11	10	9	8
	TSYNCDIS	TERM[2:0]			AQPS	AQSS[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SWTERM	PSYNC	PPS	PSS[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – TSYNCDIS Termination Synchronization Disable bit

Value	Description
1	Termination of latched PCI occurs immediately.
0	Termination of latched PCI occurs at PWM EOC.

Bits 14:12 – TERM[2:0] Termination Event Selection bits

Value	Description
111	Selects PCI Source #9
110	Selects PCI Source #8
101	Selects PCI Source #1 (PWM Generator output selected by the PWMPCI[2:0] bits).
100	PGxTRIGC trigger event
011	PGxTRIGB trigger event
010	PGxTRIGA trigger event
001	Auto-Terminate: Terminates when PCI source transitions from active to inactive.
000	Manual Terminate: Terminates on a write of '1' to the SWTERM bit location.

Bit 11 – AQPS Acceptance Qualifier Polarity Select bit

Value	Description
1	Inverted
0	Not inverted

Bits 10:8 – AQSS[2:0] Acceptance Qualifier Source Selection bits

Value	Description
111	SWPCI control bit only (qualifier forced to '0').
110	Selects PCI Source #9
101	Selects PCI Source #8
100	Selects PCI Source #1 (PWM Generator output selected by the PWMPCI[2:0] bits).
011	PWM Generator is triggered.
010	LEB is active.
001	Duty cycle is active (base PWM Generator signal).
000	No acceptance qualifier is used (qualifier forced to '1').

Bit 7 – SWTERM PCI Software Termination bit
A write of '1' to this location will produce a termination event. This bit location always reads as '0'.

Bit 6 – PSYNC PCI Synchronization Control bit

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Value	Description
1	PCI source is synchronized to PWM EOC.
0	PCI source is not synchronized to PWM EOC.

Bit 5 – PPS PCI Polarity Select bit

Value	Description
1	Inverted
0	Not inverted

Bits 4:0 – PSS[4:0] PCI Source Selection bits

Value	Description
11111	CLC1
11110	Reserved
11101	Comparator 3 output
11100	Comparator 2 output
11011	Comparator 1 output
11010	PWM Event D
11001	PWM Event C
11000	PWM Event B
10111	PWM Event A
10110	Device pin, PCI[22]
10101	Device pin, PCI[21]
10100	Device pin, PCI[20]
10011	Device pin, PCI[19]
10010	RPn input, PCI18R
10001	RPn input, PCI17R
10000	RPn input, PCI16R
01111	RPn input, PCI15R
01110	RPn input, PCI14R
01101	RPn input, PCI13R
01100	RPn input, PCI12R
01011	RPn input, PCI11R
01010	RPn input, PCI10R
01001	RPn input, PCI9R
01000	RPn input, PCI8R
00111	Reserved
00110	Reserved
00101	Reserved
00100	Reserved
00011	Internally connected to Combo Trigger B
00010	Internally connected to Combo Trigger A
00001	Internally connected to the output of PWMPCI[2:0] MUX.
00000	Tied to '0'

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12.6.28. PWM Generator x Select PCI Register High

Name: PGxSPCIH
Offset: 0x346, 0x37C, 0x3B2, 0x3E8

Note:
1. Selects '0' if selected PWM Generator is not present.

Bit	15	14	13	12	11	10	9	8
	BPEN	BPSEL[2:0]				ACP[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	SWPCI	SWPCIM[1:0]		LATMOD	TQPS	TQSS[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – BPEN PCI Bypass Enable bit

Value	Description
1	PCI function is enabled, and the local PCI logic is bypassed; the PWM Generator will be controlled by the PCI function in the PWM Generator selected by the BPSEL[2:0] bits.
0	PCI function is not bypassed.

Bits 14:12 – BPSEL[2:0] PCI Bypass Source Selection bits(1)

Value	Description
111	PCI control is sourced from PWM Generator 8 PCI logic when BPEN = 1.
110	PCI control is sourced from PWM Generator 7 PCI logic when BPEN = 1.
101	PCI control is sourced from PWM Generator 6 PCI logic when BPEN = 1.
100	PCI control is sourced from PWM Generator 5 PCI logic when BPEN = 1.
011	PCI control is sourced from PWM Generator 4 PCI logic when BPEN = 1.
010	PCI control is sourced from PWM Generator 3 PCI logic when BPEN = 1.
001	PCI control is sourced from PWM Generator 2 PCI logic when BPEN = 1.
000	PCI control is sourced from PWM Generator 1 PCI logic when BPEN = 1.

Bits 10:8 – ACP[2:0] PCI Acceptance Criteria Selection bits

Value	Description
111	Reserved
110	Reserved
101	Latched any edge
100	Latched rising edge
011	Latched
010	Any edge
001	Rising edge
000	Level-sensitive

Bit 7 – SWPCI Software PCI Control bit

Value	Description
1	Drives a '1' to PCI logic assigned to by the SWPCIM[1:0] control bits.
0	Drives a '0' to PCI logic assigned to by the SWPCIM[1:0] control bits.

Bits 6:5 – SWPCIM[1:0] Software PCI Control Mode bits

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Value	Description
11	Reserved
10	SWPCI bit is assigned to termination qualifier logic.
01	SWPCI bit is assigned to acceptance qualifier logic.
00	SWPCI bit is assigned to PCI acceptance logic.

Bit 4 – LATMOD PCI SR Latch Mode bit

Value	Description
1	SR latch is Reset-dominant in Latched Acceptance modes.
0	SR latch is Set-dominant in Latched Acceptance modes.

Bit 3 – TQPS Termination Qualifier Polarity Select bit

Value	Description
1	Inverted
0	Not inverted

Bits 2:0 – TQSS[2:0] Termination Qualifier Source Selection bits

Value	Description
111	SWPCI control bit only (qualifier forced to '0').
110	Selects PCI Source #9
101	Selects PCI Source #8
100	Selects PCI Source #1 (PWM Generator output selected by the PWMPCI[2:0] bits).
011	PWM Generator is triggered.
010	LEB is active.
001	Duty cycle is active (base PWM Generator signal).
000	No termination qualifier used (qualifier forced to '1').

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12.6.29. PWM Generator x Phase Register

Name: PGxPHASE
Offset: 0x34C, 0x382, 0x3B8, 0x3EE

Bit	15	14	13	12	11	10	9	8
	PGxPHASE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PGxPHASE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PGxPHASE[15:0] PWM Generator x Phase Register bits

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12.6.30. PWM Generator x Duty Cycle Register

Name: PGxDC
Offset: 0x34E, 0x384, 0x3BA, 0x3F0

Note:

1. Duty cycle values less than '0x0008' should not be used.

Bit	15	14	13	12	11	10	9	8
	PGxDC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PGxDC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PGxDC[15:0] PWM Generator x Duty Cycle Register bits(1)

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12.6.31. PWM Generator x Duty Cycle Adjustment Register

Name: PGxDCA
Offset: 0x350, 0x386, 0x3BC, 0x3F2

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PGxDCA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PGxDCA[7:0] PWM Generator x Duty Cycle Adjustment Value bits
Depending on the state of the selected PCI source, the PGxDCA value will be added to the value in the PGxDC register to create the effective duty cycle. When the PCI source is active, PGxDCA is added. When the PCI source is inactive, no adjustment is made. Duty cycle adjustment is disabled when PGxDCA[7:0] = 0. The PCI source is selected using the DTCMPSEL bit.

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12.6.32. PWM Generator x Period Register

Name: PGxPER
Offset: 0x352, 0x388, 0x3BE, 0x3F4

Note:

1. Period values less than '0x0010' should not be selected.

Bit	15	14	13	12	11	10	9	8
	PGxPER[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PGxPER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PGxPER[15:0] PWM Generator x Period Register bits(1)

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12.6.33. PWM Generator x Trigger A Register

Name: PGxTRIGA
Offset: 0x354, 0x38A, 0x3C0, 0x3F6

Bit	15	14	13	12	11	10	9	8
	PGxTRIGA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PGxTRIGA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PGxTRIGA[15:0] PWM Generator x Trigger A Register bits

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12.6.34. PWM Generator x Trigger B Register

Name: PGxTRIGB
Offset: 0x356, 0x38C, 0x3C2, 0x3F8

Bit	15	14	13	12	11	10	9	8
	PGxTRIGB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PGxTRIGB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PGxTRIGB[15:0] PWM Generator x Trigger B Register bits

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12.6.35. PWM Generator x Trigger C Register

Name: PGxTRIGC
Offset: 0x358, 0x38E, 0x3C4, 0x3FA

Bit	15	14	13	12	11	10	9	8
	PGxTRIGC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PGxTRIGC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PGxTRIGC[15:0] PWM Generator x Trigger C Register bits

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12.6.36. PWM Generator x Dead-Time Register Low

Name: PGxDTL
Offset: 0x35A, 0x390, 0x3C6, 0x3FC

Bit	15	14	13	12	11	10	9	8
						DTL[10:8]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
	DTL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 10:0 – DTL[10:0] PWMxL Dead-Time Delay bits

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12.6.37. PWM Generator x Dead-Time Register High

Name: PGxDTH
Offset: 0x35C, 0x392, 0x3C8, 0x3FE

Bit	15	14	13	12	11	10	9	8
						DTH[10:8]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
	DTH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 10:0 – DTH[10:0] PWMxH Dead-Time Delay bits

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12.6.38. PWM Generator x Capture Register

Name: PGxCAP
Offset: 0x35E, 0x394, 0x3CA, 0x400

Note:

1. A capture event can be manually initiated in software by writing a '1' to PGxCAP[0]. The CAP bit (PGxSTAT[5]) will indicate when a new capture value is available. A read of PGxCAP will automatically clear the CAP bit and allow a new capture event to occur. The PGxCAP[1:0] bits will always read as '0'.

Bit	15	14	13	12	11	10	9	8
	PGxCAP[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PGxCAP[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PGxCAP[15:0] PGx Time Base Capture bits(1)

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13. MOSFET Gate Driver Module

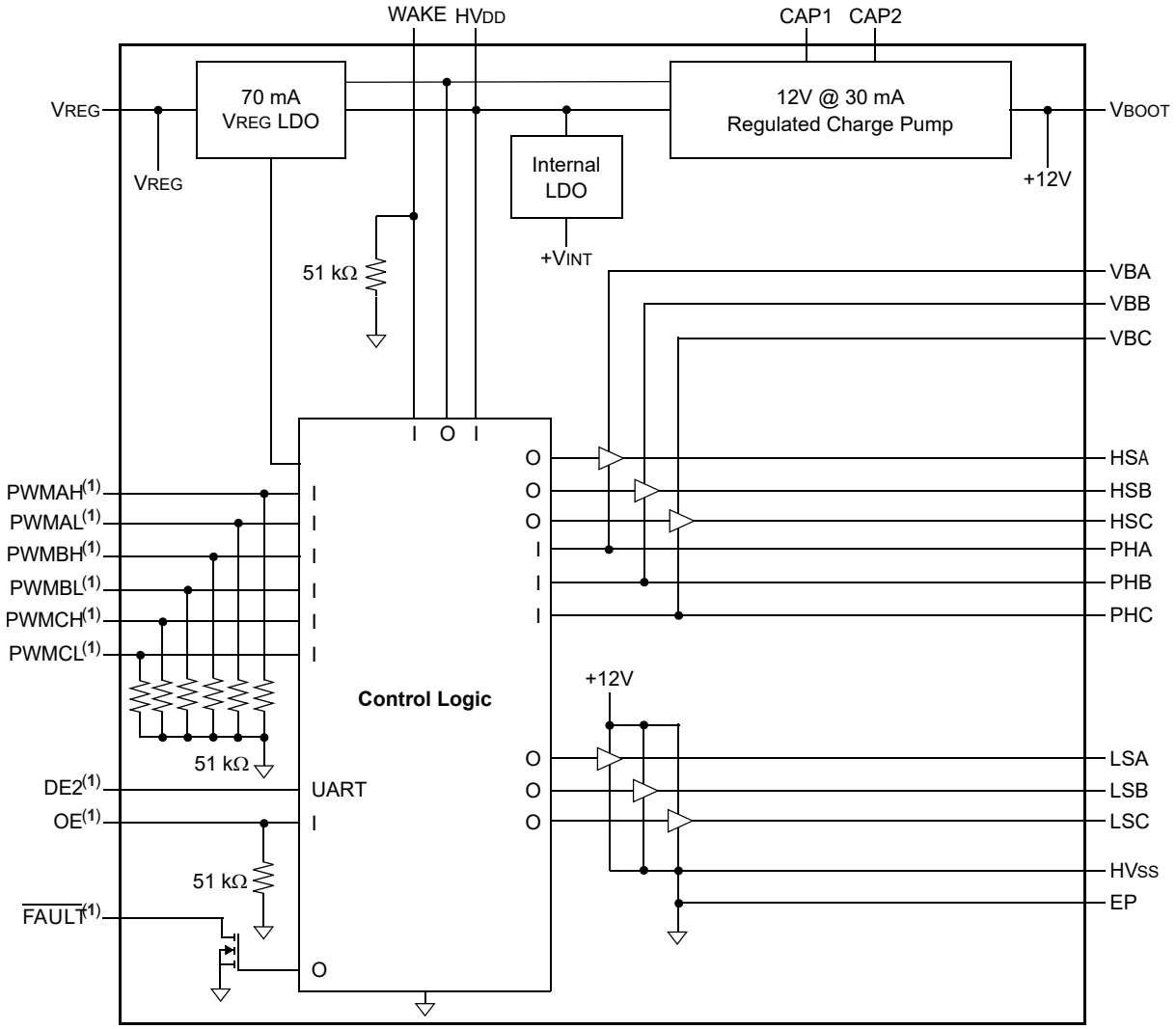
The MOSFET Gate Driver module (MOSFET Driver module) incorporates a number of functions, that when paired with the host dsPIC® DSC, provides a single chip solution for controlling low-voltage motors. The MOSFET Driver module includes:

- Bias Generator:
  - +12V Low-Dropout (LDO) Linear Regulator
    - Charge Pump
  - +3.3V @ 70 mA LDO can be used to power the Host dsPIC DSC
    - Input supply and temperature supervisor
- Motor Control Unit:
  - External drive for a three-phase bridge with NMOS/NMOS MOSFET pairs
- Communication Port:
  - Half-duplex UART with internal connection to the Host dsPIC DSC

Figure 13-1 depicts the functional block diagram of the MOSFET Driver module and Figure 13-2 depicts a typical application circuit.

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Figure 13-1. Functional Block Diagram – MOSFET Gate Driver Module

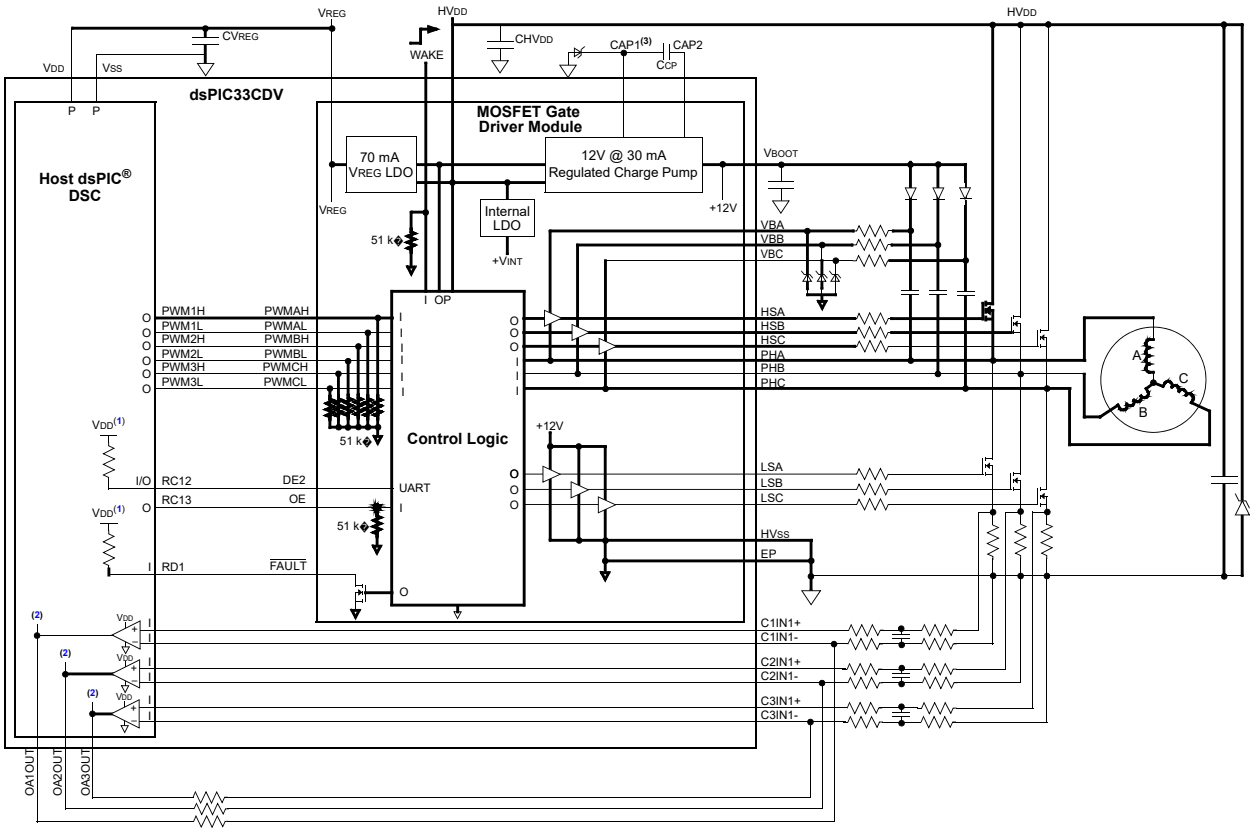


Note:

1. Device interconnect is connected directly to the Host microcontroller within the dsPIC33CDVL256MC506 device package.

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Figure 13-2. MOSFET Gate Driver Module – Typical Motor Control Application Circuit



Notes:

1. Internal pull-up resistors for RC12 and RD1 must be enabled by the user by setting the corresponding bits in the CNPUC and CNPUD registers, respectively.
2. The ADC can be configured to internally sample Op Amp outputs.
3. A Schottky diode between the CAP1 pin and HV_{SS} is recommended to ensure that the CAP1 pin absolute minimum voltage specification of -0.3V is maintained.

13.1. Communications Port (DE2 Interconnect)

Open-drain communications node. The DE2 communications is a half-duplex, 9600 baud, 8-bit, no parity communications link. The pin has a minimum drive capability of 1 mA with a VDE2 of ≤50 mV when driving low.

The following configurations are required for successful DE2 communication between the host dsPIC and the MOSFET Gate Driver module:

- Enable the internal pull-up resistor of port pin RC12 (CNPUC[12] = 1). Doing so before powering on MCP8021 can lead to current sinking through MCP8021's DE2 pin input impedance to ground.
- TRISC12 = 1. Essential for PPS input assignments to ensure data from MCP8021 reaches UART RX buffer.
- PPS assignment of both RX and TX to port pin RC12

13.2. Low-Side PWM Inputs (PWMAL, PWMBL, PWMCL)

Digital PWM Inputs for low-side driver control. Each input has a 51 kΩ pull-down to ground. The PWM signals may contain dead-time timing or the system may use the CFG2 Configuration register to set the dead time.

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13.3. High-Side PWM Inputs (PWMAH, PWMBH, PWMCH)

Digital PWM inputs for high-side driver control. Each input has a 51 kΩ pull-down to ground. The PWM signals may contain dead-time timing or the system may use the CFG2 Configuration register to set the dead time.

13.4. Output Enable (OE) Input

The Output Enable Input pin is used to enable/disable the output driver and the on-board functions. When OE is high, all device functions are enabled. When OE is low, the device operates in Standby or Sleep mode. When Standby mode is active, the V_{BOOT} output supply and charge pump are disabled. The high-side and low-side gate drive outputs are all set to a Low state within 100 ns of OE going low. The device transitions to Standby or Sleep mode, 1 ms after OE goes low.

The OE pin may be used to clear any hardware Faults. When a Fault occurs, the OE input may be used to clear the Fault by setting the pin low and then high again. The Fault is cleared by the rising edge of the OE signal if the hardware Fault is no longer active.

The OE pin is used to enable Sleep mode when the SLEEP bit in the CFG0 Configuration register is set to a '1'. OE must be low for a minimum of ms before the transition to Standby or Sleep mode will occur. This allows time for OE to be toggled, to clear any Faults, without going into Sleep mode.

The OE pin has an internal 51 kΩ pull-down to ground.

13.5. Fault Output ($\overline{\text{FAULT}}$)

$\overline{\text{FAULT}}$ Output pin. The latched open-drain output will go low while a Fault is active. Table 13-5 shows the Faults that cause the FAULT pin to go low. The pin will stay low until the Fault is inactive and the OE pin is toggled, from low-to-high, to clear the internal Fault latch.

The $\overline{\text{FAULT}}$ pin is able to sink 1mA of current while maintaining less than a 50 mV drop across the output.

The $\overline{\text{FAULT}}$ pin will also be active (low) upon initial power-up until the state machine completes the VREG state. This may be used to signal an external host that the driver is ready.

13.6. Wake Input (WAKE)

The WAKE pin has an internal 51 kΩ pull-down to ground.

The device will awaken from Sleep mode on a high level of the WAKE pin, lasting for longer than tWAIT_SETUP. The WAKE pin is capable of operating at voltage levels up to HVDD.

Note: The WAKE pin of the device has different requirements between revisions D2 and D3. See Table 13-1 for details between the two revisions.

Table 13-1. WAKE Pin Revision Details

Revision	WAKE Pin	Requirement to Wake Device from Sleep Mode
D2	Edge Sensitive	WAIT > t_{WAIT_SETUP} before sending rising-edge to WAKE pin
D3	High-Level Sensitive	Maintain a high level on the WAKE pin lasting > than t_{WAIT_SETUP}

13.7. Motor Phase Inputs (PHA, PHB, PHC)

Phase signals from the motor. These signals provide a high-side N-channel MOSFET driver bias reference and Back EMF sense input. The phase signals are also used with the bootstrap capacitors to provide a high-side gate drive via the VBx inputs.

13.8. High-Side N-MOSFET Gate Driver Outputs (HSA, HSB, HSC)

High-Side N-Channel MOSFET Gate Drive signals. Connect to the gate of the external MOSFETs. A resistor and gate- to-source capacitor may be used between HSA, HSB and HSC pins and the MOSFET gates to limit a phase node slew rate and MOSFET current.

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13.9. Bootstrap Inputs (VBA, VBB, VBC)

High-side MOSFET driver bias. Connect the VBA, VBB and VBC pins between the bootstrap charge pump diode cathode and the bootstrap charge pump capacitor. The VBOOT output is used to provide the bootstrap supply voltage at the diode anodes. The phase signals are connected to the other side of the bootstrap charge pump capacitors. The bootstrap capacitors charge to VBOOT when the phase signals are pulled low by the low-side drivers. When the low-side drivers turn off and the high-side drivers turn on, the phase signal is pulled to HVDD, causing the bootstrap voltage to rise to HVDD + 12V.

13.10. Low-Side N-MOSFET Gate Driver Outputs (LSA, LSB, LSC)

Low-Side N-Channel MOSFET Drive signals. Connect to the gate of the external MOSFETs. A resistor and gate-to-source capacitor may be used between the LSA, LSB and LSC pins and the MOSFET gates to limit current and slew rate.

13.11. Bootstrap Supply (V_{BOOT})

Bootstrap Supply voltage regulator output. The V_{BOOT} regulator output may be used to power external devices, such as Hall effect sensors or amplifiers. The regulator output requires an output capacitor for stability. The positive side of the output capacitor should be physically located as close to the V_{BOOT} pin as is practical. A minimum capacitance of 4.7 µF is required to ensure stable operation of the V_{BOOT} circuit. Larger capacitances may be used to increase transient performance. The V_{BOOT} regulator is supplied by the internal charge pump when the charge pump is active. When the charge pump is inactive, the V_{BOOT} regulator is supplied by HV_{DD}.

The type of capacitor used may be ceramic, tantalum or aluminum electrolytic. The low-ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

13.12. +3.3V (VREG)

The V_{REG} LDO may be used to power external devices, such as Hall effect sensors, amplifiers or host processors. The V_{REG} LDO is enabled when the device is not in Sleep mode and the supply voltage is above the device shutdown voltage. The LDO requires an output capacitor for stability. The positive side of the output capacitor should be physically located as close to the V_{REG} pin as is practical. For most applications, a minimum 4.7 µF of capacitance will ensure stable operation of the LDO circuit. Larger capacitances may be used to increase transient performance.

The type of capacitor used may be ceramic, tantalum or aluminum electrolytic. The low-ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

13.13. Power Supply Input (HV_{DD})

Connect HV_{DD} to the main supply voltage. This voltage should be the same as the motor voltage. The driver overcurrent and overvoltage shutdown features are relative to the HV_{DD} pin. When the HV_{DD} voltage is separate from the motor voltage, the overcurrent and overvoltage protection features may not be available.

The HV_{DD} voltage must not exceed the maximum operating limits of the device. Connect a bulk capacitor close to this pin for good load step performance and transient protection. The actual capacitance should be equal to or larger than the sum of the capacitors attached to the driver supply outputs. The attached capacitors are the V_{REG}, V_{BOOT} and VBx (three bootstrap capacitors) and the charge pump capacitances.

Equation 13-1. HV_{DD} Bulk Capacitor Calculation

$$CHV_{DD} \geq CV_{REG} + CV_{BOOT} + (3 \times CV_{BX}) + C_{CAPx}$$

The type of capacitor used may be ceramic, tantalum or aluminum electrolytic. The low-ESR characteristics of the ceramic will yield lower voltage drop, better noise and PSRR performance at high frequency.

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13.14. Charge Pump Flying Capacitor (CAP1, CAP2)

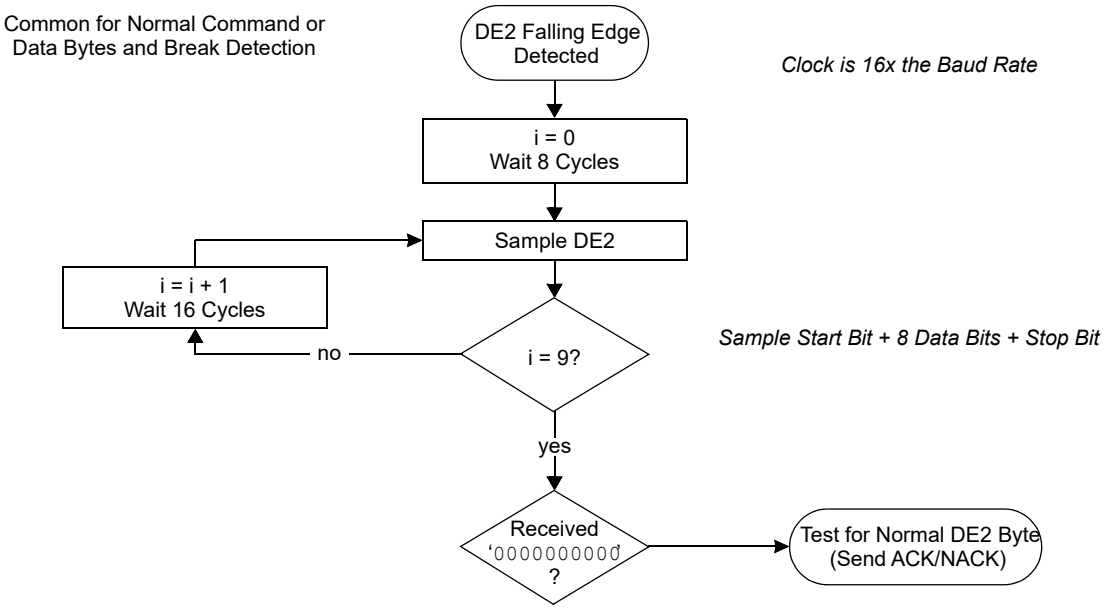
Charge Pump Flying Capacitor connections. Connect the charge pump capacitor across these two pins. The charge pump flying capacitor supplies the power for the V_{BOOT} voltage regulator when the charge pump is active.

A Schottky diode between the CAP1 pin and HV_{SS} is recommended to ensure that the CAP1 pin absolute minimum voltage specification of -0.3V is maintained.

13.15. State Diagram

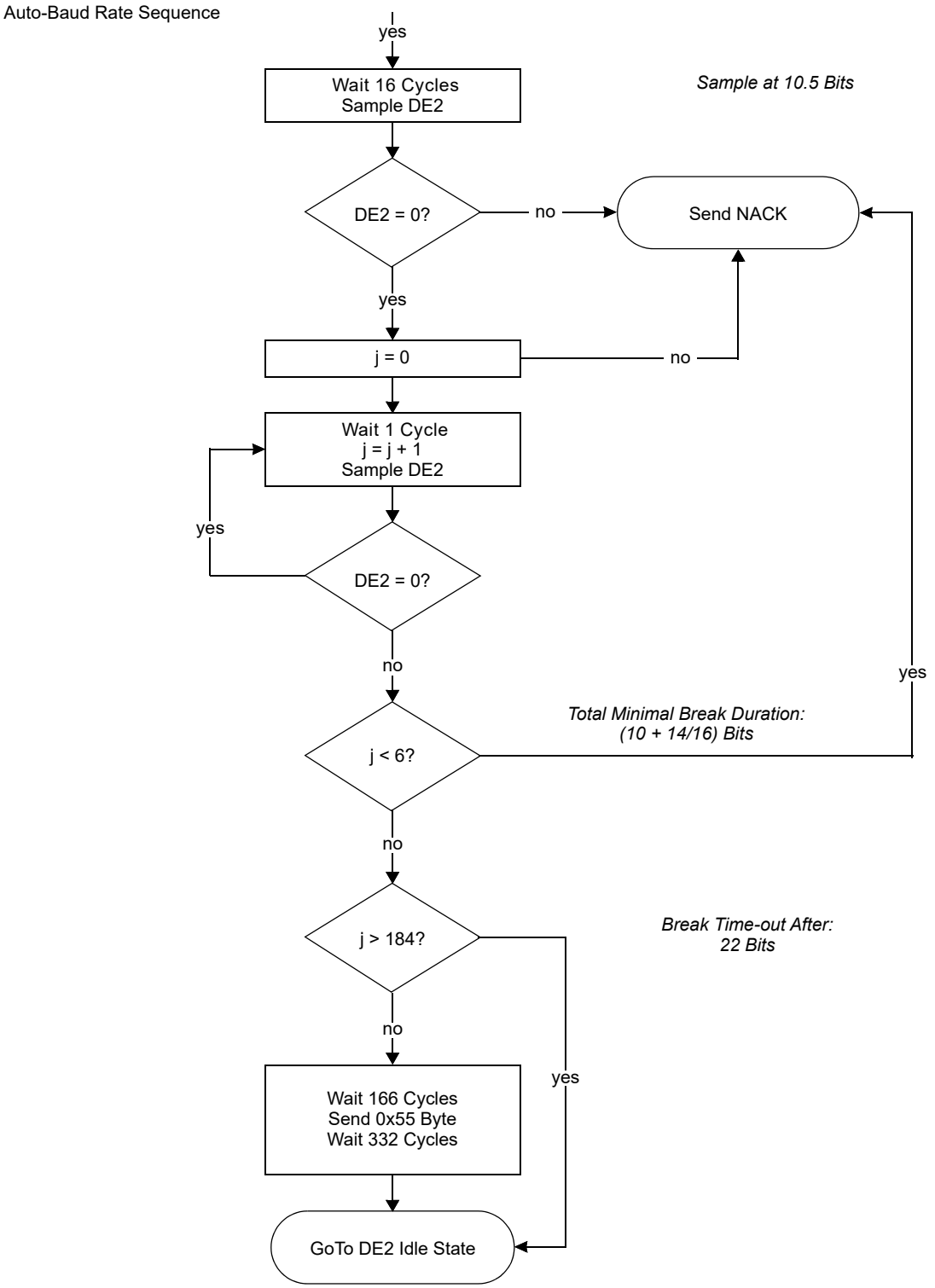
13.15.1. DE2 Receive and Auto-Baud Sequence

Figure 13-3. DE2 Data Reception and Auto-Baud Rate Sequence (Part 1)



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Figure 13-4. DE2 Data Reception and Auto-Baud Rate Sequence (Part 2)



13.16. Bias Generator

The internal bias generator controls several voltage rails. Two fixed output low-dropout linear regulators, internal bias supply LDOs and a charge pump are controlled through the bias generator. In addition, the bias generator performs supervisory functions.

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13.16.1. Charge Pump

An unregulated charge pump is utilized to boost the input to the V_{BOOT} voltage regulator during low input supply voltage conditions. When the HV_{DD} supply voltage drops below the CP_{START} voltage, the charge pump is activated. When activated, 2 x HVDD is presented to the input of the VBOOT regulator. The charge pump is capable of maintaining a VB_{OOT} output of +9V @ 15 mA for a HV_{DD} supply voltage of 5.25V to 7V. The charge pump is capable of maintaining a V_{BOOT} output of +12V @ 20 mA for a supply input voltage of 7V to 13.5V. The charge pump is disabled and bypassed at HV_{DD} voltages above 13.5V, allowing an output voltage of +12V @ 30 mA.

The charge pump requires a capacitor between pins, CAP1 and CAP2. A typical charge pump capacitor should be a 0.1 µF to 1 µF ceramic capacitor.

13.16.2. V_{BOOT} Voltage Regulator

The V_{BOOT} voltage regulator rail is used to supply bias voltage for the integrated 3-phase power MOSFET bridge drivers.

The regulator is capable of supplying 30 mA of external load current. The regulator has a minimum overcurrent limit of 40 mA.

The regulator gets its power from the integrated charge pump. When operating at supply voltages (HV_{DD}) that are above +13.5V, the integrated charge pump will be disabled and the HV_{DD} supply will power the VB_{OOT} voltage regulator. The V_{BOOT} regulator output may be lower than the designed voltage, while operating in the HV_{DD} range of +12.5V to +13.0V, due to the dropout voltage of the regulator.

The V_{BOOT} regulator requires an output capacitor, connected from V_{BOOT} to LIN_VSS, to stabilize the internal control loop and to sustain the bootstrap capacitor energy. A minimum of 4.7 µF ceramic output capacitance is required for the V_{BOOT} voltage regulator output; 10 µF is recommended when switching large MOSFET gate loads. The output capacitor forces a time delay between setting the OE pin high (to transition from Standby mode to Active mode) and the V_{BOOT} regulator voltage output rising above the voltage required to set an internal V_{BOOT} ready flag. The PWM inputs must not be activated while the V_{BOOT} output is charging the output capacitors to the V_{BOOT} ready voltage (typically 6.0V). The time required before allowing the PWM inputs to become active, after setting OE high to transition from Standby mode to Active mode, is dependent on output capacitance, any extra loads and supply voltage ramp-up time. The user should allow a minimum time of 0.94 ms for the V_{BOOT} output voltage to rise above the V_{BOOT} ready voltage. A voltage of 6V and supply current of 30 mA may be used for this delay estimation. See Equation 13-2.

Equation 13-2. OE Pin High to V_{BOOT} Ready

$$dt = (C \times dV)/(I)$$
$$dt = (4.7\ \mu F \times 6V)/(30\ mA)$$
$$dt = 0.94\ ms$$

There is a time-out function that allows the state machine to move from V_{BOOT} to active after 15 ms, regardless of the V_{BOOT} ready voltage. This time-out function prevents the driver from hanging up if the V_{BOOT} voltage is overloaded.

There is also a capacitive voltage divider formed by the three bootstrap capacitors and the V_{BOOT} capacitor. The V_{BOOT} capacitor should be selected so that when the V_{BOOT} supply is active and the bootstrap capacitors are charged, the voltage at the bootstrap capacitors will be greater than the driver undervoltage shutdown voltage, 4.5V. For a system with V_{BOOT} = 12V, VMIN = 4.5V and N = 3 x 1 µF $C_{BOOTSTRAP}$ capacitors charging at the same time, the desired CV_{BOOT} capacitor is 1.8 µF (see Equation 13-3). Since the V_{BOOT} supply requires a 4.7 µF capacitor, a 4.7 µF capacitor should be used. The initial voltage seen by the bootstrap capacitors using a 4.7 µF V_{BOOT} capacitor will be 7.32V. See Equation 13-4.

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Equation 13-3. VBOOT Capacitor

$$CV_{BOOT} = \frac{(N \times C_{BOOTSTRAP})}{(V_{BOOT}) \div (V_{MIN}) - 1}$$

Equation 13-4. Bootstrap Voltage

$$V_{BOOTSTRAP} = \frac{(V_{BOOT} \times CV_{BOOT})}{(CV_{BOOT} + N \times C_{BOOTSTRAP})}$$

The V_{BOOT} output is disabled when the driver transitions to Standby or Sleep mode. Table 13-5 shows the Faults that will also disable the V_{BOOT} voltage regulator.

13.16.3. V_{REG} Low-Dropout (LDO) Linear Regulator

The 3.3V VREG LDO is used for internal gate control logic and can also be used to power the host dsPIC DSC.

The VREG LDO is capable of supplying 70 mA of external load current. The regulator has a minimum overcurrent limit of 80 mA. When the regulator current exceeds the overcurrent limit, the regulator will enter a True Current and Voltage Foldback mode based upon load impedance. As the load impedance decreases towards zero ohms, the regulator output current and voltage will also decrease until the final foldback current and voltage are attained.

When the regulator output voltage drops below the VR_{EG} undervoltage limit, the VREGUVF Undervoltage Fault bit will be set in the STAT1 register. The regulator will remain active during the Fault. Table 13-2 shows the registers and bits associated with Faults.

The V_{REG} LDO will be disabled when the HV_{DD} supply voltage Undervoltage Fault occurs. The V_{REG} LDO will be re-enabled when the conditions in Voltage Supervisor are met.

A minimum of 4.7 µF ceramic output capacitance is required for the V_{REG} LDO; 10 µF is recommended to increase transient performance if supplying the host dsPIC DSC.

The V_{REG} LDO is disabled while the system is in Sleep mode.

13.17. Supervisor

The bias generator incorporates a voltage supervisor and a temperature supervisor.

13.17.1. Voltage Supervisor

The voltage supervisor protects the MOSFET Gate Driver, external power MOSFETs and the host dsPIC DSC from damage due to overvoltage or undervoltage of the input supply, HV_{DD}.

In the event of an undervoltage condition HV_{DD} < UVLOACT, overvoltage condition, HV_{DD} > UVLOACT or V_{REG} LDO undervoltage condition V_{REG} < $VREGUV_{FACT}$, the gate drivers, charge pump and VBOOT regulator are switched off. The bias generator, communication po rt, operational amplifiers and the remainder of the motor control unit remain active. The Failure state is flagged on the FAULT pin, and a DE2 status message is sent.

In extreme overvoltage conditions, HV_{DD} > OVSHDNACT, the V_{REG} LDO will be shut down as soon as pin OE is set to a low level. The OVSHDN status flag in the STAT0 register will be set and will remain set until the register is read by a host. The DE2 communications link will be disabled together with the V_{REG} LDO. No Fault message will be sent to the host because the device must shut down immediately to prevent high-voltage damage. The V_{REG} LDO will be re-enabled when the HV_{DD} supply voltage drops below the Overvoltage Lockout value, OVLOINACT.

In the event of a severe undervoltage condition, HV_{DD} < $UVSHDN_{ACT}$, the entire device will shut down except for the minimal circuitry required for a Power-on Reset recovery. A UVSHDN Fault will be set. The V_{REG} output will be turned off and pulled low to create a “clean” shutdown of an attached

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host processor. The Undervoltage Shutdown condition is a Latched state. The state machine will be restarted from the Power-on Reset state when either of the following two conditions are met:

1. HV_{DD} power is cycled.
2. HV_{DD} rises above UVLOINACT (6.0V).

13.17.2. Temperature Supervisor

An integrated temperature sensor self-protects the device circuitry. If the temperature rises above the overtemperature shutdown threshold, all device functions are turned off except for those required to send a DE2 Fault message. A Fault will be generated and a DE2 Fault message will be sent. The functions required to send the DE2 Fault message will then be shut down if pin OE is set to a low level. Active operation resumes when the temperature has cooled down below a set hysteresis value and the Fault has been cleared by toggling the OE pin from a logic low to a logic high.

It is desirable to signal the host dsPIC DSC with a warning message before the overtemperature threshold is reached. When the Thermal Warning Temperature (T_{WARN}) set point is exceeded, the DE2 temperature warning will be sent to the host dsPIC DSC. The warning message has no effect upon driver operation. The host dsPIC DSC may then take appropriate actions to reduce the temperature rise.

13.18. Output Enable (OE)

The Output Enable (OE) pin allows the device outputs to be disabled by external control. The Output Enable pin has three modes of operation.

13.18.1. Fault Clearing State

The OE pin is used to clear any Faults and re-enable the driver. After toggling the OE pin low-to-high, the system requires a minimum time period to re-enable and start up all of the driver blocks. The start-up time is approximately 35 µs. The maximum pulse time for the high-low-high transition to clear the Faults should be less than 900 µs to prevent the system from transitioning through Standby mode. If the high-low-high transition is longer than 1 ms, the device will start up from the Standby state.

Any Fault status bits that are set will be cleared by the low-to-high transition of the OE pin, if and only if, the Fault condition has ceased to exist. If the Fault condition still exists, the active Fault status bit will remain active. No additional Fault messages will be sent for a Fault that remains active.

13.18.2. Standby State

Standby state is entered when the OE pin goes low for longer than 1 ms and the SLEEP Configuration bit is inactive. When Standby mode is entered, the following subsystems are disabled:

- High-side gate drives (HSA, HSB, HSC) forced low
- Low-side gate drives (LSA, LSB, LSC) forced low
- V_{BOOT} LDO
- Charge pump
- Operational amplifiers if CFG0[6] = 1
- The V_{REG} LDO and DE2 communications stay active.

13.18.3. Sleep Mode

Sleep mode is entered when both a `SLEEP` command is sent to the device via DE2 communications and the OE pin is low. The SLEEP bit in the CFG0 Configuration register indicates when the device should transition to a low-power mode. The device will operate normally until the OE pin is transitioned low by an external device. At that point in time, the SLEEP bit value determines whether the device transitions to Standby mode or low-power Sleep mode. The Supply Current (I_{SUP}) during

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Sleep mode will typically be 5 µA. When Sleep mode is activated, most functions will be shut off, including the V_{REG} LDO. Only the Power-on Reset monitor and minimal state machine will remain active to detect a wake-up event. This indicates that the host processor will be shut down if the host is using the V_{REG} LDO regulator for power. The device will stay in the low-power Sleep mode until either of the following conditions is met:

- The WAKE pin receives a signal corresponding with t_{WAKE_SETUP}. Table 13-1 specifies the signal conditions based on the device revision.
- Power is cycled.

The MOSFET Gate Driver is not required to retain configuration data while in Sleep mode. When exiting Sleep mode, the host should send a new configuration message to configure the device if the default configuration values are not desired. The same configuration sequence used during power-up may be used when exiting Sleep mode.

When activated, Sleep mode will always be entered regardless of any active Fault. This allows a transition to Sleep mode when the host is powered by the V_{REG} LDO and the regulator is in an unreliable state. The SLEEP bit in the Configuration register will be ignored at power-up until the system has enabled the V_{REG} LDO and the V_{REG} LDO has entered regulation.

13.19. Faults

13.19.1. Fault Pin Output ($\overline{FAULT}$)

The $\overline{FAULT}$ pin is used as a Fault indicator. The pin is capable of sinking a minimum of 1 mA of current while maintaining less than 50 mV of voltage across the output. An external pull-up resistor to the logic supply is required.

The open-drain $\overline{FAULT}$ pin transitions low when a Fault occurs. Table 13-2 lists the Faults that activate the $\overline{FAULT}$ signal. Warnings do not activate the $\overline{FAULT}$ signal; Table 13-3 lists the warnings.

13.19.2. Fault Handling Sequence

When a Fault occurs, the following steps will occur in sequence.

1. The gate drive outputs will be immediately turned off.
2. The $\overline{FAULT}$ pin output will go low.
3. A message will be sent via the DE2 communications link if, and only if, the Fault is not a HV_{DD} Overvoltage Shutdown ($OVSHDN_{ACT}$).
4. The V_{REG} LDO will be disabled immediately if the Fault is a HV_{DD} Overvoltage Shutdown ($OVSHDN_{ACT}$) or a HV_{DD} Undervoltage Shutdown ($UVSHDN_{ACT}$) Fault.
5. The V_{REG} LDO will be disabled 5 ms after the DE2 message has been sent for an Overtemperature Shutdown (OTSHDN) Fault.

13.19.3. Fault Indicator

A “FAULT” indicator bit resides in the STAT0 register. The bit is the logical ‘OR’ of all of the Fault bits in the two Status registers. Warnings are not included in the FAULT indicator bit.

The FAULT bit will allow the user to read the STAT0 register in order to determine if a Fault is present in the system. If the bit is set, then the user may request the STAT1 message and interrogate the bits of both status messages to determine what Faults exist.

The Faults that are logically OR’d together to generate the FAULT bit are as follows:

- STAT0:OTPF
- STAT0:UVLOF
- STAT0:OVLOF

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- STAT1:REGUVF
- STAT1:XUVLOF
- STAT1:XOCPF

Table 13-2. Faults

Fault	DE2 Message
Fault Active ('OR' of all Faults)	0x85 0x01
Overtemperature	0x85 0x04
HVDD Input Undervoltage	0x85 0x08
HVDD Input Overvoltage	0x85 0x10
VREG Output Undervoltage	0x86 0x01
External MOSFET Undervoltage Lockout	0x86 0x04
External MOSFET Overcurrent Detection	0x86 0x08

Table 13-3. Warnings

Fault	DE2 Message
Temperature Warning	0x85 0x02

13.19.4. Power Control Status (PCON)

The PCON[2:0] (STAT0[7:5]) bits are Power Control status bits that may be used to determine the cause of a shutdown. They are not Fault latches. The HV_{DD} Overvoltage Shutdown Fault is an internally latched Fault that does not have a latched FAULT bit in the STAT0 or STAT1 register. That is because the device will be shut down immediately upon entering the Overvoltage Fault condition. When power is back within the device operating range, and the V_{REG} supply is re-enabled, the Host will be able to read the STAT0 register to determine the reason for a power cycle. The PCON power status bits will contain the cause of the power cycle. Table 13-4 lists the Power Status register bits in the STAT0 register.

Table 13-4. Power Status

PCON[2:0] Status Bits (STAT0[7:5])	DE2 Message
Overtemperature Shutdown (OTSHDN) occurred	0x85 0xA0
HVDD Overvoltage Shutdown (OVSHDN) occurred	0x85 0x80
Sleep occurred	0x85 0x60
HVDD Undervoltage Shutdown (UVSHDN) occurred	0x85 0x40
Power-on Reset (POR) occurred	0x85 0x20
Normal operation	0x85 0x00

13.19.4.1. Internal Function Block Status

Table 13-5 shows the effects of the OE pin, Faults and the SLEEP bit upon the functional status of the internal blocks of the dsPIC33CDVL256MC506 family.

13.19.4.2. Start-up/$\overline{\text{FAULT}}$ Pin State

During device start-up or Power-on Reset (POR), the $\overline{\text{FAULT}}$ pin will stay active (low) to indicate to the host that the device is initializing. The $\overline{\text{FAULT}}$ pin will stay active until the state machine powers up the V_{REG} LDO and completes the V_{REG} state. After the V_{REG} LDO is powered up, the $\overline{\text{FAULT}}$ pin logic checks the state of all of the latched FAULT bits. If any FAULT bit is still active, the $\overline{\text{FAULT}}$ pin will stay active and remain low.

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Table 13-5. Internal Function Block Status

System State	Fault	Conditions	Sleep Latch	V_{REG} LDO	V_{BOOT} LDO	Motor Drivers	DE2	Op Amps	Internal UVLO, OVLO, OTP
Sleep		OE = 0, SLEEP = 1	W	—	—	—	—	—	—
Standby		OE = 0, SLEEP = 0	—	A	—	—	A	C	A
Operating		OE = 1, FAULT = 1	—	A	A	A	A	A	A
Faults $\overline{FAULT}$ = 0	Driver OTPF	TJ Temperature > +160°C	—	—	—	—	D	—	A
	HV_{DD}UVLO	$HV_{DD} \le UVLO_{INACT}$	—	A	—	—	A	A	A
	HV_{DD}UVSHDN	$HV_{DD} \le UVSHDN_{INACT}$	—	—	—	—	E	—	—
	HV_{DD}OVLO	$HV_{DD} \ge OVLO_{INACT}$	—	A	—	—	A	A	A
	V_{DD}OVSHDN	HVdd ≥ $OVSHDN_{INACT}$	—	—	—	—	—	—	A
	V_{REG} LDO UVF	$V_{REG} \le 88\% V_{REG}$	—	A	—	—	A	A	A
	MOSFET UVLO	$V_{HS[A:C]} < V_{DUVLO}$ $V_{LS[A:C]} < V_{DUVLO}$	—	A	A	—	A	A	A
	MOSFET OCPF	$V_{DRAIN\ SOURCE}$ > EXTOC[1:0] setting	—	A	A	—	A	A	A
Warnings FAULT = 1	Driver Temperature	TJ Temperature > 72% T_{SD_MIN} (+115°C for +160°C driver OTP)	—	A	A	A	A	A	A
Power Status	Configuration lost if Power-on Reset, wake from Sleep or recover from HVDD Undervoltage Shutdown occurred	Set at initial power-up when HV_{DD} < $UVSHDN_{ACT}$ or when waking from Sleep	—	A	A	A	A	A	A

Legend: — = Inactive (Off); A = Active (On); C = Configurable; D = Inactive (Off) 5 ms after sent Fault message; E = Inactive (Off); R = Receiver Only; W = Wake-up (from Sleep); OCPF = Overcurrent Protection; OTPF = Overtemperature Protection; UVLO = Undervoltage Lockout; OVLO = Overvoltage Lockout; UVF = Undervoltage Fault; UVSHDN = Undervoltage Shutdown; OVSHDN = Overvoltage Shutdown

13.20. Motor Control Unit

The motor control unit is comprised of the following:

- External Drive for a 3-Phase Bridge with NMOS/NMOS MOSFET Pairs
- MOSFET Driver Undervoltage Lockout
- External MOSFET Short-Circuit Current
- $\overline{FAULT}$ Pin Output
- Cross Conduction Protection
- Programmable Dead Time
- Programmable Blanking Time

13.20.1. External Drive for A 3-Phase Bridge with NMOS/NMOS MOSFET Pairs

Each motor phase is driven with external NMOS/NMOS MOSFET pairs. These are controlled by a low-side and a high- side gate driver. The gate drivers are controlled by the host dsPIC PWM

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interconnects. A logic high turns the associated gate driver on, and a logic low turns the associated gate driver off.

The low-side gate drivers are biased by the V_{BOOT} regulator output, referenced to ground. The high-side gate drivers are a floating drive biased by a bootstrap capacitor circuit. The bootstrap capacitor is charged by the V_{BOOT} regulator whenever the accompanying low-side MOSFET is turned on.

The high-side and low-side driver outputs all go to a Low state whenever there is a Fault, when OE = `0` for more than 1 ms or when Sleep mode is active, regardless of the PWM[A:C]H/L inputs.

13.20.2. MOSFET Gate Driver Undervoltage Lockout (UVLO)

The MOSFET Gate Driver Undervoltage Lockout Fault detection monitors the available voltage used to drive the external MOSFET gates. The Fault detection is only active while the driver is actively driving the external MOSFET gate. Any time the driver bias voltage is below the gate drive Undervoltage Lockout Threshold (V_{DUVLO}) for a time longer than specified by the t_{DUVLO} parameter, the driver will not turn on when commanded on. A driver Fault will be indicated to the host dsPIC DSC on the $\overline{FAULT}$ open-drain output pin and also via a DE2 communications `Status_1` message. This is a latched Fault. Clearing the Fault requires either removal of device power or disabling and re-enabling the device via the device Output Enable (OE) input. The EXTUVLO bit in the CFG0 register is used to enable or disable the driver Undervoltage Lockout feature. This protection feature prevents the external MOSFETs from being controlled with a gate voltage not suitable to fully enhance the device.

13.20.3. External MOSFET Short-Circuit Current

Short-circuit protection monitors the voltage across the external MOSFETs during an On condition. The high-side driver voltage is measured from HV_{DD} to PH[A:C]. The low-side driver voltage is measured from PH[A:C] to ground. If a monitored voltage rises above a user-configurable threshold after the driver HS[A:C] or LS[A:C] output voltage has been driven high, all drivers will be turned off. A driver Fault will be indicated to the host dsPIC DSC on the open-drain $\overline{FAULT}$ output pin and also via a DE2 communications `Status_1` message. This is a latched Fault. Clearing the Fault requires either removal of device power or toggling the OE input pin low-to-high. This protection feature helps detect internal motor failures, such as winding to case shorts.

Note: The driver short-circuit protection is dependent on application parameters. A configuration message is provided for a set number of threshold levels. The MOSFET Gate Driver UVLO and short-circuit protection features have the option to be disabled.

The short-circuit voltage may be set via a DE2 `Set_Cfg_0` message. The EXTOC[1:0] bits of the CFG0 register are used to select the voltage level for the short-circuit comparison. If a monitored voltage differential between HV_{DD} and PH[A:C], or between PH[A:C] and PGND, exceeds the selected voltage level when the MOSFET Gate Driver is active, a Fault will be triggered. The selectable voltage levels are 250 mV, 500 mV, 750 mV and 1000 mV. The EXTSC bit of the CFG0 register is used to enable or disable the MOSFET Gate Driver short-circuit detection.

13.20.4. Gate Control Logic

The gate control logic enables level shifting of the digital inputs, polarity control and cross conduction protection.

13.20.4.1. Cross Conduction Protection

If both MOSFETs in the same half-bridge are commanded on by the digital PWM inputs, both will be turned off.

13.20.4.2. Programmable Dead Time

The gate control logic employs a break-before-make dead-time delay that is programmable. A configuration message is provided to configure the driver dead time. The programmable dead times range from 250 ns to 2000 ns (default) in 250 ns increments. The dead time allows the PWM inputs

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to be direct inversions of each other and still allow proper motor operation. The dead time internally modifies the PWMH/L gate drive timing to prevent cross conduction. The DRVDT[2:0] bits of the CFG2 register are used to set the dead-time value.

13.20.4.3. Programmable Blanking Time

A configuration message is provided to configure the driver current limit blanking time. The blanking time allows the driver to ignore any current spikes that may occur when switching the driver outputs. The allowable blanking times are 500 ns, 1 µs, 2 µs and 4 µs (default). The blanking time will start after the dead-time circuitry has timed out. The DRVBL[1:0] bits of the CFG2 register are used to set the blanking time value.

The blanking time also affects the driver undervoltage lockout. The driver undervoltage lockout latches the external MOSFET undervoltage lockout Fault if the undervoltage condition lasts longer than the time specified by the t_{DUVLO} parameter. The t_{DUVLO} parameter takes into account the blanking time if blanking is in progress.

13.21. Motor Control

The commutation loop of a BLDC motor control is a Phase-Locked Loop (PLL), which locks to the rotor's position. Note that this inner loop does not attempt to modify the position of the rotor, but modifies the commutation times to match whatever position the rotor has. An outer speed loop changes the rotor velocity, and the commutation loop locks to the rotor's position to commutate the phases at the correct times.

13.21.1. Six-Step Sensorless Motor Control

Many control algorithms can be implemented using the dsPIC33CDVL256MC506 devices with the internal MOSFET Gate Driver.

The following information provides a starting point for implementing a 3-phase sensorless motor control application. The motor is driven by energizing two windings at a time and sequencing the windings in a six-step per electrical revolution method. This method leaves one winding unenergized at all times. The voltage (Back EMF or BEMF) on that unenergized winding can be monitored to determine the rotor position.

13.21.1.1. Start-up Sequence

When the motor being driven is at rest, the BEMF voltage is equal to zero. The motor needs to be rotating for the BEMF sensor to lock onto the rotor position and commutate the motor. The recommended start-up sequence is to bring the rotor from rest, up to a speed fast enough to allow BEMF sensing. Motor operation is comprised of five modes: Disabled mode, Bootstrap mode, Lock or Align mode, Ramp mode and Run mode. Refer to the commutation state machine in Table 13-6. The order in which the host dsPIC DSC steps through the commutation state machine determines the direction that the motor rotates.

13.21.1.2. Disabled Mode (OE = 0)

When the driver output is disabled (OE = 0), all of the MOSFET driver outputs are set low.

13.21.1.3. Bootstrap Mode

The high-side driver obtains the high-side biasing voltage from the V_{BOOT} LDO, bootstrap diode and bootstrap capacitor. The bootstrap capacitors must first be charged before the high-side drives may be used. The bootstrap capacitors are all charged by activating all three low-side drivers. The active low-side drivers pull their respective phase nodes low, charging the bootstrap capacitors to the V_{BOOT} LDO voltage. The three low-side drivers should be active for at least 1.2 ms per 1 µF of bootstrap capacitance. This assumes a 12V voltage change and 30 mA (10 mA per phase) of current coming from the V_{BOOT} LDO.

13.21.1.4. Lock Mode

Before the motor can be started, the rotor should be in a known position. In Lock mode, the host dsPIC DSC drives Phase B low and Phases A and C high. This aligns the rotor 30 electrical degrees

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before the center of the first Commutation state. Lock mode must last long enough to allow the motor and its load to settle into this position.

13.21.1.5. Ramp Mode

At the end of Lock mode, Ramp mode is entered. In Ramp mode, the host dsPIC DSC steps through the commutation state machine, increasing the step rate linearly, until a minimum speed is reached that will result in a usable BEMF voltage. Ramp mode is an open-loop commutation. No knowledge of the rotor position is used.

13.21.1.6. Run Mode

At the end of Ramp mode, Run mode is entered. In Run mode, the Back EMF sensor is enabled and commutation is now under the control of the phase-locked loop. Motor speed can be regulated by an outer speed control loop.

Table 13-6. COMMUTATION STATE MACHINE

State	Outputs						BEMF Phase
	HSA	HSB	HSC	LSA	LSB	LSC	
OE = 0	OFF	OFF	OFF	OFF	OFF	OFF	N/A
BOOTSTRAP	OFF	OFF	OFF	ON	ON	ON	N/A
LOCK	ON	OFF	ON	OFF	ON	OFF	N/A
1	ON	OFF	OFF	OFF	OFF	ON	Phase B
2	OFF	ON	OFF	OFF	OFF	ON	Phase A
3	OFF	ON	OFF	ON	OFF	OFF	Phase C
4	OFF	OFF	ON	ON	OFF	OFF	Phase B
5	OFF	OFF	ON	OFF	ON	OFF	Phase A
6	ON	OFF	OFF	OFF	ON	OFF	Phase C

13.21.1.7. PWM Speed Control

The inner commutation loop is a phase-locked loop, which locks to the rotor's position. This inner loop does not attempt to modify the position of the rotor but modifies the commutation times to match whatever position the rotor has. The outer speed loop changes the rotor velocity, and the inner commutation loop locks to the rotor's position to commutate the phase at the correct times.

The outer speed loop pulse width modulates the motor drive inverter to produce the desired wave shape and voltage at the motor. The inductance of the motor then integrates this PWM pattern to produce the desired average current, thus controlling the desired torque and speed of the motor. For a trapezoidal BLDC motor drive with six-step commutation, the PWM is used to generate the average voltage to produce the desired motor current and motor speed.

There are two basic methods to PWM the inverter switches. The first method returns the reactive energy in the motor inductance to the source by reversing the voltage on the motor winding during the current decay period. This method is referred to as fast decay or chop-chop. The second method circulates the reactive current in the motor with minimal voltage applied to the inductance. This method is referred to as slow decay or chop-coast.

The preferred control method employs a chop-chop PWM for any situations where the motor is being accelerated, either positively or negatively. For improved efficiency, chop-coast PWM is employed during steady-state conditions. The chop-chop speed loop is implemented by hysteretic control, fixed off time control or Average Current mode control of the motor current. This makes for a very robust controller, since the motor current is always in instantaneous control. The motor speed presented to the chop-chop loop is reduced by approximately 9%. A fixed frequency PWM that only modulates the high-side switches implements the chop-coast loop. The chop-coast loop is presented with the full motor speed, so if it is able to control the speed, the chop-chop loop will never be satisfied and will remain saturated. The chop-chop remains able to assume full control if

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the motor torque is exceeded, either through a load change or a change in speed that produces acceleration torque. The chop-coast loop will remain saturated, with the chop-chop loop in full control, during start-up and acceleration to full speed. The bandwidth of the chop-coast loop is set to be slower than the chop-chop loop so that any transients will be handled by the chop-chop loop and the chop-coast loop will only be active in a steady-state operation.

13.22. DE2 Communication Port

A half-duplex 9600 baud UART interface is available to communicate with the host dsPIC DSC. The port is used to configure the MOSFET Gate Driver and also for status and Fault messages.

13.22.1. Communications Interface

A half-duplex, 9600 baud, 8-bit bidirectional communications interface is implemented on the DE2 interconnect. The interface consists of eight data bits, one Stop bit and one Start bit.

Dedicated UART hardware may be configured through PPS to transmit and receive messages over the DE2 communications interconnect.

The MOSFET Gate Driver side of the interface is an open-drain configuration and requires that the host dsPIC DSC uses an internal pull-up resistor to pull the DE2 interconnect high.

It is also recommended that the user enable open-drain (ODCx = 1) on the DE2 pin on the dsPIC side to allow for utilization of the pull-up, though it is not necessary if the line is properly configured for half-duplex communication.

The auto-baud frequency is temperature-dependent, as illustrated in Figure 13-4 . To establish proper DE2 communication, it is recommended to synchronize the host frequency by proceeding the auto-baud function alternatively, as described in Auto-Baud Function. The time from receiving the last bit of a command message to sending the first bit of the response message ranges from t_{DE2_RSP} to t_{DE2_WAIT}, corresponding to 0 µs to 3.125 ms. The host should refrain from sending additional messages until the previously requested message has been received in order to prevent overwriting the driver response message.

All DE2 interconnect pin configuration requirements are described in Communications Port (DE2 Interconnect) and provided in Auto-Baud Code Example.

13.22.2. Packet Format

Every internal driver status change will cause the driver to send a message to the host dsPIC DSC. The interface uses a standard UART baud rate of 9600 bits per second.

In the DE2 protocol, the transmitter and the receiver do not share a clock signal. A clock signal does not emanate from one transmitter to the other receiver. Due to this reason, the protocol is asynchronous. The protocol uses only one line to communicate, so the transmit/receive packet must be done in Half-Duplex mode. A new transmit message is allowed only when a complete packet has been transmitted and responded to.

The host must listen to the DE2 line in order to check for contentions. In case of contention, the host must release the line and wait for at least three packet length times before initiating a new transfer.

Figure 13-5 illustrates a basic DE2 data packet.

13.22.3. Packet Timing

While no data are being transmitted, a logic '1' must be placed on the open-drain DE2 line by the host dsPIC DSC using an internal pull-up resistor. A data packet is composed of one Start bit, which is always a logic '0', followed by eight data bits and a Stop bit. The Stop bit must always be a logic '1'. It takes 10 bits to transmit a byte of data.

The DE2 interface detects the Start bit by detecting the transition from logic '1' to logic '0' (note that while the data line is Idle, the logic level is high). Once the Start bit is detected, the next data bit's

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center can be assured to be 24 ticks minus 2 (worst-case synchronizer uncertainty) later. From then on, every next data bit center is 16 clock ticks later. Figure 13-6 illustrates basic packet timing.

13.22.4. Message Handling

The driver will not transition to Sleep mode while a message is being received. If a message reception is in progress before the OE = 0 to Sleep Mode Transition (t_{SLEEP}) delay times out, the message will be fully received and the contents applied to the Configuration registers, if applicable. The SLEEP bit will then be checked and the system enters Sleep mode if the SLEEP bit is still active.

13.22.5. Auto-Baud Function

The MOSFET Gate Driver provides an auto-baud feature that allows the host dsPIC DSC, communicating on the DE2 communications interconnect, to determine the actual baud rate being used by the MOSFET Gate Driver. The feature allows the host to request a 0x55 byte transmission from the MOSFET Gate Driver. The host then determines the MOSFET Gate Driver baud rate and adjusts the host internal Baud Rate Generator (BRG) to match the MOSFET Gate Driver baud rate.

The DE2 pin is used to trigger the auto-baud feature. The host sets the DE2 signal to a logic low for a period of time (auto-baud Break window) that ranges between 1.29 ms and 2.0 ms. The host then releases the DE2 pin back to the host UART control. The host UART then raises the DE2 pin to a logic high value. The MOSFET Gate Driver will respond with a standard NACK ('0b00nnnnnn', where 'nnnnnn' are the six Least Significant bits (LSbs) received) if the DE2 link was held low for less than 1.29 ms and the byte was not interpreted as a valid command. The MOSFET Gate Driver will ignore the current message if the DE2 link is held low for more than 2.0 ms.

If the driver receives a valid auto-baud request in the allotted time frame, the driver will enter an Auto-Baud state, indicating an auto-baud message has been requested. When the auto-baud function is activated, the DE2 subsystem will disable sending all unsolicited messages to the host.

If the internal Auto-Baud state is set, the driver will wait for a minimum of 0.86 ms and a maximum of 1.19 ms. After the wait time has expired, a 0x55 data byte will be immediately sent on the DE2 link by the driver.

The driver will wait 2.00 ms after sending the 0x55 baud rate data over the DE2 link before transmitting any other messages. The driver will then exit the Auto-Baud state and resume normal DE2 operations. The 2.00 ms wait is needed to allow the host to complete the auto-baud verification and update the host UART Baud Rate Generator.

The MOSFET Gate Driver will always monitor the DE2 link for a logic low before attempting to transmit.

The MOSFET Gate Driver will preempt all DE2 communications upon receiving a logic low on the DE2 link which lasts longer than ten bit times at 9600 baud (Break sequence).

The MOSFET Gate Driver will wait for a period up to 2 ms for the DE2 link to change to a Logic High state after the initial detection of a logic low on the DE2 link. If the DE2 link fails to rise to a logic high level within 2 ms of the initial logic low level, the auto-baud message will be canceled and no message will be sent. The auto-baud function will then be complete.

The driver will send any pending unsolicited messages after the auto-baud function has finished.

13.22.6. Messaging Interface

A command byte will always have the Most Significant bit (MSb) 7 set to '1'. Bits 6 and 5 are reserved for future use and should be set to '0'. Bits[4:0] are used for commands; that allow for 32 possible commands.

13.22.6.1. Host dsPIC DSC to MOSFET Gate Driver

Messages sent from the host dsPIC DSC to the MOSFET Gate Driver consist of either one or two 8-bit bytes. The first byte transmitted is the command byte. The second byte transmitted, if required, is the data for the command.

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If a multibyte command is sent to the MOSFET Gate Driver and no second byte is received by the MOSFET Gate Driver, then a "Command Not Acknowledged" message will be sent back to the host afterwards. The host must start sending the 2nd byte of a two-byte command within 1 ms of completion of the first byte to prevent a NACK message. Once the second byte Start bit is received, the MOSFET Gate Driver internal receiver logic will handle the reception of the data byte. If the data byte Stop bit is not received within the expected reception time for the last received bit, the driver will respond with a NACK message.

13.22.6.2. MOSFET Gate Driver to Host dsPIC DSC

A solicited response byte from the MOSFET Gate Driver will always echo the command byte with bit 7 set to '0' (response) and with bit 6 set to '1' for Acknowledged (ACK) or '0' for Not Acknowledged (NACK). The second byte, if required, will be the data for the host command. Any command that causes an error or is not supported will receive a NACK response.

The MOSFET Gate Driver may send unsolicited command messages to the host dsPIC DSC. All messages to the host controller do not require a response from the host controller.

13.22.7. Messages

13.22.7.1. SET_CFG_0

There is a SET_CFG_0 message that is sent by the host dsPIC DSC to the MOSFET Gate Driver to configure the driver. The SET_CFG_0 message may be sent to the driver at any time. The host is responsible for making sure the system is in a state that will not be compromised by sending the SET_CFG_0 message. The SET_CFG_0 message format is indicated in Table 13-7 . The response is indicated in Table 13-8 .

13.22.7.2. GET_CFG_0

There is a GET_CFG_0 message that is sent by the host dsPIC DSC to the dsPIC33CDVL256MC506 device to retrieve the device Configuration register. The GET_CFG_0 message format is indicated in Table 13-7 . The response is indicated in Table 13-8.

13.22.7.3. STATUS_0 and STATUS_1

There are STATUS_0 and STATUS_1 messages that are sent by the host dsPIC DSC to the MOSFET Gate Driver to retrieve the device STAT0 and STAT1 registers. Unsolicited STATUS_0 and STATUS_1messages may also be sent to the host by the MOSFET Gate Driver to inform the host of status changes. The unsolicited STATUS_0 and STATUS_1 messages will only be sent when a status bit changes to an Active state. The STATUS_0 and STATUS_1 message format is indicated in Table 13-7. The response is indicated in Table 13-8.

When a STATUS_0 or STATUS_1 message is sent to the host dsPIC DSC in response to a new Fault becoming active, the FAULT bit will be cleared, either by the host issuing a STATUS_0 or STATUS_1 request message, or by the host toggling the OE pin low then high. The FAULT bit will stay active and not be cleared if the Fault condition still exists at the time the host attempted to clear the Fault.

The PCONx bits of the STAT0 register will be set every time the device restarts due to various events (see Table 13-4). When the driver resumes operation, a single unsolicited STATUS_0 message will be sent to the host dsPIC DSC indicating a Reset has occurred. The message will be sent five milliseconds (5 ms) after the V_{REG} LDO has reached its Active state. The host should check the PCONx bits to determine the cause of the power cycle. In all cases, the configuration data may have been and should be resent to the driver. The PCONx flags are reset by a host STATUS_0 request message. If the host misses the unsolicited STATUS_0 message at start-up, the host may manually request the status by sending a STATUS_0 message to the driver. The PCONx bits of the STAT0 register will contain the source of the Power-on Reset until the STAT0 register is requested by the host.

13.22.7.4. SET_CFG_2

There is a SET_CFG_2 message that is sent by the host dsPIC DSC to the MOSFET Gate Driver to configure the driver current limit blanking time. The SET_CFG_2 message may be sent to the

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devices at any time. The host is responsible for making sure the system is in a state that will not be compromised by sending the SET_CFG_2 message. The SET_CFG_2 message format is indicated in Table 13-7. The response is indicated in Table 13-8.

13.22.7.5. GET_CFG_2

There is a GET_CFG_2 message that is sent by the Host dsPIC DSC to the MOSFET Gate Driver to retrieve the device Configuration Register #2. The GET_CFG_2 message format is indicated in Table 13-7 . The response is indicated in Table 13-8.

Figure 13-5. DE2 Packet Format

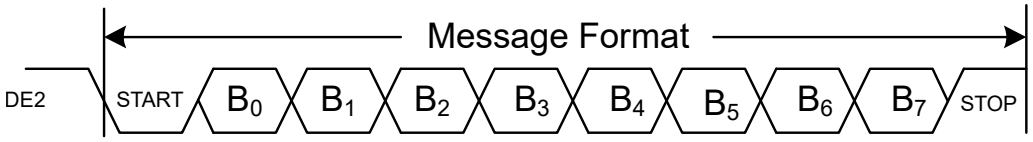


Figure 13-6. DE2 Packet Timing

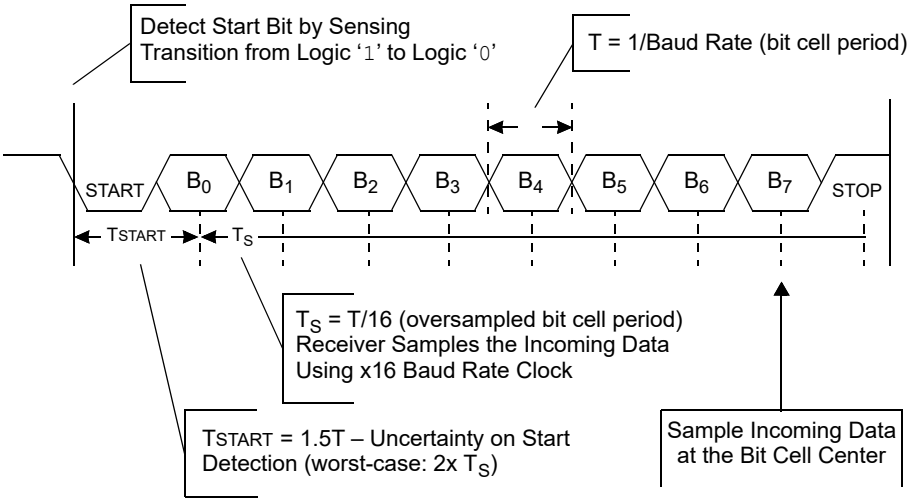


Table 13-7. DE2 Communication Commands from Host to dsPIC33CDVL256MC506

Command	Byte	Bit	Value	Description
SET_CFG_0	1		10000001 (81h)	Set Configuration Register 0

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Table 13-7. DE2 Communication Commands from Host to dsPIC33CDVL256MC506 (continued)

Command	Byte	Bit	Value	Description
	2	7	0	Reserved
		6	0	Reserved
SET_CFG_0		5	0	System enters Standby mode when OE = 0, SLEEP = 0 for more than 1 ms.
			1	System enters Sleep mode when OE = 0, SLEEP = 1 for more than 1 ms.
		4	0	Reserved
		3	0	Enable external MOSFET Undervoltage Lockout (default).
			1	Disable external MOSFET Undervoltage Lockout.
		2	0	Enable external MOSFET short-circuit detection (default).
			1	Disable external MOSFET short-circuit detection.
		1:0	00	Set external MOSFET overcurrent limit to 0.250V (default).
			01	Set external MOSFET overcurrent limit to 0.500V.
			10	Set external MOSFET overcurrent limit to 0.750V.
			11	Set external MOSFET overcurrent limit to 1.000V.
GET_CFG_0	1		10000010 (82h)	Get Configuration Register 0.
STATUS_0	1		10000101 (85h)	Get Status Register 0.
STATUS_1	1		10000110 (86h)	Get Status Register 1.

Table 13-8. DE2 Communication Messages from dsPIC33CDVL256MC506 to Host

Command	Byte	Bit	Value	Description
SET_CFG_2	1		10000111 (87h)	Set Configuration Register 2.
	2	7:5	00h	Reserved
		4:2	—	Driver dead time (for PWMH /PWML inputs)
			000	2000 ns (default)
			001	1750 ns
			010	1500 ns
			011	1250 ns
			100	1000 ns
			101	750 ns
			110	500 ns
			111	250 ns
		1:0	—	Driver blanking time (ignore switching current spikes)
			00	4 µs (default)
			01	2 µs
			10	1 µs
			11	500 ns
GET_CFG_2	1		10001000 (88h)	Get Configuration Register 2.
GET_REV_ID	1		10010000 (90h)	Get device hardware revision.

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Table 13-8. DE2 Communication Messages from dsPIC33CDVL256MC506 to Host (continued)

Command	Byte	Bit	Value	Description
SET_CFG_0	1	7:0	00000001 (01h)	Command not Acknowledged (response).
			01000001 (41h)	Command Acknowledged (response).
	2	7	0	Reserved
		6	0	Reserved
		5	0	System enters Standby mode when OE = 0, SLEEP = 0 for more than 1 ms.
			1	System enters Sleep mode when OE = 0, SLEEP = 1 for more than 1 ms.
		4	0	Reserved
		3	0	External MOSFET Undervoltage Lockout enabled (default).
			1	External MOSFET Undervoltage Lockout disabled.
		2	0	External MOSFET short-circuit detection enabled (default).
			1	External MOSFET short-circuit detection disabled.
		1:0	00	0.250V external MOSFET overcurrent limit (default)
			01	0.500V external MOSFET overcurrent limit
			10	0.750V external MOSFET overcurrent limit
			11	1.000V external MOSFET overcurrent limit
GET_CFG_0	1	7:0	00000010 (02h)	Command not Acknowledged (response).
			01000010 (42h)	Command Acknowledged (response).
	2	7	0	Reserved
		6	0	Reserved
		5	0	System enters Standby mode when OE = 0, SLEEP = 0 for more than 1 ms.
			1	System enters Sleep mode when OE = 0, SLEEP = 1 for more than 1 ms.
		4	0	Reserved
		3	0	External MOSFET Undervoltage Lockout enabled.
			1	External MOSFET Undervoltage Lockout disabled.
		2	0	External MOSFET short-circuit detection enabled.
			1	External MOSFET short-circuit detection disabled
		1:0	00	0.250V external MOSFET overcurrent limit
			01	0.500V external MOSFET overcurrent limit
			10	0.750V external MOSFET overcurrent limit
			11	1.000V external MOSFET overcurrent limit

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STATUS_0	1	7:0	00000101 (05h)	Command not Acknowledged (response).
			01000101 (45h)	Command Acknowledged (response).
			10000101 (85h)	Command sent to host (unsolicited).
	2	7:5	101	Overtemperature Shutdown (OTSHDN) occurred.
			100	Overvoltage Shutdown (OVSHDN) occurred.
			011	Sleep Shutdown (SLEEP) occurred.
			010	Undervoltage Shutdown (UVSHDN) occurred.
			001	Power-on Reset (POR) occurred.
			000	Normal operation
		4	1	Input Overvoltage (OVLOF), HVDD > 32V
		3	1	Input Undervoltage (UVLOF), HVDD < 5.5V
		2	1	Overtemperature (OTPF), TJ > +160°C
		1	1	Overtemperature Warning (OTPW), TJ > +115°C
		0	0	No Fault condition exists.
			1	A Fault condition exists.
STATUS_1	1	7:0	00000110 (06h)	Command not Acknowledged (response).
			01000110 (46h)	Command Acknowledged (response).
			10000110 (86h)	Command sent to host (unsolicited).
	2	7:4	0	Reserved
		3	1	External MOSFET Overcurrent (XOCPF) detected.
		2	1	External MOSFET Undervoltage Lockout (XUVLOF)
		1	0	Reserved
		0	1	VREG LDO Undervoltage Fault (VREGUVF)
SET_CFG_2	1	7:0	00000111 (07h)	Command not Acknowledged (response).
			01000111 (47h)	Command Acknowledged (response).
	2	7:5	00h	Reserved
		4:2	—	Driver dead time (for PWMH /PWML inputs)
			000	2000 ns (default)
			001	1750 ns
			010	1500 ns
			011	1250 ns
			100	1000 ns
			101	750 ns
			110	500 ns
			111	250 ns
		1:0	—	Driver blanking time (ignore Faults)
			00	4000 ns (default)
			01	2000 ns
			10	1000 ns
			11	500 ns

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GET_CFG_2	1	7:0	00001000 (08h)	Command not Acknowledged (response).
			01001000 (48h)	Command Acknowledged (response).
	2	7:5	00h	Reserved
		4:2	—	Driver dead time (for PWMH /PWML inputs)
			000	2000 ns
			001	1750 ns
			010	1500 ns
			011	1250 ns
			100	1000 ns
			101	750 ns
			110	500 ns
			111	250 ns
		1:0	—	Driver blanking time (ignore Faults)
			00	4000 ns
			01	2000 ns
			10	1000 ns
			11	500 ns
GET_REV_ID	1	7:0	00010000 (10h)	Command not Acknowledged (response).
			01010000 (50h)	Command Acknowledged (response).
	2	7:3	00h	Reserved
		2:0	00h-07h	Device hardware revision

13.23. MOSFET Gate Driver Registers

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13.23.1. Configuration Register 0

Name: CFG0

Bit	7	6	5	4	3	2	1	0
			SLEEP		EXTUVLO	EXTSC	EXTOC[1:0]	
Access			R/W		R/W	R/W	R/W	R/W
Reset			0		0	0	0	0

Bit 5 – SLEEP Sleep Mode bit
Bit may only be changed while in Standby mode.

Value	Description
1	System enters Sleep mode when OE = 0
0	System enters Standby mode when OE = 0

Bit 3 – EXTUVLO External MOSFET Undervoltage Lockout bit
Bit may only be changed while in Standby mode.

Value	Description
1	External MOSFET Undervoltage Lockout bit is disabled
0	External MOSFET Undervoltage Lockout bit is enabled

Bit 2 – EXTSC External MOSFET Short-Circuit Detection bit

Value	Description
1	External MOSFET Short-Circuit Detection bit is disabled
0	External MOSFET Short-Circuit Detection bit is enabled

Bits 1:0 – EXTOC[1:0] External MOSFET Overcurrent Limit Value bits

Value	Description
11	Overcurrent limit set to 1.000V
10	Overcurrent limit set to 0.750V
01	Overcurrent limit set to 0.500V
00	Overcurrent limit set to 0.250V

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13.23.2. Configuration Register 2

Name: CFG2

Bit	7	6	5	4	3	2	1	0
				DRVDT[2:0]			DRVBL[1:0]	
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:2 – DRVDT[2:0] Driver Dead-Time Selection bits

Value	Description
111	250 ns
110	500 ns
101	7500 ns
100	1000 ns
011	1250 ns
010	1500 ns
001	1750 ns
000	2000 ns

Bits 1:0 – DRVBL[1:0] Driver Blanking Time Selection bits
Bit may only be changed while in Standby mode

Value	Description
11	500 ns
10	1000 ns
01	2000 ns
00	4000 ns

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13.23.3. Status Register 0

Name: STAT0

Bit	7	6	5	4	3	2	1	0
	PCON[2:0]			OVLOF	UVLOF	OTPF	OTPW	FAULT
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – PCON[2:0] Power Control Status bits (configuration lost if non-zero value)

Value	Description
101	Overtemperature Shutdown (OTSHDN) occurred
100	Overvoltage Shutdown (OVSHDN) occurred
011	Sleep (SLEEP) shutdown occurred
110	Undervoltage Shutdown (UVSHDN) occurred
001	Power-on Reset (POR) occurred
000	Normal operation

Bit 4 – OVLOF Input Overvoltage Lockout Fault bit

Value	Description
1	HV_{DD} input voltage > 32V
0	HV_{DD} input voltage < 32V

Bit 3 – UVLOF Input Undervoltage Lockout Fault bit

Value	Description
1	HV_{DD} input voltage < 5.5V
0	HV_{DD} input voltage > 5.5V

Bit 2 – OTPF Overtemperature Protection Fault bit

Value	Description
1	Device junction temperature is > +165 C
0	Device junction temperature is < +165 C

Bit 1 – OTPW Overtemperature Protection Warning bit

Value	Description
1	Device junction temperature is > +115 C
0	Device junction temperature is < +115 C

Bit 0 – FAULT Fault Status bit

Value	Description
1	At least one Fault is active
0	No active Faults

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13.23.4. Status Register 1

Name: STAT1

Bit	7	6	5	4	3	2	1	0
					XOCPF	XUVLOF		VREGUVF
Access					R	R		R
Reset					0	0		0

Bit 3 – XOCPF External MOSFET Overcurrent Protection Fault bit
Only Valid when EXTSC (CFG0[2]) = 0.

Value	Description
1	External MOSFET VDS > EXTOC[1:0] (CFG0[1:0]) value
0	External MOSFET VDS < EXTOC[1:0] (CFG0[1:0]) value

Bit 2 – XUVLOF External MOSFET Gate Drive Undervoltage Fault bit
Only Valid when EXTUVLO (CFG0[3]) = 0.

Value	Description
1	HSx or LSx output voltage < V_{DUVLO}
0	HSx and LSx output voltage > V_{DUVLO}

Bit 0 – VREGUVF VREG LDO Undervoltage Fault bit

Value	Description
1	V_{REG} LDO output voltage < 88% of target V_{REG}
0	V_{REG} LDO output voltage > 92% of target V_{REG}

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13.23.5. Hardware Revision ID

Name: REV_ID

Bit	7	6	5	4	3	2	1	0
							REVID[1:0]	
Access							R	R
Reset							x	x

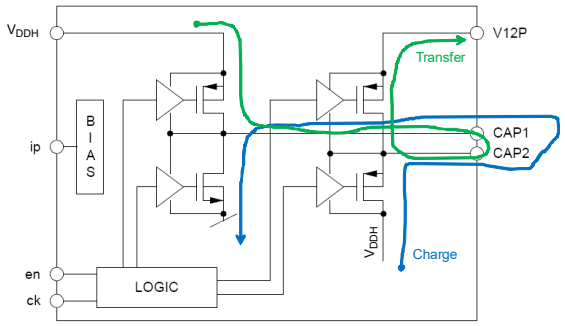
Bits 1:0 – REVID[1:0] Device Revision bits

13.24. Application Information

13.24.1. Component Calculations

13.24.1.1. Charge Pump Capacitors

Figure 13-7. Charge Pump



Let:

- I_{OUT} = 20 mA
- f_{CP} = 75 kHz (charge/discharge in one cycle)
- 50% duty cycle
- V_{DDH} = 5.5V (worst case)
  - R_{DSON} = 7.5Ω (RPMOS), 3.5Ω (RNMOS)
  - V12P = 2 × V_{DDH} (ideal)
  - C_{ESR} = 20 mΩ (ceramic capacitors)
  - V_{DROP} = 100 mV (V_{OUT} ripple)
  - T_{CHG} = T_{DCHG} = 0.5 × 1/75 kHz = 6.67 µs

13.24.1.2. Flying Capacitor

The flying capacitor should be chosen to charge to a minimum of 95% (3τ) of V_{DDH} within one half of a switching cycle.

- 3 × τ = T_{CHG}
- τ = T_{CHG}/3
- RC = T_{CHG}/3
- C = T_{CHG}/(R × 3)
- C = 6.67 µs/([7.5Ω + 3.5Ω + 0.02Ω] □ 3)

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- C = 202 nF

Choose a 180 nF capacitor.

13.24.1.3. Charge Pump Output Capacitor

Solve for the charge pump output capacitance, connected between V12P and ground, that will supply the 20 mA load for one switch cycle. The V_{BOOT} LDO pin on the dsPIC33CDVL256MC506 is the "V12P" pin referenced in the calculations.

- $C = I_{OUT} \times dt/dV$
- $C = I_{OUT}$ □ 13.3 µs/($V_{DROP} + I_{OUT} \times C_{ESR}$)
- C = 20 mA □ 13.3 µs/(0.1V + 20 mA □ 20 m□)
- C ≥ 2.65 µF

For stability reasons, the V_{BOOT} LDO and V_{REG} LDO capacitors must be at least 4.7 µF, so choose: C ≥ 4.7 µF.

13.24.1.4. Charging Path (Flying Capacitor Across CAP1 and CAP2)

- $V_{CAP} = V_{DDH} \times (1 - e\text{-}T/\tau)$
- $V_{CAP} = 5.5V \times (1 - e^{-[6.67}$ µs/([7.5Ω + 3.5Ω + 20 mΩ] x 180 nF)])

V_{CAP} = 5.31V is available for transfer on the first cycle.

13.24.1.5. Transfer Path (Flying and Output Capacitors)

- $V12P = V_{DDH} + V_{CAP} - I_{OUT} \times dt/C$
- V12P = 5.5V + 5.31V – (20 mA × 6.67 µs/180 nF)
- V12P = 10.066V

13.24.1.6. Calculate the Flying Capacitor Voltage Drop in One Cycle While Supplying 20 mA

- $dV = I_{OUT} \times dt/C$
- dV = 20 mA × 6.67 µs/180 nF
- dV = 0.741V @ 20 mA

The second and subsequent transfer cycles will have a higher voltage available for transfer, since the capacitor is not completely depleted with each cycle. V_{CAP} will then be V_{CAP} – dV after the first transfer, plus $V_{DDH} - (V_{CAP} - dV)$ times the RC constant. This repeats for each subsequent cycle, allowing a larger charge pump capacitor to be used if the system will tolerate several charge transfers before requiring full output voltage and current.

Repeating Charging Path (Flying Capacitor Across CAP1 and CAP2) for the second cycle (and subsequent by recalculating for each new value of V_{CAP} after each transfer):

- $V_{CAP} = (V_{CAP} - dV) + (V_{DDH} - (V_{CAP} - dV))\ (1 - e\text{-}T/t)$
- $V_{CAP} = (5.31V - 0.741V) + (5.5V - (5.31V - 0.741V)) \times$ $(1 - e\text{-}[6.67\ \mu s/([7.5W + 3.5W + 20\ mW] \times 180\ nF)])$
- $V_{CAP} = 4.567V + 0.934V \times 0.96535$

V_{CAP} = 5.468V is available for transfer on the second cycle.

13.24.1.7. Charge Pump Results

The maximum charge pump flying capacitor value is 202 nF to maintain a 95% voltage transfer ratio on the first charge pump cycle. Larger capacitor values may be used, but they will require more cycles to charge to maximum voltage. The minimum required output capacitor value is 2.65 µF to supply 20 mA for 13.3 µs with a 100 mV drop. A larger output capacitor may be used to cover losses due to capacitor tolerance over temperature, capacitor dielectric and PCB losses.

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These are approximate calculations. The actual voltages may vary due to incomplete charging or discharging of capacitors per cycle due to load changes. The charge pump calculations assume the charge pump is able to charge up the external boot cap within a few cycles.

13.24.2. Bootstrap Capacitor

The high-side driver bootstrap capacitor needs to power the high-side driver and gate for 1/3 of the motor electrical period for a 3-phase BLDC motor operating in Six-Step mode.

Let:

MOSFET Driver Current = 300 mA

PWM Period = 50 µs (20 kHz) Minimum Duty Cycle = 1% (500 ns) Maximum Duty Cycle = 99% (49.5 µs)

V_{IN} = 12V

Minimum Gate Drive Voltage = 8V (V_{GS})

Total Gate Charge = 130 nC (80A MOSFET)

Allowable VGS Drop (V_{DROP}) = 3V

Switch RDSON = 100 mW Driver Internal Bias Current = 20 µA (IBIAS)

Solve for the smallest capacitance that can supply:

- 130 nC of charge to the MOSFET gate
- 1 Megohm gate source resistor current
  - Driver bias current and switching losses

Q_{MOSFET} = 130 nC

$Q_{RESISTOR} = [(V_{GS}/R) \times T_{ON}]$

$Q_{DRIVER} = (I_{BIAS} \times T_{ON})$

TON = 49.5 µs (99% DC) for worst case

$Q_{RESISTOR} = Q_{RESISTOR}$

Q_{DRIVER} = 20 µA × 49.5 µs = 0.99 nC

Sum all of the energy requirements:

- $C = (Q_{MOSFET} + Q_{RESISTOR} + Q_{DRIVER})/V_{DROP}$
  - C = (130 nC + 0.594 nC + 0.99 nC)/3V
  - C = 43.86 nF

Choose a bootstrap capacitor value that is larger than 43.86 nF.

13.25. Device Protection

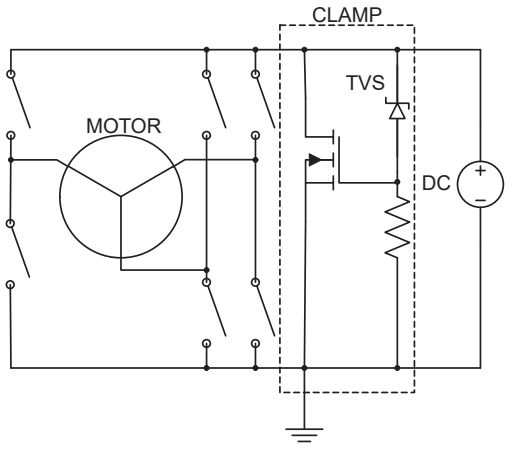
13.25.1. MOSFET Voltage Suppression

When a motor shaft is rotating and power is removed, the magnetism of the motor components will cause the motor to act like a generator. The current that was flowing into the motor will now flow out of the motor. As the motor magnetic field decays, the generator output will also decay. The voltage across the generator terminals will be proportional to the generator current and circuit impedance of the generator circuit. If the power supply is part of the return path for the current and the power supply is disconnected, then the voltage at the generator terminals will increase until the current flows. This voltage increase must be handled externally to the driver. A voltage suppression device may be used to clamp the motor terminal voltage to a level that will not exceed the maximum system operating voltage during the high-voltage transients. A voltage suppressor

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circuit may be connected from power ground to the motor power supply rail to create a path for the motor current when the supply is disconnected (Figure 13-8). The PCB traces must be capable of carrying the motor current with minimum voltage and temperature rise.

Figure 13-8. Transient Voltage Clamp



An additional method is to inactivate the high-side drivers and to activate the low-side drivers. This allows current to flow through the low-side external MOSFETs and prevents the voltage from increasing at the power supply terminals.

13.25.2. Bootstrap Voltage Suppression

The pins which handle the highest voltage during motor operation are the bootstrap pins (VBx). The bootstrap pin voltage is typically V_{BOOT} (12V) higher than the associated phase voltage. When the high-side MOSFET is conducting, the phase pin voltage is typically at HV_{DD} and the bootstrap pin voltage is typically at HV_{DD} + 12V. When the phase MOSFETs switch, current induced voltage transients occur on the phase pins. These currents are caused by the MOSFET body diode reverse recovery and MOSFET turn-on/turn-off times. Those induced voltages cause the bootstrap pin voltages to also increase. Depending on the magnitude of the phase pin voltage, the bootstrap pin voltage may exceed the safe operating voltage of the device. The current induced transients may be reduced by slowing down the turn-on and turn-off times of the MOSFETs. The external MOSFETs may be slowed down by adding a 10 to 100 ohm resistor in series with the gate drive. A 3.3 nF to 10 nF ceramic capacitor may be added that connects each MOSFET gate and source terminal. The added capacitance slows down the switching times of the MOSFET, while allowing the gate resistance to remain small enough to keep the gate clamped off. The added capacitance also results in a lower slew rate of the phase node and limits the shoot-through current caused by the body diode reverse recovery.

The high-side MOSFETs may also be slowed down by inserting a 10Ω to 25Ω resistor between each bootstrap pin and the associated bootstrap diode capacitor junction. Another 25Ω to 50Ω resistor is then added between the gate drive and the MOSFET gate. This results in a high-side turn-on resistance of 25Ω plus the series gate resistor. The high-side turn-off resistance only consists of the series gate resistance and allows for a faster shut-off time. Care must be taken to make sure the voltage drop across the bootstrap pin resistor does not cause an external MOSFET Undervoltage Fault.

When a system motor power supply voltage clamp is not used, 33V or 36V transzorbs may be connected from each bootstrap pin (VBx) to the ground. This will ensure that the bootstrap voltage does not exceed the absolute maximum voltage allowed on the pins. The resistors connected between the bootstrap pins and the bootstrap diode/capacitor junctions, mentioned in the previous paragraph, may also be used in order to limit the transzorb current and reduce the transzorb package size.

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13.25.3. Floating Gate Suppression

The gate drive pins may float when the supply voltage is lost or an overvoltage situation shuts down the driver. When an overvoltage condition exists, the driver high-side and low-side outputs are tri-state. Each external MOSFET that is connected to the gate driver should have a gate-to-source resistor to bleed off any charge that may accumulate due to the tri-state. This will help prevent inadvertent turn-on of the MOSFET.

Figure 13-9 shows the location of the overvoltage transzorbs (or equivalent circuits), gate resistors, bootstrap resistors and gate-to-source resistors.

13.25.4. MOSFET Body Diode Reverse Recovery Snubber

When motor current is flowing through the external MOSFET body diodes and the complimentary MOSFET of the phase pair turns on, the body diode reverse recovery creates a momentary short circuit until the reverse recovery time is complete. When the body diode reverse recovery is complete, the current path is opened, causing the phase node voltage to slew rapidly towards ground or HVDD levels. The rapid slew rate may cause an inversion of the gate-to-source voltage on the MOSFET that is turning on and result in that MOSFET turning off.

The fast slew rate may also cause ringing on the phase node and the sense resistor if the turn-off is too fast.

The first remedy for the low-side turn-off is to slow down the MOSFET gate-to-source turn-off. That causes the RDSON of the low-side MOSFET to gradually increase as the gate voltage drops and the low-side MOSFET slowly turns off. The slow turn-off allows the phase voltage, generated by the motor current flowing through the low-side MOSFET RDSON, to slowly rise towards the positive motor supply level.

The same scenario is also valid for turning on the low-side MOSFET when the high-side MOSFET has just been turned off and current was flowing from the high side into the motor.

The MOSFET body diode reverse recovery situation occurs when the low-side MOSFETs are turned on while the motor current is flowing to the positive source through the high-side MOSFET body diode. The diode reverse recovery time allows a short circuit to exist between the positive supply and the low-side MOSFET drain until the high-side diode is reverse biased and the reverse recovery time has elapsed. The first remedies above should be used to slow the switching speeds of the MOSFETs. Then, a snubber is added to each MOSFET to fine-tune the phase node slew rate and eliminate any further transients. Adding a drain-to-source snubber slows down the slew rate of the phase node and results in a more controlled excursion of the phase node voltage. The snubber consists of a resistor and a capacitor connected in series between the drain and source of the MOSFET. The resistor is chosen to keep the initial snubber voltage below a few volts when peak motor current is flowing through the body diode. The capacitor is then chosen to provide an RC time constant longer than the MOSFET body diode reverse recovery time. A 0.1Ω resistor is typically used, along with a 0.1 µF capacitor to provide an RC of 10 ns.

The power dissipated by the capacitor is calculated by applying Equation 13-5.

Equation 13-5. Snubber Capacitor Power Dissipation

$$P_{DISS} = 2 \times \pi \times f \times C \times V^2 \times Dissipation\ Factor$$

Where:

f = PWM Frequency
C = Capacitance
V = Motor Voltage
$Dissipation\ Factor$ = 2 × p × f × C × ESR = ESR/Xc

The capacitor and resistor form factors are chosen to handle the dissipated power.

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13.25.5. Motor Current Sense Circuitry

A sense resistor in series with the bridge ground return provides a current signal for feedback. This resistor should be non-inductive to minimize ringing from high di/dt. Any inductance in the power circuit represents potential problems in the form of additional voltage stress and ringing, as well as increasing switching times. While impractical to eliminate, careful layout and bypassing will minimize these effects. The output stage should be as compact as heat sinking will allow, with wide, short traces carrying all pulsed currents. Each half-bridge should be separately bypassed with a low-ESR/ESL capacitor, decoupling it from the rest of the circuit. Some layouts will allow the input filter capacitor to be split into three smaller values and serve double duty as the half-bridge bypass capacitors.

13.25.6. Auto-Baud Code Example

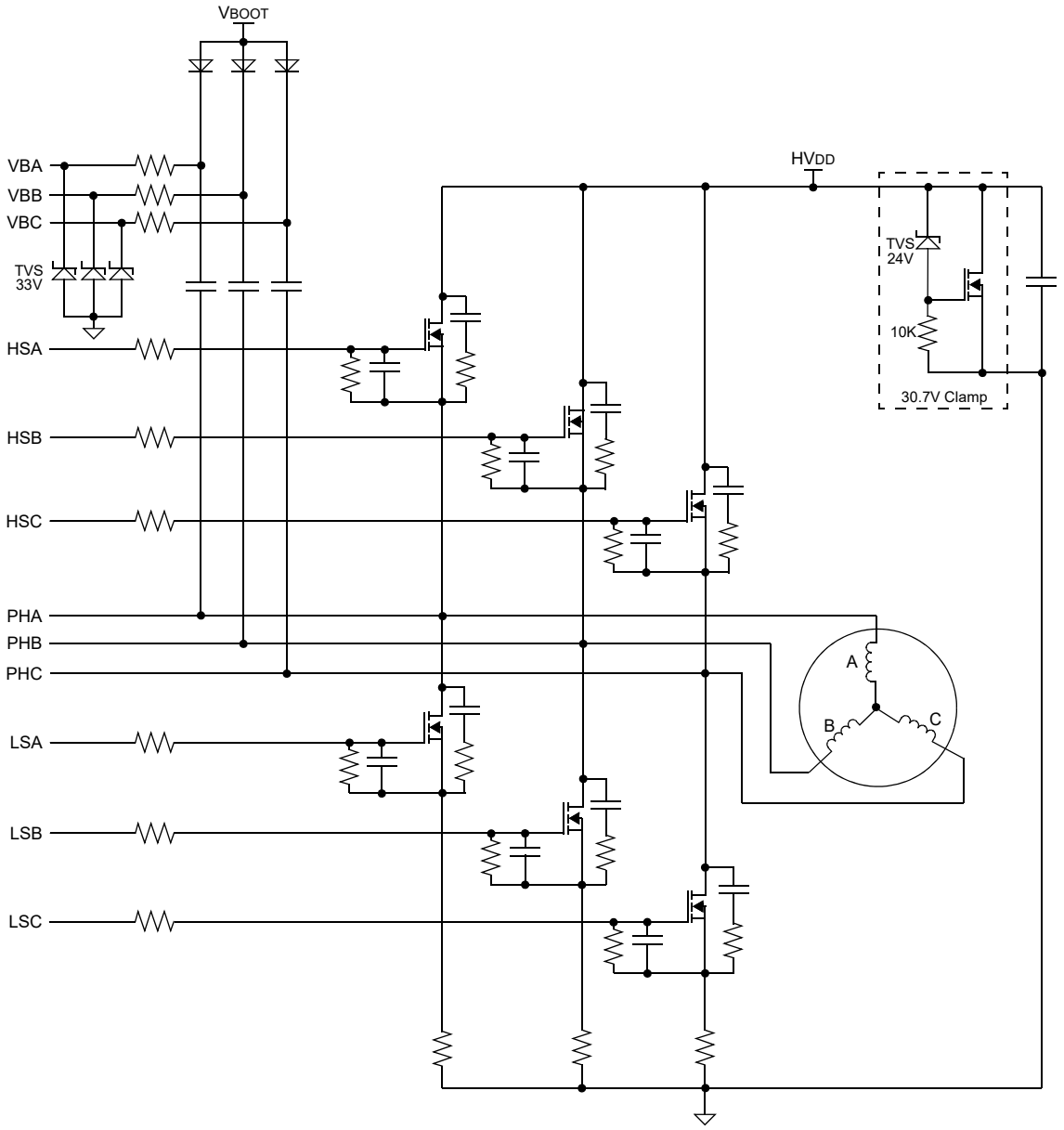
Example 13-1 is a dsPIC® DSC code example using the auto-baud function.

Example 13-1. dsPIC® DSC Auto-Baud Example

```
//#define FCY 70000000UL
#define TypBaudrate 9600uL
#define U1BRG_BAUDRATE (FCY/(16 * TypBaudrate)) - 1
#define U1BRG_BAUD_MIN ((((FCY/(16 * TypBaudrate)) - 1)*1.07f)) // plus 7%
#define U1BRG_BAUD_MAX ((((FCY/(16 * TypBaudrate)) - 1)*0.93f)) // minus 7%
#define U1BRG_BREAK (FCY/(16 * 7880uL)) - 1 //7880 baud-rate is midpoint of
required break
//window for MCP8021
//set up Oscillator_Initialize code here
void UART1_Init(void){
//UART configuration - set up PPS connections and UART module enable here
_TRISC12 = 1; //required for proper UART RX receiption of DE2 messages
_CNPUC12 = 1; //required to pull DE2 high because interconnect is open-drain
_ODC12 = 1; //recommended so pull-up is fully utilized
//PPS assignment of UART RX/TX to RC12
//enable half-duplex mode if available to auto-disable transmiter when idle
U1MODEbits.UARTEN = 1; //enable UART
U1MODEbits.URXEN = 1; //for half-duplex communication, keep RX on always and
manage TX as
//needed in auto-baud routine
//if half-duplex mode not available, activate TXEN for transmission and
disable TXEN when idle
__delay_ms(10); //10mS delay required after POR of MCP8021 and before
requesting auto-baud
}
void UART1_AutoBaud(void){
U1MODEbits.UTXEN = 1; //Transmit enabled, UxTX pin controlled by UARTx.
U1BRG = U1BRG_BREAK; //7880baud representing 1.65ms dominant with 13bit BREAK
U1MODEbits.UTXBRK = 1; //Send BREAK command
U1TXREG = 0x00; //Dummy write to start BREAK command
while(U1STAHbits.URXBE == 0){ //wait for transmission to end then read out
RXREG to
//avoid collision.
unsigned short dummy = U1RXREG;
}
U1MODEbits.UTXEN = 0; //disable TX while waiting on 0x55 from MCP8021
U1MODEbits.ABAUD = 1; //start the ABAUD counter upon receipt of next byte
(0x55)
while(U1MODEbits.ABAUD); //application should handle timeout if auto-baud does
not
complete and attempt auto-baud routine again
__delay_ms(3); //minimum delay of 2mS required after auto-baud complete
to allow for baud rate verification by host
//verify new baud clock is within limits of MCP8021 min and max baud-rate
if ((U1BRG > U1BRG_BAUD_MAX) && (U1BRG < U1BRG_BAUD_MIN)){
//success, use new baud-rate generator value
}
else{
//auto-baud out of range, reload last known good BRG value and attempt auto-
baud routine again
}
}
```


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Figure 13-9. Overvoltage Protection



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14. High-Speed, 12-Bit Analog-to-Digital Converter

Notes:

1. This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"12-Bit High-Speed, Multiple SARs A/D Converter (ADC)"** (www.microchip.com/DS70005213) in the *"dsPIC33/PIC24 Family Reference Manual"*.
2. Some registers and associated bits described in this section may not be available on all devices due to the number of implemented ADC channels. Refer to Table 1 for ADC channel availability on device variants.

dsPIC33CDVL256MC506 devices have a high-speed, 12-bit Analog-to-Digital Converter (ADC) that features a low conversion latency, high resolution and oversampling capabilities to improve performance in AC/DC and DC/DC power converters. The devices implement the ADC with one shared core.

The number of available channels and negative inputs is dependent on package size, as shown in Table 14-1.

Table 14-1. ADC External Input Availability

Package Type	External Inputs	Negative Inputs
64-pin	AN0-AN19	ANN0
48-pin	AN0-AN19	ANN0
36-pin	AN0-AN6, AN8- AN17	—
28-pin	AN0-AN6, AN8-AN11, AN16-AN17	—

14.1. ADC Features Overview

The high-speed, 12-bit multiple SARs Analog-to-Digital Converter (ADC) includes the following features:

- One Shared (common) Core
- User-Configurable Resolution of Up to 12 Bits
- Up to 3.25 Msps Conversion Rate per Channel at 12-Bit Resolution
- Low Latency Conversion
- Up to 18 Analog Input Channels with a Separate 16-Bit Conversion Result Register for Each Input Channel
- Conversion Result can be Formatted as Unsigned or Signed Data, on a per Channel Basis, for All Channels
- Channel Scan Capability
- Multiple Conversion Trigger Options, Including:
  - PWM triggers from CPU core
  - SCCP modules triggers
  - CLC modules triggers
  - External pin trigger event (ADTRG31)
  - Software trigger
- Four Integrated Digital Comparators with Dedicated Interrupts:
  - Multiple comparison options
  - Assignable to specific analog inputs

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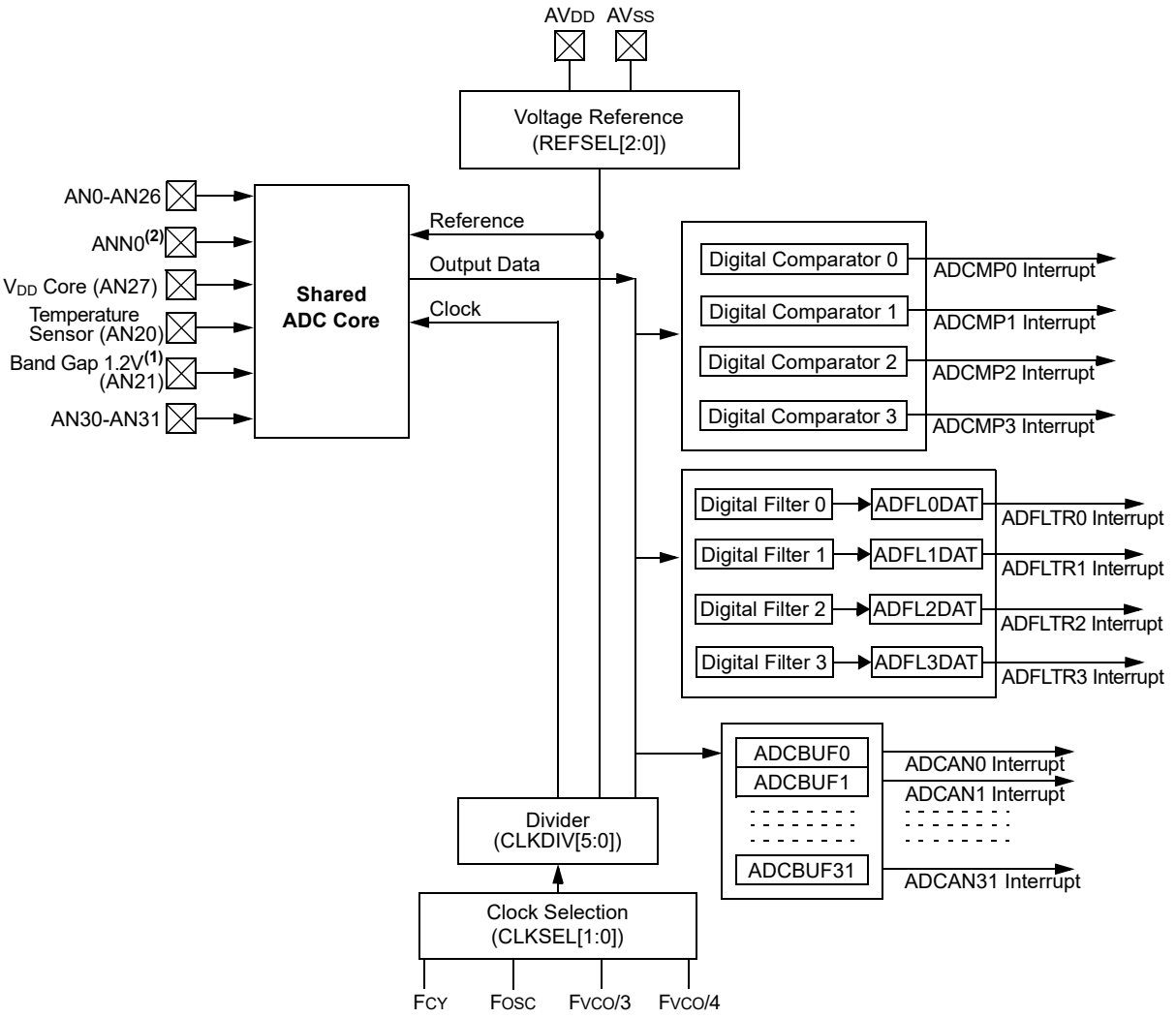
- Four Oversampling Filters with Dedicated Interrupts:
  - Provide increased resolution
  - Assignable to a specific analog input

Simplified block diagrams of the 12-bit ADC are shown in Figure 14-1 and Figure 14-2.

The analog inputs (channels) are connected through multiplexers and switches to the Sample-and-Hold (S&H) circuit of the ADC core. The core uses the channel information (the output format, the Measurement mode and the input number) to process the analog sample. When conversion is complete, the result is stored in the result buffer for the specific analog input, and passed to the digital filter and digital comparator if they were configured to use data from this particular channel. If multiple ADC inputs request conversion on the shared core, the module will convert them in a sequential manner, starting with the lowest order input.

The ADC provides each analog input the ability to specify its own trigger source. This capability allows the ADC to sample and convert analog inputs that are associated with PWM Generators operating on independent time bases.

Figure 14-1. ADC Module Block Diagram

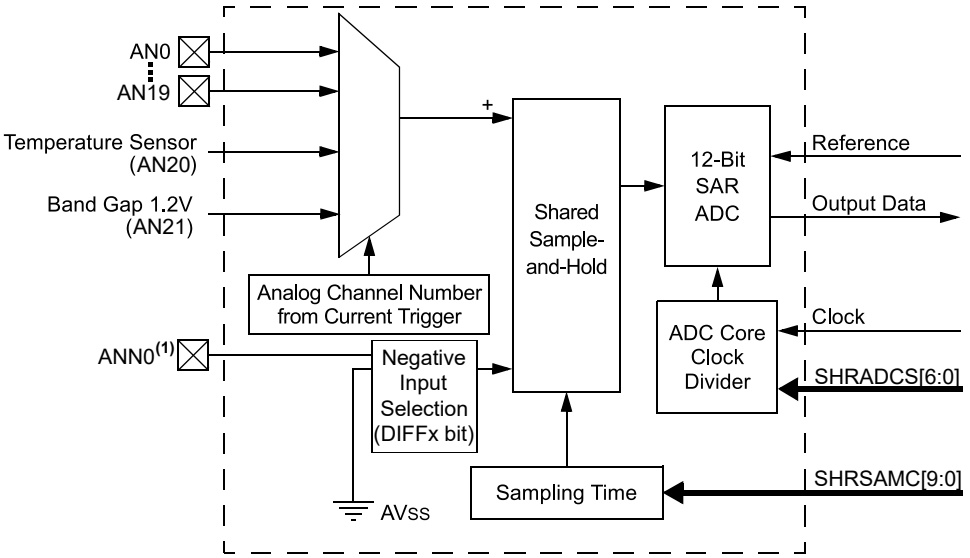


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Notes:

1. Band Gap Reference (V_{BG}) is an internal analog input and is not available on device pins.
2. Pin ANN0 is only available in the 48-pin and 64-pin packages.

Figure 14-2. Shared Core Block Diagram



Note:

1. Pin ANN0 is only available in the 48-pin and 64-pin packages.

14.1.1. Temperature Sensor

The ADC channel, AN20, is connected to a forward-biased diode. It can be used to measure a die temperature. This diode provides a voltage output that can be monitored by the ADC.

The temperature coefficient is listed in Table 34-33 in Electrical Characteristics. To get the exact gain and offset numbers, the two temperature points' calibration is recommended.

14.2. Analog-to-Digital Converter Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page contains the latest updates and additional information.

14.2.1. Differential-Mode

ANNx negative external inputs are used for Differential-mode as shown in Figure 14-2. To enable Differential-mode, the DIFF bit (in the ADMODxL or ADMODxH register) is set for the corresponding channel.

14.2.2. Key Resources

- **"12-Bit High-Speed, Multiple SARs A/D Converter (ADC)"** (www.microchip.com/DS70005213) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries

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- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

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14.3. ADC Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0B00	ADCON1L	15:8	ADON		ADSIDL					
		7:0								
0x0B02	ADCON1H	15:8								
		7:0	FORM	SHRRES[1:0]						
0x0B04	ADCON2L	15:8	REFCIE	REFERCIE		EIEN	PTGEN	SHREISEL[2:0]		
		7:0		SHRADCS[6:0]						
0x0B06	ADCON2H	15:8	REFRDY	REFERR					SHRSAMC[9:8]	
		7:0	SHRSAMC[7:0]							
0x0B08	ADCON3L	15:8	REFSEL[2:0]			SUSPEND	SUSPCIE	SUSPRDY	SHRSAMP	CNVRTCH
		7:0	SWLCTRG	SWCTRG	CNVCHSEL[5:0]					
0x0B0A	ADCON3H	15:8	CLKSEL[1:0]		CLKDIV[5:0]					
		7:0	SHREN							
0x0B0C ... 0x0B0F	Reserved									
0x0B10	ADMOD0L	15:8	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4
		7:0	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0
0x0B12	ADMOD0H	15:8	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12
		7:0	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8
0x0B14	ADMOD1L	15:8					DIFF21	SIGN21	DIFF20	SIGN20
		7:0	DIFF19	SIGN19	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16
0x0B16 ... 0x0B1F	Reserved									
0x0B20	ADIEL	15:8	IE[15:8]							
		7:0	IE[7:0]							
0x0B22	ADIEH	15:8								
		7:0			IE[21:16]					
0x0B24 ... 0x0B2F	Reserved									
0x0B30	ADSTATL	15:8	AN[15:8]RDY							
		7:0	AN[7:0]RDY							
0x0B32	ADSTATH	15:8								
		7:0			AN[21:16]RDY					
0x0B34 ... 0x0B37	Reserved									
0x0B38	ADCMP0ENL	15:8	CMPEN[15:8]							
		7:0	CMPEN[7:0]							
0x0B3A	ADCMP0ENH	15:8								
		7:0			CMPEN[21:16]					
0x0B3C	ADCMP0LO	15:8	CMPLO[15:8]							
		7:0	CMPLO[7:0]							
0x0B3E	ADCMP0HI	15:8	CMPHI[15:8]							
		7:0	CMPHI[7:0]							
0x0B40	ADCMP1ENL	15:8	CMPEN[15:8]							
		7:0	CMPEN[7:0]							
0x0B42	ADCMP1ENH	15:8								
		7:0			CMPEN[21:16]					
0x0B44	ADCMP1LO	15:8	CMPLO[15:8]							
		7:0	CMPLO[7:0]							
0x0B46	ADCMP1HI	15:8	CMPHI[15:8]							
		7:0	CMPHI[7:0]							
0x0B48	ADCMP2ENL	15:8	CMPEN[15:8]							
		7:0	CMPEN[7:0]							
0x0B4A	ADCMP2ENH	15:8								
		7:0			CMPEN[21:16]					

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ADC Control Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0B4C	ADCMP2LO	15:8	CMPLO[15:8]							
		7:0	CMPLO[7:0]							
0x0B4E	ADCMP2HI	15:8	CMPHI[15:8]							
		7:0	CMPHI[7:0]							
0x0B50	ADCMP3ENL	15:8	CMPEN[15:8]							
		7:0	CMPEN[7:0]							
0x0B52	ADCMP3ENH	15:8								
		7:0			CMPEN[21:16]					
0x0B54	ADCMP3LO	15:8	CMPLO[15:8]							
		7:0	CMPLO[7:0]							
0x0B56	ADCMP3HI	15:8	CMPHI[15:8]							
		7:0	CMPHI[7:0]							
0x0B58 ... 0x0B67	Reserved									
0x0B68	ADFL0DAT	15:8	FLDATA[15:8]							
		7:0	FLDATA[7:0]							
0x0B6A	ADFL0CON	15:8	FLEN	MODE[1:0]		OVRSAM[2:0]			IE	RDY
		7:0				FLCHSEL[4:0]				
0x0B6C	ADFL1DAT	15:8	FLDATA[15:8]							
		7:0	FLDATA[7:0]							
0x0B6E	ADFL1CON	15:8	FLEN	MODE[1:0]		OVRSAM[2:0]			IE	RDY
		7:0				FLCHSEL[4:0]				
0x0B70	ADFL2DAT	15:8	FLDATA[15:8]							
		7:0	FLDATA[7:0]							
0x0B72	ADFL2CON	15:8	FLEN	MODE[1:0]		OVRSAM[2:0]			IE	RDY
		7:0				FLCHSEL[4:0]				
0x0B74	ADFL3DAT	15:8	FLDATA[15:8]							
		7:0	FLDATA[7:0]							
0x0B76	ADFL3CON	15:8	FLEN	MODE[1:0]		OVRSAM[2:0]			IE	RDY
		7:0				FLCHSEL[4:0]				
0x0B78 ... 0x0B7F	Reserved									
0x0B80	ADTRIG0L	15:8				TRGSRC1[4:0]				
		7:0				TRGSRC0[4:0]				
0x0B82	ADTRIG0H	15:8				TRGSRC3[4:0]				
		7:0				TRGSRC2[4:0]				
0x0B84	ADTRIG1L	15:8				TRGSRC5[4:0]				
		7:0				TRGSRC4[4:0]				
0x0B86	ADTRIG1H	15:8				TRGSRC7[4:0]				
		7:0				TRGSRC6[4:0]				
0x0B88	ADTRIG2L	15:8				TRGSRC9[4:0]				
		7:0				TRGSRC8[4:0]				
0x0B8A	ADTRIG2H	15:8				TRGSRC11[4:0]				
		7:0				TRGSRC10[4:0]				
0x0B8C	ADTRIG3L	15:8				TRGSRC13[4:0]				
		7:0				TRGSRC12[4:0]				
0x0B8E	ADTRIG3H	15:8				TRGSRC15[4:0]				
		7:0				TRGSRC14[4:0]				
0x0B90	ADTRIG4L	15:8				TRGSRC17[4:0]				
		7:0				TRGSRC16[4:0]				
0x0B92	ADTRIG4H	15:8				TRGSRC19[4:0]				
		7:0				TRGSRC18[4:0]				
0x0B94	ADTRIG5L	15:8				TRGSRC21[4:0]				
		7:0				TRGSRC20[4:0]				
0x0B96 ... 0x0B9F	Reserved									

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ADC Control Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0BA0	ADCMP0CON	15:8				CHNL[4:0]				
		7:0	CMPEN	IE	STAT	BTWN	HIHI	HILO	LOHI	LOLO
0x0BA2 ... 0x0BA3	Reserved									
0x0BA4	ADCMP1CON	15:8				CHNL[4:0]				
		7:0	CMPEN	IE	STAT	BTWN	HIHI	HILO	LOHI	LOLO
0x0BA6 ... 0x0BA7	Reserved									
0x0BA8	ADCMP2CON	15:8				CHNL[4:0]				
		7:0	CMPEN	IE	STAT	BTWN	HIHI	HILO	LOHI	LOLO
0x0BAA ... 0x0BAB	Reserved									
0x0BAC	ADCMP3CON	15:8				CHNL[4:0]				
		7:0	CMPEN	IE	STAT	BTWN	HIHI	HILO	LOHI	LOLO
0x0BAE ... 0x0BCF	Reserved									
0x0BD0	ADLVLTRGL	15:8	LVLEN[15:8]							
		7:0	LVLEN[7:0]							
0x0BD2	ADLVLTRGH	15:8								
		7:0			LVLEN[21:16]					
0x0BD4 ... 0x0BEF	Reserved									
0x0BF0	ADEIEL	15:8	EIEN[15:8]							
		7:0	EIEN[7:0]							
0x0BF2	ADEIEH	15:8								
		7:0			EIEN[21:16]					
0x0BF4 ... 0x0BF7	Reserved									
0x0BF8	ADEISTATL	15:8	EISTAT[15:8]							
		7:0	EISTAT[7:0]							
0x0BFA	ADEISTATH	15:8								
		7:0			EISTAT[21:16]					
0x0BFC ... 0x0BFF	Reserved									
0x0C00	ADCON5L	15:8	SHRRDY							
		7:0	SHRPWR							
0x0C02	ADCON5H	15:8					WARMTIME[3:0]			
		7:0	SHRCIE							
0x0C04 ... 0x0C0B	Reserved									
0x0C0C	ADCBUF0	15:8	ADCBUF0[15:8]							
		7:0	ADCBUF0[7:0]							
0x0C0E	ADCBUF1	15:8	ADCBUF1[15:8]							
		7:0	ADCBUF1[7:0]							
0x0C10	ADCBUF2	15:8	ADCBUF2[15:8]							
		7:0	ADCBUF2[7:0]							
0x0C12	ADCBUF3	15:8	ADCBUF3[15:8]							
		7:0	ADCBUF3[7:0]							
0x0C14	ADCBUF4	15:8	ADCBUF4[15:8]							
		7:0	ADCBUF4[7:0]							
0x0C16	ADCBUF5	15:8	ADCBUF5[15:8]							
		7:0	ADCBUF5[7:0]							

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ADC Control Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0C18	ADCBUF6	15:8	ADCBUF6[15:8]							
		7:0	ADCBUF6[7:0]							
0x0C1A	ADCBUF7	15:8	ADCBUF7[15:8]							
		7:0	ADCBUF7[7:0]							
0x0C1C	ADCBUF8	15:8	ADCBUF8[15:8]							
		7:0	ADCBUF8[7:0]							
0x0C1E	ADCBUF9	15:8	ADCBUF9[15:8]							
		7:0	ADCBUF9[7:0]							
0x0C20	ADCBUF10	15:8	ADCBUF10[15:8]							
		7:0	ADCBUF10[7:0]							
0x0C22	ADCBUF11	15:8	ADCBUF11[15:8]							
		7:0	ADCBUF11[7:0]							
0x0C24	ADCBUF12	15:8	ADCBUF12[15:8]							
		7:0	ADCBUF12[7:0]							
0x0C26	ADCBUF13	15:8	ADCBUF13[15:8]							
		7:0	ADCBUF13[7:0]							
0x0C28	ADCBUF14	15:8	ADCBUF14[15:8]							
		7:0	ADCBUF14[7:0]							
0x0C2A	ADCBUF15	15:8	ADCBUF15[15:8]							
		7:0	ADCBUF15[7:0]							
0x0C2C	ADCBUF16	15:8	ADCBUF16[15:8]							
		7:0	ADCBUF16[7:0]							
0x0C2E	ADCBUF17	15:8	ADCBUF17[15:8]							
		7:0	ADCBUF17[7:0]							
0x0C30	ADCBUF18	15:8	ADCBUF18[15:8]							
		7:0	ADCBUF18[7:0]							
0x0C32	ADCBUF19	15:8	ADCBUF19[15:8]							
		7:0	ADCBUF19[7:0]							
0x0C34	ADCBUF20	15:8	ADCBUF20[15:8]							
		7:0	ADCBUF20[7:0]							
0x0C36	ADCBUF21	15:8	ADCBUF21[15:8]							
		7:0	ADCBUF21[7:0]							

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14.3.1. ADC Control Register 1 Low

Name: ADCON1L
Offset: 0xB00

Note:

1. Set the ADON bit only after the ADC module has been configured. Changing ADC Configuration bits when ADON = 1 will result in unpredictable behavior.

Bit	15	14	13	12	11	10	9	8
	ADON		ADSIDL					
Access	R/W		R/W					
Reset	0		0					

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – ADON ADC Enable bit(1)

Value	Description
1	ADC module is enabled.
0	ADC module is off.

Bit 13 – ADSIDL ADC Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode.
0	Continues module operation in Idle mode.

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14.3.2. ADC Control Register 1 High

Name: ADCON1H
Offset: 0xB02

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	FORM	SHRRES[1:0]						
Access	R/W	R/W	R/W					
Reset	0	1	1					

Bit 7 – FORM Fractional Data Output Format bit

Value	Description
1	Fractional
0	Integer

Bits 6:5 – SHRRES[1:0] Shared ADC Core Resolution Selection bits

Value	Description
11	12-bit resolution
10	10-bit resolution
01	8-bit resolution
00	6-bit resolution

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14.3.3. ADC Control Register 2 Low

Name: ADCON2L
Offset: 0xB04

Note:

1. For the 6-bit shared ADC core resolution (SHRRES[1:0] = 00), the SHREISEL[2:0] settings, from '100' to '111', are not valid and should not be used. For the 8-bit shared ADC core resolution (SHRRES[1:0] = 01), the SHREISEL[2:0] settings, '110' and '111', are not valid and should not be used.

Bit	15	14	13	12	11	10	9	8
	REFCIE	REFERCIE		EIEN	PTGEN	SHREISEL[2:0]		
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		SHRADCS[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit 15 – REFCIE Band Gap and Reference Voltage Ready Common Interrupt Enable bit

Value	Description
1	Common interrupt will be generated when the band gap becomes ready.
0	Common interrupt is disabled for the band gap ready event.

Bit 14 – REFERCIE Band Gap or Reference Voltage Error Common Interrupt Enable bit

Value	Description
1	Common interrupt will be generated when a band gap or reference voltage error is detected.
0	Common interrupt is disabled for the band gap and reference voltage error event.

Bit 12 – EIEN Early Interrupts Enable bit

Value	Description
1	Early interrupt feature is enabled for input channel interrupts (when EISTATx flag is set).
0	Individual interrupts are generated when conversion is done (when ANxRDY flag is set).

Bit 11 – PTGEN External Conversion request interface bit

Value	Description
1	The PTG may request conversion of an ADC input using the PTG strobe output to select the channel.
0	The ADC will not be affected by the PTG strobe output.

Bits 10:8 – SHREISEL[2:0] Shared Core Early Interrupt Time Selection bits(1)

Value	Description
111	Early interrupt is set, interrupt is generated eight T_{ADCORE} clocks prior to when data are ready.
110	Early interrupt is set, interrupt is generated seven T_{ADCORE} clocks prior to when data are ready.
101	Early interrupt is set, interrupt is generated six T_{ADCORE} clocks prior to when data are ready.
100	Early interrupt is set, interrupt is generated five T_{ADCORE} clocks prior to when the data are ready.
011	Early interrupt is set, interrupt is generated four T_{ADCORE} clocks prior to when data are ready.
010	Early interrupt is set, interrupt is generated three T_{ADCORE} clocks prior to when data are ready.
001	Early interrupt is set, interrupt is generated two T_{ADCORE} clocks prior to when data are ready.
000	Early interrupt is set, interrupt is generated one T_{ADCORE} clock prior to when data are ready.

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Bits 6:0 – SHRADCS[6:0] Shared ADC Core Input Clock Divider bits
These bits determine the number of $T_{CORESRC}$ (Source Clock Periods) for one shared T_{ADCORE} (Core Clock Period).

Value	Description
1111111	254 Source Clock Periods
. . .	
0000011	6 Source Clock Periods
0000010	4 Source Clock Periods
0000001	2 Source Clock Periods
0000000	2 Source Clock Periods

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14.3.4. ADC Control Register 2 High

Name: ADCON2H
Offset: 0xB06

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
	REFRDY	REFERR					SHRSAMC[9:8]	
Access	HSC/R	HSC/R					R/W	R/W
Reset	0	0					0	0

Bit	7	6	5	4	3	2	1	0
	SHRSAMC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – REFRDY Band Gap and Reference Voltage Ready Flag bit

Value	Description
1	Band gap is ready.
0	Band gap is not ready.

Bit 14 – REFERR Band Gap or Reference Voltage Error Flag bit

Value	Description
1	Band gap was removed after the ADC module was enabled (ADON = 1).
0	No band gap error was detected.

Bits 9:0 – SHRSAMC[9:0] Shared ADC Core Sample Time Selection bits
These bits specify the number of shared ADC Core Clock Periods (T_{ADCORE}) for the shared ADC core sample time (Sample Time = (SHRSAMC[9:0] + 2) * T_{ADCORE}).

Value	Description
1111111111	1025 T_{ADCORE}
. . .	
0000000001	3 T_{ADCORE}
0000000000	2 T_{ADCORE}

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14.3.5. ADC Control Register 3 Low

Name: ADCON3L
Offset: 0xB08

Legend:HC = Hardware Clearable bit

Note:

1. When PTGEN (ADCON2L[11]) is set, the PTG strobe output will override the functionality of these bits.

Bit	15	14	13	12	11	10	9	8
	REFSEL[2:0]			SUSPEND	SUSPCIE	SUSPRDY	SHRSAMP	CNVRTCH
Access	R/W	R/W	R/W	R/W	R/W	HSC/R	R/W	R/W/HC-0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SWLCTRG	SWCTRG	CNVCHSEL[5:0]					
Access	R/W	R/W/HC-0	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:13 – REFSEL[2:0] ADC Reference Voltage Selection bits

Value	V_{REFH}	V_{REFL}
001-111	**Unimplemented:** Do not use	
000	AV_{DD}	AV_{SS}

Bit 12 – SUSPEND All ADC Core Triggers Disable bit

Value	Description
1	All new trigger events for the ADC core are disabled.
0	The ADC core can be triggered.

Bit 11 – SUSPCIE Suspend All ADC Cores Common Interrupt Enable bit

Value	Description
1	Common interrupt will be generated when ADC core triggers are suspended (SUSPEND bit = 1) and all previous conversions are finished (SUSPRDY bit becomes set).
0	Common interrupt is not generated for suspend ADC cores event.

Bit 10 – SUSPRDY ADC Core Suspended Flag bit

Value	Description
1	The ADC core is suspended (SUSPEND bit = 1) and has no conversions in progress.
0	The ADC core has previous conversions in progress.

Bit 9 – SHRSAMP Shared ADC Core Sampling Direct Control bit(1)

This bit should be used with the individual channel conversion trigger controlled by the CNVRTCH bit. It connects an analog input, specified by the CNVCHSEL[5:0] bits, to the shared ADC core and allows extending the sampling time. This bit is not controlled by hardware and must be cleared before the conversion starts (setting CNVRTCH to '1').

Value	Description
1	Shared ADC core samples an analog input specified by the CNVCHSEL[5:0] bits.
0	Sampling is controlled by the shared ADC core hardware.

Bit 8 – CNVRTCH Software Individual Channel Conversion Trigger bit(1)

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Value	Description
1	Single trigger is generated for an analog input specified by the CNVCHSEL[5:0] bits; when the bit is set, it is automatically cleared by hardware on the next instruction cycle.
0	Next individual channel conversion trigger can be generated.

Bit 7 – SWLCTRG Software Level-Sensitive Common Trigger bit

Value	Description
1	Triggers are continuously generated for all channels with the software; level-sensitive common trigger selected as a source in the ADTRIGnL and ADTRIGxH registers.
0	No software, level-sensitive common triggers are generated.

Bit 6 – SWCTRG Software Common Trigger bit

Value	Description
1	Single trigger is generated for all channels with the software; common trigger selected as a source in the ADTRIGnL and ADTRIGxH registers; when the bit is set, it is automatically cleared by hardware on the next instruction cycle.
0	Ready to generate the next software common trigger.

Bits 5:0 – CNVCHSEL[5:0] Channel No. Selection for Software Individual Channel Conv. Trigger bits(1)
These bits define a channel to be converted when the CNVRTCH bit is set.

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14.3.6. ADC Control Register 3 High

Name: ADCON3H
Offset: 0xB0A

Notes:

1. The ADC input clock frequency, selected by the CLKSEL[1:0] bits, must not exceed parameters AD9, AD10 and AD11 in Table 34-32.
2. The ADC clock frequency, after the first divider selected by the CLKDIV[5:0] bits, must not exceed parameters AD9, AD10 and AD11 in Table 34-32.

Bit	15	14	13	12	11	10	9	8
	CLKSEL[1:0]		CLKDIV[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SHREN							
Access	R/W							
Reset	0							

Bits 15:14 – CLKSEL[1:0] ADC Module Clock Source Selection bits(1)

Value	Description
11	$F_{VCO}/4$
10	$F_{VCO}/3$
01	F_{OSC}
00	F_P

Bits 13:8 – CLKDIV[5:0] ADC Module Clock Source Divider bits(2)

The divider forms a $T_{CORESRC}$ clock used by the ADC core, from the T_{SRC} ADC module clock source, selected by the CLKSEL[1:0] bits. Then, each ADC core individually divides the $T_{CORESRC}$ clock to get a core-specific T_{ADCORE} clock using the ADCS[6:0] bits in the ADCOREXH register or the SHRADCS[6:0] bits in the ADCON2L register.

Value	Description
111111	64 Source Clock Periods
. . .	
000011	4 Source Clock Periods
000010	3 Source Clock Periods
000001	2 Source Clock Periods
000000	1 Source Clock Period

Bit 7 – SHREN Shared ADC Core Enable bit

Value	Description
1	Shared ADC core is enabled
0	Shared ADC core is disabled

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14.3.7. ADC Input Mode Control Register 0 Low

Name: ADMOD0L
Offset: 0xB10

Bit	15	14	13	12	11	10	9	8
	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – DIFF7 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 14 – SIGN7 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 13 – DIFF6 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 12 – SIGN6 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 11 – DIFF5 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 10 – SIGN5 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 9 – DIFF4 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential .
0	Channel is single-ended.

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Bit 8 – SIGN4 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 7 – DIFF3 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 6 – SIGN3 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 5 – DIFF2 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 4 – SIGN2 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 3 – DIFF1 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 2 – SIGN1 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 1 – DIFF0 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 0 – SIGN0 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

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14.3.8. ADC Input Mode Control Register 0 High

Name: ADMOD0H
Offset: 0xB12

Bit	15	14	13	12	11	10	9	8
	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – DIFF15 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 14 – SIGN15 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 13 – DIFF14 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 12 – SIGN14 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed
0	Channel output data are unsigned

Bit 11 – DIFF13 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 10 – SIGN13 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 9 – DIFF12 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

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Bit 8 – SIGN12 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 7 – DIFF11 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 6 – SIGN11 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 5 – DIFF10 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 4 – SIGN10 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 3 – DIFF9 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 2 – SIGN9 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 1 – DIFF8 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 0 – SIGN8 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

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14.3.9. ADC Input Mode Control Register 1 Low

Name: ADMOD1L
Offset: 0xB14

Bit	15	14	13	12	11	10	9	8
					DIFF21	SIGN21	DIFF20	SIGN20
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DIFF19	SIGN19	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 11 – DIFF21 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 10 – SIGN21 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 9 – DIFF20 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 8 – SIGN20 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 7 – DIFF19 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 6 – SIGN19 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 5 – DIFF18 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

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Bit 4 – SIGN18 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 3 – DIFF17 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential.
0	Channel is single-ended.

Bit 2 – SIGN17 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

Bit 1 – DIFF16 Differential-Mode for Corresponding Analog Inputs bit

Value	Description
1	Channel is differential
0	Channel is single-ended

Bit 0 – SIGN16 Output Data Sign for Corresponding Analog Input bit

Value	Description
1	Channel output data are signed.
0	Channel output data are unsigned.

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14.3.10. ADC Interrupt Enable Register Low

Name: ADIEL(1)
Offset: 0xB20

Note:

1. Bit availability is dependent on the number of supported ADC channels. Refer to Table 1 for ADC channel availability on package variants.

Bit	15	14	13	12	11	10	9	8
	IE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – IE[15:0] Common Interrupt Enable bits

Value	Description
1	Common and individual interrupts are enabled for the corresponding channel
0	Common and individual interrupts are disabled for the corresponding channel

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14.3.11. ADC Interrupt Enable Register High

Name: ADIEH(1)
Offset: 0xB22

Note:

1. Bit availability is dependent on the number of supported ADC channels. Refer to Table 1 for ADC channel availability on package variants.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			IE[21:16]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – IE[21:16] Common Interrupt Enable bits

Value	Description
1	Common and individual interrupts are enabled for the corresponding channel
0	Common and individual interrupts are disabled for the corresponding channel

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14.3.12. ADC Data Ready Status Register Low

Name: ADSTATL(1)
Offset: 0xB30

Note:

1. Bit availability is dependent on the number of supported ADC channels. Refer to Table 1 for ADC channel availability on package variants.

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
	AN[15:8]RDY							
Access	HSC/R	HSC/R	HSC/R	HSC/R	HSC/R	HSC/R	HSC/R	HSC/R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	AN[7:0]RDY							
Access	HSC/R	HSC/R	HSC/R	HSC/R	HSC/R	HSC/R	HSC/R	HSC/R
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – AN[15:8]RDY Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
1	Channel conversion result is ready in the corresponding ADCBUFx register
0	Channel conversion result is not ready

Bits 7:0 – AN[7:0]RDY Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
1	Channel conversion result is ready in the corresponding ADCBUFx register
0	Channel conversion result is not ready

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14.3.13. ADC Data Ready Status Register High

Name: ADSTATH(1)
Offset: 0xB32

Note:

1. Bit availability is dependent on the number of supported ADC channels. Refer to Table 1 for ADC channel availability on package variants.

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			AN[21:16]RDY					
Access			HSC/R	HSC/R	HSC/R	HSC/R	HSC/R	HSC/R
Reset			0	0	0	0	0	0

Bits 5:0 – AN[21:16]RDY Common Interrupt Enable for Corresponding Analog Input bits

Value	Description
1	Channel conversion result is ready in the corresponding ADCBUFx register
0	Channel conversion result is not ready

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14.3.14. ADC Digital Comparator x Channel Enable Register Low (x = 0, 1, 2, 3)

Name: ADCMPxENL(1)
Offset: 0xB38, 0xB40, 0xB48, 0xB50

Note:

1. Bit availability is dependent on the number of supported ADC channels. Refer to Table 1 for ADC channel availability on package variants.

Bit	15	14	13	12	11	10	9	8
	CMPEN[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMPEN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMPEN[15:0] Comparator Enable for Corresponding Input Channel bits

Value	Description
1	Conversion result for corresponding channel is used by the comparator
0	Conversion result for corresponding channel is not used by the comparator

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14.3.15. ADC Digital Comparator x Channel Enable Register High (x = 0, 1, 2, 3)

Name: ADCMPxENH(1)
Offset: 0xB3A, 0xB42, 0xB4A, 0xB52

Note:

1. Bit availability is dependent on the number of supported ADC channels. Refer to Table 1 for ADC channel availability on package variants.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			CMPEN[21:16]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – CMPEN[21:16] Comparator Enable for Corresponding Input Channel bits

Value	Description
1	Conversion result for corresponding channel is used by the comparator
0	Conversion result for corresponding channel is not used by the comparator

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14.3.16. ADC Comparator x Threshold Low Register

Name: ADCMPxLO
Offset: 0xB3C, 0xB44, 0xB4C, 0xB54

Bit	15	14	13	12	11	10	9	8
	CMPLO[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMPLO[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMPLO[15:0] ADC Comparator Lower Threshold bits
The register stores the 16-bit low digital comparison values for use by the digital comparators.

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14.3.17. ADC Comparator x Threshold High Register

Name: ADCMPxHI
Offset: 0xB3E, 0xB46, 0xB4E, 0xB56

Bit	15	14	13	12	11	10	9	8
	CMPHI[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMPHI[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMPHI[15:0] ADC Comparator Upper Threshold bits
The register stores the 16-bit upper digital comparison values for use by the digital comparators.

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14.3.18. Oversampling Filter x Output Register (x = 0, 1, 2, 3)

Name: ADFLxDAT
Offset: 0xB68, 0xB6C, 0xB70, 0xB74

Bit	15	14	13	12	11	10	9	8
	FLDATA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FLDATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – FLDATA[15:0] 16-Bit Output Data from Oversampling Filters bits

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14.3.19. ADC Digital Filter x Control Register (x = 0, 1, 2, 3)

Name: ADFLxCON
Offset: 0xB6A, 0xB6E, 0xB72, 0xB76

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
	FLEN	MODE[1:0]		OVRSAM[2:0]			IE	RDY
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	HSC/R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				FLCHSEL[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 15 – FLEN Filter Enable bit

Value	Description
1	Filter is enabled.
0	Filter is disabled and the RDY bit is cleared.

Bits 14:13 – MODE[1:0] Filter Mode bits

Value	Description
11	Averaging mode
10	Reserved
01	Reserved
00	Oversampling mode

Bits 12:10 – OVRSAM[2:0] Filter Averaging/Oversampling Ratio bits

If MODE[1:0] = 00:
111 = 128x (16-bit result in the ADFLxDAT register is in 12.4 format)
110 = 32x (15-bit result in the ADFLxDAT register is in 12.3 format)
101 = 8x (14-bit result in the ADFLxDAT register is in 12.2 format)
100 = 2x (13-bit result in the ADFLxDAT register is in 12.1 format)
011 = 256x (16-bit result in the ADFLxDAT register is in 12.4 format)
010 = 64x (15-bit result in the ADFLxDAT register is in 12.3 format)
001 = 16x (14-bit result in the ADFLxDAT register is in 12.2 format)
000 = 4x (13-bit result in the ADFLxDAT register is in 12.1 format)
If MODE[1:0] = 11 (12-bit result in the ADFLxDAT register in all instances):
111 = 256x
110 = 128x
101 = 64x
100 = 32x
011 = 16x
010 = 8x
001 = 4x
000 = 2x

Bit 9 – IE Filter Common ADC Interrupt Enable bit

Value	Description
1	Common ADC interrupt will be generated when the filter result will be ready.

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Value	Description
0	Common ADC interrupt will not be generated for the filter.

Bit 8 – RDY Oversampling Filter Data Ready Flag bit
This bit is cleared by hardware when the result is read from the ADFLxDAT register.

Value	Description
1	Data in the ADFLxDAT register are ready.
0	The ADFLxDAT register has been read and new data in the ADFLxDAT register are not ready.

Bits 4:0 – FLCHSEL[4:0] Oversampling Filter Input Channel Selection bits

Value	Description
11111-10110	Reserved
10101	AN21 (Band gap 1.2V)
10100	AN20 (Temperature sensor)
10011	AN19
10010	AN18
10001	AN17
10000	AN16
01111	AN15
. . .	
00000	AN0

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14.3.20. ADC Channel Trigger 0 Selection Register Low

Name: ADTRIG0L
Offset: 0xB80

Bit	15	14	13	12	11	10	9	8
				TRGSRC1[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				TRGSRC0[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – TRGSRC1[4:0] Trigger Source Selection for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2
11100	CLC1
11011-11000	Reserved
10111	Input Capture/Output Compare 4
10110	Input Capture/Output Compare 3
10101	Input Capture/Output Compare 2
10100	Input Capture/Output Compare 1
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

Bits 4:0 – TRGSRC0[4:0] Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2

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Value	Description
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

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14.3.21. ADC Channel Trigger 0 Selection Register High

Name: ADTRIG0H
Offset: 0xB82

Bit	15	14	13	12	11	10	9	8
				TRGSRC3[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				TRGSRC2[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – TRGSRC3[4:0] Trigger Source Selection for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

Bits 4:0 – TRGSRC2[4:0] Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2

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Value	Description
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

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14.3.22. ADC Channel Trigger 1 Selection Registers Low

Name: ADTRIG1L
Offset: 0xB84

Bit	15	14	13	12	11	10	9	8
				TRGSRC5[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				TRGSRC4[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – TRGSRC5[4:0] Trigger Source Selection for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

Bits 4:0 – TRGSRC4[4:0] Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2

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Value	Description
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

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14.3.23. ADC Channel Trigger 1 Selection Register High

Name: ADTRIG1H
Offset: 0xB86

Bit	15	14	13	12	11	10	9	8
				TRGSRC7[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				TRGSRC6[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – TRGSRC7[4:0] Trigger Source Selection for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

Bits 4:0 – TRGSRC6[4:0] Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2

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Value	Description
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

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14.3.24. ADC Channel Trigger 2 Selection Registers Low

Name: ADTRIG2L
Offset: 0xB88

Bit	15	14	13	12	11	10	9	8
				TRGSRC9[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				TRGSRC8[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – TRGSRC9[4:0] Trigger Source Selection for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

Bits 4:0 – TRGSRC8[4:0] Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2

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Value	Description
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

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14.3.25. ADC Channel Trigger 2 Selection Register High

Name: ADTRIG2H
Offset: 0xB8A

Bit	15	14	13	12	11	10	9	8
				TRGSRC11[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				TRGSRC10[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – TRGSRC11[4:0] Trigger Source Selection for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

Bits 4:0 – TRGSRC10[4:0] Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2

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Value	Description
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

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14.3.26. ADC Channel Trigger 3 Selection Registers Low

Name: ADTRIG3L
Offset: 0xB8C

Bit	15	14	13	12	11	10	9	8
				TRGSRC13[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				TRGSRC12[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – TRGSRC13[4:0] Trigger Source Selection for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

Bits 4:0 – TRGSRC12[4:0] Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2

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Value	Description
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 Output Compare Trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

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14.3.27. ADC Channel Trigger 3 Selection Register High

Name: ADTRIG3H
Offset: 0xB8E

Bit	15	14	13	12	11	10	9	8
				TRGSRC15[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				TRGSRC14[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – TRGSRC15[4:0] Trigger Source Selection for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

Bits 4:0 – TRGSRC14[4:0] Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2

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Value	Description
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

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14.3.28. ADC Channel Trigger 4 Selection Registers Low

Name: ADTRIG4L
Offset: 0xB90

Bit	15	14	13	12	11	10	9	8
				TRGSRC17[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				TRGSRC16[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – TRGSRC17[4:0] Trigger Source Selection for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

Bits 4:0 – TRGSRC16[4:0] Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2

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Value	Description
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

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14.3.29. ADC Channel Trigger 4 Selection Register High

Name: ADTRIG4H
Offset: 0xB92

Bit	15	14	13	12	11	10	9	8
				TRGSRC19[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				TRGSRC18[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – TRGSRC19[4:0] Trigger Source Selection for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

Bits 4:0 – TRGSRC18[4:0] Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2

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Value	Description
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

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14.3.30. ADC Channel Trigger 5 Selection Registers Low

Name: ADTRIG5L
Offset: 0xB94

Bit	15	14	13	12	11	10	9	8
				TRGSRC21[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				TRGSRC20[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – TRGSRC21[4:0] Trigger Source Selection for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

Bits 4:0 – TRGSRC20[4:0] Common Interrupt Enable for Corresponding Analog Inputs bits

Value	Description
11111	ADTRG31 (PPS input)
11110	PTG
11101	CLC2

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Value	Description
11100	CLC1
11011-11000	Reserved
10111	SCCP4 output compare trigger
10110	SCCP3 output compare trigger
10101	SCCP2 output compare trigger
10100	SCCP1 output compare trigger
10011	Reserved
10010	CLC4
10001	CLC3
10000	Reserved
01111	SCCP4 trigger
01110	SCCP3 trigger
01101	SCCP2 trigger
01100	SCCP1 trigger
01011	PWM4 Trigger 2
01010	PWM4 Trigger 1
01001	PWM3 Trigger 2
01000	PWM3 Trigger 1
00111	PWM2 Trigger 2
00110	PWM2 Trigger 1
00101	PWM1 Trigger 2
00100	PWM1 Trigger 1
00011	Reserved
00010	Level software trigger
00001	Common software trigger
00000	No trigger is enabled

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14.3.31. ADC Digital Comparator x Control Register (x = 0, 1, 2, 3)

Name: ADCMPxCON
Offset: 0xBA0, 0xBA4, 0xBA8, 0xBAC

Legend: HC = Hardware Clearable bit; HS = Hardware Settable bit; HSC = Hardware Settable/ Clearable bit

Bit	15	14	13	12	11	10	9	8
				CHNL[4:0]				
Access				HSC/R	HSC/R	HSC/R	HSC/R	HSC/R
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMPEN	IE	STAT	BTWN	HIHI	HILO	LOHI	LOLO
Access	R/W	R/W	HS/HC/R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 12:8 – CHNL[4:0] Input Channel Number bits

Value	Description
11111	Reserved
. . .	
10101	Band gap, 1.2V (AN21)
10100	Temperature sensor (AN20)
10011	AN19
10010	AN18
10001	AN17
10000	AN16
01111	AN15
. . .	
00000	AN0

Bit 7 – CMPEN Comparator Enable bit

Value	Description
1	Comparator is enabled.
0	Comparator is disabled and the STAT status bit is cleared.

Bit 6 – IE Comparator Common ADC Interrupt Enable bit

Value	Description
1	ADC interrupt will be generated if the comparator detects a comparison event.
0	ADC interrupt will not be generated for the comparator.

Bit 5 – STAT Comparator Event Status bit
This bit is cleared by hardware when the channel number is read from the CHNL[4:0] bits.

Value	Description
1	A comparison event has been detected since the last read of the CHNL[4:0] bits.
0	A comparison event has not been detected since the last read of the CHNL[4:0] bits.

Bit 4 – BTWN Between Low/High Comparator Event bit

Value	Description
1	Generates a comparator event when ADCMPxLO ≤ ADCBUFx < ADCMPxHI.
0	Does not generate a digital comparator event when ADCMPxLO ≤ ADCBUFx < ADCMPxHI.

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Bit 3 – HIHI High/High Comparator Event bit

Value	Description
1	Generates a digital comparator event when ADCBUFx ≥ ADCMPxHI.
0	Does not generate a digital comparator event when ADCBUFx ≥ ADCMPxHI.

Bit 2 – HILO High/Low Comparator Event bit

Value	Description
1	Generates a digital comparator event when ADCBUFx < ADCMPxHI.
0	Does not generate a digital comparator event when ADCBUFx < ADCMPxHI.

Bit 1 – LOHI Low/High Comparator Event bit

Value	Description
1	Generates a digital comparator event when ADCBUFx ≥ ADCMPxLO.
0	Does not generate a digital comparator event when ADCBUFx ≥ ADCMPxLO.

Bit 0 – LOLO Low/Low Comparator Event bit

Value	Description
1	Generates a digital comparator event when ADCBUFx < ADCMPxLO.
0	Does not generate a digital comparator event when ADCBUFx < ADCMPxLO.

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14.3.32. ADC Level-Sensitive Trigger Control Register Low

Name: ADLVLTRGL
Offset: 0xBD0

Bit	15	14	13	12	11	10	9	8
	LVLEN[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LVLEN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – LVLEN[15:0] Level Trigger for Corresponding Analog Input Enable bits

Value	Description
1	Input trigger is level-sensitive.
0	Input trigger is edge-sensitive.

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14.3.33. ADC Level-Sensitive Trigger Control Register High

Name: ADLVLTRGH
Offset: 0xBD2

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			LVLEN[21:16]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – LVLEN[21:16] Level Trigger for Corresponding Analog Input Enable bits

Value	Description
1	Input trigger is level-sensitive.
0	Input trigger is edge-sensitive.

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14.3.34. ADC Early Interrupt Enable Register Low

Name: ADEIEL
Offset: 0xBF0

Bit	15	14	13	12	11	10	9	8
	EIEN[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	EIEN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – EIEN[15:0] Early Interrupt Enable for Corresponding Analog Input bits

Value	Description
1	Early interrupt is enabled for the channel.
0	Early interrupt is disabled for the channel.

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14.3.35. ADC Early Interrupt Enable Register High

Name: ADEIEH
Offset: 0xBF2

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			EIEN[21:16]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – EIEN[21:16] Early Interrupt Enable for Corresponding Analog Input bits

Value	Description
1	Early interrupt is enabled for the channel.
0	Early interrupt is disabled for the channel.

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14.3.36. ADC Early Interrupt Status Register Low

Name: ADEISTATL
Offset: 0xBF8

Bit	15	14	13	12	11	10	9	8
	EISTAT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	EISTAT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – EISTAT[15:0] Early Interrupt Status for Corresponding Analog Input bits

Value	Description
1	Early interrupt was generated.
0	Early interrupt was not generated since the last ADCBUFx read.

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14.3.37. ADC Early Interrupt Status Register High

Name: ADEISTATH
Offset: 0xBFA

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			EISTAT[21:16]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – EISTAT[21:16] Early Interrupt Status for Corresponding Analog Input bits

Value	Description
1	Early interrupt was generated.
0	Early interrupt was not generated since the last ADCBUFx read.

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14.3.38. ADC Control Register 5 Low

Name: ADCON5L
Offset: 0xC00

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
	SHRRDY							
Access	R/HSC							
Reset	0							

Bit	7	6	5	4	3	2	1	0
	SHRPWR							
Access	R/W							
Reset	0							

Bit 15 – SHRRDY Shared ADC Core Ready Flag bit

Value	Description
1	ADC core is powered and ready for operation.
0	ADC core is not ready for operation.

Bit 7 – SHRPWR Shared ADC Core Power Enable bit

Value	Description
1	ADC core is powered.
0	ADC core is off.

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14.3.39. ADC Control Register 5 High

Name: ADCON5H
Offset: 0xC02

Bit	15	14	13	12	11	10	9	8
					WARMTIME[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SHRCIE							
Access	R/W							
Reset	0							

Bits 11:8 – WARMTIME[3:0] ADC Shared Core Power-up Delay bits
These bits determine the power-up delay in the number of the Core Source Clock Periods ($T_{CORESRC}$) for all ADC cores.

Value	Description
1111	32768 Source Clock Periods
1110	16384 Source Clock Periods
1101	8192 Source Clock Periods
1100	4096 Source Clock Periods
1011	2048 Source Clock Periods
1010	1024 Source Clock Periods
1001	512 Source Clock Periods
1000	256 Source Clock Periods
0111	128 Source Clock Periods
0110	64 Source Clock Periods
0101	32 Source Clock Periods
0100	16 Source Clock Periods
00xx	16 Source Clock Periods

Bit 7 – SHRCIE Shared ADC Core Ready Common Interrupt Enable bit

Value	Description
1	Common interrupt will be generated when ADC core is powered and ready for operation.
0	Common interrupt is disabled for an ADC core ready event.

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14.3.40. ADC Buffer x Register

Name: ADCBUFx
Offset: 0xC0C, 0xC0E, 0xC10, 0xC12, 0xC14, 0xC16, 0xC18, 0xC1A, 0xC1C, 0xC1E, 0xC20, 0xC22, 0xC24, 0xC26, 0xC28, 0xC2A, 0xC2C, 0xC2E, 0xC30, 0xC32, 0xC34, 0xC36

Bit	15	14	13	12	11	10	9	8
	ADCBUFx[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADCBUFx[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADCBUFx[15:0] Buffer Data bits

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15. High-Speed Analog Comparator with Slope Compensation DAC

Notes:

1. This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"High-Speed Analog Comparator Module"** (www.microchip.com/DS70005280) in the *"dsPIC33/PIC24 Family Reference Manual"*.
2. Some registers and associated bits described in this section may not be available on all devices. Refer to Memory Organization in this data sheet for device-specific register and bit information.

The high-speed analog comparator module provides a method to monitor voltage, current and other critical signals in a power conversion application that may be too fast for the CPU and ADC to capture. The analog comparator module can be used to implement Peak Current mode control, Critical Conduction mode (variable frequency) and Hysteretic Control mode. Figure 15-1 shows an overview of the comparator/DAC module.

15.1. Overview

The high-speed analog comparator module is comprised of a high-speed comparator, Pulse Density Modulation (PDM) DAC and a slope compensation unit. The slope compensation unit provides a user-defined slope which can be used to alter the DAC output. This feature is useful in applications, such as Peak Current mode control, where slope compensation is required to maintain the stability of the power supply. The user simply specifies the direction and rate of change for the slope compensation and the output of the DAC is modified accordingly.

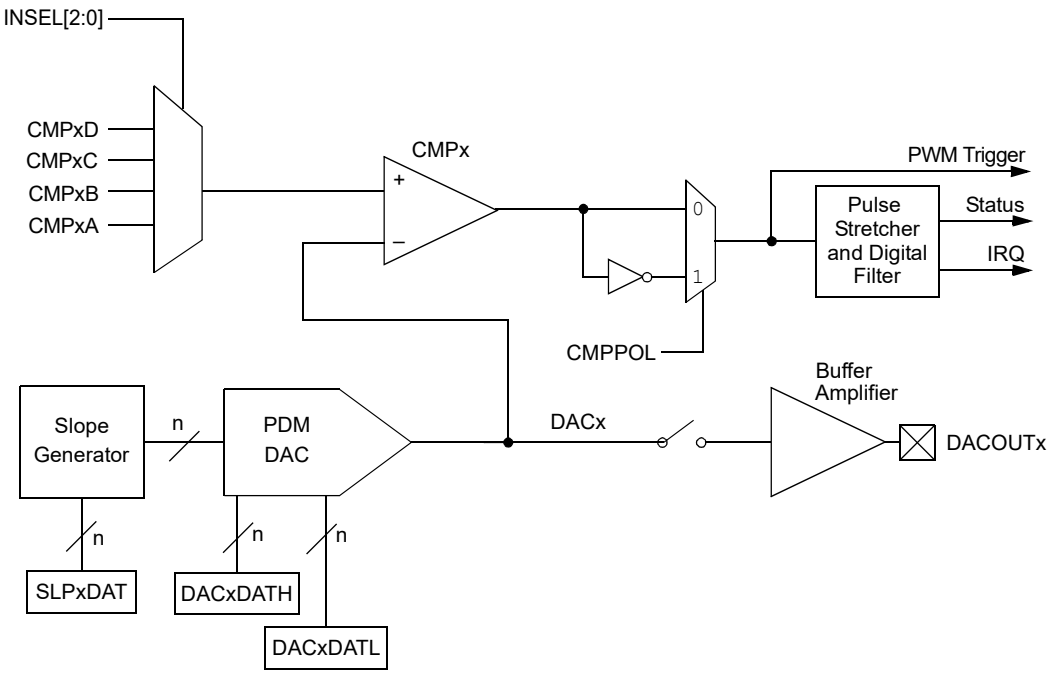
The DAC consists of a PDM unit, followed by a digitally controlled multiphase RC filter. The PDM unit uses a phase accumulator circuit to generate an output stream of pulses. The density of the pulse stream is proportional to the input data value, relative to the maximum value supported by the bit width of the accumulator. The output pulse density is representative of the desired output voltage. The pulse stream is filtered with an RC filter to yield an analog voltage. The output of the DAC is connected to the negative input of the comparator. The positive input of the comparator can be selected using a MUX from the input pins. The comparator provides a high-speed operation with a typical delay of 15 ns.

The output of the comparator is processed by the pulse stretcher and the digital filter blocks, which prevent comparator response to unintended fast transients in the inputs. Figure 15-1 shows a block diagram of the high-speed analog comparator module. The DAC module can be operated in one of three modes: Slope Generation mode, Hysteretic mode and Triangle Wave mode. Each of these modes can be used in a variety of power supply applications.

Note: The DACOUT1 pin can only be associated with a single DAC output at any given time. If more than one DACOEN bit is set, the DACOUT1 pin will be a combination of the signals.

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Figure 15-1. High-Speed Analog Comparator Module Block Diagram



Note: n = 16

15.2. Features Overview

- Two Rail-to-Rail Analog Comparators
- Four Selectable Input Sources per Comparator
- Programmable Comparator Hysteresis
- Programmable Output Polarity
- Interrupt Generation Capability
- Dedicated Pulse Density Modulation DAC for Each Analog Comparator:
  - PDM unit followed by a digitally controlled multimode multipole RC filter
- Multimode Multipole RC Output Filter:
  - Transition mode: Provides the fastest response
  - Fast mode: For tracking DAC slopes
  - Steady-State mode: Provides 12-bit resolution
- Slope Compensation Along With Each DAC:
  - Slope Generation mode
  - Hysteretic Control mode
  - Triangle Wave mode
- Functional Support for the High-Speed PWM Module Which Includes:
  - PWM duty cycle control
  - PWM period control
  - PWM Fault detect

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15.3. DAC Control Registers

The DACCTRL1L and DACCTRL2H/L registers are common configuration registers for DAC modules. The DACxCON, DACxDAT, SLPxCON and SLPxDAT registers specify the operation of individual modules.

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15.4. DAC Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0C80	DACCTRL1L	15:8	DACON		DACSIDL					
		7:0	CLKSEL[1:0]		CLKDIV[1:0]			FCLKDIV[2:0]		
0x0C82 ... 0x0C83	Reserved									
0x0C84	DACCTRL2L	15:8							TMODTIME[9:8]	
		7:0	TMODTIME[7:0]							
0x0C86	DACCTRL2H	15:8							SSTIME[9:8]	
		7:0	SSTIME[7:0]							
0x0C88	DAC0CONL	15:8	DACEN	IRQM[1:0]				CBE	DACOEN	FLTREN
		7:0	CMPSTAT	CMPPOL	INSEL[2:0]			HYSPOL	HYSSEL[1:0]	
0x0C8A	DAC0CONH	15:8							TMCB[9:8]	
		7:0	TMCB[7:0]							
0x0C8C	DAC0DATL	15:8					DACLOW[11:8]			
		7:0	DACLOW[7:0]							
0x0C8E	DAC0DATH	15:8					DACDAT[11:8]			
		7:0	DACDAT[7:0]							
0x0C90	SLP0CONL	15:8	HCFSEL[3:0]				SLPSTOPA[3:0]			
		7:0	SLPSTOPB[3:0]				SLPSTRT[3:0]			
0x0C92	SLP0CONH	15:8	SLOPEN				HME	TWME	PSE	
		7:0								
0x0C94	SLP0DAT	15:8	SLPDAT[15:8]							
		7:0	SLPDAT[7:0]							
0x0C96 ... 0x0C97	Reserved									
0x0C98	DAC1CONL	15:8	DACEN	IRQM[1:0]				CBE	DACOEN	FLTREN
		7:0	CMPSTAT	CMPPOL	INSEL[2:0]			HYSPOL	HYSSEL[1:0]	
0x0C9A	DAC1CONH	15:8							TMCB[9:8]	
		7:0	TMCB[7:0]							
0x0C9C	DAC1DATL	15:8					DACLOW[11:8]			
		7:0	DACLOW[7:0]							
0x0C9E	DAC1DATH	15:8					DACDAT[11:8]			
		7:0	DACDAT[7:0]							
0x0CA0	SLP1CONL	15:8	HCFSEL[3:0]				SLPSTOPA[3:0]			
		7:0	SLPSTOPB[3:0]				SLPSTRT[3:0]			
0x0CA2	SLP1CONH	15:8	SLOPEN				HME	TWME	PSE	
		7:0								
0x0CA4 ... 0xCA41	Reserved									
0xCA42	SLP1DAT	15:8	SLPDAT[15:8]							
		7:0	SLPDAT[7:0]							

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15.4.1. DAC Control 1 Low Register

Name: DACCTRL1L
Offset: 0xC80

Notes:

1. These bits should only be changed when DACON = 0 to avoid unpredictable behavior.
2. The input clock to this divider is the selected clock input, CLKSEL[1:0], and then divided by two.
3. Clock source and dividers should yield an effective DAC clock input as specified in Table 34-35.

Bit	15	14	13	12	11	10	9	8
	DACON		DACSIDL					
Access	R/W		R/W					
Reset	0		0					

Bit	7	6	5	4	3	2	1	0
	CLKSEL[1:0]		CLKDIV[1:0]			FCLKDIV[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit 15 – DACON Common DAC Module Enable bit

Value	Description
1	Enables DAC modules
0	Disables DAC modules and disables FSCM clocks to reduce power consumption; any pending Slope mode and/or underflow conditions are cleared

Bit 13 – DACSIDL DAC Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bits 7:6 – CLKSEL[1:0] DAC Clock Source Select bits(1,3)

Value	Description
11	F_{PLLO}
10	$F_{VCO}/3$
01	$F_{VCO}/2$
00	VCO divider output

Bits 5:4 – CLKDIV[1:0] DAC Clock Divider bits(1,3)

Value	Description
11	Divide-by-4
10	Divide-by-3 (non-uniform duty cycle)
01	Divide-by-2
00	1x

Bits 2:0 – FCLKDIV[2:0] Comparator Filter Clock Divider bits(2)

Value	Description
111	Divide-by-8
110	Divide-by-7
101	Divide-by-6
100	Divide-by-5

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Value	Description
011	Divide-by-4
010	Divide-by-3
001	Divide-by-2
000	1x

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15.4.2. DAC Control 2 Low Register

Name: DACCTRL2L
Offset: 0xC84

Note:

1. The value for TMODTIME[9:0] should be less than the SSTIME[9:0] value.

Bit	15	14	13	12	11	10	9	8
							TMODTIME[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	TMODTIME[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – TMODTIME[9:0] Transition Mode Duration bits(1)

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15.4.3. DAC Control 2 High Register

Name: DACCTRL2H
Offset: 0xC86

Note:

1. The value for SSTIME[9:0] should be greater than the TMODTIME[9:0] value.

Bit	15	14	13	12	11	10	9	8
							SSTIME[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	SSTIME[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – SSTIME[9:0] Time from Start of Transition Mode until Steady-State Filter is Enabled bits(1)

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15.4.4. DACx Control Low Register

Name: DACxCONL
Offset: 0xC88, 0xC98

Notes:
1. Changing these bits during operation may generate a spurious interrupt.
2. The edge selection is a post-polarity selection via the CMPPOL bit.

Bit	15	14	13	12	11	10	9	8
	DACEN	IRQM[1:0]				CBE	DACOEN	FLTREN
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bit	7	6	5	4	3	2	1	0
	CMPSTAT	CMPPOL	INSEL[2:0]			HYSPOL	HYSSEL[1:0]	
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – DACEN Individual DACx Module Enable bit

Value	Description
1	Enables DACx module
0	Disables DACx module to reduce power consumption; any pending Slope mode and/or underflow conditions are cleared

Bits 14:13 – IRQM[1:0] Interrupt Mode Select bits(1,2)

Value	Description
11	Generates an interrupt on either a rising or falling edge detect
10	Generates an interrupt on a falling edge detect
01	Generates an interrupt on a rising edge detect
00	Interrupts are disabled

Bit 10 – CBE Comparator Blank Enable bit

Value	Description
1	Enables the analog comparator output to be blanked (gated off) during the recovery transition following the completion of a slope operation
0	Disables the blanking signal to the analog comparator; therefore, the analog comparator output is always active

Bit 9 – DACOEN DACx Output Buffer Enable bit

Value	Description
1	DACx analog voltage is connected to the DACOUT1 pin
0	DACx analog voltage is not connected to the DACOUT1 pin

Bit 8 – FLTREN Comparator Digital Filter Enable bit

Value	Description
1	Digital filter is enabled
0	Digital filter is disabled

Bit 7 – CMPSTAT Comparator Status bit
The current state of the comparator output including the CMPPOL selection.

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Bit 6 – CMPPOL Comparator Output Polarity Control bit

Value	Description
1	Output is inverted
0	Output is noninverted

Bits 5:3 – INSEL[2:0] Comparator Input Source Select bits

Value	Description
111	Reserved
110	Reserved
101	Reserved
100	Reserved
011	CMPxD input pin
010	CMPxC input pin
001	CMPxB input pin
000	CMPxA input pin

Bit 2 – HYSPOL Comparator Hysteresis Polarity Select bit

Value	Description
1	Hysteresis is applied to the falling edge of the comparator output
0	Hysteresis is applied to the rising edge of the comparator output

Bits 1:0 – HYSSEL[1:0] Comparator Hysteresis Select bits

Value	Description
11	45 mv hysteresis
10	30 mv hysteresis
01	15 mv hysteresis
00	No hysteresis is selected

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15.4.5. DACx Control High Register

Name: DACxCONH
Offset: 0xC8A, 0xC9A

Bit	15	14	13	12	11	10	9	8
							TMCB[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	TMCB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – TMCB[9:0] DACx Leading-Edge Blanking bits
These register bits specify the blanking period for the comparator, following changes to the DAC output during Change-of-State (COS), for the input signal selected by the HCFSEL[3:0] bits in SLPxCONL.

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15.4.6. DACx Data Low Register

Name: DACxDATL
Offset: 0xC8C, 0xC9C

Bit	15	14	13	12	11	10	9	8
					DACLOW[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DACLOW[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – DACLOW[11:0] DACx Low Data bits
In Hysteretic mode, Slope Generator mode and Triangle mode, this register specifies the low data value and/or limit for the DACx module. Valid values are from 205 to 3890.

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15.4.7. DACx Data High Register

Name: DACxDATH
Offset: 0xC8E, 0xC9E

Bit	15	14	13	12	11	10	9	8
					DACDAT[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DACDAT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – DACDAT[11:0] DACx High Data bits
This register specifies the high DACx data value. Valid values are from 205 to 3890.

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15.4.8. DACx Slope Control Low Register

Name: SLPxCONL
Offset: 0xC90, 0xCA0

Bit	15	14	13	12	11	10	9	8
	HCFSEL[3:0]				SLPSTOPA[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SLPSTOPB[3:0]				SLPSTRT[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:12 – HCFSEL[3:0] Hysteretic Comparator Function Input Select bits
The selected input signal controls the switching between the DACx high limit (DACxDATH) and the DACx low limit (DACxDATL) as the data source for the PDM DAC. It modifies the polarity of the comparator, and the rising and falling edges initiate the start of the LEB counter (TMCB[9:0] bits in DACxCONH).

Input Selection	Source
1111	1
1110-0101	0
0100	PWM4H
0011	PWM3H
0010	PWM2H
0001	PWM1H
0000	0

Bits 11:8 – SLPSTOPA[3:0] Slope Stop A Signal Select bits
The selected Slope Stop A signal is logically OR'd with the selected Slope Stop B signal to terminate the slope function.

Slope Stop A Signal Selection	Source
1111	1
1110-0101	0
0100	PWM4 Trigger 2
0011	PWM3 Trigger 2
0010	PWM2 Trigger 2
0001	PWM1 Trigger 2
0000	0

Bits 7:4 – SLPSTOPB[3:0] Slope Stop B Signal Select bits
The selected Slope Stop B signal is logically OR'd with the selected Slope Stop A signal to terminate the slope function.

Slope Stop B Signal Selection	Source
1111	1
1110-0011	0
0010	CMP2 out
0001	CMP1 out
0000	0

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Bits 3:0 – SLPSTRT[3:0] Slope Start Signal Select bits

Slope Start Signal Selection	Source
1111	1
1110-0101	0
0100	PWM4 Trigger 1
0011	PWM3 Trigger 1
0010	PWM2 Trigger 1
0001	PWM1 Trigger 1
0000	0

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15.4.9. DACx Slope Control High Register

Name: SLPxCONH
Offset: 0xC92, 0xCA2

Notes:

1. HME mode requires the user to disable the slope function (SLOPEN = 0).
2. TWME mode requires the user to enable the slope function (SLOPEN = 1).

Bit	15	14	13	12	11	10	9	8
	SLOPEN				HME	TWME	PSE	
Access	R/W				R/W	R/W	R/W	
Reset	0				0	0	0	

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – SLOPEN Slope Function Enable/On bit

Value	Description
1	Enables slope function.
0	Disables slope function; slope accumulator is disabled to reduce power consumption.

Bit 11 – HME Hysteretic Mode Enable bit(1)

Value	Description
1	Enables Hysteretic mode for DACx.
0	Disables Hysteretic mode for DACx.

Bit 10 – TWME Triangle Wave Mode Enable bit(2)

Value	Description
1	Enables Triangle Wave mode for DACx.
0	Disables Triangle Wave mode for DACx.

Bit 9 – PSE Positive Slope Mode Enable bit

Value	Description
1	Slope mode is positive (increasing).
0	Slope mode is negative (decreasing).

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15.4.10. DACx Slope Data Register

Name: SLPxDAT
Offset: 0xC94, 0xCA42

Bit	15	14	13	12	11	10	9	8
	SLPDAT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SLPDAT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – SLPDAT[15:8] Slope Ramp Rate Value bits
The SLPDATx value is in 12.4 format.

Bits 7:0 – SLPDAT[7:0] Slope Ramp Rate Value bits
The SLPDATx value is in 12.4 format.

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16. Quadrature Encoder Interface (QEI)

Notes:

1. This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive resource. For more information, refer to **"Quadrature Encoder Interface (QEI)"** (www.microchip.com/DS70000601) in the *"dsPIC33/PIC24 Family Reference Manual"*.
2. Some registers and associated bits described in this section may not be available on all devices. Refer to Memory Organization in this data sheet for device-specific register and bit information.

The Quadrature Encoder Interface (QEI) module provides the interface to incremental encoders for obtaining mechanical position data. Quadrature Encoders, also known as incremental encoders or optical encoders, detect position and speed of rotating motion systems. Quadrature Encoders enable closed-loop control of motor control applications, such as Switched Reluctance (SR) and AC Induction Motors (ACIM).

A typical Quadrature Encoder includes a slotted wheel attached to the shaft of the motor and an emitter/detector module that senses the slots in the wheel. Typically, three output channels, Phase A (QEAx), Phase B (QEBx) and Index (INDXx), provide information on the movement of the motor shaft, including distance and direction.

The two channels, Phase A (QEAx) and Phase B (QEBx), are typically 90 degrees out of phase with respect to each other. The Phase A and Phase B channels have a unique relationship. If Phase A leads Phase B, the direction of the motor is deemed positive or forward. If Phase A lags Phase B, the direction of the motor is deemed negative or reverse. The Index pulse occurs once per mechanical revolution and is used as a reference to indicate an absolute position. Figure 16-1 illustrates the Quadrature Encoder Interface signals.

The Quadrature signals from the encoder can have four unique states ('01', '00', '10' and '11') that reflect the relationship between QEAx and QEBx. Figure 16-1 illustrates these states for one count cycle. The order of the states gets reversed when the direction of travel changes.

The Quadrature Decoder increments or decrements the 32-bit up/down Position x Counter (POSxCNTH/L) registers for each Change-of-State (COS). The counter increments when QEAx leads QEBx and decrements when QEBx leads QEAx. Table 16-1 shows an overview of the QEI module.

Figure 16-1. Quadrature Encoder Interface Signals

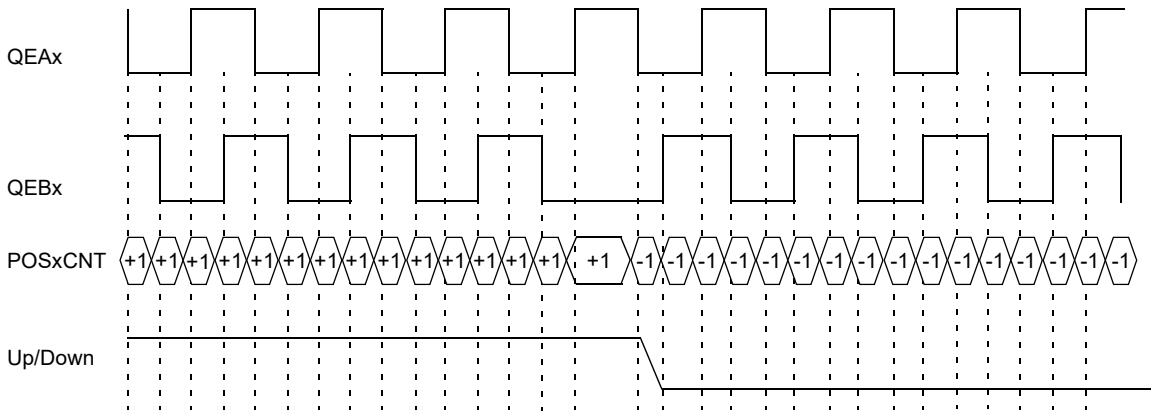


Table 16-1 shows the truth table that describes how the Quadrature signals are decoded.

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Table 16-1. Truth Table For Quadrature Encoder

Current Quadrature State		Previous Quadrature State		Action
QA	QB	QA	QB	
1	1	1	1	No count or direction change
1	1	1	0	Count up
1	1	0	1	Count down
1	1	0	0	Invalid state change; ignore
1	0	1	1	Count down
1	0	1	0	No count or direction change
1	0	0	1	Invalid state change; ignore
1	0	0	0	Count up
0	1	1	1	Count up
0	1	1	0	Invalid state change; ignore
0	1	0	1	No count or direction change
0	1	0	0	Count down
0	0	1	1	Invalid state change; ignore
0	0	1	0	Count down
0	0	0	1	Count up
0	0	0	0	No count or direction change

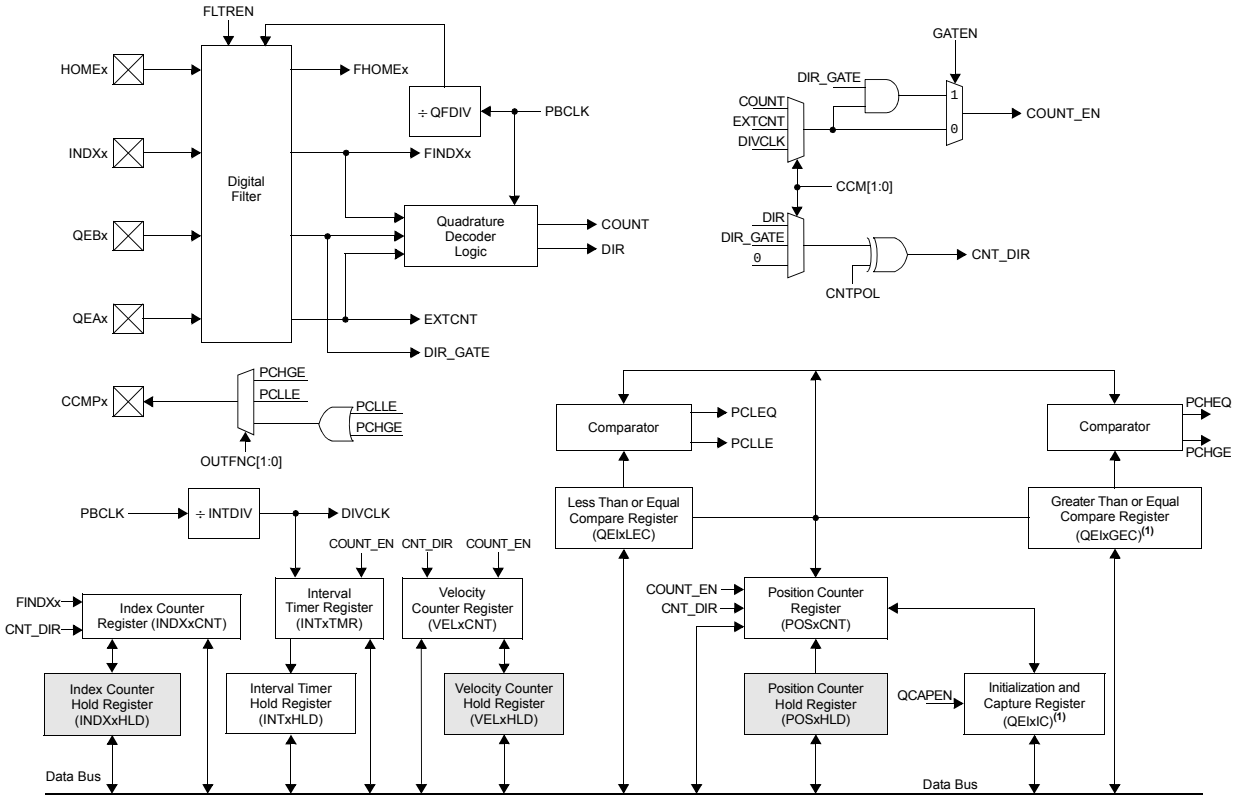
Figure 16-2 illustrates the simplified block diagram of the QEI module. The QEI module consists of decoder logic to interpret the Phase A (QEAx) and Phase B (QEBx) signals, and an up/down counter to accumulate the count. The counter pulses are generated when the Quadrature state changes. The count direction information must be maintained in a register until a direction change is detected. The module also includes digital noise filters, which condition the input signal.

The QEI module consists of the following major features:

- Four Input Pins: Two Phase Signals, an Index Pulse and a Home Pulse
- Programmable Digital Noise Filters on Inputs
- Quadrature Decoder providing Counter Pulses and Count Direction
- Count Direction Status
- 4x Count Resolution
- Index (INDXx) Pulse to Reset the Position Counter
- General Purpose 32-Bit Timer/Counter mode
- Interrupts generated by QEI or Counter Events
- 32-Bit Velocity Counter
- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 32-Bit Position Initialization/Capture Register
- 32-Bit Compare Less Than and Greater Than Registers
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Interval Timer mode

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Figure 16-2. Quadrature Encoder Interface (QEI) Module Block Diagram



Note 1: These registers map to the same memory location.
2: Shaded registers are not used in 32-bit devices. They are provided to maintain uniformity with 16-bit architecture.

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16.1. QEI Control/Status Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0140	QEI1CON	15:8	QEIEN		QEISIDL		PIMOD[2:0]		IMV[1:0]	
		7:0		INTDIV[2:0]			CNTPOL	GATEN	CCM[1:0]	
0x0142 ... 0x0143	Reserved									
0x0144	QEI1IOC	15:8	QCAPEN	FLTREN	QFDIV[2:0]			OUTFNC[1:0]		SWPAB
		7:0	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA
0x0146	QEI1IOCH	15:8								
		7:0								HCAPEN
0x0148	QEI1STAT	15:8			PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
		7:0	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
0x014A ... 0x014B	Reserved									
0x014C	POS1CNTL	15:8	POSCNT[15:8]							
		7:0	POSCNT[7:0]							
0x014E	POS1CNTH	15:8	POSCNT[31:24]							
		7:0	POSCNT[23:16]							
0x0150	POS1HLDL	15:8	POSHLD[15:8]							
		7:0	POSHLD[7:0]							
0x0152	POS1HLD	15:8	POSHLDH[31:24]							
		7:0	POSHLDH[23:16]							
0x0154	VEL1CNTL	15:8	VELCNT[15:8]							
		7:0	VELCNT[7:0]							
0x0156	VEL1CNTH	15:8	VELCNT[31:24]							
		7:0	VELCNT[23:16]							
0x0158	VEL1HLDL	15:8	VELHLD[15:8]							
		7:0	VELHLD[7:0]							
0x015A	VEL1HLDH	15:8	VELHLDH[31:24]							
		7:0	VELHLDH[23:16]							
0x015C	INT1TMRL	15:8	INTTMR[15:8]							
		7:0	INTTMR[7:0]							
0x015E	INT1TMRH	15:8	INTTMR[31:24]							
		7:0	INTTMR[23:16]							
0x0160	INT1HLDL	15:8	INTXHLD[15:8]							
		7:0	INTXHLD[7:0]							
0x0162	INT1HLDH	15:8	INTHLD[31:24]							
		7:0	INTHLD[23:16]							
0x0164	INDX1CNTL	15:8	INDXCNT[15:8]							
		7:0	INDXCNT[7:0]							
0x0166	INDX1CNTH	15:8	INDXCNT[31:24]							
		7:0	INDXCNT[23:16]							
0x0168	INDX1HLDL	15:8	INDXHLD[15:8]							
		7:0	INDXHLD[7:0]							
0x016A	INDX1HLDH	15:8	INDXHLDH[31:24]							
		7:0	INDXHLDH[23:16]							
0x016C	QEI1GECL	15:8	QEIGEC[15:8]							
		7:0	QEIGEC[7:0]							
0x016E	QEI1GECH	15:8	QEIGEC[31:24]							
		7:0	QEIGEC[23:16]							
0x0170	QEI1LECL	15:8	QEILEC[15:8]							
		7:0	QEILEC[7:0]							
0x0172	QEI1LECH	15:8	QEILEC[31:24]							
		7:0	QEILEC[23:16]							

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16.1.1. QEI1 Control Register

Name: QEI1CON
Offset: 0x140

Notes:

1. When CCMx = 10 or CCMx = 11, all of the QEI counters operate as timers and the PIMOD[2:0] bits are ignored.
2. When CCMx = 00, and QEAx and QEBx values match the Index Match Value (IMV), the POSxCNTH and POSxCNTL registers are reset.
3. The selected clock rate should be at least twice the expected maximum quadrature count rate.
4. Not all devices support this mode.
5. The QCAPEN and HCAPEN bits must be cleared during PIMODx Modes 2 through 7 to ensure proper functionality. Not all devices support HCAPEN.

Bit	15	14	13	12	11	10	9	8
	QEIEN		QEISIDL	PIMOD[2:0]			IMV[1:0]	
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		INTDIV[2:0]			CNTPOL	GATEN	CCM[1:0]	
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit 15 – QEIEN Quadrature Encoder Interface Module Enable bit

Value	Description
1	Module counters are enabled
0	Module counters are disabled, but SFRs can be read or written

Bit 13 – QEISIDL QEI Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bits 12:10 – PIMOD[2:0] Position Counter Initialization Mode Select bits(1,5)

Value	Description
111	Modulo Count mode for position counter and every Index event resets the position counter(4)
110	Modulo Count mode for position counter
101	Resets the position counter when the position counter equals the QEIxGEC register
100	Second Index event after Home event initializes the position counter with the contents of the QEIxIC register
011	First Index event after Home event initializes the position counter with the contents of the QEIxIC register
010	Next Index input event initializes the position counter with the contents of the QEIxIC register
001	Every Index input event resets the position counter
000	Index input event does not affect the position counter

Bits 9:8 – IMV[1:0] Index Match Value bits(2)

Value	Description
11	Index match occurs when QEBx = 1 and QEAx = 1
10	Index match occurs when QEBx = 1 and QEAx = 0

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Value	Description
01	Index match occurs when QEBx = 0 and QEAx = 1
00	Index match occurs when QEBx = 0 and QEAx = 0

Bits 6:4 – INTDIV[2:0] Timer Input Clock Prescale Select bits(3) (interval timer, main timer (position counter), velocity counter and Index counter internal clock divider select)

Value	Description
111	1:128 prescale value
110	1:64 prescale value
101	1:32 prescale value
100	1:16 prescale value
011	1:8 prescale value
010	1:4 prescale value
001	1:2 prescale value
000	1:1 prescale value

Bit 3 – CNTPOL Position and Index Counter/Timer Direction Select bit

Value	Description
1	Counter direction is negative unless modified by an external up/down signal
0	Counter direction is positive unless modified by an external up/down signal

Bit 2 – GATEN External Count Gate Enable bit

Value	Description
1	External gate signal controls position counter operation
0	External gate signal does not affect position counter operation

Bits 1:0 – CCM[1:0] Counter Control Mode Selection bits

Value	Description
11	Internal Timer mode
10	External Clock Count with External Gate mode
01	External Clock Count with External Up/Down mode
00	Quadrature Encoder mode

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16.1.2. QEI1 I/O Control Register

Name: QEI1IOC
Offset: 0x144

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
	QCAPEN	FLTREN	QFDIV[2:0]			OUTFNC[1:0]		SWPAB
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA
Access	R/W	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	x	x	x	x

Bit 15 – QCAPEN QEIx Position Counter Input Capture Enable bit

Value	Description
1	Index match event (positive edge) triggers a position capture event (HCAPEN must be cleared)
0	Index match event (positive edge) does not trigger a position capture event

Bit 14 – FLTREN QEAx/QEBx/INDXx/HOMEx Digital Filter Enable bit

Value	Description
1	Input pin digital filter is enabled
0	Input pin digital filter is disabled (bypassed)

Bits 13:11 – QFDIV[2:0] QEAx/QEBx/INDXx/HOMEx Digital Input Filter Clock Divide Select bits

Value	Description
111	1:256 clock divide
110	1:64 clock divide
101	1:32 clock divide
100	1:16 clock divide
011	1:8 clock divide
010	1:4 clock divide
001	1:2 clock divide
000	1:1 clock divide

Bits 10:9 – OUTFNC[1:0] QEIx Module Output Function Mode Select bits

Value	Description
11	The CNTCMPx pin goes high when POSxCNT ≤ QEIxLEC or POSxCNT ≥ QEIxGEC
10	The CNTCMPx pin goes high when POSxCNT ≤ QEIxLEC
01	The CNTCMPx pin goes high when POSxCNT ≥ QEIxGEC
00	Output is disabled

Bit 8 – SWPAB Swap QEAx and QEBx Inputs bit

Value	Description
1	QEAx and QEBx are swapped prior to Quadrature Decoder logic
0	QEAx and QEBx are not swapped

Bit 7 – HOMPOL HOMEx Input Polarity Select bit

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Value	Description
1	Input is inverted
0	Input is not inverted

Bit 6 – IDXPOL INDXx Input Polarity Select bit

Value	Description
1	Input is inverted
0	Input is not inverted

Bit 5 – QEBPOL QEBx Input Polarity Select bit

Value	Description
1	Input is inverted
0	Input is not inverted

Bit 4 – QEAPOL QEAx Input Polarity Select bit

Value	Description
1	Input is inverted
0	Input is not inverted

Bit 3 – HOME Status of HOMEx Input Pin After Polarity Control bit (read-only)

Value	Description
1	Pin is at logic '1' if HOMPOL bit is set to '0'; Pin is at logic '0' if HOMPOL bit is set to '1'
0	Pin is at logic '0' if HOMPOL bit is set to '0'; Pin is at logic '1' if HOMPOL bit is set to '1'

Bit 2 – INDEX Status of INDXx Input Pin After Polarity Control bit (read-only)

Value	Description
1	Pin is at logic '1' if the IDXPOL bit is set to '0'; Pin is at logic '0' if the IDXPOL bit is set to '1'
0	Pin is at logic '0' if the IDXPOL bit is set to '0'; Pin is at logic '1' if the IDXPOL bit is set to '1'

Bit 1 – QEB Status of QEBx Input Pin After Polarity Control and SWPAB Pin Swapping bit (read-only)

Value	Description
1	Physical pin, QEBx, is at logic '1' if QEBPOL bit is set to '0' and SWPAB bit is set to '0'; physical pin, QEBx, is at logic '0' if QEBPOL bit is set to '1' and SWPAB bit is set to '0'; physical pin, QEAx, is at logic '1' if QEBPOL bit is set to '0' and SWPAB bit is set to '1'; physical pin, QEAx, is at logic '0' if QEBPOL bit is set to '1' and SWPAB bit is set to '1'
0	Physical pin, QEBx, is at logic '0' if QEBPOL bit is set to '0' and SWPAB bit is set to '0'; physical pin, QEBx, is at logic '1' if QEBPOL bit is set to '1' and SWPAB bit is set to '0'; physical pin, QEAx, is at logic '0' if QEBPOL bit is set to '0' and SWPAB bit is set to '1'; physical pin, QEAx, is at logic '1' if QEBPOL bit is set to '1' and SWPAB bit is set to '1'

Bit 0 – QEA Status of QEAx Input Pin After Polarity Control and SWPAB Pin Swapping bit (read-only)

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Value	Description
1	Physical pin, QEAx, is at logic '1' if QEAPOL bit is set to '0' and SWPAB bit is set to '0'; physical pin, QEAx, is at logic '0' if QEAPOL bit is set to '1' and SWPAB bit is set to '0'; physical pin, QEBx, is at logic '1' if QEAPOL bit is set to '0' and SWPAB bit is set to '1'; physical pin, QEBx, is at logic '0' if QEAPOL bit is set to '1' and SWPAB bit is set to '1'
0	Physical pin, QEAx, is at logic '0' if QEAPOL bit is set to '0' and SWPAB bit is set to '0'; physical pin, QEAx, is at logic '1' if QEAPOL bit is set to '1' and SWPAB bit is set to '0'; physical pin, QEBx, is at logic '0' if QEAPOL bit is set to '0' and SWPAB bit is set to '1'; physical pin, QEBx, is at logic '1' if QEAPOL bit is set to '1' and SWPAB bit is set to '1'

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16.1.3. QEI1 I/O Control High Register

Name: QEI1IOCH(1)
Offset: 0x146

Note:

1. This register is not present on all devices.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								HCAPEN
Access								R/W
Reset								0

Bit 0 – HCAPEN Position Counter Input Capture by Home Event Enable bit

Value	Description
1	HOMEx input event (positive edge) triggers a position capture event
0	HOMEx input event (positive edge) does not trigger a position capture event

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16.1.4. QEI1 Status Register

Name: QEI1STAT
Offset: 0x148

Note:
1. This status bit is only applicable to PIMOD[2:0] modes, '011' and '100'.

Legend: C = Clearable bit; HS = Hardware Settable bit

Bit	15	14	13	12	11	10	9	8
			PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
Access			R/C/HS	R/W	R/C/HS	R/W	R/C/HS	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
Access	R/C/HS	R/W	R/C/HS	R/W	R/C/HS	R/W	R/C/HS	R/W
Reset	0	0	0	0	0	0	0	0

Bit 13 – PCHEQIRQ Position Counter Greater Than Compare Status bit

Value	Description
1	POSxCNT > QEIxGEC
0	POSxCNT < QEIxGEC

Bit 12 – PCHEQIEN Position Counter Greater Than Compare Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 11 – PCLEQIRQ Position Counter Less Than Compare Status bit

Value	Description
1	POSxCNT < QEIxLEC
0	POSxCNT > QEIxLEC

Bit 10 – PCLEQIEN Position Counter Less Than Compare Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 9 – POSOVIRQ Position Counter Overflow Status bit

Value	Description
1	Overflow has occurred
0	No overflow has occurred

Bit 8 – POSOVIEN Position Counter Overflow Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 7 – PCIIRQ Position Counter (Homing) Initialization Process Complete Status bit(1)

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Value	Description
1	POSxCNT was reinitialized
0	POSxCNT was not reinitialized

Bit 6 – PCIIEN Position Counter (Homing) Initialization Process Complete Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 5 – VELOVIRQ Velocity Counter Overflow Status bit

Value	Description
1	Overflow has occurred
0	No overflow has occurred

Bit 4 – VELOVIEN Velocity Counter Overflow Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 3 – HOMIRQ Status Flag for Home Event Status bit

Value	Description
1	Home event has occurred
0	No Home event has occurred

Bit 2 – HOMIEN Home Input Event Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 1 – IDXIRQ Status Flag for Index Event Status bit

Value	Description
1	Index event has occurred
0	No Index event has occurred

Bit 0 – IDXIEN Index Input Event Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

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16.1.5. Position 1 Counter Register Low

Name: POS1CNTL
Offset: 0x14C

Bit	15	14	13	12	11	10	9	8
	POSCNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	POSCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – POSCNT[15:0] Low Word Used to Form 32-Bit Position Counter Register (POS1CNT) bits

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16.1.6. Position 1 Counter Register High

Name: POS1CNTH
Offset: 0x14E

Bit	15	14	13	12	11	10	9	8
	POSCNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	POSCNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – POSCNT[31:16] High Word Used to Form 32-Bit Position Counter Register (POS1CNT) bits

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16.1.7. Position 1 Counter Hold Register Low

Name: POS1HLDL
Offset: 0x150

Bit	15	14	13	12	11	10	9	8
	POSHLD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	POSHLD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – POSHLD[15:0] Hold Register for Reading/Writing Position 1 Counter Register (POS1CNTH) bits

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16.1.8. Position 1 Counter Hold Register High

Name: POS1HLD
Offset: 0x152

Bit	15	14	13	12	11	10	9	8
	POSHLDH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	POSHLDH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – POSHLDH[31:16] Hold for Reading/Writing Position 1 Counter Register (POS1CNT) bits

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16.1.9. Velocity 1 Counter Register Low

Name: VEL1CNTL
Offset: 0x154

Bit	15	14	13	12	11	10	9	8
	VELCNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VELCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – VELCNT[15:0] Velocity Counter bits

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16.1.10. Velocity 1 Counter Register High

Name: VEL1CNTH(1)
Offset: 0x156

Note:

1. This register is not present on all devices.

Bit	15	14	13	12	11	10	9	8
	VELCNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VELCNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – VELCNT[31:16] Velocity Counter bits

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16.1.11. Velocity 1 Counter Hold Register Low

Name: VEL1HLDL(1)
Offset: 0x158

Note:

1. This register is not present on all devices.

Bit	15	14	13	12	11	10	9	8
	VELHLD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VELHLD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – VELHLD[15:0] Velocity Counter Hold Value bits

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16.1.12. Velocity 1 Counter Hold Register High

Name: VEL1HLDH
Offset: 0x15A

Bit	15	14	13	12	11	10	9	8
	VELHLDH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VELHLDH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – VELHLDH[31:16] Velocity Counter Hold Value bits

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16.1.13. Interval 1 Timer Register Low

Name: INT1TMRL
Offset: 0x15C

Bit	15	14	13	12	11	10	9	8
	INTTMR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTTMR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTTMR[15:0] Low Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

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16.1.14. Interval 1 Timer Register High

Name: INT1TMRH
Offset: 0x15E

Bit	15	14	13	12	11	10	9	8
	INTTMR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTTMR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTTMR[31:16] High Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

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16.1.15. Index 1 Counter Hold Register Low

Name: INT1HLDL
Offset: 0x160

Bit	15	14	13	12	11	10	9	8
	INTXHLD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTXHLD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTXHLD[15:0] Low Word Used to Form 32-Bit Interval Timer Hold Register (INTxHLD) bits

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16.1.16. Index 1 Counter Hold Register High

Name: INT1HLDH
Offset: 0x162

Bit	15	14	13	12	11	10	9	8
	INTHLD[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTHLD[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTHLD[31:16] High Word Used to Form 32-Bit Interval Timer Hold Register (INTxHLD) bits

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16.1.17. Index 1 Counter Register Low

Name: INDX1CNTL
Offset: 0x164

Bit	15	14	13	12	11	10	9	8
	INDXCNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INDXCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INDXCNT[15:0] Low Word Used to Form 32-Bit Index 1 Counter Register (INDX1CNT) bits

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16.1.18. Index 1 Counter Register High

Name: INDX1CNTH
Offset: 0x166

Bit	15	14	13	12	11	10	9	8
	INDXCNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INDXCNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INDXCNT[31:16] High Word Used to Form 32-Bit Index 1 Counter Register (INDX1CNT) bits

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16.1.19. Index 1 Counter Hold Register Low

Name: INDX1HLDL
Offset: 0x168

Bit	15	14	13	12	11	10	9	8
	INDXHLD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INDXHLD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INDXHLD[15:0] Hold Register for Reading/Writing Index 1 Counter Low Word Register (INDX1CNTH) bits

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16.1.20. Index 1 Counter Hold Register High

Name: INDX1HLDH
Offset: 0x16A

Bit	15	14	13	12	11	10	9	8
	INDXHLDH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INDXHLDH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INDXHLDH[31:16] Hold Register for Reading/Writing Index 1 Counter High Word Register (INDX1CNTH) bits

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16.1.21. QEI1 Greater Than or Equal Compare Register Low

Name: QEI1GECL
Offset: 0x16C

Bit	15	14	13	12	11	10	9	8
	QEIGEC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	QEIGEC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – QEIGEC[15:0] Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

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16.1.22. QEI1 Greater Than or Equal Compare Register High

Name: QEI1GECH
Offset: 0x16E

Bit	15	14	13	12	11	10	9	8
	QEIGEC[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	QEIGEC[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – QEIGEC[31:16] High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

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16.1.23. QEI1 Less Than or Equal Compare Register Low

Name: QEI1LECL
Offset: 0x170

Bit	15	14	13	12	11	10	9	8
	QEILEC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	QEILEC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – QEILEC[15:0] Low Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

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16.1.24. QEI1 Less Than or Equal Compare Register High

Name: QEI1LECH
Offset: 0x172

Bit	15	14	13	12	11	10	9	8
	QEILEC[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	QEILEC[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – QEILEC[31:16] High Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

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17. Universal Asynchronous Receiver Transmitter (UART)

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Multiprotocol Universal Asynchronous Receiver Transmitter (UART) Module"** (www.microchip.com/DS70005288) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The Universal Asynchronous Receiver Transmitter (UART) is a flexible serial communication peripheral used to interface dsPIC® microcontrollers with other equipment, including computers and peripherals. The UART is a full-duplex, asynchronous communication channel that can be used to implement protocols, such as RS-232 and RS-485. The UART also supports the following hardware extensions:

- LIN/J2602
- IrDA®
- Digital Multiplex (DMX)
- Smart Card

The primary features of the UART are:

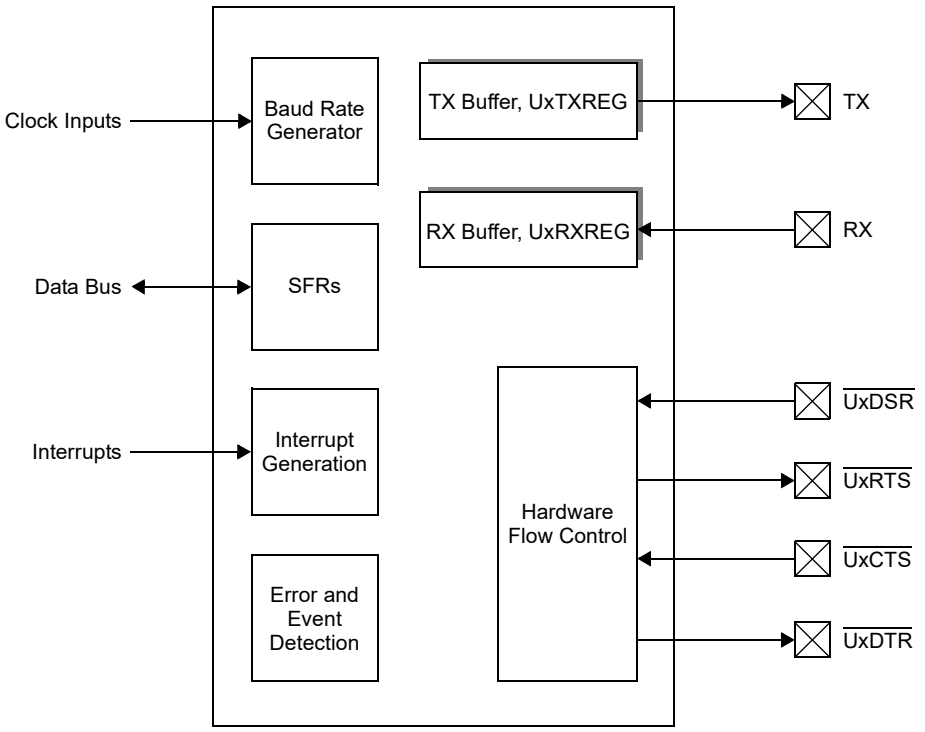
- Full or Half-Duplex Operation
- Up to 8-Deep TX and RX First-In First-Out (FIFO) Buffers
- 8-Bit or 9-Bit Data Width
- Configurable Stop Bit Length
- Flow Control
- Auto-Baud Calibration
- Parity, Framing and Buffer Overrun Error Detection
- Address Detect
- Break Transmission
- Transmit and Receive Polarity Control
- Manchester Encoder/Decoder
- Operation in Sleep mode
- Wake from Sleep on Sync Break Received Interrupt

17.1. Architectural Overview

The UART transfers bytes of data, to and from device pins, using First-In First-Out (FIFO) buffers up to eight bytes deep. The status of the buffers and data is made available to user software through Special Function Registers (SFRs). The UART implements multiple interrupt channels for handling transmit, receive and error events. A simplified block diagram of the UART is shown in Figure 17-1.

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Figure 17-1. Simplified UARTx Block Diagram



17.2. Character Frame

A typical UART character frame is shown in Figure 17-2. The Idle state is high with a 'Start' condition indicated by a falling edge. The Start bit is followed by the number of data, parity/address detect and Stop bits defined by the MOD[3:0] (UxMODE[3:0]) bits selected.

Figure 17-2. UART Character Frame



17.3. Data Buffers

Both transmit and receive functions use buffers to store data shifted to/from the pins. These buffers are FIFOs and are accessed by reading the SFRs, UxTXREG and UxRXREG, respectively. Each data buffer has multiple flags associated with its operation to allow software to read the status. Interrupts can also be configured based on the space available in the buffers. The transmit and receive buffers can be cleared and their pointers reset using the associated TX/RX Buffer Empty Status bits, UTXBE (UxSTAH[5]) and URXBE (UxSTAH[1]).

17.4. Protocol Extensions

The UART provides hardware support for LIN/J2602, DMX and smart card protocol extensions to reduce software overhead. A protocol extension is enabled by writing a value to the MOD[3:0] (UxMODE[3:0]) selection bits and further configured using the UARTx Timing Parameter registers, UxP1, UxP2, UxP3 and UxP3H. Details regarding operation and usage are discussed in their respective chapters. Not all protocols are available on all devices.

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17.5. UART Control/Status Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0238	U1MODE	15:8	UARTEN		USIDL	WAKE	RXBIMD		BRKOVR	UTXBRK
		7:0	BRGH	ABAUD	UTXEN	URXEN	MOD[3:0]			
0x023A	U1MODEH	15:8	SLPEN	ACTIVE			BCLKMOD	BCLKSEL[1:0]		HALFDPLX
		7:0	RUNOVF	URXINV	STSEL[1:0]		C0EN	UTXINV	FLO[1:0]	
0x023C	U1STA	15:8	TXMTIE	PERIE	ABDOVE	CERIE	FERIE	RXBKIE	OERIE	TXCIE
		7:0	TRMT	PERR	ABDOVF	CERIF	FERR	RXBKIF	OERR	TXCIF
0x023E	U1STAH	15:8			UTXISEL[2:0]			URXISEL[2:0]		
		7:0	TXWRE	STPMD	UTXBE	UTXBF	RIDLE	XON	URXBE	URXBF
0x0240	U1BRG	15:8	BRG[15:8]							
		7:0	BRG[7:0]							
0x0242	U1BRGH	15:8								
		7:0					BRG[19:16]			
0x0244	U1RXREG	15:8								
		7:0	RXREG[7:0]							
0x0246 ... 0x0247	Reserved									
0x0248	U1TXREG	15:8	LAST							
		7:0	TXREG[7:0]							
0x024A ... 0x024B	Reserved									
0x024C	U1P1	15:8								P1[8:0]
		7:0	P1[8:0]							
0x024E	U1P2	15:8								P2[8:0]
		7:0	P2[8:0]							
0x0250	U1P3	15:8	P3[15:8]							
		7:0	P3[7:0]							
0x0252	U1P3H	15:8								
		7:0	P3[23:16]							
0x0254	U1TXCHK	15:8								
		7:0	TXCHK[7:0]							
0x0256	U1RXCHK	15:8								
		7:0	RXCHK[7:0]							
0x0258	U1SCCON	15:8								
		7:0			TXRPT[1:0]		CONV	T0PD	PRTCL	
0x025A	U1SCINT	15:8			RXRPTIF	TXRPTIF		BTCIF	WTCIF	GTCIF
		7:0			RXRPTIE	TXRPTIE		BTCIE	WTCIE	GTCIE
0x025C	U1INT	15:8								
		7:0	WUIF	ABDIF				ABDIE		
0x025E ... 0x025F	Reserved									
0x0260	U2MODE	15:8	UARTEN		USIDL	WAKE	RXBIMD		BRKOVR	UTXBRK
		7:0	BRGH	ABAUD	UTXEN	URXEN	MOD[3:0]			
0x0262	U2MODEH	15:8	SLPEN	ACTIVE			BCLKMOD	BCLKSEL[1:0]		HALFDPLX
		7:0	RUNOVF	URXINV	STSEL[1:0]		C0EN	UTXINV	FLO[1:0]	
0x0264	U2STA	15:8	TXMTIE	PERIE	ABDOVE	CERIE	FERIE	RXBKIE	OERIE	TXCIE
		7:0	TRMT	PERR	ABDOVF	CERIF	FERR	RXBKIF	OERR	TXCIF
0x0266	U2STAH	15:8			UTXISEL[2:0]			URXISEL[2:0]		
		7:0	TXWRE	STPMD	UTXBE	UTXBF	RIDLE	XON	URXBE	URXBF
0x0268	U2BRG	15:8	BRG[15:8]							
		7:0	BRG[7:0]							
0x026A	U2BRGH	15:8								
		7:0					BRG[19:16]			
0x026C	U2RXREG	15:8								
		7:0	RXREG[7:0]							

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UART Control/Status Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x026E ... 0x026F	Reserved									
0x0270	U2TXREG	15:8	LAST							
		7:0	TXREG[7:0]							
0x0272 ... 0x0273	Reserved									
0x0274	U2P1	15:8								P1[8:0]
		7:0	P1[8:0]							
0x0276	U2P2	15:8								P2[8:0]
		7:0	P2[8:0]							
0x0278	U2P3	15:8	P3[15:8]							
		7:0	P3[7:0]							
0x027A	U2P3H	15:8								
		7:0	P3[23:16]							
0x027C	U2TXCHK	15:8								
		7:0	TXCHK[7:0]							
0x027E	U2RXCHK	15:8								
		7:0	RXCHK[7:0]							
0x0280	U2SCCON	15:8								
		7:0			TXRPT[1:0]		CONV	T0PD	PRTCL	
0x0282	U2SCINT	15:8			RXRPTIF	TXRPTIF		BTCIF	WTCIF	GTCIF
		7:0			RXRPTIE	TXRPTIE		BTCIE	WTCIE	GTCIE
0x0284	U2INT	15:8								
		7:0	WUIF	ABDIF				ABDIE		
0x0286 ... 0x0EFF	Reserved									
0x0F00	U3MODE	15:8	UARTEN		USIDL	WAKE	RXBIMD		BRKOVR	UTXBRK
		7:0	BRGH	ABAUD	UTXEN	URXEN	MOD[3:0]			
0x0F02	U3MODEH	15:8	SLPEN	ACTIVE			BCLKMOD	BCLKSEL[1:0]		HALFDPLX
		7:0	RUNOVF	URXINV	STSEL[1:0]		C0EN	UTXINV	FLO[1:0]	
0x0F04	U3STA	15:8	TXMTIE	PERIE	ABDOVE	CERIE	FERIE	RXBKIE	OERIE	TXCIE
		7:0	TRMT	PERR	ABDOVF	CERIF	FERR	RXBKIF	OERR	TXCIF
0x0F06	U3STAH	15:8			UTXISEL[2:0]				URXISEL[2:0]	
		7:0	TXWRE	STPMD	UTXBE	UTXBF	RIDLE	XON	URXBE	URXBF
0x0F08	U3BRG	15:8	BRG[15:8]							
		7:0	BRG[7:0]							
0x0F0A	U3BRGH	15:8								
		7:0					BRG[19:16]			
0x0F0C	U3RXREG	15:8								
		7:0	RXREG[7:0]							
0x0F0E ... 0x0F0F	Reserved									
0x0F10	U3TXREG	15:8	LAST							
		7:0	TXREG[7:0]							
0x0F12 ... 0x0F13	Reserved									
0x0F14	U3P1	15:8								P1[8:0]
		7:0	P1[8:0]							
0x0F16	U3P2	15:8								P2[8:0]
		7:0	P2[8:0]							
0x0F18	U3P3	15:8	P3[15:8]							
		7:0	P3[7:0]							
0x0F1A	U3P3H	15:8								
		7:0	P3[23:16]							
0x0F1C	U3TXCHK	15:8								
		7:0	TXCHK[7:0]							

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UART Control/Status Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0F1E	U3RXCHK	15:8								
		7:0	RXCHK[7:0]							
0x0F20	U3SCCON	15:8								
		7:0			TXRPT[1:0]		CONV	T0PD	PRTCL	
0x0F22	U3SCINT	15:8			RXRPTIF	TXRPTIF		BTCIF	WTCIF	GTCIF
		7:0			RXRPTIE	TXRPTIE		BTCIE	WTCIE	GTCIE
0x0F24	U3INT	15:8								
		7:0	WUIF	ABDIF				ABDIE		

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17.5.1. UARTx Configuration Register

Name: UxMODE
Offset: 0x238, 0x260, 0xF00

Note:
1. R/HS/HC in DMX and LIN mode.

Legend: HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
	UARTEN		USIDL	WAKE	RXBIMD		BRKOVR	UTXBRK
Access	R/W		R/W	R/W	R/W		R/W	R/W/HC
Reset	0		0	0	0		0	0

Bit	7	6	5	4	3	2	1	0
	BRGH	ABAUD	UTXEN	URXEN	MOD[3:0]			
Access	R/W	R/W/HC	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – UARTEN UART Enable bit

Value	Description
1	UART is ready to transmit and receive.
0	UART state machine, FIFO Buffer Pointers and counters are reset; registers are readable and writable.

Bit 13 – USIDL UART Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode.
0	Continues module operation in Idle mode.

Bit 12 – WAKE Wake-up Enable bit

Value	Description
1	Module will continue to sample the RX pin – interrupt generated on falling edge, bit cleared in hardware on following rising edge; if ABAUD is set, Auto-Baud Detection (ABD) will begin immediately.
0	RX pin is not monitored nor rising edge detected.

Bit 11 – RXBIMD Receive Break Interrupt Mode bit

Value	Description
1	RXBKIF flag when a minimum of 23 (DMX)/11 (asynchronous or LIN/J2602) low bit periods are detected.
0	RXBKIF flag when the Break makes a low-to-high transition after being low for at least 23/11-bit periods.

Bit 9 – BRKOVR Send Break Software Override bit
Overrides the TX Data Line:

Value	Description
1	Makes the TX line active (Output 0 when UTXINV = 0, Output 1 when UTXINV = 1).
0	TX line is driven by the shifter.

Bit 8 – UTXBRK UART Transmit Break bit(1)

Value	Description
1	Sends Sync Break on next transmission; cleared by hardware upon completion.
0	Sync Break transmission is disabled or has completed.

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Bit 7 – BRGH High Baud Rate Select bit

Value	Description
1	High Speed: Baud rate is baudclk/4.
0	Low Speed: Baud rate is baudclk/16.

Bit 6 – ABAUD Auto-Baud Detect Enable bit (read-only when MOD[3:0] = 1xxx)

Value	Description
1	Enables baud rate measurement on the next character – requires reception of a Sync field (55h); cleared in hardware upon completion.
0	Baud rate measurement is disabled or has completed.

Bit 5 – UTXEN UART Transmit Enable bit

Value	Description
1	Transmit enabled – except during Auto-Baud Detection.
0	Transmit disabled – all transmit counters, pointers and state machines are Reset; TX buffer is not flushed, status bits are not Reset.

Bit 4 – URXEN UART Receive Enable bit

Value	Description
1	Receive enabled – except during Auto-Baud Detection.
0	Receive disabled – all receive counters, pointers and state machines areReset; RX buffer is not flushed, status bits are not Reset.

Bits 3:0 – MOD[3:0] UART Mode bits

Value	Description
Other	Reserved
1111	Smart card
1110	IrDA®
1101	Reserved
1100	LIN Commander/Responder
1011	LIN Responder only
1010	DMX
1001	Reserved
1000	Reserved
0111	Reserved
0110	Reserved
0101	Reserved
0100	Asynchronous 9-bit UART with address detect, ninth bit = 1 signals address.
0011	Asynchronous 8-bit UART without address detect, ninth bit is used as an even parity bit.
0010	Asynchronous 8-bit UART without address detect, ninth bit is used as an odd parity bit.
0001	Asynchronous 7-bit UART
0000	Asynchronous 8-bit UART

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17.5.2. UARTx Configuration Register High

Name: UxMODEH
Offset: 0x23A, 0x262, 0xF02

Bit	15	14	13	12	11	10	9	8
	SLPEN	ACTIVE			BCLKMOD	BCLKSEL[1:0]		HALFDPLX
Access	R/W	R			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUNOVF	URXINV	STSEL[1:0]		C0EN	UTXINV	FLO[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – SLPEN Run During Sleep Enable bit

Value	Description
1	UART BRG clock runs during Sleep.
0	UART BRG clock is turned off during Sleep.

Bit 14 – ACTIVE UART Running Status bit

Value	Description
1	UART clock request is active (user can not update the UxMODE/UxMODEH registers).
0	UART clock request is not active (user can update the UxMODE/UxMODEH registers).

Bit 11 – BCLKMOD Baud Clock Generation Mode Select bit

Value	Description
1	Uses fractional Baud Rate Generation.
0	Uses legacy divide-by-x counter for baud clock generation (x = 4 or 16 depending on the BRGH bit).

Bits 10:9 – BCLKSEL[1:0] Baud Clock Source Selection bits

Value	Description
11	F_{VCODIV}
10	F_{OSC}
01	$F_{VCO}/5$
00	F_P

Bit 8 – HALFDPLX UART Half-Duplex Selection Mode bit

Value	Description
1	Half-Duplex mode: UxTX is driven as an output when transmitting and tri-stated when TX is Idle.
0	Full-Duplex mode: UxTX is driven as an output at all times when both UARTEN and UTXEN are set.

Bit 7 – RUNOVF Run During Overflow Condition Mode bit

Value	Description
1	When an Overflow Error (OERR) condition is detected, the RX shifter continues to run so as to remain synchronized with incoming RX data; data are not transferred to UxRXREG when it is full (i.e., no UxRXREG data are overwritten).
0	When an Overflow Error (OERR) condition is detected, the RX shifter stops accepting new data (Legacy mode).

Bit 6 – URXINV UART Receive Polarity bit

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Value	Description
1	Inverts RX polarity; Idle state is low.
0	Input is not inverted; Idle state is high.

Bits 5:4 – STSEL[1:0] Number of Stop Bits Selection bits

Value	Description
11	2 Stop bits sent, 1 checked at receive.
10	2 Stop bits sent, 2 checked at receive.
01	1.5 Stop bits sent, 1.5 checked at receive.
00	1 Stop bit sent, 1 checked at receive.

Bit 3 – C0EN Enable Legacy Checksum (C0) Transmit and Receive bit

Value	Description
1	Checksum Mode 1 (enhanced LIN checksum in LIN mode; add all TX/RX words in all other modes).
0	Checksum Mode 0 (legacy LIN checksum in LIN mode; not used in all other modes).

Bit 2 – UTXINV UART Transmit Polarity bit

Value	Description
1	Inverts TX polarity; TX is low in Idle state.
0	Output data are not inverted; TX output is high in Idle state.

Bits 1:0 – FLO[1:0] Flow Control Enable bits (Only valid when MOD[3:0] = 0xxx)

Value	Description
11	Reserved
10	$\overline{\text{RTS}}$-$\overline{\text{DSR}}$ (for TX side)/$\overline{\text{CTS}}$-DTR (for RX side) hardware flow control
01	XON/XOFF software flow control
00	Flow control off

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17.5.3. UARTx Status Register

Name: UxSTA
Offset: 0x23C, 0x264, 0xF04

Legend: HC = Hardware Clearable bit; HS = Hardware Settable bit

Bit	15	14	13	12	11	10	9	8
	TXMTIE	PERIE	ABDOVE	CERIE	FERIE	RXBKIE	OERIE	TXCIE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRMT	PERR	ABDOVF	CERIF	FERR	RXBKIF	OERR	TXCIF
Access	R	R	R/W/HS	R/W/HC	R	R/W/HC	R/W/HC	R/W/HC
Reset	1	0	0	0	0	0	0	0

Bit 15 – TXMTIE Transmit Shifter Empty Interrupt Enable bit

Value	Description
1	Interrupt is enabled.
0	Interrupt is disabled.

Bit 14 – PERIE Parity Error Interrupt Enable bit

Value	Description
1	Interrupt is enabled.
0	Interrupt is disabled.

Bit 13 – ABDOVE Auto-Baud Rate Acquisition Interrupt Enable bit

Value	Description
1	Interrupt is enabled.
0	Interrupt is disabled.

Bit 12 – CERIE Checksum Error Interrupt Enable bit

Value	Description
1	Interrupt is enabled.
0	Interrupt is disabled.

Bit 11 – FERIE Framing Error Interrupt Enable bit

Value	Description
1	Interrupt is enabled.
0	Interrupt is disabled.

Bit 10 – RXBKIE Receive Break Interrupt Enable bit

Value	Description
1	Interrupt is enabled.
0	Interrupt is disabled.

Bit 9 – OERIE Receive Buffer Overflow Interrupt Enable bit

Value	Description
1	Interrupt is enabled.

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Value	Description
0	Interrupt is disabled.

Bit 8 – TXCIE Transmit Collision Interrupt Enable bit

Value	Description
1	Interrupt is enabled.
0	Interrupt is disabled.

Bit 7 – TRMT Transmit Shifter Empty Interrupt Flag bit (read-only)

Value	Description
1	Transmit Shift Register (TSR) is empty (end of last Stop bit when STPMD = 1 or middle of first Stop bit when STPMD = 0).
0	Transmit Shift Register is not empty.

Bit 6 – PERR Parity Error/Address Received/Forward Frame Interrupt Flag bit

LIN and Parity Modes:
1 = Parity error detected
0 = No parity error detected
Address Mode:
1 = Address received
0 = No address detected
All Other Modes:
Not used.

Bit 5 – ABDOVF Auto-Baud Rate Acquisition Interrupt Flag bit (must be cleared by software)

Value	Description
1	BRG rolled over during the auto-baud rate acquisition sequence (must be cleared in software).
0	BRG has not rolled over during the auto-baud rate acquisition sequence.

Bit 4 – CERIF Checksum Error Interrupt Flag bit (must be cleared by software)

Value	Description
1	Checksum error
0	No checksum error

Bit 3 – FERR Framing Error Interrupt Flag bit

Value	Description
1	Framing Error: Inverted level of the Stop bit corresponding to the topmost character in the buffer; propagates through the buffer with the received character.
0	No framing error.

Bit 2 – RXBKIF Receive Break Interrupt Flag bit (must be cleared by software)

Value	Description
1	A Break was received.
0	No Break was detected.

Bit 1 – OERR Receive Buffer Overflow Interrupt Flag bit (must be cleared by software)

Value	Description
1	Receive buffer has overflowed.
0	Receive buffer has not overflowed.

Bit 0 – TXCIF Transmit Collision Interrupt Flag bit (must be cleared by software)

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Value	Description
1	Transmitted word is not equal to the received word.
0	Transmitted word is equal to the received word.

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17.5.4. UARTx Status Register High

Name: UxSTAH
Offset: 0x23E, 0x266, 0xF06

Note:

1. The receive watermark interrupt is not set if PERIF or FERIF is set and the corresponding IE bit is set.

Legend: S = Settable bit, HS = Hardware Settable bit

Bit	15	14	13	12	11	10	9	8
		UTXISEL[2:0]				URXISEL[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	TXWRE	STPMD	UTXBE	UTXBF	RIDLE	XON	URXBE	URXBF
Access	R/W/HS	R/W	R/S	R	R	R	R/S	R
Reset	0	0	1	0	1	1	1	0

Bits 14:12 – UTXISEL[2:0] UART Transmit Interrupt Select bits

Value	Description
111	Sets transmit interrupt when there is one empty slot left in the buffer.
. . .	
010	Sets transmit interrupt when there are six or more empty slots in the buffer.
001	Sets transmit interrupt when there are seven or more empty slots in the buffer.
000	Sets transmit interrupt when there are eight or more empty slots in the buffer; TX buffer is empty.

Bits 10:8 – URXISEL[2:0] UART Receive Interrupt Select bits(1)

Value	Description
111	Triggers receive interrupt when there are eight words in the buffer; RX buffer is full.
. . .	
001	Triggers receive interrupt when there are two or more words in the buffer.
000	Triggers receive interrupt when there is one or more words in the buffer.

Bit 7 – TXWRE TX Write Transmit Error Status bit

LIN and Parity Modes:
1 = A new byte was written when buffer was full or when P2[8:0] = 0 (must be cleared by software).
0 = No error.
Address Detect Mode:
1 = A new byte was written when buffer was full or to P1[8:0] when P1x was full (must be cleared by software).
0 = No error.
Other Modes:
1 = A new byte was written when buffer was full (must be cleared by software).
0 = No error.

Bit 6 – STPMD Stop Bit Detection Mode bit

Value	Description
1	Triggers RXIF at the end of the last Stop bit.
0	Triggers RXIF in the middle of the first (or second, depending on the STSEL[1:0] setting) Stop bit.

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Bit 5 – UTXBE UART TX Buffer Empty Status bit

Value	Description
1	Transmit buffer is empty; writing '1' when UTXEN = 0 will reset the TX FIFO Pointers and counters.
0	Transmit buffer is not empty.

Bit 4 – UTXBF UART TX Buffer Full Status bit

Value	Description
1	Transmit buffer is full.
0	Transmit buffer is not full.

Bit 3 – RIDLE Receive Idle bit

Value	Description
1	UART RX line is in the Idle state.
0	UART RX line is receiving something.

Bit 2 – XON UART in XON Mode bit
Only valid when FLO[1:0] control bits are set to XON/XOFF mode.

Value	Description
1	UART has received XON.
0	UART has not received XON or XOFF was received.

Bit 1 – URXBE UART RX Buffer Empty Status bit

Value	Description
1	Receive buffer is empty; writing '1' when URXEN = 0 will reset the RX FIFO Pointers and counters.
0	Receive buffer is not empty.

Bit 0 – URXBF UART RX Buffer Full Status bit

Value	Description
1	Receive buffer is full.
0	Receive buffer is not full.

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17.5.5. UARTx Baud Rate Register

Name: UxBRG
Offset: 0x240, 0x268, 0xF08

Bit	15	14	13	12	11	10	9	8
	BRG[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BRG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BRG[15:0] Baud Rate Divisor bits

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17.5.6. UARTx Baud Rate Register High

Name: UxBRGH
Offset: 0x242, 0x26A, 0xF0A

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					BRG[19:16]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – BRG[19:16] Baud Rate Divisor bits

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17.5.7. UARTx Receive Buffer Register

Name: UxRXREG
Offset: 0x244, 0x26C, 0xF0C

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	RXREG[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – RXREG[7:0] Received Character Data bits

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17.5.8. UARTx Transmit Buffer Register

Name: UxTXREG
Offset: 0x248, 0x270, 0xF10

Legend: x = Bit is unknown

Bit	15	14	13	12	11	10	9	8
	LAST							
Access	W							
Reset	x							

Bit	7	6	5	4	3	2	1	0
	TXREG[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	x	x	x	x	x	x	x	x

Bit 15 – LAST Last Byte Indicator for Smart Card Support bit

Bits 7:0 – TXREG[7:0] Transmitted Character Data bits
If the buffer is full, further writes to the buffer are ignored.

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17.5.9. UARTx Timing Parameter 1 Register

Name: UxP1
Offset: 0x24C, 0x274, 0xF14

Bit	15	14	13	12	11	10	9	8
								P1[8:0]
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
	P1[8:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 8:0 – P1[8:0] Parameter 1 bits

DMX TX:
Number of bytes to transmit – 1 (not including Start code).
LIN Commander TX:
PID to transmit (bits[5:0]).
Asynchronous TX with Address Detect:
Address to transmit. A '1' is automatically inserted into bit 9 (bits[7:0]).
Smart Card Mode:
Guard Time Counter bits. This counter is operated on the bit clock whose period is always equal to one ETU (bits[8:0]).
Other Modes:
Not used.

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17.5.10. UARTx Timing Parameter 2 Register

Name: UxP2
Offset: 0x24E, 0x276, 0xF16

Bit	15	14	13	12	11	10	9	8
								P2[8:0]
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
	P2[8:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 8:0 – P2[8:0] Parameter 2 bits

DMX RX:
The first byte number to receive – 1, not including Start code (bits[8:0]).
LIN Responder TX:
Number of bytes to transmit (bits[7:0]).
Asynchronous RX with Address Detect:
Address to start matching (bits[7:0]).
Smart Card Mode:
Block Time Counter bits. This counter is operated on the bit clock whose period is always equal to one ETU (bits[8:0]).
Other Modes:
Not used.

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17.5.11. UARTx Timing Parameter 3 Register

Name: UxP3
Offset: 0x250, 0x278, 0xF18

Bit	15	14	13	12	11	10	9	8
	P3[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	P3[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – P3[15:0] Parameter 3 bits

DMX RX:
The last byte number to receive – 1, not including Start code (bits[8:0]).
LIN Responder RX:
Number of bytes to receive (bits[7:0]).
Asynchronous RX:
Used to mask the UxP2 address bits; `1` = P2 address bit is used, `0` = P2 address bit is masked off (bits[7:0]).
Smart Card Mode:
Waiting Time Counter bits (bits[15:0]).
Other Modes:
Not used.

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17.5.12. UARTx Timing Parameter 3 Register High

Name: UxP3H
Offset: 0x252, 0x27A, 0xF1A

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P3[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – P3[23:16] Parameter 3 High bits
Smart Card Mode:
Waiting Time Counter bits (bits[23:16]).
Other Modes:
Not used.

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17.5.13. UARTx Transmit Checksum Register

Name: UxTXCHK
Offset: 0x254, 0x27C, 0xF1C

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	TXCHK[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TXCHK[7:0] Transmit Checksum bits (calculated from TX words)
LIN Modes:
C0EN = 1: Sum of all transmitted data + addition carries, including PID.
C0EN = 0: Sum of all transmitted data + addition carries, excluding PID.
LIN Responder:
Cleared when Break is detected.
LIN Commander/Responder:
Cleared when Break is detected.
Other Modes:
C0EN = 1: Sum of every byte transmitted + addition carries.
C0EN = 0: Value remains unchanged.

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17.5.14. UARTx Receive Checksum Register

Name: UxRXCHK
Offset: 0x256, 0x27E, 0xF1E

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	RXCHK[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – RXCHK[7:0] Receive Checksum bits (calculated from RX words)

LIN Modes:
C0EN = 1: Sum of all received data + addition carries, including PID.
C0EN = 0: Sum of all received data + addition carries, excluding PID.
LIN Responder:
Cleared when Break is detected.
LIN Commander/Responder:
Cleared when Break is detected.
Other Modes:
C0EN = 1: Sum of every byte received + addition carries.
C0EN = 0: Value remains unchanged.

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17.5.15. UARTx Smart Card Configuration Register

Name: UxSCCON
Offset: 0x258, 0x280, 0xF20

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			TXRPT[1:0]		CONV	T0PD	PRTCL	
Access			R/W	R/W	R/W	R/W	R/W	
Reset			0	0	0	0	0	

Bits 5:4 – TXRPT[1:0] Transmit Repeat Selection bits

Value	Description
11	Retransmits the error byte four times.
10	Retransmits the error byte three times.
01	Retransmits the error byte twice.
00	Retransmits the error byte once.

Bit 3 – CONV Logic Convention Selection bit

Value	Description
1	Inverse logic convention
0	Direct logic convention

Bit 2 – T0PD Pull-Down Duration for T = 0 Error Handling bit

Value	Description
1	2 ETU
0	1 ETU

Bit 1 – PRTCL Smart Card Protocol Selection bit

Value	Description
1	T = 1
0	T = 0

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17.5.16. UARTx Smart Card Interrupt Register

Name: UxSCINT
Offset: 0x25A, 0x282, 0xF22

Legend: HS = Hardware Settable bit

Bit	15	14	13	12	11	10	9	8
			RXRPTIF	TXRPTIF		BTCIF	WTCIF	GTCIF
Access			R/W/HS	R/W/HS		R/W/HS	R/W/HS	R/W/HS
Reset			0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
			RXRPTIE	TXRPTIE		BTCIE	WTCIE	GTCIE
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bit 13 – RXRPTIF Receive Repeat Interrupt Flag bit

Value	Description
1	Parity error has persisted after the same character has been received five times (four retransmits).
0	Flag is cleared.

Bit 12 – TXRPTIF Transmit Repeat Interrupt Flag bit

Value	Description
1	Line error has been detected after the last retransmit per TXRPT[1:0].
0	Flag is cleared.

Bit 10 – BTCIF Block Time Counter Interrupt Flag bit

Value	Description
1	Block Time Counter has reached 0.
0	Block Time Counter has not reached 0.

Bit 9 – WTCIF Waiting Time Counter Interrupt Flag bit

Value	Description
1	Waiting Time Counter has reached 0.
0	Waiting Time Counter has not reached 0.

Bit 8 – GTCIF Guard Time Counter Interrupt Flag bit

Value	Description
1	Guard Time Counter has reached 0.
0	Guard Time Counter has not reached 0.

Bit 5 – RXRPTIE Receive Repeat Interrupt Enable bit

Value	Description
1	An interrupt is invoked when a parity error has persisted after the same character has been received five times (four retransmits).
0	Interrupt is disabled.

Bit 4 – TXRPTIE Transmit Repeat Interrupt Enable bit

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Value	Description
1	An interrupt is invoked when a line error is detected after the last retransmit per TXRPT[1:0] has been completed.
0	Interrupt is disabled.

Bit 2 – BTCIE Block Time Counter Interrupt Enable bit

Value	Description
1	Block Time Counter interrupt is enabled.
0	Block Time Counter interrupt is disabled.

Bit 1 – WTCIE Waiting Time Counter Interrupt Enable bit

Value	Description
1	Waiting Time Counter interrupt is enabled.
0	Waiting Time Counter interrupt is disabled.

Bit 0 – GTCIE Guard Time Counter Interrupt Enable bit

Value	Description
1	Guard Time Counter interrupt is enabled.
0	Guard Time Counter interrupt is disabled.

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17.5.17. UARTx Interrupt Register

Name: UxINT
Offset: 0x25C, 0x284, 0xF24

Legend: HS = Hardware Settable bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	WUIF	ABDIF				ABDIE		
Access	R/W/HS	R/W/HS				R/W		
Reset	0	0				0		

Bit 7 – WUIF Wake-up Interrupt Flag bit

Value	Description
1	Sets when WAKE = 1 and RX makes a '1' to '0' transition; triggers event interrupt (must be cleared by software).
0	WAKE is not enabled or WAKE is enabled, but no wake-up event has occurred.

Bit 6 – ABDIF Auto-Baud Completed Interrupt Flag bit

Value	Description
1	Sets when ABD sequence makes the final '1' to '0' transition; triggers event interrupt (must be cleared by software).
0	ABAUD is not enabled or ABAUD is enabled but auto-baud has not completed.

Bit 2 – ABDIE Auto-Baud Completed Interrupt Enable Flag bit

Value	Description
1	Allows ABDIF to set an event interrupt.
0	ABDIF does not set an event interrupt.

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18. LIN Transceiver Module

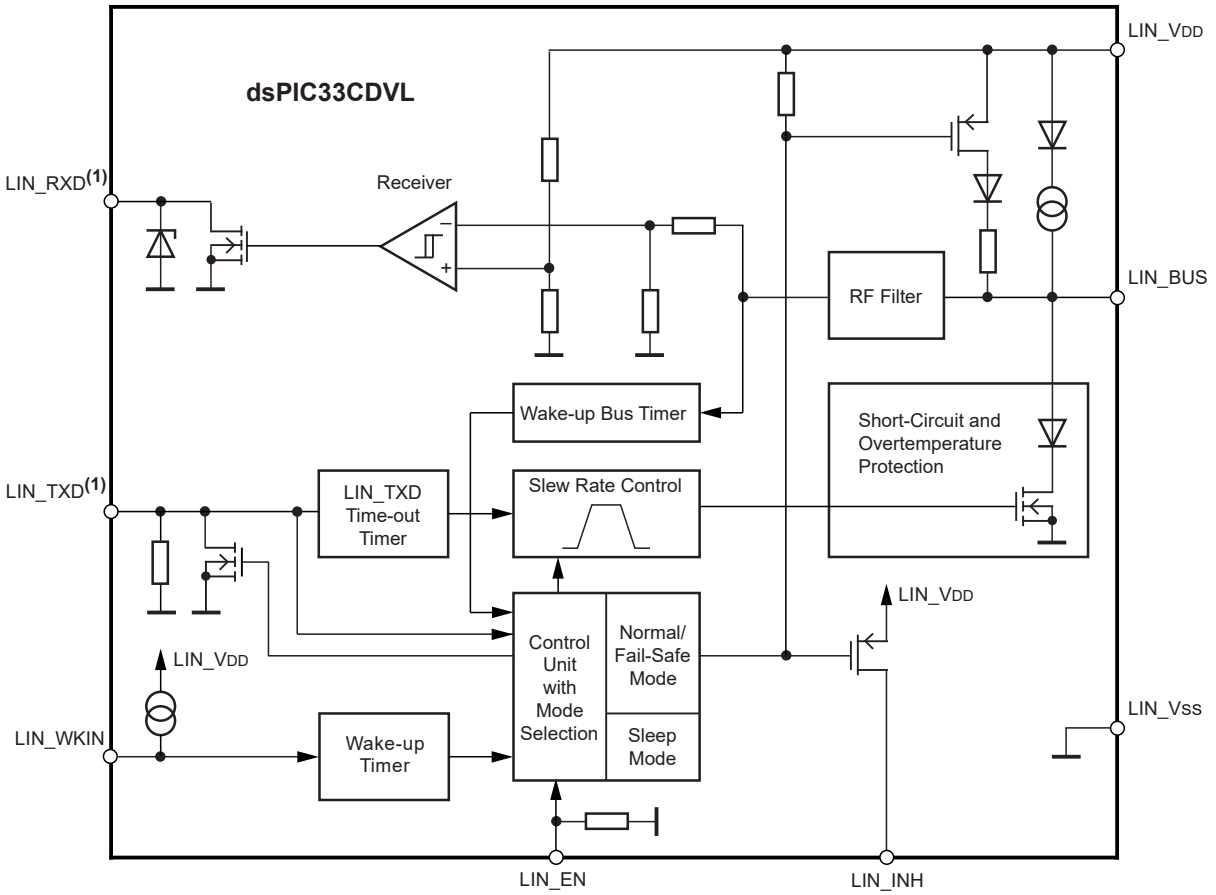
The fully integrated LIN Transceiver is designed in compliance with the LIN Specification 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2. It interfaces the LIN protocol handler and the physical layer. The device is designed to handle the low-speed data communication in vehicles, for example, in convenience electronics. Improved slope control at the LIN bus ensures data communication up to 20 kbaud. Sleep mode ensures minimal current consumption even in the case of a floating bus line or a short circuit on the LIN bus to LIN_VSS.

The primary features of the LIN Transceiver module are:

- Supply Voltage Up to 40V
- Operating Voltage VS = 5V to 28V
- Very Low Supply Current
  - Sleep mode: Typically 9 µA
  - Fail-Safe mode: Typically 80 µA
  - Normal mode: Typically 250 µA
- Fully Compatible with 3.3V and 5V Devices
- LIN Physical Layer According to LIN 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2
- Wake-up Capability via LIN bus (100 µs dominant)
- External Wake-up via LIN_WKIN pin (100 µs low level)
- LIN_INH Output to Control an External Voltage Regulator or to Switch the Commander Pull-up
- Wake-up Source Recognition
- LIN_TXD Time-out Timer
- Bus Pin is Overtemperature and Short-Circuit Protected vs. LIN_VSS and Battery
- Advanced EMC and ESD Performance
- Fulfills the OEM *"Hardware Requirements for LIN in Automotive Applications Rev.1.3"*
- Interference and Damage Protection According to ISO7637
  Qualified According to AEC-Q100

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Figure 18-1. LIN Transceiver Module Block Diagram



Note:

1. Pin is connected to a device interconnect; see Table 1-1 for more information.

18.1. Pin Description

18.1.1. Supply Pin (LIN_VDD)

LIN operating voltage is VS = 5V to 28V. Undervoltage detection is implemented to disable transmission if VS falls below typical, 4.5V, thereby avoiding false bus messages. After switching on VS, the IC starts in Fail-Safe mode and the LIN_INH output is switched on.

The supply current in Sleep mode is typically 9 µA.

18.1.2. Ground Pin (LIN_VSS)

The IC does not affect the LIN bus in the event of LIN_VSS disconnection. It is able to handle a ground shift of up to 11.5% of V_S.

18.1.3. Bus Pin (LIN_BUS)

A low-side driver with internal current limitation and thermal shutdown, as well as an internal pull-up resistor according to LIN Specification 2.x, is implemented. The voltage range is from -27V to +40V. This pin exhibits no reverse current from the LIN bus to V_S, even in the event of a LIN_VSS shift or V_{BAT} disconnection. The LIN receiver thresholds comply with the LIN protocol specification.

The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope controlled.

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During a short circuit at LIN_BUS to V_{BAT}, the output limits the output current to IBUS_LIM. Due to the power dissipation, the chip temperature exceeds Toff and the LIN_BUS output is switched off. The chip cools down and after a hysteresis of T_{HYS}, switches the output on again. LIN_RXD stays on high because LIN_BUS is high.

During a short circuit from LIN_BUS to LIN_V_{SS}, the IC can be switched into Sleep mode, and even in this case, the current consumption is lower than 100 µA. If the short circuit disappears, the IC starts with a remote wake-up.

The reverse current is <2 µA at pin LIN_BUS during loss of V_{BAT}. This is optimal behavior for bus systems where some Responder nodes are supplied from battery or ignition.

18.1.4. Input/Output (LIN_TXD)

In Normal mode, the LIN_TXD pin is the microcontroller interface for controlling the state of the LIN_BUS output. LIN_TXD must be pulled to ground in order to drive the LIN bus low. If LIN_TXD is high, the LIN_BUS output transistor is turned off and the bus is in the Recessive state. If the LIN_TXD pin stays at LIN_V_{SS} level while switching into Normal mode, it must be pulled to a high level longer than 10 µs before the LIN Transceiver can be activated. This feature prevents the bus line from being accidentally driven to a Dominant state after Normal mode has been activated (also in case of a short circuit at LIN_TXD to LIN_V_{SS}). During Fail-Safe mode, this pin is used as an output and signals the Fail-Safe source.

The LIN_TXD pin provides a pull-down resistor in order to have a defined level if LIN_TXD is disconnected.

An internal timer prevents the bus line from being driven permanently in the Dominant state. If LIN_TXD is forced to low longer than t_{dom} > 20 ms, the LIN bus driver is switched to the Recessive state. Nevertheless, when switching to Sleep mode, the actual level at the LIN_TXD pin is relevant.

To reactivate the LIN bus driver, switch LIN_TXD to high (>10 µs).

18.1.5. Output Pin (LIN_RXD)

In Normal mode, this pin reports the state of the LIN bus to the microcontroller. LIN high (Recessive state) is indicated by a high level at LIN_RXD; LIN low (Dominant state) is indicated by a low level at LIN_RXD.

The output is an open-drain; therefore, it is compatible with a 3.3V or 5V power supply. The AC characteristics are defined by an external pull-up resistor of 4.7 kOhm to 5V and a load capacitor of 20 pF.

In Unpowered mode, LIN_RXD is switched off.

18.1.6. Enable Input Pin (LIN_EN)

The enable input pin controls the Operating mode of the device. If LIN_EN is high, the circuit is in Normal mode, with transmission paths from LIN_TXD to LIN_- BUS and from LIN_BUS to LIN_RXD both active.

If LIN_EN is switched to low while LIN_TXD is still high, the device is forced to Sleep mode. No data transmission is then possible and current consumption is reduced to IVS_{sleep}, typically 9 µA.

The LIN_EN pin provides a pull-down resistor to force the transceiver into Recessive mode if LIN_EN is disconnected.

18.1.7. Inhibit Output Pin (LIN_INH)

This pin is used to control an external voltage regulator or to switch the LIN Commander pull-up resistor on/off in case the device is used in a Commander node. The inhibit pin provides an internal switch toward the LIN_V_{DD} pin, which is protected by temperature monitoring. If the device is in Normal or Fail-Safe mode, the inhibit high-side switch is turned on. When the device is in Sleep

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mode, the inhibit switch is turned off, thus disabling the voltage regulator or other connected external devices.

A wake-up event on the LIN bus or at the LIN_WKIN pin switches the LIN_INH pin to the VS level. After a system power-up (VS rises from zero), the LIN_INH pin switches to the VS level automatically.

18.1.8. Wake Pin (LIN_WKIN)

This pin is a high-voltage input used for waking up the device from Sleep mode. It is usually connected to an external switch in the application to generate a local wake-up. A pull-up current source with typically 10 µA is implemented. The voltage threshold for a wake-up signal is typically 2V below the V_S voltage.

If a local wake-up is not needed in the application, the LIN_WKIN pin can be connected directly to the LIN_V_{DD} pin.

18.2. Functional Description

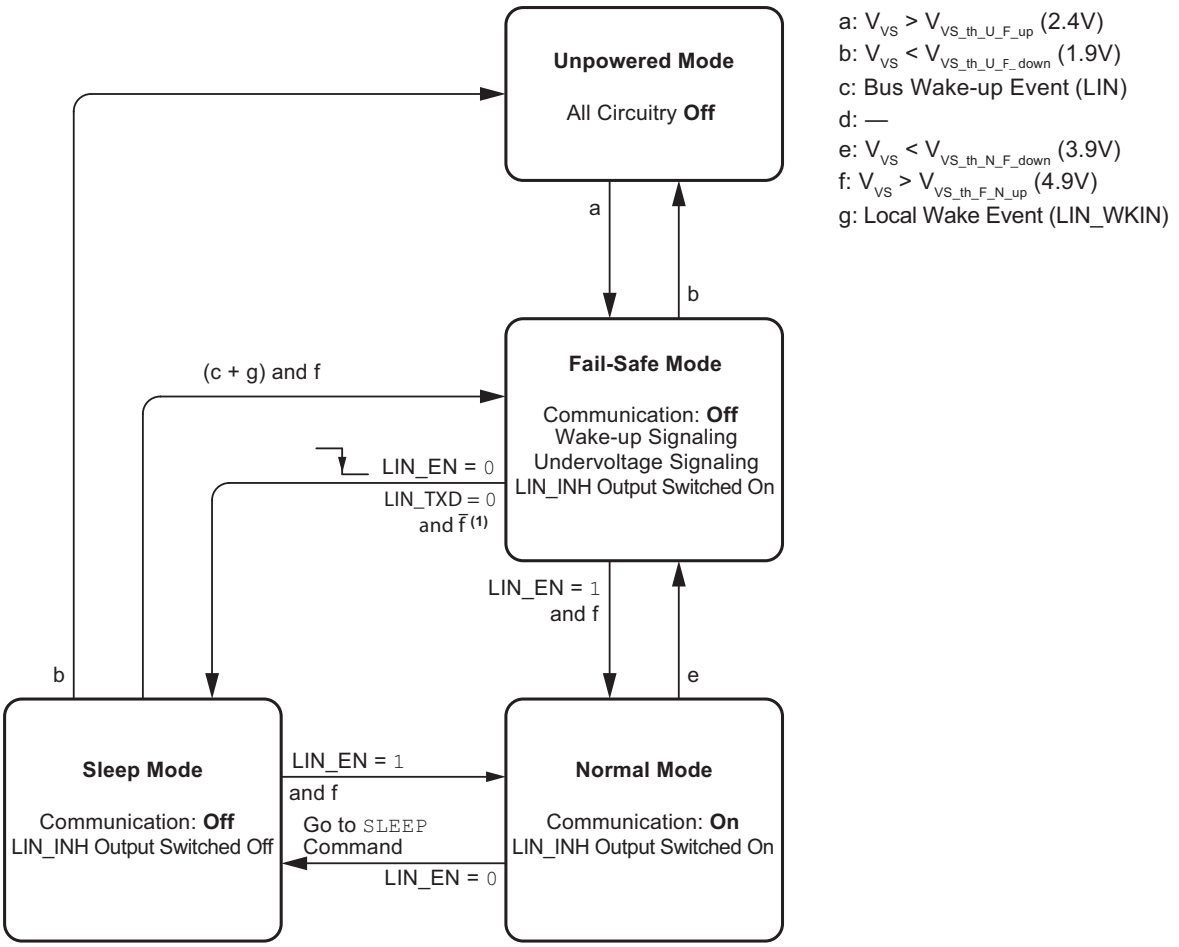
18.2.1. Physical Layer Compatibility

Since the LIN physical layer is independent of higher LIN layers (for example, LIN protocol layer), all nodes with a LIN physical layer according to Revision 2.x can be mixed with LIN physical layer nodes based on earlier versions (for instance, LIN 1.0, LIN 1.1, LIN 1.2 and LIN 1.3) without any restrictions.

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18.2.2. Operating Modes

Figure 18-2. Operating Modes



Note:

1. Condition f is valid for V_S ramp up; at V_S ramp down condition, e is valid instead of f.

Table 18-1. LIN Transceiver Operating Modes

Operating Mode	Transceiver	LIN_INH	LIN_BUS	LIN_TXD	LIN_RXD
Fail-Safe	Off	On, except VS < $V_{VS\_th\_N\_F\_down}$	Recessive	Signaling Fail-Safe Sources (see Table 18-2)	
Normal	On	On	LIN_TXD Dependent	Follows Data Transmission	
Sleep/Unpowered	Off	Off	Recessive	Low	High Ohmic

18.2.3. Normal Mode

This is the normal Transmitting and Receiving mode of the LIN interface in accordance with LIN Specification 2.x.

18.2.4. Sleep Mode

A falling edge at LIN_EN switches the IC into Sleep mode. While in Sleep mode, the transmission path is disabled and the device is in Low-Power mode. Supply current from V_{BAT} is typically 9 µA. In

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Sleep mode, the LIN_INH pin is switched off. The internal termination between the LIN_BUS pin and LIN_V_{DD} pin is disabled.

Only a weak pull-up current (typically 10 µA) between the LIN_BUS pin and LIN_V_{DD} pin is present. Sleep mode can be activated independently from the actual level on the LIN_BUS or LIN_WKIN pin.

If the LIN_TXD pin is short-circuited to LIN_V_{SS}, it is possible to switch to Sleep mode via LIN_EN after t> t_{dom}.

18.2.5. Fail-safe Mode

The device automatically switches to Fail-Safe mode at system power-up or after a wake-up event. The LIN_INH output is switched on and the LIN transceiver is switched off. The IC stays in this mode until LIN_EN is switched to high. The IC then changes to Normal mode. During Fail-Safe mode, the LIN_TXD pin is an output, and together with the LIN_RXD output pin, signals the fail-safe source.

If the device enters Fail-Safe mode coming from the Normal mode (LIN_EN = 1) due to a VS undervoltage condition (V_{VS} < $V_{VS\_th\_N\_F\_down}$), it is possible to switch into Sleep mode by a falling edge at the LIN_EN input. With this feature, the current consumption is further reduced.

A wake-up event from Sleep mode is signaled to the microcontroller using the LIN_RXD pin and the LIN_TXD pin. A V_S undervoltage condition is also signaled at these two pins. The coding is shown in Table 18-2.

Table 18-2. Signaling In Fail-Safe Mode

Fail-Safe Sources	LIN_TXD(1)	LIN_RXD
LIN Wake-up (LIN_BUS pin)	Low	Low
Local Wake-up (LIN_WKIN pin)	Low	High
VS_{th} (battery) Undervoltage Detection, V_S < 3.9V	High	Low

Note:

1. Assuming an external pull-up resistor (typically 5 kW) has been added on pin LIN_TXD to the power supply of the microcontroller. Wake-up Scenarios from Sleep Mode.

18.2.6. FIGURE 17-4: LOCAL WAKE-UP FROM WAKE-UP SWITCH

18.3. Wake-up Scenarios from Sleep Mode

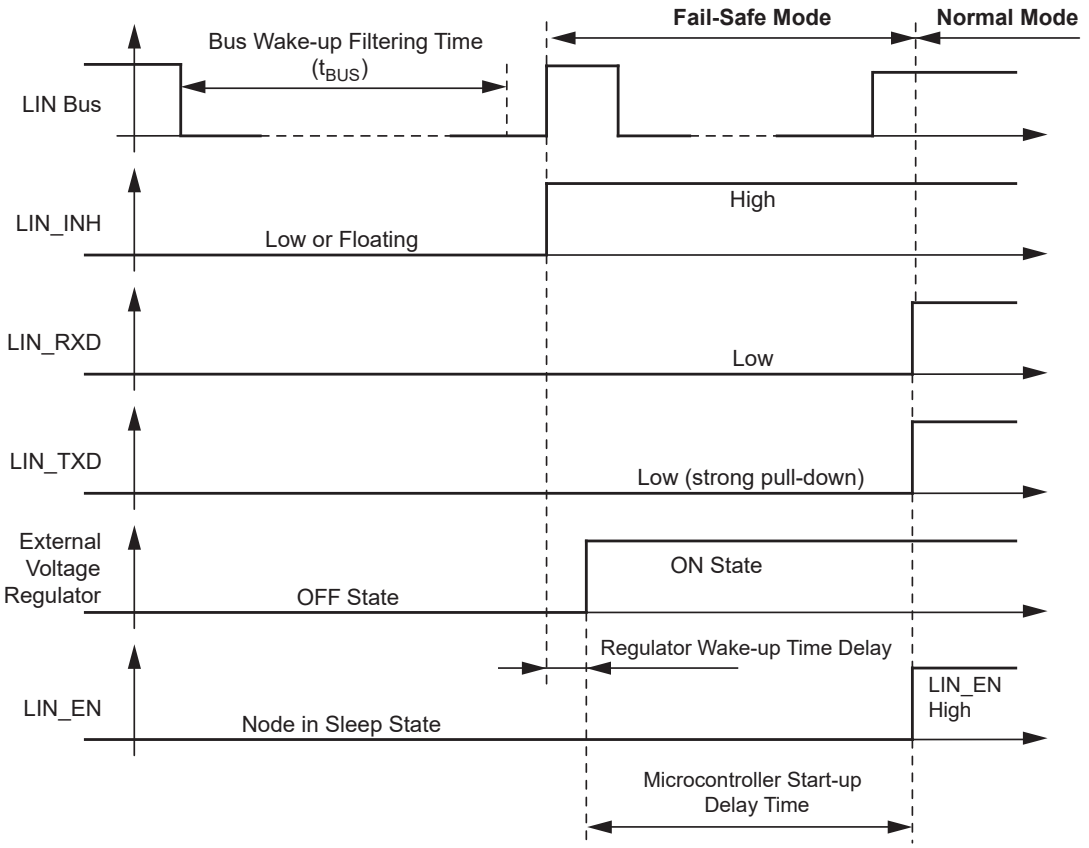
18.3.1. Remote Wake-Up Via LIN_BUS

18.3.1.1. Remote Wake-up from Sleep Mode

A voltage lower than the LIN pre-wake detection, V_{LINL} at the LIN_BUS pin, activates the internal LIN receiver, and starts the wake-up detection timer. A falling edge at the LIN_BUS pin, followed by a dominant bus level maintained for a certain period of time (>t_{bus}), and following a rising edge at the LIN_BUS pin, results in a remote wake-up request and the device switches to Fail-Safe mode. The LIN_INH pin is activated (switches to V_S), and the internal termination resistor is switched on. The remote wake-up request is indicated by a low level at pin LIN_RXD and interrupts the microcontroller.

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Figure 18-3. LIN Wake-Up from Sleep Mode

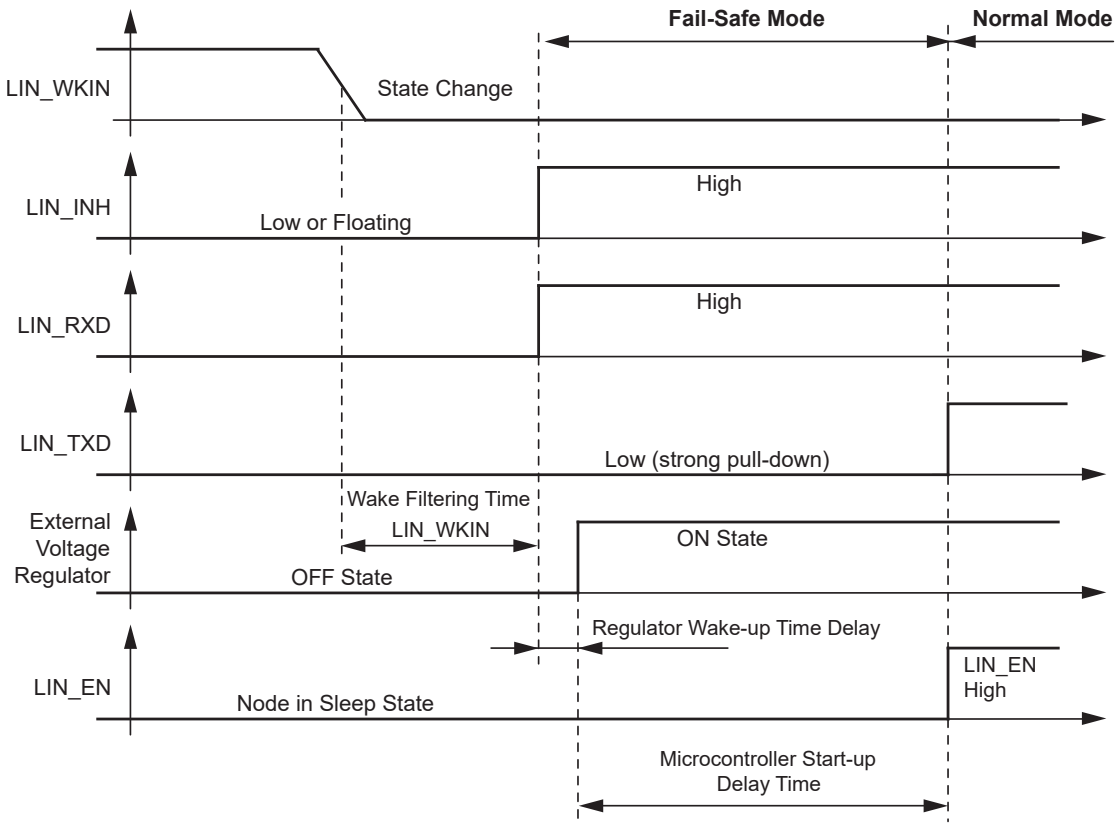


18.3.2. Local Wake-up Through LIN_WKIN Pin

A falling edge at the LIN_WKIN pin followed by a low level maintained for a certain period of time (>t_{WKin}) results in a local wake-up request and the device switches to Fail-Safe mode. The LIN_INH pin is activated (switches to V_S) and the internal Responder termination resistor is switched on. The local wake-up request is indicated by a low level at the LIN_TXD pin and a high level at the LIN_RXD pin, generating an interrupt for the microcontroller. Even when the LIN_WKIN pin is low, it is possible to switch to Sleep mode via the LIN_EN pin. In this case, the wake-up signal has to be switched to high >10 µs before the negative edge at LIN_WKIN starts a new local wake-up request.

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Figure 18-4. Local Wake-Up from Wake-Up Switch



18.3.3. Wake-up Source Recognition

The device can distinguish between different wake-up sources. The wake-up source can be read on the LIN_TXD and LIN_RXD pins in Fail-Safe mode, according to Table 17-3, if an external pull-up resistor (typically 5 kW) has been added on pin LIN_TXD to the power supply of the microcontroller. These flags are reset immediately if the microcontroller sets pin LIN_EN to high and the IC is in Normal mode.

Table 18-3. Signaling in Fail-Safe Mode

Fail-Safe Sources	LIN_TXD(1)	LIN_RXD
LIN Wake-up (LIN_BUS pin)	Low	Low
Local Wake-up (LIN_WKIN pin)	Low	High
VS_{th} (battery) Undervoltage Detection (V_S < 3.9V)	High	Low

Note:

1. Assuming an external pull-up resistor (typically 5 kW) has been added on pin LIN_TXD to the power supply of the microcontroller.

18.4. Behavior Under Low Supply Voltage Condition

After the battery voltage has been connected to the application circuit, the voltage at the LIN_V_{DD} pin increases according to the block capacitor used in the application (see Figure 18-1). If V_{VS} is higher than the minimum V_S operation threshold, $V_{VS\_th\_U\_F\_up}$, the IC mode changes from Unpowered mode to Fail-Safe mode, the LIN_INH output is switched on and the LIN transceiver can be activated.

If during Sleep mode, the voltage level of V_{VS} drops below the undervoltage detection threshold,$V_{VS\_th\_N\_F\_down}$ (typically 4.3V), the Operation mode is not changed and no wake-up is

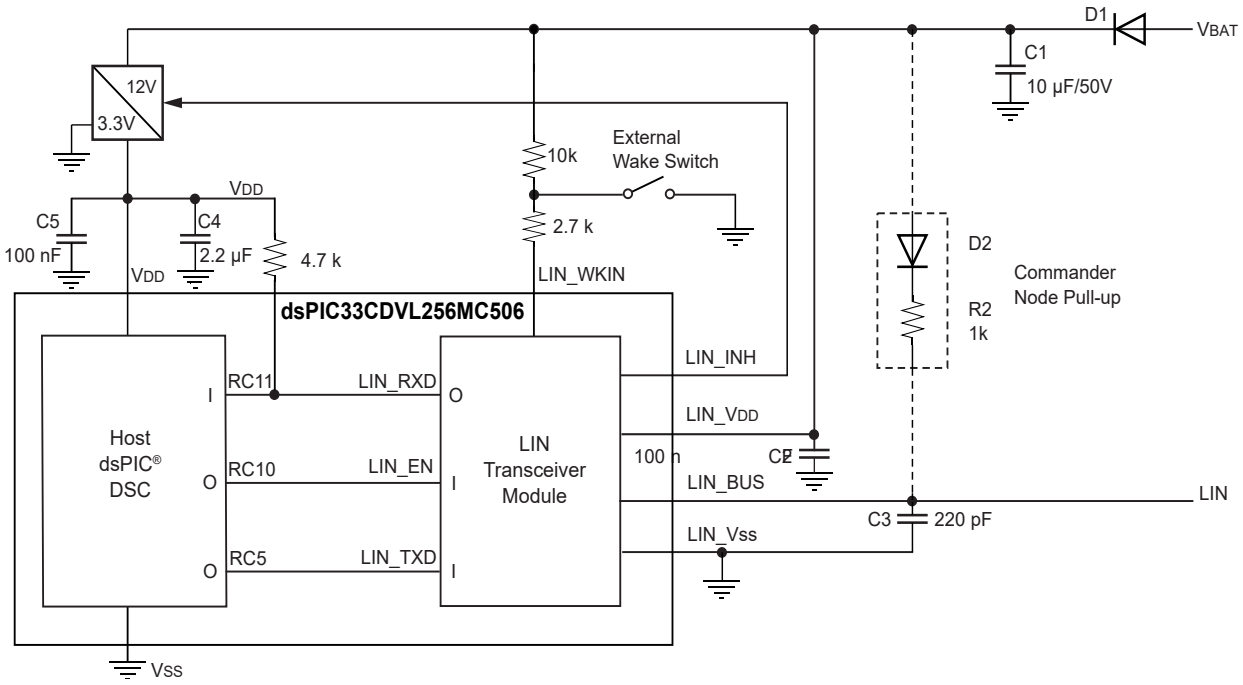
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possible. Only if the supply voltage on the LIN_V_{DD} pin drops below the VS operation threshold, $V_{VS\_th\_U\_F\_down}$ (typically 2.05V), does the IC switch to Unpowered mode.

If, during Normal mode, the voltage level on the LIN_V_{DD} pin drops below the VS undervoltage detection threshold, $V_{VS\_th\_N\_F\_down}$ (typically 4.3V), the IC switches to Fail-Safe mode. This means that the LIN transceiver is disabled in order to avoid malfunctions or false bus messages. If the supply voltage, V_{VS}, drops further below the V_S operation threshold, $V_{VS\_th\_U\_F\_down}$ (typically 2.05V), the IC switches to Unpowered mode and the LIN_INH output switches off.

18.5. Application Circuit

Figure 18-5. Typical Application Circuit



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19. Serial Peripheral Interface (SPI)

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Serial Peripheral Interface (SPI) with Audio Codec Support"** (www.microchip.com/DS70005136) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SPI module is compatible with the Motorola® SPI and SIOP interfaces. All devices in the dsPIC33CDVL256MC506 family include two SPI modules.

On 48-pin and 64-pin devices, the SPI instance, SPI2, can operate at higher speeds when selected as a non-PPS pin. The selection is done using the SPI2PIN bit (FDEVOPT[13]). If the bit for SPI2PIN is '1', the PPS pin will be used. When SPI2PIN is '0', the SPI signals are routed to dedicated pins.

The module supports operation in two Buffer modes. In Standard Buffer mode, data are shifted through a single serial buffer. In Enhanced Buffer mode, data are shifted through a FIFO buffer. The FIFO level depends on the configured mode.

Note: The FIFO depth for this device is four (in 8-Bit Data mode).

Variable length data can be transmitted and received, ranging from 2 to 32 bits.

Note: Do not perform Read-Modify-Write operations (such as bit-oriented instructions) on the SPIxBUF register in either Standard or Enhanced Buffer mode.

The module also supports a basic framed SPI protocol while operating in either Host or Client mode. A total of four framed SPI configurations are supported.

The module also supports Audio modes. Four different Audio modes are available.

- I^2S mode
- Left Justified mode
- Right Justified mode
- PCM/DSP mode

If an audio protocol data transfer takes place between two devices, one device is usually the Host and the other is the Client. However, audio data can be transferred between two Clients. Because the audio protocols require free-running clocks, the Host can be a third-party controller. In either case, the Host generates two free-running clocks: SCKx and LRC (Left, Right Channel Clock/$\overline{SSx}$/FSYNC). In each of these modes, the serial clock is free-running and audio data are always transferred.

The SPI serial interface consists of four pins:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- $\overline{SSx}$: Active-Low Client Select or Frame Synchronization I/O Pulse

The SPI module can be configured to operate using two, three or four pins. In the 3-pin mode, $\overline{SSx}$ is not used. In the 2-pin mode, both SDOx and $\overline{SSx}$ are not used.

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The SPI module has the ability to generate three interrupts, reflecting the events that occur during the data communication. The following types of interrupts can be generated:

1. Receive interrupts are signaled by SPIxRXIF. This event occurs when:
   - RX watermark interrupt
   - SPIROV = 1
   - SPIRBF = 1
   - SPIRBE = 1

   provided the respective mask bits are enabled in SPIxIMSKL/H.
2. Transmit interrupts are signaled by SPIxTXIF. This event occurs when:
   - TX watermark interrupt
   - SPITUR = 1
   - SPITBF = 1
   - SPITBE = 1

   provided the respective mask bits are enabled in SPIxIMSKL/H.
3. General interrupts are signaled by SPIxGIF. This event occurs when:
   - FRMERR = 1
   - SPIBUSY = 1
   - SRMT = 1

   provided the respective mask bits are enabled in SPIxIMSKL/H.

Block diagrams of the module in Standard and Enhanced modes are shown in Figure 19-1 and Figure 19-2.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1, SPI2 or SPI3. Special Function Registers will follow a similar notation. For example, SPIxCON1 and SPIxCON2 refer to the control registers for any of the three SPI modules.

To set up the SPIx module for the Standard Host mode of operation:

1. If using interrupts:
   a. Clear the interrupt flag bits in the respective IFSx register.
   b. Set the interrupt enable bits in the respective IECx register.
   c. Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
2. Write the desired settings to the SPIxCON1L and SPIxCON1H registers with the MSTEN bit (SPIxCON1L[5]) = 1.
3. Clear the SPIROV bit (SPIxSTATL[6]).
4. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L[15]).
5. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data are written to the SPIxBUFL and SPIxBUFH registers.

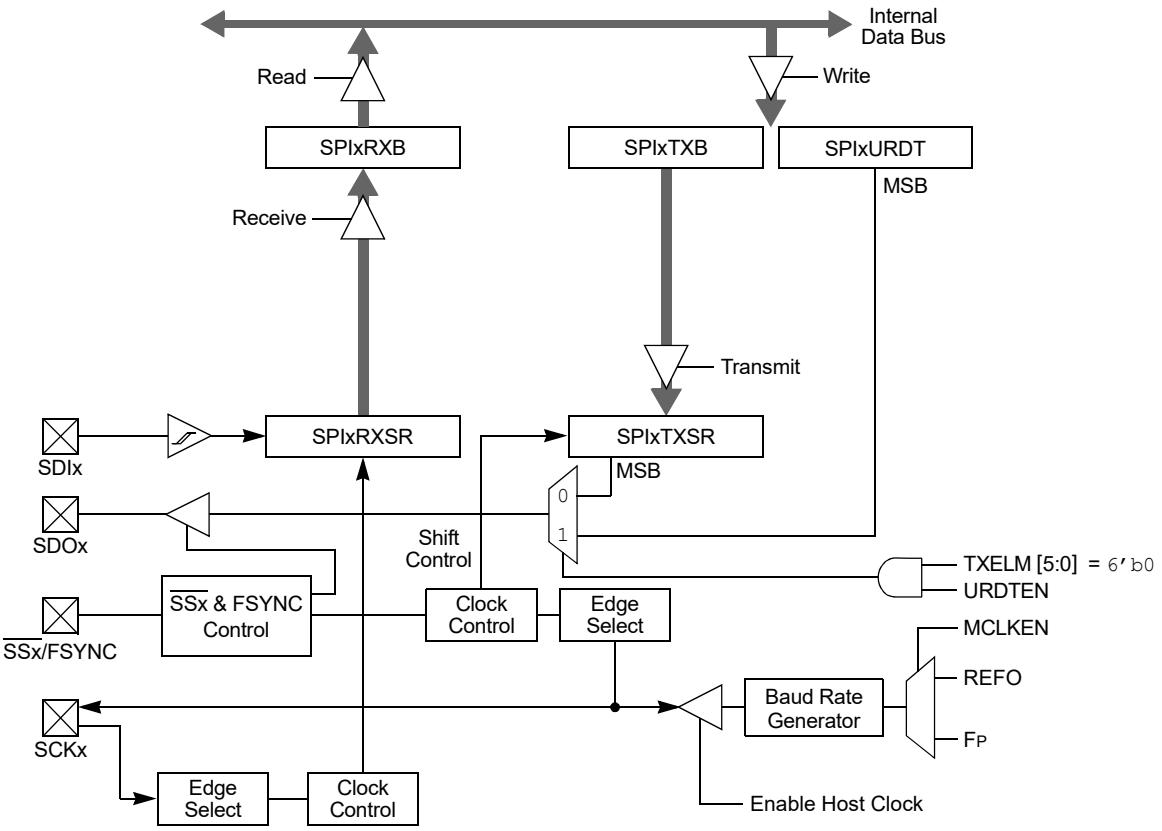
To set up the SPIx module for the Standard Client mode of operation:

1. Clear the SPIxBUF registers.
2. If using interrupts:
   a. Clear the SPIxBUFL and SPIxBUFH registers.
   b. Set the interrupt enable bits in the respective IECx register.
   c. Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.

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3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with the MSTEN bit (SPIxCON1L[5]) = 0.
4. Clear the SMP bit.
5. If the CKE bit (SPIxCON1L[8]) is set, then the SSEN bit (SPIxCON1L[7]) must be set to enable the $\overline{SSx}$ pin.
6. Clear the SPIROV bit (SPIxSTATL[6]).
7. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L[15]).

Figure 19-1. SPIx Module Block Diagram (Standard Mode)



To set up the SPIx module for the Enhanced Buffer Host mode of operation:

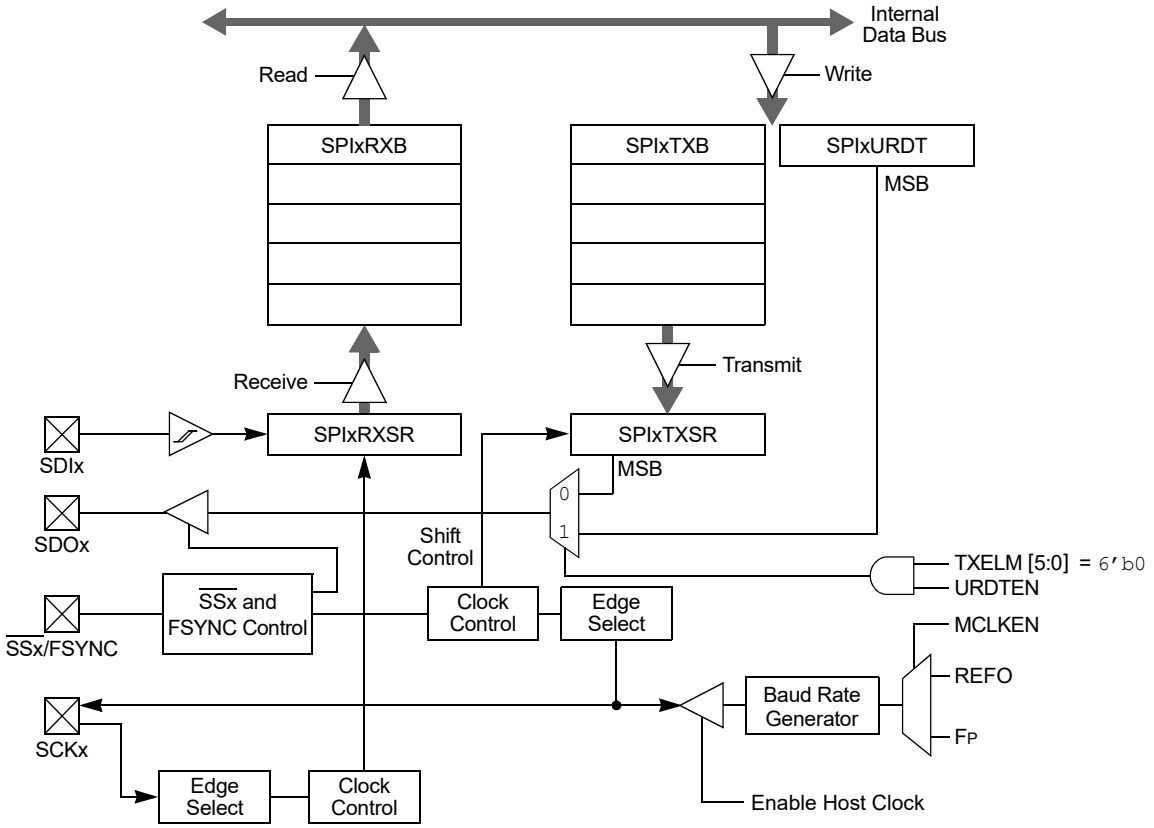
1. If using interrupts:
   a. Clear the interrupt flag bits in the respective IFSx register.
   b. Set the interrupt enable bits in the respective IECx register.
   c. Write the SPIxIP bits in the respective IPCx register.
2. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with MSTEN (SPIxCON1L[5]) = 1.
3. Clear the SPIROV bit (SPIxSTATL[6]).
4. Select Enhanced Buffer mode by setting the ENHBUF bit (SPIxCON1L[0]).
5. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L[15]).
6. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data are written to the SPIxBUFL and SPIxBUFH registers.

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To set up the SPIx module for the Enhanced Buffer Client mode of operation:

1. Clear the SPIxBUFL and SPIxBUFH registers.
2. If using interrupts:
   Clear the interrupt flag bits in the respective IFSx register.
   Set the interrupt enable bits in the respective IECx register.
   Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with the MSTEN bit (SPIxCON1L[5]) = 0.
4. Clear the SMP bit.
5. If the CKE bit is set, then the SSEN bit must be set, thus enabling the $\overline{SSx}$ pin.
6. Clear the SPIROV bit (SPIxSTATL[6]).
7. Select Enhanced Buffer mode by setting the ENHBUF bit (SPIxCON1L[0]).
8. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L[15]).

Figure 19-2. SPIx Module Block Diagram (Enhanced Mode)



To set up the SPIx module for Audio mode:

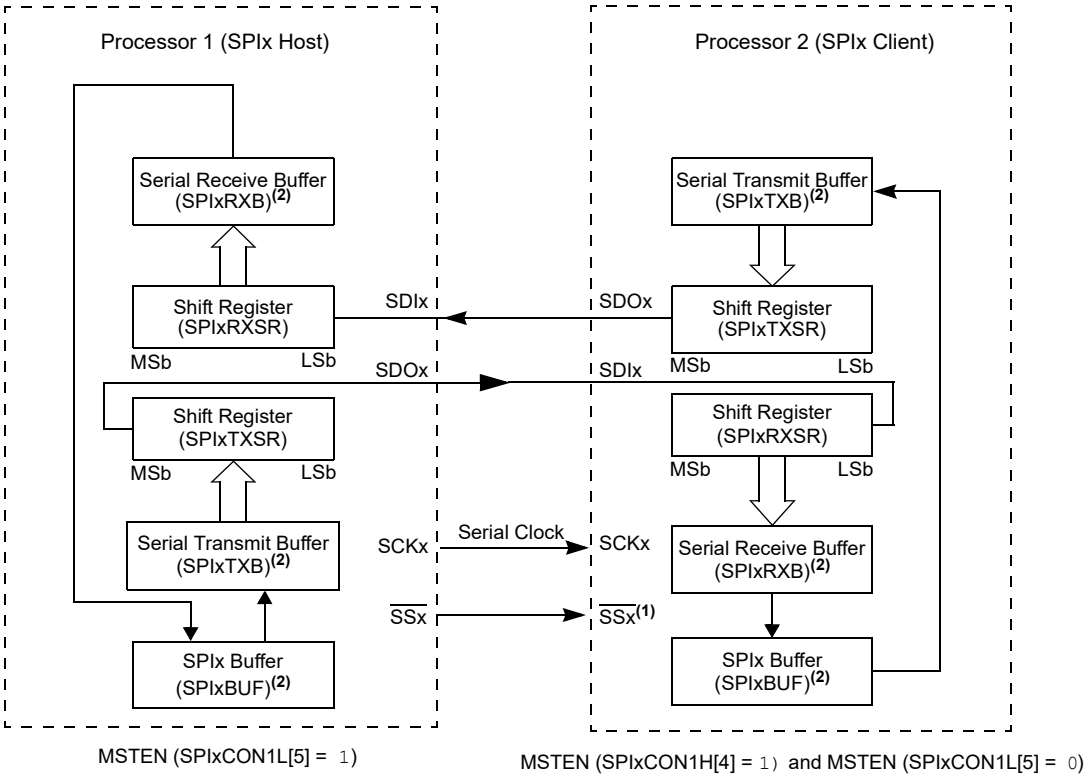
1. Clear the SPIxBUFL and SPIxBUFH registers.
2. If using interrupts:
   a. Clear the interrupt flag bits in the respective IFSx register.
   b. Set the interrupt enable bits in the respective IECx register.

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c. Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.

3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with AUDEN (SPIxCON1H[15]) = 1.
4. Clear the SPIROV bit (SPIxSTATL[6]).
5. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L[15]).
6. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data are written to the SPIxBUFL and SPIxBUFH registers.

Figure 19-3. SPIx Host/Client Connection (Standard Mode)

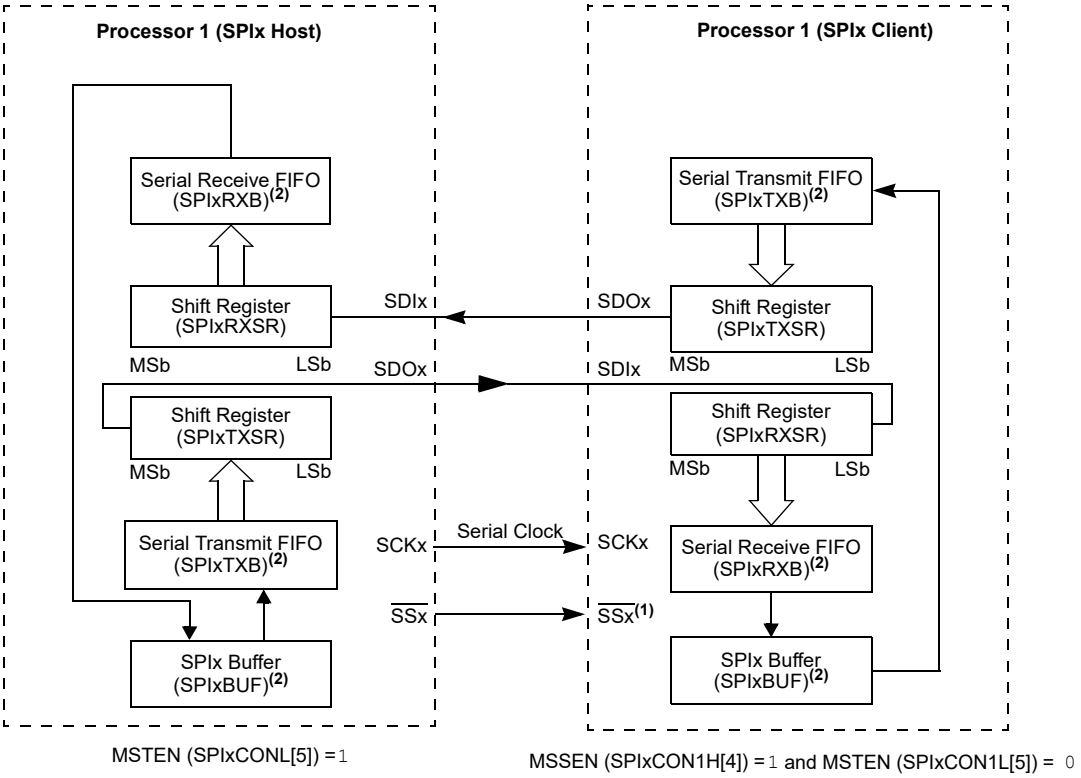


Note 1: Using the $\overline{SSx}$ pin in Client mode of operation is optional.

2: User must write transmit data to read the received data from SPIxBUF. The SPIxTXB and SPIxRXB registers are memory-mapped to SPIxBUF.

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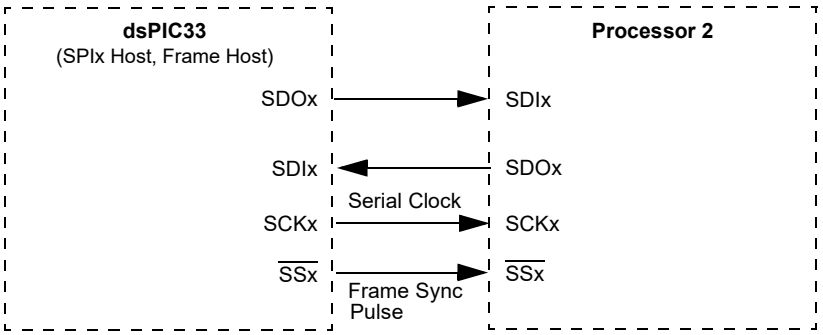
Figure 19-4. SPIx Host/Client Connection (Enhanced Buffer Modes)



Note 1: Using the $\overline{SSx}$ pin in Client mode is optional.

2: User must write transmit data to read the received data from SPIxBUF. The SPIxTXB and SPIxRXB registers are memory-mapped to SPIxBUF.

Figure 19-5. SPIx Host, Frame Host Connection Diagram



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Figure 19-6. SPIx Host, Frame Client Connection Diagram

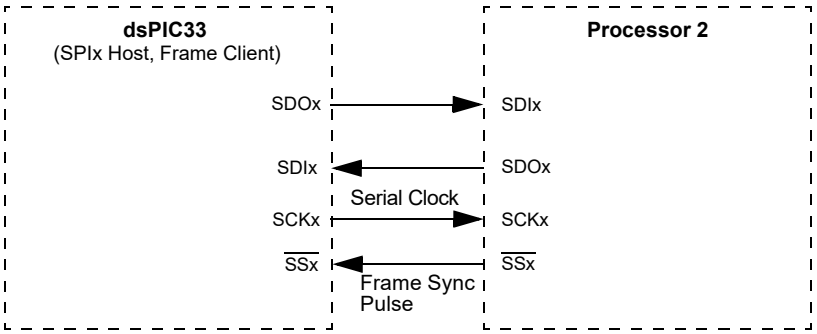


Figure 19-7. SPIx Client, Frame Host Connection Diagram

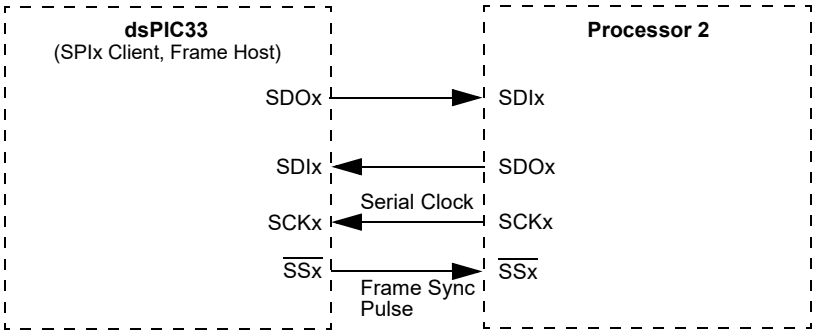
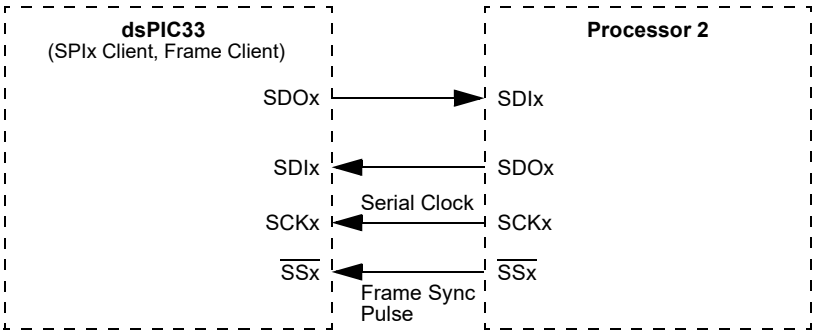


Figure 19-8. SPIx Client, Frame Client Connection Diagram



Equation 19-1. Relationship Between Device and SPIx Clock Speed

$$Baud\ Rate = \frac{FPB}{(2 * (SPIxBRG + 1))}$$

Where:

FPB is the Peripheral Bus Clock Frequency.

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19.1. SPI Control/Status Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x02AC	SPI1CON1L	15:8	SPIEN		SPISIDL	DISSDO	MODE32 and MODE16[1:0]		SMP	CKE
		7:0	SSEN	CKP	MSTEN	DISSDI	DISSCK	MCLKEN	SPIFE	ENHBUF
0x02AE	SPI1CON1H	15:8	AUDEN	SPISGNEXT	IGNROV	IGNTUR	AUDMONO	URDTEN	AUDMOD[1:0]	
		7:0	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT[2:0]		
0x02B0	SPI1CON2L	15:8								
		7:0	WLENGTH[4:0]							
0x02B2 ... 0x02B3	Reserved									
0x02B4	SPI1STATL	15:8				FRMERR	SPIBUSY			SPITUR
		7:0	SRMT	SPIROV	SPIRBE		SPITBE		SPITBF	SPIRBF
0x02B6	SPI1STATH	15:8			RXELM[5:0]					
		7:0			TXELM[5:0]					
0x02B8	SPI1BUFL	15:8	DATA[15:8]							
		7:0	DATA[7:0]							
0x02BA	SPI1BUFH	15:8	DATA[31:24]							
		7:0	DATA[23:16]							
0x02BC	SPI1BRGL	15:8				BRG[12:8]				
		7:0	BRG[7:0]							
0x02BE ... 0x02BF	Reserved									
0x02C0	SPI1IMSKL	15:8				FRMERREN	BUSYEN			SPITUREN
		7:0	SRMTEN	SPIROVEN	SPIRBEN		SPITBEN		SPITBFEN	SPIRBFEN
0x02C2	SPI1IMSKH	15:8	RXWIEN		RXMSK[5:0]					
		7:0	TXWIEN		TXMSK[5:0]					
0x02C4	SPI1URDTL	15:8	SPI1URDTL[15:8]							
		7:0	SPI1URDTL[7:0]							
0x02C6	SPI1URDTH	15:8	SPI1URDTH[31:24]							
		7:0	SPI1URDTH[23:16]							
0x02C8	SPI2CON1L	15:8	SPIEN		SPISIDL	DISSDO	MODE32 and MODE16[1:0]		SMP	CKE
		7:0	SSEN	CKP	MSTEN	DISSDI	DISSCK	MCLKEN	SPIFE	ENHBUF
0x02CA	SPI2CON1H	15:8	AUDEN	SPISGNEXT	IGNROV	IGNTUR	AUDMONO	URDTEN	AUDMOD[1:0]	
		7:0	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT[2:0]		
0x02CC	SPI2CON2L	15:8								
		7:0	WLENGTH[4:0]							
0x02CE ... 0x02CF	Reserved									
0x02D0	SPI2STATL	15:8				FRMERR	SPIBUSY			SPITUR
		7:0	SRMT	SPIROV	SPIRBE		SPITBE		SPITBF	SPIRBF
0x02D2	SPI2STATH	15:8			RXELM[5:0]					
		7:0			TXELM[5:0]					
0x02D4	SPI2BUFL	15:8	DATA[15:8]							
		7:0	DATA[7:0]							
0x02D6	SPI2BUFH	15:8	DATA[31:24]							
		7:0	DATA[23:16]							
0x02D8	SPI2BRGL	15:8				BRG[12:8]				
		7:0	BRG[7:0]							
0x02DA ... 0x02DB	Reserved									
0x02DC	SPI2IMSKL	15:8				FRMERREN	BUSYEN			SPITUREN
		7:0	SRMTEN	SPIROVEN	SPIRBEN		SPITBEN		SPITBFEN	SPIRBFEN
0x02DE	SPI2IMSKH	15:8	RXWIEN		RXMSK[5:0]					
		7:0	TXWIEN		TXMSK[5:0]					
0x02E0	SPI2URDTL	15:8	SPI2URDTL[15:8]							
		7:0	SPI2URDTL[7:0]							

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SPI Control/Status Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x02E2	SPI2URDTH	15:8	SPI2URDTH[31:24]							
		7:0	SPI2URDTH[23:16]							

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19.1.1. SPIx Control Register 1 Low

Name: SPIxCON1L
Offset: 0x2AC, 0x2C8

Notes:

1. When AUDEN = 1, this module functions as if CKE = 0, regardless of its actual value.
2. When FRMEN = 1, SSEN is not used.
3. MCLKEN can only be written when the SPIEN bit = 0.
4. This channel is not meaningful for DSP/PCM mode as LRC follows FRMSYPW.

Bit	15	14	13	12	11	10	9	8
	SPIEN		SPISIDL	DISSDO	MODE32 and MODE16[1:0]		SMP	CKE
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SSEN	CKP	MSTEN	DISSDI	DISSCK	MCLKEN	SPIFE	ENHBUF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – SPIEN SPIx On bit

Value	Description
1	Enables module.
0	Turns off and resets module, disables clocks, disables interrupt event generation and allows SFR modifications.

Bit 13 – SPISIDL SPIx Stop in Idle Mode bit

Value	Description
1	Halts in CPU Idle mode.
0	Continues to operate in CPU Idle mode.

Bit 12 – DISSDO Disable SDOx Output Port bit

Value	Description
1	SDOx pin is not used by the module; pin is controlled by port function.
0	SDOx pin is controlled by the module.

Bits 11:10 – MODE32 and MODE16[1:0] Serial Word Length Select bits(1,4)

MODE32	MODE16	AUDEN	Communication
1	x	0	32-Bit
0	1		16-Bit
0	0		8-Bit
1	1	1	24-Bit Data, 32-Bit FIFO, 32-Bit Channel/64-Bit Frame
1	0		32-Bit Data, 32-Bit FIFO, 32-Bit Channel/64-Bit Frame
0	1		16-Bit Data, 16-Bit FIFO, 32-Bit Channel/64-Bit Frame
0	0		16-Bit FIFO, 16-Bit Channel/32-Bit Frame

Bit 9 – SMP SPIx Data Input Sample Phase bit

Client Mode:
Input data are always sampled at the middle of data output time, regardless of the SMP setting.
Host Mode:

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Value	Description
1	Input data are sampled at the end of data output time.
0	Input data are sampled at the middle of data output time.

Bit 8 – CKE SPIx Clock Edge Select bit(1)

Value	Description
1	Transmit happens on transition from active clock state to Idle clock state.
0	Transmit happens on transition from Idle clock state to active clock state.

Bit 7 – SSEN Client Select Enable bit (Client mode)(2)

Value	Description
1	$\overline{SSx}$ pin is used by the macro in Client mode; $\overline{SSx}$ pin is used as the Client select input.
0	$\overline{SSx}$ pin is not used by the macro ($\overline{SSx}$ pin will be controlled by the port I/O).

Bit 6 – CKP Clock Polarity Select bit

Value	Description
1	Idle state for clock is a high level; active state is a low level.
0	Idle state for clock is a low level; active state is a high level.

Bit 5 – MSTEN Host Mode Enable bit

Value	Description
1	Host mode
0	Client mode

Bit 4 – DISSDI Disable SDIx Input Port bit

Value	Description
1	SDIx pin is not used by the module; pin is controlled by port function.
0	SDIx pin is controlled by the module.

Bit 3 – DISSCK Disable SCKx Output Port bit

Value	Description
1	SCKx pin is not used by the module; pin is controlled by port function.
0	SCKx pin is controlled by the module.

Bit 2 – MCLKEN Master Clock Enable bit(3)

Value	Description
1	REFO is used by the BRG.
0	F_P is used by the BRG.

Bit 1 – SPIFE Frame Sync Pulse Edge Select bit

Value	Description
1	Frame Sync pulse (Idle-to-active edge) coincides with the first bit clock.
0	Frame Sync pulse (Idle-to-active edge) precedes the first bit clock.

Bit 0 – ENHBUF Enhanced Buffer Enable bit

Value	Description
1	Enhanced Buffer mode is enabled.
0	Enhanced Buffer mode is disabled.

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19.1.2. SPIx Control Register 1 High

Name: SPIxCON1H
Offset: 0x2AE, 0x2CA

Notes:

1. AUDEN can only be written when the SPIEN bit = 0.
2. AUDMONO can only be written when the SPIEN bit = 0 and is only valid for AUDEN = 1.
3. URDTEN is only valid when IGNTUR = 1.
4. The AUDMOD[1:0] bits can only be written when the SPIEN bit = 0 and are only valid when AUDEN = 1. When NOT in PCM/DSP mode, this module functions as if FRMSYPW = 1, regardless of its actual value.

Bit	15	14	13	12	11	10	9	8
	AUDEN	SPISGNEXT	IGNROV	IGNTUR	AUDMONO	URDTEN	AUDMOD[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – AUDEN Audio Codec Support Enable bit(1)

Value	Description
1	Audio protocol is enabled; MSTEN controls the direction of both SCKx and frame (a.k.a. LRC), and this module functions as if FRMEN = 1, FRMSYNC = MSTEN, FRMCNT[2:0] = 001 and SMP = 0, regardless of their actual values.
0	Audio protocol is disabled.

Bit 14 – SPISGNEXT SPIx Sign-Extend RX FIFO Read Data Enable bit

Value	Description
1	Data from RX FIFO are sign-extended.
0	Data from RX FIFO are not sign-extended.

Bit 13 – IGNROV Ignore Receive Overflow bit

Value	Description
1	A Receive Overflow (ROV) is NOT a critical error; during ROV, data in the FIFO are not overwritten by the received data.
0	An ROV is a critical error that stops SPI operation.

Bit 12 – IGNTUR Ignore Transmit Underrun bit

Value	Description
1	A Transmit Underrun (TUR) is NOT a critical error and data indicated by URDTEN are transmitted until the SPIxTXB is not empty.
0	A TUR is a critical error that stops SPI operation.

Bit 11 – AUDMONO Audio Data Format Transmit bit(2)

Value	Description
1	Audio data are mono (i.e., each data word is transmitted on both left and right channels).
0	Audio data are stereo.

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Bit 10 – URDTEN Transmit Underrun Data Enable bit(3)

Value	Description
1	Transmits data out of SPIxURDT register during Transmit Underrun conditions.
0	Transmits the last received data during Transmit Underrun conditions.

Bits 9:8 – AUDMOD[1:0] Audio Protocol Mode Selection bits(4)

Value	Description
11	PCM/DSP mode
10	Right Justified mode: This module functions as if SPIFE = 1, regardless of its actual value.
01	Left Justified mode: This module functions as if SPIFE = 1, regardless of its actual value.
00	I^2S mode: This module functions as if SPIFE = 0, regardless of its actual value.

Bit 7 – FRMEN Framed SPIx Support bit

Value	Description
1	Framed SPIx support is enabled ($\overline{SSx}$ pin is used as the FSYNC input/output).
0	Framed SPIx support is disabled.

Bit 6 – FRMSYNC Frame Sync Pulse Direction Control bit

Value	Description
1	Frame Sync pulse input (Client).
0	Frame Sync pulse output (Host).

Bit 5 – FRMPOL Frame Sync/Client Select Polarity bit

Value	Description
1	Frame Sync pulse/Client select is active-high.
0	Frame Sync pulse/Client select is active-low.

Bit 4 – MSSEN Host Mode Client Select Enable bit

Value	Description
1	SPIx Client select support is enabled with polarity determined by FRMPOL ($\overline{SSx}$ pin is automatically driven during transmission in Host mode).
0	Client select SPIx support is disabled ($\overline{SSx}$ pin will be controlled by port I/O).

Bit 3 – FRMSYPW Frame Sync Pulse-Width bit

Value	Description
1	Frame Sync pulse is one serial word length wide (as defined by MODE[32,16]/WLENGTH[4:0]).
0	Frame Sync pulse is one clock (SCKx) wide.

Bits 2:0 – FRMCNT[2:0] Frame Sync Pulse Counter bits
Controls the number of serial words transmitted per Sync pulse.

Value	Description
111	Reserved
110	Reserved
101	Generates a Frame Sync pulse every 32 serial words.
100	Generates a Frame Sync pulse every 16 serial words.
011	Generates a Frame Sync pulse every 8 serial words.
010	Generates a Frame Sync pulse every 4 serial words.
001	Generates a Frame Sync pulse every 2 serial words (value used by audio protocols).
000	Generates a Frame Sync pulse each serial word.

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19.1.3. SPIx Control Register 2 Low

Name: SPIxCON2L
Offset: 0x2B0, 0x2CC

Notes:

1. These bits are effective when AUDEN = 0 only.
2. Varying the length by changing these bits does not affect the depth of the TX/RX FIFO.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				WLENGTH[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – WLENGTH[4:0] Variable Word Length bits(1,2)

Value	Description
11111	32-bit data
11110	31-bit data
11101	30-bit data
11100	29-bit data
11011	28-bit data
11010	27-bit data
11001	26-bit data
11000	25-bit data
10111	24-bit data
10110	23-bit data
10101	22-bit data
10100	21-bit data
10011	20-bit data
10010	19-bit data
10001	18-bit data
10000	17-bit data
01111	16-bit data
01110	15-bit data
01101	14-bit data
01100	13-bit data
01011	12-bit data
01010	11-bit data
01001	10-bit data
01000	9-bit data
00111	8-bit data
00110	7-bit data
00101	6-bit data
00100	5-bit data
00011	4-bit data
00010	3-bit data
00001	2-bit data
00000	See MODE[32,16] bits in SPIxCON1L[11:10]

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19.1.4. SPIx Status Register Low

Name: SPIxSTATL
Offset: 0x2B4, 0x2D0

Note:

1. SPITUR is cleared when SPIEN = 0. When IGNTUR = 1, SPITUR provides the dynamic status of the Transmit Underrun condition, but does not stop RX/TX operation and does not need to be cleared by software.

Legend: C = Clearable bit; HS = Hardware Settable bit; HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
				FRMERR	SPIBUSY			SPITUR
Access				R/C/HS	R/HSC			R/HSC
Reset				0	0			0

Bit	7	6	5	4	3	2	1	0
	SRMT	SPIROV	SPIRBE		SPITBE		SPITBF	SPIRBF
Access	R/HSC	R/C/HS	R/HSC		R/HSC		R/HSC	R/HSC
Reset	0	0	1		1		0	0

Bit 12 – FRMERR SPIx Frame Error Status bit

Value	Description
1	Frame error is detected.
0	No frame error is detected.

Bit 11 – SPIBUSY SPIx Activity Status bit

Value	Description
1	Module is currently busy with some transactions.
0	No ongoing transactions (at time of read).

Bit 8 – SPITUR SPIx Transmit Underrun Status bit(1)

Value	Description
1	Transmit buffer has encountered a Transmit Underrun condition.
0	Transmit buffer does not have a Transmit Underrun condition.

Bit 7 – SRMT Shift Register Empty Status bit

Value	Description
1	No current or pending transactions (i.e., neither SPIxTXB or SPIxTXSR contains data to transmit).
0	Current or pending transactions.

Bit 6 – SPIROV SPIx Receive Overflow Status bit

Value	Description
1	A new byte/half-word/word has been completely received when the SPIxRXB was full.
0	No overflow.

Bit 5 – SPIRBE SPIx RX Buffer Empty Status bit

Standard Buffer mode:
Automatically set in hardware when SPIxBUF is read from, reading SPIxRXB. Automatically cleared in hardware when SPIx transfers data from SPIxRXSR to SPIxRXB.
Enhanced Buffer mode:

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Indicates RXELM[5:0] = 000000.

Value	Description
1	RX buffer is empty.
0	RX buffer is not empty.

Bit 3 – SPITBE SPIx Transmit Buffer Empty Status bit

Standard Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxTXB to SPIxTXSR. Automatically cleared in hardware when SPIxBUF is written, loading SPIxTXB.
Enhanced Buffer mode:
Indicates TXELM[5:0] = 000000.

Value	Description
1	SPIxTXB is empty.
0	SPIxTXB is not empty.

Bit 1 – SPITBF SPIx Transmit Buffer Full Status bit

Standard Buffer mode:
Automatically set in hardware when SPIxBUF is written, loading SPIxTXB. Automatically cleared in hardware when SPIx transfers data from SPIxTXB to SPIxTXSR.
Enhanced Buffer mode:
Indicates TXELM[5:0] = 111111.

Value	Description
1	SPIxTXB is full.
0	SPIxTXB not full.

Bit 0 – SPIRBF SPIx Receive Buffer Full Status bit

Standard Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxRXSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer mode:
Indicates RXELM[5:0] = 111111.

Value	Description
1	SPIxRXB is full.
0	SPIxRXB is not full.

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19.1.5. SPIx Status Register High

Name: SPIxSTATH
Offset: 0x2B6, 0x2D2

Notes:
1. RXELM3 and TXELM3 bits are only present when FIFODEPTH = 8 or higher.
2. RXELM4 and TXELM4 bits are only present when FIFODEPTH = 16 or higher.
3. RXELM5 and TXELM5 bits are only present when FIFODEPTH = 32.

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
			RXELM[5:0]					
Access			R/HSC	R/HSC	R/HSC	R/HSC	R/HSC	R/HSC
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			TXELM[5:0]					
Access			R/HSC	R/HSC	R/HSC	R/HSC	R/HSC	R/HSC
Reset			0	0	0	0	0	0

Bits 13:8 – RXELM[5:0] Receive Buffer Element Count bits (valid in Enhanced Buffer mode)(1,2,3)

Bits 5:0 – TXELM[5:0] Transmit Buffer Element Count bits (valid in Enhanced Buffer mode)(1,2,3)

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19.1.6. SPIx Buffer Register Low

Name: SPIxBUFL
Offset: 0x2B8, 0x2D4

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DATA[15:0] SPI FIFO Data bits

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19.1.7. SPIx Buffer Register High

Name: SPIxBUFH
Offset: 0x2BA, 0x2D6

Bit	15	14	13	12	11	10	9	8
	DATA[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DATA[31:16] SPI FIFO Data bits

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19.1.8. SPIx Baud Rate Generator Register Low

Name: SPIxBRGL
Offset: 0x2BC, 0x2D8

Note:

1. Changing the BRG value when SPIEN = 1 causes undefined behavior.

Bit	15	14	13	12	11	10	9	8
				BRG[12:8]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BRG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 12:0 – BRG[12:0] SPI Baud Rate Generator Divisor bits(1)

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19.1.9. SPIx Interrupt Mask Register Low

Name: SPIxIMSKL
Offset: 0x2C0, 0x2DC

Bit	15	14	13	12	11	10	9	8
				FRMERREN	BUSYEN			SPITUREN
Access				R/W	R/W			R/W
Reset				0	0			0

Bit	7	6	5	4	3	2	1	0
	SRMTEN	SPIROVEN	SPIRBEN		SPITBEN		SPITBFEN	SPIRBFEN
Access	R/W	R/W	R/W		R/W		R/W	R/W
Reset	0	0	0		0		0	0

Bit 12 – FRMERREN Enable Interrupt Events via FRMERR bit

Value	Description
1	Frame error generates an interrupt event.
0	Frame error does not generate an interrupt event.

Bit 11 – BUSYEN Enable Interrupt Events via SPIBUSY bit

Value	Description
1	SPIBUSY generates an interrupt event.
0	SPIBUSY does not generate an interrupt event.

Bit 8 – SPITUREN Enable Interrupt Events via SPITUR bit

Value	Description
1	Transmit Underrun (TUR) generates an interrupt event.
0	Transmit Underrun does not generate an interrupt event.

Bit 7 – SRMTEN Enable Interrupt Events via SRMT bit

Value	Description
1	Shift Register Empty (SRMT) generates interrupt events.
0	Shift Register Empty does not generate interrupt events.

Bit 6 – SPIROVEN Enable Interrupt Events via SPIROV bit

Value	Description
1	SPIx Receive Overflow (ROV) generates an interrupt event.
0	SPIx Receive Overflow does not generate an interrupt event.

Bit 5 – SPIRBEN Enable Interrupt Events via SPIRBE bit

Value	Description
1	SPIx RX buffer empty generates an interrupt event.
0	SPIx RX buffer empty does not generate an interrupt event.

Bit 3 – SPITBEN Enable Interrupt Events via SPITBE bit

Value	Description
1	SPIx transmit buffer empty generates an interrupt event.
0	SPIx transmit buffer empty does not generate an interrupt event.

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Bit 1 – SPITBFEN Enable Interrupt Events via SPITBF bit

Value	Description
1	SPIx transmit buffer full generates an interrupt event.
0	SPIx transmit buffer full does not generate an interrupt event.

Bit 0 – SPIRBFEN Enable Interrupt Events via SPIRBF bit

Value	Description
1	SPIx receive buffer full generates an interrupt event.
0	SPIx receive buffer full does not generate an interrupt event.

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19.1.10. SPIx Interrupt Mask Register High

Name: SPIxIMSKH
Offset: 0x2C2, 0x2DE

Notes:

1. Mask values higher than FIFODEPTH are not valid. The module will not trigger a match for any value in this case.
2. RXMSK2 and TXMSK2 bits are only present when FIFODEPTH = 8 or higher.
3. RXMSK3 and TXMSK3 bits are only present when FIFODEPTH = 16 or higher.
4. RXMSK4 and TXMSK4 bits are only present when FIFODEPTH = 32.

Bit	15	14	13	12	11	10	9	8
	RXWIEN		RXMSK[5:0]					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXWIEN		TXMSK[5:0]					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 15 – RXWIEN Receive Watermark Interrupt Enable bit

Value	Description
1	Triggers receive buffer element watermark interrupt when RXMSK[5:0] ≤ RXELM[5:0].
0	Disables receive buffer element watermark interrupt.

Bits 13:8 – RXMSK[5:0] RX Buffer Mask bits(1,2,3,4)
RX mask bits; used in conjunction with the RXWIEN bit.

Bit 7 – TXWIEN Transmit Watermark Interrupt Enable bit

Value	Description
1	Triggers transmit buffer element watermark interrupt when TXMSK[5:0] = TXELM[5:0].
0	Disables transmit buffer element watermark interrupt.

Bits 5:0 – TXMSK[5:0] TX Buffer Mask bits(1,2,3,4)
TX mask bits; used in conjunction with the TXWIEN bit.

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19.1.11. SPIx Underrun Data Register Low

Name: SPIxURDTL
Offset: 0x2C4, 0x2E0

Bit	15	14	13	12	11	10	9	8
	SPIxURDTL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SPIxURDTL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SPIxURDTL[15:0] SPI Underrun Data bits

These bits are only used when URDTEN = 1. This register holds the data to transmit when a Transmit Underrun condition occurs.
When the MODE[32:16] or WLENGTH[4:0] bits select 16 to 9-bit data, the SPIx only uses URDATA[15:0]. When the MODE[32:16] or WLENGTH[4:0] bits select 8 to 2-bit data, the SPIx only uses URDATA[7:0].

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19.1.12. SPIx Underrun Data Register Low

Name: SPIxURDTH
Offset: 0x2C6, 0x2E2

Bit	15	14	13	12	11	10	9	8
	SPIxURDTH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SPIxURDTH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SPIxURDTH[31:16] SPI Underrun Data bits

These bits are only used when URDTEN = 1. This register holds the data to transmit when a Transmit Underrun condition occurs.
When the MODE[32:16] or WLENGTH[4:0] bits select 32 to 25-bit data, the SPIx only uses URDATA[31:16]. When the MODE[32:16] or WLENGTH[4:0] bits select 24 to 17-bit data, the SPIx only uses URDATA[23:16].

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20. Inter-Integrated Circuit (I^2C)

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Inter-Integrated Circuit (I^2C)"** (www.microchip.com/DS70000195) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The Inter-Integrated Circuit (I^2C) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may include serial EEPROMs, display drivers, A/D converters, etc.

The I^2C module supports these features:

- 7-Bit and 10-Bit Device Addresses
- General Call Address as Defined in the I^2C Protocol
- Both 100 kHz and 400 kHz Bus Specifications
- Configurable Address Masking
- Multi-Main Modes to Prevent Loss of Messages in Arbitration
- Bus Repeater Mode, Allowing the Acceptance of All Messages as a Secondary, Regardless of the Address
- Automatic SCL

A block diagram of the module is shown in Figure 20-1.

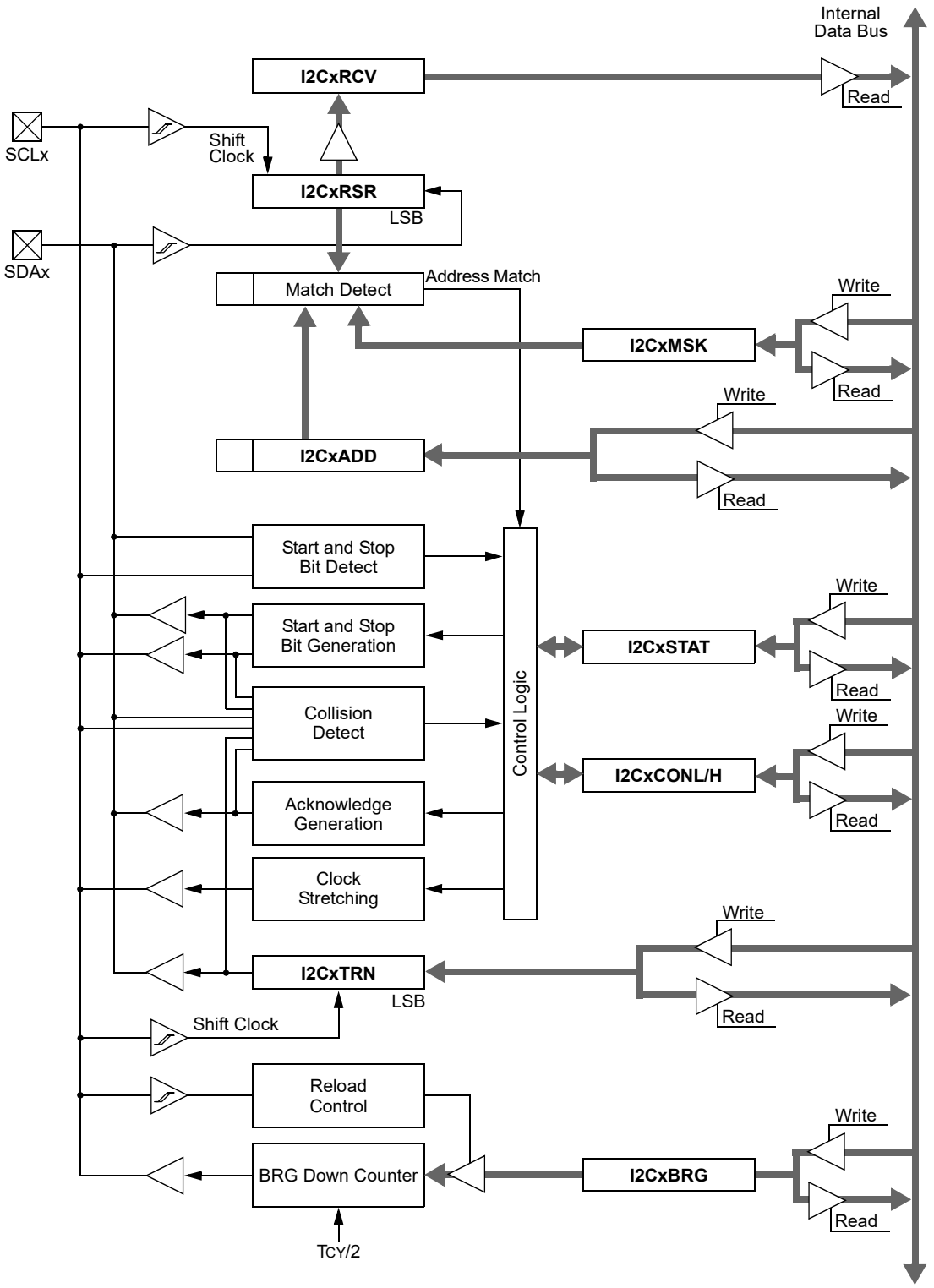
20.1. Communicating as a Host in a Single Host Environment

The details of sending a message in Host mode depend on the communication protocol for the device being communicated with. Typically, the sequence of events is as follows:

1. Assert a Start condition on SDAx and SCLx.
2. Send the I^2C device address byte to the Client with a write indication.
3. Wait for and verify an Acknowledge from the Client.
4. Send the first data byte (sometimes known as the command) to the Client.
5. Wait for and verify an Acknowledge from the Client.
6. Send the serial memory address low byte to the Client.
7. Repeat Steps 4 and 5 until all data bytes are sent.
8. Assert a Repeated Start condition on SDAx and SCLx.
9. Send the device address byte to the Client with a read indication.
10. Wait for and verify an Acknowledge from the Client.
11. Enable Host reception to receive serial memory data.
12. Generate an ACK or NACK condition at the end of a received byte of data.
13. Generate a Stop condition on SDAx and SCLx.

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Figure 20-1. I2Cx Block Diagram



20.2. Setting Baud Rate When Operating as a Bus Main

To compute the Baud Rate Generator reload value, use Equation 18-1.

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Equation 20-1. Computing Baud Rate Reload Value[1,2,3]

$$I2CxBRG = ((1/F_{SCL} - Delay) \bullet F_P/2) - 2$$

Notes:

1. These clock rate values are for guidance only. The actual clock rate should be measured in its intended application.
2. Typical value of delay varies from 110 ns to 150 ns.
3. I2CxBRG values of 0 to 3 are expressly forbidden. The user should never program the I2CxBRG with a value of 0x0, 0x1, 0x2 or 0x3 as indeterminate results may occur.

20.3. Secondary Address Masking

The I2C1MSK register (I2C1MSK) designates address bit positions as “don’t care” for both 7-Bit and 10-Bit Addressing modes. Setting a particular bit location (= 1) in the I2C1MSK register causes the Secondary module to respond, whether the corresponding address bit value is a ‘0’ or a ‘1’. For example, when I2C1MSK is set to ‘0010000000’, the Secondary module will detect both addresses, ‘0000000000’ and ‘0010000000’.

To enable address masking, the Intelligent Peripheral Management Interface (IPMI) must be disabled by clearing the STRICT bit (I2CxCONL[11]).

Note: As a result of changes in the I^{2}C protocol, the addresses in Table 20-2 are reserved and will not be Acknowledged in Secondary mode. This includes any address mask settings that include any of these addresses.

Table 20-1. I2Cx Clock Rates[1,2]

F_{CY}	F_{SCL}	I2CxBRG Value	
		Decimal	Hexadecimal
100 MHz	1 MHz	41	29
100 MHz	400 kHz	116	74
100 MHz	100 kHz	491	1EB
80 MHz	1 MHz	32	20
80 MHz	400 kHz	92	5C
80 MHz	100 kHz	392	188
60 MHz	1 MHz	24	18
60 MHz	400 kHz	69	45
60 MHz	100 kHz	294	126
40 MHz	1 MHz	15	0F
40 MHz	400 kHz	45	2D
40 MHz	100 kHz	195	C3
20 MHz	1 MHz	7	7
20 MHz	400 kHz	22	16
20 MHz	100 kHz	97	61

Notes:

1. Based on $F_{CY} = F_{OSC}/2$; Doze mode and PLL are disabled.
2. These clock rate values are for guidance only. The actual clock rate can be affected by various system-level parameters. The actual clock rate should be measured in its intended application.

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Table 20-2. I2Cx Reserved Addresses[1]

Secondary Address	R/W Bit	Description
0000 000	0	General Call Address[2]
0000 000	1	Start Byte
0000 001	x	Cbus Address
0000 01x	x	Reserved
0000 1xx	x	HS Mode Host Code
1111 0xx	x	10-Bit Client Upper Byte[3]
1111 1xx	x	Reserved

Note:

1. The address bits listed here will never cause an address match independent of address mask settings.
2. This address will be Acknowledged only if GCEN = 1.
3. A match on this address can only occur on the upper byte in 10-Bit Addressing mode.

20.4. SMBus Support

The dsPIC33CDVL256MC506 family devices have support for SMBus through options in the input voltage thresholds. There are two control bits to select one of three options: SMEN (I2CxCONL[8]) and Configuration bit, SMBEN (FDEVOPT[10]). I2C1CONL details the setting of these control bits.

Table 20-3. I^2C Pin Voltage Threshold

	SMEN SFR Bit (I2CxCONL[8])	SMBEN Configuration Bit (FDEVOPT[10])
I^2C (default)	0	x
SMBus 2.0	1	0
SMBus 3.0	1	1

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20.5. I2C Control/Status Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0200	I2C1CONL	15:8	I2CEN		I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
		7:0	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
0x0202	I2C1CONH	15:8								
		7:0		PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
0x0204	I2C1STAT	15:8	ACKSTAT	TRSTAT	ACKTIM			BCL	GCSTAT	ADD10
		7:0	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF
0x0206 ... 0x0207	Reserved									
0x0208	I2C1ADD	15:8							ADD[9:8]	
		7:0	ADD[7:0]							
0x020A ... 0x020B	Reserved									
0x020C	I2C1MSK	15:8							MSK[9:8]	
		7:0	MSK[7:0]							
0x020E ... 0x020F	Reserved									
0x0210	I2C1BRG	15:8	I2CBRG[15:8]							
		7:0	I2CBRG[7:0]							
0x0212 ... 0x0213	Reserved									
0x0214	I2C1TRN	15:8								
		7:0	I2CTXDATA[7:0]							
0x0216 ... 0x0217	Reserved									
0x0218	I2C2RCV	15:8								
		7:0	I2CRXDATA[7:0]							

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20.5.1. I2C1 Control Register Low

Name: I2C1CONL
Offset: 0x200

Notes:

1. Automatically cleared to '0' at the beginning of Client transmission; automatically cleared to '0' at the end of Client reception.
2. Automatically cleared to '0' at the beginning of Client transmission.

Legend: HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
	I2CEN		I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
Access	R/W		R/W/HC	R/W	R/W	R/W	R/W	R/W
Reset	0		0	1	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
Access	R/W	R/W	R/W	R/W/HC	R/W/HC	R/W/HC	R/W/HC	R/W/HC
Reset	0	0	0	0	0	0	0	0

Bit 15 – I2CEN I2C1 Enable bit (writable by software only)

Value	Description
1	Enables the I2C1 module and configures the SDAx and SCLx pins as serial port pins.
0	Disables the I2C1 module; all I^2C pins are controlled by port functions.

Bit 13 – I2CSIDL I2C1 Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode.
0	Continues module operation in Idle mode.

Bit 12 – SCLREL SCLx Release Control bit (I^2C Client mode only)**(1)**

If STREN = 1:**(2)**

User software may write '0' to initiate a clock stretch and write '1' to release the clock. Hardware clears at the beginning of every client data byte transmission. Hardware clears at the end of every client address byte reception. Hardware clears at the end of every client data byte reception.

Value	Description
1	Releases the SCLx clock.
0	Holds the SCLx clock low (clock stretch).

If STREN = 0:

User software may only write '1' to release the clock. Hardware clears at the beginning of every Client data byte transmission. Hardware clears at the end of every Client address byte reception.

Value	Description
1	Releases the SCLx clock.
0	Holds the SCLx clock low (clock stretch).

Bit 11 – STRICT I2C1 Strict Reserved Address Rule Enable bit

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Value	Description
1	Strict Reserved Addressing is enforced; for reserved addresses. (In Client Mode) – The device doesn't respond to reserved address space and addresses falling in that category are NACKed. (In Host Mode) – The device is allowed to generate addresses with reserved address space.
0	Reserved Addressing would be Acknowledged. (In Client Mode) – The device will respond to an address falling in the reserved address space. When there is a match with any of the reserved addresses, the device will generate an ACK. (In Host Mode) – Reserved.

Bit 10 – A10M 10-Bit Client Address Flag bit

Value	Description
1	I2CxADD is a 10-bit Client address.
0	I2CxADD is a 7-bit Client address.

Bit 9 – DISSLW Slew Rate Control Disable bit

Value	Description
1	Slew rate control is disabled for Standard Speed mode (100 kHz, also disabled for 1 MHz mode).
0	Slew rate control is enabled for High-Speed mode (400 kHz).

Bit 8 – SMEN SMBus Input Levels Enable bit

Value	Description
1	Enables input logic so that thresholds are compliant with the SMBus specification.
0	Disables SMBus-specific inputs.

Bit 7 – GCEN General Call Enable bit (in I^2C Client mode only)

Value	Description
1	Enables interrupt when a general call address is received in I2CxRSR; the module is enabled for reception.
0	General call address is disabled.

Bit 6 – STREN SCL1 Clock Stretch Enable bit
In I^2C Client mode only; used in conjunction with the SCLREL bit.

Value	Description
1	Enables clock stretching.
0	Disables clock stretching.

Bit 5 – ACKDT Acknowledge Data bit
In I^2C Host mode during Host Receive mode. The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
In I^2C Client mode when AHEN = 1 or DHEN = 1, the value that the Client will transmit when it initiates an Acknowledge sequence at the end of an address or data reception.

Value	Description
1	NACK is sent.
0	ACK is sent.

Bit 4 – ACKEN Acknowledge Sequence Enable bit
In I^2C Host mode only; applicable during Host Receive mode.

Value	Description
1	Initiates the Acknowledge sequence on SDAx and SCLx pins and transmits the ACKDT data bit.
0	Acknowledge sequence is Idle.

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Bit 3 – RCEN Receive Enable bit (in I^2C Host mode only)

Value	Description
1	Enables Receive mode for I^2C; automatically cleared by hardware at the end of the 8-bit received data byte.
0	Receive sequence is not in progress.

Bit 2 – PEN Stop Condition Enable bit (in I^2C Host mode only)

Value	Description
1	Initiates Stop condition on SDAx and SCLx pins.
0	Stop condition is Idle.

Bit 1 – RSEN Restart Condition Enable bit (in I^2C Host mode only)

Value	Description
1	Initiates Restart condition on SDAx and SCLx pins.
0	Restart condition is Idle.

Bit 0 – SEN Start Condition Enable bit (in I^2C Host mode only)

Value	Description
1	Initiates Start condition on SDAx and SCLx pins.
0	Start condition is Idle.

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20.5.2. I2C1 Control Register High

Name: I2C1CONH
Offset: 0x202

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit 6 – PCIE Stop Condition Interrupt Enable bit

Value	Description
1	Enables interrupt on detection of Stop condition.
0	Stop detection interrupts are disabled.

Bit 5 – SCIE Start Condition Interrupt Enable bit

Value	Description
1	Enables interrupt on detection of Start or Restart conditions.
0	Start detection interrupts are disabled.

Bit 4 – BOEN Buffer Overwrite Enable bit

Value	Description
1	I2CxRCV is updated, and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if the RBF bit = 0.
0	I2CxRCV is only updated when I2COV is clear.

Bit 3 – SDAHT SDAx Hold Time Selection bit

Value	Description
1	Minimum of 300 ns hold time on SDAx after the falling edge of SCLx.
0	Minimum of 100 ns hold time on SDAx after the falling edge of SCLx.

Bit 2 – SBCDE Client Mode Bus Collision Detect Enable bit
If, on the rising edge of SCLx, SDAx is sampled low when the module is outputting a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.

Value	Description
1	Enables Client bus collision interrupts.
0	Client bus collision interrupts are disabled.

Bit 1 – AHEN Address Hold Enable bit

Value	Description
1	Following the eighth falling edge of SCLx for a matching received address byte; SCLREL bit (I2CxCONL[12]) will be cleared and SCLx will be held low.
0	Address holding is disabled.

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Bit 0 – DHEN Data Hold Enable bit

Value	Description
1	Following the eighth falling edge of SCLx for a received data byte; Client hardware clears the SCLREL bit (I2CxCONL[12]) and SCLx is held low.
0	Data holding is disabled.

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20.5.3. I2C1 Status Register

Name: I2C1STAT
Offset: 0x204

Legend: C = Clearable bit; HS = Hardware Settable bit; HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
	ACKSTAT	TRSTAT	ACKTIM			BCL	GCSTAT	ADD10
Access	R/HSC	R/HSC	R/HSC			R/C/HSC	R/HSC	R/HSC
Reset	0	0	0			0	0	0

Bit	7	6	5	4	3	2	1	0
	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF
Access	R/C/HS	R/C/HS	R/HSC	R/HSC	R/HSC	R/HSC	R/HSC	R/HSC
Reset	0	0	0	0	0	0	0	0

Bit 15 – ACKSTAT Acknowledge Status bit
(updated in all Host and Client modes)

Value	Description
1	Acknowledge was not received from Client.
0	Acknowledge was received from Client.

Bit 14 – TRSTAT Transmit Status bit
(when operating as I^2C Host; applicable to Host transmit operation)

Value	Description
1	Host transmit is in progress (8 bits + ACK).
0	Host transmit is not in progress.

Bit 13 – ACKTIM Acknowledge Time Status bit
(valid in I^2C Client mode only)

Value	Description
1	Indicates I^2C bus is in an Acknowledge sequence, set on eighth falling edge of SCLx clock.
0	Not an Acknowledge sequence, cleared on ninth rising edge of SCLx clock.

Bit 10 – BCL Bus Collision Detect bit
(Host/Client mode; cleared when I^2C module is disabled, I2CEN = 0)

Value	Description
1	A bus collision has been detected during a Host or Client transmit operation.
0	No bus collision has been detected.

Bit 9 – GCSTAT General Call Status bit
(cleared after Stop detection)

Value	Description
1	General call address was received.
0	General call address was not received.

Bit 8 – ADD10 10-Bit Address Status bit
(cleared after Stop detection)

Value	Description
1	10-bit address was matched.

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Value	Description
0	10-bit address was not matched.

Bit 7 – IWCOL I2Cx Write Collision Detect bit

Value	Description
1	An attempt to write to the I2CxTRN register failed because the I^2C module is busy; must be cleared in software.
0	No collision.

Bit 6 – I2COV I2Cx Receive Overflow Flag bit

Value	Description
1	A byte was received while the I2CxRCV register is still holding the previous byte; I2COV is a “don’t care” in Transmit mode and must be cleared in software.
0	No overflow.

Bit 5 – D/$\overline{A}$ Data/$\overline{\text{Address}}$ bit
(when operating as I^2C Client)

Value	Description
1	Indicates that the last byte received was data.
0	Indicates that the last byte received or transmitted was an address.

Bit 4 – P I2Cx Stop bit
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.

Value	Description
1	Indicates that a Stop bit has been detected last.
0	Stop bit was not detected last.

Bit 3 – S I2Cx Start bit
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.

Value	Description
1	Indicates that a Start (or Repeated Start) bit was detected last.
0	Start bit was not detected last.

Bit 2 – R/$\overline{W}$ Read/$\overline{\text{Write}}$ Information bit
(when operating as I^2C Client)

Value	Description
1	Read: Indicates that the data transfer is output from the Client.
0	Write: Indicates that the data transfer is input to the Client.

Bit 1 – RBF Receive Buffer Full Status bit

Value	Description
1	Receive is complete, I2CxRCV is full.
0	Receive is not complete, I2CxRCV is empty.

Bit 0 – TBF Transmit Buffer Full Status bit

Value	Description
1	Transmit is in progress, I2CxTRN is full (8 bits of data).
0	Transmit is complete, I2CxTRN is empty.

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20.5.4. I2C1 Address Register

Name: I2C1ADD
Offset: 0x208

Bit	15	14	13	12	11	10	9	8
							ADD[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	ADD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – ADD[9:0] I2C1 Address bits

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20.5.5. I2C1 Client Mode Address Mask Register

Name: I2C1MSK
Offset: 0x20C

Bit	15	14	13	12	11	10	9	8
							MSK[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	MSK[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – MSK[9:0] I2C1 Mask for Address Bit x Select bits

Value	Description
1	Enables masking for bit x of the incoming message address; a bit match is not required in this position.
0	Disables masking for bit x; a bit match is required in this position.

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20.5.6. I2C1 Baud Rate Generator Register

Name: I2C1BRG
Offset: 0x210

Bit	15	14	13	12	11	10	9	8
	I2CBRG[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	I2CBRG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – I2CBRG[15:0] I2C1 Baud Rate Generator bits

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20.5.7. I2C1 Transmit Register

Name: I2C1TRN
Offset: 0x214

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	I2CTXDATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – I2CTXDATA[7:0] I2C1 Transmit Data bits

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20.5.8. I2C2 Receive Register

Name: I2C2RCV
Offset: 0x218

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	I2CRXDATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – I2CRXDATA[7:0] I2C2 Receive Data bits

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21. Single-Edge Nibble Transmission (SENT)

Note: This data sheet summarizes the features of this group of dsPIC33CDVL256MC506 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Single-Edge Nibble Transmission (SENT) Module"** (www.microchip.com/DS70005145) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The Single-Edge Nibble Transmission (SENT) module is based on the SAE J2716, *"SENT – Single-Edge Nibble Transmission for Automotive Applications"*. The SENT protocol is a one-way, single-wire, time-modulated serial communication, based on successive falling edges. It is intended for use in applications where high-resolution sensor data needs to be communicated from a sensor to an Engine Control Unit (ECU).

The SENTx module has the following major features:

- Selectable Transmit or Receive Mode
- Synchronous or Asynchronous Transmit Modes
- Automatic Data Rate Synchronization
- Optional Automatic Detection of CRC Errors in Receive Mode
- Optional Hardware Calculation of CRC in Transmit Mode
- Support for Optional Pause Pulse Period
- Data Buffering for One Message Frame
- Selectable Data Length for Transmit/Receive, Up to Six Nibbles
- Automatic Detection of Framing Errors

The SENT protocol timing is based on a predetermined time unit, T_{TICK}. Both the transmitter and receiver must be preconfigured for T_{TICK}, which can vary from 3 to 90 µs. A SENT message frame starts with a Sync pulse. The purpose of the Sync pulse is to allow the receiver to calculate the data rate of the message encoded by the transmitter. The SENT specification allows messages to be validated with up to a 20% variation in T_{TICK}. This allows the transmitter and receiver to run from different clocks that may be inaccurate and drift with time and temperature. The data nibbles are four bits in length and are encoded as the data value + 12 ticks. This yields a 0 value of 12 ticks and the maximum value, 0xF, of 27 ticks.

A SENT message consists of the following:

- A synchronization/calibration period of 56 tick times
- A status nibble of 12-27 tick times
- Up to six data nibbles of 12-27 tick times
- A CRC nibble of 12-27 tick times
- An optional pause pulse period of 12-768 tick times

Figure 21-1 shows a block diagram of the SENTx module.

Figure 21-2 shows the construction of a typical 6-nibble data frame, with the numbers representing the minimum or maximum number of tick times for each section.

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Figure 21-1. SENTx Module Block Diagram

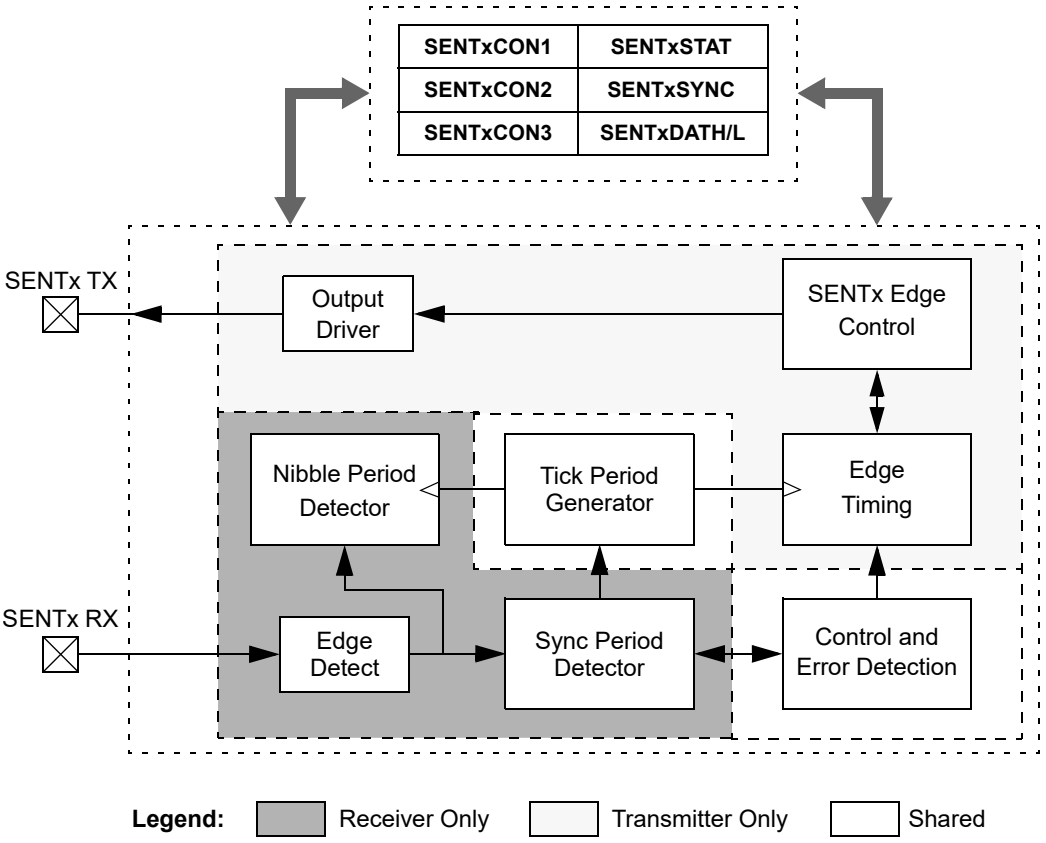
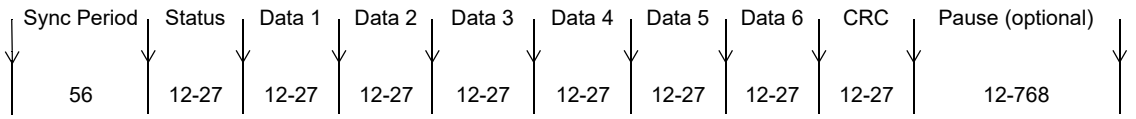


Figure 21-2. SENTx Protocol Data Frames



21.1. Transmit Mode

By default, the SENTx module is configured for transmit operation. The module can be configured for continuous asynchronous message frame transmission, or alternatively, for Synchronous mode triggered by software. When enabled, the transmitter will send a Sync, followed by the appropriate number of data nibbles, an optional CRC and optional pause pulse. The tick period used by the SENTx transmitter is set by writing a value to the TICKTIME[15:0] (SENTxCON2L[15:0]) bits. The tick period calculations are shown in Equation 21-1.

Equation 21-1. TICK Period Calculation

$$TICKTIME[15:0] = \frac{T_{TICK}}{T_{CLK}} - 1$$

An optional pause pulse can be used in Asynchronous mode to provide a fixed message frame time period. The frame period used by the SENTx transmitter is set by writing a value to the FRAMETIME[15:0] (SENTxCON3L[15:0]) bits. The formulas used to calculate the value of frame time are shown in Equation 21-2.

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Equation 21-2. Frame Time Calculations

$$FRAMETIME[15:0] = T_{TICK}/T_{FRAME}$$

Where:
848 + 12N ≥ FRAMETIME [15:0] ≥ 122 + 27N, for
1 ≤ N ≤ 6
T_{FRAME} = Total time of the message frame
N = The number of data nibbles in message

Note: The module will not produce a pause period with less than 12 ticks, regardless of the FRAMETIME[15:0] value. FRAMETIME[15:0] values beyond 2047 will have no effect on the length of a data frame.

21.1.1. Transmit Mode Configuration

21.1.1.1. Initializing the SENTx Module

Perform the following steps to initialize the module:

1. Write RCVEN (SENT1CON1L[11]) = 0 for Transmit mode.
2. Write TXM (SENT1CON1L[10]) = 0 for Asynchronous Transmit mode or TXM = 1 for Synchronous mode.
3. Write NIBCNT[2:0] (SENT1CON1L[2:0]) for the desired data frame length.
4. Write CRCEN (SENT1CON1L[8]) for hardware or software CRC calculation.
5. Write PPP (SENT1CON1L[7]) for optional pause pulse.
6. If PPP = 1, write T_{FRAME} to SENT1CON3L.
7. Write SENT1CON2L with the appropriate value for the desired tick period.
8. Enable interrupts and set interrupt priority.
9. Write initial status and data values to SENT1DATH/L.
10. If CRCEN = 0, calculate CRC and write the value to CRC[3:0] (SENT1DATL[3:0]).
11. Set the SNTEN (SENT1CON1L[15]) bit to enable the module.

User software updates to SENT1DATH/L must be performed after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt to trigger data writes.

21.2. Receive Mode

The module can be configured for receive operation by setting the RCVEN (SENT1CON1L[11]) bit. The time between each falling edge is compared to SYNCMIN[15:0] (SENT1CON3L[15:0]) and SYNCMAX[15:0] (SENT1CON2L[15:0]), and if the measured time lies between the minimum and maximum limits, the module begins to receive data. The validated Sync time is captured in the SENT1SYNC register and the tick time is calculated. Subsequent falling edges are verified to be within the valid data width and the data are stored in the SENT1DATL/H registers. An interrupt event is generated at the completion of the message and the user software should read the SENTx Data registers before the reception of the next nibble. The equation for SYNCMIN[15:0] and SYNCMAX[15:0] is shown in Equation 21-3.

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Equation 21-3. SYNCMIN[15:0] and SYNCMAX[15:0] Calculations

$$T_{TICK} = T_{CLK} \bullet (TICKTIME[15:0] + 1)$$
$$FRAMETIME[15:0] = T_{TICK}/T_{FRAME}$$
$$SyncCount = 8 \text{ x } F_{RCV} \text{ x } T_{TICK}$$
$$SYNCMIN[15:0] = 0.8 \text{ x } SyncCount$$
$$SYNCMAX[15:0] = 1.2 \text{ x } SyncCount$$
$$FRAMETIME[15:0] \geq 122 + 27N$$
$$FRAMETIME[15:0] \geq 848 + 12N$$

Where:
T_{FRAME} = Total time of the message from ms
N = The number of data nibbles in message, 1-6
F_{RCV} = FCY x Prescaler
T_{CLK} = FCY/Prescaler

For T_{TICK} = 3.0 µs and F_{CLK} = 4 MHz, SYNCMIN[15:0] = 76.

Note: To ensure a Sync period can be identified, the value written to SYNCMIN[15:0] must be less than the value written to SYNCMAX[15:0].

21.2.1. Receive Mode Configuration

21.2.1.1. Initializing the SENTx Module

Perform the following steps to initialize the module:

1. Write RCVEN (SENT1CON1L[11]) = 1 for Receive mode.
2. Write NIBCNT[2:0] (SENT1CON1L[2:0]) for the desired data frame length.
3. Write CRCEN (SENT1CON1L[8]) for hardware or software CRC validation.
4. Write PPP (SENT1CON1L[7]) = 1 if pause pulse is present.
5. Write SENT1CON2L with the value of SYNCMAXx (Nominal Sync Period + 20%).
6. Write SENT1CON3L with the value of SYNCMINx (Nominal Sync Period – 20%).
7. Enable interrupts and set interrupt priority.
8. Set the SNTEN (SENT1CON1L[15]) bit to enable the module.

The data should be read from the SENT1DATL/H registers after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt trigger.

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21.3. SENT Control/Status Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x80	SENT1CON1L	15:8	SNTEN		SNTSIDL		RCVEN	TXM	TXPOL	CRCEN
		7:0	PPP	SPCEN		PS		NIBCNT[2:0]		
0x82 ... 0x83	Reserved									
0x84	SENT1CON2L	15:8	SENT1CON2[15:8]							
		7:0	SENT1CON2[7:0]							
0x86 ... 0x87	Reserved									
0x88	SENT1CON3L	15:8	SENT1CON3[15:8]							
		7:0	SENT1CON3[7:0]							
0x8A ... 0x8B	Reserved									
0x8C	SENT1STATL	15:8								
		7:0	PAUSE	NIB[2:0]			CRCERR	FRMERR	RXIDLE	SYNCTXEN
0x8E ... 0x8F	Reserved									
0x90	SENT1SYNC	15:8	SENTSYNC[15:8]							
		7:0	SENTSYNC[7:0]							
0x92 ... 0x93	Reserved									
0x94	SENT1DATL	15:8	DATA4[3:0]				DATA5[3:0]			
		7:0	DATA6[3:0]				CRC[3:0]			
0x96	SENT1DATH	15:8	STAT[3:0]				DATA1[3:0]			
		7:0	DATA2[3:0]				DATA3[3:0]			

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21.3.1. SENT1 Control Register 1

Name: SENT1CON1L
Offset: 0x080

Notes:
1. This bit has no function in Receive mode (RCVEN = 1).
2. This bit has no function in Transmit mode (RCVEN = 0).

Bit	15	14	13	12	11	10	9	8
	SNTEN		SNTSIDL		RCVEN	TXM	TXPOL	CRCEN
Access	R/W		R/W		R/W	R/W	R/W	R/W
Reset	0		0		0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PPP	SPCEN		PS		NIBCNT[2:0]		
Access	R/W	R/W		R/W		R/W	R/W	R/W
Reset	0	0		0		0	0	0

Bit 15 – SNTEN SENTx Enable bit

Value	Description
1	SENTx is enabled
0	SENTx is disabled

Bit 13 – SNTSIDL SENTx Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when the device enters Idle mode
0	Continues module operation in Idle mode

Bit 11 – RCVEN SENTx Receive Enable bit

Value	Description
1	SENTx operates as a receiver
0	SENTx operates as a transmitter (sensor)

Bit 10 – TXM SENTx Transmit Mode bit(1)

Value	Description
1	SENTx transmits data frame only when triggered using the SYNCTXEN status bit
0	SENTx transmits data frames continuously while SNTEN = 1

Bit 9 – TXPOL SENTx Transmit Polarity bit(1)

Value	Description
1	SENTx data output pin is low in the Idle state
0	SENTx data output pin is high in the Idle state

Bit 8 – CRCEN CRC Enable bit
Module in Receive Mode (RCVEN = 1):
1 = SENTx performs CRC verification on received data using the preferred J2716 method
0 = SENTx does not perform CRC verification on received data
Module in Transmit Mode (RCVEN = 1):
1 = SENTx automatically calculates CRC using the preferred J2716 method
0 = SENTx does not calculate CRC

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Bit 7 – PPP Pause Pulse Present bit

Value	Description
1	SENTx is configured to transmit/receive SENT messages with pause pulse
0	SENTx is configured to transmit/receive SENT messages without pause pulse

Bit 6 – SPCEN Short PWM Code Enable bit(2)

Value	Description
1	SPC control from external source is enabled
0	SPC control from external source is disabled

Bit 4 – PS SENTx Module Clock Prescaler (divider) bit

Value	Description
1	Divide-by-4
0	Divide-by-1

Bits 2:0 – NIBCNT[2:0] Nibble Count Control bits

Value	Description
111	Reserved; do not use
110	Module transmits/receives six data nibbles in a SENT data pocket
101	Module transmits/receives five data nibbles in a SENT data pocket
100	Module transmits/receives four data nibbles in a SENT data pocket
011	Module transmits/receives three data nibbles in a SENT data pocket
010	Module transmits/receives two data nibbles in a SENT data pocket
001	Module transmits/receives one data nibble in a SENT data pocket
000	Reserved; do not use

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21.3.2. SENT1 Control Register 2

Name: SENT1CON2L
Offset: 0x084

Bit	15	14	13	12	11	10	9	8
	SENT1CON2[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SENT1CON2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SENT1CON2[15:0] SENT1 Control Register 2 bits

The SENT1CON2L register is a 16-bit readable and writable register.

Transmit mode:

Stores the 16-bit value for TICKTIME[15:0], the period of the tick clock generator.

Receive mode:

Stores the 16-bit value for SYNCMAX[15:0], the maximum time interval for a valid Sync period.

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21.3.3. SENT1 Control Register 3

Name: SENT1CON3L
Offset: 0x088

Bit	15	14	13	12	11	10	9	8
	SENT1CON3[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SENT1CON3[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SENT1CON3[15:0] SENT1 Control Register 3 bits

In Transmit modes:
Stores the 16-bit value of FRAMETIME[15:0], the total number of ticks for a data frame when the pause pulse is used.
Receive mode:
Stores the 16-bit value for SYNCMIN[15:0], the minimum time interval for a valid Sync period.

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21.3.4. SENT1 Status Register

Name: SENT1STATL
Offset: 0x08C

Note:

1. In Receive mode (RCVEN = 1), the SYNCTXEN bit is read-only.

Legend: C = Clearable bit; HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PAUSE	NIB[2:0]			CRCERR	FRMERR	RXIDLE	SYNCTXEN
Access	R	R	R	R	R	R/C	R	R/W/HC
Reset	0	0	0	0	0	0	0	0

Bit 7 – PAUSE Pause Period Status bit

Value	Description
1	The module is transmitting/receiving a pause period.
0	The module is not transmitting/receiving a pause period.

Bits 6:4 – NIB[2:0] Nibble Status bits

Module in Transmit Mode (RCVEN = 0):
111 = Module is transmitting a CRC nibble.
110 = Module is transmitting Data Nibble 6.
101 = Module is transmitting Data Nibble 5.
100 = Module is transmitting Data Nibble 4.
011 = Module is transmitting Data Nibble 3.
010 = Module is transmitting Data Nibble 2.
001 = Module is transmitting Data Nibble 1.
000 = Module is transmitting a status nibble or pause period, or is not transmitting.

Module in Receive Mode (RCVEN = 1):
111 = Module is receiving a CRC nibble or was receiving this nibble when an error occurred.
110 = Module is receiving Data Nibble 6 or was receiving this nibble when an error occurred.
101 = Module is receiving Data Nibble 5 or was receiving this nibble when an error occurred.
100 = Module is receiving Data Nibble 4 or was receiving this nibble when an error occurred.
011 = Module is receiving Data Nibble 3 or was receiving this nibble when an error occurred.
010 = Module is receiving Data Nibble 2 or was receiving this nibble when an error occurred.
001 = Module is receiving Data Nibble 1 or was receiving this nibble when an error occurred.
000 = Module is receiving a status nibble or waiting for Sync

Bit 3 – CRCERR CRC Status bit (Receive mode only)

Value	Description
1	A CRC error has occurred for the 1-6 data nibbles in SENT1DATL/H.
0	A CRC error has not occurred.

Bit 2 – FRMERR Framing Error Status bit (Receive mode only)

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Value	Description
1	A data nibble was received with less than 12 tick periods or greater than 27 tick periods.
0	Framing error has not occurred.

Bit 1 – RXIDLE SENTx Receiver Idle Status bit (Receive mode only)

Value	Description
1	The SENTx data bus has been Idle (high) for a period of SYNCMAX[15:0] or greater.
0	The SENTx data bus is not Idle.

Bit 0 – SYNCTXEN SENTx Synchronization Period Status/Transmit Enable bit(1)

Module in Receive Mode (RCVEN = 1):

1 = A valid synchronization period was detected; the module is receiving nibble data.

0 = No synchronization period has been detected; the module is not receiving nibble data.

Module in Asynchronous Transmit Mode (RCVEN = 0, TXM = 0):

The bit always reads as '1' when the module is enabled, indicating the module transmits SENTx data frames continuously. The bit reads '0' when the module is disabled.

Module in Synchronous Transmit Mode (RCVEN = 0, TXM = 1):

1 = The module is transmitting a SENTx data frame.

0 = The module is not transmitting a data frame, user software may set SYNCTXEN to start another data frame transmission.

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21.3.5. SENT1 Sync Period Timer Register

Name: SENT1SYNC(1)
Offset: 0x090

Note:

1. This register is not available in Transmit mode (RCVEN = 0).

Bit	15	14	13	12	11	10	9	8
	SENTSYNC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SENTSYNC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SENTSYNC[15:0] Captured Sync Period bits
In Receive mode, the length of the synchronization time period is captured.

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21.3.6. SENT1 Receive Data Register Low

Name: SENT1DATL(1)
Offset: 0x094

Note:

1. Register bits are read-only in Receive mode (RCVEN = 1). In Transmit mode, the CRC[3:0] bits are read-only when automatic CRC calculation is enabled (RCVEN = 0, CRCEN = 1).

Bit	15	14	13	12	11	10	9	8
	DATA4[3:0]				DATA5[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA6[3:0]				CRC[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:12 – DATA4[3:0] Data Nibble 4 Data bits

Bits 11:8 – DATA5[3:0] Data Nibble 5 Data bits

Bits 7:4 – DATA6[3:0] Data Nibble 6 Data bits

Bits 3:0 – CRC[3:0] CRC Nibble Data bits

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21.3.7. SENT1 Receive Data Register High

Name: SENT1DATH(1)
Offset: 0x096

Note:

1. Register bits are read-only in Receive mode (RCVEN = 1). In Transmit mode, the CRC[3:0] bits are read-only when automatic CRC calculation is enabled (RCVEN = 0, CRCEN = 1).

Bit	15	14	13	12	11	10	9	8
	STAT[3:0]				DATA1[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA2[3:0]				DATA3[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:12 – STAT[3:0] Status Nibble Data bits

Bits 11:8 – DATA1[3:0] Data Nibble 1 Data bits

Bits 7:4 – DATA2[3:0] Data Nibble 2 Data bits

Bits 3:0 – DATA3[3:0] Data Nibble 3 Data bits

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22. Timer1

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timer1 Module"** (www.microchip.com/DS70005279) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be Operated in Asynchronous Counter mode
- Asynchronous Timer
- Operational during CPU Sleep mode
- Software Selectable Prescalers 1:1, 1:8, 1:64 and 1:256
- External Clock Selection Control
- The Timer1 External Clock Input (T1CK) can Optionally be Synchronized to the Internal Device Clock and the Clock Synchronization is Performed after the Prescaler

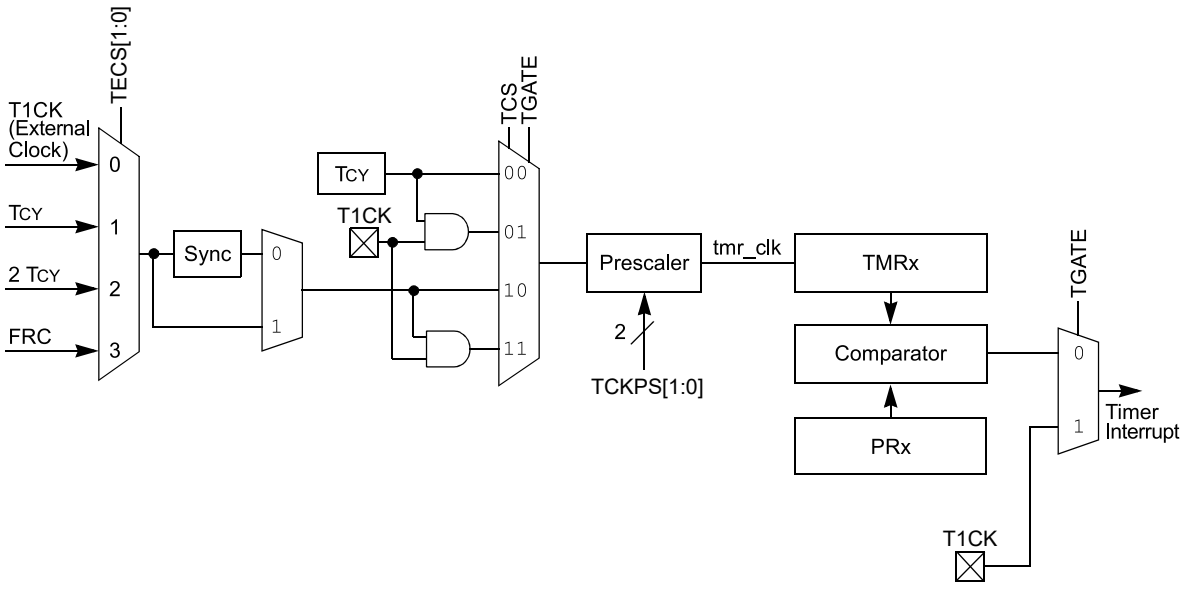
If Timer1 is used for SCCP, the timer should be running in Synchronous mode.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

A block diagram of Timer1 is shown in Figure 22-1.

Figure 22-1. 16-Bit Timer1 Module Block Diagram



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22.1. Timer1 Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0100	T1CON	15:8	TON		SIDL	TMWDIS	TMWIP	PRWIP	TECS[1:0]	
		7:0	TGATE		TCKPS[1:0]			TSYNC	TCS	
0x0102 ... 0x0103	Reserved									
0x0104	TMR1	15:8	TMR[15:8]							
		7:0	TMR[7:0]							
0x0106 ... 0x0107	Reserved									
0x0108	PR1	15:8	PR[15:8]							
		7:0	PR[7:0]							

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22.1.1. Timer1 Control Register

Name: T1CON
Offset: 0x100

Note:

1. When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.

Bit	15	14	13	12	11	10	9	8
	TON		SIDL	TMWDIS	TMWIP	PRWIP	TECS[1:0]	
Access	R/W		R/W	R/W	R	R	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TGATE		TCKPS[1:0]			TSYNC	TCS	
Access	R/W		R/W	R/W		R/W	R/W	
Reset	0		0	0		0	0	

Bit 15 – TON Timer1 On bit(1)

Value	Description
1	Starts 16-bit Timer1.
0	Stops 16-bit Timer1.

Bit 13 – SIDL Timer1 Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when the device enters Idle mode.
0	Continues module operation in Idle mode.

Bit 12 – TMWDIS Asynchronous Timer1 Write Disable bit

Value	Description
1	Timer writes are ignored while a posted write to TMR1 or PR1 is synchronized with the asynchronous clock domain.
0	Back-to-back writes are enabled in Asynchronous mode.

Bit 11 – TMWIP Asynchronous Timer1 Write in Progress bit

Value	Description
1	Write to the timer in Asynchronous mode is pending.
0	Write to the timer in Asynchronous mode is complete.

Bit 10 – PRWIP Asynchronous Period Write in Progress bit

Value	Description
1	Write to the Period register in Asynchronous mode is pending.
0	Write to the Period register in Asynchronous mode is complete.

Bits 9:8 – TECS[1:0] Timer1 Extended Clock Select bits

Value	Description
11	FRC
10	F_{OSC}
01	F_P
00	External Clock comes from the T1CK pin.

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Bit 7 – TGATE Timer1 Gated Time Accumulation Enable bit

When TCS = 1:

This bit is ignored.

When TCS = 0:

Value	Description
1	Gated time accumulation is enabled.
0	Gated time accumulation is disabled.

Bits 5:4 – TCKPS[1:0] Timer1 Input Clock Prescale Select bits

Value	Description
11	1:256
10	1:64
01	1:8
00	1:1

Bit 2 – TSYNC Timer1 External Clock Input Synchronization Select bit(1)

When TCS = 0:

This bit is ignored.

When TCS = 1:

Value	Description
1	Synchronizes the External Clock input.
0	Does not synchronize the External Clock input.

Bit 1 – TCS Timer1 Clock Source Select bit(1)

Value	Description
1	External Clock source selected by TECS[1:0].
0	Internal peripheral clock (F_P).

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22.1.2. Timer1 Counter Register

Name: TMR1
Offset: 0x104

Bit	15	14	13	12	11	10	9	8
	TMR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TMR[15:0] Timer Value bits

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22.1.3. Period Register 1

Name: PR1
Offset: 0x108

Bit	15	14	13	12	11	10	9	8
	PR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PR[15:0] Period Register bits

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23. Capture/Compare/PWM/Timer Modules (SCCP)

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Capture/Compare/PWM/Timer (MCCP and SCCP)"** (www.microchip.com/DS30003035) in the *"dsPIC33/PIC24 Family Reference Manual"*.

dsPIC33CDVL256MC506 family devices include several Capture/Compare/PWM/Timer base modules, which provide the functionality of three different peripherals from earlier PIC24F devices. The module can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

Single Capture/Compare/PWM (SCCP) output modules provide only one PWM output.

The SCCP module can be operated only in one of the three major modes at any time. The other modes are not available unless the module is reconfigured for the new mode.

A conceptual block diagram for the module is shown in Figure 23-1. All three modes share a time base generator and a common Timer register pair (CCPxTMRH/L); other shared hardware components are added as a particular mode requires.

Each module has a total of six control and status registers:

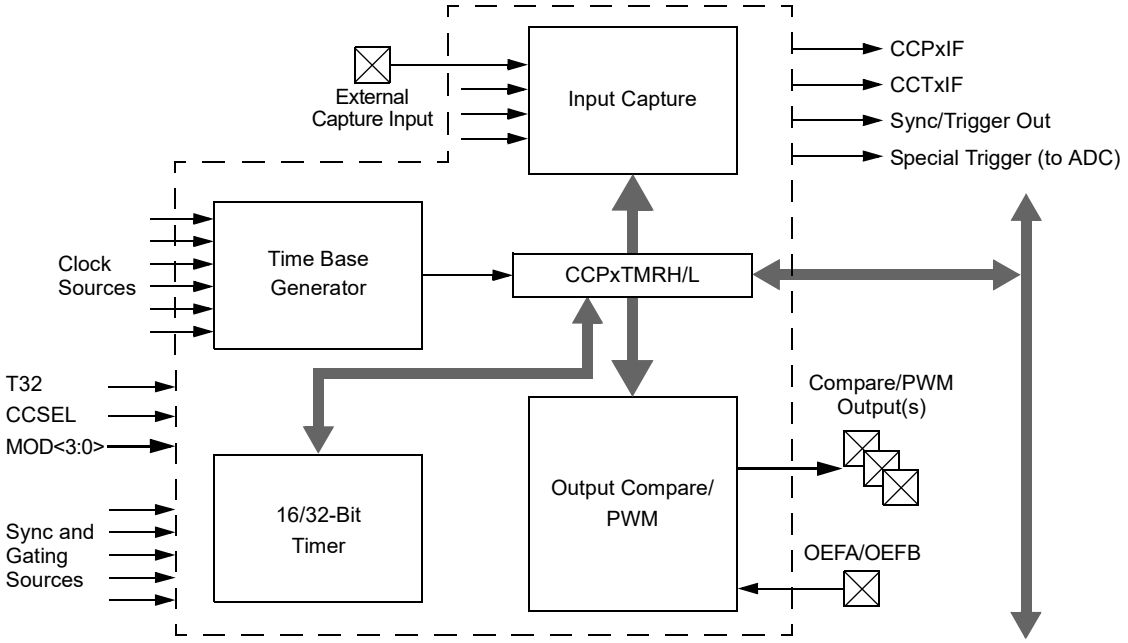
- CCPxCON1L
- CCPxCON1H
- CCPxCON2L
- CCPxCON2H
- CCPxCON3H
- CCPxSTATL

Each module also includes eight buffer/counter registers that serve as Timer Value registers or data holding buffers:

- CCPxTMRH/CCPxTMRL (CCPx Timer High/Low Counters)
- CCPxPRH/CCPxPRL (CCPx Timer Period High/Low)
- CCPxRA (CCPx Primary Output Compare Data Buffer)
- CCPxRB (CCPx Secondary Output Compare Data Buffer)
- CCPxBUFH/CCPxBUFL (CCPx Input Capture High/Low Buffers)

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Figure 23-1. SCCPx Conceptual Block Diagram

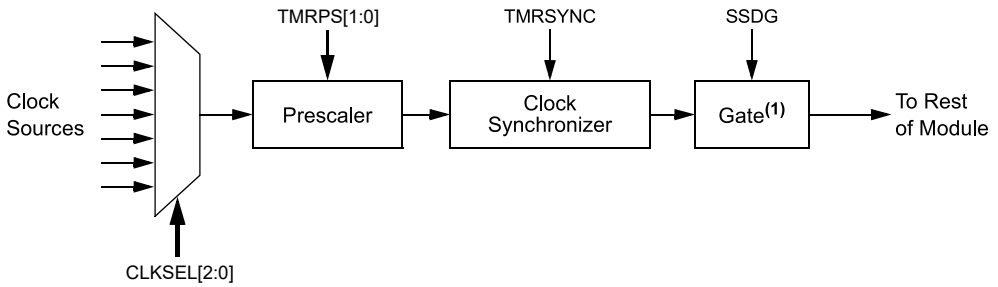


23.1. Time Base Generator

The Timer Clock Generator (TCG) generates a clock for the module's internal time base, using one of the clock signals already available on the microcontroller. This is used as the time reference for the module in its three major modes. The internal time base is shown in Figure 23-2.

There are eight inputs available to the clock generator, which are selected using the CLKSEL[2:0] bits (CCPxCON1L[10:8]). Available sources include the FRC, LPRC and the TCLKI External Clock inputs. The system clock is the default source (CLKSEL[2:0] = 000).

Figure 23-2. Timer Clock Generator



Note 1: Gating is available in Timer modes only.

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23.2. General Purpose Timer

Timer mode is selected when CCSEL = 0 and MOD[3:0] = 0000. The timer can function as a 32-bit timer or a dual 16-bit timer, depending on the setting of the T32 bit (Table 23-1).

Table 23-1. Timer Operation Mode

T32 (CCPxCON1L[5])	Operating Mode
0	Dual Timer Mode (16-bit)
1	Timer Mode (32-bit)

Dual 16-Bit Timer mode provides a simple timer function with two independent 16-bit timer/counters. The primary timer uses CCPxTMRL and CCPxPRL. Only the primary timer can interact with other modules on the device. It generates the SCCPx sync out signals for use by other SCCP modules. It can also use the SYNC[4:0] bits signal generated by other modules.

The secondary timer uses CCPxTMRH and CCPxPRH. It is intended to be used only as a periodic interrupt source for scheduling CPU events. It does not generate an output sync/trigger signal like the primary time base. In Dual Timer mode, the CCPx Secondary Timer Period register, CCPxPRH, generates the SCCP compare event (CCPxIF) used by many other modules on the device.

The 32-Bit Timer mode uses the CCPxTMRL and CCPxTMRH registers together as a single 32-bit timer. When CCPxTMRL overflows, CCPxTMRH increments by one. This mode provides a simple timer function when it is important to track long time periods. Note that the T32 bit (CCPxCON1L[5]) should be set before the CCPxTMRL or CCPxPRH registers are written to initialize the 32-bit timer.

23.2.1. Sync and Trigger Operation

In both 16-bit and 32-bit modes, the timer can also function in either synchronization (“sync”) or trigger operation. Both use the SYNC[4:0] bits (CCPxCON1H[4:0]) to determine the input signal source. The difference is how that signal affects the timer.

In sync operation, the timer Reset or clear occurs when the input selected by SYNC[4:0] is asserted. The timer immediately begins to count again from zero unless it is held for some other reason. Sync operation is used whenever the TRIGEN bit (CCPxCON1H[7]) is cleared. SYNC[4:0] can have any value, except ‘11111’.

In trigger operation, the timer is held in Reset until the input selected by SYNC[4:0] is asserted; when it occurs, the timer starts counting. Trigger operation is used whenever the TRIGEN bit is set. In Trigger mode, the timer will continue running after a trigger event as long as the CCPTRIG bit (CCPxSTATL[7]) is set. To clear CCPTRIG, the TRCLR bit (CCPxSTATL[5]) must be set to clear the trigger event, reset the timer and hold it at zero until another trigger event occurs. On dsPIC33CDVL256MC506 family devices, trigger operation can only be used when the system clock is the time base source (CLKSEL[2:0] = 000).

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Figure 23-3. Dual 16-Bit Timer Mode

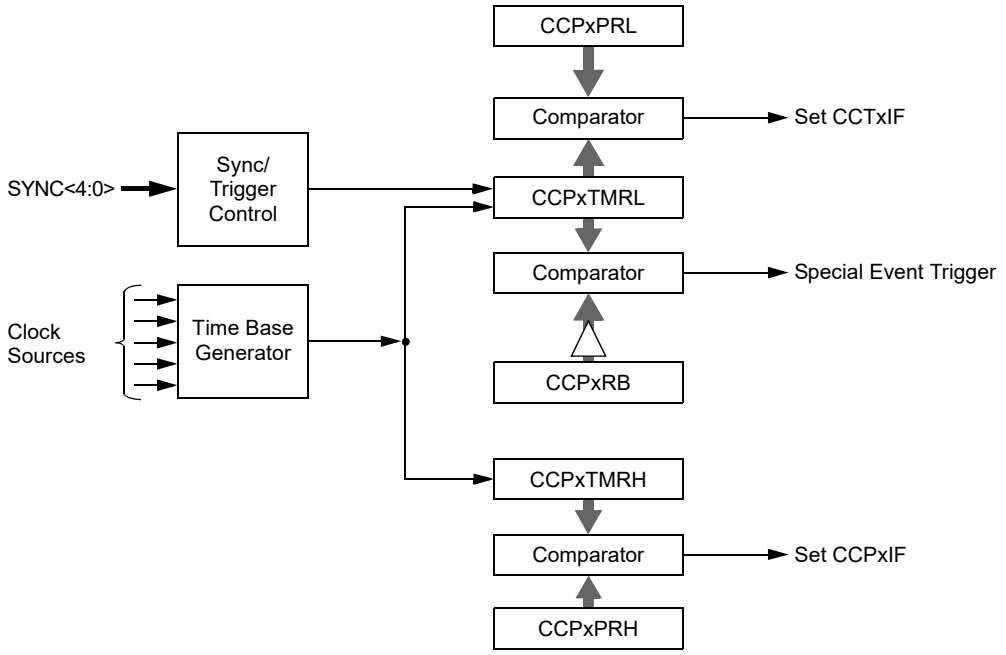
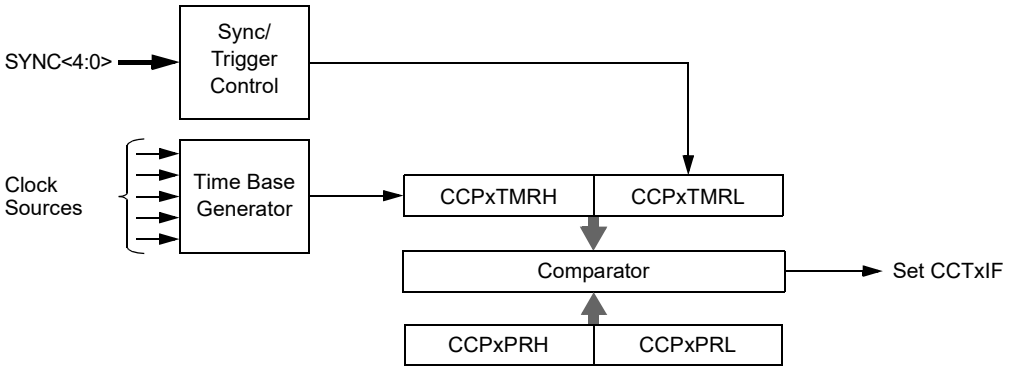


Figure 23-4. 32-Bit Timer Mode



23.3. Output Compare Mode

Output Compare mode compares the Timer register value with the value of one or two Compare registers, depending on its mode of operation. The Output Compare x module, on compare match events, has the ability to generate a single output transition or a train of output pulses. Like most PIC® MCU peripherals, the Output Compare x module can also generate interrupts on a compare match event.

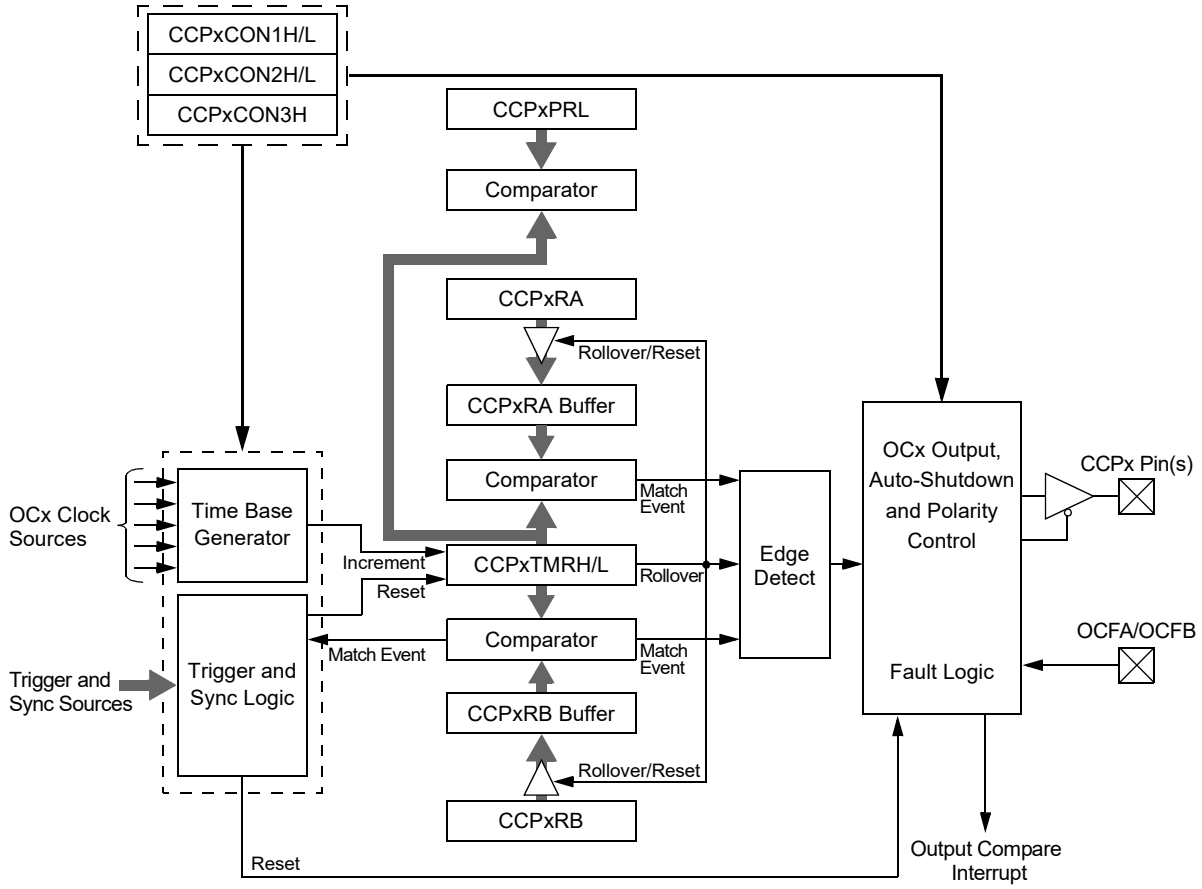
Table 23-2 shows the various modes available in Output Compare modes.

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Table 23-2. Output Compare x/PWMx Modes

MOD[3:0] (CCPxCON1L[3:0])	T32 (CCPxCON1L[5])	Operating Mode	
0001	0	Output High on Compare (16-bit)	Single Edge Mode
0001	1	Output High on Compare (32-bit)	
0010	0	Output Low on Compare (16-bit)	
0010	1	Output Low on Compare (32-bit)	
0011	0	Output Toggle on Compare (16-bit)	
0011	1	Output Toggle on Compare (32-bit)	
0100	0	Dual Edge Compare (16-bit)	Dual Edge Mode
0101	0	Dual Edge Compare (16-bit buffered)	PWM Mode

Figure 23-5. Output Compare x Block Diagram



23.4. Input Capture Mode

Input Capture mode is used to capture a timer value from an independent timer base upon an event on an input pin or other internal trigger source. The input capture features are useful in applications requiring frequency (time period) and pulse measurement. Figure 23-6 depicts a simplified block diagram of Input Capture mode.

Input Capture mode uses a dedicated 16/32-bit, synchronous, up-counting timer for the capture function. The timer value is written to the FIFO when a capture event occurs. The internal value may be read (with a synchronization delay) using the CCPxTMRH/L registers.

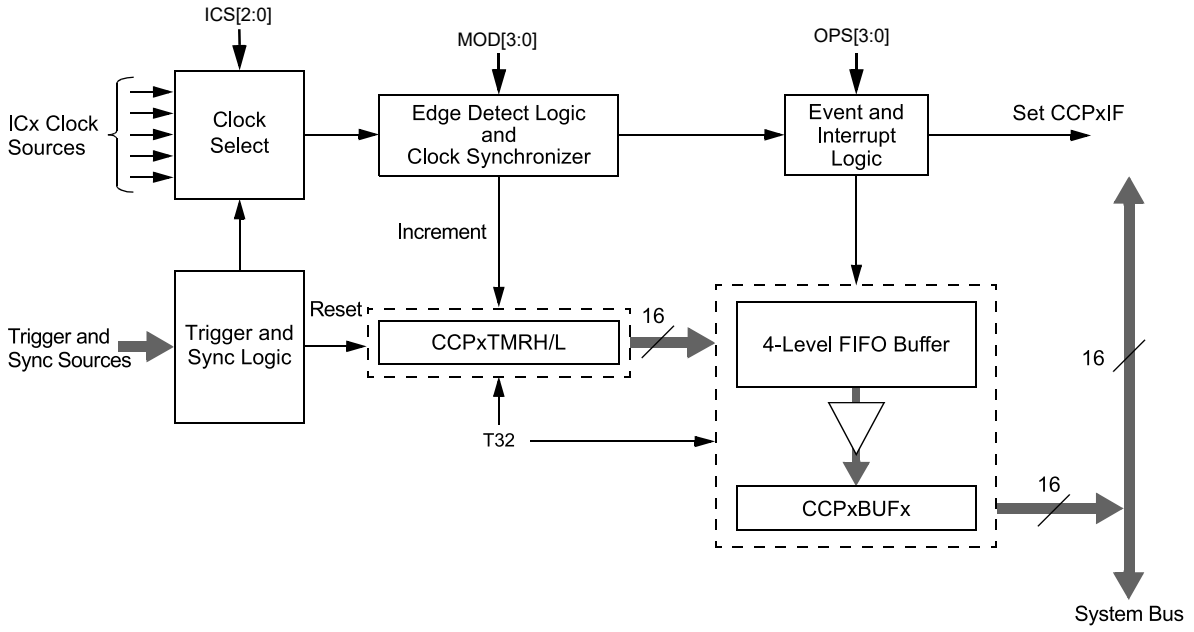
To use Input Capture mode, the CCSEL bit (CCPxCON1L[4]) must be set. The T32 and the MOD[3:0] bits are used to select the proper Capture mode, as shown in Table 23-3.

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Table 23-3. Input Capture x Modes

MOD[3:0] (CCPxCON1L[3:0])	T32 (CCPxCON1L[5])	Operating Mode
0000	0	Edge Detect (16-bit capture)
0000	1	Edge Detect (32-bit capture)
0001	0	Every Rising (16-bit capture)
0001	1	Every Rising (32-bit capture)
0010	0	Every Falling (16-bit capture)
0010	1	Every Falling (32-bit capture)
0011	0	Every Rising/Falling (16-bit capture)
0011	1	Every Rising/Falling (32-bit capture)
0100	0	Every 4th Rising (16-bit capture)
0100	1	Every 4th Rising (32-bit capture)
0101	0	Every 16th Rising (16-bit capture)
0101	1	Every 16th Rising (32-bit capture)

Figure 23-6. Input Capture x Block Diagram



23.5. Auxiliary Output

The SCCPx modules have an auxiliary (secondary) output that provides other peripherals access to internal module signals. The auxiliary output is intended to connect to other SCCP modules or other digital peripherals to provide these types of functions:

- Time Base Synchronization
- Peripheral Trigger and Clock Inputs
- Signal Gating

The type of output signal is selected using the AUXOUT[1:0] control bits (CCPxCON2H[4:3]). The type of output signal is also dependent on the module operating mode.

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Table 23-4. Auxiliary Output

AUXOUT[1:0]	CCSEL	MOD[3:0]	Comments	Signal Description
00	x	xxxx	Auxiliary output disabled	No Output
01	0	0000	Time Base modes	Time Base Period Reset or Rollover
10				Special Event Trigger Output
11				No Output
01	0	0001 through 1111	Output Compare modes	Time Base Period Reset or Rollover
10				Output Compare Event Signal
11				Output Compare Signal
01	1	xxxx	Input Capture modes	Time Base Period Reset or Rollover
10				Reflects the Value of the ICDIS bit
11				Input Capture Event Signal

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23.6. SCCP Control/Status Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0950	CCP1CON1L	15:8	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
		7:0	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
0x0952	CCP1CON1H	15:8	OPSSRC	RTRGEN			OPS3[3:0]			
		7:0	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
0x0954	CCP1CON2L	15:8	PWMRSEN	ASDGM		SSDG				
		7:0	ASDG[7:0]							
0x0956	CCP1CON2H	15:8	OENSYNC							OCAEN
		7:0	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
0x0958 ... 0x0959	Reserved									
0x095A	CCP1CON3H	15:8	OETRIG		OSCNT[2:0]					
		7:0			POLACE		PSSACE[1:0]			
0x095C	CCP1STATL	15:8						ICGARM		
		7:0	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
0x095E	CCP1STATH	15:8								
		7:0				PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP
0x0960	CCP1TMRL	15:8	TMR[15:8]							
		7:0	TMR[7:0]							
0x0962	CCP1TMRH	15:8	TMR[31:24]							
		7:0	TMR[23:16]							
0x0964	CCP1PRL	15:8	PR[15:8]							
		7:0	PR[7:0]							
0x0966	CCP1PRH	15:8	PR[31:24]							
		7:0	PR[23:16]							
0x0968	CCP1RAL	15:8	CMP[15:8]							
		7:0	CMP[7:0]							
0x096A ... 0x096B	Reserved									
0x096C	CCP1RBL	15:8	CMP[15:8]							
		7:0	CMP[7:0]							
0x096E ... 0x096F	Reserved									
0x0970	CCP1BUFL	15:8	BUF[15:8]							
		7:0	BUF[7:0]							
0x0972	CCP1BUFH	15:8	BUF[31:24]							
		7:0	BUF[23:16]							
0x0974	CCP2CON1L	15:8	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
		7:0	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
0x0976	CCP2CON1H	15:8	OPSSRC	RTRGEN			OPS3[3:0]			
		7:0	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
0x0978	CCP2CON2L	15:8	PWMRSEN	ASDGM		SSDG				
		7:0	ASDG[7:0]							
0x097A	CCP2CON2H	15:8	OENSYNC							OCAEN
		7:0	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
0x097C ... 0x097D	Reserved									
0x097E	CCP2CON3H	15:8	OETRIG		OSCNT[2:0]					
		7:0			POLACE		PSSACE[1:0]			
0x0980	CCP2STATL	15:8						ICGARM		
		7:0	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
0x0982	CCP2STATH	15:8								
		7:0				PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP
0x0984	CCP2TMRL	15:8	TMR[15:8]							
		7:0	TMR[7:0]							

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SCCP Control/Status Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0986	CCP2TMRH	15:8	TMR[31:24]							
		7:0	TMR[23:16]							
0x0988	CCP2PRL	15:8	PR[15:8]							
		7:0	PR[7:0]							
0x098A	CCP2PRH	15:8	PR[31:24]							
		7:0	PR[23:16]							
0x098C	CCP2RAL	15:8	CMP[15:8]							
		7:0	CMP[7:0]							
0x098E ... 0x098F	Reserved									
0x0990	CCP2RBL	15:8	CMP[15:8]							
		7:0	CMP[7:0]							
0x0992 ... 0x0993	Reserved									
0x0994	CCP2BUFL	15:8	BUF[15:8]							
		7:0	BUF[7:0]							
0x0996	CCP2BUFH	15:8	BUF[31:24]							
		7:0	BUF[23:16]							
0x0998	CCP3CON1L	15:8	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
		7:0	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
0x099A	CCP3CON1H	15:8	OPSSRC	RTRGEN			OPS3[3:0]			
		7:0	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
0x099C	CCP3CON2L	15:8	PWMRSEN	ASDGM		SSDG				
		7:0	ASDG[7:0]							
0x099E	CCP3CON2H	15:8	OENSYNC							OCAEN
		7:0	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
0x09A0 ... 0x09A1	Reserved									
0x09A2	CCP3CON3H	15:8	OETRIG		OSCNT[2:0]					
		7:0			POLACE		PSSACE[1:0]			
0x09A4	CCP3STATL	15:8						ICGARM		
		7:0	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
0x09A6	CCP3STATH	15:8								
		7:0				PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP
0x09A8	CCP3TMRL	15:8	TMR[15:8]							
		7:0	TMR[7:0]							
0x09AA	CCP3TMRH	15:8	TMR[31:24]							
		7:0	TMR[23:16]							
0x09AC	CCP3PRL	15:8	PR[15:8]							
		7:0	PR[7:0]							
0x09AE	CCP3PRH	15:8	PR[31:24]							
		7:0	PR[23:16]							
0x09B0	CCP3RAL	15:8	CMP[15:8]							
		7:0	CMP[7:0]							
0x09B2 ... 0x09B3	Reserved									
0x09B4	CCP3RBL	15:8	CMP[15:8]							
		7:0	CMP[7:0]							
0x09B6 ... 0x09B7	Reserved									
0x09B8	CCP3BUFL	15:8	BUF[15:8]							
		7:0	BUF[7:0]							
0x09BA	CCP3BUFH	15:8	BUF[31:24]							
		7:0	BUF[23:16]							
0x09BC	CCP4CON1L	15:8	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
		7:0	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			

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SCCP Control/Status Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x09BE	CCP4CON1H	15:8	OPSSRC	RTRGEN			OPS3[3:0]			
		7:0	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
0x09C0	CCP4CON2L	15:8	PWMRSEN	ASDGM		SSDG				
		7:0	ASDG[7:0]							
0x09C2	CCP4CON2H	15:8	OENSYNC							OCAEN
		7:0	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
0x09C4 ... 0x09C5	Reserved									
0x09C6	CCP4CON3H	15:8	OETRIG		OSCNT[2:0]					
		7:0			POLACE		PSSACE[1:0]			
0x09C8	CCP4STATL	15:8						ICGARM		
		7:0	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
0x09CA	CCP4STATH	15:8								
		7:0				PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP
0x09CC	CCP4TMRL	15:8	TMR[15:8]							
		7:0	TMR[7:0]							
0x09CE	CCP4TMRH	15:8	TMR[31:24]							
		7:0	TMR[23:16]							
0x09D0	CCP4PRL	15:8	PR[15:8]							
		7:0	PR[7:0]							
0x09D2	CCP4PRH	15:8	PR[31:24]							
		7:0	PR[23:16]							
0x09D4	CCP4RAL	15:8	CMP[15:8]							
		7:0	CMP[7:0]							
0x09D6 ... 0x09D7	Reserved									
0x09D8	CCP4RBL	15:8	CMP[15:8]							
		7:0	CMP[7:0]							
0x09DA ... 0x09DB	Reserved									
0x09DC	CCP4BUFL	15:8	BUF[15:8]							
		7:0	BUF[7:0]							
0x09DE	CCP4BUFH	15:8	BUF[31:24]							
		7:0	BUF[23:16]							

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23.6.1. CCPx Control 1 Low Register

Name: CCPxCON1L
Offset: 0x950, 0x974, 0x998, 0x9BC

Bit	15	14	13	12	11	10	9	8
	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – CCPON CCPx Module Enable bit

Value	Description
1	Module is enabled with an operating mode specified by the MOD[3:0] control bits.
0	Module is disabled.

Bit 13 – CCPSIDL CCPx Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode.
0	Continues module operation in Idle mode.

Bit 12 – CCPSLP CCPx Sleep Mode Enable bit

Value	Description
1	Module continues to operate in Sleep modes.
0	Module does not operate in Sleep modes.

Bit 11 – TMRSYNC Time Base Clock Synchronization bit

Value	Description
1	Asynchronous module time base clock is selected and synchronized to the internal system clocks (CLKSEL[2:0] ≠ 000).
0	Synchronous module time base clock is selected and does not require synchronization (CLKSEL[2:0] = 000).

Bits 10:8 – CLKSEL[2:0] CCPx Time Base Clock Select bits

Value	Description
111	PPS TCKIx input
110	CLC4 out
101	CLC3 out
100	CLC2 out
011	CLC1 out
010	F_{OSC}
001	Reference Clock (REFCLKO)
000	F_P

Bits 7:6 – TMRPS[1:0] Time Base Prescale Select bits

Value	Description
11	1:64 Prescaler

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Value	Description
10	1:16 Prescaler
01	1:4 Prescaler
00	1:1 Prescaler

Bit 5 – T32 32-Bit Time Base Select bit

Value	Description
1	Uses 32-bit time base for timer, single edge output compare or input capture function.
0	Uses 16-bit time base for timer, single edge output compare or input capture function.

Bit 4 – CCSEL Capture/Compare Mode Select bit

Value	Description
1	Input capture peripheral.
0	Output Compare/PWM/Timer peripheral (exact function is selected by the MOD[3:0] bits).

Bits 3:0 – MOD[3:0] CCPx Mode Select bits

For CCSEL = 1 (Input Capture modes):

Value	Description
1xxx	Reserved
011x	Reserved
0101	Capture every 16th rising edge.
0100	Capture every 4th rising edge.
0011	Capture every rising and falling edge.
0010	Capture every falling edge.
0001	Capture every rising edge.
0000	Capture every rising and falling edge (Edge Detect mode).

For CCSEL = 0 (Output Compare/Timer modes):

Value	Description
1111	External Input mode: Pulse generator is disabled, source is selected by ICS[2:0].
1110	Reserved
110x	Reserved
10xx	Reserved
0111	Reserved
0110	Reserved
0101	Dual Edge Compare mode, buffered
0100	Dual Edge Compare mode
0011	16-Bit/32-Bit Single Edge mode, toggles output on compare match.
0010	16-Bit/32-Bit Single Edge mode, drives output low on compare match.
0001	16-Bit/32-Bit Single Edge mode, drives output high on compare match.
0000	16-Bit/32-Bit Timer mode, output functions are disabled.

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23.6.2. CCPx Control 1 High Register

Name: CCPxCON1H
Offset: 0x952, 0x976, 0x99A, 0x9BE

Notes:

1. This control bit has no function in Input Capture modes.
2. This control bit has no function when TRIGEN = 0.
3. Output postscale settings, from 1:5 to 1:16 (0100–1111), will result in a FIFO buffer overflow for Input Capture modes.

Bit	15	14	13	12	11	10	9	8
	OPSSRC	RTRGEN			OPS3[3:0]			
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OPSSRC Output Postscaler Source Select bit(1)

Value	Description
1	Output postscaler scales module trigger output events
0	Output postscaler scales time base interrupt events

Bit 14 – RTRGEN Retrigger Enable bit(2)

Value	Description
1	Time base can be retriggered when TRIGEN bit = 1
0	Time base may not be retriggered when TRIGEN bit = 1

Bits 11:8 – OPS3[3:0] CCPx Interrupt Output Postscale Select bits(3)

Value	Description
1111	Interrupt every 16th time base period match
1110	Interrupt every 15th time base period match
. . .	
0100	Interrupt every 5th time base period match
0011	Interrupt every 4th time base period match or 4th input capture event
0010	Interrupt every 3rd time base period match or 3rd input capture event
0001	Interrupt every 2nd time base period match or 2nd input capture event
0000	Interrupt after each time base period match or input capture event

Bit 7 – TRIGEN CCPx Trigger Enable bit

Value	Description
1	Trigger operation of time base is enabled
0	Trigger operation of time base is disabled

Bit 6 – ONESHOT One-Shot Trigger Mode Enable bit

Value	Description
1	One-Shot Trigger mode is enabled; trigger duration is set by OSCNT[2:0]
0	One-Shot Trigger mode is disabled

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Bit 5 – ALTSYNC CCPx Clock Select bit

Value	Description
1	An alternate signal is used as the module synchronization output signal
0	The module synchronization output signal is the Time Base Reset/rollover event

Bits 4:0 – SYNC[4:0] CCPx Synchronization Source Select bits

23.6.3. Synchronization Sources

Table 23-5. Synchronization Sources

SYNC[4:0]	Synchronization Source
00000	None; Timer with Rollover on CCPxPR Match or FFFFh
00001	Module's Own Timer Sync Out
00010	Sync Output SCCP2
00011	Sync Output SCCP3
00100	Sync Output SCCP4
00101-01000	Reserved
01001	INT0
01010	INT1
01011	INT2
01100	UART1 RX Edge Detect
01101	UART1 TX Edge Detect
01110	UART2 RX Edge Detect
01111	UART2 TX Edge Detect
10000	CLC1 Output
10001	CLC2 Output
10010	CLC3 Output
10011	CLC4 Output
10100	UART3 RX Edge Detect
10101	UART3 TX Edge Detect
10110	Reserved
10111	Comparator 1 Output
11000	Comparator 2 Output
11001-11110	Reserved
11111	None; Timer with Auto-Rollover (FFFFh → 0000h)

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23.6.4. CCPx Control 2 Low Register

Name: CCPxCON2L
Offset: 0x954, 0x978, 0x99C, 0x9C0

Bit	15	14	13	12	11	10	9	8
	PWMRSEN	ASDGM		SSDG				
Access	R/W	R/W		R/W				
Reset	0	0		0				

Bit	7	6	5	4	3	2	1	0
	ASDG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – PWMRSEN CCPx PWM Restart Enable bit

Value	Description
1	ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended.
0	ASEVT bit must be cleared in software to resume PWM activity on output pins.

Bit 14 – ASDGM CCPx Auto-Shutdown Gate Mode Enable bit

Value	Description
1	Waits until the next Time Base Reset or rollover for shutdown to occur.
0	Shutdown event occurs immediately.

Bit 12 – SSDG CCPx Software Shutdown/Gate Control bit

Value	Description
1	Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting of ASDGM bit still applies).
0	Normal module operation.

Bits 7:0 – ASDG[7:0] CCPx Auto-Shutdown/Gating Source Enable bits

Value	Description
1	ASDGx Source n is enabled (see Auto-Shutdown and Gating Sources for auto-shutdown/gating sources).
0	ASDGx Source n is disabled.

23.6.5. Auto-Shutdown and Gating Sources

Table 23-6. Auto-Shutdown and Gating Sources

ASDG[x] Bit	Auto-Shutdown/Gating Source			
	SCCP1	SCCP2	SCCP3	SCCP4
0	Comparator 1 Output			
1	Comparator 2 Output			
2	OCFC			
3	OCFD			
4	ICM1(1)	ICM2(1)	ICM3(1)	ICM4(1)
5	CLC1(1)			
6	OCFA(1)			
7	OCFB(1)			

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Table 23-6. Auto-Shutdown and Gating Sources (continued)

ASDG[x] Bit	Auto-Shutdown/Gating Source			
	SCCP1	SCCP2	SCCP3	SCCP4

Note:

1. Selected by Peripheral Pin Select (PPS).

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23.6.6. CCPx Control 2 High Register

Name: CCPxCON2H
Offset: 0x956, 0x97A, 0x99E, 0x9C2

Bit	15	14	13	12	11	10	9	8
	OENSYNC							OCAEN
Access	R/W							R/W
Reset	0							0

Bit	7	6	5	4	3	2	1	0
	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 15 – OENSYNC Output Enable Synchronization bit

Value	Description
1	Updates by output enable bits occur on the next Time Base Reset or rollover.
0	Updates by output enable bits occur immediately.

Bit 8 – OCAEN Output Enable/Steering Control bit

Value	Description
1	OCMA pin is controlled by the CCPx module and produces an output compare or PWM signal.
0	OCMA pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin.

Bits 7:6 – ICGSM[1:0] Input Capture Gating Source Mode Control bits

Value	Description
11	Reserved
10	One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1).
01	One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0).
00	Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events.

Bits 4:3 – AUXOUT[1:0] Auxiliary Output Signal on Event Selection bits

Value	Description
11	Input capture or output compare event; no signal in Timer mode.
10	Signal output is defined by module operating mode (see Auxiliary Output).
01	Time base rollover event (all modes).
00	Disabled

Bits 2:0 – ICS[2:0] Input Capture Source Select bits

Value	Description
111	CLC4 output
110	CLC3 output
101	CLC2 output
100	CLC1 output
011	Reserved
010	Comparator 2 output
001	Comparator 1 output
000	SCCP Input Capture x (ICx) pin (PPS)

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23.6.7. CCPx Control 3 High Register

Name: CCPxCON3H
Offset: 0x95A, 0x97E, 0x9A2, 0x9C6

Bit	15	14	13	12	11	10	9	8
	OETRIG	OSCNT[2:0]						
Access	R/W	R/W	R/W	R/W				
Reset	0	0	0	0				

Bit	7	6	5	4	3	2	1	0
			POLACE		PSSACE[1:0]			
Access			R/W		R/W	R/W		
Reset			0		0	0		

Bit 15 – OETRIG CCPx Dead-Time Select bit

Value	Description
1	For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered.
0	Normal output pin operation.

Bits 14:12 – OSCNT[2:0] One-Shot Event Count bits

Value	Description
111	Extends one-shot event by seven time base periods (eight time base periods total).
110	Extends one-shot event by six time base periods (seven time base periods total).
101	Extends one-shot event by five time base periods (six time base periods total).
100	Extends one-shot event by four time base periods (five time base periods total).
011	Extends one-shot event by three time base periods (four time base periods total).
010	Extends one-shot event by two time base periods (three time base periods total).
001	Extends one-shot event by one time base period (two time base periods total).
000	Does not extend one-shot trigger event.

Bit 5 – POLACE CCPx Output Pins, OCxA, OCxC and OCxE, Polarity Control bit

Value	Description
1	Output pin polarity is active-low.
0	Output pin polarity is active-high.

Bits 3:2 – PSSACE[1:0] PWMx Output Pins, OCxA, OCxC and OCxE, Shutdown State Control bits

Value	Description
11	Pins are driven active when a shutdown event occurs.
10	Pins are driven inactive when a shutdown event occurs.
0x	Pins are in a High-Impedance state when a shutdown event occurs.

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23.6.8. CCPx Status Register

Name: CCPxSTATL
Offset: 0x95C, 0x980, 0x9A4, 0x9C8

Legend: C = Clearable bit; W1 = Write '1' Only bit

Bit	15	14	13	12	11	10	9	8
						ICGARM		
Access						W1		
Reset						0		

Bit	7	6	5	4	3	2	1	0
	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
Access	R	W1	W1	R/C	R/C	R/C	R/C	R/C
Reset	0	0	0	0	0	0	0	0

Bit 10 – ICGARM Input Capture Gate Arm bit
A write of '1' to this location will arm the input capture gating logic for a one-shot gate event when ICGSM[1:0] = 01 or 10. Bit always reads as '0'.

Bit 7 – CCPTRIG CCPx Trigger Status bit

Value	Description
1	Timer has been triggered and is running.
0	Timer has not been triggered and is held in Reset.

Bit 6 – TRSET CCPx Trigger Set Request bit
Writes '1' to this location to trigger the timer when TRIGEN = 1 (location always reads as '0').

Bit 5 – TRCLR CCPx Trigger Clear Request bit
Writes '1' to this location to cancel the timer trigger when TRIGEN = 1 (location always reads as '0').

Bit 4 – ASEVT CCPx Auto-Shutdown Event Status/Control bit

Value	Description
1	A shutdown event is in progress; CCPx outputs are in the Shutdown state.
0	CCPx outputs operate normally.

Bit 3 – SCEVT Single Edge Compare Event Status bit

Value	Description
1	A single edge compare event has occurred.
0	A single edge compare event has not occurred.

Bit 2 – ICDIS Input Capture x Disable bit

Value	Description
1	Event on Input Capture x pin (ICx) does not generate a capture event.
0	Event on Input Capture x pin will generate a capture event.

Bit 1 – ICOV Input Capture x Buffer Overflow Status bit

Value	Description
1	The Input Capture x FIFO buffer has overflowed.
0	The Input Capture x FIFO buffer has not overflowed.

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Bit 0 – ICBNE Input Capture x Buffer Status bit

Value	Description
1	Input Capture x buffer has data available.
0	Input Capture x buffer is empty.

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23.6.9. CCPx Status Register High

Name: CCPxSTATH
Offset: 0x95E, 0x982, 0x9A6, 0x9CA

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP
Access				R	R	R	R/C	R
Reset				0	0	0	0	0

Bit 4 – PRLWIP CCPxPRL Write in Progress Status bit

Bit 3 – TMRHWIP CCPxTMRH Write in Progress Status bit

Value	Description
1	An update to the CCPxTMRH register with the buffered contents is in progress.
0	An update to the CCPxTMRH register is not in progress.

Bit 2 – TMRLWIP CCPxTMRL Write in Progress Status bit

Value	Description
1	An update to the CCPxTMRL register with the buffered contents is in progress.
0	An update to the CCPxTMRL register is not in progress.

Bit 1 – RBWIP CCPxRB Write in Progress Status bit

Value	Description
1	An update to the CCPxRB register with the buffered contents is in progress.
0	An update to the CCPxRB register is not in progress.

Bit 0 – RAWIP CCPxRA Write in Progress Status bit

Value	Description
1	An update to the CCPxRA register with the buffered contents is in progress.
0	An update to the CCPxRA register is not in progress.

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23.6.10. CCPx Time Base Register Low

Name: CCPxTMRL
Offset: 0x960, 0x984, 0x9A8, 0x9CC

Bit	15	14	13	12	11	10	9	8
	TMR[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TMR[15:0] 16-Bit Time Base Value bits

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23.6.11. CCPx Time Base High Register

Name: CCPxTMRH
Offset: 0x962, 0x986, 0x9AA, 0x9CE

Bit	15	14	13	12	11	10	9	8
	TMR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TMR[31:16] 16-Bit Time Base Value bits

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23.6.12. CCPx Period Low Register

Name: CCPxPRL
Offset: 0x964, 0x988, 0x9AC, 0x9D0

Bit	15	14	13	12	11	10	9	8
	PR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PR[15:0] Period Low Register bits

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23.6.13. CCPx Period High Register

Name: CCPxPRH
Offset: 0x966, 0x98A, 0x9AE, 0x9D2

Bit	15	14	13	12	11	10	9	8
	PR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PR[31:16] Period Register bits

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23.6.14. CCPx Primary Compare Register Low (Timer/Compare Modes Only)

Name: CCPxRAL
Offset: 0x968, 0x98C, 0x9B0, 0x9D4

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMP[15:0] Primary Compare Value bits
The 16-bit value to be compared against the CCP time base.

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23.6.15. CCPx Secondary Compare Register Low (Timer/Compare Modes Only)

Name: CCPxRBL
Offset: 0x96C, 0x990, 0x9B4, 0x9D8

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMP[15:0] Secondary Compare Value bits
The 16-bit value to be compared against the CCP time base.

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23.6.16. CCPx Capture Buffer Register Low (Capture Modes Only)

Name: CCPxBUFL
Offset: 0x970, 0x994, 0x9B8, 0x9DC

Bit	15	14	13	12	11	10	9	8
	BUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BUF[15:0] Compare Buffer Value bits
Indicates the oldest captured time base value in the FIFO.

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23.6.17. CCPx Capture Buffer High Register (Capture Modes Only)

Name: CCPxBUFH
Offset: 0x972, 0x996, 0x9BA, 0x9DE

Bit	15	14	13	12	11	10	9	8
	BUF[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUF[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BUF[31:16] Compare Buffer Value bits

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24. Configurable Logic Cell (CLC)

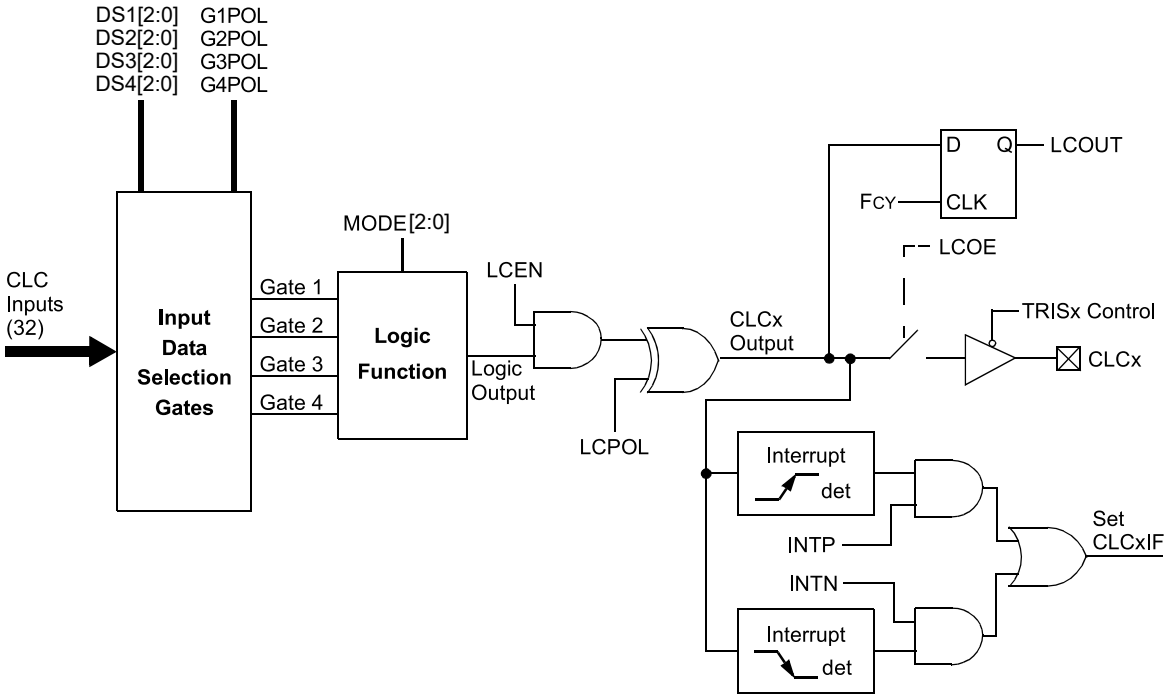
Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Configurable Logic Cell (CLC)"** (www.microchip.com/DS70005298) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs, since the CLC module can operate outside the limitations of software execution, and supports a vast amount of output designs.

There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 24-1 shows an overview of the module.

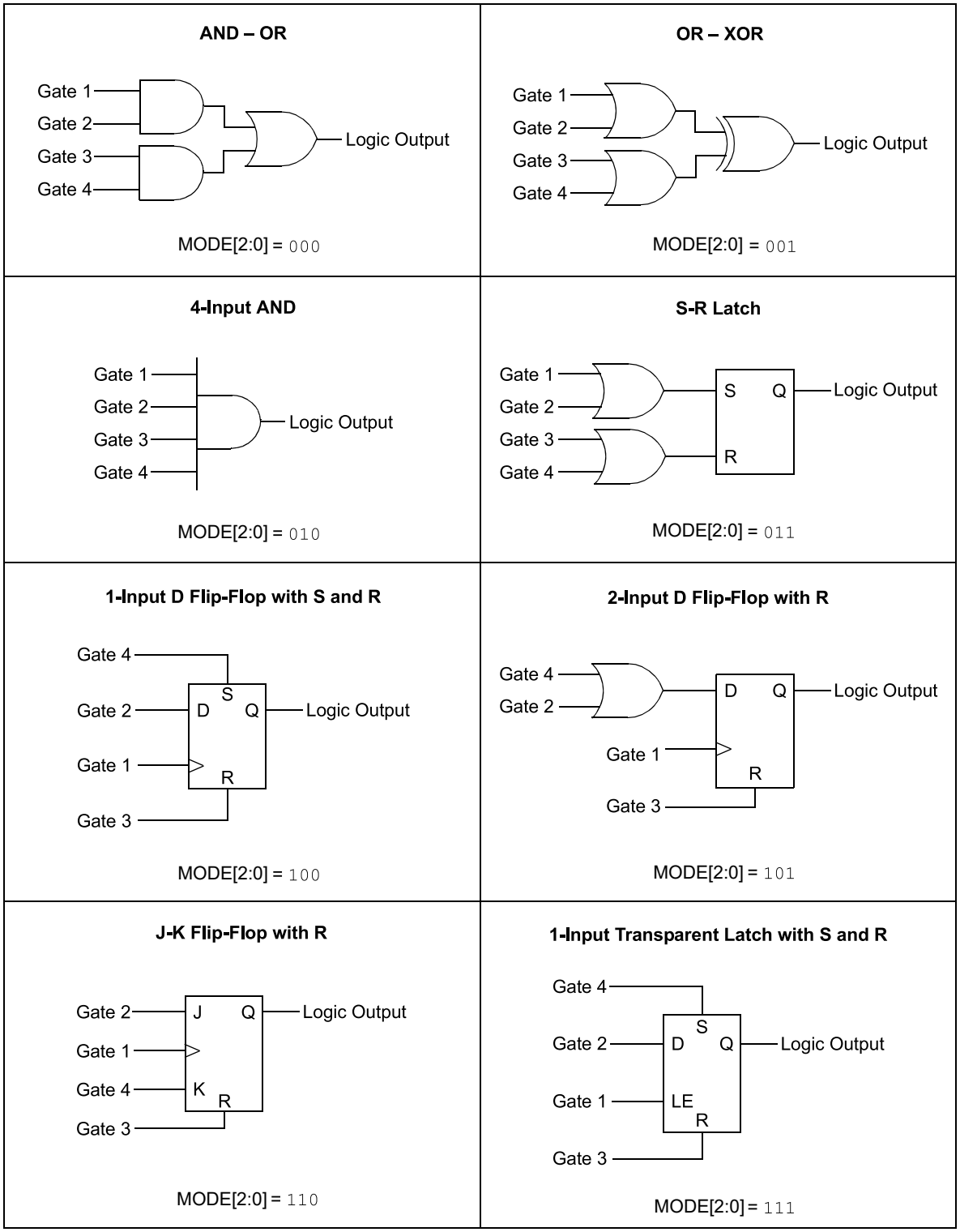
Figure 24-3 shows the details of the data source multiplexers and Figure 24-2 shows the logic input gate connections.

Figure 24-1. CLCx Module



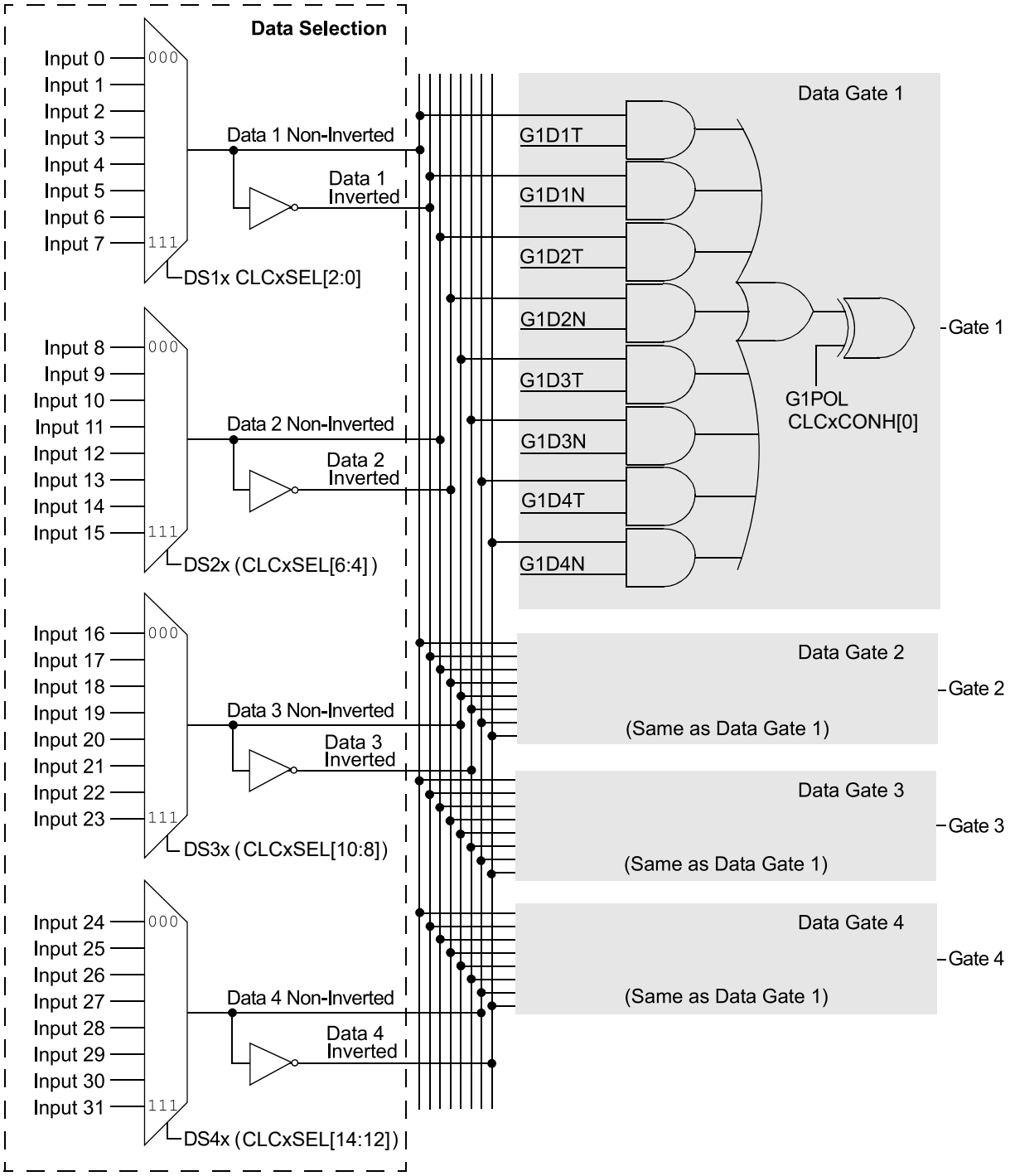
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Figure 24-2. CLCx Logic Function Combinatorial Options



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Figure 24-3. CLCx Input Source Selection Diagram



Note: All controls are undefined at power-up.

24.1. Control Registers

The CLCx Control registers (CLCxCONL and CLCxCONH) are used to enable the module and interrupts, control the output enable bit, select output polarity and select the logic function. The

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CLCx Control registers also allow the user to control the logic polarity of not only the cell output, but also some intermediate variables.

The CLCx Input MUX Select register (CLCxSEL) allows the user to select up to four data input sources using the four data input selection multiplexers. Each multiplexer has a list of eight data sources available.

The CLCx Gate Logic Input Select registers (CLCxGLSL and CLCxGLSH) allow the user to select which outputs from each of the selection MUXes are used as inputs to the input gates of the logic cell. Each data source MUX outputs both a true and a negated version of its output. All of these eight signals are enabled and ORed together by the logic cell input gates. If no inputs are selected (CLCxGLS = 0x00), the output will be zero or one, depending on the GxPOL bits.

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24.2. CLC Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xC0	CLC1CONL	15:8	LCEN				INTP	INTN		
		7:0	LCOE	LCOUT	LCPOL				MODE[2:0]	
0xC2	CLC1CONH	15:8								
		7:0					G4POL	G3POL	G2POL	G1POL
0xC4	CLC1SEL	15:8		DS4[2:0]					DS3[2:0]	
		7:0		DS2[2:0]					DS1[2:0]	
0xC6 ... 0xC7	Reserved									
0xC8	CLC1GLSL	15:8	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
		7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0xCA	CLC1GLSH	15:8	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
		7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0xCC	CLC2CONL	15:8	LCEN				INTP	INTN		
		7:0	LCOE	LCOUT	LCPOL				MODE[2:0]	
0xCE	CLC2CONH	15:8								
		7:0					G4POL	G3POL	G2POL	G1POL
0xD0	CLC2SEL	15:8		DS4[2:0]					DS3[2:0]	
		7:0		DS2[2:0]					DS1[2:0]	
0xD2 ... 0xD3	Reserved									
0xD4	CLC2GLSL	15:8	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
		7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0xD6	CLC2GLSH	15:8	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
		7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0xD8	CLC3CONL	15:8	LCEN				INTP	INTN		
		7:0	LCOE	LCOUT	LCPOL				MODE[2:0]	
0xDA	CLC3CONH	15:8								
		7:0					G4POL	G3POL	G2POL	G1POL
0xDC	CLC3SEL	15:8		DS4[2:0]					DS3[2:0]	
		7:0		DS2[2:0]					DS1[2:0]	
0xDE ... 0xDF	Reserved									
0xE0	CLC3GLSL	15:8	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
		7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0xE2	CLC3GLSH	15:8	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
		7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0xE4	CLC4CONL	15:8	LCEN				INTP	INTN		
		7:0	LCOE	LCOUT	LCPOL				MODE[2:0]	
0xE6	CLC4CONH	15:8								
		7:0					G4POL	G3POL	G2POL	G1POL
0xE8	CLC4SEL	15:8		DS4[2:0]					DS3[2:0]	
		7:0		DS2[2:0]					DS1[2:0]	
0xEA ... 0xEB	Reserved									
0xEC	CLC4GLSL	15:8	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
		7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0xEE	CLC4GLSH	15:8	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
		7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N

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24.2.1. CLCx Control Register Low

Name: CLCxCONL
Offset: 0x0C0, 0x0CC, 0x0D8, 0x0E4

Bit	15	14	13	12	11	10	9	8
	LCEN				INTP	INTN		
Access	R/W				R/W	R/W		
Reset	0				0	0		

Bit	7	6	5	4	3	2	1	0
	LCOE	LCOUT	LCPOL			MODE[2:0]		
Access	R	R	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bit 15 – LCEN CLCx Enable bit

Value	Description
1	CLCx is enabled and mixing input signals.
0	CLCx is disabled and has logic zero outputs.

Bit 11 – INTP CLCx Positive Edge Interrupt Enable bit

Value	Description
1	Interrupt will be generated when a rising edge occurs on LCOUT.
0	Interrupt will not be generated.

Bit 10 – INTN CLCx Negative Edge Interrupt Enable bit

Value	Description
1	Interrupt will be generated when a falling edge occurs on LCOUT.
0	Interrupt will not be generated.

Bit 7 – LCOE CLCx Port Enable bit

Value	Description
1	CLCx port pin output is enabled.
0	CLCx port pin output is disabled.

Bit 6 – LCOUT CLCx Data Output Status bit

Value	Description
1	CLCx output high.
0	CLCx output low.

Bit 5 – LCPOL CLCx Output Polarity Control bit

Value	Description
1	The output of the module is inverted.
0	The output of the module is not inverted.

Bits 2:0 – MODE[2:0] CLCx Mode bits

Value	Description
111	Single input transparent latch with S and R.
110	JK flip-flop with R.

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Value	Description
101	Two-input D flip-flop with R.
100	Single input D flip-flop with S and R.
011	SR latch
010	Four-input AND
001	Four-input OR-XOR
000	Four-input AND-OR

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24.2.2. CLCx Control Register High

Name: CLCxCONH
Offset: 0x0C2, 0x0CE, 0x0DA, 0x0E6

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					G4POL	G3POL	G2POL	G1POL
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – G4POL Gate 4 Polarity Control bit

Value	Description
1	Channel 4 logic output is inverted when applied to the logic cell.
0	Channel 4 logic output is not inverted.

Bit 2 – G3POL Gate 3 Polarity Control bit

Value	Description
1	Channel 3 logic output is inverted when applied to the logic cell.
0	Channel 3 logic output is not inverted.

Bit 1 – G2POL Gate 2 Polarity Control bit

Value	Description
1	Channel 2 logic output is inverted when applied to the logic cell.
0	Channel 2 logic output is not inverted.

Bit 0 – G1POL Gate 1 Polarity Control bit

Value	Description
1	Channel 1 logic output is inverted when applied to the logic cell.
0	Channel 1 logic output is not inverted.

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24.2.3. CLCx Input MUX Select Register

Name: CLCxSEL
Offset: 0x0C4, 0x0D0, 0x0DC, 0x0E8

Note:
1. Valid only when SPI is used on PPS.

Bit	15	14	13	12	11	10	9	8
		DS4[2:0]				DS3[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
		DS2[2:0]				DS1[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bits 14:12 – DS4[2:0] Data Selection MUX 4 Signal Selection bits

Value	Description
111	SCCP3 auxiliary out
110	SCCP1 auxiliary out
101	CLCIND RP pin
100	Reserved
011	SPI1 Input (SDI)(1)
010	Reserved
001	CLC2 output
000	PWM Event A

Bits 10:8 – DS3[2:0] Data Selection MUX 3 Signal Selection bits

Value	Description
111	SCCP4 OC output
110	SCCP3 OC output
101	CLC4 out
100	UART1 RX
011	SPI1 Output (SDO)(1)
010	Comparator 2 output
001	CLC1 output
000	CLCINC I/O pin

Bits 6:4 – DS2[2:0] Data Selection MUX 2 Signal Selection bits

Value	Description
111	SCCP2 OC output
110	SCCP1 OC output
101	SCCP2 trigger
100	SCCP1 trigger
011	UART1 TX
010	Comparator 1 output
001	Reserved
000	CLCINB I/O pin

Bits 2:0 – DS1[2:0] Data Selection MUX 1 Signal Selection bits

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Value	Description
111	SCCP4 auxiliary out
110	SCCP2 auxiliary out
101	Reserved
100	REFCLKO output
011	INTRC/LPRC clock source
010	CLC3 out
001	F_{CY}
000	CLCINA I/O pin

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24.2.4. CLCx Gate Logic Input Select Low Register

Name: CLCxGLSL
Offset: 0x0C8, 0x0D4, 0x0E0, 0x0EC

Bit	15	14	13	12	11	10	9	8
	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – G2D4T Gate 2 Data Source 4 True Enable bit

Value	Description
1	Data Source 4 signal is enabled for Gate 2.
0	Data Source 4 signal is disabled for Gate 2.

Bit 14 – G2D4N Gate 2 Data Source 4 Negated Enable bit

Value	Description
1	Data Source 4 inverted signal is enabled for Gate 2.
0	Data Source 4 inverted signal is disabled for Gate 2.

Bit 13 – G2D3T Gate 2 Data Source 3 True Enable bit

Value	Description
1	Data Source 3 signal is enabled for Gate 2.
0	Data Source 3 signal is disabled for Gate 2.

Bit 12 – G2D3N Gate 2 Data Source 3 Negated Enable bit

Value	Description
1	Data Source 3 inverted signal is enabled for Gate 2.
0	Data Source 3 inverted signal is disabled for Gate 2.

Bit 11 – G2D2T Gate 2 Data Source 2 True Enable bit

Value	Description
1	Data Source 2 signal is enabled for Gate 2.
0	Data Source 2 signal is disabled for Gate 2.

Bit 10 – G2D2N Gate 2 Data Source 2 Negated Enable bit

Value	Description
1	Data Source 2 inverted signal is enabled for Gate 2.
0	Data Source 2 inverted signal is disabled for Gate 2.

Bit 9 – G2D1T Gate 2 Data Source 1 True Enable bit

Value	Description
1	Data Source 1 signal is enabled for Gate 2.
0	Data Source 1 signal is disabled for Gate 2.

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Bit 8 – G2D1N Gate 2 Data Source 1 Negated Enable bit

Value	Description
1	Data Source 1 inverted signal is enabled for Gate 2.
0	Data Source 1 inverted signal is disabled for Gate 2.

Bit 7 – G1D4T Gate 1 Data Source 4 True Enable bit

Value	Description
1	Data Source 4 signal is enabled for Gate 1.
0	Data Source 4 signal is disabled for Gate 1.

Bit 6 – G1D4N Gate 1 Data Source 4 Negated Enable bit

Value	Description
1	Data Source 4 inverted signal is enabled for Gate 1.
0	Data Source 4 inverted signal is disabled for Gate 1.

Bit 5 – G1D3T Gate 1 Data Source 3 True Enable bit

Value	Description
1	Data Source 3 signal is enabled for Gate 1.
0	Data Source 3 signal is disabled for Gate 1.

Bit 4 – G1D3N Gate 1 Data Source 3 Negated Enable bit

Value	Description
1	Data Source 3 inverted signal is enabled for Gate 1.
0	Data Source 3 inverted signal is disabled for Gate 1.

Bit 3 – G1D2T Gate 1 Data Source 2 True Enable bit

Value	Description
1	Data Source 2 signal is enabled for Gate 1.
0	Data Source 2 signal is disabled for Gate 1.

Bit 2 – G1D2N Gate 1 Data Source 2 Negated Enable bit

Value	Description
1	Data Source 2 inverted signal is enabled for Gate 1.
0	Data Source 2 inverted signal is disabled for Gate 1.

Bit 1 – G1D1T Gate 1 Data Source 1 True Enable bit

Value	Description
1	Data Source 1 signal is enabled for Gate 1.
0	Data Source 1 signal is disabled for Gate 1.

Bit 0 – G1D1N Gate 1 Data Source 1 Negated Enable bit

Value	Description
1	Data Source 1 inverted signal is enabled for Gate 1.
0	Data Source 1 inverted signal is disabled for Gate 1.

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24.2.5. CLCx Gate Logic Input Select High Register

Name: CLCxGLSH
Offset: 0x0CA, 0x0D6, 0x0E2, 0x0EE

Bit	15	14	13	12	11	10	9	8
	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – G4D4T Gate 4 Data Source 4 True Enable bit

Value	Description
1	Data Source 4 signal is enabled for Gate 4.
0	Data Source 4 signal is disabled for Gate 4.

Bit 14 – G4D4N Gate 4 Data Source 4 Negated Enable bit

Value	Description
1	Data Source 4 inverted signal is enabled for Gate 4.
0	Data Source 4 inverted signal is disabled for Gate 4.

Bit 13 – G4D3T Gate 4 Data Source 3 True Enable bit

Value	Description
1	Data Source 3 signal is enabled for Gate 4.
0	Data Source 3 signal is disabled for Gate 4.

Bit 12 – G4D3N Gate 4 Data Source 3 Negated Enable bit

Value	Description
1	Data Source 3 inverted signal is enabled for Gate 4.
0	Data Source 3 inverted signal is disabled for Gate 4.

Bit 11 – G4D2T Gate 4 Data Source 2 True Enable bit

Value	Description
1	Data Source 2 signal is enabled for Gate 4.
0	Data Source 2 signal is disabled for Gate 4.

Bit 10 – G4D2N Gate 4 Data Source 2 Negated Enable bit

Value	Description
1	Data Source 2 inverted signal is enabled for Gate 4.
0	Data Source 2 inverted signal is disabled for Gate 4.

Bit 9 – G4D1T Gate 4 Data Source 1 True Enable bit

Value	Description
1	Data Source 1 signal is enabled for Gate 4.
0	Data Source 1 signal is disabled for Gate 4.

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Bit 8 – G4D1N Gate 4 Data Source 1 Negated Enable bit

Value	Description
1	Data Source 1 inverted signal is enabled for Gate 4.
0	Data Source 1 inverted signal is disabled for Gate 4.

Bit 7 – G3D4T Gate 3 Data Source 4 True Enable bit

Value	Description
1	Data Source 4 signal is enabled for Gate 3.
0	Data Source 4 signal is disabled for Gate 3.

Bit 6 – G3D4N Gate 3 Data Source 4 Negated Enable bit

Value	Description
1	Data Source 4 inverted signal is enabled for Gate 3.
0	Data Source 4 inverted signal is disabled for Gate 3.

Bit 5 – G3D3T Gate 3 Data Source 3 True Enable bit

Value	Description
1	Data Source 3 signal is enabled for Gate 3.
0	Data Source 3 signal is disabled for Gate 3.

Bit 4 – G3D3N Gate 3 Data Source 3 Negated Enable bit

Value	Description
1	Data Source 3 inverted signal is enabled for Gate 3.
0	Data Source 3 inverted signal is disabled for Gate 3.

Bit 3 – G3D2T Gate 3 Data Source 2 True Enable bit

Value	Description
1	Data Source 2 signal is enabled for Gate 3.
0	Data Source 2 signal is disabled for Gate 3.

Bit 2 – G3D2N Gate 3 Data Source 2 Negated Enable bit

Value	Description
1	Data Source 2 inverted signal is enabled for Gate 3.
0	Data Source 2 inverted signal is disabled for Gate 3.

Bit 1 – G3D1T Gate 3 Data Source 1 True Enable bit

Value	Description
1	Data Source 1 signal is enabled for Gate 3.
0	Data Source 1 signal is disabled for Gate 3.

Bit 0 – G3D1N Gate 3 Data Source 1 Negated Enable bit

Value	Description
1	Data Source 1 inverted signal is enabled for Gate 3.
0	Data Source 1 inverted signal is disabled for Gate 3.

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25. Peripheral Trigger Generator (PTG)

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Peripheral Trigger Generator (PTG)"** (www.microchip.com/DS70000669) in the *"dsPIC33/PIC24 Family Reference Manual"*.

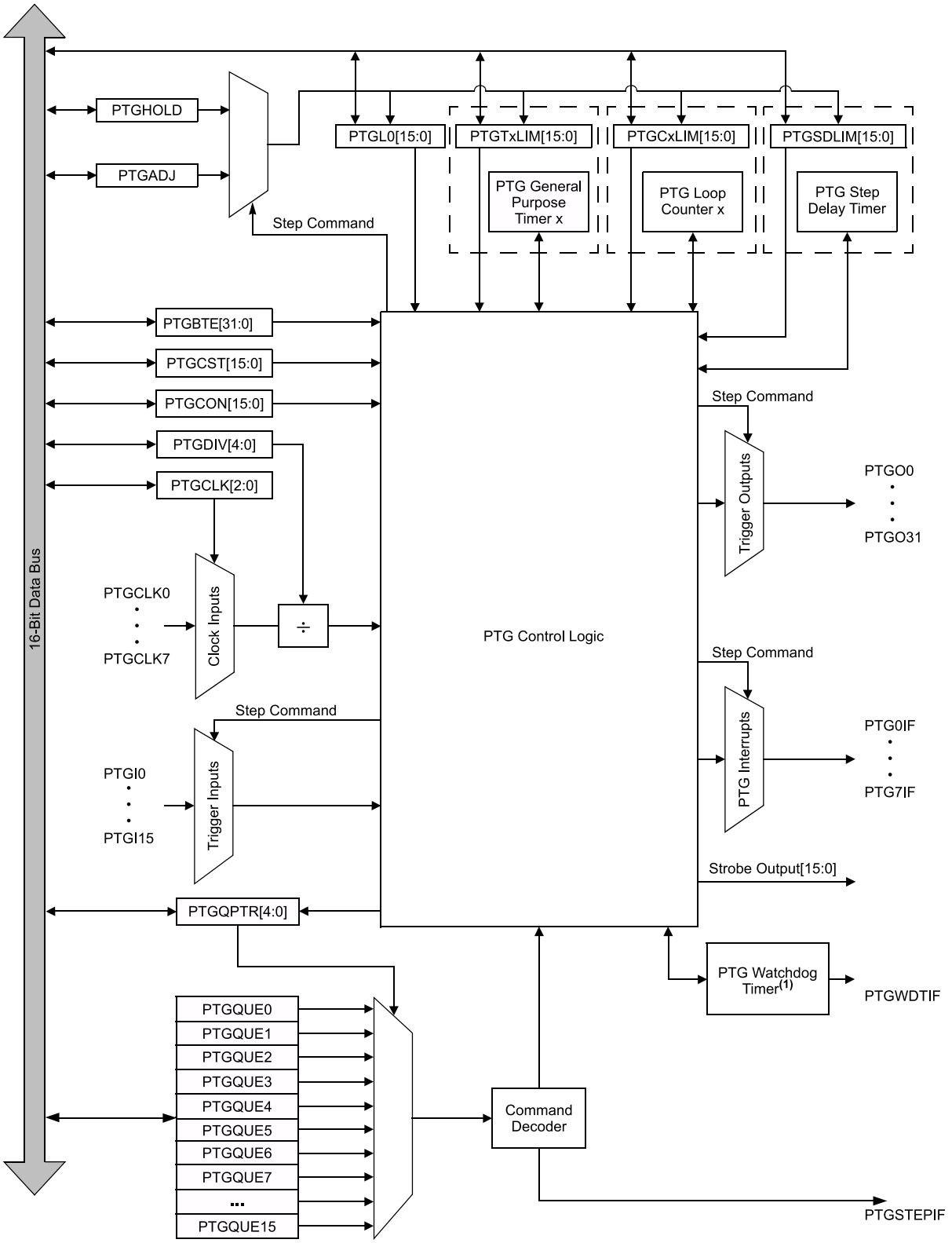
The dsPIC33CDVL256MC506 family Peripheral Trigger Generator (PTG) module is a user-programmable sequencer that is capable of generating complex trigger signal sequences to coordinate the operation of other peripherals. The PTG module is designed to interface with the modules, such as an Analog-to-Digital Converter (ADC), output compare and PWM modules, timers and interrupt controllers.

25.1. Features

- Behavior is Step Command Driven:
  - Step commands are eight bits wide
- Commands are Stored in a Step Queue:
  - Queue depth is up to 32 entries
  - Programmable Step execution time (Step delay)
- Supports the Command Sequence Loop:
  - Can be nested one-level deep
  - Conditional or unconditional loop
  - Two 16-bit loop counters
- 15 Hardware Input Triggers:
  - Sensitive to either positive or negative edges, or a high or low level
- One Software Input Trigger
- Generates Up to 32 Unique Output Trigger Signals
- Generates Two Types of Trigger Outputs:
  - Individual
  - Broadcast
- Strobed Output Port for Literal Data Values:
  - 5-bit literal write (literal part of a command)
  - 16-bit literal write (literal held in the PTGL0 register)
- Generates up to Ten Unique Interrupt Signals
- Two 16-Bit General Purpose Timers
- Flexible Self-Contained Watchdog Timer (WDT) to Set an Upper Limit to Trigger Wait Time
- Single-Step Command Capability in Debug Mode
- Selectable Clock (System, Pulse-Width Modulator (PWM) or ADC)
- Programmable Clock Divider

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Figure 25-1. PTG Block Diagram



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Notes:

1. Dedicated Watchdog Timer for the PTG module, independent of the device Watchdog Timer.
2. Some devices support only PTGBTE[15:0] (16 outputs).

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25.2. PTG Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0900	PTGCST	15:8	PTGEN		PTGSIDL	PTGTOGL		PTGSWT	PTGSSEN	PTGIVIS
		7:0	PTGSTRT	PTGWTO	PTGBUSY				PTGITM[1:0]	
0x0902	PTGCON	15:8	PTGCLK[2:0]					PTGDIV[4:0]		
		7:0	PTGPWD[3:0]					PTGWDT[2:0]		
0x0904	PTGBTEL	15:8	PTGBTE[15:8]							
		7:0	PTGBTE[7:0]							
0x0906	PTGBTEH	15:8	PTGBTE[31:24]							
		7:0	PTGBTE[23:16]							
0x0908	PTGHOLD	15:8	PTGHOLD[15:8]							
		7:0	PTGHOLD[7:0]							
0x090A ... 0x090B	Reserved									
0x090C	PTGT0LIM	15:8	PTGT0LIM[15:8]							
		7:0	PTGT0LIM[7:0]							
0x090E ... 0x090F	Reserved									
0x0910	PTGT1LIM	15:8	PTGT1LIM[15:8]							
		7:0	PTGT1LIM[7:0]							
0x0912 ... 0x0913	Reserved									
0x0914	PTGSDLIM	15:8	PTGSDLIM[15:8]							
		7:0	PTGSDLIM[7:0]							
0x0916 ... 0x0917	Reserved									
0x0918	PTGC0LIM	15:8	PTGC0LIM[15:8]							
		7:0	PTGC0LIM[7:0]							
0x091A ... 0x091B	Reserved									
0x091C	PTGC1LIM	15:8	PTGC1LIM[15:8]							
		7:0	PTGC1LIM[7:0]							
0x091E ... 0x091F	Reserved									
0x0920	PTGADJ	15:8	PTGADJ[15:8]							
		7:0	PTGADJ[7:0]							
0x0922 ... 0x0923	Reserved									
0x0924	PTGL0	15:8	PTGL0[15:8]							
		7:0	PTGL0[7:0]							
0x0926 ... 0x0927	Reserved									
0x0928	PTGQPTR	15:8								
		7:0				PTGQPTR[4:0]				
0x092A ... 0x092F	Reserved									
0x0930	PTGQUE0	15:8	STEP1[7:0]							
		7:0	STEP0[7:0]							
0x0932	PTGQUE1	15:8	STEP3[7:0]							
		7:0	STEP2[7:0]							
0x0934	PTGQUE2	15:8	STEP5[7:0]							
		7:0	STEP4[7:0]							

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PTG Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0936	PTGQUE3	15:8	STEP7[7:0]							
		7:0	STEP6[7:0]							
0x0938	PTGQUE4	15:8	STEP9[7:0]							
		7:0	STEP8[7:0]							
0x093A	PTGQUE5	15:8	STEP11[7:0]							
		7:0	STEP10[7:0]							
0x093C	PTGQUE6	15:8	STEP13[7:0]							
		7:0	STEP12[7:0]							
0x093E	PTGQUE7	15:8	STEP15[7:0]							
		7:0	STEP14[7:0]							
0x0940	PTGQUE8	15:8	STEP17[7:0]							
		7:0	STEP16[7:0]							
0x0942	PTGQUE9	15:8	STEP19[7:0]							
		7:0	STEP18[7:0]							
0x0944	PTGQUE10	15:8	STEP21[7:0]							
		7:0	STEP20[7:0]							
0x0946	PTGQUE11	15:8	STEP23[7:0]							
		7:0	STEP22[7:0]							
0x0948	PTGQUE12	15:8	STEP25[7:0]							
		7:0	STEP24[7:0]							
0x094A	PTGQUE13	15:8	STEP27[7:0]							
		7:0	STEP26[7:0]							
0x094C	PTGQUE14	15:8	STEP29[7:0]							
		7:0	STEP28[7:0]							
0x094E	PTGQUE15	15:8	STEP31[7:0]							
		7:0	STEP30[7:0]							

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25.2.1. PTG Control/Status Low Register

Name: PTGCST
Offset: 0x900

Notes:
1. These bits apply to the PTGWHI and PTGWLO commands only.
2. This bit is only used with the PTGCTRL Step command software trigger option.
3. The PTGSSEN bit may only be written when in Debug mode.

Bit	15	14	13	12	11	10	9	8
	PTGEN		PTGSIDL	PTGTOGL		PTGSWT	PTGSSEN	PTGIVIS
Access	R/W		R/W	R/W		R/W	R/W	R/W
Reset	0		0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	PTGSTRT	PTGWTO	PTGBUSY				PTGITM[1:0]	
Access	R/W	R/W	R/W				R/W	R/W
Reset	0	0	0				0	0

Bit 15 – PTGEN PTG Broadcast Trigger Enable bit

Value	Description
1	PTG is enabled.
0	PTG is disabled.

Bit 13 – PTGSIDL PTG Freeze in Debug Mode bit

Value	Description
1	Halts PTG operation when device is Idle.
0	PTG operation continues when device is Idle.

Bit 12 – PTGTOGL PTG Toggle Trigger Output bit

Value	Description
1	Toggles state of TRIG output for each execution of PTGTRIG.
0	Generates a single TRIG pulse for each execution of PTGTRIG.

Bit 10 – PTGSWT PTG Software Trigger bit(2)

Value	Description
1	If the PTG state machine is executing the “Wait for software trigger” Step command (OPTION[3:0] = 1010 or 1011), the command will complete and execution will continue.
0	No action other than to clear the bit.

Bit 9 – PTGSSEN PTG Single-Step Command bit(3)

Value	Description
1	Enables single Step when in Debug mode .
0	Disables single step.

Bit 8 – PTGIVIS PTG Counter/Timer Visibility bit

Value	Description
1	Reading the PTGSDLIM, PTGCxLIM or PTGTxLIM registers returns the current values of their corresponding Counter/Timer registers (PTGSDLIM, PTGCxLIM and PTGTxLIM).

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Value	Description
0	Reading the PTGSDLIM, PTGCxLIM or PTGTxLIM registers returns the value of these Limit registers.

Bit 7 – PTGSTRT PTG Start Sequencer bit

Value	Description
1	Starts to sequentially execute the commands (Continuous mode).
0	Stops executing the commands .

Bit 6 – PTGWTO PTG Watchdog Timer Time-out Status bit

Value	Description
1	PTG Watchdog Timer has timed out.
0	PTG Watchdog Timer has not timed out.

Bit 5 – PTGBUSY PTG State Machine Busy bit

Value	Description
1	PTG is running on the selected clock source; no SFR writes are allowed to PTGCLK[2:0] or PTGDIV[4:0].
0	PTG state machine is not running.

Bits 1:0 – PTGITM[1:0] PTG Input Trigger Operation Selection bits(1)

Value	Description
11	Single-level detect with Step delay not executed on exit of command (regardless of the PTGCTRL command) (Mode 3).
10	Single-level detect with Step delay executed on exit of command (Mode 2).
01	Continuous edge detect with Step delay not executed on exit of command (regardless of the PTGCTRL command) (Mode 1).
00	Continuous edge detect with Step delay executed on exit of command (Mode 0).

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25.2.2. PTG Control/Status Register

Name: PTGCON
Offset: 0x902

Bit	15	14	13	12	11	10	9	8
	PTGCLK[2:0]			PTGDIV[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTGPWD[3:0]					PTGWDT[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bits 15:13 – PTGCLK[2:0] PTG Module Clock Source Selection bits

Value	Description
111	CLC1 output
110	$F_{VCO}/4$
101	Reserved
100	Reserved
011	Input from Timer1 Clock pin, T1CK
010	ADC clock
001	F_{OSC}
000	F_P

Bits 12:8 – PTGDIV[4:0] PTG Module Clock Prescaler (Divider) bits

Value	Description
11111	Divide-by-32
11110	Divide-by-31
. . .	
00001	Divide-by-2
00000	Divide-by-1

Bits 7:4 – PTGPWD[3:0] PTG Trigger Output Pulse-Width (in PTG clock cycles) bits

Value	Description
1111	All trigger outputs are 16 PTG clock cycles wide.
1110	All trigger outputs are 15 PTG clock cycles wide.
. . .	
0001	All trigger outputs are 2 PTG clock cycles wide.
0000	All trigger outputs are 1 PTG clock cycle wide.

Bits 2:0 – PTGWDT[2:0] PTG Watchdog Timer Time-out Selection bits

Value	Description
111	Watchdog Timer will time out after 512 PTG clocks.
110	Watchdog Timer will time out after 256 PTG clocks.
101	Watchdog Timer will time out after 128 PTG clocks.
100	Watchdog Timer will time out after 64 PTG clocks.
011	Watchdog Timer will time out after 32 PTG clocks.
010	Watchdog Timer will time out after 16 PTG clocks.
001	Watchdog Timer will time out after 8 PTG clocks.

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Value	Description
000	Watchdog Timer is disabled.

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25.2.3. PTG Broadcast Trigger Enable Low Register

Name: PTGBTEL
Offset: 0x904

Bit	15	14	13	12	11	10	9	8
	PTGBTE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTGBTE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PTGBTE[15:0] PTG Broadcast Trigger Enable bits

Value	Description
1	Generates trigger when the broadcast command is executed.
0	Does not generate trigger when the broadcast command is executed.

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25.2.4. PTG Broadcast Trigger Enable Low Register

Name: PTGBTEH
Offset: 0x906

Bit	15	14	13	12	11	10	9	8
	PTGBTE[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTGBTE[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PTGBTE[31:16] PTG Broadcast Trigger Enable bits

Value	Description
1	Generates trigger when the broadcast command is executed.
0	Does not generate trigger when the broadcast command is executed.

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25.2.5. PTG Hold Register

Name: PTGHOLD
Offset: 0x908

Bit	15	14	13	12	11	10	9	8
	PTGHOLD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTGHOLD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PTGHOLD[15:0] PTG General Purpose Hold Register bits
This register holds the user-supplied data to be copied to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 register using the `PTGCOPY` command.

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25.2.6. PTG Timer0 Limit Register

Name: PTGT0LIM
Offset: 0x90C

Bit	15	14	13	12	11	10	9	8
	PTGT0LIM[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTGT0LIM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PTGT0LIM[15:0] PTG Timer0 Limit Register bits
General Purpose Timer0 Limit register.

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25.2.7. PTG Timer1 Limit Register

Name: PTGT1LIM
Offset: 0x910

Bit	15	14	13	12	11	10	9	8
	PTGT1LIM[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTGT1LIM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PTGT1LIM[15:0] PTG Timer1 Limit Register bits
General Purpose Timer1 Limit register.

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25.2.8. PTG Step Delay Limit Register

Name: PTGSDLIM
Offset: 0x914

Bit	15	14	13	12	11	10	9	8
	PTGSDLIM[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTGSDLIM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PTGSDLIM[15:0] PTG Step Delay Limit Register bits
This register holds a PTG Step delay value representing the number of additional PTG clocks between the start of a Step command and the completion of a Step command.

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25.2.9. PTG Counter 0 Limit Register

Name: PTGC0LIM
Offset: 0x918

Bit	15	14	13	12	11	10	9	8
	PTGC0LIM[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTGC0LIM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PTGC0LIM[15:0] PTG Counter 0 Limit Register bits
This register is used to specify the loop count for the `PTGJMPC0` Step command or as a Limit register for the General Purpose Counter 0.

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25.2.10. PTG Counter 1 Limit Register

Name: PTGC1LIM
Offset: 0x91C

Bit	15	14	13	12	11	10	9	8
	PTGC1LIM[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTGC1LIM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PTGC1LIM[15:0] PTG Counter 1 Limit Register bits
This register is used to specify the loop count for the `PTGJMPC1` Step command or as a Limit register for the General Purpose Counter 1.

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25.2.11. PTG Adjust Register

Name: PTGADJ
Offset: 0x920

Bit	15	14	13	12	11	10	9	8
	PTGADJ[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTGADJ[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PTGADJ[15:0] PTG Adjust Register bits
This register holds the user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 register using the `PTGADD` command.

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25.2.12. PTG Literal 0 Register

Name: PTGL0
Offset: 0x924

Bit	15	14	13	12	11	10	9	8
	PTGL0[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTGL0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PTGL0[15:0] PTG Literal 0 Register bits
This register holds the 6-bit value to be written to the CNVCHSEL[5:0] bits (ADCON3L[5:0]) with the `PTGCTRL` Step command.

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25.2.13. PTG Step Queue Pointer Register

Name: PTGQPTR
Offset: 0x928

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PTGQPTR[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – PTGQPTR[4:0] PTG Step Queue Pointer Register bits
This register points to the currently active Step command in the Step queue.

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25.2.14. PTG Step Queue 0 Pointer Register

Name: PTGQUE0
Offset: 0x930

Bit	15	14	13	12	11	10	9	8
	STEP1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP1[7:0] PTG Command 2n+1 bits(2)
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP0[7:0] PTG Command 2n bits(2)
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.15. PTG Step Queue 1 Pointer Register

Name: PTGQUE1
Offset: 0x932

Bit	15	14	13	12	11	10	9	8
	STEP3[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP3[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP2[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.16. PTG Step Queue 2 Pointer Register

Name: PTGQUE2
Offset: 0x934

Bit	15	14	13	12	11	10	9	8
	STEP5[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP4[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP5[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP4[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.17. PTG Step Queue 3 Pointer Register

Name: PTGQUE3
Offset: 0x936

Bit	15	14	13	12	11	10	9	8
	STEP7[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP6[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP7[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP6[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.18. PTG Step Queue 4 Pointer Register

Name: PTGQUE4
Offset: 0x938

Bit	15	14	13	12	11	10	9	8
	STEP9[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP8[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP9[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP8[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.19. PTG Step Queue 5 Pointer Register

Name: PTGQUE5
Offset: 0x93A

Bit	15	14	13	12	11	10	9	8
	STEP11[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP10[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP11[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP10[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.20. PTG Step Queue 6 Pointer Register

Name: PTGQUE6
Offset: 0x93C

Bit	15	14	13	12	11	10	9	8
	STEP13[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP12[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP13[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP12[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.21. PTG Step Queue 7 Pointer Register

Name: PTGQUE7
Offset: 0x93E

Bit	15	14	13	12	11	10	9	8
	STEP15[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP14[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP15[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP14[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.22. PTG Step Queue 8 Pointer Register

Name: PTGQUE8
Offset: 0x0940

Bit	15	14	13	12	11	10	9	8
	STEP17[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP16[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP17[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP16[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.23. PTG Step Queue 9 Pointer Register

Name: PTGQUE9
Offset: 0x942

Bit	15	14	13	12	11	10	9	8
	STEP19[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP18[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP19[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP18[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.24. PTG Step Queue 10 Pointer Register

Name: PTGQUE10
Offset: 0x944

Bit	15	14	13	12	11	10	9	8
	STEP21[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP20[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP21[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP20[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.25. PTG Step Queue 11 Pointer Register

Name: PTGQUE11
Offset: 0x946

Bit	15	14	13	12	11	10	9	8
	STEP23[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP22[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP23[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP22[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.26. PTG Step Queue 12 Pointer Register

Name: PTGQUE12
Offset: 0x948

Bit	15	14	13	12	11	10	9	8
	STEP25[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP24[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP25[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP24[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.27. PTG Step Queue 13 Pointer Register

Name: PTGQUE13
Offset: 0x94A

Bit	15	14	13	12	11	10	9	8
	STEP27[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP26[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP27[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP26[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.28. PTG Step Queue 14 Pointer Register

Name: PTGQUE14
Offset: 0x94C

Bit	15	14	13	12	11	10	9	8
	STEP29[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STEP28[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP29[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP28[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

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25.2.29. PTG Step Queue 15 Pointer Register

Name: PTGQUE15
Offset: 0x94E

Bit	15	14	13	12	11	10	9	8
	STEP31[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	STEP30[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – STEP31[7:0] PTG Command 2n+1 bits
A queue location for storage of the STEP(2n+1) command byte, where 'n' is from PTGQUEn.

Bits 7:0 – STEP30[7:0] PTG Command 2n bits
A queue location for storage of the STEP(2n) command byte, where 'n' is the odd numbered Step Queue Pointers.

25.3. PTG Step Commands

Table 25-1. PTG Step Command Format and Description

Step Command Byte							
STEPx[7:0]							
CMD[3:0]				OPTION[3:0]			
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Step Command	CMD[3:0]	Command Description
PTGCTRL	0000	Execute the control command as described by the OPTION[3:0] bits.
PTGADD	0001	Add contents of the PTGADJ register to the target register as described by the OPTION[3:0] bits.
PTGCOPY		Copy contents of the PTGHOLD register to the target register as described by the OPTION[3:0] bits.
PTGSTRB	001x	Copy the values contained in the bits, CMD[0]:OPTION[3:0], to the strobe output bits[4:0].
PTGWHI	0100	Wait for a low-to-high edge input from a selected PTG trigger input as described by the OPTION[3:0] bits.
PTGWLO	0101	Wait for a high-to-low edge input from a selected PTG trigger input as described by the OPTION[3:0] bits.
—	0110	Reserved; do not use.(1)
PTGIRQ	0111	Generate individual interrupt request as described by the OPTION[3:0] bits.
PTGTRIG	100x	Generate individual trigger output as described by the bits, CMD[0]:OPTION[3:0].
PTGJMP	101x	Copy the values contained in the bits, CMD[0]:OPTION[3:0], to the PTGQPTR register and jump to that Step queue.
PTGJMPC0	110x	PTGC0 = PTGC0LIM: Increment the PTGQPTR register.
		PTGC0 ≠ PTGC0LIM: Increment Counter 0 (PTGC0) and copy the values contained in the bits, CMD[0]:OPTION[3:0] to the PTGQPTR register, and jump to that Step queue.

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PTG Step Commands (continued)		
Step Command	**CMD[3:0]**	**Command Description**
PTGJMPC1	111x	PTGC1 = PTGC1LIM: Increment the PTGQPTR register.
		PTGC1 ≠ PTGC1LIM: Increment Counter 1 (PTGC1) and copy the values contained in the bits, CMD[0]:OPTION[3:0], to the PTGQPTR register, and jump to that Step queue.

Notes:

1. In general, reserved commands or options will execute, but they do not have any effect (i.e., execute as a NOP instruction).
2. Reserved options must not be used with the PTGWHI/PTGWLO commands.

Table 25-2. PTG Command Options

Step Command	OPTION[3:0]	Command Description
PTGCTRL(1)	0000	NOP.
	0001	Reserved; do not use.
	0010	Disable Step delay timer (PTGSD).
	0011	Reserved; do not use.
	0100	Reserved; do not use.
	0101	Reserved; do not use.
	0110	Enable Step delay timer (PTGSD).
	0111	Reserved; do not use.
	1000	Start and wait for the PTG Timer0 to match the PTGT0LIM register.
	1001	Start and wait for the PTG Timer1 to match the PTGT1LIM register.
	1010	Wait for the software trigger (level, PTGSWT = 1).
	1011	Wait for the software trigger (positive edge, PTGSWT = 0 to 1).
	1100	Copy the PTGC0LIM register contents to the strobe output.
	1101	Copy the PTGC1LIM register contents to the strobe output.
	1110	Copy the PTGL0 register contents to the strobe output.
	1111	Generate the triggers indicated in the PTGBTE register.
PTGADD(1)	0000	Add the PTGADJ register contents to the PTGC0LIM register.
	0001	Add the PTGADJ register contents to the PTGC1LIM register.
	0010	Add the PTGADJ register contents to the PTGT0LIM register.
	0011	Add the PTGADJ register contents to the PTGT1LIM register.
	0100	Add the PTGADJ register contents to the PTGSDLIM register.
	0101	Add the PTGADJ register contents to the PTGL0 register.
	0110	Reserved; do not use.
	0111	Reserved; do not use.
PTGCOPY(1)	1000	Copy the PTGHOLD register contents to the PTGC0LIM register.
	1001	Copy the PTGHOLD register contents to the PTGC1LIM register.
	1010	Copy the PTGHOLD register contents to the PTGT0LIM register.
	1011	Copy the PTGHOLD register contents to the PTGT1LIM register.
	1100	Copy the PTGHOLD register contents to the PTGSDLIM register.
	1101	Copy the PTGHOLD register contents to the PTGL0 register.
	1110	Reserved; do not use.
	1111	Reserved; do not use.

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Table 25-2. PTG Command Options (continued)

Step Command	OPTION[3:0]	Command Description
PTGWHI[1] or PTGWLO[1]	0000	PTGI0 (see Table 25-3 for input assignments).
	•••	•••
	1111	PTGI15 (see Table 25-3 for input assignments).
PTGIRQ[1]	0000	Generate PTG Interrupt 0.
	•••	•••
	0111	Generate PTG Interrupt 7.
	1000	Reserved; do not use.
	•••	•••
	1111	Reserved; do not use.
PTGTRIG	0000	PTGO0 (see Table 25-4 for input assignments).
	0001	PTGO1 (see Table 25-4 for input assignments).
	•••	•••
	1110	PTGO30 (see Table 25-4 for input assignments).
	1111	PTGO31 (see Table 25-4 for input assignments).

Note:

1. All reserved commands or options will execute, but they do not have any affect (i.e., execute as a NOP instruction).

Table 25-3. PTG Input Descriptions

PTG Input Number	PTG Input Description
PTGI 0	Trigger Input from PWM1 ADC Trigger 2
PTGI 1	Trigger Input from PWM2 ADC Trigger 2
PTGI 2	Trigger Input from PWM3 ADC Trigger 2
PTGI 3	Trigger Input from PWM4 ADC Trigger 2
PTGI 4-6	Reserved
PTGI 7	Trigger Input from SCCP4
PTGI 8	Reserved
PTGI 9	Trigger Input from Comparator 1
PTGI 10	Trigger Input from Comparator 2
PTGI 11	Reserved
PTGI 12	Trigger Input from CLC1
PTGI 13	Trigger Input ADC Done Group Interrupt
PTGI 14	Reserved
PTGI 15	Trigger Input from INT2 PPS

Table 25-4. PTG Output Descriptions

PTG Output Number	PTG Output Description
PTGO0 to PTGO11	Reserved
PTGO12	ADC TRGSRC[30]
PTGO13 to PTGO23	Reserved
PTGO24	PPS Output RP46
PTGO25	PPS Output RP47
PTGO26	PPS Input RP6
PTGO27	PPS Input RP7
PTGO28 to PTGO31	Reserved

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Note: On the dsPIC33CDVL256MC506 family of devices, the PTG strobe output may request the conversion of an ADC channel indicated by the strobed data. This functionality is enabled by setting PTGEN (ADCON2L[11]) to 1 in the ADC control registers, and operates similarly to using CNVCHSEL (ADCON3L[5:0]) and CNVRTCH (ADCON3L[8]) to select and convert a channel. The difference is that effectively, upon each strobe output, CNVCHSEL is written with the strobed data and CNVRTCH is automatically asserted to request the conversion immediately. The regular functionality of CNVCHSEL and CNVRTCH is not available when PTGEN = 1.

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26. 32-Bit Programmable Cyclic Redundancy Check (CRC) Generator

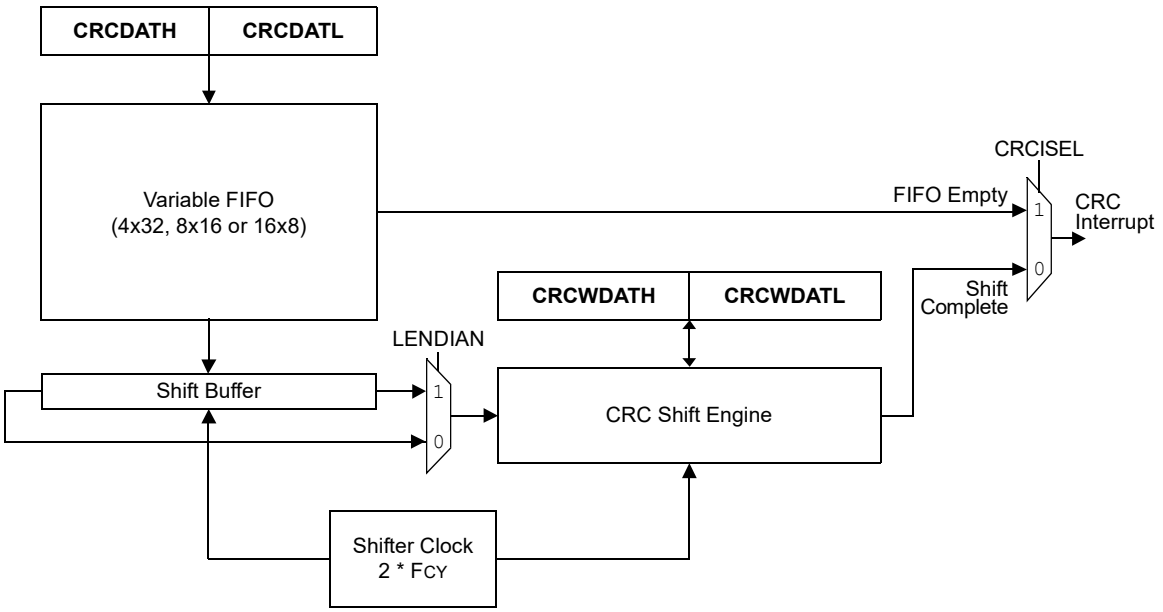
Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. For more information, refer to **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (www.microchip.com/ DS30009729) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, Up to 32 Bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

A simple version of the CRC shift engine is displayed in Figure 26-1.

Figure 26-1. CRC Module Block Diagram



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26.1. CRC Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xB0	CRCCONL	15:8	CRCEN		CSIDL	VWORD[4:0]				
		7:0	CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	MOD		
0xB2	CRCCONH	15:8				DWIDTH[4:0]				
		7:0				PLEN[4:0]				
0xB4	CRCXORL	15:8	X[14:7]							
		7:0	X[6:0]							
0xB6	CRCXORH	15:8	X[31:24]							
		7:0	X[23:16]							
0xB8	CRCDATL	15:8	CRCDAT[15:8]							
		7:0	CRCDAT[7:0]							
0xBA	CRCDATH	15:8	CRCDAT[31:24]							
		7:0	CRCDAT[23:16]							
0xBC	CRCWDATL	15:8	CRCWDAT[15:8]							
		7:0	CRCWDAT[7:0]							
0xBE	CRCWDATH	15:8	CRCWDAT[31:24]							
		7:0	CRCWDAT[23:16]							

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26.1.1. CRC Control Register Low

Name: CRCCONL
Offset: 0x0B0

Legend: HSC = Hardware Settable/Clearable bit; HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
	CRCEN		CSIDL	VWORD[4:0]				
Access	R/W		R/W	HSC/R	HSC/R	HSC/R	HSC/R	HSC/R
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	MOD		
Access	HSC/R	HSC/R	R/W	HC/R/W	R/W	R/W		
Reset	0	1	0	0	0	0		

Bit 15 – CRCEN CRC Enable bit

Value	Description
1	Enables module.
0	Disables module.

Bit 13 – CSIDL CRC Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode.
0	Continues module operation in Idle mode.

Bits 12:8 – VWORD[4:0] Pointer Value bits
Indicates the number of valid words in the FIFO. Has a maximum value of 8 when PLEN[4:0] ≥ 7 or 16 when PLEN[4:0] ≤ 7.

Bit 7 – CRCFUL CRC FIFO Full bit

Value	Description
1	FIFO is full.
0	FIFO is not full.

Bit 6 – CRCMPT CRC FIFO Empty bit

Value	Description
1	FIFO is empty.
0	FIFO is not empty.

Bit 5 – CRCISEL CRC Interrupt Selection bit

Value	Description
1	Interrupt on FIFO is empty; the final word of data is still shifting through the CRC.
0	Interrupt on shift is complete and results are ready.

Bit 4 – CRCGO CRC Start bit

Value	Description
1	Starts CRC serial shifter.
0	CRC serial shifter is turned off.

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Bit 3 – LENDIAN Data Shift Direction Select bit

Value	Description
1	Data word is shifted into the FIFO, starting with the LSb (little-endian).
0	Data word is shifted into the FIFO, starting with the MSb (big-endian).

Bit 2 – MOD CRC Calculation Mode bit

Value	Description
1	Alternate mode
0	Legacy mode bit

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26.1.2. CRC Control Register High

Name: CRCCONH
Offset: 0x0B2

Bit	15	14	13	12	11	10	9	8
				DWIDTH[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				PLEN[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – DWIDTH[4:0] Data Word Width Configuration bits
Configures the width of the data word (Data Word Width – 1).

Bits 4:0 – PLEN[4:0] Polynomial Length Configuration bits
Configures the length of the polynomial (Polynomial Length – 1).

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26.1.3. CRC XOR Polynomial Register, Low Byte

Name: CRCXORL
Offset: 0x0B4

Bit	15	14	13	12	11	10	9	8
	X[14:7]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	X[6:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bits 15:8 – X[14:7] XOR of Polynomial Term x^n Enable bits

Bits 7:1 – X[6:0] XOR of Polynomial Term x^n Enable bits

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26.1.4. CRC XOR Polynomial Register, High Byte

Name: CRCXORH
Offset: 0x0B6

Bit	15	14	13	12	11	10	9	8
	X[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	X[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – X[31:16] XOR of Polynomial Term x^n Enable bits

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26.1.5. CRC Data Register Low

Name: CRCDATL
Offset: 0x0B8

Bit	15	14	13	12	11	10	9	8
	CRCDAT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CRCDAT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CRCDAT[15:0] CRC Data Low bits

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26.1.6. CRC Data Register High

Name: CRCDATH
Offset: 0x0BA

Bit	15	14	13	12	11	10	9	8
	CRCDAT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CRCDAT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CRCDAT[31:16] CRC Data High bits

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26.1.7. CRC Result Register Low

Name: CRCWDATL
Offset: 0x0BC

Bit	15	14	13	12	11	10	9	8
	CRCWDAT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CRCWDAT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CRCWDAT[15:0] CRC Result Low bits

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26.1.8. CRC Result Register High

Name: CRCWDATH
Offset: 0x0BE

Bit	15	14	13	12	11	10	9	8
	CRCWDAT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CRCWDAT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CRCWDAT[31:16] CRC Result High bits

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27. Current Bias Generator (CBG)

Notes:

1. This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Current Bias Generator (CBG)"** (www.microchip.com/DS70005253) in the *"dsPIC33/PIC24 Family Reference Manual"*.
2. Some registers and associated bits described in this section may not be available on all devices. Refer to Memory Organization in this data sheet for device-specific register and bit information.

The Current Bias Generator (CBG) consists of two classes of current sources: 10 µA and 50 µA sources. The major features of each current source are:

- 10 µA Current Sources:
  - Current sourcing only
  - Up to four independent sources
- 50 µA Current Sources:
  - Selectable current sourcing or sinking
  - Selectable current mirroring for sourcing and sinking

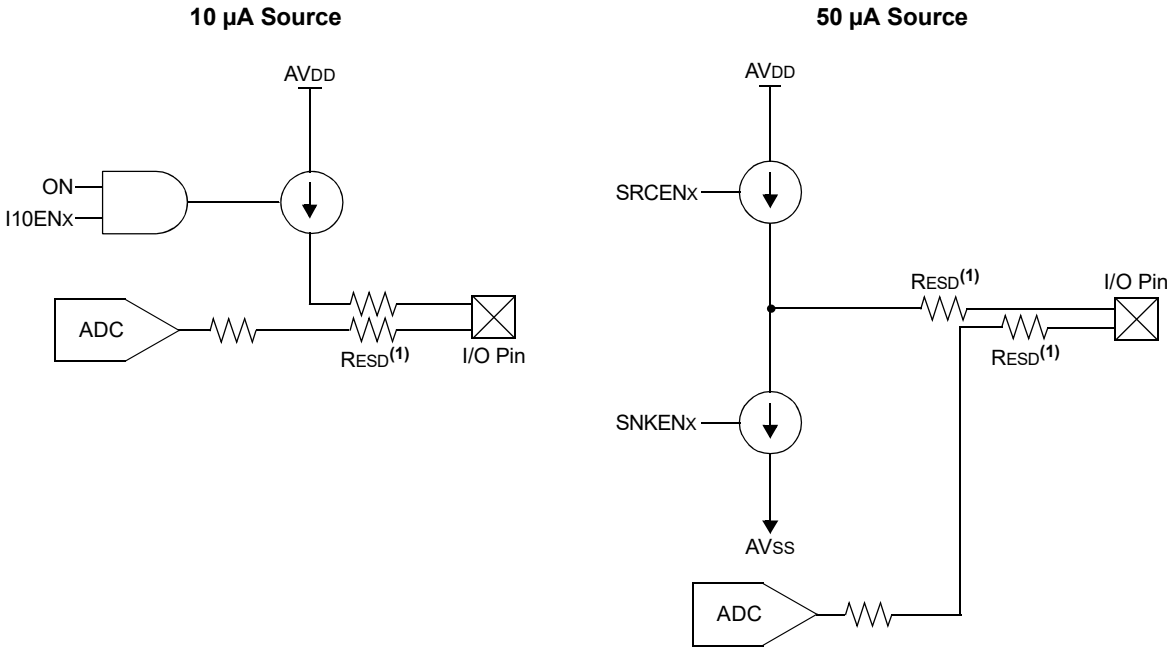
Table 27-1. CBG Channel Availability

Package Type	ISRCx	IBIASx
64-pin	0, 1, 2, 3	0, 1, 2, 3

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A simplified block diagram of the CBG module is shown in Figure 27-1.

Figure 27-1. Constant-Current Source Module Block Diagram[2]



Notes:

1. R_{ESD} is typically 350 Ohms.
2. The ADC analog input is shown only for clarity. Each analog peripheral connected to the pin has a separate Electrostatic Discharge (ESD) resistor.

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27.1. Current Bias Generator Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x08F0	BIASCON	15:8	ON							
		7:0					I10EN3	I10EN2	I10EN1	I10EN0
0x08F2 ... 0x08F3	Reserved									
0x08F4	IBIASCON0L	15:8			SHRSRCEN1	SHRSNKEN1	GENSRCEN1	GENSNKEN1	SRCEN1	SNKEN1
		7:0			SHRSRCEN0	SHRSNKEN0	GENSRCEN0	GENSNKEN0	SRCEN0	SNKEN0
0x08F6	IBIASCON0H	15:8			SHRSRCEN3	SHRSNKEN3	GENSRCEN3	GENSNKEN3	SRCEN3	SNKEN3
		7:0			SHRSRCEN2	SHRSNKEN2	GENSRCEN2	GENSNKEN2	SRCEN2	SNKEN2

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27.1.1. Current Bias Generator Control Register

Name: BIASCON
Offset: 0x8F0

Bit	15	14	13	12	11	10	9	8
	ON							
Access	R/W							
Reset	0							

Bit	7	6	5	4	3	2	1	0
					I10EN3	I10EN2	I10EN1	I10EN0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – ON Current Bias Module Enable bit

Value	Description
1	Module is enabled
0	Module is disabled

Bit 3 – I10EN3 10 µA Enable for Output 3 bit

Value	Description
1	10 µA output is enabled
0	10 µA output is disabled

Bit 2 – I10EN2 10 µA Enable for Output 2 bit

Value	Description
1	10 µA output is enabled
0	10 µA output is disabled

Bit 1 – I10EN1 10 µA Enable for Output 1 bit

Value	Description
1	10 µA output is enabled
0	10 µA output is disabled

Bit 0 – I10EN0 10 µA Enable for Output 0 bit

Value	Description
1	10 µA output is enabled
0	10 µA output is disabled

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27.1.2. Current Bias Generator 50 µA Current Source Control Low Register

Name: IBIASCON0L
Offset: 0x8F4

Bit	15	14	13	12	11	10	9	8
			SHRSRCEN1	SHRSNKEN1	GENSRCEN1	GENSNKEN1	SRCEN1	SNKEN1
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			SHRSRCEN0	SHRSNKEN0	GENSRCEN0	GENSNKEN0	SRCEN0	SNKEN0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 13 – SHRSRCEN1 Share Source Enable for Output #1 bit

Value	Description
1	Sourcing Current Mirror mode is enabled (uses reference from another source)
0	Sourcing Current Mirror mode is disabled

Bit 12 – SHRSNKEN1 Share Sink Enable for Output #1 bit

Value	Description
1	Sinking Current Mirror mode is enabled (uses reference from another source)
0	Sinking Current Mirror mode is disabled

Bit 11 – GENSRCEN1 Generated Source Enable for Output #1 bit

Value	Description
1	Source generates the current source mirror reference
0	Source does not generate the current source mirror reference

Bit 10 – GENSNKEN1 Generated Sink Enable for Output #1 bit

Value	Description
1	Source generates the current sink mirror reference
0	Source does not generate the current sink mirror reference

Bit 9 – SRCEN1 Source Enable for Output #1 bit

Value	Description
1	Current source is enabled
0	Current source is disabled

Bit 8 – SNKEN1 Sink Enable for Output #1 bit

Value	Description
1	Current sink is enabled
0	Current sink is disabled

Bit 5 – SHRSRCEN0 Share Source Enable for Output #0 bit

Value	Description
1	Sourcing Current Mirror mode is enabled (uses reference from another source)
0	Sourcing Current Mirror mode is disabled

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Bit 4 – SHRSNKEN0 Share Sink Enable for Output #0 bit

Value	Description
1	Sinking Current Mirror mode is enabled (uses reference from another source)
0	Sinking Current Mirror mode is disabled

Bit 3 – GENSRCEN0 Generated Source Enable for Output #0 bit

Value	Description
1	Source generates the current source mirror reference
0	Source does not generate the current source mirror reference

Bit 2 – GENSNKEN0 Generated Sink Enable for Output #0 bit

Value	Description
1	Source generates the current sink mirror reference
0	Source does not generate the current sink mirror reference

Bit 1 – SRCEN0 Source Enable for Output #0 bit

Value	Description
1	Current source is enabled
0	Current source is disabled

Bit 0 – SNKEN0 Sink Enable for Output #0 bit

Value	Description
1	Current sink is enabled
0	Current sink is disabled

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27.1.3. Current Bias Generator 50 µA Current Source Control High Register

Name: IBIASCON0H
Offset: 0x8F6

Bit	15	14	13	12	11	10	9	8
			SHRSRCEN3	SHRSNKEN3	GENSRCEN3	GENSNKEN3	SRCEN3	SNKEN3
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			SHRSRCEN2	SHRSNKEN2	GENSRCEN2	GENSNKEN2	SRCEN2	SNKEN2
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 13 – SHRSRCEN3 Share Source Enable for Output #3 bit

Value	Description
1	Sourcing Current Mirror mode is enabled (uses reference from another source)
0	Sourcing Current Mirror mode is disabled

Bit 12 – SHRSNKEN3 Share Sink Enable for Output #3 bit

Value	Description
1	Sinking Current Mirror mode is enabled (uses reference from another source)
0	Sinking Current Mirror mode is disabled

Bit 11 – GENSRCEN3 Generated Source Enable for Output #3 bit

Value	Description
1	Source generates the current source mirror reference
0	Source does not generate the source source mirror reference

Bit 10 – GENSNKEN3 Generated Sink Enable for Output #3 bit

Value	Description
1	Source generates the current sink mirror reference
0	Source does not generate the current sink mirror reference

Bit 9 – SRCEN3 Source Enable for Output #3 bit

Value	Description
1	Current source is enabled
0	Current source is disabled

Bit 8 – SNKEN3 Sink Enable for Output #3 bit

Value	Description
1	Current sink is enabled
0	Current sink is disabled

Bit 5 – SHRSRCEN2 Share Source Enable for Output #2 bit

Value	Description
1	Sourcing Current Mirror mode is enabled (uses reference from another source)
0	Sourcing Current Mirror mode is disabled

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Bit 4 – SHRSNKEN2 Share Sink Enable for Output #2 bit

Value	Description
1	Sinking Current Mirror mode is enabled (uses reference from another source)
0	Sinking Current Mirror mode is disabled

Bit 3 – GENSRCEN2 Generated Source Enable for Output #2 bit

Value	Description
1	Source generates the current source mirror reference
0	Source does not generate the current source mirror reference

Bit 2 – GENSNKEN2 Generated Sink Enable for Output #2 bit

Value	Description
1	Source generates the current sink mirror reference
0	Source does not generate the current sink mirror reference

Bit 1 – SRCEN2 Source Enable for Output #2 bit

Value	Description
1	Current source is enabled
0	Current source is disabled

Bit 0 – SNKEN2 Sink Enable for Output #2 bit

Value	Description
1	Current sink is enabled
0	Current sink is disabled

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28. Operational Amplifier

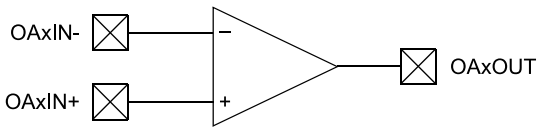
Note: Some device variants support only two op amp instances. Refer to Table 1 and Table 28-1 for availability.

Table 28-1. Op Amp Availability

Package Type	Op Amps
28-pin	1, 2
36-pin	1, 2, 3
48-pin	1, 2, 3
64-pin	1, 2, 3

The dsPIC33CDVL256MC506 family implements three instances of operational amplifiers (op amps). The op amps can be used for a wide variety of purposes, including signal conditioning and filtering. The three op amps are functionally identical. The block diagram for a single amplifier is shown in Figure 28-1 .

Figure 28-1. Single Operational Amplifier Block Diagram



The op amps are controlled by two SFR registers: AMPCON1L and AMPCON1H. They remain in a Low-Power state until the AMPON bit is set. Each op amp can then be enabled independently by setting the corresponding AMPENx bit (x = 1, 2, 3).

The NCHDISx bit provides some flexibility regarding input range versus Integral Nonlinearity (INL). When NCHDISx = 0 (default), the op amps have a wider input voltage range (see AC Characteristics and Timing Parameters). When NCHDISx = 1, the wider input range is traded for improved INL performance (lower INL).

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28.1. Operational Amplifier Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x08DC	AMPCON1L	15:8	AMPON							
		7:0						AMPEN3	AMPEN2	AMPEN1
0x08DE	AMPCON1H	15:8								
		7:0						NCHDIS3	NCHDIS2	NCHDIS1

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28.1.1. Op Amp Control Register Low

Name: AMPCON1L
Offset: 0x8DC

Bit	15	14	13	12	11	10	9	8
	AMPON							
Access	R/W							
Reset	0							

Bit	7	6	5	4	3	2	1	0
						AMPEN3	AMPEN2	AMPEN1
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 15 – AMPON Op Amp Enable/On bit

Value	Description
1	Enables op amp modules if their respective AMPENx bits are also asserted
0	Disables all op amp modules

Bit 2 – AMPEN3 Op Amp #3 Enable bit

Value	Description
1	Enables Op Amp #3 if the AMPON bit is also asserted
0	Disables Op Amp #3

Bit 1 – AMPEN2 Op Amp #2 Enable bit

Value	Description
1	Enables Op Amp #2 if the AMPON bit is also asserted
0	Disables Op Amp #2

Bit 0 – AMPEN1 Op Amp #1 Enable bit

Value	Description
1	Enables Op Amp #1 if the AMPON bit is also asserted
0	Disables Op Amp #1

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28.1.2. Op Amp Control Register High

Name: AMPCON1H
Offset: 0x8DE

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						NCHDIS3	NCHDIS2	NCHDIS1
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – NCHDIS3 Op Amp #3 N Channel Disable bit

Value	Description
1	Disables Op Amp #3 N channels input stage; reduced INL, but lowered input voltage range
0	Wide input range for Op Amp #3

Bit 1 – NCHDIS2 Op Amp #2 N Channel Disable bit

Value	Description
1	Disables Op Amp #2 N channels input stage; reduced INL, but lowered input voltage range
0	Wide input range for Op Amp #2

Bit 0 – NCHDIS1 Op Amp #1 N Channel Disable bit

Value	Description
1	Disables Op Amp #1 N channels input stage; reduced INL, but lowered input voltage range
0	Wide input range for Op Amp #1

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29. Deadman Timer (DMT)

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Deadman Timer (DMT)"** (www.microchip.com/DS70005155) in the *"dsPIC33/PIC24 Family Reference Manual"*.

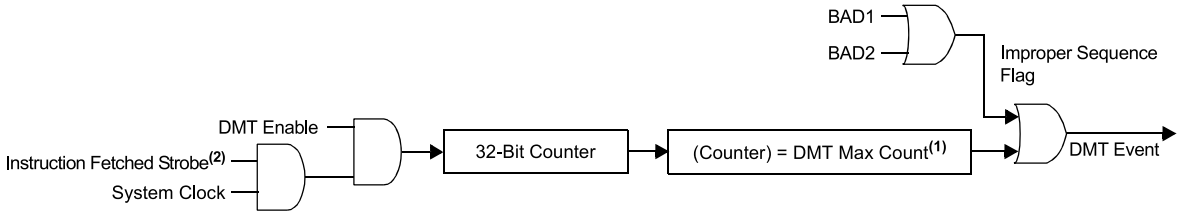
The primary function of the Deadman Timer (DMT) is to interrupt the processor in the event of a software malfunction. The DMT, which works on the system clock, is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

DMT can be enabled in the Configuration fuse or by software in the DMTCON register by setting the ON bit. The DMT consists of a 32-bit counter with a time-out count match value, as specified by the two 16-bit Configuration Fuse registers: FDMTCNTL and FDMTCNTH.

A DMT is typically used in mission-critical and safety-critical applications, where any single failure of the software functionality and sequencing must be detected.

Figure 29-1 shows a block diagram of the Deadman Timer module.

Figure 29-1. Deadman Timer Block Diagram



Notes:

1. DMT Max Count is controlled by the initial value of the FDMTCNTL and FDMTCNTH Configuration registers.
2. DMT window interval is controlled by the value of the FDMTIVTL and FDMTIVTH Configuration registers.

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29.1. Deadman Timer Control/Status Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x5C	DMTCON	15:8	ON							
		7:0								
0x5E ... 0x5F	Reserved									
0x60	DMTPRECLR	15:8	STEP1[7:0]							
		7:0								
0x62 ... 0x63	Reserved									
0x64	DMTCLR	15:8								
		7:0	STEP2[7:0]							
0x66 ... 0x67	Reserved									
0x68	DMTSTAT	15:8								
		7:0	BAD1	BAD2	DMTEVENT					WINOPN
0x6A ... 0x6B	Reserved									
0x6C	DMTCNTL	15:8	COUNTER[15:8]							
		7:0	COUNTER[7:0]							
0x6E	DMTCNTH	15:8	COUNTER[31:24]							
		7:0	COUNTER[23:16]							
0x70	DMTHOLDREG	15:8	UPRCNT[15:8]							
		7:0	UPRCNT[7:0]							
0x72 ... 0x73	Reserved									
0x74	DMTPSCNTL	15:8	PSCNT[15:8]							
		7:0	PSCNT[7:0]							
0x76	DMTPSCNTH	15:8	PSCNT[31:24]							
		7:0	PSCNT[23:16]							
0x78	DMTPSINTVL	15:8	PSINTV[15:8]							
		7:0	PSINTV[7:0]							
0x7A	DMTPSINTVH	15:8	PSINTV[31:24]							
		7:0	PSINTV[23:16]							

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29.1.1. Deadman Timer Control Register

Name: DMTCON
Offset: 0x05C

Note:

1. This bit has control only when DMTDIS = 0 in the FDMT register.

Bit	15	14	13	12	11	10	9	8
	ON							
Access	R/W							
Reset	0							

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – ON DMT Enable bit(1)

Value	Description
1	Deadman Timer module is enabled.
0	Deadman Timer module is not enabled.

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29.1.2. Deadman Timer Preclear Register

Name: DMTPRECLR
Offset: 0x060

Bit	15	14	13	12	11	10	9	8
	STEP1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 15:8 – STEP1[7:0] DMT Preclear Enable bits

Value	Description
01000000	Enables the Deadman Timer preclear (Step 1).
All Other Write Patterns	Sets the BAD1 flag; these bits are cleared when a DMT Reset event occurs. STEP1[7:0] bits are also cleared if the STEP2[7:0] bits are loaded with the correct value in the correct sequence.

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29.1.3. Deadman Timer Clear Register

Name: DMTCLR
Offset: 0x064

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	STEP2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – STEP2[7:0] DMT Clear Timer bits

Value	Description
00001000	Clears STEP1[7:0], STEP2[7:0] and the Deadman Timer if preceded by the correct loading of the STEP1[7:0] bits in the correct sequence. The write to these bits may be verified by reading the DMTCNTL/H registers and observing the counter being reset.
All Other Write Patterns	Sets the BAD2 bit; the value of STEP1[7:0] will remain unchanged and the new value being written to STEP2[7:0] will be captured. These bits are cleared when a DMT Reset event occurs.

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29.1.4. Deadman Timer Status Register

Name: DMTSTAT
Offset: 0x068

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BAD1	BAD2	DMTEVENT					WINOPN
Access	R/W	R/W	R/W					R/W
Reset	0	0	0					0

Bit 7 – BAD1 Deadman Timer BAD STEP1[7:0] Value Detect bit

Value	Description
1	Incorrect STEP1[7:0] value was detected.
0	Incorrect STEP1[7:0] value was not detected.

Bit 6 – BAD2 Deadman Timer BAD STEP2[7:0] Value Detect bit

Value	Description
1	Incorrect STEP2[7:0] value was detected.
0	Incorrect STEP2[7:0] value was not detected.

Bit 5 – DMTEVENT Deadman Timer Event bit

Value	Description
1	Deadman Timer event was detected (counter expired, or BAD STEP1[7:0] or STEP2[7:0] value was entered prior to counter increment).
0	Deadman Timer event was not detected.

Bit 0 – WINOPN Deadman Timer Clear Window bit

Value	Description
1	Deadman Timer clear window is open.
0	Deadman Timer clear window is not open.

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29.1.5. Deadman Timer Count Register Low

Name: DMTCNTL
Offset: 0x06C

Bit	15	14	13	12	11	10	9	8
	COUNTER[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNTER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COUNTER[15:0] Read Current Contents of Lower DMT Counter bits

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29.1.6. Deadman Timer Count Register High

Name: DMTCNTH
Offset: 0x06E

Bit	15	14	13	12	11	10	9	8
	COUNTER[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNTER[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COUNTER[31:16] Read Current Contents of Lower DMT Counter bits

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29.1.7. DMT Hold Register

Name: DMTHOLDREG(1)
Offset: 0x070

Note:

1. The DMTHOLDREG register is initialized to '0' on Reset, and is only loaded when the DMTCNTL and DMTCNTH registers are read.

Bit	15	14	13	12	11	10	9	8
	UPRCNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	UPRCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – UPRCNT[15:0] DMTCNTH Register Value When DMTCNTL and DMTCNTH Were Last Read bits

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29.1.8. DMT Post-Configure Count Status Register Low

Name: DMTPSCNTL
Offset: 0x074

Bit	15	14	13	12	11	10	9	8
	PSCNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSCNT[15:0] Lower DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTL Configuration register.

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29.1.9. DMT Post-Configure Count Status Register High

Name: DMTPSCNTH
Offset: 0x076

Bit	15	14	13	12	11	10	9	8
	PSCNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSCNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSCNT[31:16] Higher DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTH Configuration register.

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29.1.10. DMT Post-Configure Interval Status Register Low

Name: DMTPSINTVL
Offset: 0x078

Bit	15	14	13	12	11	10	9	8
	PSINTV[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSINTV[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSINTV[15:0] Lower DMT Window Interval Configuration Status bits
This is always the value of the FDMTIVTL Configuration register.

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29.1.11. DMT Post-Configure Interval Status Register High

Name: DMTPSINTVH
Offset: 0x07A

Bit	15	14	13	12	11	10	9	8
	PSINTV[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSINTV[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSINTV[31:16] Higher DMT Window Interval Configuration Status bits
This is always the value of the FDMTIVTH Configuration register.

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30. Power-Saving Features

The dsPIC33CDVL256MC506 family devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitute lower consumed power.

dsPIC33CDVL256MC506 family devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as time-sensitive communications.

30.1. Clock Frequency and Clock Switching

The dsPIC33CDVL256MC506 family devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON[10:8]). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in Oscillator with High-Frequency PLL.

30.2. Instruction-Based Power-Saving Modes

The dsPIC33CDVL256MC506 family devices have two special power-saving modes that are entered through the execution of a special `PWRSAV` instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the `PWRSAV` instruction is shown in Example 30-1 and Example 30-2.

Note: `SLEEP_MODE` and `IDLE_MODE` are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

Example 30-1. `PWRSAV` Instruction Syntax in Assembly

```
PWRSAV #SLEEP_MODE    ; Put the device into Sleep mode
PWRSAV #IDLE_MODE     ; Put the device into Idle mode
```

Example 30-2. `PWRSAV` Instruction Syntax in C Language

```
Sleep ()    ; Put the device into Sleep mode
Idle ()     ; Put the device into Idle mode
```


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30.2.1. Sleep Mode

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device's current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification on the I/O ports or peripherals that use an External Clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into standby when Sleep mode is entered by clearing the VREGS (RCON[8]) bit (default configuration).

If the application requires a faster wake-up time and can accept higher current requirements, the VREGS (RCON[8]) bit can be set to keep the internal regulator and the Flash regulator active during Sleep mode. The available Low-Power Sleep modes are shown in Table 30-1. Additional regulator information is available in On-Chip Voltage Regulator.

Table 30-1. Low-Power Sleep Modes

Relative Power	LPWREN	VREGS	MODE
Highest	0	1	Full power, active
—	0	0	Full power, standby
—	1 **(1)**	1	Low power, active
Lowest	1 **(1)**	0	Low power, standby

Note:

1. Low-Power modes, when LPWREN = 1, can only be used in the industrial temperature range.

30.2.2. Idle Mode

The following occurs in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see Peripheral Module Disable).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes up from Idle mode on any of these events:

- Any interrupt that is individually enabled

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- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (two to four clock cycles later), starting with the instruction following the `PWRSAV` instruction or the first instruction in the ISR.

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the SIDL bit in the Timer1 Control register (T1CON[13]).

30.3. Interrupts Coincident with Power Save Instructions

Any interrupt that coincides with the execution of a `PWRSAV` instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

30.4. Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV[11]). The ratio between peripheral and core clock speeds is determined by the DOZE[2:0] bits (CLKDIV[14:12]). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV[15]). By default, interrupt events have no effect on Doze mode operation.

30.5. Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have any effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note: If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

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30.6. Power-Saving Control Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0FA0	PMDCON	15:8					PMDLOCK			
		7:0								
0x0FA2 ... 0x0FA3	Reserved									
0x0FA4	PMD1	15:8					T1MD	QEIMD	PWMMD	
		7:0	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD		C1MD	ADC1MD
0x0FA6	PMD2	15:8								
		7:0					CCP4MD	CCP3MD	CCP2MD	CCP1MD
0x0FA8	PMD3	15:8								
		7:0	CRCMD				U3MD			
0x0FAA	PMD4	15:8								
		7:0					REFOMD			
0x0FAC ... 0x0FAD	Reserved									
0x0FAE	PMD6	15:8					DMA3MD	DMA2MD	DMA1MD	DMA0MD
		7:0								
0x0FB0	PMD7	15:8							CMP2MD	CMP1MD
		7:0					PTGMD			
0x0FB2	PMD8	15:8			OPAMPMD		SENT1MD			
		7:0			CLC4MD	CLC3MD	CLC2MD	CLC1MD	BIASMD	

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30.6.1. PMD Control Register

Name: PMDCON
Offset: 0xFA0

Bit	15	14	13	12	11	10	9	8
					PMDLOCK			
Access					R/W			
Reset					0			

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 11 – PMDLOCK Peripheral Remapping Register Lock bit

Value	Description
1	All PMD registers are locked and cannot be written.
0	All PMD registers are unlocked and can be written.

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30.6.2. Peripheral Module Disable 1 Control Register

Name: PMD1(1,2)
Offset: 0xFA4

Notes:

1. When a peripheral is disabled (PMD = 1), its clocks are gated off and its Reset is asserted, providing a reduced power consumption.
2. Since the Reset to the peripheral is asserted when PMD = 1, the module's registers must be reinitialized to their desired values whenever the corresponding PMD bit is cleared.

Bit	15	14	13	12	11	10	9	8
					T1MD	QEIMD	PWMMD	
Access					R/W	R/W	R/W	
Reset					0	0	0	

Bit	7	6	5	4	3	2	1	0
	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD		C1MD	ADC1MD
Access	R/W	R/W	R/W	R/W	R/W		R/W	R/W
Reset	0	0	0	0	0		0	0

Bit 11 – T1MD Timer1 Module Disable bit

Value	Description
1	Timer1 module is disabled
0	Timer1 module is enabled

Bit 10 – QEIMD QEI Module Disable bit

Value	Description
1	QEI module is disabled
0	QEI module is enabled

Bit 9 – PWMMD PWM Module Disable bit

Value	Description
1	PWM module is disabled
0	PWM module is enabled

Bit 7 – I2C1MD I2C1 Module Disable bit

Value	Description
1	I2C1 module is disabled
0	I2C1 module is enabled

Bit 6 – U2MD UART2 Module Disable bit

Value	Description
1	UART2 module is disabled
0	UART2 module is enabled

Bit 5 – U1MD UART1 Module Disable bit

Value	Description
1	UART1 module is disabled
0	UART1 module is enabled

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Bit 4 – SPI2MD SPI2 Module Disable bit

Value	Description
1	SPI2 module is disabled
0	SPI2 module is enabled

Bit 3 – SPI1MD SPI1 Module Disable bit

Value	Description
1	SPI1 module is disabled
0	SPI1 module is enabled

Bit 1 – C1MD CAN1 Module Disable bit

Value	Description
1	CAN1 module is disabled
0	CAN1 module is enabled

Bit 0 – ADC1MD ADC Module Disable bit

Value	Description
1	ADC module is disabled
0	ADC module is enabled

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30.6.3. Peripheral Module Disable 2 Control Register

Name: PMD2[1,2]
Offset: 0xFA6

Notes:

1. When a peripheral is disabled (PMD = 1), its clocks are gated off and its Reset is asserted, providing a reduced power consumption.
2. Since the Reset to the peripheral is asserted when PMD = 1, the module's registers must be reinitialized to their desired values whenever the corresponding PMD bit is cleared.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					CCP4MD	CCP3MD	CCP2MD	CCP1MD
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – CCP4MD SCCP4 Module Disable bit

Value	Description
1	SCCP4 module is disabled.
0	SCCP4 module is enabled.

Bit 2 – CCP3MD SCCP3 Module Disable bit

Value	Description
1	SCCP3 module is disabled.
0	SCCP3 module is enabled.

Bit 1 – CCP2MD SCCP2 Module Disable bit

Value	Description
1	SCCP2 module is disabled.
0	SCCP2 module is enabled.

Bit 0 – CCP1MD SCCP1 Module Disable bit

Value	Description
1	SCCP1 module is disabled.
0	SCCP1 module is enabled.

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30.6.4. Peripheral Module Disable 3 Control Register

Name: PMD3[1,2]
Offset: 0xFA8

Notes:

1. When a peripheral is disabled (PMD = 1), its clocks are gated off and its Reset is asserted, providing a reduced power consumption.
2. Since the Reset to the peripheral is asserted when PMD = 1, the module's registers must be reinitialized to their desired values whenever the corresponding PMD bit is cleared.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	CRCMD				U3MD			
Access	R/W				R/W			
Reset	0				0			

Bit 7 – CRCMD CRC Module Disable bit

Value	Description
1	CRC module is disabled.
0	CRC module is enabled.

Bit 3 – U3MD UART3 Module Disable bit

Value	Description
1	UART3 module is disabled.
0	UART3 module is enabled.

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30.6.5. Peripheral Module Disable 4 Control Register

Name: PMD4(1,2)
Offset: 0xFAA

Notes:

1. When a peripheral is disabled (PMD = 1), its clocks are gated off and its Reset is asserted, providing a reduced power consumption.
2. Since the Reset to the peripheral is asserted when PMD = 1, the module's registers must be reinitialized to their desired values whenever the corresponding PMD bit is cleared.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					REFOMD			
Access					R/W			
Reset					0			

Bit 3 – REFOMD Reference Clock Module Disable bit

Value	Description
1	Reference clock module is disabled.
0	Reference clock module is enabled.

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30.6.6. Peripheral Module Disable 6 Control Register

Name: PMD6(1,2)
Offset: 0xFAE

Notes:

1. When a peripheral is disabled (PMD = 1), its clocks are gated off and its Reset is asserted, providing a reduced power consumption.
2. Since the Reset to the peripheral is asserted when PMD = 1, the module's registers must be reinitialized to their desired values whenever the corresponding PMD bit is cleared.

Bit	15	14	13	12	11	10	9	8
					DMA3MD	DMA2MD	DMA1MD	DMA0MD
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 11 – DMA3MD DMA3 Module Disable bit

Value	Description
1	DMA3 module is disabled.
0	DMA3 module is enabled.

Bit 10 – DMA2MD DMA2 Module Disable bit

Value	Description
1	DMA2 module is disabled.
0	DMA2 module is enabled.

Bit 9 – DMA1MD DMA1 Module Disable bit

Value	Description
1	DMA1 module is disabled.
0	DMA1 module is enabled.

Bit 8 – DMA0MD DMA0 Module Disable bit

Value	Description
1	DMA0 module is disabled.
0	DMA0 module is enabled.

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30.6.7. Peripheral Module Disable 7 Control Register

Name: PMD7(1,2)
Offset: 0xFB0

Notes:

1. When a peripheral is disabled (PMD = 1), its clocks are gated off and its Reset is asserted, providing a reduced power consumption.
2. Since the Reset to the peripheral is asserted when PMD = 1, the module's registers must be reinitialized to their desired values whenever the corresponding PMD bit is cleared.

Bit	15	14	13	12	11	10	9	8
							CMP2MD	CMP1MD
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
					PTGMD			
Access					R/W			
Reset					0			

Bit 9 – CMP2MD Comparator 2 Disable bit

Value	Description
1	Comparator 2 module is disabled
0	Comparator 2 module is enabled

Bit 8 – CMP1MD Comparator 1 Disable bit

Value	Description
1	Comparator 1 module is disabled
0	Comparator 1 module is enabled

Bit 3 – PTGMD PTG Module Disable bit

Value	Description
1	PTG module is disabled
0	PTG module is enabled

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30.6.8. Peripheral Module Disable 8 Control Register

Name: PMD8(1,2)
Offset: 0xFB2

Notes:

1. When a peripheral is disabled (PMD = 1), its clocks are gated off and its Reset is asserted, providing a reduced power consumption.
2. Since the Reset to the peripheral is asserted when PMD = 1, the module's registers must be reinitialized to their desired values whenever the corresponding PMD bit is cleared.

Bit	15	14	13	12	11	10	9	8
			OPAMPMD		SENT1MD			
Access			R/W		R/W			
Reset			0		0			

Bit	7	6	5	4	3	2	1	0
			CLC4MD	CLC3MD	CLC2MD	CLC1MD	BIASMD	
Access			R/W	R/W	R/W	R/W	R/W	
Reset			0	0	0	0	0	

Bit 13 – OPAMPMD Op Amp Module Disable bit

Value	Description
1	Op Amp module is disabled
0	Op Amp module is enabled

Bit 11 – SENT1MD SENT1 Module Disable bit

Value	Description
1	SENT1 module is disabled
0	SENT1 module is enabled

Bit 5 – CLC4MD CLC4 Module Disable bit

Value	Description
1	CLC4 module is disabled
0	CLC4 module is enabled

Bit 4 – CLC3MD CLC3 Module Disable bit

Value	Description
1	CLC3 module is disabled
0	CLC3 module is enabled

Bit 3 – CLC2MD CLC2 Module Disable bit

Value	Description
1	CLC2 module is disabled
0	CLC2 module is enabled

Bit 2 – CLC1MD CLC1 Module Disable bit

Value	Description
1	CLC1 module is disabled
0	CLC1 module is enabled

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Bit 1 – BIASMD Current Bias Module Disable bit

Value	Description
1	Current bias module is disabled
0	Current bias module is enabled

30.7. Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page contains the latest updates and additional information.

30.7.1. Key Resources

- **"Watchdog Timer and Power-Saving Modes"** (www.microchip.com/DS70000615) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

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31. Special Features

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip website (www.microchip.com).

The dsPIC33CDVL256MC506 family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation
- Brown-out Reset (BOR)

31.1. Configuration Bits

In dsPIC33CDVL256MC506 family devices, the Configuration Words are implemented as volatile memory. This means that configuration data will get loaded to volatile memory (from the Flash Configuration Words) each time the device is powered up. Configuration data are stored at the end of the on-chip program memory space, known as the Flash Configuration Words. Their specific locations are shown in Table 31-1. The configuration data are automatically loaded from the Flash Configuration Words to the proper Configuration Shadow registers during device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Words for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled. Program code executing out of configuration space will cause a device Reset.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration Words.

Table 31-1. dsPIC33CDV(L)XXXMCX06 Configuration Addresses

Register Name	128k Address	256k Address
FSEC	0x015F00	0x02BF00
FBSLIM	0x015F10	0x02BF10
FSIGN	0x015F14	0x02BF14
FOSCSEL	0x015F18	0x02BF18
FOSC	0x015F1C	0x02BF1C
FWDT	0x015F20	0x02BF20
FPOR	0x015F24	0x02BF24
FICD	0x015F28	0x02BF28
FDMTIVTL	0x015F2C	0x02BF2C
FDMTIVTH	0x015F30	0x02BF30
FDMTCNTL	0x015F34	0x02BF34
FDMTCNTH	0x015F38	0x02BF38
FDMT	0x015F3C	0x02BF3C
FDEVOPT	0x015F40	0x02BF40

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Table 31-1. dsPIC33CDV(L)XXXMCX06 Configuration Addresses (continued)

Register Name	128k Address	256k Address
FALTREG	0x015F44	0x02BF44

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31.2. Configuration Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0F00	FSEC	23:16								
		15:8	AIVTDIS				CSS[2:0]			CWRP
		7:0	GSS[1:0]		GWRP		BSEN	BSS[1:0]		BWRP
0x0F03 ... 0x0F0F	Reserved									
0x0F10	FBSLIM	23:16								
		15:8				BSLIM[12:8]				
		7:0	BSLIM[7:0]							
0x0F13	Reserved									
0x0F14	FSIGN	23:16								
		15:8	SIGN							
		7:0								
0x0F17	Reserved									
0x0F18	FOSCSEL	23:16								
		15:8								
		7:0	IESO					FNOSC[2:0]		
0x0F1B	Reserved									
0x0F1C	FOSC	23:16								
		15:8				XTBST	XTCFG[1:0]			PLLKEN
		7:0	FCKSM[1:0]					OSCIOFNC	POSCMD[1:0]	
0x0F1F	Reserved									
0x0F20	FWDT	23:16								
		15:8	FWDTEN			SWDTPS[4:0]			WDTWIN[1:0]	
		7:0	WINDIS	RCLKSEL[1:0]			RWDTPS[4:0]			
0x0F23	Reserved									
0x0F24	FPOR	23:16								
		15:8								
		7:0		BISTDIS	Reserved[1:0]					
0x0F27	Reserved									
0x0F28	FICD	23:16								
		15:8								
		7:0			JTAGEN				ICS[1:0]	
0x0F2B	Reserved									
0x0F2C	FDMTIVTL	23:16								
		15:8	DMTIVT[15:8]							
		7:0	DMTIVT[7:0]							
0x0F2F	Reserved									
0x0F30	FDMTIVTH	23:16								
		15:8	DMTIVT[31:24]							
		7:0	DMTIVT[23:16]							
0x0F33	Reserved									
0x0F34	FDMTCNTL	23:16								
		15:8	DMTCNT[15:8]							
		7:0	DMTCNT[7:0]							
0x0F37	Reserved									
0x0F38	FDMTCNTH	23:16								
		15:8	DMTCNT[31:24]							
		7:0	DMTCNT[23:16]							
0x0F3B	Reserved									
0x0F3C	FDMT	23:16								
		15:8								
		7:0								DMTDIS
0x0F3F	Reserved									
0x0F40	FDEVOPT	23:16								
		15:8			SPI2PIN	DUPPWM		SMBEN	Reserved[1:0]	
		7:0	Reserved		ALTI2C3	ALTI2C2	ALTI2C1	Reserved		
0x0F43	Reserved									

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Configuration Registers (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0F44	FALTREG	23:16								
		15:8		CTXT4[2:0]				CTXT3[2:0]		
		7:0		CTXT2[2:0]				CTXT1[2:0]		

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31.2.1. FSEC Configuration Register

Name: FSEC
Offset: 0xF00

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	AIVTDIS				CSS[2:0]			CWRP
Access	R/PO				R/PO	R/PO	R/PO	R/PO
Reset	1				1	1	1	1

Bit	7	6	5	4	3	2	1	0
	GSS[1:0]		GWRP		BSEN	BSS[1:0]		BWRP
Access	R/PO	R/PO	R/PO		R/PO	R/PO	R/PO	R/PO
Reset	1	1	1		1	0	1	1

Bit 15 – AIVTDIS Alternate Interrupt Vector Table Disable bit

Value	Description
1	Disables AIVT.
0	Enables AIVT.

Bits 11:9 – CSS[2:0] Configuration Segment Code Flash Protection Level bits

Value	Description
111	No protection (other than CWRP write protection).
110	Standard security
10x	Enhanced security
0xx	High security

Bit 8 – CWRP Configuration Segment Write-Protect bit

Value	Description
1	Configuration Segment is not write-protected.
0	Configuration Segment is write-protected.

Bits 7:6 – GSS[1:0] General Segment Code Flash Protection Level bits

Value	Description
11	No protection (other than GWRP write protection).
10	Standard security
0x	High security

Bit 5 – GWRP General Segment Write-Protect bit

Value	Description
1	User program memory is not write-protected.
0	User program memory is write-protected.

Bit 3 – BSEN Boot Segment Control bit

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Value	Description
1	No Boot Segment.
0	Boot Segment size is determined by BSLIM[12:0].

Bits 2:1 – BSS[1:0] Boot Segment Code Flash Protection Level bits

Value	Description
11	No protection (other than BWRP write protection).
10	Standard security
0x	High security

Bit 0 – BWRP Boot Segment Write-Protect bit

Value	Description
1	User program memory is not write-protected.
0	User program memory is write-protected.

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31.2.2. FBSLIM Configuration Register

Name: FBSLIM
Offset: 0xF10

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				BSLIM[12:8]				
Access				R/PO	R/PO	R/PO	R/PO	R/PO
Reset				1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	BSLIM[7:0]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 12:0 – BSLIM[12:0] Boot Segment Code Flash Page Address Limit bits
Contains the page address of the first active General Segment page. The value to be programmed is the inverted page address, such that programming additional '0's can only increase the Boot Segment size.

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31.2.3. FSIGN Configuration Register

Name: FSIGN
Offset: 0xF14

Legend: r = Reserved bit; PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access	r	r	r	r	r	r	r	r
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	SIGN							
Access	PO	r	r	r	r	r	r	r
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Reset	1	1	1	1	1	1	1	1

Bit 15 – SIGN Active Panel Signature bit

Value	Description
1	Active Panel Signature bit is erased (CP data are not valid).
0	Active Panel Signature bit is programmed (CP data are valid).

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31.2.4. FOSCSEL Configuration Register

Name: FOSCSEL
Offset: 0xF18

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	IESO					FNOSC[2:0]		
Access	R/PO					R/PO	R/PO	R/PO
Reset	1					1	1	1

Bit 7 – IESO Internal External Switchover bit

Value	Description
1	Internal External Switchover mode is enabled (Two-Speed Start-up is enabled).
0	Internal External Switchover mode is disabled (Two-Speed Start-up is disabled).

Bits 2:0 – FNOSC[2:0] Initial Oscillator Source Selection bits

Value	Description
111	Internal Fast RC (FRC) Oscillator with Postscaler
110	Backup Fast RC (BFRC)
101	LPRC Oscillator
100	Reserved
011	Primary Oscillator with PLL (XTPLL, HSPLL, ECPLL)
010	Primary (XT, HS, EC) Oscillator
001	Internal Fast RC Oscillator with PLL (FRCPLL)
000	Fast RC (FRC) Oscillator

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31.2.5. FOSC Configuration Register

Name: FOSC
Offset: 0xF1C

Note:

1. A time-out period will occur when the system clock switching logic requests the PLL clock source and the PLL is not already enabled.

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				XTBST	XTCFG[1:0]			PLLKEN
Access				R/PO	R/PO	R/PO		R/PO
Reset				1	1	1		1

Bit	7	6	5	4	3	2	1	0
	FCKSM[1:0]					OSCIOFNC	POSCMD[1:0]	
Access	R/PO	R/PO				R/PO	R/PO	R/PO
Reset	1	1				1	1	1

Bit 12 – XTBST Oscillator Kick-Start Programmability bit

Value	Description
1	Boosts the kick-start.
0	Default kick-start.

Bits 11:10 – XTCFG[1:0] Crystal Oscillator Drive Select bits
Current gain programmability for oscillator (output drive).

Value	Description
11	Gain3 (use for 24-32 MHz crystals)
10	Gain2 (use for 16-24 MHz crystals)
01	Gain1 (use for 8-16 MHz crystals)
00	Gain0 (use for 4-8 MHz crystals)

Bit 8 – PLLKEN PLL Lock Status Control bit(1)

Value	Description
1	PLL lock signal will be used to disable the PLL clock output if the lock is lost.
0	PLL lock signal is not used; the PLL clock output will not be disabled if the lock is lost.

Bits 7:6 – FCKSM[1:0] Clock Switching Mode bits

Value	Description
1x	Clock switching is disabled, Fail-Safe Clock Monitor is disabled.
01	Clock switching is enabled, Fail-Safe Clock Monitor is disabled.
00	Clock switching is enabled, Fail-Safe Clock Monitor is enabled.

Bit 2 – OSCIOFNC OSCO Pin Function bit (except in XT and HS modes)(1)

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Value	Description
1	OSCO is the clock output.
0	OSCO is the general purpose digital I/O pin.

Bits 1:0 – POSCMD[1:0] Primary Oscillator Mode Select bits

Value	Description
11	Primary Oscillator is disabled.
10	HS Crystal Oscillator mode (10 MHz-32 MHz)
01	XT Crystal Oscillator mode (3.5 MHz-10 MHz)
00	EC (External Clock) mode

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31.2.6. FWDT Configuration Register

Name: FWDT
Offset: 0xF20

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	FWDTEN	SWDTPS[4:0]					WDTWIN[1:0]	
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	WINDIS	RCLKSEL[1:0]		RWDTPS[4:0]				
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bit 15 – FWDTEN Watchdog Timer Enable bit

Value	Description
1	WDT is enabled in hardware.
0	WDT controller via the ON bit (WDTCONL[15]).

Bits 14:10 – SWDTPS[4:0] Sleep Mode Watchdog Timer Period Select bits

Value	Description
11111	Divide by 2 ^ 31 = 2,147,483,648
11110	Divide by 2 ^ 30 = 1,073,741,824
. . .	
00001	Divide by 2 ^ 1, 2
00000	Divide by 2 ^ 0, 1

Bits 9:8 – WDTWIN[1:0] Watchdog Timer Window Select bits

Value	Description
11	WDT window is 25% of the WDT period.
10	WDT window is 37.5% of the WDT period.
01	WDT window is 50% of the WDT period.
00	WDT Window is 75% of the WDT period.

Bit 7 – WINDIS Watchdog Timer Window Enable bit

Value	Description
1	Watchdog Timer is in Non-Window mode.
0	Watchdog Timer is in Window mode.

Bits 6:5 – RCLKSEL[1:0] Watchdog Timer Clock Select bits

Value	Description
11	LPRC clock
10	FRC clock
01	Peripheral clock

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Value	Description
00	Reserved

Bits 4:0 – RWDTPS[4:0] Run Mode Watchdog Timer Period Select bits

Value	Description
11111	Divide by 2 ^ 31 = 2,147,483,648
11110	Divide by 2 ^ 30 = 1,073,741,824
. . .	
00001	Divide by 2 ^ 1, 2
00000	Divide by 2 ^ 0, 1

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31.2.7. FPOR Configuration Register

Name: FPOR
Offset: 0xF24

Legend: PO = Program Once bit, r = Reserved bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		BISTDIS	Reserved[1:0]					
Access		R/PO	r	r				
Reset		1	1	1				

Bit 6 – BISTDIS Memory BIST Feature Disable bit

Value	Description
1	Normal start-up operation after Reset; executes instruction at 0x000000.
0	Optional start-up operation after Reset; executes instruction at start of boot space.

Bits 5:4 – Reserved[1:0] Maintain as '1' bits.

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31.2.8. FICD Configuration Register

Name: FICD
Offset: 0xF28

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			JTAGEN				ICS[1:0]	
Access			R/PO				R/PO	R/PO
Reset			1				1	1

Bit 5 – JTAGEN JTAG Enable bit

Value	Description
1	JTAG port is enabled.
0	JTAG port is disabled.

Bits 1:0 – ICS[1:0] ICD Communication Channel Select bits

Value	Description
11	Host communicates on PGC1 and PGD1.
10	Host communicates on PGC2 and PGD2.
01	Host communicates on PGC3 and PGD3.
00	Reserved, do not use.

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31.2.9. FDMTIVTL Configuration Register

Name: FDMTIVTL
Offset: 0xF2C

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DMTIVT[15:8]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	DMTIVT[7:0]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 15:0 – DMTIVT[15:0] DMT Window Interval Lower 16 bits

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31.2.10. FDMTIVTH Configuration Register

Name: FDMTIVTH
Offset: 0xF30

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DMTIVT[31:24]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DMTIVT[23:16]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 15:0 – DMTIVT[31:16] DMT Window Interval Higher 16 bits

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31.2.11. FDMTCNTL Configuration Register

Name: FDMTCNTL
Offset: 0xF34

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DMTCNT[15:8]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	DMTCNT[7:0]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 15:0 – DMTCNT[15:0] DMT Instruction Count Time-out Value Lower 16 bits

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31.2.12. FDMTCNTH Configuration Register

Name: FDMTCNTH
Offset: 0xF38

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DMTCNT[31:24]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DMTCNT[23:16]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 15:0 – DMTCNT[31:16] DMT Instruction Count Time-out Value Upper 16 bits

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31.2.13. FDMT Configuration Register

Name: FDMT
Offset: 0xF3C

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								DMTDIS
Access								R/PO
Reset								1

Bit 0 – DMTDIS DMT Disable bit

Value	Description
1	Deadman Timer is disabled and can be enabled by software using the ON bit (DMTCON[15]).
0	Deadman Timer is enabled and cannot be disabled by software.

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31.2.14. FDEVOPT Configuration Register

Name: FDEVOPT
Offset: 0xF40

Note:

1. Fixed pin option is only available for higher pin packages (48-pin, 64-pin and 80-pin).

Legend: PO = Program Once bit; r = Reserved bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
			SPI2PIN	DUPPWM		SMBEN	Reserved[1:0]	
Access			R/PO	R/PO		R/PO	r	r
Reset			1	1		1	0	0

Bit	7	6	5	4	3	2	1	0
	Reserved		ALTI2C3	ALTI2C2	ALTI2C1	Reserved		
Access	r		R/PO	R/PO	R/PO	r		
Reset	1		1	1	1	1		

Bit 13 – SPI2PIN Main SPI #2 Fast I/O Pad Disable bit(1)

Value	Description
1	Host SPI2 uses PPS (I/O remap) to make connections with device pins.
0	Host SPI2 uses direct connections with specified device pins.

Bit 12 – DUPPWM DUPPWM bit

Value	Description
1	PWM4 functions on PPS and fixed pins .
0	PWM4 functions only on fixed pins.

Bit 10 – SMBEN Select Input Voltage Threshold for I^2C Pads to be SMBus 3.0 Compliant bit

Value	Description
1	Enables SMBus 3.0 input threshold voltage.
0	I^2C pad input buffer operation.

Bits 9:8 – Reserved[1:0] Maintain as '0' bits

Bit 7 – Reserved Maintain as '1' bit

Bit 5 – ALTI2C3 Alternate I2C3 Pin Mapping bit

Value	Description
1	Default location for SCL3/SDA3 pins.
0	Alternate location for SCL3/SDA3 pins (ASCL3/ASDA3).

Bit 4 – ALTI2C2 Alternate I2C2 Pin Mapping bit

Value	Description
1	Default location for SCL2/SDA2 pins.

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Value	Description
0	Alternate location for SCL2/SDA2 pins (ASCL2/ASDA2).

Bit 3 – ALTI2C1 Alternate I2C1 Pin Mapping bit

Value	Description
1	Default location for SCL1/SDA1 pins.
0	Alternate location for SCL1/SDA1 pins (ASCL1/ASDA1).

Bit 2 – Reserved Maintain as '1' bit

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31.2.15. FALTREG Configuration Register

Name: FALTREG
Offset: 0xF44

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
		CTXT4[2:0]				CTXT3[2:0]		
Access		R/PO	R/PO	R/PO		R/PO	R/PO	R/PO
Reset		1	1	1		1	1	1

Bit	7	6	5	4	3	2	1	0
		CTXT2[2:0]				CTXT1[2:0]		
Access		R/PO	R/PO	R/PO		R/PO	R/PO	R/PO
Reset		1	1	1		1	1	1

Bits 14:12 – CTXT4[2:0] Specifies Alternate Working Register Set #4 with IPLs bits

Value	Description
111	Not assigned
110	Alternate Register Set #4 is assigned to IPL Level 7.
101	Alternate Register Set #4 is assigned to IPL Level 6.
100	Alternate Register Set #4 is assigned to IPL Level 5.
011	Alternate Register Set #4 is assigned to IPL Level 4.
010	Alternate Register Set #4 is assigned to IPL Level 3.
001	Alternate Register Set #4 is assigned to IPL Level 2.
000	Alternate Register Set #4 is assigned to IPL Level 1.

Bits 10:8 – CTXT3[2:0] Specifies Alternate Working Register Set #3 with IPLs bits

Value	Description
111	Not assigned
110	Alternate Register Set #3 is assigned to IPL Level 7.
101	Alternate Register Set #3 is assigned to IPL Level 6.
100	Alternate Register Set #3 is assigned to IPL Level 5.
011	Alternate Register Set #3 is assigned to IPL Level 4.
010	Alternate Register Set #3 is assigned to IPL Level 3.
001	Alternate Register Set #3 is assigned to IPL Level 2.
000	Alternate Register Set #3 is assigned to IPL Level 1.

Bits 6:4 – CTXT2[2:0] Specifies Alternate Working Register Set #2 with IPLs bits

Value	Description
111	Not assigned
110	Alternate Register Set #2 is assigned to IPL Level 7.
101	Alternate Register Set #2 is assigned to IPL Level 6.
100	Alternate Register Set #2 is assigned to IPL Level 5.
011	Alternate Register Set #2 is assigned to IPL Level 4.
010	Alternate Register Set #2 is assigned to IPL Level 3.
001	Alternate Register Set #2 is assigned to IPL Level 2.

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Value	Description
000	Alternate Register Set #2 is assigned to IPL Level 1.

Bits 2:0 – CTXT1[2:0] Specifies Alternate Working Register Set #1 with IPLs bits

Value	Description
111	Not assigned
110	Alternate Register Set #1 is assigned to IPL Level 7.
101	Alternate Register Set #1 is assigned to IPL Level 6.
100	Alternate Register Set #1 is assigned to IPL Level 5.
011	Alternate Register Set #1 is assigned to IPL Level 4.
010	Alternate Register Set #1 is assigned to IPL Level 3.
001	Alternate Register Set #1 is assigned to IPL Level 2.
000	Alternate Register Set #1 is assigned to IPL Level 1.

31.3. Device Calibration and Identification

The dsPIC33CDVL256MC506 devices have two Identification registers, near the end of configuration memory space, that store the Device ID (DEVID) and Device Revision (DEVREV). These registers are used to determine the mask, variant and manufacturing information about the device. These registers are read-only and are shown in DEVREV and DEVID.

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31.3.1. Device Revision Register

Name: DEVREV

Legend: R = Read-only bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					DEVREV[3:0]			
Access					R	R	R	R
Reset								

Bits 3:0 – DEVREV[3:0] Device Revision bits

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31.3.2. Device ID Register

Name: DEVID

Note:

1. See Device IDs for the list of Device Identifier bits.

Legend: R = Read-only bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	FAMID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	DEV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 15:8 – FAMID[7:0] Device Family Identifier bits

Value	Description
1000 0111	dsPIC33CDVL256MC506 family

Bits 7:0 – DEV[7:0] Individual Device Identifier bits(1)

31.3.3. Device IDs

Table 31-2. Device IDs for the dsPIC33CDVL256MC506 Family

Device	DEVID
dsPIC33CDVL256MC106	0xA23A
dsPIC33CDVL128MC106	0xA22A
dsPIC33CDV256MC106	0xA21A
dsPIC33CDV128MC106	0xA20A

31.4. User OTP Memory

The dsPIC33CDVL256MC506 family devices contain 64 One-Time-Programmable (OTP) double words, located at addresses, 801700h through 8017FEh. Each 48-bit OTP double word can only be written one time. The OTP Words can be used for storing checksums, code revisions, manufacturing dates, manufacturing lot numbers or any other application-specific information.

The OTP area is not cleared by any erase command. This memory can be written only once.

31.5. On-Chip Voltage Regulator

All of the dsPIC33CDVL256MC506 family devices have an internal voltage regulator to supply power to the core at 1.2V (typical).

The voltage regulator power can be controlled by the LPWREN bit in the VREGCON register when LPWREN (VREGCON[15]) = 1. Then, the regulators are put into a lower power mode.

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The regulators have Low-Power and Standby modes for use in Sleep modes. For additional information about Sleep, see Sleep Mode. When the regulators are in Low-Power mode (LPWREN = 1), the power available to the core is limited.

Before the LPWREN bit is set, the device should be placed into a Low Power state by disabling peripherals and lowering the CPU frequency (e.g., 8 MHz FRC without PLL). The output voltages of the three regulators can be controlled independently by the user, which provides the capability to save additional power during Sleep mode.

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31.5.1. Voltage Regulator Control Register

Name: VREGCON

Note:

1. Low-Power mode can only be used within the industrial temperature range. The CPU should be run at a slow speed (8 MHz or less) before setting this bit.

Legend: r = Reserved bit

Bit	15	14	13	12	11	10	9	8
	LPWREN	Reserved[14:8]						
Access	R/W	r	r	r	r	r	r	r
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	Reserved[7:0]							
Access	r	r	r	r	r	r	r	r
Reset	0	0	0	0	0	0	0	0

Bit 15 – LPWREN Low-Power Mode Enable bit(1)

Value	Description
1	Voltage regulators are in Low-Power mode.
0	Voltage regulators are in Full Power mode.

Bits 14:0 – Reserved[14:0] Maintain as '0' bits

31.6. Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse which resets the device. The BOR selects the clock source based on the device Configuration bit selections.

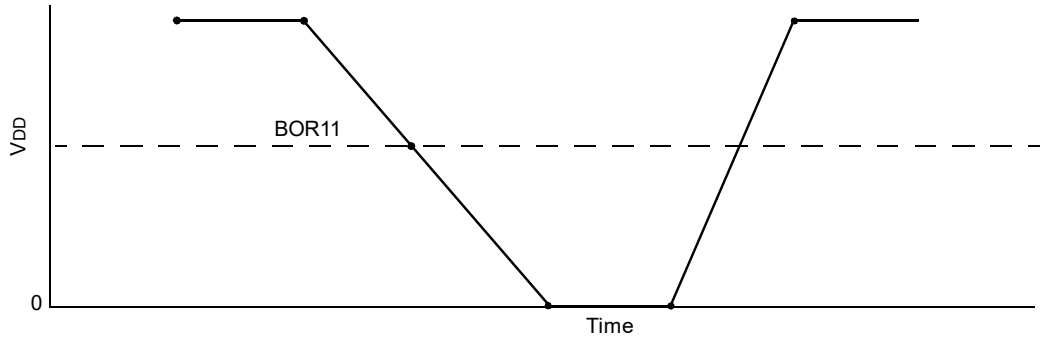
If an Oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON[5]) is '1'.

The BOR status bit (RCON[1]) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle mode and resets the device should V_{DD} fall below the BOR threshold voltage.

If V_{DD} drops below the BO11 value in Figure 31-1, V_{DD} must be brought down to 0V before ramping the device back up to operation range.

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Figure 31-1. POR Event on V_{DD}



Note:

1. If V_{DD} drops below the BO11 value in Table 34-5, V_{DD} must be brought down to 0V before ramping the device back up to operation range.

31.7. Dual Watchdog Timer (WDT)

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Dual Watchdog Timer"**, (www.microchip.com/DS70005250) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The dsPIC33 dual Watchdog Timer (WDT) is described in this section. Refer to Figure 31-2 for a block diagram of the WDT.

The WDT, when enabled, operates from the internal Low-Power RC (LPRC) Oscillator clock source or a selectable clock source in Run mode. The WDT can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. The WDT can be configured in Windowed mode or Non-Windowed mode. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode (Power Save mode). If the WDT expires and issues a device Reset, the WTDO bit in the RCON register will be set.

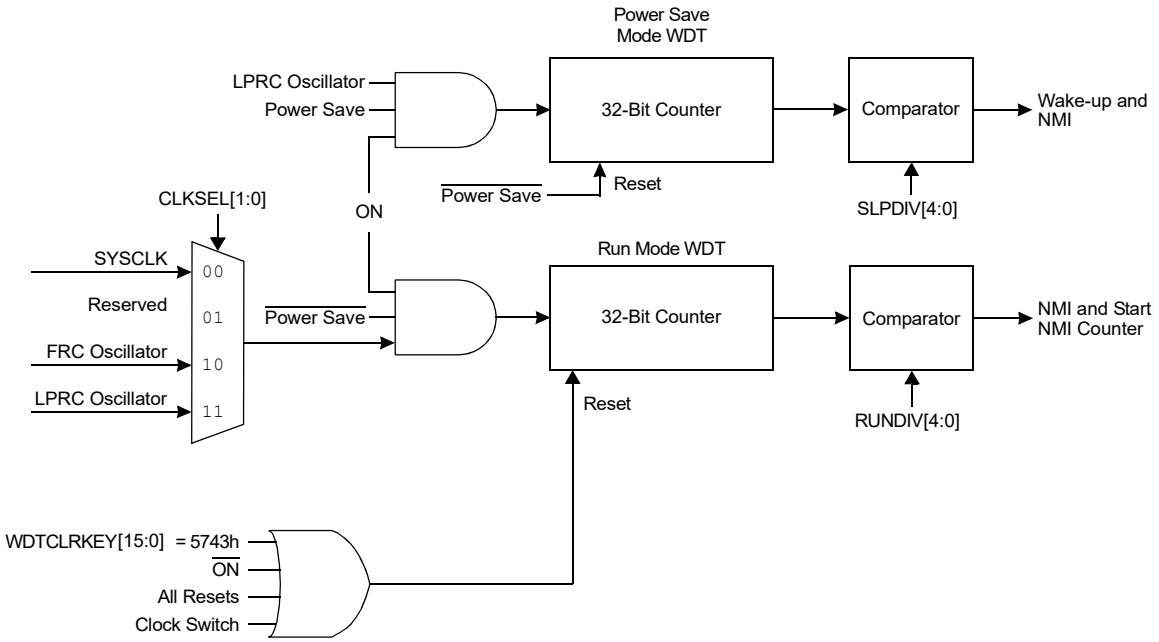
Note: Run mode WDT is made to stall during NVM operation whenever code execution and NVM operation happen on the same Flash partition, and it resumes its counter once after NVM programming.

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The following are some of the key features of the WDT modules:

- Configuration or Software Controlled
- Separate User-Configurable Time-out Periods for Run and Sleep/Idle
- Can Wake the Device from Sleep or Idle
- User-Selectable Clock Source in Run Mode
- Operates from LPRC in Sleep/Idle Mode

Figure 31-2. Watchdog Timer Block Diagram



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31.7.1. Watchdog Timer Control Register Low

Name: WDTCONL

Notes:

1. A read of this bit will result in a '1' if the WDT is enabled by the device configuration or by software. The user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
2. The user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
3. These bits reflect the value of the Configuration bits.
4. The WDTWINEN bit reflects the status of the Configuration bit if the bit is set. If the bit is cleared, the value is controlled by software.
5. The available clock sources are device-dependent.

Legend: y = Value from Configuration bit on POR; HS = Hardware Settable bit

Bit	15	14	13	12	11	10	9	8
	ON			RUNDIV[4:0]				
Access	R/W			R	R	R	R	R
Reset	0			0	0	0	0	y

Bit	7	6	5	4	3	2	1	0
	CLKSEL[1:0]		SLPDIV[4:0]					WDTWINEN
Access	R	R	R	R	R	R	R	HS/R/W
Reset	0	0	0	0	0	0	y	0

Bit 15 – ON Watchdog Timer Enable bit(1,2)

Value	Description
1	Enables the Watchdog Timer if it is not enabled by the device configuration.
0	Disables the Watchdog Timer if it was enabled in software.

Bits 12:8 – RUNDIV[4:0] WDT Run Mode Postscaler Status bits(3)

Value	Description
11111	Divide by 2 ^ 31 = 2,147,483,648
11110	Divide by 2 ^ 30 = 1,073,741,824
	...
00001	Divide by 2 ^ 1, 2
00000	Divide by 2 ^ 0, 1

Bits 7:6 – CLKSEL[1:0] WDT Run Mode Clock Select Status bits(3,5)

Value	Description
11	LPRC Oscillator
10	FRC Oscillator
01	Reserved
00	SYSCLK

Bits 5:1 – SLPDIV[4:0] Sleep and Idle Mode WDT Postscaler Status bits(3)

Value	Description
11111	Divide by 2 ^ 31 = 2,147,483,648

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Value	Description
11110	Divide by 2 ^ 30 = 1,073,741,824 ...
00001	Divide by 2 ^ 1, 2
00000	Divide by 2 ^ 0, 1

Bit 0 – WDTWINEN Watchdog Timer Window Enable bit(4)

Value	Description
1	Enables Window mode.
0	Disables Window mode.

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31.7.2. Watchdog Timer Control Register High

Name: WDTCONH

Bit	15	14	13	12	11	10	9	8
	WDTCLRKEY[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WDTCLRKEY[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WDTCLRKEY[15:0] Watchdog Timer Clear Key bits
To clear the Watchdog Timer and prevent a time-out, the software must write the value 0x5743 to this location using a single 16-bit write.

31.8. JTAG Interface

The dsPIC33CDVL256MC506 family devices implement a JTAG interface, which supports boundary scan device testing. The JTAG interface only supports boundary scan; programming is not supported.

Note: Refer to **"Programming and Diagnostics"** (www.microchip.com/DS70000608) in the *"dsPIC33/PIC24 Family Reference Manual"* for further information on usage, configuration and operation of the JTAG interface.

31.9. In-Circuit Serial Programming™ (ICSP™)

The dsPIC33CDVL256MC506 family devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the *"dsPIC33CDVL256MC506 Family Flash Programming Specification"* (www.microchip.com/DS70005446) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGC1 and PGD1
- PGC2 and PGD2
- PGC3 and PGD3

31.10. In-Circuit Debugger

When a supported emulator is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGCx (Emulation/Debug Clock) and PGDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGC1 and PGD1
- PGC2 and PGD2
- PGC3 and PGD3

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To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, V_{DD}, V_{SS} and the PGCx/PGDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two or five I/O pins (PGCx and PGDx).

31.11. Code Protection and CodeGuard™ Security

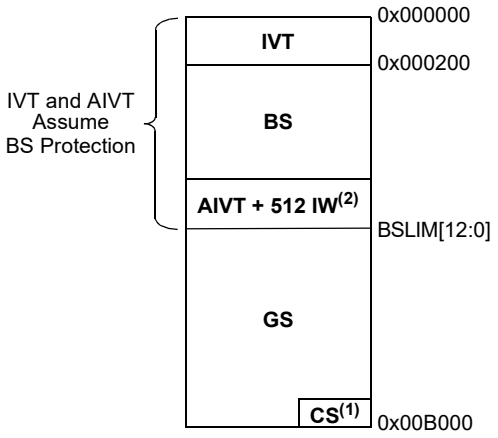
dsPIC33CDVL256MC506 family devices offer multiple levels of security for protecting individual intellectual property. The program Flash protection can be broken up into three segments: Boot Segment (BS), General Segment (GS) and Configuration Segment (CS). The Boot Segment has the highest security privilege and can be thought to have limited restrictions when accessing other segments. The General Segment has the least security and is intended for the end user system code. The Configuration Segment contains only the device user configuration data, which are located at the end of the program memory space.

The code protection features are controlled by the Configuration registers, FSEC and FBSLIM. The FSEC register controls the code-protect level for each segment and whether that segment is write-protected. The size of BS and GS will depend on the BSLIM[12:0] bits setting and whether the Alternate Interrupt Vector Table (AIVT) is enabled. The BSLIM[12:0] bits define the number of pages for BS, with each page containing 1024 IW. The smallest BS size is one page, which will consist of the Interrupt Vector Table (IVT) and 512 IW of code protection.

If the AIVT is enabled, the last page of BS will contain the AIVT and will not contain any BS code. With AIVT enabled, the smallest BS size is now two pages (2048 IW), with one page for the IVT and BS code, and the other page for the AIVT. Write protection of the BS does not cover the AIVT. The last page of BS can always be programmed or erased by BS code. The General Segment will start at the next page and will consume the rest of the program Flash, except for the Flash Configuration Words. The IVT will assume GS security only if BS is not enabled. The IVT is protected from being programmed or page erased when either security segment has enabled write protection.

The different device security segments are shown in Figure 31-3. Here, all three segments are shown but are not required. If only basic code protection is required, then GS can be enabled independently or combined with CS, if desired.

Figure 31-3. Security Segments Example



Note 1: If CS is write-protected, the last page (GS + CS) of program memory will be protected from an erase condition.

2: The last half (256 IW) of the last page of BS is unusable program memory.

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32. Instruction Set Summary

Note: This data sheet summarizes the features of the dsPIC33CDVL256MC506 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"16-Bit MCU and DSC Programmer's Reference Manual"* (www.microchip.com/DS70000157).

The dsPIC33C instruction set is almost identical to that of the dsPIC30F and dsPIC33F.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- DSP operations
- Control operations

Table 32-1 lists the general symbols used in describing the instructions.

The dsPIC33 instruction set summary in Table 32-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register 'Wb' without any address modifier
- The second source operand, which is typically a register 'Ws' with or without an address modifier
- The destination of the result, which is typically a register 'Wd' with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value 'f'
- The destination, which could be either the file register 'f' or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register 'Wb')

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register 'Wb' without any address modifier
- The second source operand, which is a literal value

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- The destination of the result (only if not the same as the first source operand), which is typically a register 'Wd' with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write-back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register 'Wn' or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the eight MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed. In these cases, the execution takes multiple instruction cycles, with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Table 32-1. Symbols Used in Opcode Descriptions

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
a ∈ {b, c, d}	a is selected from the set of values b, c, d
[n:m]	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator Write-Back Destination Address register ∈ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word-addressed instructions) ∈ {0...15}
Note: In dsPIC33CDVL256MC506 devices, read and Read-Modify-Write (RMW) operations on non-CPU Special Function Registers require an additional cycle when compared to dsPIC30F, dsPIC33F, PIC24F and PIC24H devices.	

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Table 32-1. Symbols Used in Opcode Descriptions (continued)

Field	Description
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x0000...0x1FFF}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {0...15}
lit5	5-bit unsigned literal ∈ {0...31}
lit8	8-bit unsigned literal ∈ {0...255}
lit10	10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {0...16384}
lit16	16-bit unsigned literal ∈ {0...65535}
lit23	23-bit unsigned literal ∈ {0...8388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512...511}
Slit16	16-bit signed literal ∈ {-32768...32767}
Slit6	6-bit signed literal ∈ {-16...16}
Wb	Base W register ∈ {W0...W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier Working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier Working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 Working registers ∈ {W0...W15}
Wnd	One of 16 Destination Working registers ∈ {W0...W15}
Wns	One of 16 Source Working registers ∈ {W0...W15}
WREG	W0 (Working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] }
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4...W7}
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4...W7}

Note: In dsPIC33CDVL256MC506 devices, read and Read-Modify-Write (RMW) operations on non-CPU Special Function Registers require an additional cycle when compared to dsPIC30F, dsPIC33F, PIC24F and PIC24H devices.

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Table 32-2. Instruction Set Overview

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(1)	Status Flags Affected
1	ADD	ADD	Acc	Add Accumulators	1	1	OA,OB,SA,SB
		ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD	f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD	Wso,#Slit4,Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BFEXT	BFEXT	bit4,wid5,Ws,Wb	Bit Field Extract from Ws to Wb	2	2	None
		BFEXT	bit4,wid5,f,Wb	Bit Field Extract from f to Wb	2	2	None
7	BFINS	BFINS	bit4,wid5,Wb,Ws	Bit Field Insert from Wb into Ws	2	2	None
		BFINS	bit4,wid5,Wb,f	Bit Field Insert from Wb into f	2	2	None
		BFINS	bit4,wid5,lit8,Ws	Bit Field Insert from #lit8 to Ws	2	2	None
8	BOOTSWP	BOOTSWP		Swap the Active and Inactive Program Flash Space	1	2	None

Notes:

1. Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2. For dsPIC33CDVL256MC506 devices, the divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times.

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Table 32-2. Instruction Set Overview (continued)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles[1]	Status Flags Affected
9	BRA	BRA	C,Expr	Branch if Carry	1	1 (4)/1	None
		BRA	GE,Expr	Branch if Greater Than or Equal	1	1 (4)/1	None
		BRA	GEU,Expr	Branch if unsigned Greater Than or Equal	1	1 (4)/1	None
		BRA	GT,Expr	Branch if Greater Than	1	1 (4)/1	None
		BRA	GTU,Expr	Branch if Unsigned Greater Than	1	1 (4)/1	None
		BRA	LE,Expr	Branch if Less Than or Equal	1	1 (4)/1	None
		BRA	LEU,Expr	Branch if Unsigned Less Than or Equal	1	1 (4)/1	None
		BRA	LT,Expr	Branch if Less Than	1	1 (4)/1	None
		BRA	LTU,Expr	Branch if Unsigned Less Than	1	1 (4)/1	None
		BRA	N,Expr	Branch if Negative	1	1 (4)/1	None
		BRA	NC,Expr	Branch if Not Carry	1	1 (4)/1	None
		BRA	NN,Expr	Branch if Not Negative	1	1 (4)/1	None
		BRA	NOV,Expr	Branch if Not Overflow	1	1 (4)/1	None
		BRA	NZ,Expr	Branch if Not Zero	1	1 (4)/1	None
		BRA	OA,Expr	Branch if Accumulator A Overflow	1	1 (4)/1	None
		BRA	OB,Expr	Branch if Accumulator B Overflow	1	1 (4)/1	None
		BRA	OV,Expr	Branch if Overflow	1	1 (4)/1	None
		BRA	SA,Expr	Branch if Accumulator A Saturated	1	1 (4)/1	None
		BRA	SB,Expr	Branch if Accumulator B Saturated	1	1 (4)/1	None
		BRA	Expr	Branch Unconditionally	1	4/2	None
		BRA	Z,Expr	Branch if Zero	1	1 (4)/1	None
		BRA	Wn	Computed Branch	1	4	None
10	BREAK	BREAK		Stop User Code Execution	1	1	None
11	BSET	BSET	f,#bit4	Bit Set f	1	1	None
			Ws,#bit4	Bit Set Ws	1	1	None
12	BSW	BSW.C	Ws,Wb	Write C Bit to Ws[Wb]	1	1	None
		BSW.Z	Ws,Wb	Write Z Bit to Ws[Wb]	1	1	None
13	BTG	BTG	f,#bit4	Bit Toggle f	1	1	None
		BTG	Ws,#bit4	Bit Toggle Ws	1	1	None
14	BTSC	BTSC	f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
		BTSC	Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
15	BTSS	BTSS	f,#bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS	Ws,#bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None

Notes:

1. Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2. For dsPIC33CDVL256MC506 devices, the divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times.

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Table 32-2. Instruction Set Overview (continued)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(1)	Status Flags Affected
16	BTST	BTST	f,#bit4	Bit Test f	1	1	Z
		BTST.C	Ws,#bit4	Bit Test Ws to C	1	1	C
		BTST.Z	Ws,#bit4	Bit Test Ws to Z	1	1	Z
		BTST.C	Ws,Wb	Bit Test Ws[Wb] to C	1	1	C
		BTST.Z	Ws,Wb	Bit Test Ws[Wb] to Z	1	1	Z
17	BTSTS	BTSTS	f,#bit4	Bit Test then Set f	1	1	Z
		BTSTS.C	Ws,#bit4	Bit Test Ws to C, then Set	1	1	C
		BTSTS.Z	Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z
18	CALL	CALL	lit23	Call Subroutine	2	4/(2)	SFA
		CALL	Wn	Call Indirect Subroutine	1	4(2)	SFA
		CALL.L	Wn	Call Indirect Subroutine (long address)	1	4(2)	SFA
19	CLR	CLR	f	f = 0x0000	1	1	None
		CLR	WREG	WREG = 0x0000	1	1	None
		CLR	Ws	Ws = 0x0000	1	1	None
		CLR	Acc,Wx,Wxd,Wy,Wyd,AWB	Clear Accumulator	1	1	OA,OB,SA,SB
20	CLRWDT	CLRWDT		Clear Watchdog Timer	1	1	WDTO,Sleep
21	COM	COM	f	f = f	1	1	N,Z
		COM	f,WREG	WREG = f	1	1	N,Z
		COM	Ws,Wd	Wd = Ws	1	1	N,Z
22	CP	CP	f	Compare f with WREG	1	1	C,DC,N,OV,Z
		CP	Wb,#lit8	Compare Wb with lit8	1	1	C,DC,N,OV,Z
		CP	Wb,Ws	Compare Wb with Ws (Wb – Ws)	1	1	C,DC,N,OV,Z
23	CP0	CP0	f	Compare f with 0x0000	1	1	C,DC,N,OV,Z
		CP0	Ws	Compare Ws with 0x0000	1	1	C,DC,N,OV,Z
24	CPB	CPB	f	Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,#lit8	Compare Wb with lit8, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,Ws	Compare Wb with Ws, with Borrow (Wb – Ws – C)	1	1	C,DC,N,OV,Z
25	CPSEQ	CPSEQ	Wb,Wn	Compare Wb with Wn, Skip if =	1	1 (2 or 3)	None
	CPBEQ	CPBEQ	Wb,Wn,Expr	Compare Wb with Wn, Branch if =	1	1 (5)	None
26	CPSGT	CPSGT	Wb,Wn	Compare Wb with Wn, Skip if >	1	1 (2 or 3)	None
	CPBGT	CPBGT	Wb,Wn,Expr	Compare Wb with Wn, Branch if >	1	1 (5)	None
27	CPSLT	CPSLT	Wb,Wn	Compare Wb with Wn, Skip if <	1	1 (2 or 3)	None
		CPBLT	Wb,Wn,Expr	Compare Wb with Wn, Branch if <	1	1 (5)	None

Notes:

1. Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2. For dsPIC33CDVL256MC506 devices, the divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times.

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Table 32-2. Instruction Set Overview (continued)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles[1]	Status Flags Affected
28	CPSNE	CPSNE	Wb,Wn	Compare Wb with Wn, Skip if ≠	1	1 (2 or 3)	None
		CPBNE	Wb,Wn,Expr	Compare Wb with Wn, Branch if ≠	1	1 (5)	None
29	CTXTSWP	CTXTSWP	#lit3	Switch CPU Register Context to Context Defined by lit3	1	2	None
30	CTXTSWP	CTXTSWP	Wn	Switch CPU Register Context to Context Defined by Wn	1	2	None
31	DAW.B	DAW.B	Wn	Wn = Decimal Adjust Wn	1	1	C
32	DEC	DEC	f	f = f – 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws – 1	1	1	C,DC,N,OV,Z
33	DEC2	DEC2	f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws – 2	1	1	C,DC,N,OV,Z
34	DISI	DISI	#lit14	Disable Interrupts for k Instruction Cycles	1	1	None
35	DIVF[2]	DIVF	Wm,Wn	Signed 16/16-Bit Fractional Divide	1	18/6	N,Z,C,OV
36	DIV.S[2]	DIV.S	Wm,Wn	Signed 16/16-Bit Integer Divide	1	18/6	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-Bit Integer Divide	1	18/6	N,Z,C,OV
37	DIV.U[2]	DIV.U	Wm,Wn	Unsigned 16/16-Bit Integer Divide	1	18/6	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-Bit Integer Divide	1	18/6	N,Z,C,OV
38	DIVF2[2]	DIVF2	Wm,Wn	Signed 16/16-Bit Fractional Divide (W1:W0 preserved)	1	6	N,Z,C,OV
39	DIV2.S[3]	DIV2.S	Wm,Wn	Signed 16/16-Bit Integer Divide (W1:W0 preserved)	1	6	N,Z,C,OV
		DIV2.SD	Wm,Wn	Signed 32/16-Bit Integer Divide (W1:W0 preserved)	1	6	N,Z,C,OV
40	DIV2.U[2]	DIV2.U	Wm,Wn	Unsigned 16/16-Bit Integer Divide (W1:W0 preserved)	1	6	N,Z,C,OV
		DIV2.UD	Wm,Wn	Unsigned 32/16-Bit Integer Divide (W1:W0 preserved)	1	6	N,Z,C,OV
41	DO	DO	#lit15,Expr	Do Code to PC + Expr, lit15 + 1 Times	2	2	None
		DO	Wn,Expr	Do code to PC + Expr, (Wn) + 1 Times	2	2	None

Notes:

1. Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2. For dsPIC33CDVL256MC506 devices, the divide instructions must be preceded with a "`REPEAT #5`" instruction, such that they are executed six consecutive times.

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Table 32-2. Instruction Set Overview (continued)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles[1]	Status Flags Affected
42	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
43	EDAC	EDAC	Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
44	EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
46	FBCL	FBCL	Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	C
47	FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	C
48	FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	C
49	FLIM	FLIM	Wb, Ws	Force Data (Upper and Lower) Range Limit without Limit Excess Result	1	1	N,Z,OV
		FLIM.V	Wb, Ws, Wd	Force Data (Upper and Lower) Range Limit with Limit Excess Result	1	1	N,Z,OV
50	GOTO	GOTO	Expr	Go to Address	2	4/2	None
		GOTO	Wn	Go to Indirect	1	4/2	None
		GOTO.L	Wn	Go to Indirect (long address)	1	4/2	None
51	INC	INC	f	f = f + 1	1	1	C,DC,N,OV,Z
		INC	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
52	INC2	INC2	f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2	f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2	Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
53	IOR	IOR	f	f = f .IOR. WREG	1	1	N,Z
		IOR	f,WREG	WREG = f .IOR. WREG	1	1	N,Z
		IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
54	LAC	LAC	Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		LAC.D	Wso, #Slit4, Acc	Load Accumulator Double	1	2	OA,SA,OB,SB
56	LNK	LNK	#lit14	Link Frame Pointer	1	1	SFA
57	LSR	LSR	f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z

Notes:

1. Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2. For dsPIC33CDVL256MC506 devices, the divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times.

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Table 32-2. Instruction Set Overview (continued)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles[1]	Status Flags Affected
58	MAC	MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB	Multiply and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
		MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
59	MAX	MAX	Acc	Force Data Maximum Range Limit	1	1	N,OV,Z
		MAX.V	Acc, Wnd	Force Data Maximum Range Limit with Result	1	1	N,OV,Z
60	MIN	MIN	Acc	If Accumulator A Less than B Load Accumulator with B or vice versa	1	1	N,OV,Z
		MIN.V	Acc, Wd	If Accumulator A Less than B Accumulator Force Minimum Data Range Limit with Limit Excess Result	1	1	N,OV,Z
		MINZ	Acc	Accumulator Force Minimum Data Range Limit	1	1	N,OV,Z
		MINZ.V	Acc, Wd	Accumulator Force Minimum Data Range Limit with Limit Excess Result	1	1	N,OV,Z
61	MOV	MOV	f,Wn	Move f to Wn	1	1	None
		MOV	f	Move f to f	1	1	None
		MOV	f,WREG	Move f to WREG	1	1	None
		MOV	#lit16,Wn	Move 16-Bit Literal to Wn	1	1	None
		MOV.b	#lit8,Wn	Move 8-Bit Literal to Wn	1	1	None
		MOV	Wn,f	Move Wn to f	1	1	None
		MOV	Wso,Wdo	Move Ws to Wd	1	1	None
		MOV	WREG,f	Move WREG to f	1	1	None
		MOV.D Wns,Wd		Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws,Wnd		Move Double from Ws to W(nd + 1):W(nd)	1	2	None
62	MOVPAG	MOVPAG	#lit10,DSRPAG	Move 10-Bit Literal to DSRPAG	1	1	None
		MOVPAG	#lit8,TBLPAG	Move 8-Bit Literal to TBLPAG	1	1	None
		MOVPAG	Ws, DSRPAG	Move Ws[9:0] to DSRPAG	1	1	None
		MOVPAG	Ws, TBLPAG	Move Ws[7:0] to TBLPAG	1	1	None
64	MOVSAC	MOVSAC	Acc,Wx,Wxd,Wy,Wyd,AWB	Prefetch and Store Accumulator	1	1	None

Notes:

1. Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2. For dsPIC33CDVL256MC506 devices, the divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times.

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Table 32-2. Instruction Set Overview (continued)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(1)	Status Flags Affected
65	MPY	MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
66	MPY.N	MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	-(Multiply Wm by Wn) to Accumulator	1	1	None
67	MSC	MSC Wm*Wm,Acc,Wx,Wxd, Wy,Wyd,AWB	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB

Notes:

1. Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2. For dsPIC33CDVL256MC506 devices, the divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times.

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Table 32-2. Instruction Set Overview (continued)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles[1]	Status Flags Affected
68	MUL	MUL.SS	Wb,Ws,Wnd	{Wnd + 1, Wnd} = Signed(Wb) * Signed(Ws)	1	1	None
		MUL.SS	Wb,Ws,Acc	Accumulator = Signed(Wb) * Signed(Ws)	1	1	None
		MUL.SU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = Signed(Wb) * Unsigned(Ws)	1	1	None
		MUL.SU	Wb,Ws,Acc	Accumulator = Signed(Wb) * Unsigned(Ws)	1	1	None
		MUL.SU	Wb,#lit5,Acc	Accumulator = Signed(Wb) * Unsigned(lit5)	1	1	None
		MUL.US	Wb,Ws,Wnd	{Wnd + 1, Wnd} = Unsigned(Wb) * Signed(Ws)	1	1	None
		MUL.US	Wb,Ws,Acc	Accumulator = Unsigned(Wb) * Signed(Ws)	1	1	None
		MUL.UU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = Unsigned(Wb) * Unsigned(Ws)	1	1	None
		MUL.UU	Wb,#lit5,Acc	Accumulator = Unsigned(Wb) * Unsigned(lit5)	1	1	None
		MUL.UU	Wb,Ws,Acc	Accumulator = Unsigned(Wb) * Unsigned(Ws)	1	1	None
		MULW.SS	Wb,Ws,Wnd	Wnd = Signed(Wb) * Signed(Ws)	1	1	None
		MULW.SU	Wb,Ws,Wnd	Wnd = Signed(Wb) * Unsigned(Ws)	1	1	None
		MULW.US	Wb,Ws,Wnd	Wnd = Unsigned(Wb) * Signed(Ws)	1	1	None
		MULW.UU	Wb,Ws,Wnd	Wnd = Unsigned(Wb) * Unsigned(Ws)	1	1	None
		MUL.SU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = Signed(Wb) * Unsigned(lit5)	1	1	None
		MUL.SU	Wb,#lit5,Wnd	Wnd = Signed(Wb) * Unsigned(lit5)	1	1	None
		MUL.UU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = Unsigned(Wb) * Unsigned(lit5)	1	1	None
		MUL.UU	Wb,#lit5,Wnd	Wnd = Unsigned(Wb) * Unsigned(lit5)	1	1	None
		MUL	f	W3:W2 = f * WREG	1	1	None

Notes:

1. Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2. For dsPIC33CDVL256MC506 devices, the divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times.

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Table 32-2. Instruction Set Overview (continued)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(1)	Status Flags Affected
69	NEG	NEG	Acc	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG	f	f = f + 1	1	1	C,DC,N,OV,Z
		NEG	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		NEG	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
70	NOP	NOP		No Operation	1	1	None
		NOPR		No Operation	1	1	None
71	NORM	NORM	Acc, Wd	Normalize Accumulator	1	1	N,OV,Z
72	POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		POP.S		Pop Shadow Registers	1	1	All
73	PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S		Push Shadow Registers	1	1	None
74	PWRSAV	PWRSAV #lit1		Go into Sleep or Idle mode	1	1	WDTO,Sleep
75	RCALL	RCALL	Expr	Relative Call	1	4/2 (2)	SFA
		RCALL	Wn	Computed Call	1	4/2 (2)	SFA
76	REPEAT	REPEAT	#lit15	Repeat Next Instruction lit15 + 1 Times	1	1	None
		REPEAT	Wn	Repeat Next Instruction (Wn) + 1 Times	1	1	None
77	RESET	RESET		Software Device Reset	1	1	None
78	RETFIE	RETFIE		Return from Interrupt	1	6 (5)/3 (2)	SFA
79	RETLW	RETLW	#lit10,Wn	Return with Literal in Wn	1	6 (5)/3 (2)	SFA
80	RETURN	RETURN		Return from Subroutine	1	6 (5)/3 (2)	SFA
81	RLC	RLC	f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
		RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z
82	RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z

Notes:

1. Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2. For dsPIC33CDVL256MC506 devices, the divide instructions must be preceded with a "`REPEAT #5`" instruction, such that they are executed six consecutive times.

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Table 32-2. Instruction Set Overview (continued)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(1)	Status Flags Affected
83	RRC	RRC	f	f = Rotate Right through Carry f	1	1	C,N,Z
		RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z
		RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z
84	RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	f,WREG	WREG = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N,Z
85	SAC	SAC	Acc,#Slit4,Wdo	Store Accumulator	1	1	None
		SAC.R	Acc,#Slit4,Wdo	Store Rounded Accumulator	1	1	None
		SAC.D	#Slit4, Wdo	Store Accumulator Double	1	1	None
86	SE	SE	Ws,Wnd	Wnd = Sign-Extended Ws	1	1	C,N,Z
87	SETM	SETM	f	f = 0xFFFF	1	1	None
		SETM	WREG	WREG = 0xFFFF	1	1	None
		SETM	Ws	Ws = 0xFFFF	1	1	None
88	SFTAC	SFTAC	Acc,Wn	Arithmetic Shift Accumulator by (Wn)	1	1	OA,OB,OAB, SA,SB,SAB
		SFTAC	Acc,#Slit6	Arithmetic Shift Accumulator by Slit6	1	1	OA,OB,OAB, SA,SB,SAB
89	SL	SL	f	f = Left Shift f	1	1	C,N,OV,Z
		SL	f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL	Ws,Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
91	SUB	SUB	Acc	Subtract Accumulators	1	1	OA,OB,OAB, SA,SB,SAB
		SUB	f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB	f,WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB	#lit10,Wn	Wn = Wn – lit10	1	1	C,DC,N,OV,Z
		SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
92	SUBB	SUBB	f	f = f – WREG – (C)	1	1	C,DC,N,OV,Z
		SUBB	f,WREG	WREG = f – WREG – (C)	1	1	C,DC,N,OV,Z
		SUBB	#lit10,Wn	Wn = Wn – lit10 – (C)	1	1	C,DC,N,OV,Z
		SUBB	Wb,Ws,Wd	Wd = Wb – Ws – (C)	1	1	C,DC,N,OV,Z
		SUBB	Wb,#lit5,Wd	Wd = Wb – lit5 – (C)	1	1	C,DC,N,OV,Z

Notes:

1. Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2. For dsPIC33CDVL256MC506 devices, the divide instructions must be preceded with a "`REPEAT #5`" instruction, such that they are executed six consecutive times.

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Table 32-2. Instruction Set Overview (continued)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(1)	Status Flags Affected
93	SUBR	SUBR	f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	f,WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
94	SUBBR	SUBBR	f	f = WREG – f – (C)	1	1	C,DC,N,OV,Z
		SUBBR	f,WREG	WREG = WREG – f – (C)	1	1	C,DC,N,OV,Z
		SUBBR	Wb,Ws,Wd	Wd = Ws – Wb – (C)	1	1	C,DC,N,OV,Z
		SUBBR	Wb,#lit5,Wd	Wd = lit5 – Wb – (C)	1	1	C,DC,N,OV,Z
95	SWAP	SWAP.b	Wn	Wn = Nibble Swap Wn	1	1	None
		SWAP	Wn	Wn = Byte Swap Wn	1	1	None
96	TBLRDH	TBLRDH	Ws,Wd	Read Prog[23:16] to Wd[7:0]	1	5/3 (2)	None
97	TBLRDL	TBLRDL	Ws,Wd	Read Prog[15:0] to Wd	1	5/3 (2)	None
98	TBLWTH	TBLWTH	Ws,Wd	Write Ws[7:0] to Prog[23:16]	1	2	None
99	TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog[15:0]	1	2	None
101	ULNK	ULNK		Unlink Frame Pointer	1	1	SFA
104	XOR	XOR	f	f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
105	ZE	ZE	Ws,Wnd	Wnd = Zero-Extend Ws	1	1	C,Z,N

Notes:

1. Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2. For dsPIC33CDVL256MC506 devices, the divide instructions must be preceded with a "`REPEAT #5`" instruction, such that they are executed six consecutive times.

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33. Development Support

Move a design from concept to production in record time with Microchip's award-winning development tools. Microchip tools work together to provide state-of-the-art debugging for any project with easy-to-use Graphical User Interfaces (GUIs) in our free MPLAB® X and Atmel Studio Integrated Development Environments (IDEs), and our code generation tools. Providing the ultimate ease-of-use experience, Microchip's line of programmers, debuggers, and emulators work seamlessly with our software tools. Microchip development boards help evaluate the best silicon device for an application, while our line of third-party tools rounds out our comprehensive development tool solutions.

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34. Electrical Characteristics

This section provides an overview of the dsPIC33CDVL256MC506 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33CDVL256MC506 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Table 34-1. Absolute Maximum Ratings(1)

Parameter	Rating
Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on V_{DD} with respect to V_{SS}	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to V_{SS}(3)	-0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS}(3)	-0.3V to +5.5V
Maximum current out of V_{SS} pin	300 mA
Maximum current into V_{DD} pin(2)	300 mA
Maximum current sunk/sourced by any regular I/O pin	15 mA
Maximum current sunk/sourced by an I/O pin with increased current drive strength (RB1, RC8, RC9 and RD8)	25 mA
Maximum current sunk by a group of I/Os between two V_{SS} pins(4)	75 mA
Maximum current sourced by a group of I/Os between two V_{DD} pins(4)	75 mA
Maximum current sunk by all I/Os(2,5)	200 mA
Maximum current sourced by all I/Os(2,5)	200 mA

Notes:

1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those, or any other conditions above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Maximum allowable current is a function of device maximum power dissipation (see **DC Characteristics**).
3. See the Pin Diagrams section for the 5V tolerant pins.
4. Not applicable to AV_{DD} and AV_{SS} pins.
5. For 28-pin packages, the maximum current sunk/sourced by all I/Os is limited to 150 mA.

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34.1. DC Characteristics

Table 34-2. dsPIC33CDVL256MC506 Family Operating Conditions

V_{DD} Range	Temperature Range	Maximum CPU Clock Frequency
3.0V to 3.6V	-40°C to +125°C	100 MHz

Table 34-3. Thermal Operating Conditions

Rating	Symbol	Min.	Max.	Unit
Industrial Temperature Devices				
Operating Junction Temperature Range	T_J	-40	+125	°C
Operating Ambient Temperature Range	T_A	-40	+85	°C
Extended Temperature Devices				
Operating Junction Temperature Range	T_J	-40	+150	°C
Operating Ambient Temperature Range	T_A	-40	+125	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$	P_D	$P_{INT} + P_{I/O}$		W
I/O Pin Power Dissipation: $I/O = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$				
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$		W

Table 34-4. Thermal Packaging Characteristics[1]

Package	Symbol	Typ.	Unit
64L VGQFN 9x9x0.927 mm	θ_{JA}	18.567	°C/W
64L VQFN 8x8x0.9 mm	θ_{JA}	19.691	°C/W

Note:

1. Junction to ambient thermal resistance, Theta-$_{JA}$ (θ_{JA}) numbers are achieved by package simulations.

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Table 34-5. Operating Voltage Specifications

Operating Conditions (unless otherwise stated): **-40°C ≤ T_A ≤ +85°C for Industrial** **-40°C ≤ T_A ≤ +125°C for Extended**						
Param No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
DC10	V_{DD}	**Supply Voltage**	3.0	3.6	V	
DC11	AV_{DD}	**Supply Voltage**	Greater of: V_{DD} – 0.3 or 3.0	Lesser of: V_{DD} + 0.3 or 3.6	V	The difference between AV_{DD} supply and V_{DD} supply must not exceed ±300 mV at all times, including during device power-up
DC16	V_{POR}	**V_{DD} Start Voltage** to Ensure Internal Power-on Reset Signal	—	V_{SS}	V	
DC17	SV_{DD}	**V_{DD} Rise Rate** to Ensure Internal Power-on Reset Signal	0.03	—	V/ms	0V-3V in 100 ms
BO10	V_{BOR}(1)	**BOR Event** on V_{DD} Transition High-to-Low	2.68	2.99	V	
BO11	V_{POR}	**POR Event** on V_{DD} Transition High-to-Low	—	—	V	V_{DD} **(Notes 2, 3)**

Notes:

1. Device is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$. Analog modules (ADC and comparators) may have degraded performance. The V_{BOR} parameter is for design guidance only and is not tested in manufacturing.
2. If V_{DD} drops below the BO11 value, V_{DD} must be brought down to 0V before ramping the device back up to operation range.

Table 34-6. Operating Current (I_{DD})(2)

Parameter No.	Typ.(1)	Max.	Units	Conditions		
DC20	6.7	10.0	mA	-40°C	3.3V	10 MIPS (N = 1, N2 = 5, N3 = 2, M = 50, F_{VCO} = 400 MHz, F_{PLLO} = 40 MHz)
	6.5	10.0	mA	+25°C		
	7.2	15.0	mA	+85°C		
	9.0	22.0	mA	+125°C		
DC21	8.5	12.5	mA	-40°C	3.3V	20 MIPS (N = 1, N2 = 5, N3 = 1, M = 60, F_{VCO} = 480 MHz, F_{PLLO} = 280 MHz)
	8.3	12.5	mA	+25°C		
	8.9	17.0	mA	+85°C		
	10.7	25.0	mA	+125°C		
DC22	12.5	18.5	mA	-40°C	3.3V	40 MIPS (N = 1, N2 = 3, N3 = 1, M = 60, F_{VCO} = 480 MHz, F_{PLLO} = 160 MHz)
	12.3	18.5	mA	+25°C		
	13.1	20.0	mA	+85°C		
	14.5	28.0	mA	+125°C		
DC23	17.8	22.0	mA	-40°C	3.3V	70 MIPS (N = 1, N2 = 2, N3 = 1, M = 70, F_{VCO} = 560 MHz, F_{PLLO} = 280 MHz)
	17.7	22.0	mA	+25°C		
	18.3	30.0	mA	+85°C		
	20.0	35.0	mA	+125°C		
DC24	22.3	28.0	mA	-40°C	3.3V	90 MIPS (N = 1, N2 = 2, N3 = 1, M = 90, F_{VCO} = 720 MHz, F_{PLLO} = 360 MHz)
	22.0	28.0	mA	+25°C		
	23.0	33.0	mA	+85°C		
	23.5	35.0	mA	+125°C		

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Table 34-6. Operating Current (I_{DD})[2] (continued)

Parameter No.	Typ.[1]	Max.	Units	Conditions		
DC25	21.8	28.0	mA	-40°C	3.3V	100 MIPS (N = 1, N2 = 1, N3 = 1, M = 50, F_{VCO} = 400 MHz, F_{PLLO} = 400 MHz)
	20.7	28.0	mA	+25°C		
	21.4	33.0	mA	+85°C		
	23.0	38.0	mA	+125°C		

Notes:

1. Data in the "Typ." column are for design guidance only and are not tested.
2. I_{DD} is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. Base run current (I_{DD}) is measured as follows:
   - Oscillator is switched to EC+PLL mode in software
   - OSC1 pin is driven with external 8 MHz square wave with levels from 0.3V to V_{DD} – 0.3V
   - OSC2 pin is configured as an I/O in the Configuration Words (OSCIOFNC (FOSC[2]) = `0`)
   - FSCM is disabled (FCKSM[1:0] (FOSC[7:6]) = `01`)
   - Watchdog Timer is disabled (FWDT[15]) = `0` and WDTCONL[15] = `0`)
   - All I/O pins (except OSC1) are configured as outputs and driving low
   - No peripheral modules are operating or being clocked (defined PMDx bits are all '`1`'s)
   - JTAG is disabled (JTAGEN (FICD[5]) = `0`)
   - `NOP` instructions are executed in `while(1)` loop

Table 34-7. Idle Current (I_{IDLE})[2]

Parameter No.	Typ.[1]	Max.	Units	Conditions		
DC30	5.5	7.5	mA	-40°C	3.3V	10 MIPS (N = 1, N2 = 5, N3 = 2, M = 50, F_{VCO} = 400 MHz, F_{PLLO} = 40 MHz)
	5.3	7.5	mA	+25°C		
	5.8	12.5	mA	+85°C		
	7.7	20.0	mA	+125°C		
DC31	6.1	9.0	mA	-40°C	3.3V	20 MIPS (N = 1, N2 = 5, N3 = 1, M = 50, F_{VCO} = 400 MHz, F_{PLLO} = 80 MHz)
	5.8	9.0	mA	+25°C		
	6.5	15.0	mA	+85°C		
	8.2	20.0	mA	+125°C		
DC32	7.6	12.0	mA	-40°C	3.3V	40 MIPS (N = 1, N2 = 3, N3 = 1, M = 60, F_{VCO} = 480 MHz, F_{PLLO} = 160 MHz)
	7.4	12.0	mA	+25°C		
	8.2	15.0	mA	+85°C		
	9.7	22.0	mA	+125°C		
DC33	9.7	15.0	mA	-40°C	3.3V	70 MIPS (N = 1, N2 = 2, N3 = 1, M = 70, F_{VCO} = 660 MHz, F_{PLLO} = 280 MHz)
	9.5	15.0	mA	+25°C		
	10.5	20.0	mA	+85°C		
	11.8	25.0	mA	+125°C		
DC34	11.7	17.0	mA	-40°C	3.3V	90 MIPS (N = 1, N2 = 2, N3 = 1, M = 90, F_{VCO} = 720 MHz, F_{PLLO} = 360 MHz)
	11.6	17.0	mA	+25°C		
	12.2	20.0	mA	+85°C		
	13.8	26.0	mA	+125°C		
DC35	10.1	17.0	mA	-40°C	3.3V	100 MIPS (N = 1, N2 = 1, N3 = 1, M = 50, F_{VCO} = 400 MHz, F_{PLLO} = 400 MHz)
	10.0	17.0	mA	+25°C		
	11.5	22.0	mA	+85°C		
	12.2	28.0	mA	+125°C		

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Table 34-7. Idle Current (I_{IDLE})(2) (continued)

Parameter No.	Typ.(1)	Max.	Units	Conditions

Notes:

1. Data in the "Typ." column are for design guidance only and are not tested.
2. Base Idle current (I_{IDLE}) is measured as follows:
   - Oscillator is switched to EC+PLL mode in software
   - OSC1 pin is driven with external 8 MHz square wave with levels from 0.3V to V_{DD} – 0.3V
   - OSC2 is configured as an I/O in the Configuration Words (OSCIOFNC (FOSC[2]) = 0)
   - FSCM is disabled (FCKSM[1:0] (FOSC[7:6]) = 01)
   - Watchdog Timer is disabled (FWDTEN (FWDT[15]) = 0)
   - All I/O pins (except OSC1) are configured as outputs and driving low
   - No peripheral modules are operating or being clocked (defined PMDx bits are all '1's)
   - JTAG is disabled (JTAGEN (FICD[5]) = 0)
   - Flash in standby with NVMSIDL (NVMCON[12]) = 1

Table 34-8. Power-Down Current (I_{PD})(2)

Parameter No.	Typ.(1)	Max.	Units	Conditions		
DC40	0.285	0.7	mA	-40°C	3.3V	VREGS bit (RCON[8]) = 0, LPWREN bit (VREGCON[15]) = 1
	0.32	1.0	mA	+25°C		
	1.5	5.0	mA	+85°C		
DC41	2.1	—	mA	-40°C	3.3V	VREGS bit (RCON[8]) = 1, LPWREN bit (VREGCON[15]) = 0
	2.0	—	mA	+25°C		
	2.5	—	mA	+85°C		
	4.5	15.0	mA	+125°C(3)		

Notes:

1. Data in the "Typ." column are for design guidance only and are not tested.
2. Base Sleep current (I_{PD}) is measured as follows:
   - CPU core is off, oscillator is configured in EC mode and External Clock is active; OSCI is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
   - CLKO is configured as an I/O input pin in the Configuration Word
   - FSCM is disabled (FCKSM[1:0] (FOSC[7:6]) = 01)
   - All I/O pins are configured as output low
   - $\overline{MCLR}$ = V_{DD}, WDT and FSCM are disabled
   - All peripheral modules are disabled (PMDx bits are all set)
   - The VREGS bit (RCON[8]) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
   - JTAG is disabled
3. The regulators are in High-Power mode, LPWREN (VREGCON[15]) = 0.

Table 34-9. Doze Current (I_{DOZE})

Parameter No.	Typ.(1)	Doze Ratio	Units	Conditions		
DC70	14.1	1:2	mA	-40°C	3.3V	70 MIPS (N = 1, N2 = 2, N3 = 1, M = 70, F_{VCO} = 560 MHz, F_{PLLO} = 280 MHz)
	10.0	1.128	mA			
	14.0	1:2	mA	+25°C		
	9.7	1.128	mA			
	14.3	1:2	mA	+85°C		
	9.4	1.128	mA			
	16.5	1:2	mA	+125°C		
	12.0	1.128	mA			

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Table 34-9. Doze Current (I_{DOZE}) (continued)

Parameter No.	Typ.(1)	Doze Ratio	Units	Conditions		
DC71	16.6	1:2	mA	-40°C	3.3V	100 MIPS (N = 1, N2 = 1, N3 = 1, M = 50, F_{VCO} = 400 MHz, F_{PLLO} = 400 MHz)
	10.4	1.128	mA			
	16.2	1:2	mA	+25°C		
	10.3	1.128	mA			
	16.6	1:2	mA	+85°C		
	11.2	1.128	mA			
	18.5	1:2	mA	+125°C		
	12.5	1.128	mA			

Note:

1. Data in the “Typ.” column are for design guidance only and are not tested.

Table 34-10. Watchdog Timer Delta Current (ΔI_{WDT})(1)

Parameter No.	Typ.	Units	Conditions	
DC61	1	µA	-40°C	3.3V
	2	µA	+25°C	
	4	µA	+85°C	
	11	µA	+125°C	

Note:

1. The ΔI_{WDT} current is the additional current consumed when the module is enabled. This includes the LPRC/BFRC clock current. This current should be added to the base I_{PD} current. All parameters are characterized but not tested during manufacturing.

Table 34-11. PWM Delta Current(1)

Parameter No.	Typ.	Max.	Units	Conditions		
DC100	6.2	6.8	mA	-40°C	3.3V	PWM Output Frequency = 500 kHz, PWM Input (F_{PLLO} = 500 MHz), (V_{CO} = 1000 MHz, PLLFBD = 125)
	6.1	6.7	mA	+25°C		
	6.2	7.4	mA	+85°C		
	7.0	8.6	mA	+125°C		
DC101	5.2	5.9	mA	-40°C	3.3V	PWM Output Frequency = 500 kHz, PWM Input (F_{PLLO} = 400 MHz), (V_{CO} = 400 MHz, PLLFBD = 100)
	5.1	5.6	mA	+25°C		
	5.2	5.7	mA	+85°C		
	5.6	6.2	mA	+125°C		
DC102	2.5	3.8	mA	-40°C	3.3V	PWM Output Frequency = 500 kHz, PWM Input (F_{PLLO} = 200 MHz), (V_{CO} = 200 MHz, PLLFBD = 50)
	2.6	3.8	mA	+25°C		
	2.5	3.8	mA	+85°C		
	2.5	3.8	mA	+125°C		
DC103	1.4	2.0	mA	-40°C	3.3V	PWM Output Frequency = 500 kHz, PWM Input (F_{PLLO} = 100 MHz), (V_{CO} = 100 MHz, PLLFBD = 25)
	1.4	2.0	mA	+25°C		
	1.4	2.0	mA	+85°C		
	1.4	2.0	mA	+125°C		

Note:

1. All parameters are characterized but not tested during manufacturing.

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Table 34-12. ADC Delta Current[1]

Parameter No.	Typ.	Max.	Units	Conditions		
DC120	5.4	6.2	mA	-40°C	3.3V	T_{AD} = 14.3 ns (3.5 Msps conversion rate)
	5.4	6.2	mA	+25°C		
	5.5	6.2	mA	+85°C		
	5.6	6.3	mA	+125°C		

Note:

1. All parameters are characterized but not tested during manufacturing.

Table 34-13. Comparator + DAC Delta Current[1]

Parameter No.	Typ.	Max.	Units	Conditions		
DC130	1.4	1.8	mA	-40°C	3.3V	F_{PLLO} @ 500 MHz
	1.3	1.6	mA	+25°C		
	1.3	1.6	mA	+85°C		
	1.4	1.8	mA	+125°C		

Note:

1. All parameters are characterized but not tested during manufacturing.

Table 34-14. Op Amp Delta Current[1]

Parameter No.	Typ.	Max.	Units	Conditions	
DC140	0.21	1.0	mA	-40°C	3.3V
	0.22	1.0	mA	+25°C	
	0.23	1.0	mA	+85°C	
	0.47	2.0	mA	+125°C	

Note:

1. Listed delta currents are for only one op amp instance. All parameters are characterized but not tested during manufacturing.

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Table 34-15. I/O Pin Input Specifications

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended						
Param No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
DI10	V_{IL}	Input Low-Level Voltage				
		Any I/O Pin and $\overline{MCLR}$	V_{SS}	0.2 V_{DD}	V	
		I/O Pins with SDAx, SCLx	V_{SS}	0.3 V_{DD}	V	SMBus disabled
		I/O Pins with SDAx, SCLx	V_{SS}	0.8	V	SMBus enabled
		I/O Pins with SDAx, SCLx	V_{SS}	0.8	V	SMBus 3.0 enabled
DI20	V_{IH}	Input High-Level Voltage(1)				
		I/O Pins Not 5V Tolerant	0.8 V_{DD}	V_{DD}	V	
		I/O Pins 5V Tolerant and $\overline{MCLR}$	0.8 V_{DD}	5.5	V	
		I/O Pins 5V Tolerant with SDAx, SCLx	0.8 V_{DD}	5.5	V	SMBus disabled
		I/O Pins 5V Tolerant with SDAx, SCLx	2.1	5.5	V	SMBus enabled
		I/O Pins 5V Tolerant with SDAx, SCLx	1.35	V_{DD}	V	SMBus 3.0 enabled
		I/O Pins Not 5V Tolerant with SDAx, SCLx	0.8 V_{DD}	V_{DD}	V	SMBus disabled
		I/O Pins Not 5V Tolerant with SDAx, SCLx	2.1	V_{DD}	V	SMBus enabled
		I/O Pins Not 5V Tolerant with SDAx, SCLx	1.35	V_{DD}	V	SMBus 3.0 enabled
DI30	I_{CNPU}	Input Current with Pull-up Resistor Enabled(2)	175	545	µA	V_{DD} = 3.3V, V_{PIN} = V_{SS}
DI31	I_{CNPD}	Input Current with Pull-Down Resistor Enabled(2)	65	360	µA	V_{DD} = 3.3V, V_{PIN} = V_{DD}
DI50	I_{IL}	Input Leakage Current I/O Pins and $\overline{MCLR}$ Pin	-700	—	nA	V_{PIN} = V_{SS}
			—	700	nA	V_{PIN} = V_{DD}

Notes:

1. See the **"Pin Diagrams"** section for the 5V tolerant I/O pins.
2. Characterized but not tested.

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Table 34-16. I/O Pin Input Injection Current Specifications

Operating Conditions (unless otherwise stated): **3.0V ≤ V_{DD} ≤ 3.6V,** **-40°C ≤ T_A ≤ +85°C for Industrial** **-40°C ≤ T_A ≤ +125°C for Extended**						
Param No.	**Sym**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
DI60a	I_{ICL}	**Input Low Injection Current**	0	-5[1,4]	mA	This parameter applies to all pins
DI60b	I_{ICH}	**Input High Injection Current**	0	+5[2,3,4]	mA	This parameter applies to all pins, except all 5V tolerant pins
DI60c	Σ_{LICT}	**Total Input Injection Current (sum of all I/O and control pins)**	-20[5]	+20[5]	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins $\Sigma (\lvert I_{ICL} \rvert + \lvert I_{ICH} \rvert) \le \Sigma_{LICT}$

Notes:

1. V_{IL} Source < (V_{SS} – 0.3).
2. V_{IH} Source > (V_{DD} + 0.3) for non-5V tolerant pins only.
3. 5V tolerant pins do not have an internal high-side diode to V_{DD} and therefore, cannot tolerate any “positive” input injection current.
4. Injection currents can affect the ADC results.
5. Any number and/or combination of I/O pins, not excluded under I_{ICL} or I_{ICH} conditions, are permitted in the sum.

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Table 34-17. I/O Pin Output Specifications

Operating Conditions (unless otherwise stated): $3.0V \le V_{DD} \le 3.6V$, $-40°C \le T_A \le +85°C$ for Industrial, $-40°C \le T_A \le +125°C$ for Extended					
Param.	**Symbol**	**Characteristic**	**Typ.(1)**	**Units**	**Conditions**
DO10	V_{OL}	Sink Driver Voltage	0.2	V	I_{SINK} = 3.0 mA, V_{DD} = 3.3V
			0.4	V	I_{SINK} = 6.0 mA, V_{DD} = 3.3V
			0.6	V	I_{SINK} = 9.0 mA, V_{DD} = 3.3V
		Sink Driver Voltage for RB1, RC8, RC9, RD8 Pins	0.25	V	I_{SINK} = 6.0 mA, V_{DD} = 3.3V
			0.5	V	I_{SINK} = 12.0 mA, V_{DD} = 3.3V
			0.75	V	I_{SINK} = 18.0 mA, V_{DD} = 3.3V
DO20	V_{OH}	Source Driver Voltage	3.1	V	I_{SOURCE} = 3.0 mA, V_{DD} = 3.3V
			2.9	V	I_{SOURCE} = 6.0 mA, V_{DD} = 3.3V
			2.7	V	I_{SOURCE} = 9.0 mA, V_{DD} = 3.3V
		Source Driver Voltage for RB1, RC8, RC9, RD8 Pins	3.1	V	I_{SOURCE} = 6.0 mA, V_{DD} = 3.3V
			2.8	V	I_{SOURCE} = 12.0 mA, V_{DD} = 3.3V
			2.6	V	I_{SOURCE} = 18.0 mA, V_{DD} = 3.3V

Note:

1. Data in the “Typ.” column are at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

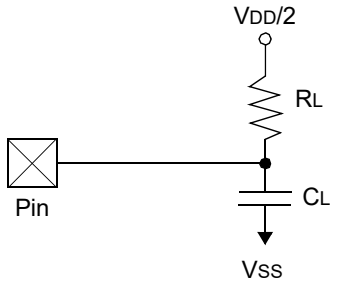
Table 34-18. Program Flash Memory Specifications

Operating Conditions (unless otherwise stated): $3.0V \le V_{DD} \le 3.6V$, $-40°C \le T_A \le +85°C$ for Industrial, $-40°C \le T_A \le +125°C$ for Extended						
Param No.	**Sym**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
Program Flash Memory						
D130	E_P	Cell Endurance	10,000	—	E/W	
D134	T_{RETD}	Characteristic Retention	20	—	Year	
D137a	T_{PE}	Self-Timed Page Erase Time	—	20	ms	
D137b	T_{CE}	Self-Timed Chip Erase Time	—	20	ms	
D138a	T_{WW}	Self-Timed Double-Word Write Cycle Time	—	52.3	µs	6 bytes, data are not all ‘1’s
D138b	T_{RW}	Self-Timed Row Write Cycle Time	—	2.2	ms	384 bytes, data are not all ‘1’s

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34.2. AC Characteristics and Timing Parameters

Figure 34-1. Load Conditions for I/O Specifications



RL = 464Ω
CL = 50 pF

Figure 34-2. I/O Timing Requirements

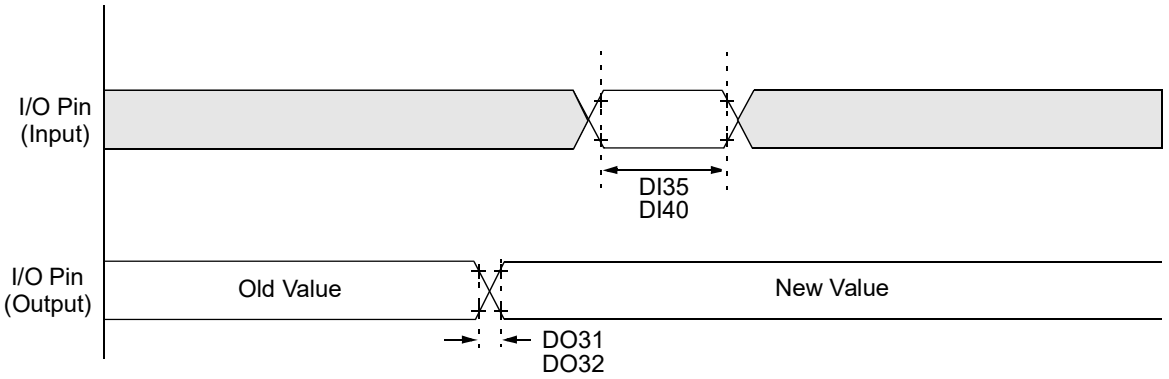


Table 34-19. I/O Timing Requirements

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended					
Param No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**
DO31	$T_{IO}R$	Port Output Rise Time(1)	—	10	ns
DO32	$T_{IO}F$	Port Output Fall Time(1)	—	10	ns
DI35	T_{INP}	INTx Input Pins High or Low Time	20	—	ns
DI40	T_{RPB}	I/O and CNx Inputs High or Low Time	2	—	T_{CY}

Note:

1. This parameter is characterized but not tested in manufacturing.

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Figure 34-3. External Clock Timing

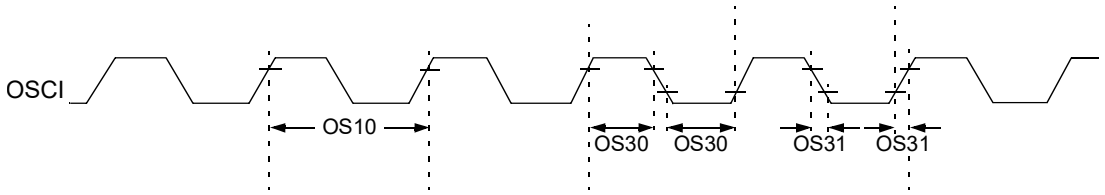


Table 34-20. External Clock Timing Requirements

Operating Conditions (unless otherwise stated): **3.0V ≤ V_{DD} ≤ 3.6V,** **-40°C ≤ T_A ≤ +85°C for Industrial** **-40°C ≤ T_A ≤ +125°C for Extended**						
Param No.	**Sym**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
OS10	F_{IN}	External CLKI Frequency	DC	64	MHz	EC
		Oscillator Crystal Frequency	3.5	10	MHz	XT
			10	32	MHz	HS
OS30	$T_{OS}L$, $T_{OS}H$	External Clock in (OSCI) High or Low Time	0.45 x OS10	0.55 x OS10	ns	EC
OS31	$T_{OS}R$, $T_{OS}F$	External Clock in (OSCI) Rise or Fall Time(1)	—	10	ns	EC

Note:
1. This parameter is characterized but not tested in manufacturing.

Table 34-21. PLL Clock Timing Specifications

Operating Conditions (unless otherwise stated): **3.0V ≤ V_{DD} ≤ 3.6V,** **-40°C ≤ T_A ≤ +85°C for Industrial** **-40°C ≤ T_A ≤ +125°C for Extended**					
Param No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**
OS50	F_{PLLI}	PLL Input Frequency Range	8	64	MHz
OS51	F_{PFP}	Phase Frequency Detector Input Frequency (after first divider)	8	F_{VCO}/16	MHz
OS52	F_{VCO}	VCO Output Frequency	400	1600	MHz
OS53	T_{LOCK}	Lock Time for PLL(1)	—	250	µS

Note:
1. This parameter is characterized but not tested in manufacturing.

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Table 34-22. FRC Oscillator Specifications

Operating Conditions (unless otherwise stated): **3.0V ≤ V_{DD} ≤ 3.6V,** **-40°C ≤ T_A ≤ +85°C for Industrial** **-40°C ≤ T_A ≤ +125°C for Extended**							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(3)**	**Max**	**Units**	**Conditions**
F20	A_{FRC}	FRC Accuracy @ 8 MHz(1,2)	-2.0(4)	—	2.0	%	-40°C ≤ T_A ≤ -5°C
			-1.5	—	1.5	%	-5°C ≤ T_A ≤ +85°C
			-2.0	—	2.0	%	+85°C ≤ T_A ≤ +125°C
F21	T_{FRC}	FRC Oscillator Start-up Time(5)	—	—	15	µS	
F22	S_{TUNE}	OSCTUN Step-Size	—	0.05	—	%/bit	

Notes:

1. To achieve this accuracy, physical stress applied to the microcontroller package (ex., by flexing the PCB) must be kept to a minimum.
2. Frequency is calibrated at +25°C and 3.3V. The TUNx bits can be used to compensate for temperature drift.
3. Data in the "Typ" column are 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
4. Due to the effect of aging, this value may drift by an additional -0.5% over the lifetime of the device.
5. This parameter is characterized but not tested in manufacturing.

Table 34-23. BFRC Oscillator Specifications

Operating Conditions (unless otherwise stated): **3.0V ≤ V_{DD} ≤ 3.6V,** **-40°C ≤ T_A ≤ +85°C for Industrial** **-40°C ≤ T_A ≤ +125°C for Extended**					
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**
F40	A_{BFRC}	BFRC Accuracy @ 8 MHz	-17	17	%

Table 34-24. Internal LPRC Accuracy

Operating Conditions (unless otherwise stated): **3.0V ≤ V_{DD} ≤ 3.6V,** **-40°C ≤ T_A ≤ +85°C for Industrial** **-40°C ≤ T_A ≤ +125°C for Extended**					
Param No.	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
LPRC @ 32.768 kHz					
F21	LPRC	-25	+25	%	-40°C ≤ T_A ≤ 0°C
		-10	+10	%	0°C ≤ T_A ≤ +85°C
		-15	+15	%	+85°C ≤ T_A ≤ +125°C
		-25	+25	%	-40°C ≤ T_A ≤ +125°C

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Figure 34-4. BOR and Master Clear Reset Timing Characteristics

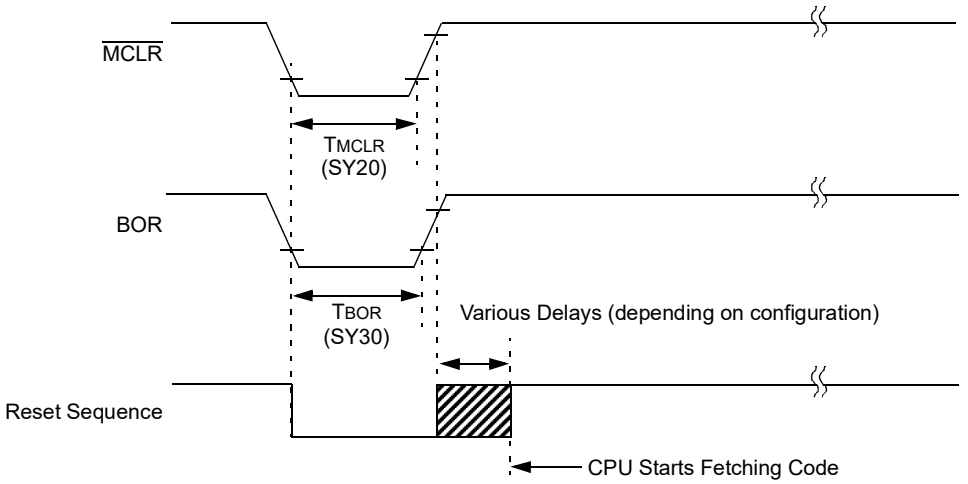


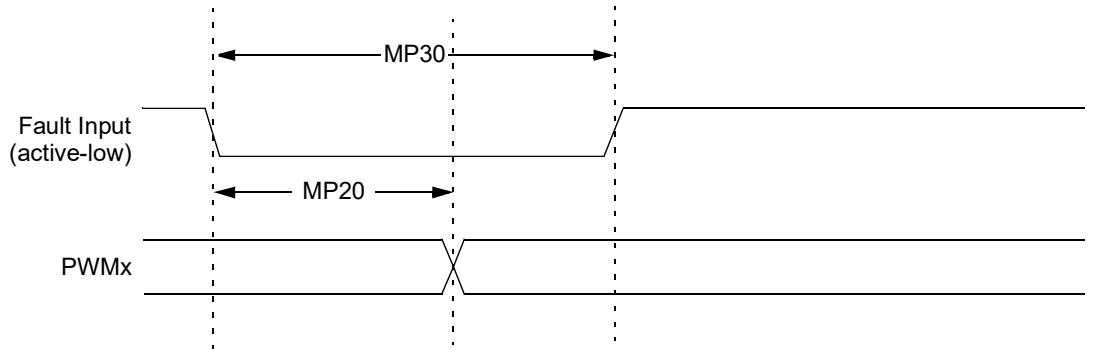
Table 34-25. Reset, Watchdog Timer, Oscillator Start-up Timer Timing Requirements

Operating Conditions (unless otherwise stated): **3.0V ≤ V_{DD} ≤ 3.6V,** **-40°C ≤ T_A ≤ +85°C for Industrial** **-40°C ≤ T_A ≤ +125°C for Extended**							
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SY00	T_{PU}	Power-up Period	—	200	—	µs	FNOSC[2:0] are FRC
SY10	T_{OST}	Oscillator Start-up	—	1024 T_{OSC}	—	—	T_{OSC} = OSCI period
SY13	T_{IOZ}	I/O High-Impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	1.5	—	µs	
SY20	T_{MCLR}	$\overline{MCLR}$ Pulse Width (low)	2	—	—	µs	
SY30	T_{BOR}	BOR Pulse Width (low)	1	—	—	µs	
SY35	T_{FSCM}	Fail-Safe Clock Monitor Delay	—	—	40	µs	
SY37	$T_{OSCDFRC}$	FRC Oscillator Start-up Delay	—	—	15	µs	From POR event
SY38	$T_{OSCDLPRC}$	LPRC Oscillator Start-up Delay	—	—	50	µs	From Reset event

Notes:

1. These parameters are characterized but not tested in manufacturing.
2. Data in the "Typ." column are at 3.3V, +25°C unless otherwise stated.

Figure 34-5. High-Speed PWMx Module Timing Characteristics



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Table 34-26. High-Speed PWMx Module Timing Requirements

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended					
Param No.	Symbol	Characteristic(1)	Min.	Max.	Units
MP10	F_{IN}	PWM Input Frequency	—	500	MHz
MP20	T_{FD}	Fault Input ↓ to PWMx I/O Change	—	26	ns
MP30	T_{FH}	Fault Input Pulse Width	8	—	ns

Note:

1. These parameters are characterized but not tested in manufacturing.

Figure 34-6. SPIx Module Host Mode (CKE = 0) Timing Characteristics

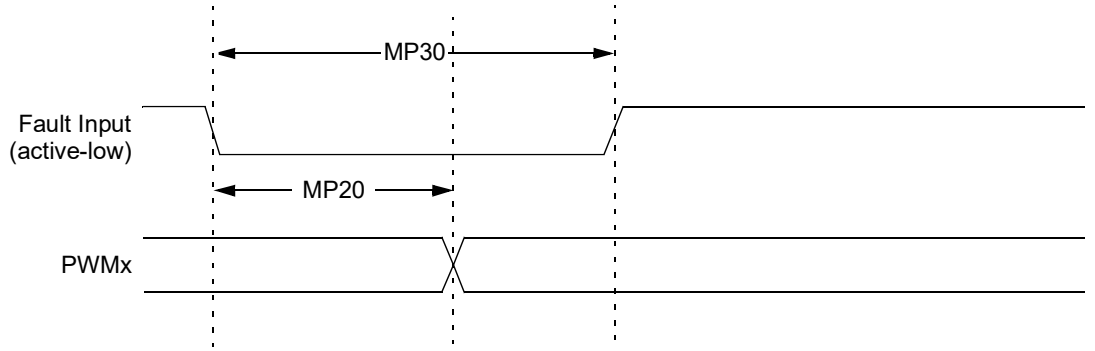
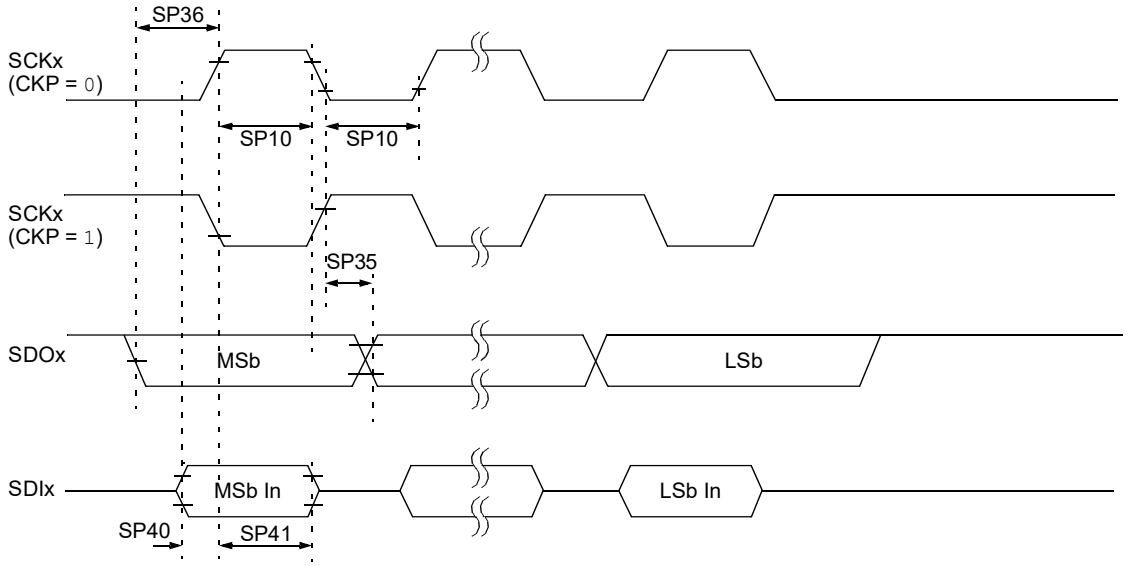


Figure 34-7. SPIx Module Host Mode (CKE = 1) Timing Characteristics



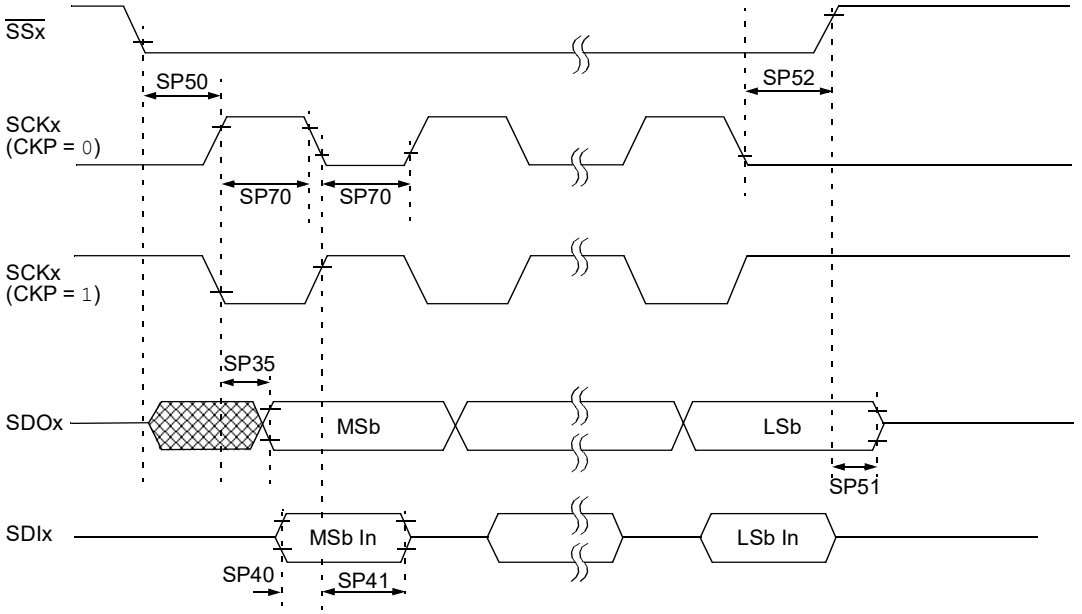
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Table 34-27. SPIx Module Host Mode Timing Requirements

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended					
Param. No.	Symbol	Characteristics(1)	Min	Max	Units
SP10	$T_{SC}L$, $T_{SC}H$	SCKx Output Low or High Time	15	—	ns
SP35	$T_{SC}H2_{DO}V$, $T_{SC}L2_{DO}V$	SDOx Data Output Valid after SCKx Edge	—	20	ns
SP36	$T_{DO}V2_{SC}$, $T_{DO}V2_{SC}L$	SDOx Data Output Setup to First SCKx Edge	3	—	ns
SP40	$T_{DI}V2_{SC}H$, $T_{DI}V2_{SC}L$	Setup Time of SDIx Data Input to SCKx Edge	10	—	ns
SP41	$T_{SC}H2_{DI}L$, $T_{SC}L2_{DI}L$	Hold Time of SDIx Data Input to SCKx Edge	15	—	ns

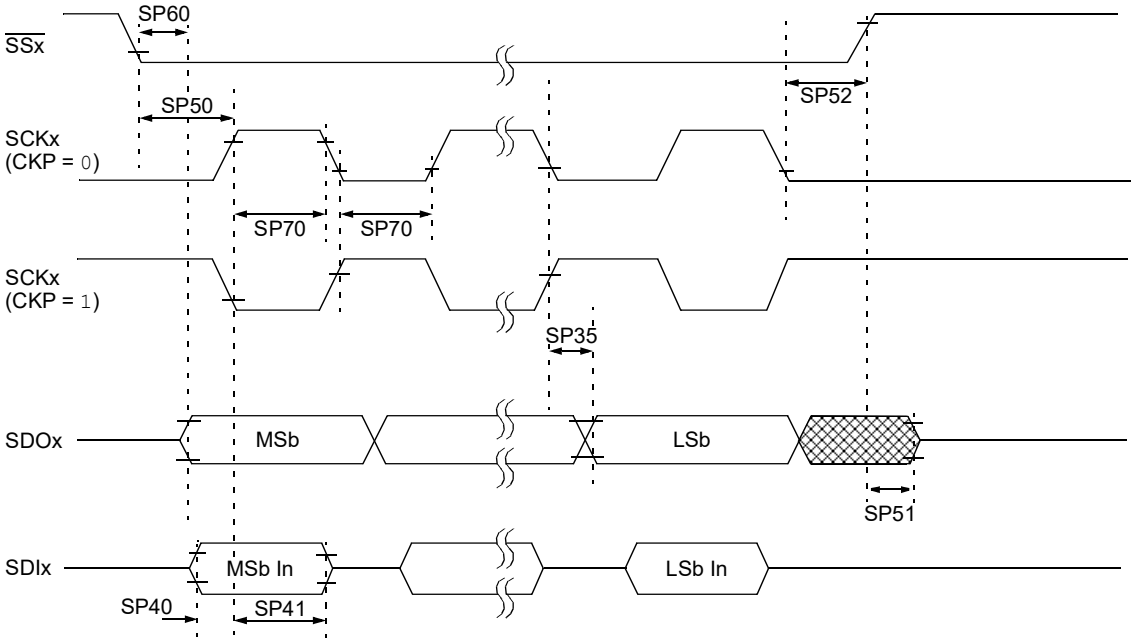
Note:
1. These parameters are characterized but not tested in manufacturing.

Figure 34-8. SPIx Module Client Mode (CKE = 0) Timing Characteristics



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Figure 34-9. SPIx Module Client Mode (CKE = 1) Timing Characteristics



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Table 34-28. SPIx Module Client Mode Timing Requirements

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended					
Param. No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**
SP70	$T_{SC}L$, $T_{SC}H$	SCKx Input Low Time or High Time	15	—	ns
SP35	$T_{SC}H2_{DO}V$, $T_{SC}L2_{DO}V$	SDOx Data Output Valid after SCKx Edge	—	20	ns
SP40	$T_{DI}V2_{SC}H$, $T_{DI}V2_{SC}L$	Setup Time of SDIx Data Input to SCKx Edge	10	—	ns
SP41	$T_{SC}H2_{DI}L$, $T_{SC}L2_{DI}L$	Hold Time of SDIx Data Input to SCKx Edge	15	—	ns
SP50	$T_{SS}L2_{SC}H$, $T_{SS}L2_{SC}L$	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	120	—	ns
SP51	$T_{SS}H2_{DO}Z$	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	8	50	ns
SP52	$T_{SC}H2_{SS}H$, $T_{SC}L2_{SS}H$	$\overline{SSx}$ ↑ after SCKx Edge	1.5 T_{CY} + 40	—	ns
SP60	$T_{SS}L2_{DO}V$	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	50	ns

Note:

1. These parameters are characterized but not tested in manufacturing.

Figure 34-10. I2Cx Bus Start/Stop Bits Timing Characteristics (Host Mode)

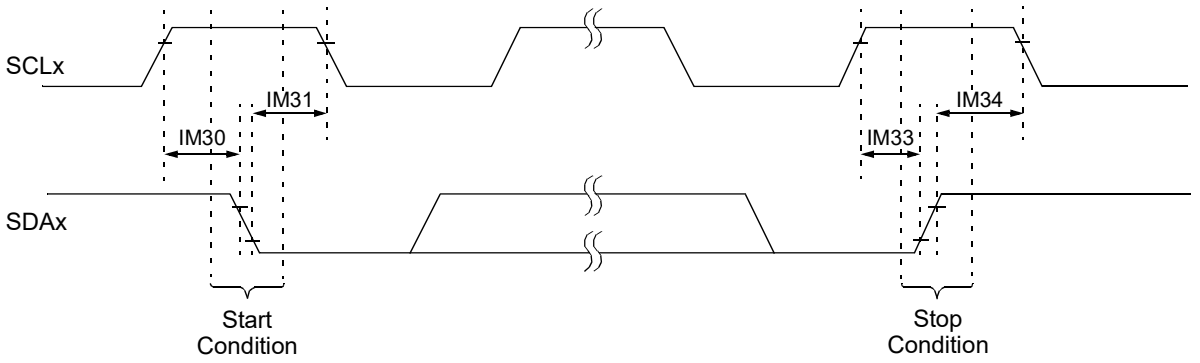
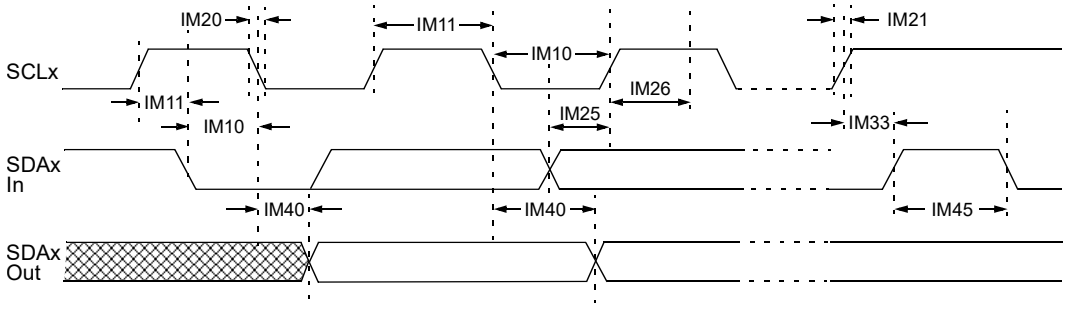


Figure 34-11. I2Cx Bus Data Timing Characteristics (Host Mode)



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Table 34-29. I2Cx Bus Data Timing Requirements (Host Mode)

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM10	$T_{LO:SCL}$	Clock Low Time	100 kHz mode	T_{CY} * (BRG + 1)	—	µs	
			400 kHz mode	T_{CY} * (BRG + 1)	—	µs	
			1 MHz mode	T_{CY} * (BRG + 1)	—	µs	
IM11	$T_{HI:SCL}$	Clock High Time	100 kHz mode	T_{CY} * (BRG + 1)	—	µs	
			400 kHz mode	T_{CY} * (BRG + 1)	—	µs	
			1 MHz mode	T_{CY} * (BRG + 1)	—	µs	
IM20	$T_{F:SCL}$	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	
			400 kHz mode	20 x (V_{DD}/5.5V)	300	ns	
			1 MHz mode	20 x (V_{DD}/5.5V)	120	ns	
IM21	$T_{R:SCL}$	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode	—	120	ns	
IM25	$T_{SU:DAT}$	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode	50	—	ns	
IM26	$T_{HD:DAT}$	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode	0	0.3	µs	
IM30	$T_{SU:STA}$	Start Condition Setup Time	100 kHz mode	T_{CY} * (BRG + 1)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	T_{CY} * (BRG + 1)	—	µs	
			1 MHz mode	T_{CY} * (BRG + 1)	—	µs	
IM31	$T_{HD:STA}$	Start Condition Hold Time	100 kHz mode	T_{CY} * (BRG + 1)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	T_{CY} * (BRG + 1)	—	µs	
			1 MHz mode	T_{CY} * (BRG + 1)	—	µs	
IM33	$T_{SU:STO}$	Stop Condition Setup Time	100 kHz mode	T_{CY} * (BRG + 1)	—	µs	
			400 kHz mode	T_{CY} * (BRG + 1)	—	µs	
			1 MHz mode	T_{CY} * (BRG + 1)	—	µs	
IM34	$T_{HD:STO}$	Stop Condition Hold Time	100 kHz mode	T_{CY} * (BRG + 1)	—	ns	
			400 kHz mode	T_{CY} * (BRG + 1)	—	ns	
			1 MHz mode	T_{CY} * (BRG + 1)	—	ns	
IM40	$T_{AA:SCL}$	Output Valid from Clock	100 kHz mode	—	3450	ns	
			400 kHz mode	—	900	ns	
			1 MHz mode	—	450	ns	
IM45	$T_{BF:SDA}$	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode	0.5	—	µs	
IM50	C_B	Bus Capacitive Loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
			1 MHz mode	—	10	pF	
IM51	T_{PGD}	Pulse Gobbler Delay		65	390	ns	

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Table 34-29. I2Cx Bus Data Timing Requirements (Host Mode) (continued)

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended						
Param No.	**Symbol**	**Characteristics**	**Min.(1)**	**Max.**	**Units**	**Conditions**

Note:

1. BRG is the value of the I^2C Baud Rate Generator.

Figure 34-12. I2Cx Bus Start/Stop Bits Timing Characteristics (Client Mode)

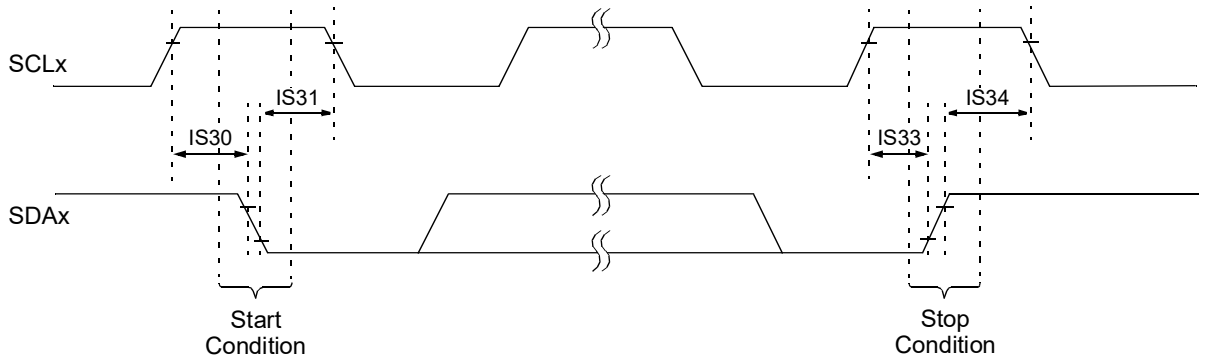


Figure 34-13. I2Cx Bus Data Timing Characteristics (Client Mode)

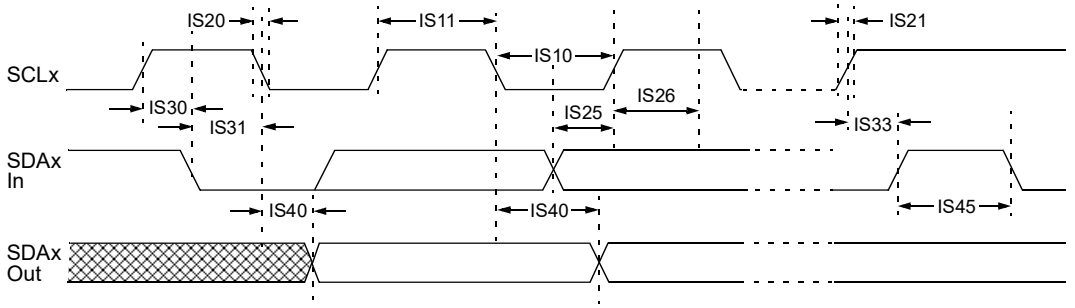


Table 34-30. I2Cx Bus Data Timing Requirements (Client Mode)

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended							
Param No.	**Sym**	**Characteristics**		**Min.**	**Max.**	**Units**	**Conditions**
IS10	$T_{LO:SCL}$	Clock Low Time	100 kHz mode	4.7	—	µs	CPU clock must be minimum 800 kHz
			400 kHz mode	1.3	—	µs	CPU clock must be minimum 3.2 MHz
			1 MHz mode	0.5	—	µs	

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Table 34-30. I2Cx Bus Data Timing Requirements (Client Mode) (continued)

Operating Conditions (unless otherwise stated):
3.0V ≤ V_{DD} ≤ 3.6V,
-40°C ≤ T_A ≤ +85°C for Industrial
-40°C ≤ T_A ≤ +125°C for Extended

Param No.	Sym	Characteristics		Min.	Max.	Units	Conditions
IS11	$T_{HI:SCL}$	Clock High Time	100 kHz mode	4.0	—	µs	CPU clock must be minimum 800 kHz
			400 kHz mode	0.6	—	µs	CPU clock must be minimum 3.2 MHz
			1 MHz mode	0.26	—	µs	
IS20	$T_{F:SCL}$	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	
			400 kHz mode	20 x (V_{DD}/5.5V)	300	ns	
			1 MHz mode	20 x (V_{DD}/5.5V)	120	ns	
IS21	$T_{R:SCL}$	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode	—	120	ns	
IS25	$T_{SU:DAT}$	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode	50	—	ns	
IS26	$T_{HD:DAT}$	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
			1 MHz mode	0	0.3	µs	
IS30	$T_{SU:STA}$	Start Condition Setup Time	100 kHz mode	4.7	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	µs	
			1 MHz mode	0.26	—	µs	
IS31	$T_{HD:STA}$	Start Condition Hold Time	100 kHz mode	4.0	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
			1 MHz mode	0.26	—	µs	
IS33	$T_{SU:STO}$	Stop Condition Setup Time	100 kHz mode	4.0	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode	0.26	—	µs	
IS34	$T_{HD:STO}$	Stop Condition Hold Time	100 kHz mode	> 0	—	µs	
			400 kHz mode	> 0	—	µs	
			1 MHz mode	> 0	—	µs	
IS40	$T_{AA:SCL}$	Output Valid from Clock	100 kHz mode	0	3.45	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode	0	0.45	µs	
IS45	$T_{BF:SDA}$	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode	0.5	—	µs	
IS50	C_B	Bus Capacitive Loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
			1 MHz mode	—	10	pF	

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Figure 34-14. UARTx Module Timing Characteristics

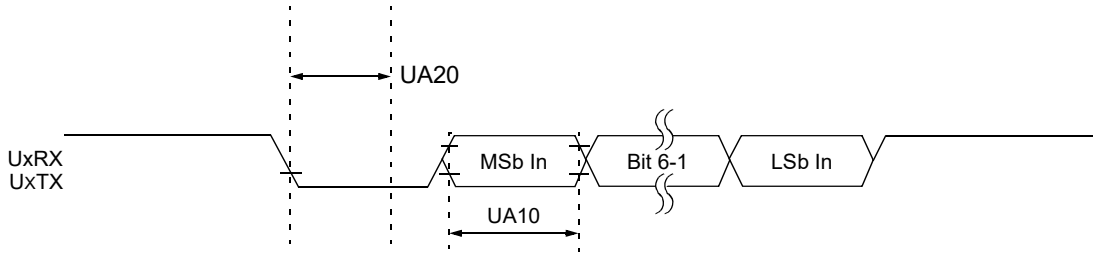


Table 34-31. UARTx Module Timing Requirements

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended					
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Max.**	**Units**
UA10	T_{UABAUD}	UARTx Baud Time	40	—	ns
UA11	F_{BAUD}	UARTx Baud Rate	—	40	Mbps
UA20	T_{CWF}	Start Bit Pulse Width to Trigger UARTx Wake-up	50	—	ns

Note:
1. These parameters are characterized but not tested in manufacturing.

Table 34-32. ADC Module Specifications

Operating Conditions (unless otherwise stated):(4) 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input							
AD9	F_{SRC}	ADC Module Input Frequency	—	—	500	MHz	Clock frequency selected by the CLKSELx bits
AD10	$F_{CORESRC}$	ADC Control Clock Frequency	—	—	250	MHz	Clock frequency after the first divider controlled by the CLKDIVx bits
AD11	F_{ADCORE}	ADC SAR Core Clock Frequency	—	—	70	MHz	SAR core frequency after the second divider controlled by the ADCSx or SHRADCSx bits
AD12	V_{INH}-V_{INL}	Full-Scale Input Span	AV_{SS}	—	AV_{DD}	V	
AD14	V_{IN}	Absolute Input Voltage	AV_{SS} – 0.3	—	AV_{DD} + 0.3	V	
AD17	R_{IN}	Recommended Impedance of Analog Voltage Source	—	100	—	W	For minimum sampling time (**Note 1**)
AD61	C_{HOLD}	Capacitance	—	12.5	—	pF	**(Note 1)**
AD62	R_{IC}	Input Resistance	—	500	1000	Ohm	Includes R_{SS} **(Note 1)**
AD66	V_{BG}	Internal Band Gap Input Voltage	1.14	1.2	1.26	V	**(Note 1)**
ADC Accuracy							
AD20	Nr	Resolution	12 data bits			bits	

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Table 34-32. ADC Module Specifications (continued)

Operating Conditions (unless otherwise stated):[4] 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
AD21b	INL_1S	Integral Nonlinearity	-3	-1.5/+1.5	+3	LSb	3.5 Msps [5], T_{ADC} = 4nS (250 MHz), $T_{CORESRC}$ = 8 nS (125 MHz), T_{ADCORE} = 16 nS (62.5 MHz), Sampling Time = 4 T_{ADCORE}, V_{DD} = 3.3V, AV_{DD} = 3.3V
AD22b	DNL_1S	Differential Nonlinearity	-1	-1/+1.5	+3	LSb	
AD23b	GERR_1S	Gain Error	—	+4	—	LSb	
AD24b	OERR_1S	Offset Error	—	-4	—	LSb	
AD21d	INL _3S	Integral Nonlinearity	—	-5/+5	—	LSb	2.7 Msps[6], T_{ADC} = 4 nS (250 MHz), $T_{CORESRC}$ = 8 nS (125 MHz), T_{ADCORE} = 16 nS (62.5 MHz), Sampling Time = 10 T_{ADCORE}, V_{DD} = 3.3V, AV_{DD} = 3.3V, all core conversions are started simultaneously.
AD22d	DNL_3S	Differential Nonlinearity	—	-1/+2	—	LSb	
AD23d	GERR_3S	Gain Error	—	+5	—	LSb	
AD24d	OERR_3S	Offset Error	—	-5	—	LSb	
AD25c	—	Monotonicity	—	—	—	LSb	**Guaranteed**
Dynamic Performance							
AD31b	SINAD	Signal-to-Noise and Distortion	56	—	70	dB	**Notes 2,3**
AD34b	ENOB	Effective Number of Bits	9.8	10.2	11.4	bits	**Notes 2,3**
AD50	T_{AD}	ADC Clock Period	14.3	—	—	ns	
AD51	F_{TP}	Throughput Rate	—	—	2.7	Msps	Shared Core **(Note 5)**

Notes:

1. These parameters are not characterized or tested in manufacturing.
2. These parameters are characterized but not tested in manufacturing.
3. Characterized with a 1 kHz sine wave.
4. The ADC module is functional at V_{BORMIN} < V_{DD} < V_{DDMIN}, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.
5. The throughput includes 10 T_{ADCORE} sampling time and 13 T_{ADCORE} conversion time.

Table 34-33. Die Temperature Diode Specifications

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TD01	T_{COEFF}	Temperature Coefficient	—	-1.5	—	mV/C	**Note 1**

Note:

1. These parameters are not characterized or tested in manufacturing.

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Table 34-34. High-Speed Analog Comparator Module Specifications

Operating Conditions (unless otherwise stated):(2) 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended							
Param No.	Sym	Characteristic	Min.	Typ.(1)	Max	Units	Comments
CM09	F_{IN}	Input Frequency	400	—	500	MHz	-40°C ≤ T_A ≤ +85°C
			400	—	480		+85°C < T_A ≤ +125°C
CM10	V_{IOFF}	Input Offset Voltage	-20	—	20	mV	
CM11	V_{ICM}	Input Common-Mode Voltage Range	AV_{SS}	—	AV_{DD}	V	**Note 1**
CM13	CMRR	Common-Mode Rejection Ratio	65	—	—	dB	**Note 1**
CM14	T_{RESP}	Large Signal Response	—	15	—	ns	V+ input step of 100 mV while V- input is held at $AV_{DD}/2$
CM15	V_{HYST}	Input Hysteresis	15	—	45	mV	Depends on HYSSEL[1:0] (1)

Notes:

1. These parameters are for design guidance only and are not tested in manufacturing.
2. The comparator module is functional at V_{BORMIN} < V_{DD} < V_{DDMIN}, but with degraded performance. Unless otherwise stated, module functionality is tested but not characterized.

Table 34-35. DACx Module Specifications

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended							
Param No.	Symbol	Characteristic	Min.	Typ.(1)	Max.	Units	Comments
DA02	CV_{RES}	Resolution		12		bits	
DA03	INL	Integral Nonlinearity Error	-38	—	0	LSB	
DA04	DNL	Differential Nonlinearity Error	-5	—	5	LSB	
DA05	EOFF	Offset Error	-3.5	—	21.5	LSB	
DA06	EG	Gain Error	0	—	41	LSB	
DA07	T_{SET}	Settling Time	600	750	2000	ns	Output with 2% of desired output voltage with a 10-90% or 90-10% Step
DA08	V_{OUT}	Voltage Output Range	0.165	—	3.135	V	V_{DD} = 3.3V
DA09	T_{TR}	Transition Time	—	340	—	ns	
DA10	T_{SS}	Steady-State Time	—	550	—	ns	

Note:

1. Data in the "Typ." column are at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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Table 34-36. DAC Output (DACOUT1 Pin) Specifications

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended							
Param No.	Sym	Characteristic	Min	Typ	Max	Units	Comments
DA11	R_{LOAD}	Resistive Output Load Impedance	10k	—	—	Ohm	
DA11a	C_{LOAD}	Output Load Capacitance	—	—	35	pF	Including output pin capacitance
DA12	I_{OUT}	Output Current Drive Strength	—	3	—	mA	Sink and source

Table 34-37. Current Bias Generator Specifications(1)

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended					
Param No.	Symbol	Characteristic	Min.	Max.	Units
CC03	I10SRC	10 µA Source Current	8.8	11.2	µA
CC04	I50SRC	50 µA Source Current	44	56	µA
CC05	I50SNK	50 µA Sink Current	-44	-56	µA

Note:

1. Parameters are characterized but not tested in manufacturing.

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Table 34-38. Operational Amplifier Specifications

Operating Conditions (unless otherwise stated): 3.0V ≤ V_{DD} ≤ 3.6V, -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
OA01	GBWP	Gain Bandwidth Product	—	20	—	MHz	
OA02	SR	Slew Rate	—	40	—	V/µs	
OA03	V_{IOFF}	Input Offset Voltage	-3(3)	-1/+1	+3(3)	mV	Unity gain configuration
			-8	-3/+3	+8	mV	Open-loop configuration
OA04	V_{IBC}	Input Bias Current	—	—	—	mV	**Note 2**
OA05	V_{ICM}	Common-Mode Input Voltage Range	AV_{SS}	—	AV_{DD}	V	NCHDISx = 0
			AV_{SS}	—	AV_{DD} – 1.4	V	NCHDISx = 1
OA07	CMRR	Common-Mode Rejection Ratio	—	68	—	dB	
OA08	PSRR	Power Supply Rejection Ratio	—	74	—	dB	
OA09	V_{OR}	Output Voltage Range	AV_{SS}	—	AV_{DD}	mV	0.5V input overdrive, no output loading **(Note 1)**
OA11	C_{LOAD}	Output Load Capacitance	—	—	30	uF	Including output pin capacitance **(Note 1)**
OA12	I_{OUT}	Output Current Drive Strength	—	3	—	mA	Sink and source
OA13	P_{MARGIN}	Phase Margin	44	—	—	degree	Unity gain **(Note 1)**
OA14	G_{MARGIN}	Gain Margin	7	—	—	dB	Unity gain **(Note 1)**
OA15	OLG	Open-Loop Gain	68	75	—		**Note 1**

Notes:

1. Parameters are for design guidance only and are not tested in manufacturing.
2. The op amps use CMOS input circuitry with negligible input bias current. The maximum “effective bias current” is the I/O pin leakage specified by electrical Parameter DI50.
3. This parameter is characterized but not tested in manufacturing.

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35. High-Temperature Electrical Characteristics

This section provides an overview of the dsPIC33CDVL256MC506 family devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40°C to +150°C are identical to those shown in Electrical Characteristics for operation between -40°C to +125°C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC20 in Electrical Characteristics is the Industrial and Extended temperature equivalent of HDC20.

Absolute maximum ratings for the dsPIC33CDVL256MC506 family are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Table 35-1. Absolute Maximum Ratings(1)

Parameter	Rating
Ambient temperature under bias	-40°C to +150°C
Storage temperature	-65°C to +150°C
Voltage on V_{DD} with respect to V_{SS}	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to V_{SS}(3)	-0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 3.0V$(3)	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 3.0V$(3)	-0.3V to +3.6V
Maximum current out of V_{SS} pin	300 mA
Maximum current into V_{DD} pin(2)	300 mA
Maximum current sunk/sourced by any regular I/O pin	15 mA
Maximum current sunk/sourced by an I/O pin with increased current drive strength (RB1, RC8, RC9 and RD8)	25 mA
Maximum current sunk by a group of I/Os between two V_{SS} pins(4)	75 mA
Maximum current sourced by a group of I/Os between two V_{DD} pins(4)	75 mA
Maximum current sunk by all I/Os(2,5)	200 mA
Maximum current sourced by all I/Os(2,5)	200 mA

Notes:

1. Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those, or any other conditions above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Maximum allowable current is a function of device maximum power dissipation (see Table 34-3).
3. See the **"Pin Diagrams"** section for the 5V tolerant pins.
4. Not applicable to AV_{DD} and AV_{SS} pins.
5. For 28-pin packages, the maximum current sunk/sourced by all I/Os is limited by 150 mA.

35.1. DC Characteristics

Table 35-2. Operating MIPS vs. Voltage

V_{DD} Range	Temperature Range	Maximum CPU Clock Frequency
3.0V to 3.6V	-40°C to +150°C	70 MHz

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Table 35-3. Thermal Operating Conditions

Rating	Symbol	Min.	Max.	Unit
High-Temperature Devices				
Operating Junction Temperature Range	T_J	-40	+165	°C
Operating Ambient Temperature Range	T_A	-40	+150	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $I/O = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$		W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$		W

Table 35-4. Operating Voltage Specifications

Operating Conditions (unless otherwise stated): **-40°C ≤ T_A ≤ +150°C for High**						
Param No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
HDC10	V_{DD}	**Supply Voltage**	3.0	3.6	V	
HDC16	V_{POR}	**V_{DD} Start Voltage** to Ensure Internal Power-on Reset Signal	—	V_{SS}	V	
HDC17	SV_{DD}	**V_{DD} Rise Rate** to Ensure Internal Power-on Reset Signal	0.03	—	V/ms	0V-3V in 100 ms
HBO10	V_{BOR}(1)	**BOR Event** on V_{DD} Transition High-to-Low	2.68	2.99	V	

Note:

1. Device is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$. Analog modules (ADC and comparators) may have degraded performance. The V_{BOR} parameter is for design guidance only and is not tested in manufacturing.

Table 35-5. Operating Current (I_{DD})(2)

Parameter No.	Typ.(1)	Max.	Units	Conditions		
HDC20	15.0	30.0	mA	+150°C	3.3V	10 MIPS (N1 = 1, N2 = 5, N3 = 2, M = 50, F_{VCO} = 400 MHz, F_{PLLO} = 40 MHz)
HDC21	16.5	35.0	mA	+150°C	3.3V	20 MIPS (N1 = 1, N2 = 5, N3 = 1, M = 50, F_{VCO} = 400 MHz, F_{PLLO} = 80 MHz)
HDC22	18.5	40.0	mA	+150°C	3.3V	40 MIPS (N1 = 1, N2 = 3, N3 = 1, M = 60, F_{VCO} = 480 MHz, F_{PLLO} = 160 MHz)
HDC23	25.5	50.0	mA	+150°C	3.3V	70 MIPS (N1 = 1, N2 = 2, N3 = 1, M = 70, F_{VCO} = 560 MHz, F_{PLLO} = 280 MHz)

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Table 35-5. Operating Current (I_{DD})[2] (continued)

Parameter No.	Typ.[1]	Max.	Units	Conditions

Notes:

1. Data in the "Typ." column are for design guidance only and are not tested.
2. Base Run current (I_{DD}) is measured as follows:
   - Oscillator is switched to EC+PLL mode in software
   - OSC1 pin is driven with external 8 MHz square wave with levels from 0.3V to V_{DD} – 0.3V
   - OSC2 pin is configured as an I/O in the Configuration Words (OSCIOFNC (FOSC[2]) = `0`)
   - FSCM is disabled (FCKSM[1:0] (FOSC[7:6]) = `01`)
   - Watchdog Timer is disabled (FWDT[15]) = `0` and WDTCONL[15] = `0`)
   - All I/O pins (except OSC1) are configured as outputs and driving low
   - No peripheral modules are operating or being clocked (defined PMDx bits are all '1's)
   - JTAG is disabled (JTAGEN (FICD[5]) = `0`)
   - `NOP` instructions are executed in `while(1)` loop

Table 35-6. Idle Current (I_{IDLE})[2]

Parameter No.	Typ.[1]	Max.	Units	Conditions		
HDC40	11.0	20.0	mA	+150°C	3.3V	10 MIPS (N1 = 1, N2 = 5, N3 = 2, M = 50, F_{VCO} = 400 MHz, F_{PLLO} = 40 MHz)
HDC41	11.5	20.0	mA	+150°C	3.3V	20 MIPS (N1 = 1, N2 = 5, N3 = 1, M = 50, F_{VCO} = 400 MHz, F_{PLLO} = 80 MHz)
HDC42	12.5	25.0	mA	+150°C	3.3V	40 MIPS (N1 = 1, N2 = 3, N3 = 1, M = 60, F_{VCO} = 480 MHz, F_{PLLO} = 160 MHz)
HDC43	14.0	30.0	mA	+150°C	3.3V	70 MIPS (N1 = 1, N2 = 2, N3 = 1, M = 70, F_{VCO} = 560 MHz, F_{PLLO} = 280 MHz)

Notes:

1. Data in the "Typ." column are for design guidance only and are not tested.
2. Base Idle current (I_{IDLE}) is measured as follows:
   - Oscillator is switched to EC+PLL mode in software
   - OSC1 pin is driven with external 8 MHz square wave with levels from 0.3V to V_{DD} – 0.3V
   - OSC2 is configured as an I/O in the Configuration Words (OSCIOFNC (FOSC[2]) = `0`)
   - FSCM is disabled (FCKSM[1:0] (FOSC[7:6]) = `01`)
   - Watchdog Timer is disabled (FWDT[15]) = `0` and WDTCONL[15] = `0`)
   - All I/O pins (except OSC1) are configured as outputs and driving low
   - No peripheral modules are operating or being clocked (defined PMDx bits are all '1's)
   - JTAG is disabled (JTAGEN (FICD[5]) = `0`)
   - Flash in standby with NVMSIDL (NVMCON[12]) = `1`

Table 35-7. Power-Down Current (I_{PD})[2]

Param No.	Characteristic	Typ.[1]	Max.	Units	Conditions	
HDC60	Base Power-Down Current	7.6	20.0	mA	+150°C	3.3V

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Table 35-7. Power-Down Current (I_{PD})[2] (continued)

Param No.	Characteristic	Typ.[1]	Max.	Units	Conditions

Notes:

1. Data in the “Typ.” column are for design guidance only and are not tested.
2. Base Power-Down current (I_{PD}) is measured as follows:
   - OSC1 pin is driven with external 8 MHz square wave with levels from 0.3V to V_{DD} – 0.3V
   - OSC2 is configured as an I/O in the Configuration Words (OSCIOFNC (FOSC[2]) = 0)
   - FSCM is disabled (FCKSM[1:0] (FOSC[7:6]) = 01)
   - Watchdog Timer is disabled (FWDT[15]) = 0 and WDTCONL[15] = 0)
   - All I/O pins (except OSC1) are configured as outputs and driving low
   - No peripheral modules are operating or being clocked (defined PMDx bits are all ‘1’s)
   - JTAG is disabled (JTAGEN (FICD[5]) = 0)
   - The regulators are in Active mode, VREGS bit = 1 (Standby mode only valid up to +85°C)
   - The regulators are in Full-Power mode, LPWREN bit = 0 (Low-Power mode only valid up to +85°C)

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Table 35-8. Doze Current (I_{DOZE})

Parameter No.	Typ.(1)	Max.	Doze Ratio	Units	Conditions		
HDC70	18.5	30.0	1:2	mA	+150°C	3.3V	70 MIPS (N = 1, N2 = 2, N3 = 1, M = 70, F_{VCO} = 560 MHz, F_{PLLO} = 280 MHz)
	15.0	25.0	1:128	mA			

Note:

1. Data in the "Typ." column are for design guidance only and are not tested.

Table 35-9. Watchdog Timer Delta Current (ΔI_{WDT})(1)

Parameter No.	Typ.	Max.	Units	Conditions	
HDC61	28	—	µA	+150°C	3.3V

Note:

1. The ΔI_{WDT} current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current. All parameters are characterized but not tested during manufacturing.

Table 35-10. PWM Delta Current

Parameter No.	Typ.	Max.	Units	Conditions		
HDC100	8.0	10.0	mA	+150°C	3.3V	PWM Output Frequency = 500 kHz, PWM Input (F_{PLLO} = 500 MHz), (V_{CO} = 1000 MHz, PLLFBD = 125)
HDC101	6.0	8.0	mA	+150°C	3.3V	PWM Output Frequency = 500 kHz, PWM Input (F_{PLLO} = 400 MHz), (V_{CO} = 400 MHz, PLLFBD = 50)
HDC102	2.6	4.0	mA	+150°C	3.3V	PWM Output Frequency = 500 kHz, PWM Input (F_{PLLO} = 200 MHz), (V_{CO} = 200 MHz, PLLFBD = 50)
HDC103	1.5	2.5	mA	+150°C	3.3V	PWM Output Frequency = 500 kHz, PWM Input (F_{PLLO} = 100 MHz), (V_{CO} = 100 MHz, PLLFBD = 50)

Table 35-11. ADC Delta Current(1)

Parameter No.	Typ.	Max.	Units	Conditions		
HDC120	6.0	8.5	mA	+150°C	3.3V	T_{AD} = 14.3 ns (3.5 Msps conversion rate)

Note:

1. Shared core continuous conversion. T_{AD} = 14.3 nS (3.5 Msps conversion rate). Listed delta currents are for only one ADC core. All parameters are characterized but not tested during manufacturing.

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Table 35-12. Comparator + DAC Delta Current

Parameter No.	Min.	Typ.	Max.	Units	Conditions		
HDC130	—	2.0	4.0	mA	+150°C	3.3V	F_{PLLO} @ 500 MHz(1)

Note:

1. Listed delta currents are for only one comparator + DAC instance. All parameters are characterized but not tested during manufacturing.

Table 35-13. Op Amp Delta Current(1)

Parameter No.	Typ.	Max.	Units	Conditions	
HDC140	0.8	2.5	mA	+150°C	3.3V

Note:

1. Listed delta currents are for only one op amp instance. All parameters are characterized but not tested during manufacturing.

Table 35-14. I/O Pin Input Specifications

Operating Conditions (unless otherwise stated): **3.0V < V_{DD} < 3.6V** **-40°C < T_A < +150°C for High**					
Param No.	**Symbol**	**Characteristic**	**Min.(3)**	**Max.(4)**	**Units**
HDI50	I_{IL}	**Input Leakage Current(1)**			
		I/O Pins 5V Tolerant(2)	-800	800	nA
		I/O Pins Not 5V Tolerant(2)	-800	800	nA
		$\overline{MCLR}$	-800	800	nA
		OSCI	-800	800	nA

Notes:

1. Negative current is defined as current sourced by the pin.
2. See the **"Pin Diagrams"** section for the 5V tolerant I/O pins.
3. $V_{PIN} = V_{SS}$.
4. $V_{PIN} = V_{DD}$.

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Table 35-15. Internal FRC Accuracy

Operating Conditions (unless otherwise stated): **3.0V < V_{DD} < 3.6V** **-40°C < T_A < +150°C for High**				
Param No.	**Characteristic**	**Min.**	**Max.**	**Units**
HF20a	FRC @ 8 MHz(1)	-3	+3	%
Note: 1. Frequency is calibrated at +25°C and 3.3V.				

Table 35-16. High-Speed Analog Comparator Module Specifications(1)

Operating Conditions (unless otherwise stated): **3.0V < V_{DD} < 3.6V** **-40°C < T_A < +150°C for High**							
Param No.	**Sym**	**Characteristic**	**Min.**	**Typ.(1)**	**Max**	**Units**	**Comments**
HCM09	F_{IN}	Input Frequency	400	—	475	MHz	
Note: 1. These parameters are for design guidance only and are not tested in manufacturing.							

Table 35-17. DACx Module Specifications

Operating Conditions (unless otherwise stated): **3.0V < V_{DD} < 3.6V** **-40°C < T_A < +150°C for High**							
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
HDA03	INL	Integral Nonlinearity Error	-45	—	0	LSB	
HDA04	DNL	Differential Nonlinearity Error	-5	—	5	LSB	
HDA05	EOFF	Offset Error	-21	—	21	LSB	
HDA06	EG	Gain Error	-41	—	41	LSB	

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36. MOSFET Gate Driver Electrical Characteristics

Table 36-1. Absolute Maximum Ratings(†)

Parameter	Rating
Input Voltage, HV_{DD}	(GND – 0.3V) to +40V
Internal Power Dissipation	Internally Limited
Operating Junction Temperature(2)	-40°C to +165°C
Transient Junction Temperature(1)	+170°C
Storage Temperature(2)	-55°C to +165°C
Digital I/O	-0.3V to 5.5V
Low-Voltage Analog I/O	-0.3V to 5.5V
VBx, WAKE	(GND – 0.3V) to +40V
PHx, HSx	(GND – 5.5V) to +40V
VBOOT, LSx.	(GND – 0.3V) to +13.2V
CAP1, CAP2	(GND – 0.3V) to +40V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes:

1. Transient junction temperatures should not exceed one second in duration. Sustained junction temperatures above +170°C may impact the device reliability.
2. The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θJA). Exceeding the maximum allowable power dissipation may cause the device operating junction temperature to exceed the maximum +165°C rating. Sustained junction temperatures above +165°C can impact the device reliability.).

Table 36-2. AC/DC Characteristics

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, HV_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF, C_{CP} = 220 nF.						
Parameters	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Power Supply Input						
Input Operating Voltage	HV_{DD}	4.5	—	40	V	V_{REG} active
		6.0	—	29.0		Driver output active
Input Supply Current	I_{SUP}	—	5	15	µA	Sleep mode, T_J = +25°C
		—	180	330		Standby, OE = 0V
		—	500	—		Active, HV_{DD} > 13, 5V, OE > VDIG_HI_TH
		—	1200	—		Active, HV_{DD} = 6V, T_J = +25°C

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Table 36-2. AC/DC Characteristics (continued)

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, HV_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF, C_{CP} = 220 nF.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Input Supply Current	I_{SUP}	—	5	15	µA	Sleep mode, T_J = +25°C
		—	200	350		Standby, OPAMP = 1, OE = 0V
		—	800	1300		Standby, OPAMP = 0, OE = 0V
		—	1000	—		Active, HV_{DD} > 13, 5V, OE > $V_{DIG\_HI\_TH}$
		—	1500	—		Active, OE > $V_{DIG\_HI\_TH}$, HV_{DD} = 7V, TJ = +25°C
Bias Generator						
+12V Regulated Charge Pump (V_{BOOT})						
Charge Pump Current	I_{CP}	20	—	—	mA	HV_{DD} = 9.0V
Charge Pump Start	CP_{START}	12.50	12.75	—	V	Falling
Charge Pump Stop	CP_{STOP}	—	13.25	14	V	Rising
Charge Pump Frequency	CP_{FSW}	—	76.80	—	kHz	HV_{DD} = 9.0V
		—	0	—		HV_{DD} = 14V
Charge Pump Switch Resistance	CP_{RDSON}	—	14	—	W	RDSON sum of high side and low side(1)
Output Voltage	V_{BOOT}	—	12	—	V	HV_{DD} ≥ 14V, I_{OUT} = 30 mA
		9	12	—		7V ≤ HV_{DD} < 14V, C_{CP} = 150 nF, I_{OUT} = 20 mA
		9	—	—		6.25V ≤ HV_{DD} < 7V, C_{CP} = 270 nF, I_{OUT} = 15 mA
Output Voltage Tolerance	$\|TOLV_{OUT12}\|$	—	—	4.0	%	I_{OUT} = 30 mA
Output Capability	I_{BOOT}	30	—	—	mA	Average current
Output Current Limit	$I_{BOOTLIMIT}$	50	60	80	mA	Average current
Output Voltage Temperature Coefficient	TCV_{OUT12}	—	160	—	ppm/°C	**Note 1**
Line Regulation	$\|\Delta V_{OUT}/ (V_{OUT} \times \Delta)\|$	—	0.1	0.5	%/V	14V < HV_{DD} < 19V, I_{OUT} = 30 mA
Load Regulation	$\Delta V_{OUT}/V_{OUT}\|$	—	0.2	1.0	%	I_{OUT} = 0.1 mA to 30 mA, HV_{DD} = 14V

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Table 36-2. AC/DC Characteristics (continued)

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, HV_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF, C_{CP} = 220 nF.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Power Supply Rejection Ratio	PSRR	—	60	—	dB	f = 1 kHz, IOUT = 10 mA(1)
Output Capacitor Capacitance Range	CV_{BOOT}	4.7	—	10	µF	Ceramic, Tantalum, Electrolytic(1)
Output Capacitor ESR Range	$CESR_{VBOOT}$	0.010	—	1.0	W	**Note 1**
Flying Capacitor Capacitance Range	C_{CP}	100	220	1000	nF	**Note 1**
V_{BOOT} Ready Threshold	V12sm_pg	—	50	—	%Vboot	State machine V_{BOOT} Power Good threshold to move to next state (1)
+3.3V Linear Regulator (VREG)						
Output Voltage	V_{REG}	—	—	—	V	HV_{DD} = 6V, I_{OUT} = 70 mA
		3.168	3.3	3.432		V_{REG} = 3.3V
Output Voltage Tolerance	$\lvert TOLV_{REG} \rvert$	—	—	4.0	%	—
Output Current	I_{OUT}	70	—	—	mA	Average current
Output Foldback Current Corner	I_{FOLD}	80	95	120	mA	Average current
Output Foldback Current Limit	I_{FOLD_LIM}	—	10	—	mA	R_{LOAD} = 10 mW
Line Regulation	$\lvert \Delta V_{OUT} / (V_{OUT} \times \Delta V_{DD}) \rvert$	—	0.1	0.5	%/V	V_{REG} = 3.3V: 6V < H_{VDD} < 19V, IOUT = 70 mA; V_{REG} = 5V: 7.5V < HV_{DD} < 19V, I_{OUT} = 70 mA
Load Regulation	$\lvert \Delta V_{OUT} / V_{OUT} \rvert$	—	0.2	1.0	%	$_{IOUT}$ = 0.1 mA to 70 mA
Power Supply Rejection Ratio	PSRR	—	60	—	dB	f = 1 kHz, I_{OUT} = 10 mA (1)
Output Capacitor Capacitance Range	CV_{REG}	4.7	—	30	µF	Ceramic, Tantalum, Electrolytic(1)
Output Capacitor ESR Range	$CESR_{VREG}$	0.010	—	1.0	W	**Note 1**
Voltage Supervisor						
V_{REG} Undervoltage Fault Inactive	$VREGUV_{FINACT}$	—	92	—	$\%V_{REG}$	V_{REG} rising
V_{REG} Undervoltage Fault Active	$VREGUV_{FACT}$	—	88	—	$\%V_{REG}$	V_{REG} falling

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Table 36-2. AC/DC Characteristics (continued)

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, HV_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF, C_{CP} = 220 nF.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
V_{REG} Undervoltage Fault Hysteresis	$VREGUV_{FHYS}$	—	4	—	$\%V_{REG}$	—
HV_{DD} Undervoltage Lockout Inactive	$UVLO_{INACT}$	—	6.0	6.25	V	Rising
HV_{DD} Undervoltage Lockout Active	$UVLO_{ACT}$	5.1	5.5	—	V	Falling
HV_{DD} Undervoltage Lockout Hysteresis	$UVLO_{HYS}$	—	0.5	—	V	—
HV_{DD} Undervoltage Shutdown Active	$UVSHDN_{ACT}$	4.0	4.25	4.5	V	HV_{DD} < $UVSHDN_{ACT}$
HV_{DD} Undervoltage Shutdown Inactive	$UVSHDN_{INACT}$	$UVLO_{INACT}$			V	HV_{DD} > $UVLO_{INACT}$
HV_{DD} Overvoltage Lockout Active	OVLOACT	—	32.0	33.0	V	HV_{DD} rising
HV_{DD} Overvoltage Lockout Inactive	$OVLO_{INACT}$	29.0	30.0	—	V	HV_{DD} falling
HV_{DD} Overvoltage Lockout Hysteresis	$OVLO_{HYS}$	—	2.0	—	V	—
Temperature Supervisor						
Thermal Warning Temperature	T_{WARN}	—	140	—	°C	Rising temperature
Thermal Warning Hysteresis	DT_{WARN}	—	15	—	°C	Falling temperature
Thermal Shutdown Temperature	T_{SD}	170	210	—	°C	Rising temperature(1)
Thermal Shutdown Hysteresis	ΔT_{SD}	—	25	—	°C	Falling temperature
Motor Control Unit						
Gate Output Drivers						
Output Driver Source Current	I_{SOURCE}	0.25	0.37	—	A	HS[A:C], LS[A:C] (1)
Output Driver Sink Current	I_{SINK}	0.3	0.49	—	A	HS[A:C], LS[A:C] (1)
Output Driver Source Resistance	$R_{DSONSOURCE}$	—	14	26	W	I_{OUT} = -10 mA, HS[A:C], LS[A:C]

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Table 36-2. AC/DC Characteristics (continued)

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, HV_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF, C_{CP} = 220 nF.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Output Driver Sink Resistance LS	$R_{DSONSINK}LS$	—	14	26	W	I_{OUT} = 10 mA, LS[A:C]
Output Driver Sink Resistance HS Dynamic	$R_{DSONSINK}HSDYN$	—	14	26	W	IOUT = 10 mA, HS[A:C], t < 1 ms
Output Driver Sink Resistance HS	$R_{DSONSINK}HS$	—	19	31	W	I_{OUT} = 10 mA, HS[A:C]
Output Driver Fault Blanking Time (UVLO and OCP); Set in the DRVBL[1:0] bits (CFG2[1:0])	t_{BLANK}	3900	4400	4900	ns	00 – Default (1)
		2000	2200	2400		01(1)
		900	1100	1300		10(1)
		400	550	700		11(1)
Output Driver UVLO Threshold	V^{DUVLO}	4	—	4.5	V	Configuration Register 0(bit 3 = 0)
Output Driver PWM Dead Time; Set in the DRVDT[2:0] bits (CFG2[4:2])	t_{PWM_DEAD}	1800	2000	2200	ns	000 – Default (1)
		1550	1750	1950		001(1)
		1350	1500	1650		010(1)
		1100	1250	1400		011(1)
		900	1000	1150		100(1)
		650	750	900		101(1)
		450	500	650		110(1)
		200	250	350		111(1)
Output Driver Propagation Delay Time On	$t_{GATE\_PROP\_ON}$	—	40	80	ns	From PWMxy active to HSx/LSx > 10% (1)
Output Driver Propagation Delay Time Off	$t_{GATE\_PROP\_OFF}$	—	40	80	ns	From PWMxy inactive to HSx/LSx < 90% (1)
Output Driver HS Drive Voltage	V_{HS}	4.5	12	12.5	V	With respect to Phase pin(1)
Output Driver LS Drive Voltage	V_{ls}	4.5	12	12.5	V	With respect to ground (1)
Output Driver Short-Circuit Protection Threshold(High Side: HV_{DD} – VPHX), (Low Side: VPHX – P_{GND}); Set in the EXTOC[1:0] bits (CFG0[1:0])	Dsc_thr	0.230	0.250	0.270	V	00 – Default (1)
		0.470	0.500	0.530		01(1)
		0.720	0.750	0.780		10(1)
		0.960	1.000	1.040		11(1)
Output Driver Short-Circuit Filter Time	T_{SC_DLY}	230	—	600	ns	C_{LOAD} = 1000 pF, HV_{DD} = 12V, detection after filtering(1)

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Table 36-2. AC/DC Characteristics (continued)

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, HV_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF, C_{CP} = 220 nF.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Filter Time for All Other Faults	T_{FLT_DLY}	1400	—	3600	ns	**Note 1**
Power-up or Sleep to Standby	t_{POWER}	—	5	—	ms	IVREG = 70 mA
Standby to Motor Operational	t_{MOTOR}	—	35	—	µs	OE high-low-high transition < 1 ms Fault clearing pulse**(1)**
		—	5	10	ms	OE low-high transition, Standby state to operational**(1)**
		—	—	16	ms	OE low-high transition, Standby state to operational if VBOOT fails to reach V12sm_pg(1)
Fault to Driver Output Turn-Off	T_{FAULT_OFF}	—	—	—	µs	CLOAD = 1000 pF, HVDD = 12V, time after Fault occurs(1)
		—	0.420	1.0		XOCP**(1)**
		—	2.4	4.0		OVLO(1)
		—	4.2	6.0		All other Faults**(1)**
OE Low to Driver Output Turn-Off	T_{DEL_OFF}	—	3.2	4.0	µs	CLOAD = 1000 pF, HVDD = 12V, time after OE = Low**(1)**
OE Low to Standby State	$t_{STANDBY}$	0.9	—	1.35	ms	Time after OE = Low, SLEEP bit = 0
OE Low to Sleep State	t_{SLEEP}	0.9	—	1.35	ms	Time after OE = Low, SLEEP bit = 1
OE Fault Clearing Pulse	t_{FAULT_CLR}	1	—	900	µs	OE high-low-high transition time
Operational Amplifiers (DSTEMP)						
Input Offset Voltage	V_{OS}	-10	—	+10	mV	V_{CM} = 0V
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	V_{CM} = 0V**(1)**
Input Bias Current	I_B	-1	—	+1	µA	—
Common-Mode Input Range	V_{CMR}	-0.3	—	V_{REG}	V	—
Common-Mode Rejection Ratio	CMRR	—	80	—	dB	Freq = 1 kHz, I_{OUT} = 10 µA**(1)**

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Table 36-2. AC/DC Characteristics (continued)

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, HV_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF, C_{CP} = 220 nF.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Maximum Output Voltage Range	V_{OL}, V_{OH}	0.15	—	VREG – 0.300	V	I_{OUT} = ±200 µA
Slew Rate	SR	—	±7	—	V/µs	Symmetrical, C_{LOAD} = 20 pF(1)
Gain Bandwidth Product	GBWP	4	10.0	—	MHz	**Note 1**
I/O Ports						
Digital Interface						
Digital Input/ Output	$DIGITAL_{I/O}$	0	—	5.5	V	V_{REG} = 5.0V version(1)
		0	—	3.3		V_{REG} = 3.3V version(1)
Digital Open-Drain Low Voltage	$DIGITALV_{I/O}$	—	—	50	mV	I_{LOAD} = 1 mA
Digital Input Rising Threshold	$V_{DIG\_HI\_TH}$	—	—	1.26	V	—
Digital Input Falling Threshold	$V_{DIG\_LO\_TH}$	0.54	—	—	V	—
Digital Input Current	I_{DIG}	—	30	100	µA	V_{DIG} = 3.0V
		—	0.2	—		V_{DIG} = 0V
Input Pull-Down Resistance	R_{PULLDN}	—	51	—	kΩ	PWM[A:C]H/L, OE pins
Analog Interface						
Analog Low-Voltage Input	$ANALOG_{VIN}$	0	—	5.5	V	Excludes high-voltage pins(1)
Analog Low-Voltage Output	$ANALOG_{VOUT}$	0	—	Vreg	V	Excludes high-voltage pins (1)
WAKE Input(2)						
Input Voltage	$WAKE_{I/O}$	0	—	HVdd	V	—
Input Rising Threshold	$V_{WAKE\_HI\_TH}$	—	—	1.26	V	**Note 1**
Input Falling Threshold	$V_{WAKE\_LO\_TH}$	0.54	—	—	V	—
Input Current	I_{WAKE}	—	0.2	—	µA	VWAKE = 0.0V (1)
		—	70	—		VWAKE = 3.3V (1)
		—	106	—		VWAKE = 5.0V (1)
		—	596	—		VWAKE = 28V (1)
Input Pull-Down Resistance	R_{WAKE_PULLDN}	—	51	—	kW	—
WAKE Signal Setup Time	t_{WAIT_SETUP}	150	—	—	µs	Minimum time WAKE pin must be logic high before triggering wake-up
DE2 Communications						

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Table 36-2. AC/DC Characteristics (continued)

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, HV_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF, C_{CP} = 220 nF.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Baud Rate	BAUD	9030	9600	10170	bps	Half-duplex
Power-up Delay	PU_DELAY	—	6	10	ms	Time from rising HV_{DD} ≥ 6V to DE2 starts sending POR message, CV_{REG} = 1 µF (1)
DE2 Sink Current	I_{DE2_SINK}	1	—	—	mA	V_{DE2} ≤ 50 mV (1)
DE2 Message Response Time	t_{DE2_RSP}	0	—	1	ms	Time from last received Stop bit to response Start bit
DE2 Host Wait Time	t_{DE2_WAIT}	2.8	—	—	ms	Minimum time for host to wait for response; three packets based on 9600 Baud
DE2 Message Receive Time-out	$DE2_{RCVTOUT}$	—	—	1.45	ms	Time after Start bit received to NACK for no Stop bit
Auto-Baud Detection Window (Break)	$ABAUD_{DET}$	1.29	—	2.00	ms	Window for valid detection of continuous logic low on DE2 link
Auto-Baud Response Delay	$ABAUD_{DLY}$	—	1.00	—	ms	Delay from ABAUDDET to start of sending 0x55 byte
Auto-Baud Complete Delay	$ABAUD_{COMP}$	—	2.00	—	ms	Delay after sending 0x55 byte before exiting auto-baud function
Delay Between Bytes of Multibyte Message from Host	$t_{DE2\_HOST\_MULTI\_DLY}$	—	—	1.3	ms	Delay between message bytes arriving from host

Notes:

1. Limits based on design, simulation or characterization. Not production tested.
2. The WAKE pin must remain high for > t_{WAIT_SETUP} time to successfully awaken the device from Sleep.

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37. LIN Transceiver Electrical Characteristics

Table 37-1. Absolute Maximum Ratings(1)

Parameter	Rating
Input Voltage, LIN_V_{DD}	(LIN_V_{SS} – 0.3V) to +40.0V
Logic Pins (LIN_RXD, LIN_TXD, LIN_EN) Voltage Levels	-0.3V to +5.5V
Logic Output DC Currents	-5 mA to +5 mA
LIN_BUS DC Voltage	-27V to +40V
LIN_BUS DC Voltage Transient (Pulse Time <500 ms)	-27V to +43V
LIN_BUS DC Current	200 mA
LIN_INH DC Voltage	-0.3V to (LIN_VDD + 0.3V)
LIN_INH DC Current	-100 mA to +30 mA
LIN_WKIN DC Voltage	-0.3V to +40V

Note:

1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 37-2. Electrical Characteristics

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type
Operating Conditions (unless otherwise stated): 5V < V_S < 28V, -40°C < T_J < +150°C; all values refer to LIN_V_{SS} pins								
LIN_V_{DD} Pin								
Nominal DC Voltage Range		LIN_VDD	V_S	5	13.5	28	V	A
Supply Current in Sleep Mode	Sleep mode, V_{LIN} > V_S – 0.5V, V_S < 14V, T = +27°C	LIN_V_{DD}	$I_{VSsleep}$	3	9	15	µA	B
	Sleep mode,V_{LIN} > V_S – 0.5V, V_S < 14V	LIN_V_{DD}	$I_{VSsleep}$	3	11	20	µA	A
	Sleep mode, V_{LIN} = 0V, bus shorted to LIN_VSS, V_S < 14V	LIN_V_{DD}	$I_{VSsleep\_short}$	20	50	100	µA	A
Supply Current in Normal Mode	Bus recessive, V_S < 14V	LIN_V_{DD}	I_{VSrec}	150	250	320	µA	A
Supply Current in Normal Mode	Bus dominant (internal LIN pull-up resistor active),V_S < 14V	LIN_VDD	I_{VSdom}	200	700	950	µA	A

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Table 37-2. Electrical Characteristics (continued)

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type
Operating Conditions (unless otherwise stated): 5V < V_S < 28V, -40°C < T_J < +150°C; all values refer to LIN_V_{SS} pins								
Supply Current in Fail-Safe Mode	Bus recessive, V_S < 14V	LIN_V_{DD}	I_{VSfail}	40	80	110	µA	A
LIN_VDD Undervoltage Threshold (switching from Normal to Fail-Safe mode)	Decreasing supply voltage	LIN_V_{DD}	$V_{VS\_th\_N\_F\_down}$	3.9	4.3	4.7	V	A
	Increasing supply voltage	LIN_V_{DD}	$V_{VS\_th\_N\_F\_up}$	4.1	4.6	4.9	V	A
LIN_V_{DD} Undervoltage Hysteresis		LIN_V_{DD}	$V_{VS\_hys\_F\_N}$	0.1	0.25	0.4	V	A
LIN_V_{DD} Operation Threshold (switching to Unpowered mode)	Switch to Unpowered mode	LIN_V_{DD}	$V_{VS\_th\_U\_down}$	1.9	2.05	2.3	V	A
	Switch from Unpowered mode to Fail-Safe mode	LIN_VDD	$V_{VS\_th\_U\_F\_up}$	2.0	2.25	2.4	V	A
LIN_V_{DD} Undervoltage Hysteresis		LIN_V_{DD}	$V_{VS\_hys\_U}$	0.1	0.2	0.3	V	A
LIN_RXD Output Pin (open-drain)								
Low-Level Output Sink Capability	Normal mode, V_{LIN} = 0V, I_{RXD} = 2 mA	LIN_RXD	V_{RXDL}	—	0.2	0.4	V	A
High-Level Leakage Current	Normal mode, V_{LIN} = V_S, V_{RXD} = 5V	LIN_RXD	I_{RXDH}	-3	—	+3	µA	A
LIN_TXD Input/Output Pin								
Low-Level Voltage Input		LIN_TXD	V_{TXDL}	-0.3	—	+0.8	V	A
High-Level Voltage Input		LIN_TXD	V_{TXDH}	2	—	5.5	V	A
Pull-Down Resistor	V_{TXD} = 5V	LIN_TXD	R_{TXD}	150	200	300	kW	A
Low-Level Leakage Current	V_{TXD} = 0V	LIN_TXD	I_{TXD}	-3	—	+3	µA	A
Low-Level Output Sink Current at Wake-up Request	Fail-Safe mode, V_{TXD} = 0.4V	LIN_RXD	I_{TXD}	2	2.5	8	mA	A
LIN_EN Input Pin								
Low-Level Voltage Input		LIN_EN	V_{ENL}	-0/3	—	+0.8	V	A
High-Level Voltage Input		LIN_EN	V_{ENH}	2	—	5.5	V	A
Pull-Down Resistor	V_{EN} = 5V	LIN_EN	R_{EN}	50	125	200	kW	A

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Table 37-2. Electrical Characteristics (continued)

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type
Operating Conditions (unless otherwise stated): 5V < V_S < 28V, -40°C < T_J < +150°C; all values refer to LIN_V_{SS} pins								
Low-Level Input Current	V_{EN} = 0V	LIN_EN	I_{EN}	-3	—	+3	µA	A
LIN_WKIN Input Pin								
High-Level Input Voltage		LIN_WKIN	V_{WKinH}	V_S – 1V	—	V_S + 0.3V	V	A
Low-Level Input Voltage	Initializes a wake-up signal	LIN_WKIN	V_{WKinL}	-1	—	V_S – 3.3V	V	A
LIN_WKIN Pull-up Current	V_S < 28V, V_{WKin} = 0V	LIN_WKIN	I_{WKin}	-30	-10	—	µA	A
High-Level Leakage Current	V_S = 28V, V_{WKin} = 28V	LIN_WKIN	I_{WKinL}	-5	—	+5	µA	A
Debounce Time of Low Pulse for Wake-up via LIN_WKIN	V_{WKin} = 0V	LIN_WKIN	t_{WKin}	50	100	150	µs	A
LIN_INH Output Pin								
Switch-on Resistance Between LIN_V_{DD} and LIN_INH	Normal or Fail-Safe mode, I_{INH} = -15 mA	LIN_INH	$R_{DSon,INH}$	—	12	25	W	A
Leakage Current	Transceiver in Sleep mode, V_{INH} = 0V/28V, V_S = 28V	LIN_INH	$I_{leak,INH}$	-3	—	+3	µA	A
High-Level Voltage	Normal or Fail-Safe mode, I_{INH} = -15 mA	LIN_INH	V_{INH}	V_S – 0.375	—	V_S	V	A
LIN Bus Driver: Bus Load Conditions:Load 1 (small): 1 nF, 1 kW; Load 2 (large): 10 nF, 500W; External Pull-up, R_{RXD} = 4.7 kW; C_{RXD} = 20 pF; Load 3 (medium): 6.8 nF, 660W characterized on samples. Duty Cycle 1 and Duty Cycle 2 specify the timing parameters for proper operation at 20 kb/s and Duty Cycle 3 and Duty Cycle 4 at 10.4 kb/s.								
Driver Recessive Output Voltage	Load1/ Load2	LIN_BUS	V_{BUSrec}	0.9 x V_S	—	V_S	V	A
Driver Dominant Voltage	V_{VS} = 7V, R_{load} = 500W	LIN_BUS	V_{LoSUP}	—	—	1.2	V	A
Driver Dominant Voltage	V_{VS} = 18V, R_{load} = 500W	LIN_BUS	V_{HiSUP}	—	—	2	V	A
Driver Dominant Voltage	V_{VS} = 7V, R_{load} = 1000W	LIN_BUS	V_{LoSUP_1k}	0.6	—	—	V	A
Driver Dominant Voltage	V_{VS} = 18V, R_{load} = 1000W	LIN_BUS	V_{HiSUP_1k}	0.8	—	—	V	A

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Table 37-2. Electrical Characteristics (continued)

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type
Operating Conditions (unless otherwise stated): 5V < V_S < 28V, -40°C < T_J < +150°C; all values refer to LIN_V_{SS} pins								
Pull-up Resistor to LIN_V_{DD}	Serial diode is mandatory	LIN_BUS	R_{LIN}	20	30	47	kW	A
Voltage Drop at the Serial Diodes	In pull-up path with R_{slave}, $I_{SerDiode}$ = 10 mA	LIN_BUS	$V_{SerDiode}$	0.4	—	1.0	V	D
LIN_BUS Current Limitation	V_{BUS} = V_{Bat_max}	LIN_BUS	I_{BUS_LIM}	40	120	200	mA	A
Input Leakage Current at the Receiver Including Pull-up Resistor as Specified	Input leakage current driver off, V_{BUS} = 0V, V_{BAT} = 12V	LIN_BUS	$I_{BUS\_PAS\_dom}$	-1	-0.35	—	mA	A
Leakage Current LIN_BUS Recessive	Driver off, 8V < V_{BAT} < 18V, 8V < V_{BUS} < 18V, V_{BUS} >V_{BAT}	LIN_BUS	$I_{BUS\_PAS\_rec}$	—	10	20	µA	A
Leakage Current when Control Unit Disconnected from Ground;Loss of Local Ground must not Affect Communication in the Residual Network	GND_{Device} = V_S, V_{BAT} = 12V, 0V < V_{BUS} < 18V	LIN_BUS	$I_{BUS\_NO\_gnd}$	-10	+0.5	+10	µA	A
Leakage Current at Disconnected Battery; Node has to Sustain the Current that can Flow Under this Condition; Bus Must Remain Operational Under this Condition	V_{BAT} disconnected, V_{SUP_Device} = LIN_VSS, 0V < V_{BUS} < 18V	LIN_BUS	$I_{BUS\_NO\_bat}$	—	0.1	2	µA	A
Capacitance on Pin LIN_BUS to LIN_V_{SS}		LIN_BUS	C_{LIN}	—	—	20	pF	D
LIN Bus Receiver								

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Table 37-2. Electrical Characteristics (continued)

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type
Operating Conditions (unless otherwise stated): 5V < V_S < 28V, -40°C < T_J < +150°C; all values refer to LIN_V_{SS} pins								
Center of Receiver Threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2	LIN_BUS	V_{BUS_CNT}	0.475 x V_S	0.5 x V_S	0.525 x V_S	V	A
Receiver Dominant State	V_{EN} = 5V	LIN_BUS	V_{BUSdom}	-27	—	0.4 x V_S	V	A
Receiver Recessive State	V_{EN} = 5V	LIN_BUS	V_{BUSrec}	0.6 x V_S	—	40	V	A
Receiver Input Hysteresis	V_{hys} = V_{th_rec} – V_{th_dom}	LIN_BUS	V_{BUShys}	0.028 x V_S	0.1 x V_S	0.175 x V_S	V	A
Pre-Wake Detection LIN_BUS High-Level Input Voltage		LIN_BUS	V_{LINH}	V_S – 2V	—	V_S + 0.3V	V	A
Pre-Wake Detection LIN_BUS Low-Level Input Voltage	Activates the LIN receiver	LIN_BUS	V_{LINL}	-27	—	V_S – 3.3V	V	A
Internal Timers								
Dominant Time for Wake-up via LIN_BUS	V_{LIN} = 0V	LIN_BUS	t_{bus}	50	100	150	µs	A
Time Delay for Mode Change from Fail-Safe into Normal Mode viaLIN_EN Pin	V_{EN} = 5V	LIN_EN	t_{norm}	5	15	20	µs	A
Time Delay for Mode Change from Normal Mode to Sleep Mode via LIN_EN Pin	V_{EN} = 0V	LIN_EN	t_{sleep}	5	15	20	µs	A
Time Delay for Mode Change from Sleep Mode to Normal Mode via LIN_EN Pin	V_{EN} = 5V	LIN_EN	t_{s_norm}	—	150	300	µs	A
LIN_TXD Dominant Time-out Time	V_{TXD} = 0V	LIN_TXD	t_{dom}	20	40	60	ms	A

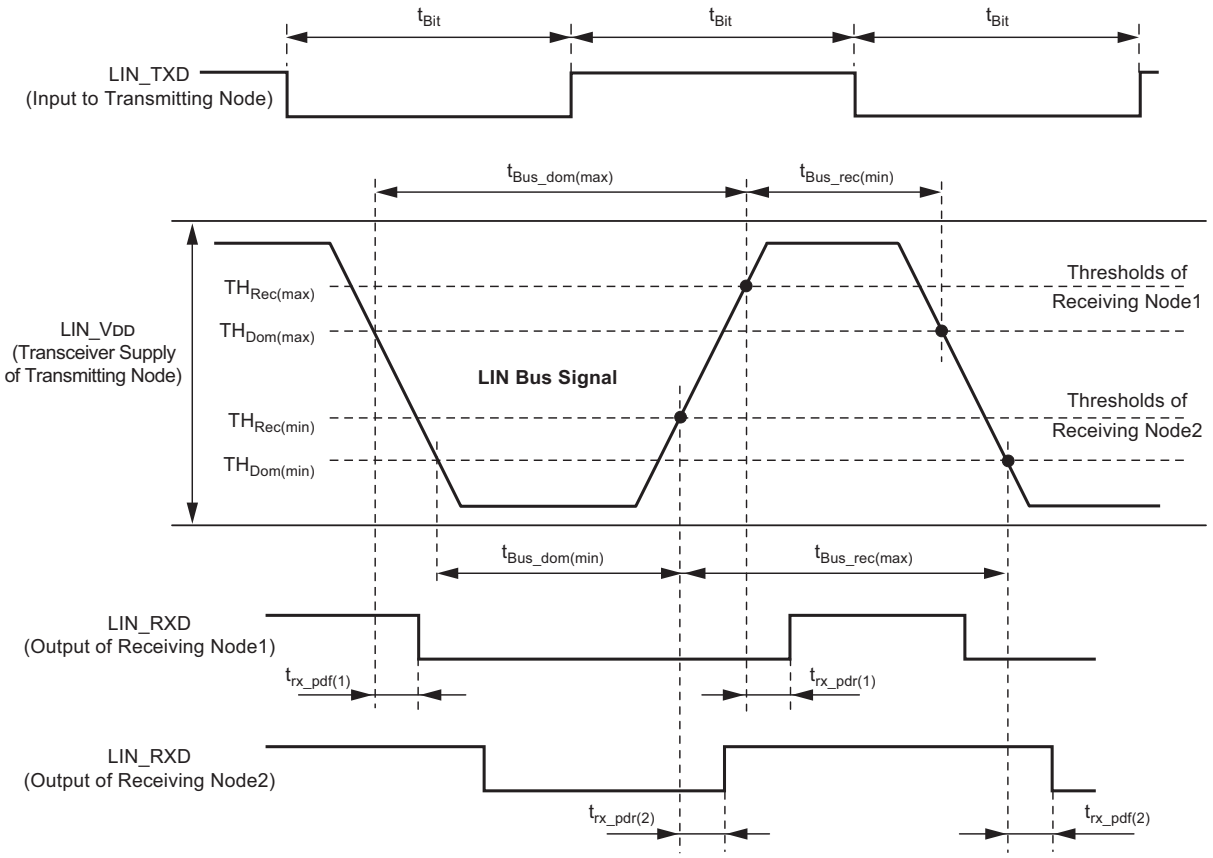
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Table 37-2. Electrical Characteristics (continued)

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type
Operating Conditions (unless otherwise stated): 5V < V_S < 28V, -40°C < T_J < +150°C; all values refer to LIN_V_{SS} pins								
Duty Cycle 1	$TH_{Rec(max)}$ = 0.744 x V_S, $TH_{Dom(max)}$ = 0.581 x V_S, V_S = 7.0V to 18V, t_{Bit} = 50 µs, D1 = t_{bus_rec} (min) / (2 x t_{Bit})	LIN_BUS	D1	0.396	—	—	—	A
Duty Cycle 2	$TH_{Rec(min)}$ = 0.422 x V_S, $TH_{Dom(min)}$ = 0.284 x V_S, V_S = 7.6V to 18V, t_{Bit} = 50 µs, D2 = t_{bus_rec} (max) / (2 x t_{Bit})	LIN_BUS	D2	—	—	0.581	—	A
Duty Cycle 3	$TH_{Rec(max)}$ = 0.778 x V_S, $TH_{Dom(max)}$ = 0.616 x V_S, V_S = 7.0V to 18V, t_{Bit} = 96 µs, D3 = t_{bus_rec} (min) / (2 x t_{Bit})	LIN_BUS	D3	0.417	—	—	—	A
Duty Cycle 4	$TH_{Rec(max)}$ = 0.778 x V_S, $TH_{Dom(max)}$ = 0.616 x V_S, V_S = 7.0V to 18V, t_{Bit} = 96 µs, D4 = t_{bus_rec} (max) / (2 x t_{Bit})	LIN_BUS	D4	—	—	0.590	—	A
Slope Time Falling and Rising Edge at LIN_BUS	V_S = 7.0V to 18V	LIN_BUS	t_{SLOPE_fall},t_{SLOPE_rise}	3.5	—	22.5	µs	A
Receiver Electrical AC Parameters of the LIN Physical Layer;LIN Receiver, LIN_RXD Load Conditions: C_{RXD} = 20 pF, R_{RXD} = 4.7 kW								
Propagation Delay of Receiver	V_S = 7.0V to 18V, t_{rx_pd} = max(t_{rx_pdr}, t_{rx_pdf})	LIN_RXD	t_{rx_pd}	—	—	6	µs	A
Symmetry of Receiver Propagation Delay Rising Edge Minus Falling Edge	V_S = 7.0V to 18V, t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf}	LIN_RXD	t_{rx_sym}	-2	—	+2	µs	A
Legend: Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design Parameter								

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Figure 37-1. Definition of LIN Bus Timing Characteristics

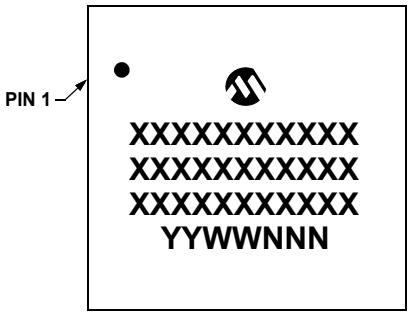


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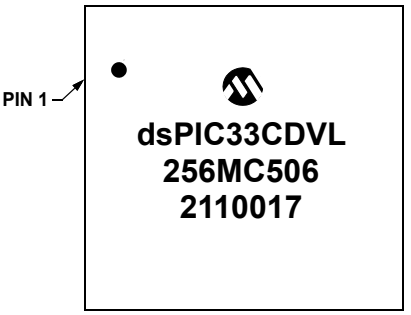
38. Packaging Information

38.1. Package Marking Information

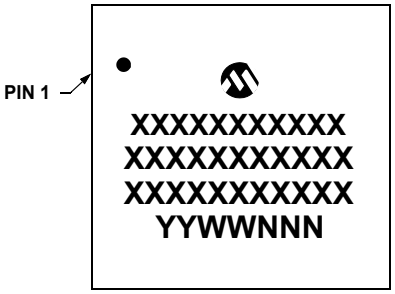
64-Lead VGQFN (9x9 mm)



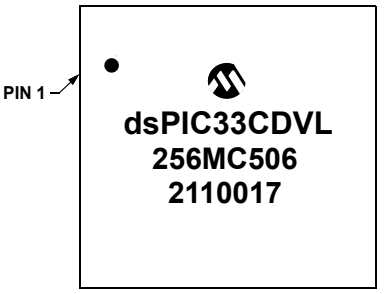
Example



64-Lead VGQFN (8x8 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

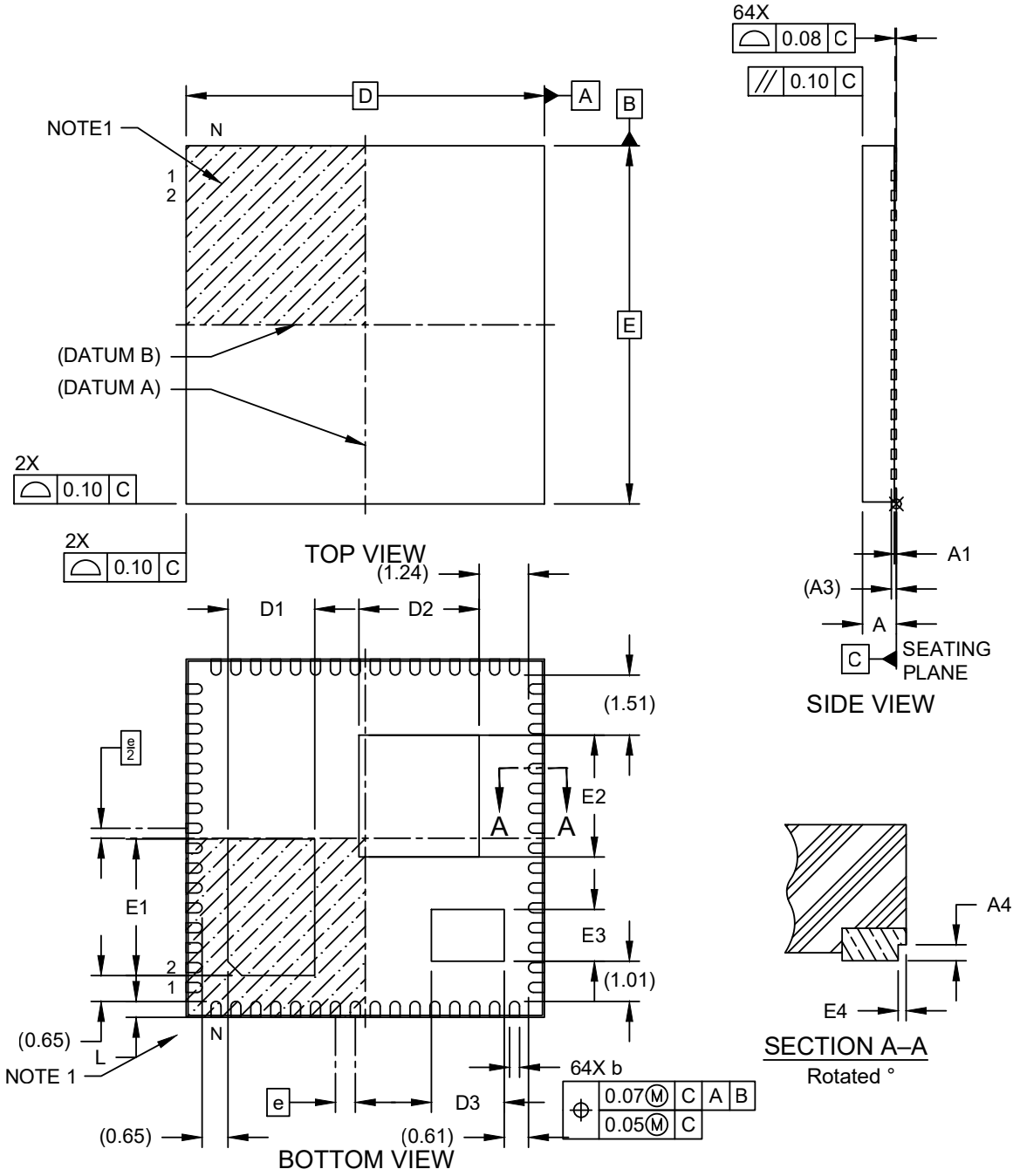
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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38.2. Package Details

64-Lead Very-Thin Grid-Array Quad Flatpack No-Lead Package (8QW) - 9x9x0.927 mm Body [VGQFN] with 3 Exposed Pads and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

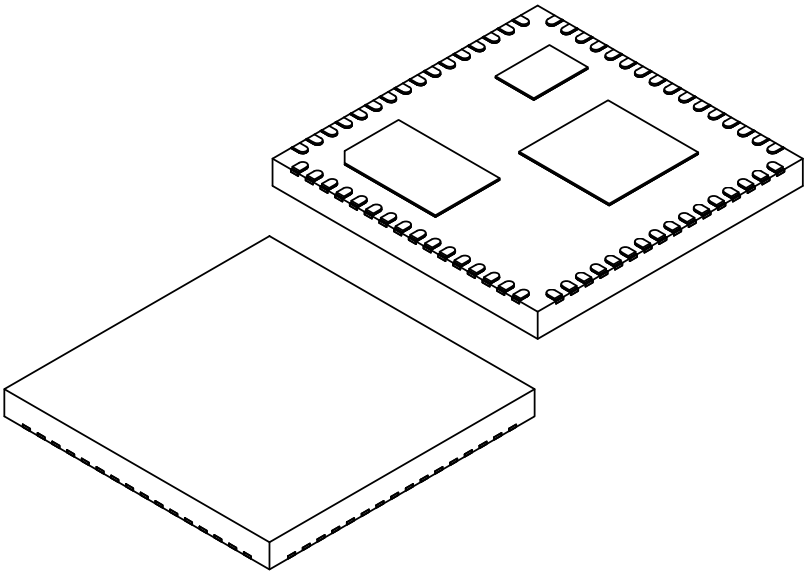


Microchip Technology Drawing C04-00669 Rev B Sheet 1 of 2

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64-Lead Very-Thin Grid-Array Quad Flatpack No-Lead Package (8QW) - 9x9x0.927 mm Body [VGQFN] with 3 Exposed Pads and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.827	0.877	0.927
Standoff	A1	0.00	-	0.05
Terminal Thickness	A3		0.127 REF	
Overall Length	D		9.00 BSC	
Overall Width	E		9.00 BSC	
Exposed Pad 1 Length	D1	2.08	2.18	2.28
Exposed Pad 1 Width	E1	3.33	3.43	3.53
Exposed Pad 2 Length	D2	2.92	3.02	3.12
Exposed Pad 2 Width	E2	2.96	3.06	3.16
Exposed Pad 3 Length	D3	1.73	1.83	1.93
Exposed Pad 3 Width	E3	1.20	1.30	1.40
Terminal Width	b	0.175	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Wettable Flank Step Cut Width	E4	0.01	0.05	0.09
Wettable Flank Step Cut Depth	A4	0.03	-	-

Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. The package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M

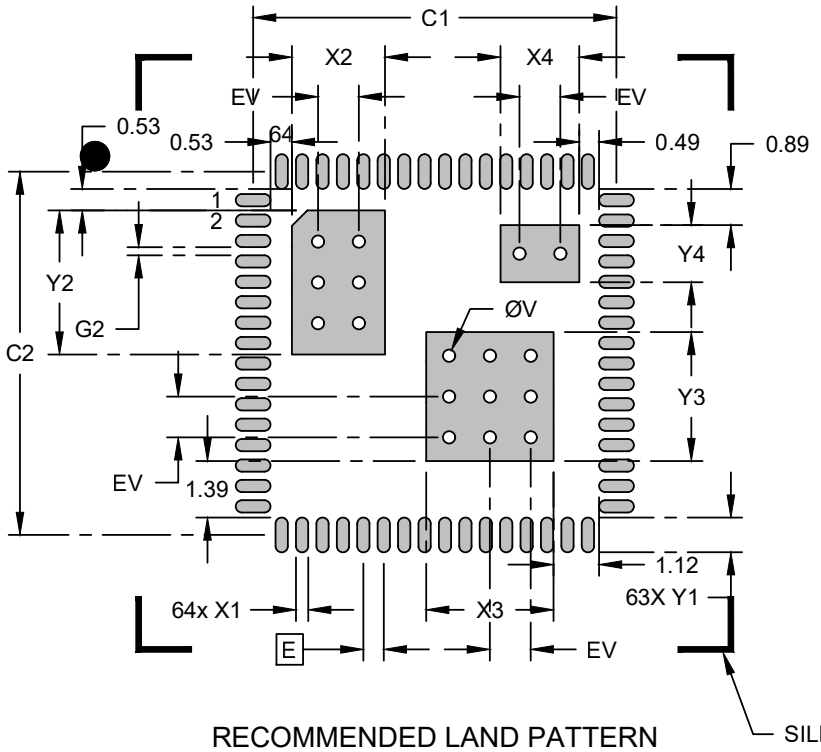
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
   REF: Reference Dimension, usually without tolerance, is for information purposes only.

Microchip Technology Drawing C04-00669 Rev B Sheet 2 of 2

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64-Lead Very-Thin Grid-Array Quad Flatpack No-Lead Package (8QW) - 9x9x0.927 mm Body [VGQFN] with 3 Exposed Pads and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Contact Pad to Contact Pad (X60)	G2	0.20		
Thermal Via Diameter	V		1.00	
Thermal Via Pitch	EV		0.30	

Units		MM
Dimension Limits		MAX
Center Pad 1 Width	X2	2.28
Center Pad 1 Length	Y2	3.53
Center Pad 2 Width	X3	3.12
Center Pad 2 Length	Y3	3.16
Center Pad 3 Width	X4	1.93
Center Pad 3 Length	Y4	1.40

Notes:

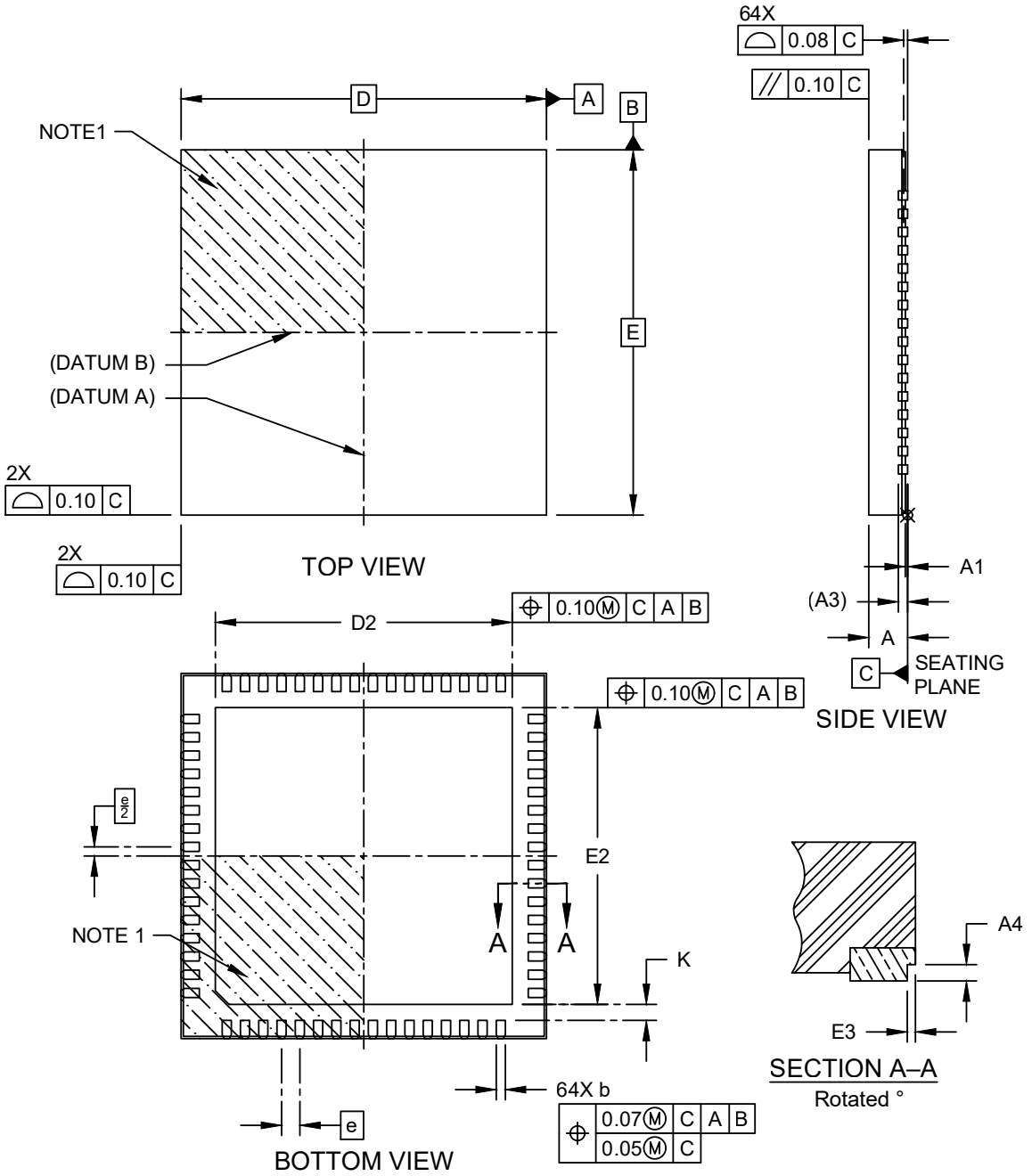
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
2. For best soldering results, please refer to the current industry standard IPC-7093.

Microchip Technology Drawing C04-02669 Rev B

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64-Lead Very-Thin Quad Flatpack No-Lead Package (8PW) - 8x8x0.9 mm Body [VQFN] With 6.5x6.5 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

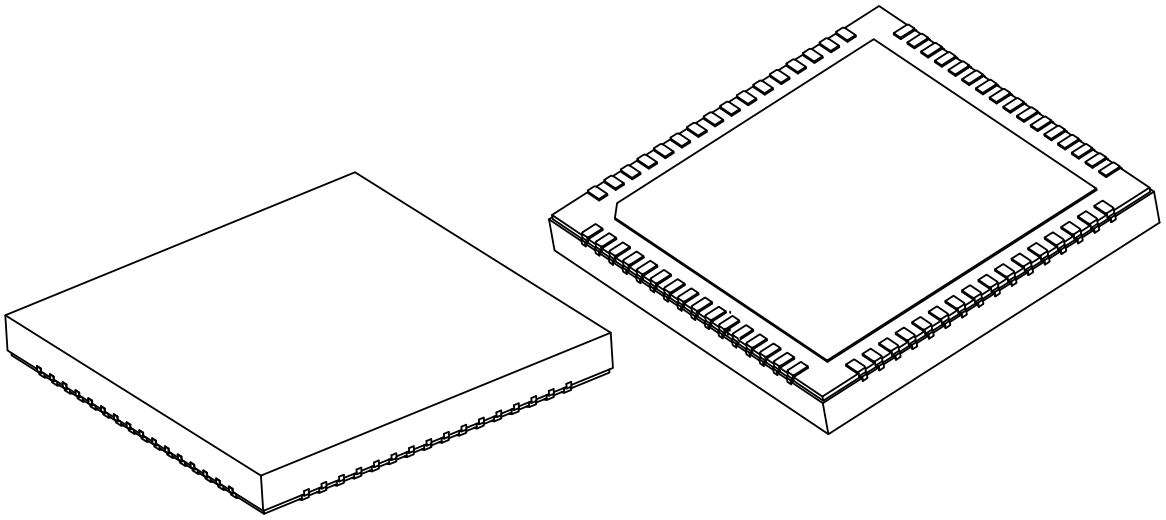


Microchip Technology Drawing C04-00668 Rev A Sheet 1 of 2

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64-Lead Very-Thin Quad Flatpack No-Lead Package (8PW) - 8x8x0.9 mm Body [VQFN] With 6.5x6.5 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		64	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.40	6.50	6.60
Overall Width	E		8.0 BSC	
Exposed Pad Width	E2	6.40	6.50	6.60
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.35	-	-
Wettable Flank Step Cut Width	E3	0.001	-	0.04
Wettable Flank Step Cut Depth	A4	0.100	0.125	0.150

Notes:

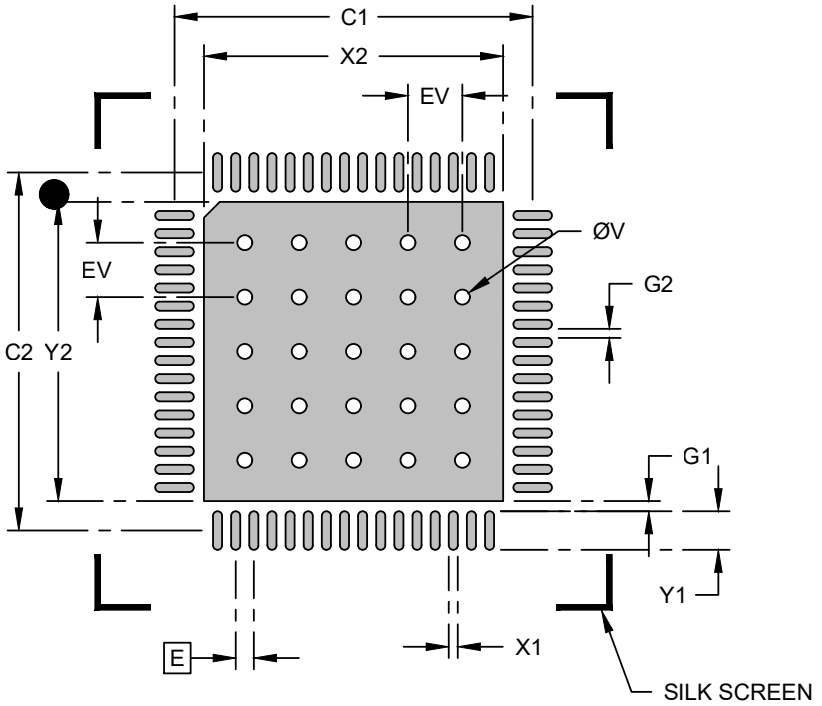
1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. The package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
   REF: Reference Dimension, usually without tolerance, is for information purposes only.

Microchip Technology Drawing C04-00668 Rev A Sheet 2 of 2

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64-Lead Very-Thin Quad Flatpack No-Lead Package (8PW) - 8x8x0.9 mm Body [VQFN] With 6.5x6.5 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40	
Center Pad Width	X2			6.60
Center Pad Length	Y2			6.60
Contact Pad Spacing	C1		7.90	
Contact Pad Spacing	C2		7.90	
Contact Pad Width (Xnn)	X1			0.20
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.23		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
2. For best soldering results, please refer to the current industry standard IPC-7093.

Microchip Technology Drawing C04-02668 Rev A

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39. Revision History

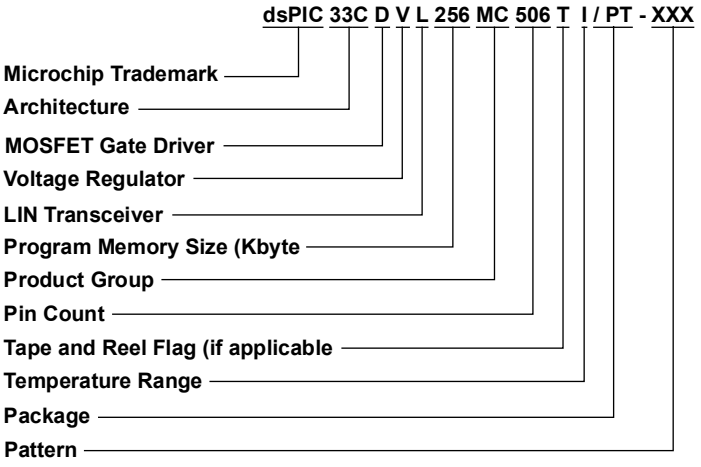
Revision A (February 2026)

This is the initial version of the document.

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40. Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.



Device:	dsPIC33CDVL256MC506, dsPIC33CDV256MC506, dsPIC33CDVL128MC506, dsPIC33CDV128MC506, dsPIC33CDVL256MC106, dsPIC33CDV256MC106, dsPIC33CDVL128MC106, dsPIC33CDV128MC106	
Architecture:	33	16-Bit Digital Signal Controller
Flash Memory Family:	C	Single Core
Product Group:	MC	Motor Control
Pin Count:	06	64-pin
Tape & Reel Option:	Blank	Tube or Tray
	T	Tape & Reel
Temperature Range:	I	-40°C to +85°C (Industrial)
	E	-40°C to +125°C (Extended)
	H	-40°C to +150°C (High)
Package:	8QW	64L VGQFN (9mm)
	8PW	64L VQFN (8mm)

Examples:

- dsPIC33CDVL256MC506-I/8QW: dsPIC33, Enhanced Performance, 256-Kbyte Program Memory, 64-Pin, Industrial Temperature, 9mm VGQFN package.

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

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ISBN: 979-8-3371-1999-1

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