Obsolete Device

CW01

4-Channel Low-Phase-Noise Low-Power Continuous Wave Transmitter

Features

- Low Phase Noise
- 100V Open Drain N-channel
- High-speed D Flip-flop
- High-speed MOSFET Gate Driver
- Up to 200 MHz Clock Input
- V_{DD} and V_{LL} Undervoltage Lockout

Applications

- Diagnostic Medical Ultrasound
- Fluid Flow Measurement

General Description

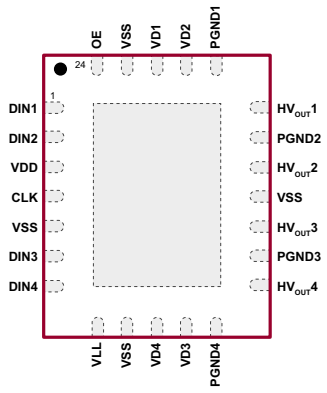
The CW01 is a 4-channel low-phase-noise continuous wave transmitter IC. A high-speed D flip-flop is provided to allow the D_{IN} frequency to be aligned to a high-frequency clock. The output N-channel is turned on when a logic high is clocked into the D flip-flop. Data are clocked-in during the low-to-high transition.

V_{D1}, V_{D2}, V_{D3} and V_{D4} are four individual input supply voltages for the N-channel output MOSFET gate drivers. High peak currents are drawn from these gate drives when the output MOSFETs are switching. To minimize jitter caused by voltage ripples, each channel has its own gate drive voltage pin—V_{D1}, V_{D2}, V_{D3} and V_{D4}. A series ferrite bead and a decoupling capacitor are recommended on each V_{DX} pin to minimize output jitter and channel-to-channel crosstalk.

Both V_{DD} and V_{LL} have undervoltage lockout to prevent spurious turn-on.

Package Type

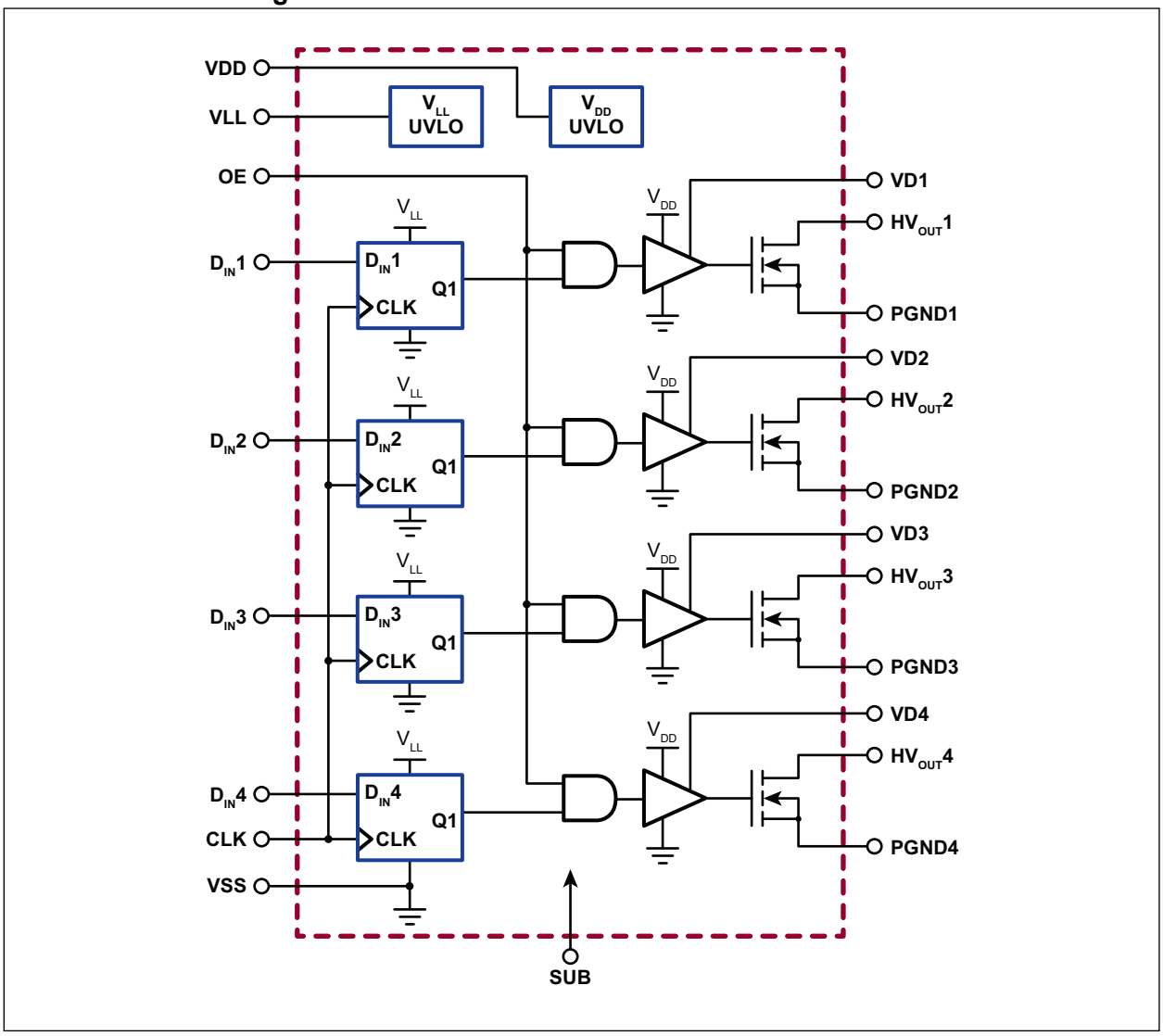
24-lead QFN
(Top view)



See Table 2-1 for pin information.

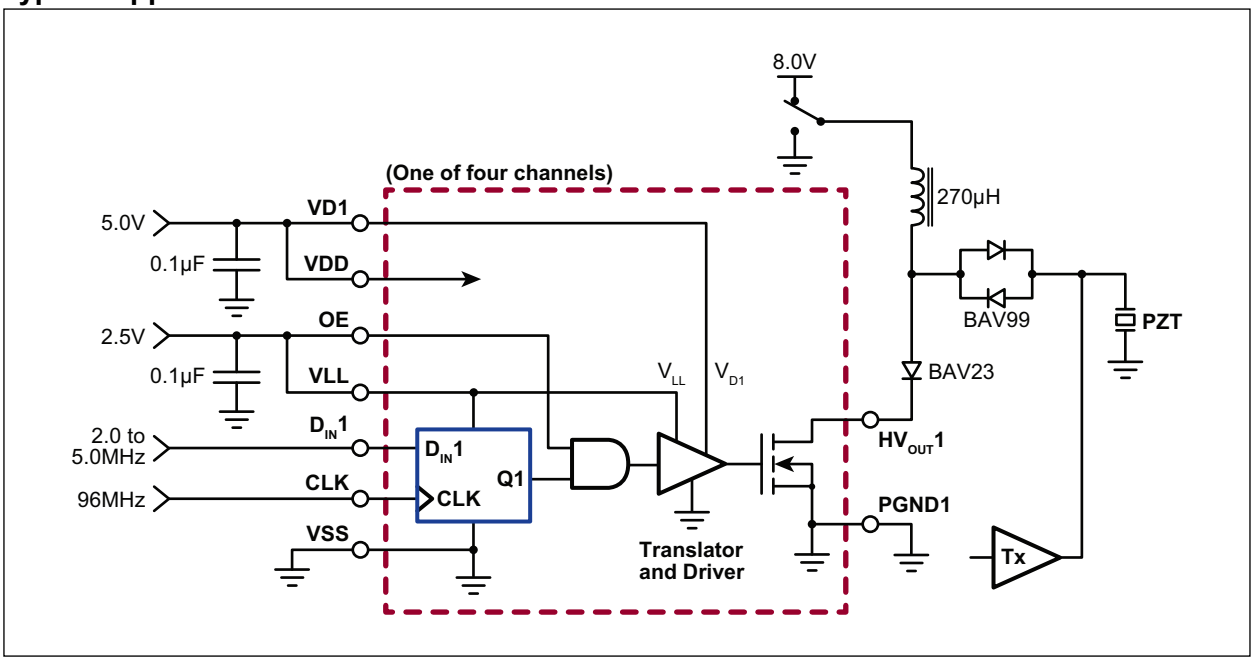
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Functional Block Diagram



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Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Logic Supply, V_{LL} ..... –0.3V to +6V
Level Translator Voltage, V_{DD} ..... –0.5V to +6V
Gate Drive Voltage, V_{DX} ..... –0.5V to +6V
High-voltage Output Drain Voltage, HV_{OUT} ..... –0.5 to +120V
Operating Junction Temperature, T_J ..... –40°C to +125°C
Storage Temperature, T_S ..... –65°C to +150°C
Power Dissipation (T_A = 25°C):
24-lead QFN 3W

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{DD} = V_{DX} = 5V, V_{LL} = 2.5V, T_J = 25ºC unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
High-voltage Output	HV_{OUT}	0	—	100	V	
V_{DD} Voltage Range	V_{DD}	4.5	5	5.5	V	
V_{DD} Rise Time	$t_{VDD–ON}$	50	—	—	µs	
V_{LL} Voltage Range	V_{LL}	1.65	2.5	5.5	V	
V_{LL} Rise Time	$t_{VLL–ON}$	50	—	—	µs	
Logic Input Voltage Range	V_{DIN}	0	—	V_{LL}	V	
Gate Drive Voltage	V_{DX}	4.5	5	5.5	V	
V_{DX} Rise Time	$t_{VDX–ON}$	50	—	—	µs	
V_{DD} Quiescent Current	I_{DDQ}	—	63	100	µA	
V_{DD} Average Current	I_{DD}	—	23.5	30	mA	f_{CLK} = 200 MHz, f_{OUT} = 5 MHz, All four channels active
V_{LL} Quiescent Current	I_{LLQ}	—	8.1	20	µA	
V_{LL} Average Current	I_{LL}	—	380	600	µA	f_{CLK} = 200 MHz, f_{OUT} = 5 MHz, All four channels active
V_{DX} Quiescent Current	I_{DXQ}	—	0	1	µA	
V_{DX} Average Current	I_{DX}	—	11.3	30	mA	f_{CLK} = 200 MHz, f_{OUT} = 5 MHz, All four channels active
Input Logic High Voltage	V_{IH}	0.8 V_{LL}	—	V_{LL}	V	
Input Logic Low Voltage	V_{IL}	0	—	0.2 V_{LL}	V	
Input Logic High Current	I_{IH}	—	—	1	µA	
Input Logic High Current	I_{IL}	–1	—	—	µA	
Output On-resistance	R_{ON}	—	4.7	7	Ω	I_{IN} = 100 mA
Output Saturation Current	I_{SAT}	—	0.8	—	A	V_{DD} = HV_{OUT} = 5V
High-voltage Output Leakage	I_{HVleak}	—	—	10	µA	HV_{OUT} = 100V
UVLO Trip Point for V_{LL}	UVLO_V_{LL}	—	1.5	—	V	
UVLO Trip Point for V_{DD}	UVLO_V_{DD}	—	4	—	V	

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AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{DD} = V_{DX} = 5V, V_{LL} = 2.5V, T_J = 25ºC unless otherwise specified.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Clock Frequency	f_{CLK}	0	—	200	MHz	
Clock Rise and Fall Times	t_r, t_f	—	0.5	5	ns	
Set-up Time, D_{IN} to CLK	t_{SU}	2	—	—	ns	
Hold Time, D_{IN} from CLK	t_H	1	—	—	ns	
HV_{OUT} Fall Time	t_{HVf}	—	0.8	—	ns	Load = 50Ω to 8V (See **Timing Waveforms**.)
HV_{OUT} Rise Time	t_{HVr}	—	3.3	—	ns	Load = 50Ω to 8V (See **Timing Waveforms**.)
Delay Time from CLK to HV_{OUT} from Low to High	t_{dLH}	—	5.1	—	ns	Load = 50Ω to 8V (See **Timing Waveforms**.)
Delay Time from CLK to HV_{OUT} from High to Low	t_{dHL}	—	2.6	—	ns	Load = 50Ω to 8V (See **Timing Waveforms**.)
Delay Time Matching for t_{dLH}	$\Delta t_{dLHdelay}$	—	0.5	1	ns	
Delay Time Matching for t_{dHL}	$\Delta t_{dHLdelay}$	—	0.5	1	ns	
Output Enable Turn-on Time	$t_{OE(ON)}$	—	—	10	µs	
Output Enable Turn-off Time	$t_{OE(OFF)}$	—	—	0.1	µs	
Output Capacitance	C_{OUT}	—	8	—	pF	At 8V
		—	4	—	pF	At 100V
Phase Noise	N_{Phase}	—	–171	–160	dBC/Hz	dB below carrier, CLK = 80 MHz, D_{IN} = 2 MHz, Frequency offset = 1 kHz, Noise bandwidth = 140 Hz (See Figure 3-1 and Figure 3-2.)

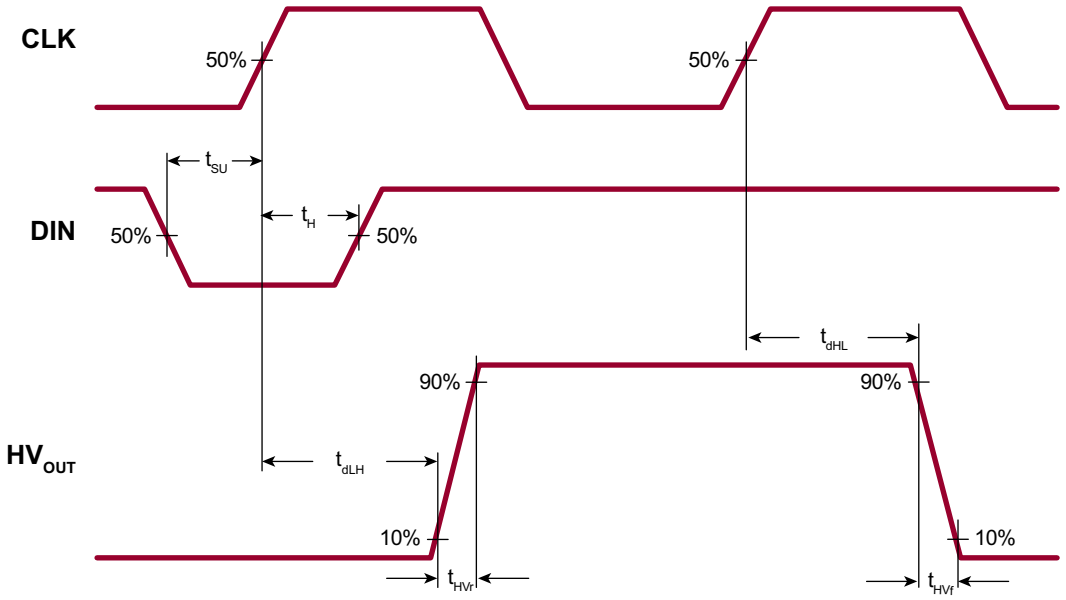
TEMPERATURE SPECIFICATIONS

Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	–40	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
24-lead QFN	θ_{JA}	—	26.9	—	°C/W	**Note 1**

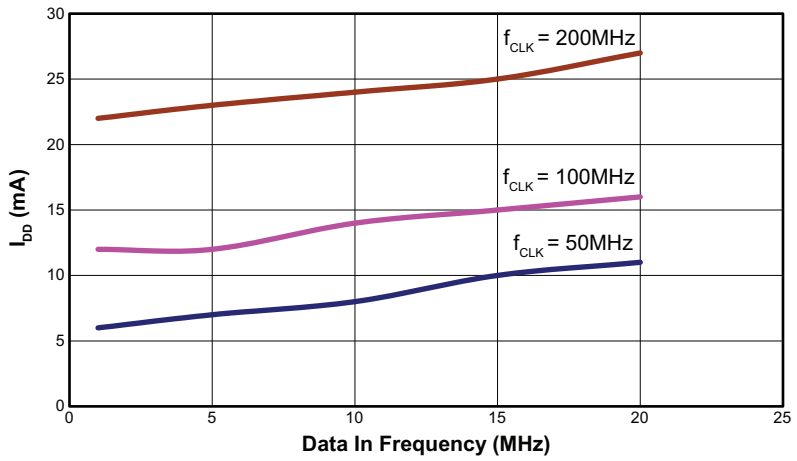
Note 1: Device is mounted on a 4-layer 3” by 4” board.

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Timing Waveforms



Typical Performance Curve



I_{DD} vs. D_{IN} Frequency

(Test conditions: V_{LL} = 2.5V, V_{DD} = 5V, V_{D1} = V_{D2} = V_{D3} = V_{D4} = 5V, no load)

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2.0 PIN DESCRIPTION

Table 2-1 shows the description of pins in CW01.
Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	DIN1	D flip-flop logic input for HVOUT1. Logic high will turn on output N-channel.
2	DIN2	D flip-flop logic input for HVOUT2. Logic high will turn on output N-channel.
3	VDD	Level translator supply. Should be at the same potential as VDX.
4	CLK	Logic clock input
5	VSS	Ground. Should be externally shorted to all PGND and VSS pins.
6	DIN3	D flip-flop logic input for HVOUT3. Logic high will turn on output N-channel.
7	DIN4	D flip-flop logic input for HVOUT4. Logic high will turn on output N-channel.
8	VLL	Logic input supply voltage
9	VSS	Ground. Should be externally shorted to all PGND and VSS pins.
10	VD4	Gate drive supply voltage for HVOUT4. Should be at the same potential as VDD.
11	VD3	Gate drive supply voltage for HVOUT3. Should be at the same potential as VDD.
12	PGND4	Power ground for HVOUT4. Should be externally shorted to all PGND and VSS pins.
13	HVOUT4	Drain output for HVOUT4
14	PGND3	Power ground for HVOUT3. Should be externally shorted to all PGND and VSS pins.
15	HVOUT3	Drain output for HVOUT3
16	VSS	Ground. Should be externally shorted to all PGND and VSS pins.
17	HVOUT2	Drain output for HVOUT2
18	PGND2	Power ground for HVOUT2. Should be externally shorted to all PGND and VSS pins.
19	HVOUT1	Drain output for HVOUT1
20	PGND1	Power ground for HVOUT1. Should be externally shorted to all PGND and VSS pins.
21	VD2	Gate drive supply voltage for HVOUT2. Should be at the same potential as VDD.
22	VD1	Gate drive supply voltage for HVOUT1. Should be at the same potential as VDD.
23	VSS	Ground. Should be externally shorted to all PGND and VSS pins.
24	OE	Output enable logic input. Logic low will turn off all HVOUT.
Center Pad		Should be externally shorted to all PGND and VSS pins.

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3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 and Figure 3-2 illustrate the test circuits for CW01.

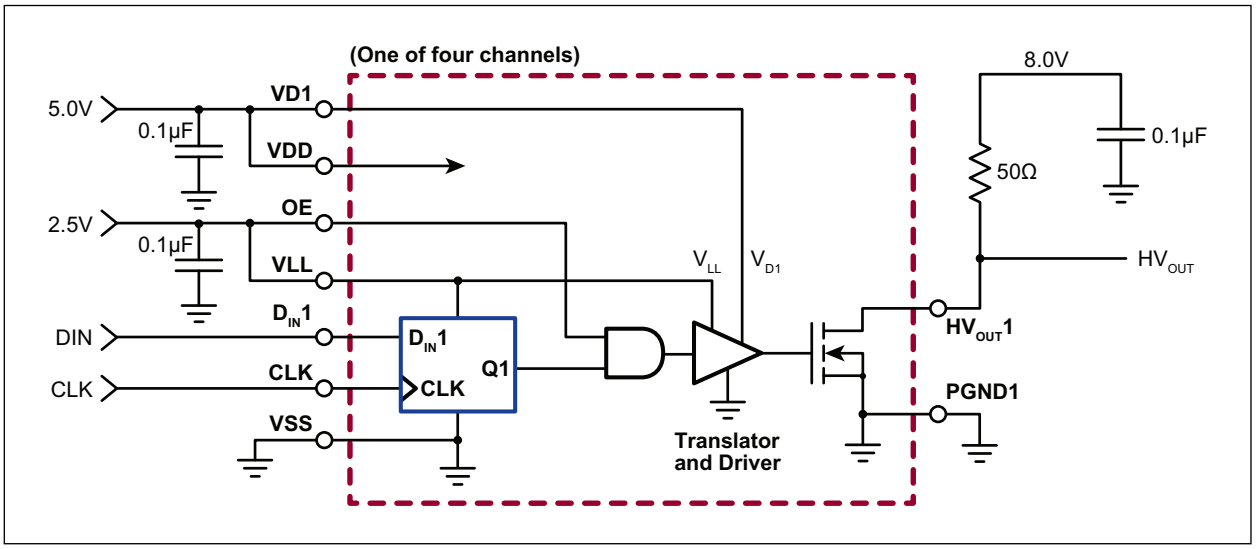


FIGURE 3-1: *AC Timing.*

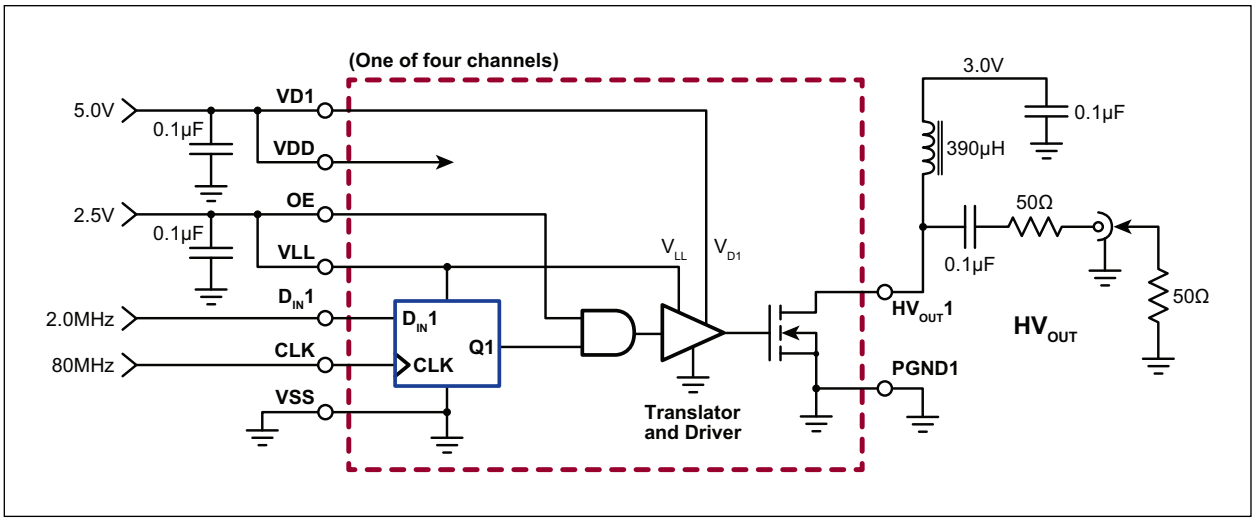


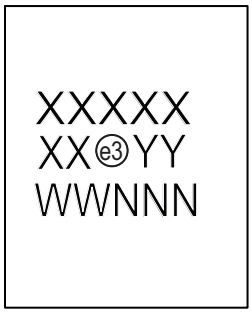
FIGURE 3-2: *Phase Noise.*

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4.0 PACKAGING INFORMATION

4.1 Package Marking Information

24-lead QFN



Example

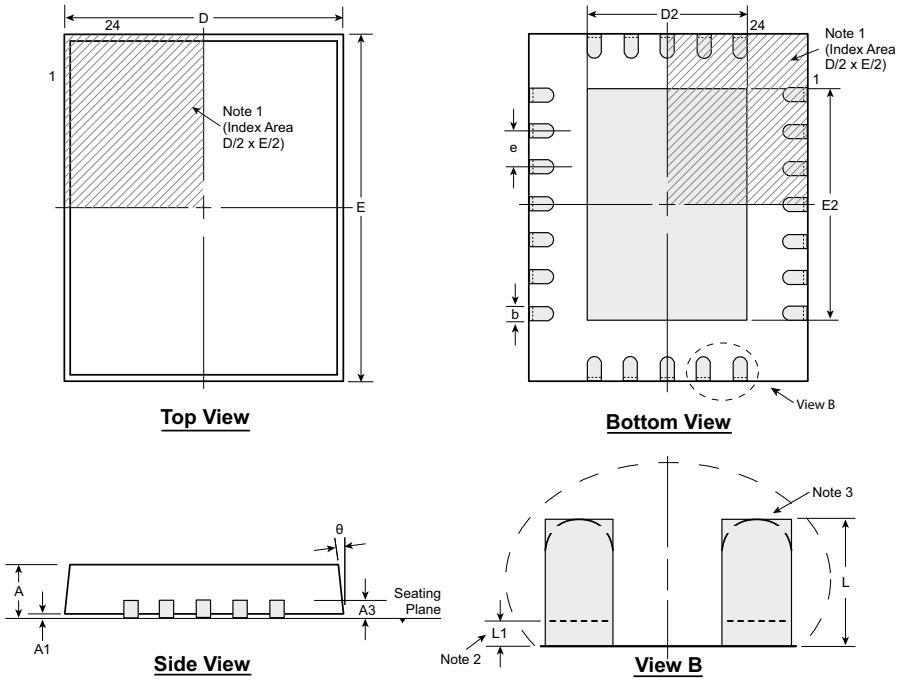


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

24-Lead QFN Package Outline (K6)

4.00x5.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	3.85*	2.50	4.85*	3.50	0.50 BSC	†0.30	0.00	0°
	NOM	0.90	0.02		0.25	4.00	2.65	5.00	3.65		0.40	-	-
	MAX	1.00	0.05		0.30	4.15*	2.80	5.15*	3.80		†0.50	0.15	14°

JEDEC Registration MO-220, Variation VGHD-1, Issue K, June 2006
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

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APPENDIX A: REVISION HISTORY

Revision B (February 2026)

- Added the Obsolete Device label on the first page.

Revision A (July 2017)

- Converted Supertex Doc# DSFP-CW01 to Microchip DS20005810B
- Changed the package marking format
- Made minor text changes throughout the document

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	CW01	=	Four-Channel Low-Phase-Noise Low-Power Continuous Wave Transmitter
Package:	K6	=	24-lead QFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	3000/Reel for a K6 Package

Example:

a) CW01K6-G: Four-Channel Low-Phase-Noise Low-Power Continuous Wave Transmitter, 24-lead QFN, 3000/Reel

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