ZL40294B

20-Output DB2000QL PCIe Buffer with Ultra-Low Additive Jitter

Features

- Fully Compliant with Intel DB2000QL Specification
- 20 Low-Power Push-Pull HCSL PCIe Outputs
- Supports Latest PCIe Gen 5.0, Gen 6.0, and Gen 7.0 Spec
- Ultra-Low Additive Jitter: 12 fs Typical in DB2000QL Band
- PCIe Gen 6 Additive Phase Jitter: 4 fs Typical RMS
- PCIe Gen 7 Additive Phase Jitter: 3.5 fs Typical RMS
- 12 kHz to 20 MHz Additive Phase Jitter: 32 fs Typical at 156.25 MHz
- Supports Clock Frequencies from 0 MHz to 400 MHz
- Supports 3.3V Power Supplies
- Embedded Low Drop Out (LDO) Voltage Regulator Provides Superior Power Supply Noise Rejection
- Maximum Output to Output Skew of 50 ps
- SMBus Interface
- Side-Band Interface (SBI)
- Eight OE Pins
- Embedded Series Termination Resistors for 85Ω Differential Transmission Line
- Transparent for Spread Spectrum Clock
- Extended temperature range -40°C to +105°C

Applications

- PCI Express Generation 1/2/3/4/5/6/7 Clock Distribution
- Intel QPI
- Servers
- Storage and Data Centers
- Switches and Routers

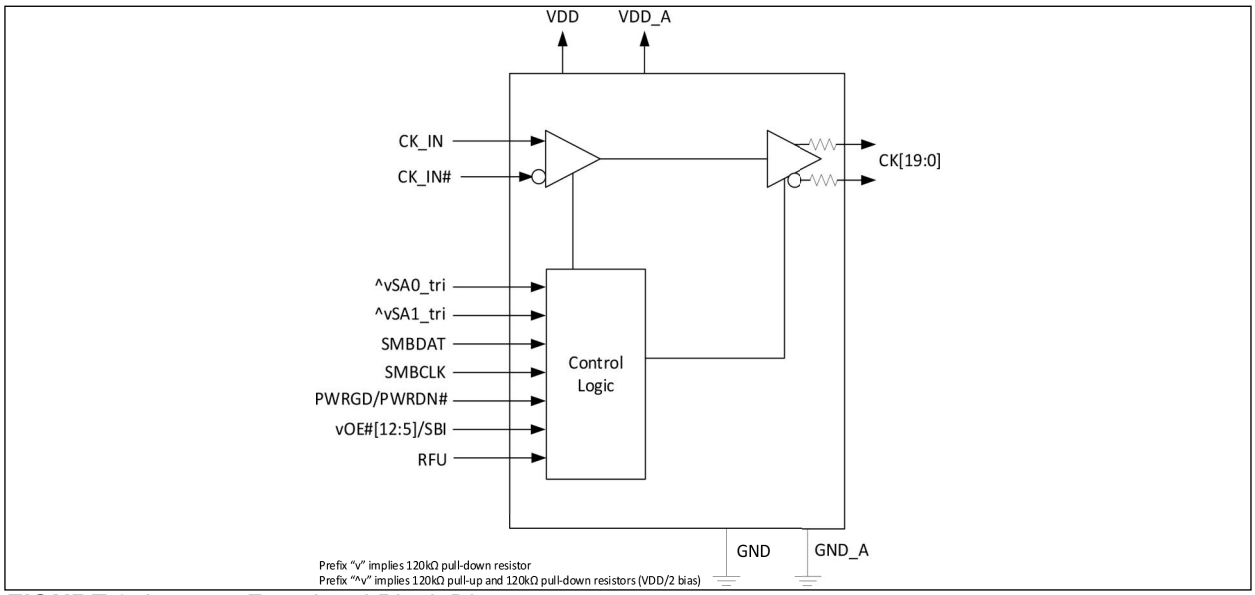

FIGURE 0-1: *Functional Block Diagram*

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TABLE OF CONTENTS

1.0 “Pin Diagram” **6**
2.0 “Pin Descriptions” **7**
3.0 “Functional Description” **11**
3.1 “Clock Inputs” 11
3.2 “Clock Outputs” 12
3.3 “Termination of Unused Outputs” 12
3.4 “Power Supply Filtering” 12
3.5 “OE# and Output Enables (Control Register)” 13
3.6 “OE# Assertion (Transition from ‘1’ to ‘0’)” 13
3.7 “OE# De-Assertion (Transition from ‘0’ to ‘1’)” 13
3.8 “PWRGD/PWRDN#” 14
3.9 “PWRDN# Assertion” 14
3.10 “PWRGD Assertion” 14
3.11 “Programming via SMBus” 15
3.12 “SMBus Byte Read/Write” 16
3.13 “SMBus Block Read/Write” 17
3.14 “Side-Band Interface” 17
3.15 “Typical Jitter Performance” 19
4.0 “Register Maps” **21**
5.0 “AC and DC Electrical Characteristics” **27**
5.1 “Absolute Maximum Ratings” 27
5.2 “DC Electrical Specification” 27
5.3 “AC Electrical Specification” 30
5.4 “Side-Band Interface Characteristics” 36
6.0 “Packaging Information” **39**
6.1 “Package Marking Information” 39
7.0 “Package Outline” **40**
8.0 “Acronyms and Abbreviations” **43**
Appendix A: “Data Sheet Revision History” **44**
“Product Identification System” **45**

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List of Figures

FIGURE 0-1: “Functional Block Diagram” 1
FIGURE 1-1: “Pin Diagram.” 6
FIGURE 3-1: “Input Driven by a Push-Pull Differential Output.” 11
FIGURE 3-2: “Input Driven by an HCSL Output.” 11
FIGURE 3-3: “Input Driven by a Single-Ended Output.” 12
FIGURE 3-4: “Terminating Differential Outputs.” 12
FIGURE 3-5: “Power Supply Filtering.” 13
FIGURE 3-6: “PWRDN# Assertion” 14
FIGURE 3-7: “PWRGD and VDD Relationship Diagram.” 15
FIGURE 3-8: “PWRGD Assertion.” 15
FIGURE 3-9: “SMBus Byte Read.” 16
FIGURE 3-10: “SMBus Byte Write.” 16
FIGURE 3-11: “SMBus Block Read.” 17
FIGURE 3-12: “SMBus Block Write.” 17
FIGURE 3-13: “Side-Band Interface Control Logic (Functional Description).” 18
FIGURE 3-14: “Side-Band Interface Functional Timing.” 18
FIGURE 3-15: “Phase Noise Plot.” 19
FIGURE 5-1: “DC Test Load (as per DB2000QL).” 28
FIGURE 5-2: “Single-Ended Measurement Points for t_{RISE} and tFALL.” 29
FIGURE 5-3: “Single-Ended Measurement Points for V_{OVS}, VUDS, VRB.” 29
FIGURE 5-4: “Differential (CK, CK#) Measurement Points.” 29
FIGURE 5-5: “AC Test Load as per DB2000QL Specifications.” 33
FIGURE 5-6: “SMBus Timing.” 36
FIGURE 5-7: “Side-Band Interface Timing.” 36

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List of Tables

TABLE 2-1: “Pin Descriptions” 7
TABLE 3-1: “OE Functionality” 13
TABLE 3-2: “PWRGD/PWRDN# Functionality” 14
TABLE 3-3: “SMBus Address Table” 16
TABLE 4-1: “Byte 0: Output Enable” 21
TABLE 4-2: “Byte 1: Output Enable Control Register” 21
TABLE 4-3: “Byte 2: Output Enable Control Register” 21
TABLE 4-4: “Byte 3: OE# Pin Realtime Readback Control Register” 22
TABLE 4-5: “Byte 4: Reserved Control Register” 22
TABLE 4-6: “Byte 6: Device ID Control Register” 23
TABLE 4-7: “Byte 7: Byte Count Register” 23
TABLE 4-8: “Byte 8: SBI Mask (Functional Only when SBEN = 1)” 24
TABLE 4-9: “Byte 9: SBI Mask (Functional Only When SBEN = 1)” 24
TABLE 4-10: “Byte 10: SBI Mask (Functional Only when SBEN = 1)” 25
TABLE 5-1: “Absolute Maximum Ratings*” 27
TABLE 5-2: “DC Operating Characteristics*” 27
TABLE 5-3: “Differential DC Output Characteristics*” 28
TABLE 5-4: “Power Noise Tolerance*” 30
TABLE 5-5: “Skew and Jitter: Normal Input Clock Conditions” 30
TABLE 5-6: “Skew and Jitter: Degraded Input Clock Conditions” 32
TABLE 5-7: “Differential Output Clock AC Characteristics” 34
TABLE 5-8: “Differential Input Clock AC Characteristics” 34
TABLE 5-9: “Current Consumption” 34
TABLE 5-10: “SMBus Electrical Characteristics” 35
TABLE 5-11: “Side-Band Interface” 36
TABLE 5-12: “6 mm × 6 mm VGQFN Package Thermal Properties (4-Layer JEDEC PCB)” 37

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1.0 PIN DIAGRAM

The device is packaged in a 6 mm × 6 mm 80-lead VGQFN.

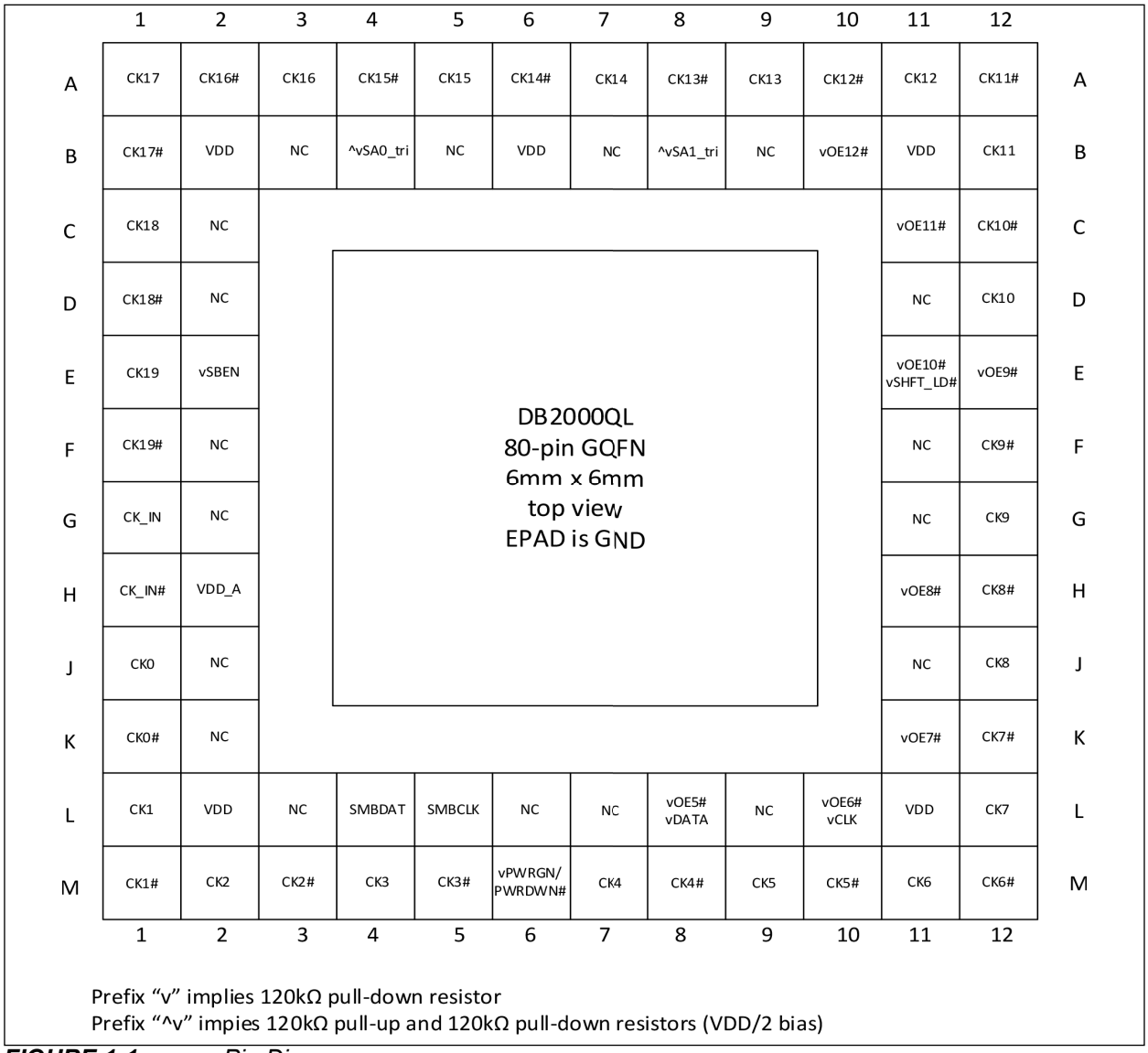

FIGURE 1-1: *Pin Diagram.*

2.0 PIN DESCRIPTIONS

The I/O column in Table 2-1 uses the following symbols:

- I = Input
- I_{PU} = Input with 120 kΩ internal pull-up resistor
- I_{PD} = Input with 120 kΩ internal pull-down resistor
- O = Output
- I/O = Input/Output Drain pin
- NC = No connect pin
- P = Power supply pin
- I_{TRI} = Tri-level input pin biased to VDD/2 by internal 120 kΩ pull-up and 120 kΩ pull-down resistors

TABLE 2-1: PIN DESCRIPTIONS

Pin Number	Pin Name	Input/Output	Description
Input Reference			
G1	CK_IN	I	Input Differential or Single Ended Reference. Input frequency range 0 Hz to 400 MHz.
H1	CK_IN#		
Output Clocks			
J1	CK0	O	Ultra-Low Additive Jitter Differential Outputs 0 to 19. Output frequency range 0 MHz to 400 MHz
K1	CK0#		
L1	CK1		
M1	CK1#		
M2	CK2		
M3	CK2#		
M4	CK3		
M5	CK3#		
M7	CK4		
M8	CK4#		
M9	CK5		
M10	CK5#		
M11	CK6		
M12	CK6#		
L12	CK7		
K12	CK7#		
J12	CK8		
H12	CK8#		
G12	CK9		
F12	CK9#		
D12	CK10		
C12	CK10#		
B12	CK11		
A12	CK11#		
A11	CK12		
AS10	CK12#		
A9	CK13		
A8	CK13#		
A7	CK14		

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TABLE 2-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Pin Name	Input/Output	Description
A6	CK14#	O	Ultra-Low Additive Jitter Differential Outputs 0 to 19 Output frequency range 0 MHz to 400 MHz
A5	CK15		
A4	CK15#		
A3	CK16		
A2	CK16#		
A1	CK17		
B1	CK17#		
C1	CK18		
D1	CK18#		
E1	CK19		
F1	CK19#		
Hardware Control			
K11	vOE7#	I_{PD}	Output Enable. Logic level on these pins enables/disables corresponding output: OE_n# = CKn/n# 0 = Active 1 = Low/Low both pulled low by 42.5Ω
H11	vOE8#		
E12	vOE9#		
C11	vOE11#		
B10	vOE12#		
L8	vOE5#/vDATA	I_{PD}	Output Enable/Data Input for Side Band Interface. When Side-Band interface is disabled (pin SBEN pulled low) this pin is Output Enable and the description is the same as for pin K11 above. When Side-Band interface is enabled (pin SBEN pulled high) this pin is Data Input for Side-Band interface.
L10	vOE6#/vCLK	I_{PD}	Output Enable/Clock Input for Side Band Interface. When Side-Band Interface is disabled (pin SBEN pulled low) this pin is Output Enable and the description is the same as for pin K11 above. When Side-Band interface is enabled (pin SBEN pulled high) this pin is Clock Input for Side-Band interface.
E11	vOE10#/ vSHFT_LD#	I_{PD}	Output Enable/Shift Load for Side Band Interface. When Side-Band interface is disabled (pin SBEN pulled low) this pin is Output Enable and the description is the same as for pin K11 above. When Side-Band interface is enabled (pin SBEN pulled high) this pin is Shift Load Input for Side-Band interface. A falling edge on this pin transfers the sideband shift register content to the output register.
E2	vSBEN	I_{PD}	Side-Band Interface Enable. When this pin is low, the Side-Band interface is disabled and OE pins and OE Register bits (via SMBus) can be used to enable/disable outputs. When this pin is high, the Side-Band interface can be used to enable/disable outputs, and OE pins and OE Register bits (via SMBus) are disabled.
M6	PWRGD/ PWRDN#	I	Power Up/Power Down.
SMBus Control			
L5	SMBCLK	I	SMBus Client Clock Input.
L4	SMBDAT	I/O	Input/Open Drain SMBus Data.

TABLE 2-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Pin Name	Input/Output	Description
B4	^vSA0_tri	I_{TRI}	Tri Level Address Selection Inputs.
B8	^vSA1_tri		
Power and Ground			
B2	VDD	P	Positive Supply Voltage. Connect to 3.3V supply.
B6			
B11			
L2			
L11			
H2	VDD_A	P	Positive Analog Supply Voltage. Connect 3.3V Power Supply.
E-Pad	GND	P	Ground. Connect to ground.
No Connect Pins			
B3	N/C	—	No Connect. These pins are not connected to the die. Leave them open. One of these pins might be used for future modifications of DB2000QL spec. The current DB2000QL v1.0 standard calls for Reserved for Future Upgrades (RFU) pin but does not assign it to any pin number.
B5			
B7			
B9			
C2			
D2			
D11			
F2			
F11			
G2			
G11			
J2			
J11			
K2			
L3			
L6			
L7			
L9			

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3.0 FUNCTIONAL DESCRIPTION

The ZL40294B is an ultra-low additive jitter, low power 1 to 20 fanout buffer which is fully compliant with Intel DB2000QL Standard.

The device operates from 3.3V±5% supply as per Intel spec. Its operation is ensured over the extended industrial temperature range -40°C to +105°C.

3.1 Clock Inputs

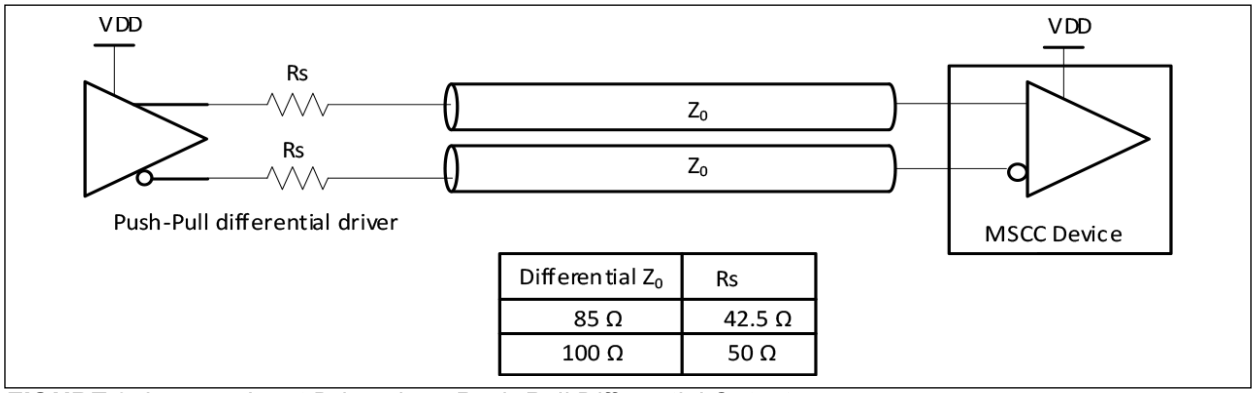
The following blocks diagram shows how to terminate different signals fed to the inputs of ZL40294B device.

The device input can be fed with transmission lines of any impedance. Examples below show only 50Ω single ended, 85Ω differential and 100Ω differential which are the most common ones in practice. Figure 3-1 and Figure 3-2 show how to terminate the input when driven from a push-pull and traditional HCSL drivers respectively.

Figure 3-3 shows how to terminate a single ended output such as LVCMOS. This example assumes 50Ω transmission line which is the most common for single ended CMOS signaling. Ideally, resistors R1 and R2 should be 100Ω each and $R_O + R_S$ should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance.

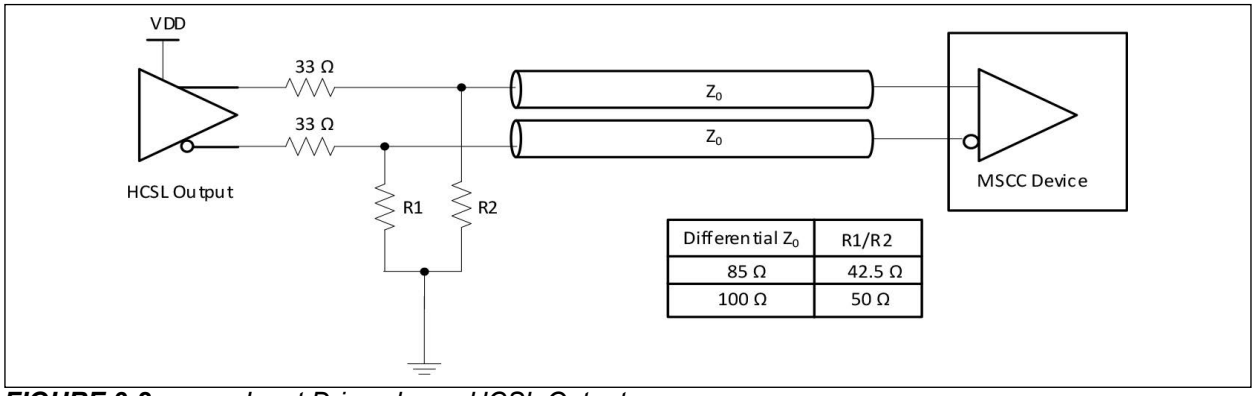
If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor RS should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Figure 3-3). The source resistors of R_S = 270Ω could be used for standard LVCMOS driver. This will provide 516 mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) *(1/(270Ω + 50Ω)) = 5.16 mA.

For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.



Differential Z_0	Rs
85 Ω	42.5 Ω
100 Ω	50 Ω

FIGURE 3-1: *Input Driven by a Push-Pull Differential Output.*



Differential Z_0	R1/R2
85 Ω	42.5 Ω
100 Ω	50 Ω

FIGURE 3-2: *Input Driven by an HCSL Output.*

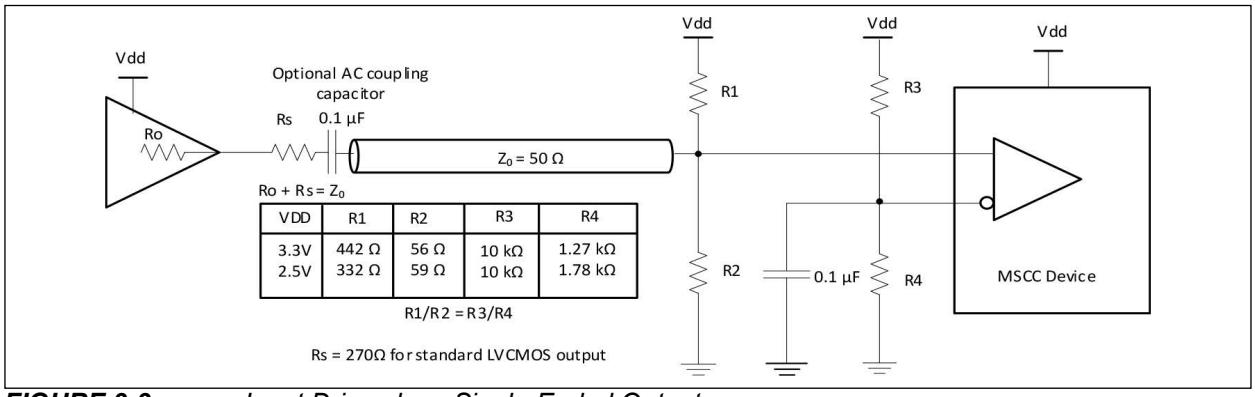


FIGURE 3-3: *Input Driven by a Single-Ended Output.*

3.2 Clock Outputs

Differential outputs have embedded termination resistors as shown in Figure 3-4. This provides significant saving relative to traditional current based HCSL outputs which require four resistors per differential pair (80 resistors for 20 outputs).

Embedded termination resistors in ZL40294B are matched for 85Ω differential transmission line.

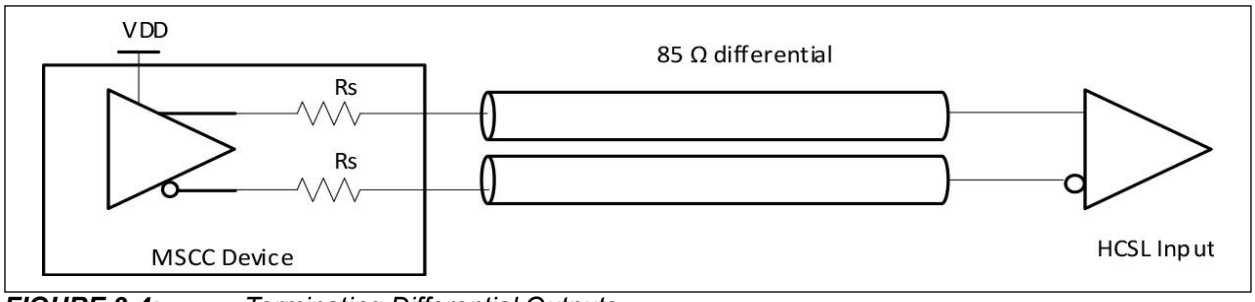


FIGURE 3-4: *Terminating Differential Outputs.*

3.3 Termination of Unused Outputs

Unused outputs should be left unconnected.

3.4 Power Supply Filtering

Each power pin (VDDA and VDD) should be decoupled with 0.1 µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board each power supply could be further insulated with low DC resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Figure 3-5 shows recommended decoupling.

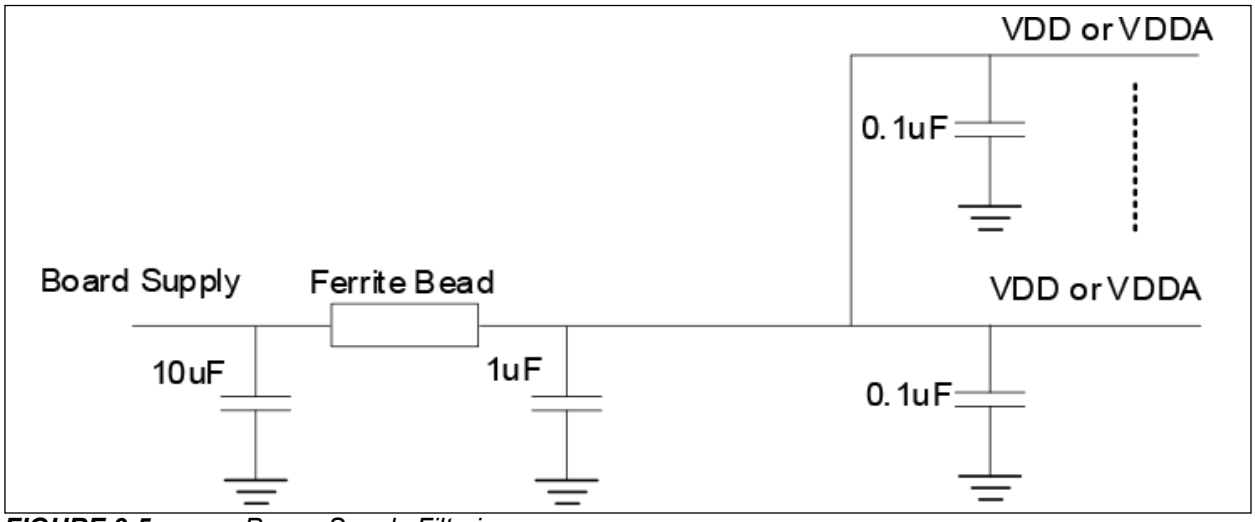


FIGURE 3-5: *Power Supply Filtering.*

3.5 OE# and Output Enables (Control Register)

Each output can be individually enabled or disabled by SMBus control register bits or via OE# pin. The OE# pins are asynchronous asserted-low signals. The Output Enable bits in the SMBus registers are active high and are set to enable by default.

OE# pins are mapped to CK[12:5] outputs.

Note that the logic level for assertion or de-assertion is different in software than it is on hardware. This follows hardware default nomenclature for communication channels (e.g., output is enabled if OE# pin is pulled low) and still maintains software programming logic (e.g., output is enabled if OE register is true).

Refer to Table 3-1 for the truth table for enabling and disabling outputs via hardware and software. Note that both the control register bit must be a ‘1’ AND the OE# pin must be a ‘0’ for the output to be active.

TABLE 3-1: OE FUNCTIONALITY

Inputs		OE# Hardware Pins and Control Register Bits			
PWRGD/ PWRDN#	CK_IN/ CK_IN#	SMBUS Enable Bit	OE# Pin	CK/CK# [12:5]	CK/CK# [4:0] and [19:13]
0	X	X	X	0	0
1	Running	0	X	0	0
		1	0	Running	Running
		1	1	0	Running

3.6 OE# Assertion (Transition from ‘1’ to ‘0’)

All differential outputs that were disabled are to resume normal operation in a glitch free manner. The latency from the assertion to active outputs is 0 - 10 CK clock periods.

3.7 OE# De-Assertion (Transition from ‘0’ to ‘1’)

The impact of de-asserting OE# is each corresponding output will transition from normal operation to disabled in a glitch free manner. A minimum of four valid clocks will be provided after the de-assertion of OE#. The maximum latency from the de-assertion to disabled outputs is 10 CK clock periods.

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3.8 PWRGD/PWRDN#

PWRGD is asserted high and de-asserted low. De-assertion of PWRGD (pulling the signal low) is equivalent to indicating a power-down condition. PWRGD (assertion) is used by the ZL40294B to sample initial configurations such as SA selections.

After PWRGD has been asserted high for the first time, the pin becomes a PWRDN# (Power Down) pin which is used to disable (drive low/low) all clocks cleanly and instruct the device to invoke power savings mode. PWRDN# is a completely asynchronous active low input. When entering power savings mode, PWRDN# should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner. When PWRDN# is de-asserted high, all clocks will start and stop without any abnormal behavior and will meet all AC and DC parameters.

The assertion and de-assertion of PWRDN# is asynchronous.

Disabling of the CK_IN input clock prior to assertion of PWRDN# is an undefined mode and not recommended. Operation in this mode may result in glitches.

TABLE 3-2: PWRGD/PWRDN# FUNCTIONALITY

PWRGD/PWRDN#	CK	CK#
0	Low	Low
1	Normal	Normal

3.9 PWRDN# Assertion

When PWRDN# is sampled low by two consecutive rising edges of CK#, all differential outputs will be disabled on the next CK# high to low transition.

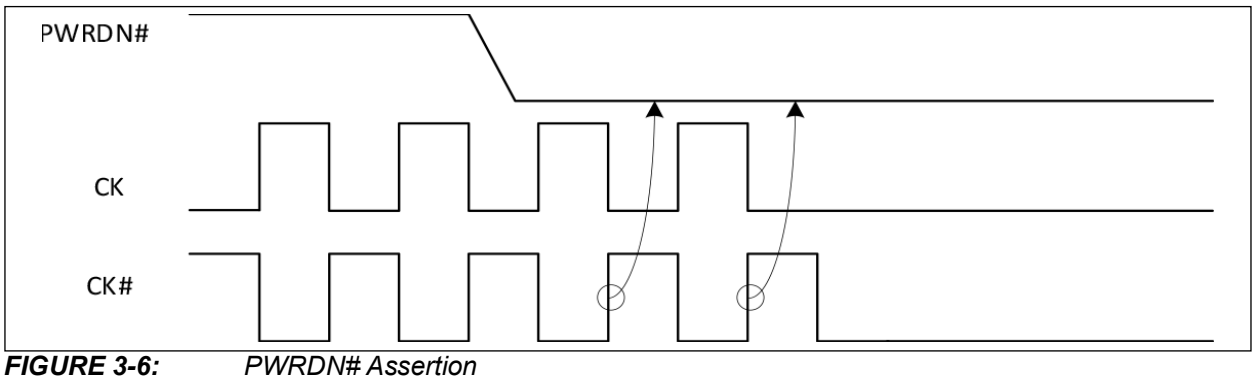

FIGURE 3-6: *PWRDN# Assertion*

3.10 PWRGD Assertion

PWRGD to the clock buffer should not be asserted before V_{DD} reaches $V_{DD(MIN)}$. Prior to $V_{DD(MIN)}$ it is recommended to hold PWRGD low (less than 0.5 V).

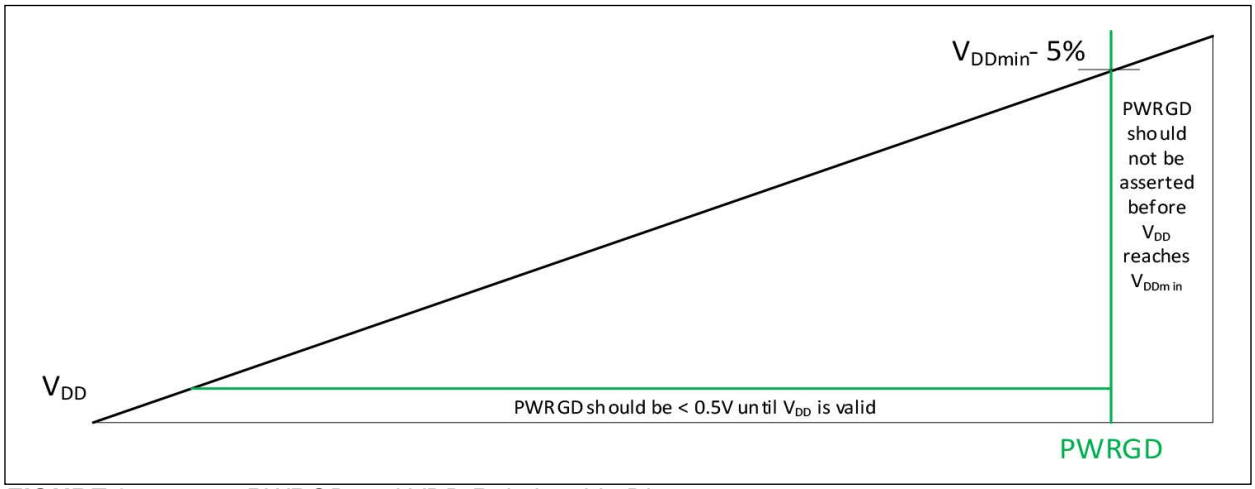

FIGURE 3-7: *PWRGD and VDD Relationship Diagram.*

The power-up latency T_{STABLE} is to be less than 1.8 ms. This is the time from the valid CK_IN input clocks and the assertion of the PWRGD signal to the time that stable clocks are output from the buffer chip. All differential outputs stopped in a disabled condition resulting from power down must be driven high in less than 300 µs of PWRGD assertion to a voltage greater than 200 mV.

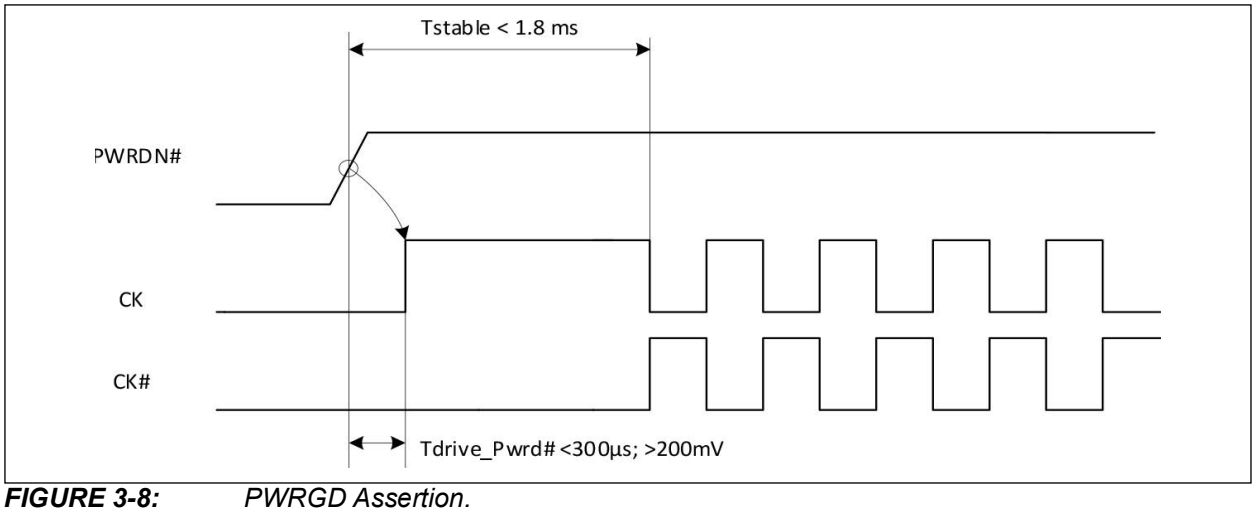

FIGURE 3-8: *PWRGD Assertion.*

3.11 Programming via SMBus

The address selection is done via SA_0 and SA_1 tri-level hardware pins, which select the appropriate address for the device.

The two tri-level input pins that can configure the ZL40294B to nine different addresses (refer to Table 5-2 for VIL_Tri, VIM_Tri, VIH_Tri signal level).

TABLE 3-3: SMBUS ADDRESS TABLE

SA_1	SA_0	SMBus Address
L	L	D8
L	M	DA
L	H	DE
M	L	C2
M	M	C4
M	H	C6
H	L	CA
H	M	CC
H	H	CE

3.12 SMBus Byte Read/Write

Reading or writing a register in a SMBus client device in byte mode always involves specifying the register number.

Read. The standard byte read is as shown in Figure 3-9. It is an extension of the byte write. The write start condition is repeated then the client device starts sending data and the host acknowledges it until the last byte is sent. The host terminates the transfer with a NAK then a stop condition. For byte operation, the 2*7th bit of the command byte must be set. For block operations, the 2*7th bit must be reset. If the bit is not set, the next byte must be the byte transfer count.

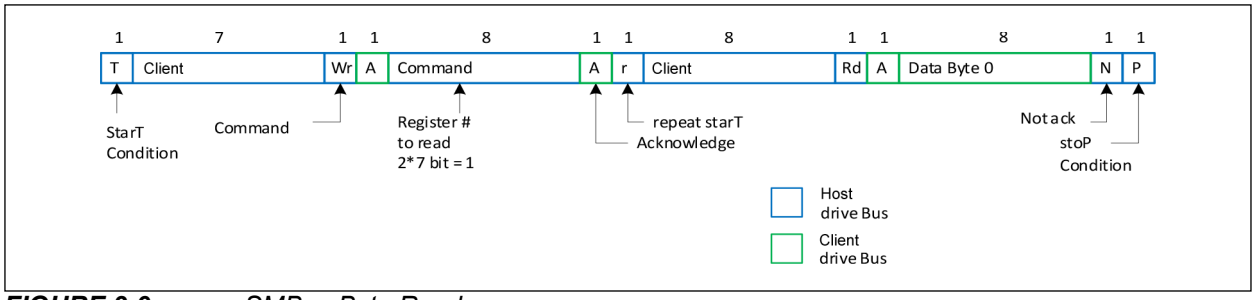

FIGURE 3-9: *SMBus Byte Read.*

Write. Figure 3-10 illustrates a simple typical byte write. For byte operation the 2*7th bit of the command byte must be set. For block operations, the 2*7th bit must be reset. If the bit is not set the next byte must be the byte transfer count. The count can be between 1 and 32. It cannot be zero or exceed 32.

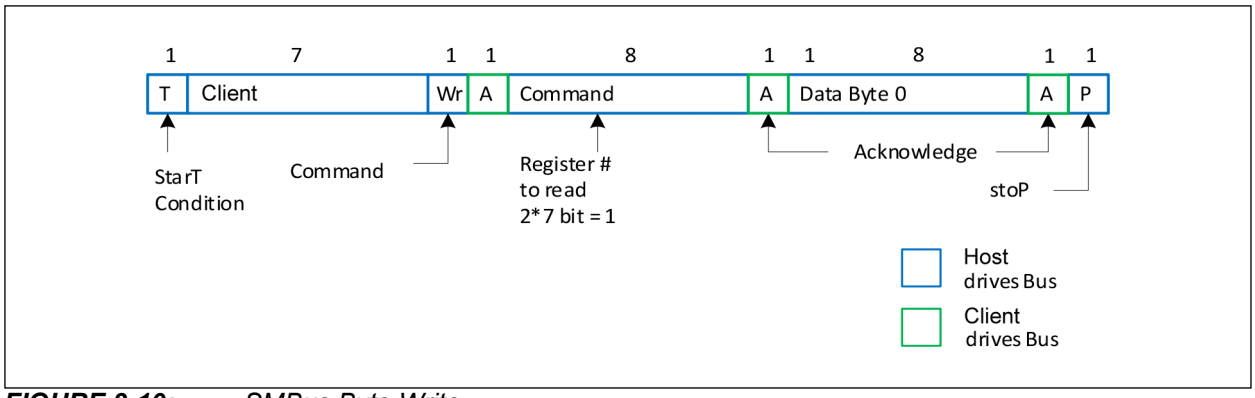

FIGURE 3-10: *SMBus Byte Write.*

3.13 SMBus Block Read/Write

Read. After the client address is sent with the r/w condition bit set, the command byte is sent with the MSB = 0. The client Ack's the register index in the command byte. The host sends a repeat start function. After the client Ack's, this the client sends the number of bytes it wants to transfer (>0 and <33). The host Ack's each byte except the last and sends a stop function.

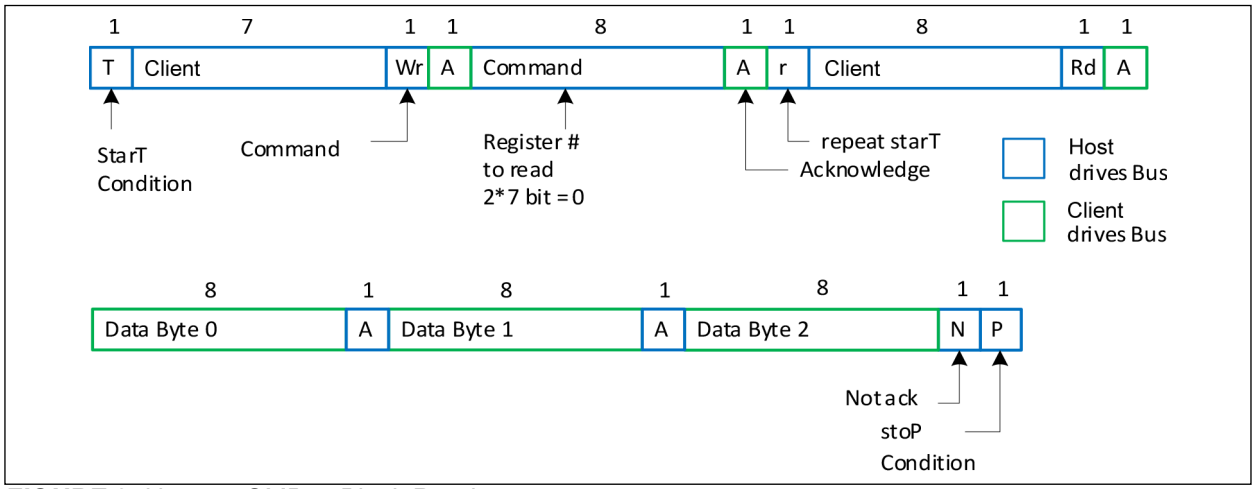

FIGURE 3-11: *SMBus Block Read.*

Write. After the client address is sent with the r/w condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate what register to start the transfer at. If the command byte is 00h, the client device will be compatible with existing block mode client devices. The next byte of a write must be the count of bytes that the host will transfer to the client device. The byte count must be greater than zero and less than 33. Following this byte are the data bytes to be transferred to the client device. The client device always acknowledges each byte received. The transfer is terminated after the client sends the Ack and the host sends a stop function.

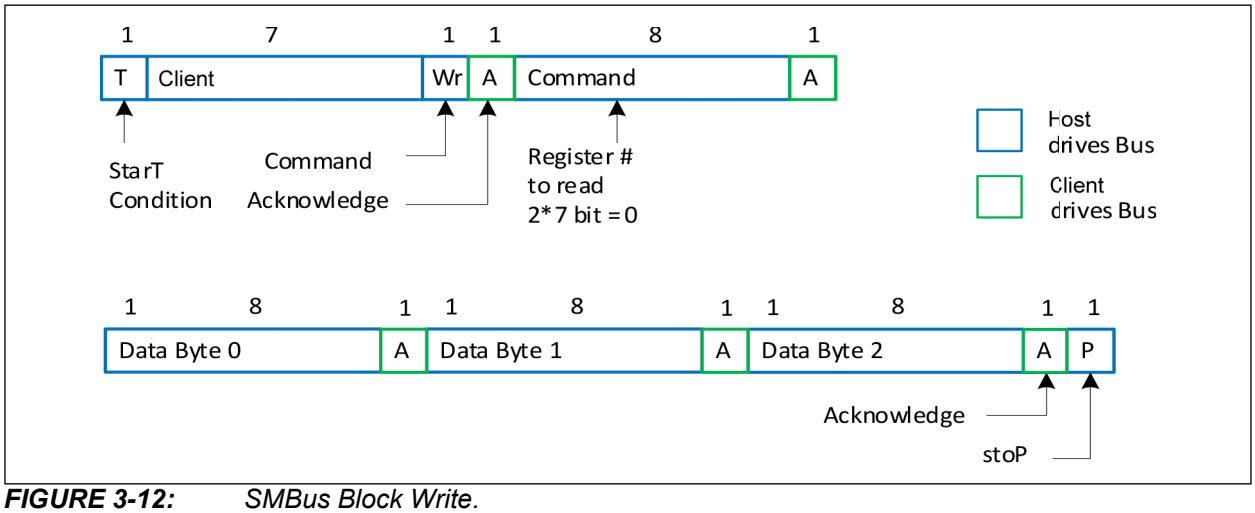

FIGURE 3-12: *SMBus Block Write.*

3.14 Side-Band Interface

Besides OE pins and SMBUS interface, the device outputs can be enabled/disabled via a simple 3-wire serial interface referred to as the Side-Band Interface (SBI).

This interface consists of the vDATA, vCLK and vSHFT_LD# pins. When the vSHFT_LD# pin is high, the rising edge of vCLK can shift vDATA into the shift register. After shifting data, the falling edge of vSHFT_LD# clocks the shift register contents to the Output register.

Both the SBI and the traditional interface feed common output enable/disable synchronization logic ensuring glitch free enable and disable outputs, regardless of the method used.

Both interfaces are not active at the same time, and the SBEN pin selects which interface is active. Tying the SBEN high enables the SBI. Tying the SBEN pin low enables the traditional OE# pin/SMBus output-enable interface.

When the SBI is enabled, OE[7:9, 11,12]# are disabled and vDATA, vCLK and vSHFT_LD# are enabled on vOE5#, vOE6# and vOE10# respectively. Additionally, SMBus registers for masking off the disable function of the shift register (0 value of a bit) become active.

When set to 1, the mask register forces its respective output to ‘enabled.’ This prevents accidentally disabling critical outputs when using the SBI.

A SMBus read-back bit in Byte 4 indicates which output-enable control interface is enabled.

When the SBI is enabled and power has been applied, the SBI is active, even if the PWRGD/PWRDN# pin indicates the part is in powerdown. This allows loading the shift register and transferring the contents to the output register before the assertion of PWRGD.

Note that the mask registers are part of the normal SMBus interface and cannot be accessed when the PWRGD/PWRDN# is low. Figure 3-13 provides a functional description of the SBI.

The SBI and the traditional SMBus output-enable registers both default to the ‘output enabled’ state at power-up. The mask registers default to zero at power-up, allowing the shift register bits to disable their respective output.

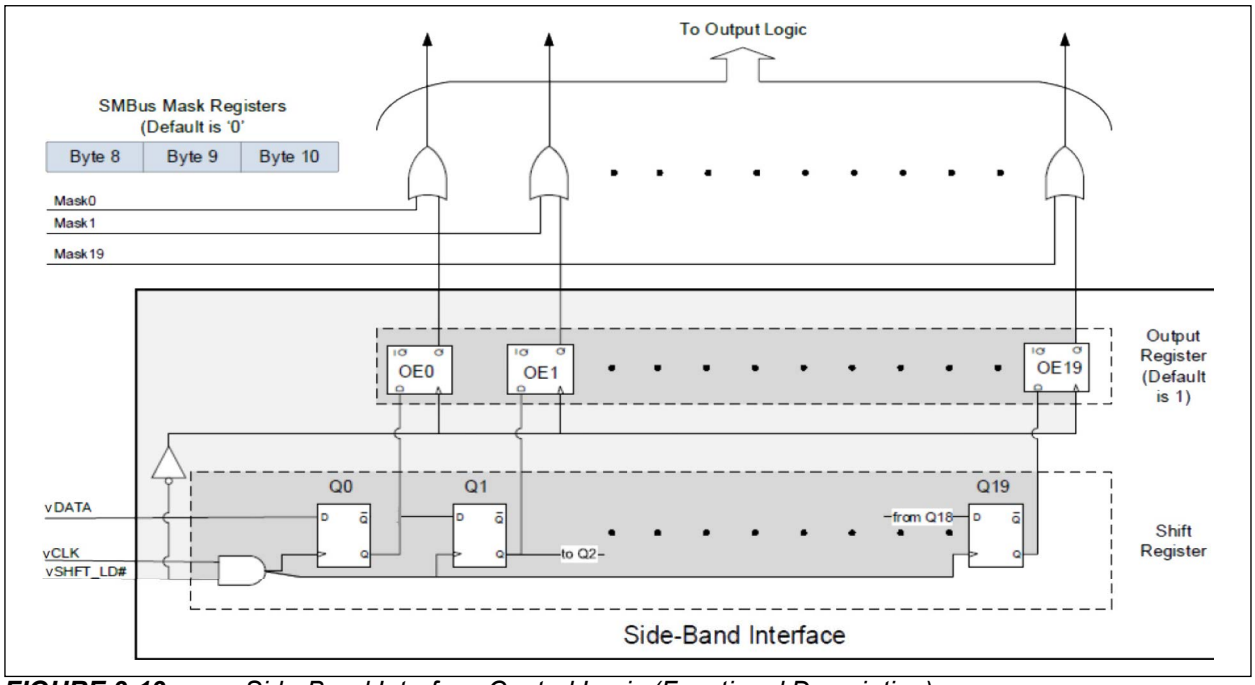

FIGURE 3-13: *Side-Band Interface Control Logic (Functional Description).*

Figure 3-14 shows the basic timing of the side-band interface. The vSHFT_LD# pin goes high to enable the CLK input. Next, the rising edge of CLK clocks enable vDATA into the shift register. After the 20th clock cycle for output 19, it stops the clock low and drive the vSHFT_LD# pin low. The falling edge of vSHFT_LD# clocks the shift register contents to the output register, enabling or disabling the outputs. It always shifts 20 bits of data into the shift register to control the outputs.

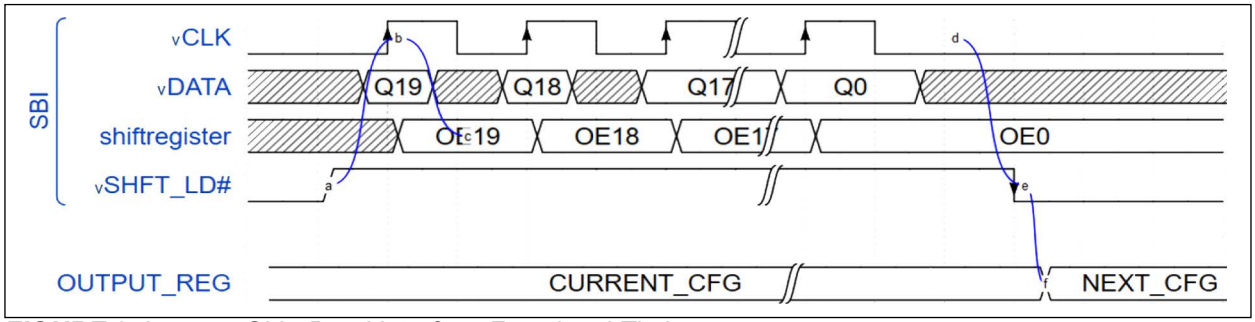

FIGURE 3-14: *Side-Band Interface Functional Timing.*

The SBI supports clock rates up to 10 MHz. Multiple devices may share vCLK and vDATA pins. Dedicating a vSHFT_LD# pin to each device allows its use as a chip-select pin. When the vSHFT_LD# pin is low, the device ignores any activity on the vCLK and vDATA pins.

3.15 Typical Jitter Performance

Following figure shows a typical phase noise for 100 MHz clock frequency. The light blue curve is the phase noise of the input clock fed to the device and the dark blue is the phase noise of the output clock. The plot shows a phase noise floor of –167 dBc/Hz and additive jitter in 12 kHz to 20 MHz of 48 fs.

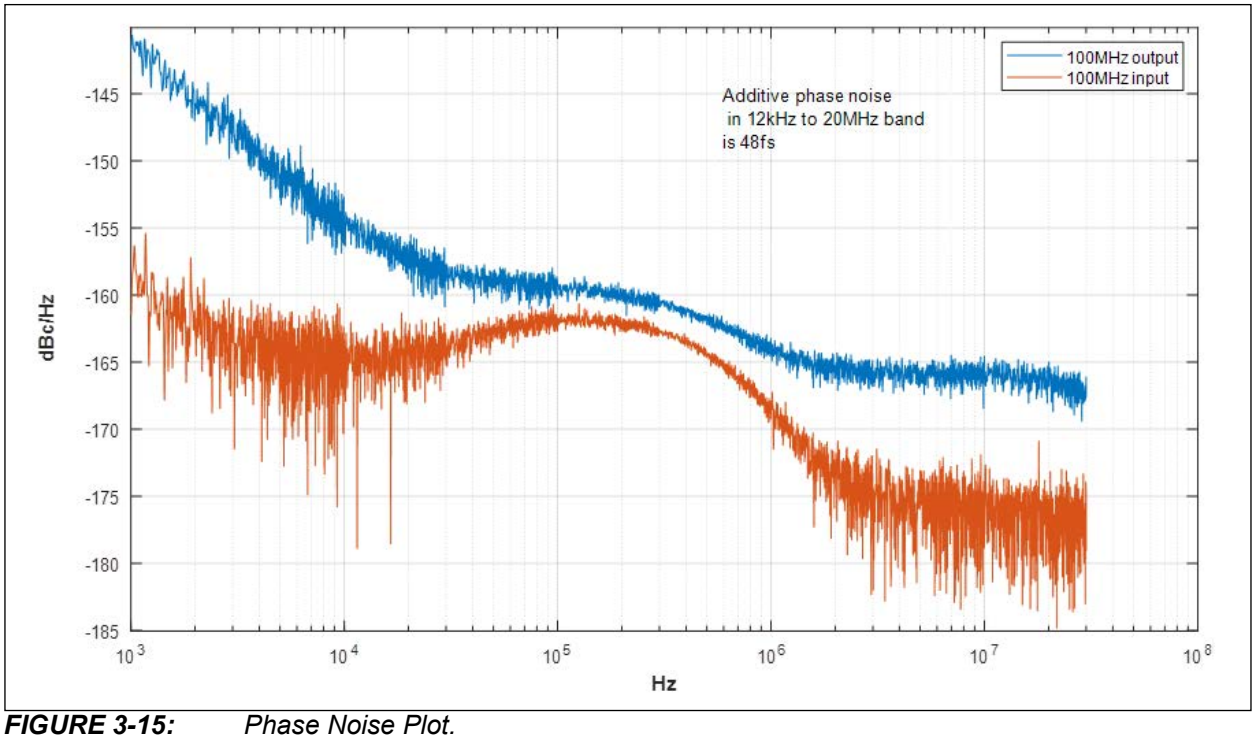

FIGURE 3-15: *Phase Noise Plot.*

The additive jitter is calculated as:

EQUATION 3-1:

$$J_{ADD} = \sqrt{(J^2{}_{OUT} - J^2{}_{IN})}$$

Where J_{OUT} and J_{IN} are respectively output and input jitter in the band of interest.

4.0 REGISTER MAPS

TABLE 4-1: BYTE 0: OUTPUT ENABLE

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Reserved	—	—	—	0	—
1	Reserved	—	—	—	0	—
2	Reserved	—	—	—	0	—
3	Output Enable CK_16	Low	Enabled	RW	1	CK[16]
4	Output Enable CK_17	Low	Enabled	RW	1	CK[17]
5	Output Enable CK_18	Low	Enabled	RW	1	CK[18]
6	Output Enable CK_19	Low	Enabled	RW	1	CK[19]
7	Reserved	—	—	—	0	—

TABLE 4-2: BYTE 1: OUTPUT ENABLE CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable CK_0	Low	Enabled	RW	1	CK[0]
1	Output Enable CK_1	Low	Enabled	RW	1	CK[1]
2	Output Enable CK_2	Low	Enabled	RW	1	CK[2]
3	Output Enable CK_3	Low	Enabled	RW	1	CK[3]
4	Output Enable CK_4	Low	Enabled	RW	1	CK[4]
5	Output Enable CK_5	Low	Enabled	RW	1	CK[5]
6	Output Enable CK_6	Low	Enabled	RW	1	CK[6]
7	Output Enable CK_7	Low	Enabled	RW	1	CK[7]

TABLE 4-3: BYTE 2: OUTPUT ENABLE CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable CK_8	Low	Enabled	RW	1	CK[8]
1	Output Enable CK_9	Low	Enabled	RW	1	CK[9]
2	Output Enable CK_10	Low	Enabled	RW	1	CK[10]
3	Output Enable CK_11	Low	Enabled	RW	1	CK[11]
4	Output Enable CK_12	Low	Enabled	RW	1	CK[12]
5	Output Enable CK_13	Low	Enabled	RW	1	CK[13]
6	Output Enable CK_14	Low	Enabled	RW	1	CK[14]
7	Output Enable CK_15	Low	Enabled	RW	1	CK[15]

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TABLE 4-4: BYTE 3: OE# PIN REALTIME READBACK CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Realtime Readback of OE_5#	OE_5# Low	OE_5# High	R	Realtime	CK[5]
1	Realtime Readback of OE_6#	OE_6# Low	OE_6# High	R	Realtime	CK[6]
2	Realtime Readback of OE_7#	OE_7# Low	OE_7# High	R	Realtime	CK[7]
3	Realtime Readback of OE_8#	OE_8# Low	OE_8# High	R	Realtime	CK[8]
4	Realtime Readback of OE_9#	OE_9# Low	OE_9# High	R	Realtime	CK[9]
5	Realtime Readback of OE_10#	OE_10# Low	OE_10# High	R	Realtime	CK[10]
6	Realtime Readback of OE_11#	OE_11# Low	OE_11# High	R	Realtime	CK[11]
7	Realtime Readback of OE_12#	OE_12# Low	OE_12# High	R	Realtime	CK[12]

TABLE 4-5: BYTE 4: RESERVED CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	RB_SBEN	Pin Low	Pin High	Input	Real time	—
1	Reserved	—	—	—	—	—
2	Reserved	—	—	—	—	—
3	Reserved	—	—	—	—	—
4	Reserved	—	—	—	—	—
5	Reserved	—	—	—	—	—
6	Reserved	—	—	—	—	—
7	Reserved	—	—	—	—	—

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TABLE 4-6: BYTE 6: DEVICE ID CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Device ID 0	—	—	R	0	—
1	Device ID 1	—	—	R	1	—
2	Device ID 2	—	—	R	1	—
3	Device ID 3	—	—	R	1	—
4	Device ID 4	—	—	R	1	—
5	Device ID 5	—	—	R	0	—
6	Device ID 6	—	—	R	1	—
7	Device ID 7 (MSB)	—	—	R	1	—

TABLE 4-7: BYTE 7: BYTE COUNT REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	BC0 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
1	BC1 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
2	BC2 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
3	BC2 - Writing to this register configures how many bytes will be read back	—	—	RW	1	—
4	BC3 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
5	BC4 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
6	Reserved	—	—	RW	0	—
7	Reserved	—	—	RW	0	—

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TABLE 4-8: BYTE 8: SBI MASK (FUNCTIONAL ONLY WHEN SBEN = 1)

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Mask0 - Masks off Side Band Disable	Side Band shift register may disable the output	Forces output to always be enabled regardless of Side Band shift register value	RW	0	CK[0]
1	Mask1 - Masks off Side Band Disable			RW	0	CK[1]
2	Mask2 - Masks off Side Band Disable			RW	0	CK[2]
3	Mask3 - Masks off Side Band Disable			RW	0	CK[3]
4	Mask4 - Masks off Side Band Disable			RW	0	CK[4]
5	Mask5 - Masks off Side Band Disable			RW	0	CK[5]
6	Mask6 - Masks off Side Band Disable			RW	0	CK[6]
7	Mask7 - Masks off Side Band Disable			RW	0	CK[7]

TABLE 4-9: BYTE 9: SBI MASK (FUNCTIONAL ONLY WHEN SBEN = 1)

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Mask8 - Masks off Side Band Disable	Side Band shift register may disable the output	Forces output to always be enabled regardless of Side Band shift register value	RW	0	CK[8]
1	Mask9 - Masks off Side Band Disable			RW	0	CK[9]
2	Mask10 - Masks off Side Band Disable			RW	0	CK[10]
3	Mask11 - Masks off Side Band Disable			RW	0	CK[11]
4	Mask12 - Masks off Side Band Disable			RW	0	CK[12]
5	Mask13 - Masks off Side Band Disable			RW	0	CK[13]
6	Mask14 - Masks off Side Band Disable			RW	0	CK[14]
7	Mask15 - Masks off Side Band Disable			RW	0	CK[15]

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TABLE 4-10: BYTE 10: SBI MASK (FUNCTIONAL ONLY WHEN SBEN = 1)

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Mask16 - Masks off Side Band Disable	Side Band shift register may disable the output	Forces output to always be enabled regardless of Side Band shift register value	RW	0	CK[16]
1	Mask17 - Masks off Side Band Disable			RW	0	CK[17]
2	Mask18 - Masks off Side Band Disable			RW	0	CK[18]
3	Mask19 - Masks off Side Band Disable			RW	0	CK[19]
4	Reserved			RW	0	—
5	Reserved			RW	0	—
6	Reserved			RW	0	—
7	Reserved			RW	0	—

5.0 AC AND DC ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

TABLE 5-1: ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min.	Max.	Units	Notes
3.3V Core Supply Voltage	V_{DD_A}	—	4.6	V	Note 3
3.3V I/O Supply Voltage	V_{DD}	—	4.6	V	Note 3
3.3V Input High Voltage	V_{IH}	—	4.6	V	Note 1, Note 3
3.3V Input Low Voltage	V_{IL}	–0.5	—	V	Note 3
Storage Temperature	T_S	–65	150	°C	Note 3
Input ESD Protection	$V_{DD\text{-}IN}$	2000	—	V	Note 2

* Exceeding these values may cause permanent damage.
* Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated.

Note 1: Maximum V_{IH} is not to exceed maximum V_{DD}.
2: Human body model.
3: Consult manufacturer regarding extended operation in excess of normal DC operating parameters.

5.2 DC Electrical Specification

TABLE 5-2: DC OPERATING CHARACTERISTICS*

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
3.3V Core Supply Voltage	V_{DD_A}	3.135	3.3	3.465	V	—
3.3V I/O Supply Voltage	V_{DD}	3.135	3.3	3.465	V	—
3.3V Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V	—
3.3V Input Low Voltage	V_{IL}	V_{SS} - 0.3	—	0.8	V	—
Input Leakage Current	I_{IL}	–5	—	+5	µA	—
Input Low Voltage, 3-Level CMOS Input	V_{IL3}	V_{SS} - 0.3	—	0.9	V	Note 1
Input Midrange Voltage, 3-Level CMOS Input	V_{IM3}	1.3	—	1.8	V	Note 1
Input High Voltage, 3-Level CMOS Input	V_{IH3}	2.4	—	V_{DD}	V	Note 1
Input Capacitance	C_{IN}	—	—	4.5	pF	Note 2
Output Capacitance	C_{OUT}	—	—	4.5	pF	Note 2
Ambient Temperature	T_A	–40	—	105	°C	—

* Voltages are with respect to ground (GND) unless otherwise stated.

Note 1: Spec assumption based on Intel DB1900Z specification revision 1.5 Table 3-2. VIL3,min changed from 0 to V_{SS} - 0.3 to match DB2000QL VIL,min spec.
2: For parasitic simulation, use IBIS model.

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TABLE 5-3: DIFFERENTIAL DC OUTPUT CHARACTERISTICS*

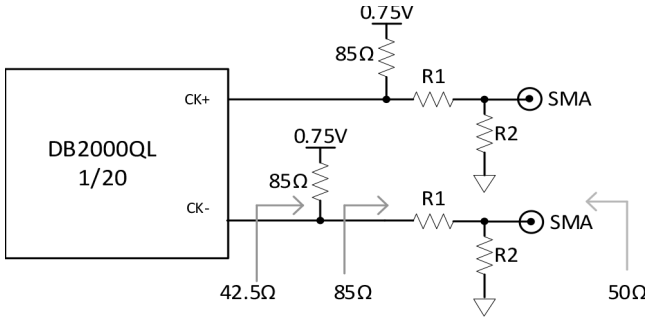
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Maximum Voltage (Over-shoot)	V_{OVS}	—	—	V_{HIGH} + 75	mV	Note 1
Maximum Voltage (Under-shoot)	V_{UDS}	—	—	V_{LOW} – 75	mV	Note 1
Voltage High	V_{HIGH}	225	—	270	mV	Note 1
Voltage Low	V_{LOW}	10	—	150	mV	Note 1
Absolute Crossing Point Voltages	$V_{CROSS_ABSOLUTE}$	130	—	200	mV	Note 1
Relative Crossing Point Voltages	$V_{CROSS_RELATIVE}$	—	—	35	mV	Note 1
Output Buffer Differential Impedance	Z_{DIFF}	85 –5%	—	85 +5%	Ω	Note 2
Output Buffer Differential Impedance	$Z_{DIFF_CROSSING}$	85 –20%	—	85 +20%	Ω	Note 3

* Voltages are with respect to ground (GND) unless otherwise stated.

Note 1: Measured into DC test load, see Figure 5-1.

2: Measured at V_{OL}/V_{OH}.

3: Measured during a transition.



Eq1. R1 + (R2||50Ω) = 85Ω

Eq2. ((42.5Ω || 85Ω) + R1)||R2 = 50Ω

R1 = 47.8Ω, standard 1% value R1 = 47Ω
R2 = 145.8Ω, standard 1% value R2 = 147Ω

FIGURE 5-1: *DC Test Load (as per DB2000QL).*

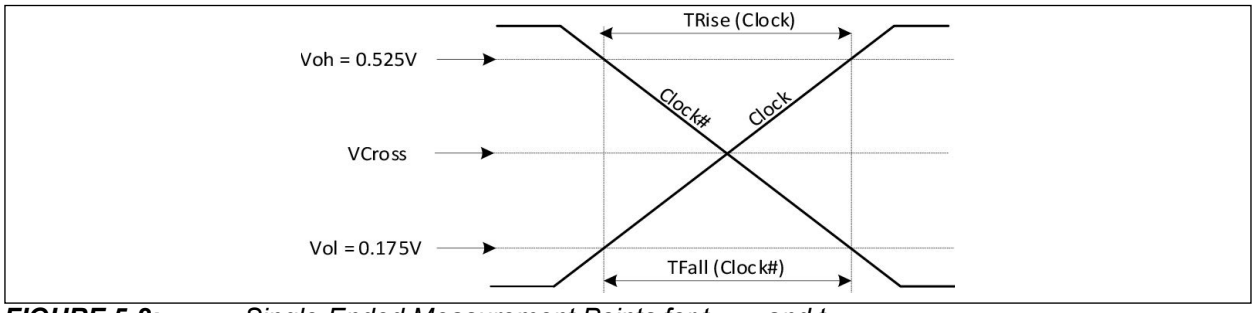


FIGURE 5-2: *Single-Ended Measurement Points for t_{RISE} and t_{FALL}.*

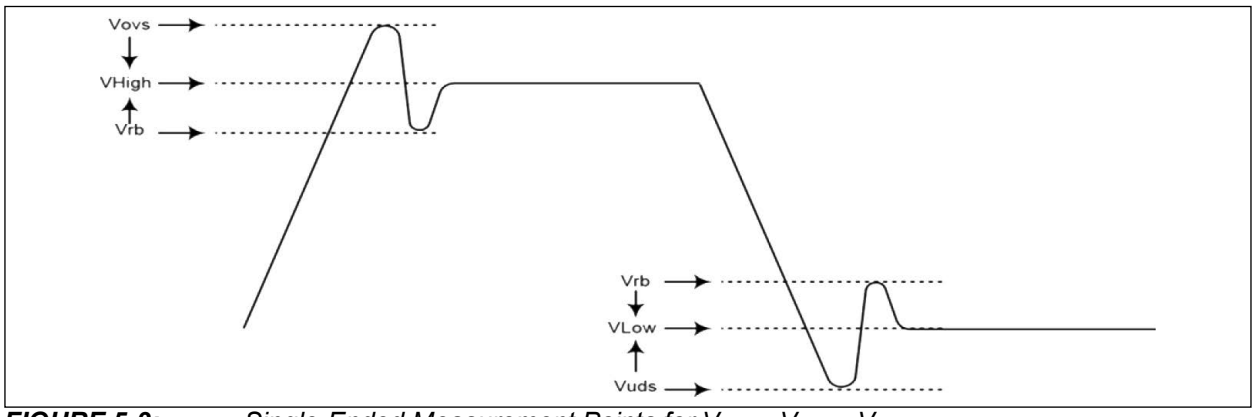


FIGURE 5-3: *Single-Ended Measurement Points for V_{OVS}, V_{UDS}, V_{RB}.*

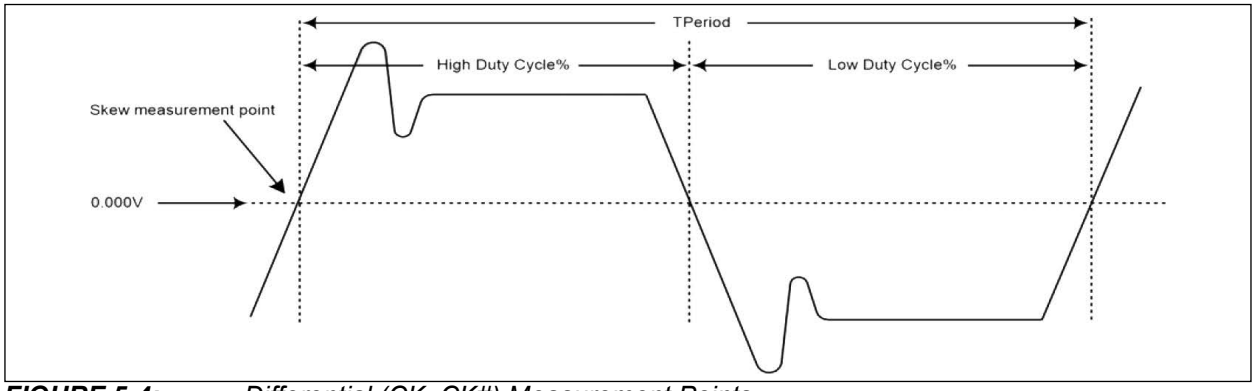


FIGURE 5-4: *Differential (CK, CK#) Measurement Points.*

5.3 AC Electrical Specification

TABLE 5-4: POWER NOISE TOLERANCE*

VDD Electrical Noise Range	Symbol	Min.	Typ.	Max.	Units	Notes
f_{NOISE} = 12 kHz to 20 MHz	N_{VDD_MID}	100	—	—	mV_{PP}	Note 1, Note 2
f_{NOISE} > 20 MHz	N_{VDD_HIGH}	50	—	—	mV_{PP}	Note 1, Note 2
f_{NOISE} = 12 kHZ to 20 MHz	$N_{VDD_A_MID}$	40	—	—	mV_{PP}	Note 1, Note 2
f_{NOISE} > 20 MHz	$N_{VDD_A_HIGH}$	20	—	—	mV_{PP}	Note 1, Note 2

* The device meets all specification in the presence of noise specified in this table.

Note 1: Jitter and electrical characteristics are met with specified AC noise present on any of the power pins.

2: Over the specified frequency range, a single sinusoid tone should be assumed swept as the worst case.

TABLE 5-5: SKEW AND JITTER: NORMAL INPUT CLOCK CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Input-to-Output Delay	I/O_{DELAY}	1.1	1.3	1.5	ns	Note 1, Note 3, Note 5
Input-to-Output Delay Variation as Temperature Changes from –40°C to +85°C	$I/O_{DELAY}\Delta(T)$	0.13	0.14	0.15	ns	Note 1, Note 3, Note 5
Output-to-Output Skew	O/O_{DELAY}	—	—	50	ps	Note 1, Note 2, Note 5
RMS Additive Jitter as per DB2000QL Spec	AJ_{RMS}	—	11.6	13.6	fs_{RMS}	Note 1, Note 2, Note 4, Note 5
Peak-to-Peak Additive Jitter	$p\text{-}pAJ_{RMS}$	—	—	0.8	ps	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 1.0 (1.5 MHz to 22 MHz)	$T_{jPCIe_1.0}$	—	0.52	0.62	ps_{PP}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 2.0 high band (1.5 MHz to 50 MHz)	$T_{jPCIe_2.0_high}$	—	60.9	71.6	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 2.0 low band (10 kHz to 1.5 MHz)	$T_{jPCIe_2.0_low}$	—	16.1	20.4	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 2.0 low band (5 MHz to 16 MHz)	$T_{jPCIe_2.0_mid}$	—	47.1	55.5	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$T_{jPCIe_3.0}$	—	13.8	16.3	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$T_{jPCIe_4.0}$	—	13.8	16.3	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$T_{jPCIe_5.0}$	—	6.6	8.5	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 6.0 (PLL_BW = 0.5 MHz to 1.0 MHz, CDR for 64 GT/s CC)	$T_{jPCIe_6.0}$	—	4.1	5.2	fs_{RMS}	Note 1, Note 2, Note 5

Note 1: Measured into AC test load as per Figure 5-5.

2: Measured from differential crossing point to differential crossing point.

3: Input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

4: Integrated after the measurement filter. See Intel DB2000QL specification Jitter Measurement section for the measurement filter details.

5: Normal input clock conditions: Differential input voltage 1600 mV and input clock slew rate >3.5V/ns.

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TABLE 5-5: SKEW AND JITTER: NORMAL INPUT CLOCK CONDITIONS (CONTINUED)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Additive Jitter as per PCIe 7.0 (PLL_BW = 0.35 MHz to 0.7 MHz, CDR for 128 GT/s CC)	$T_{jPCIe_7.0}$	—	3.5	4.2	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per Intel QPI 9.6 Gbps	T_{jQPI}	—	26	31.5	fs_{RMS}	Note 1, Note 2, Note 5
Additive RMS Jitter in 1 MHz to 20 MHz band	$T_{j_1M_20M}$	—	46.2	54.3	fs_{RMS}	Note 1, Note 2, Note 5 (100 MHz clock)
		—	38.1	46.1	fs_{RMS}	Note 1, Note 2, Note 5 (133 MHz clock)
		—	33.9	39.4	fs_{RMS}	Note 1, Note 2, Note 5 (156.25 MHz clock)
		—	24.1	28.1	fs_{RMS}	Note 1, Note 2, Note 5 (312.50 MHz clock)
Additive RMS Jitter in 12 kHz to 20 MHz band	$T_{j_12k_20M}$	—	48.2	56.7	fs_{RMS}	Note 1, Note 2, Note 5 (100 MHz clock)
		—	39.8	48.2	fs_{RMS}	Note 1, Note 2, Note 5 (133 MHz clock)
		—	32.2	41.4	fs_{RMS}	Note 1, Note 2, Note 5 (156.25 MHz clock)
		—	24.3	30.4	fs_{RMS}	Note 1, Note 2, Note 5 (312.50 MHz clock)
Additive RMS Jitter in 12 kHz to 40 MHz band	$T_{j_12k_40M}$	—	63.7	75.2	fs_{RMS}	Note 1, Note 2, Note 5 (100 MHz clock)
		—	56.6	68.5	fs_{RMS}	Note 1, Note 2, Note 5 (133 MHz clock)
		—	46	56.4	fs_{RMS}	Note 1, Note 2, Note 5 (156.25 MHz clock)
		—	32	38.9	fs_{RMS}	Note 1, Note 2, Note 5 (312.50 MHz clock)

Note 1: Measured into AC test load as per Figure 5-5.

2: Measured from differential crossing point to differential crossing point.

3: Input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

4: Integrated after the measurement filter. See Intel DB2000QL specification Jitter Measurement section for the measurement filter details.

5: Normal input clock conditions: Differential input voltage 1600 mV and input clock slew rate >3.5V/ns.

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TABLE 5-5: SKEW AND JITTER: NORMAL INPUT CLOCK CONDITIONS (CONTINUED)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Noise Floor	N_F	—	–166	–163	dBc/Hz	Note 1, Note 2, Note 5 (100 MHz clock)
		—	–165	–162	dBc/Hz	Note 1, Note 2, Note 5 (133 MHz clock)
		—	–165	–162	dBc/Hz	Note 1, Note 2, Note 5 (156.25 MHz clock)
		—	–163	–160	dBc/Hz	Note 1, Note 2, Note 5 (312.50 MHz clock)

Note 1: Measured into AC test load as per Figure 5-5.

2: Measured from differential crossing point to differential crossing point.

3: Input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

4: Integrated after the measurement filter. See Intel DB2000QL specification Jitter Measurement section for the measurement filter details.

5: Normal input clock conditions: Differential input voltage 1600 mV and input clock slew rate >3.5V/ns.

TABLE 5-6: SKEW AND JITTER: DEGRADED INPUT CLOCK CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Input-to-Output Delay	I/O_{DELAY}	1.1	1.3	1.5	ns	Note 1, Note 3, Note 5
Input-to-Output Delay Variation as Temperature Changes from –40°C to +85°C	$I/O_{DELAY}\Delta(T)$	0.13	0.14	0.15	ns	Note 1, Note 3, Note 5
Output-to-Output Skew	O/O_{DELAY}	—	—	50	ps	Note 1, Note 2, Note 5
RMS Additive Jitter as per DB2000QL Spec	AJ_{RMS}	—	12.6	15	fs_{RMS}	Note 1, Note 2, Note 4, Note 5
Peak-to-Peak Additive Jitter	$p\text{-}pAJ_{RMS}$	—	—	0.9	ps	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 1.0 (1.5 MHz to 22 MHz)	$T_{jPCIe_1.0}$	—	0.57	0.68	ps_{PP}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 2.0 high band (1.5 MHz to 50 MHz)	$T_{jPCIe_2.0_high}$	—	66.4	79	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 2.0 low band (10 kHz to 1.5 MHz)	$T_{jPCIe_2.0_low}$	—	17	21	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 2.0 low band (5 MHz to 16 MHz)	$T_{jPCIe_2.0_mid}$	—	51.5	61.1	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$T_{jPCIe_3.0}$	—	15.1	17.9	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$T_{jPCIe_4.0}$	—	15.1	17.9	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$T_{jPCIe_5.0}$	—	7.2	9.4	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 6.0 (PLL_BW = 0.5 MHz to 1.0 MHz, CDR for 64 GT/s CC)	$T_{jPCIe_6.0}$	—	4.5	5.7	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per PCIe 7.0 (PLL_BW = 0.35 MHz to 0.7 MHz, CDR for 128 GT/s CC)	$T_{jPCIe_7.0}$	—	3.9	4.7	fs_{RMS}	Note 1, Note 2, Note 5
Additive Jitter as per Intel QPI 9.6 Gbps	T_{jQPI}	—	30	36.4	fs_{RMS}	Note 1, Note 2, Note 5

Note 1: Measured into AC test load as per Figure 5-5.

2: Measured from differential crossing point to differential crossing point.

3: Input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

4: Integrated after the measurement filter. See Intel DB2000QL specification Jitter Measurement section for the measurement filter details.

5: Degraded input clock conditions: Differential input voltage 800 mV and input clock slew rate = 1.5V/ns.

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TABLE 5-6: SKEW AND JITTER: DEGRADED INPUT CLOCK CONDITIONS (CONTINUED)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Additive RMS Jitter in 1 MHz to 20 MHz band	$T_{j_1M_20M}$	—	50.3	59.6	fs_{RMS}	Note 1, Note 2, Note 5 (100 MHz clock)
		—	44.2	53.7	fs_{RMS}	Note 1, Note 2, Note 5 (133 MHz clock)
		—	36.5	45	fs_{RMS}	Note 1, Note 2, Note 5 (156.25 MHz clock)
Additive RMS Jitter in 12 kHz to 20 MHz band	$T_{j_12k_20M}$	—	52.4	62	fs_{RMS}	Note 1, Note 2, Note 5 (100 MHz clock)
		—	46	56	fs_{RMS}	Note 1, Note 2, Note 5 (133 MHz clock)
		—	38.4	47.1	fs_{RMS}	Note 1, Note 2, Note 5 (156.25 MHz clock)
Additive RMS Jitter in 12 kHz to 40 MHz band	$T_{j_12k_40M}$	—	69.4	82.8	fs_{RMS}	Note 1, Note 2, Note 5 (100 MHz clock)
		—	65.7	80.3	fs_{RMS}	Note 1, Note 2, Note 5 (133 MHz clock)
		—	52.4	64.4	fs_{RMS}	Note 1, Note 2, Note 5 (156.25 MHz clock)
Noise Floor	N_F	—	–165	–162	dBc/Hz	Note 1, Note 2, Note 5 (100 MHz clock)
		—	–164	–161	dBc/Hz	Note 1, Note 2, Note 5 (133 MHz clock)
		—	–164	–161	dBc/Hz	Note 1, Note 2, Note 5 (156.25 MHz clock)

Note 1: Measured into AC test load as per Figure 5-5.

2: Measured from differential crossing point to differential crossing point.

3: Input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

4: Integrated after the measurement filter. See Intel DB2000QL specification Jitter Measurement section for the measurement filter details.

5: Degraded input clock conditions: Differential input voltage 800 mV and input clock slew rate = 1.5V/ns.

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FIGURE 5-5: *AC Test Load as per DB2000QL Specifications.*

TABLE 5-7: DIFFERENTIAL OUTPUT CLOCK AC CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Clock Stabilization Time from PWRGD	T_{STAB}	—	—	1.8	ms	Note 1
Edge Rate at V_{CROSS}	EDGE_RATE	2	—	20	V/ns	Note 1
Slew Rate at V_{CROSS}	RISE_MATCHING/FALL_-MATCHING	—	—	20%	V	Note 1

Note 1: Measured into Figure 5-5 AC test load.

TABLE 5-8: DIFFERENTIAL INPUT CLOCK AC CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
Edge Rate	Input_Slew_Rate	0.7	—	—	V/ns
Total Variation of V_{CROSS} over All Edges	Total_Δ_Vcross	—	—	140	mV
Input Voltage	Input_Voltage	200	—	—	mv diff

TABLE 5-9: CURRENT CONSUMPTION

Parameter	Parameter Condition	Symbol	Min.	Typ.	Max.	Units	Notes
Active Mode Supply Current	f_{IN} = 100 MHz, All CKx/CKx# outputs enabled	I_{DDPG}	—	205	240	mA	Note 1, Note 2
	f_{IN} = 100 MHz, All CKx/CKx# outputs disabled		—	48	55		Note 1, Note 3
	f_{IN} = 133 MHz, All CKx/CKx# outputs enabled		—	257	308		Note 1, Note 2
	f_{IN} = 133 MHz, All CKx/CKx# outputs disabled		—	49	56		Note 1, Note 3
Power Down Mode Supply Current	f_{IN} = 100 MHz	I_{DDPD}	—	21	25	mA	Note 1, Note 4
	f_{IN} = 133 MHz		—	22	26		Note 1, Note 4

Note 1: VDD = 3.3V +5%.

2: Device operating in active mode (Pin PWRGD/PWRDN# = 1) with all 20 CKx/CKx# outputs enabled (all OE_xN pin = 0, all OCR1, OCR2, OCR3 register OEx bits = 1).

3: Device operating in active mode (Pin PWRGD/PWRDN# = 1) with all 20 CKx/CKx# outputs disabled (all OCR1, OCR2, OCR3 register OEx bits = 0).

4: Device operating in low power mode (Pin PWRGD/PWRDN# = 0).

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TABLE 5-10: SMBUS ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Max.	Notes
Nominal Bus Voltage	$V_{DD(SMB)}$	2.7V	5.5V	Note 1
Input Low Voltage	V_{IL}	—	0.8V	—
Input High Voltage	V_{IH}	2.1V	$V_{DD(SMB)}$	—
Output Low Voltage	V_{OL}	—	0.4V	At $I_{PULLUP(MAX)}$
Input Leakage Current	I_{LEAK}	—	±10 µA	—
Current Sinking at $V_{OL(MAX)}$	I_{PULLUP}	4 mA	—	—
Pin Capacitive Load	C_I	—	10 pF	—
Signal Noise Immunity from 10 MHz to 100 MHz	V_{NOISE}	300 mV_{PP}	—	—
Noise Spike Suppression Time	t_{SPIKE}	0 ns	50 ns	Note 3
SMBus Operating Frequency	f_{SMB}	10 kHz	100 kHz	100 kHz Mode
		10 kHz	400 kHz	400 kHz Mode
Bus Freetime between Stop and Start Condition	t_{BUF}	4.7 µs	—	100 kHz Mode
		1.3 µs	—	400 kHz Mode
Hold Time after (Repeated) Start Condition After this period, the first clock is generated.	$t_{HD:STA}$	4.0 µs	—	100 kHz Mode
		0.6 µs	—	400 kHz Mode
Repeated Start Condition Setup Time	$t_{SU:STA}$	4.7 µs	—	100 kHz Mode
		0.6 µs	—	400 kHz Mode
Stop Condition Setup Time	$t_{SU:STO}$	4.0 µs	—	100 kHz Mode
		0.6 µs	—	400 kHz Mode
Data Hold Time	$t_{HD:DAT}$	300 ns	—	100 kHz Mode
		0 ns	—	400 kHz Mode
Data Setup Time	$t_{SU:DAT}$	250 ns	—	100 kHz Mode
		100 ns	—	400 kHz Mode
Clock Low Period	t_{LOW}	4.7 µs	—	100 kHz Mode
		1.3 µs	—	400 kHz Mode
Clock High Period	t_{HIGH}	4.0 µs	50 µs	100 kHz Mode
		0.6 µs	50 µs	400 kHz Mode
Clock/Data Fall Time	t_f	—	300 ns	Note 2
Clock/Data Rise Time	t_r	—	1000 ns	100 kHz Mode, Note 2
		—	300 ns	400 kHz Mode, Note 2

Note 1: 3V to 5V ±10%.

2: Rise and fall time is defined as follows:
$t_r = (V_{IL(MAX)} - 0.15)$ to $(V_{IH(MIN)} + 0.15)$
$t_f = (V_{IH(MIN)} + 0.15)$ to $(V_{IL(MAX)} - 0.15)$

3: Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

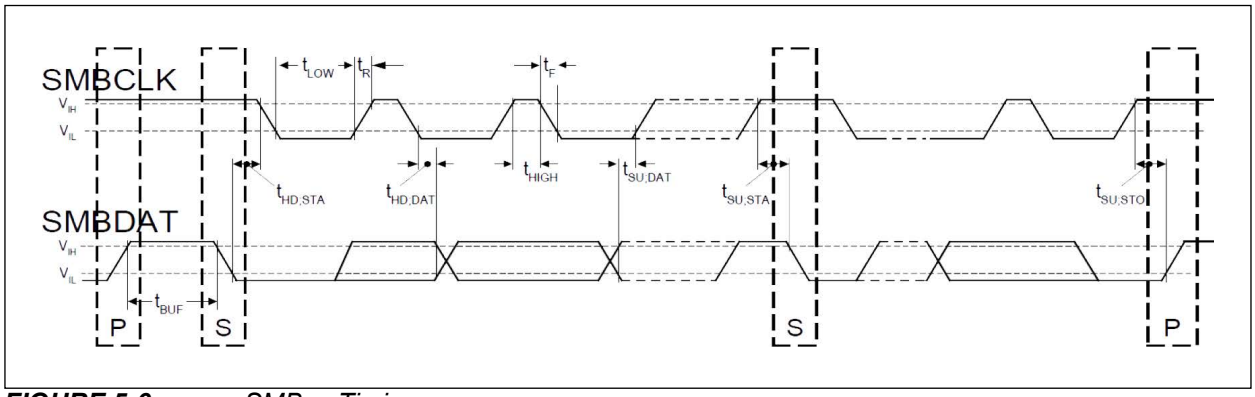

FIGURE 5-6: SMBus Timing.

5.4 Side-Band Interface Characteristics

TABLE 5-11: SIDE-BAND INTERFACE

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Clock Period	t_{PERIOD}	40	—	—	ns	—
vSHFT_LD# setup to vCLK rising edge	t_{SETUP}	15	—	—	ns	—
vDATA setup to vCLK rising edge	t_{DSU}	10	—	—	ns	—
vDATA hold after vCLK rising edge	t_{DSHOLD}	5	—	—	ns	—
Delay from vCLK rising edge to vSHFT_LD# falling edge	t_{DELAY}	15	—	—	ns	—
Delay from vSHFT_LD# falling edge to next output configuration taking effect	t_{PD}	4	—	10	clocks	Note 1
Slew Rate	t_{SLEW}	0.5	—	—	V/ns	—
Note 1: Refers to device differential input clock.						

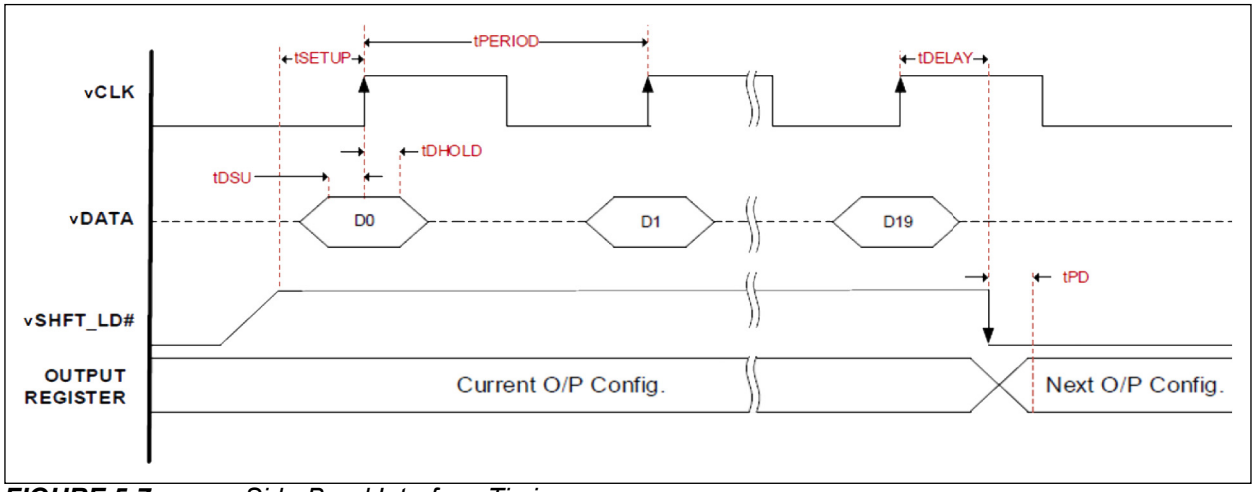

FIGURE 5-7: Side-Band Interface Timing.

TABLE 5-12: 6 MM × 6 MM VGQFN PACKAGE THERMAL PROPERTIES (4-LAYER JEDEC PCB)

Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A	—	105	°C
Maximum Junction Temperature	$T_{J(MAX)}$	—	125	°C
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	Still air	31	°C/W
		1 m/s airflow	26.7	
		2.5 m/s airflow	25.3	
		5 m/s airflow	24.3	
Junction to Board Thermal Resistance	θ_{JB}	—	14.8	°C/W
Junction to Case Thermal Resistance	θ_{JC}	—	30.4	°C/W
Junction to Pad Thermal Resistance (Note 2)	θ_{JP}	Still air	1.8	°C/W
Junction to Top-Center Thermal Characterization Parameter	ψ_{JT}	Still air	0.4	°C/W

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on a 4-layer JEDEC standard test board and dissipating maximum power

2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package)

TABLE 5-13: 6 MM × 6 MM VGQFN PACKAGE THERMAL PROPERTIES (8-LAYER CUSTOM PCB)

Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A	—	105	°C
Maximum Junction Temperature	$T_{J(MAX)}$	—	125	°C
Junction-to-Ambient Thermal Resistance (Note 1)	θ_{JA}	Still air	15.4	°C/W
		1 m/s airflow	12.2	
		2.5 m/s airflow	11.6	
		5 m/s airflow	11.2	
Junction-to-Board Thermal Resistance	θ_{JB}	—	6.0	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	—	29.2	°C/W
Junction-to-Pad Thermal Resistance (Note 2)	θ_{JP}	Still air	1.7	°C/W
Junction-to-Top-Center Thermal Characterization	ψ_{JT}	Still air	0.3	°C/W

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on a 8 layer custom PCB test board and dissipating maximum power

2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package)

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6.0 PACKAGING INFORMATION

6.1 Package Marking Information

80-Lead VGQFN*	Example
XXXXXXXX X X (e3) YYWWNNN	ZL40294B Z Z (e3) 2431DB7

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

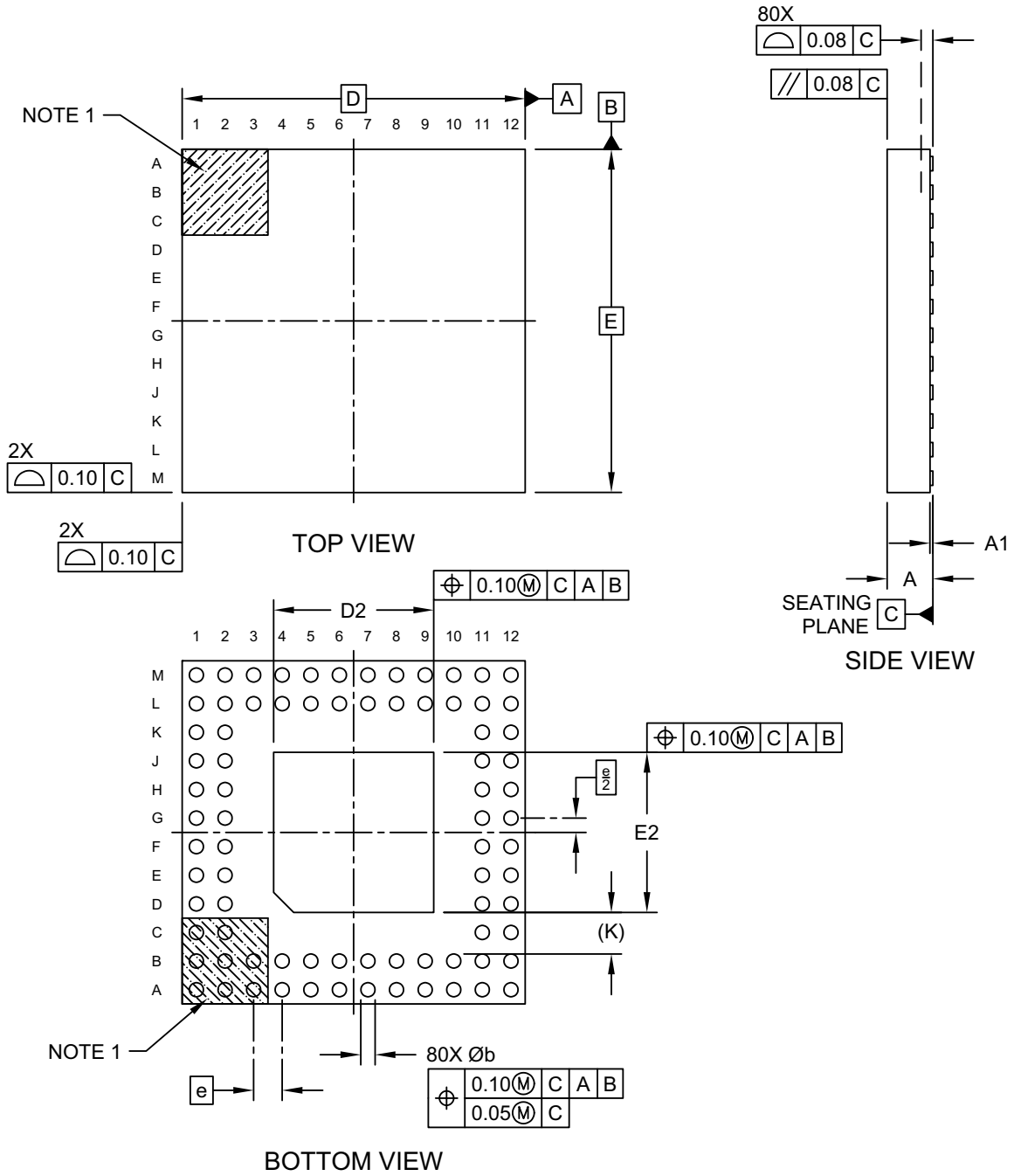
Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space: 6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN; 2 Characters = NN; 1 Character = N

7.0 PACKAGE OUTLINE

80-Lead 6 mm x 6 mm VGQFN Package Outline and Recommended Land Pattern

80-Lead Very, Thin Plastic Grid Array Quad Flat, No Lead (4KW) - 6x6x0.85 mm Body [VGQFN] With 2.8 mm Exposed Pad

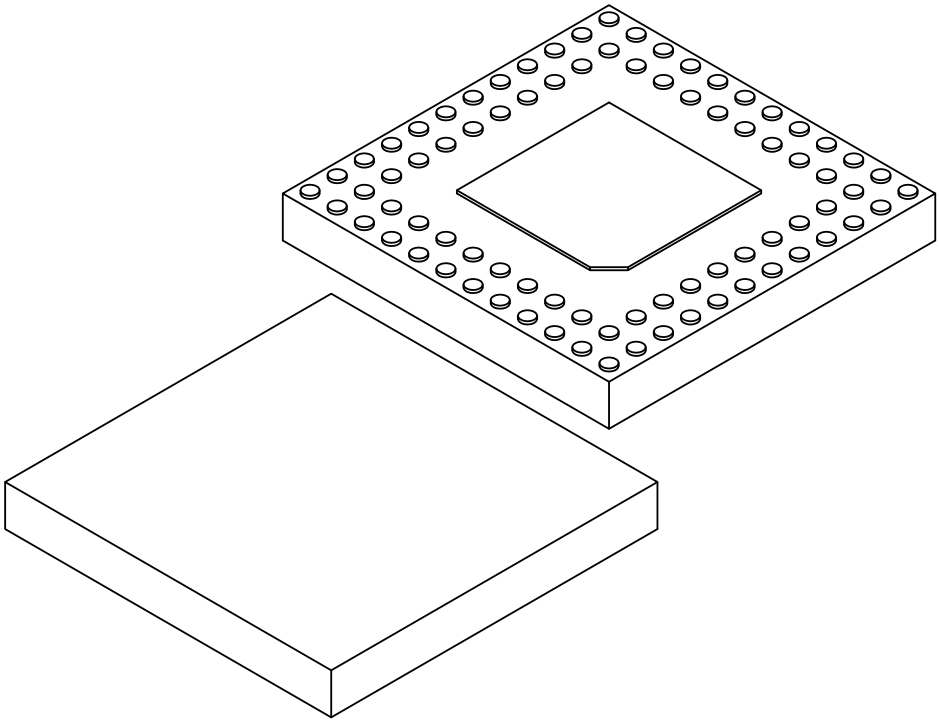
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-590 Rev A Sheet 1 of 2

80-Lead Very, Thin Plastic Grid Array Quad Flat, No Lead (4KW) - 6x6x0.85 mm Body [VGQFN] With 2.8 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	80		
Pitch	e	0.50 BSC		
Overall Height	A	–	–	0.85
Standoff	A1	0.02	0.05	0.08
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	2.70	2.80	2.90
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	2.70	2.80	2.90
Terminal Width	b	0.20	0.25	0.30
Terminal-to-Exposed-Pad	K	0.725 REF		

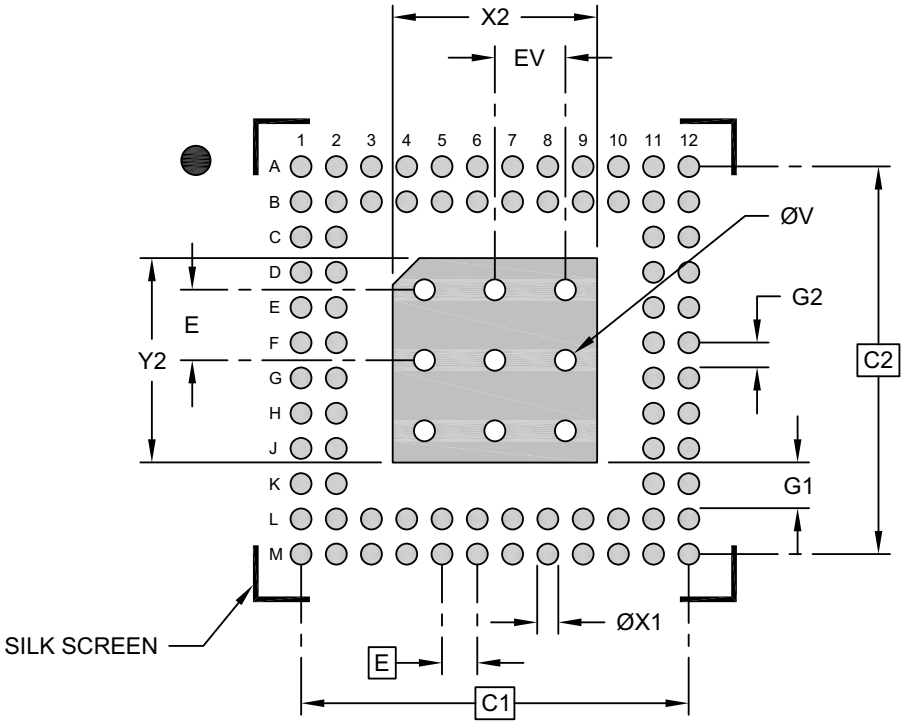
Notes:

1. Terminal A1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-590 Rev A Sheet 2 of 2

80-Lead Very, Thin Plastic Grid Array Quad Flat, No Lead (4KW) - 6x6x0.85 mm Body [VGQFN] With 2.8 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.90
Optional Center Pad Length	Y2			2.90
Contact Pad Spacing	C1		5.50 BSC	
Contact Pad Spacing	C2		5.50 BSC	
Contact Pad Diameter (X80)	X1			0.30
Contact Pad to Center Pad (X32)	G1	0.65		
Contact Pad to Contact Pad	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2590 Rev A

8.0 ACRONYMS AND ABBREVIATIONS

APLL	analog phase locked loop
CML	current mode logic
GbE	gigabit Ethernet
HCSL	high-speed current steering logic
HSTL	high-speed transceiver logic
I/O	input/output
LOS	loss of signal
LVDS	low-voltage differential signal
LVPECL	low-voltage positive emitter-coupled logic
PFD	phase/frequency detector
PLL	phase locked loop
ppb	parts per billion
ppm	parts per million
pk-pk	peak-to-peak
RMS	root-mean-square
RO	read-only
R/W	read/write
SS or SSM	spread spectrum modulation
TCXO	temperature-compensated crystal oscillator
UI	unit interval
UI_{PP} or UI_{P-P}	unit interval, peak to peak
XO	crystal oscillator

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006962A (02-12-25)	—	Initial release of ZL40294B data sheet as Microchip DS20006962A.
DS20006962B (09-26-25)	Features	Added PCIe Gen 7.0 information.
	Applications	Added PCIe Gen 7.0 information.
	Table 5-5	Added values for PCIe Gen 7.0 performance.
	Table 5-6	Added values for PCIe Gen 7.0 performance.
DS20006962C (03-16-26)	20-Output DB2000QL PCIe Buffer with Ultra-Low Additive Jitter	Added “PCIe” to the document title.
	Features	Changed maximum clock frequencies value to 400 (eighth bullet point). Added extended temperature range bullet point to the end of this section.
	Table 2-1	Changed each mention of the maximum output frequency range value to 400 for all pins.
	Section 3.0	Added “extended” before “industrial temperature” and corrected maximum value listed to “105.”
	Table 5-2	Fixed typo (misspelling of “Current”) and corrected Ambient Temperature Max. value to 105.
	Table 5-5	Added additional 312.50 MHz values for Additive RMS Jitter bands and noise floor.
	Table 5-12	Added “4-Layer JEDEC PCB” to table title. Added Junction-to-Ambient Thermal Resistance row/value for 5 m/s airflow.
	Table 5-13	Created new table for 6 mm × 6 mm VGQFN Package Thermal Properties (8-Layer Custom PCB).
DS20006962D (04-23-26)	Table 5-12, Table 5-13	Updated thermal values in both tables.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Device	X	X	X	X
Part Number	Chip Carrier Type	Package	Media Type	Finish

Device:	ZL40294B: 20-Output DB2000QL PCIe Buffer with Ultra-Low Additive Jitter
Chip Carrier Type:	L = Leadless Chip Carrier
Package:	D = 80-Lead 6 mm × 6 mm VGQFN
Media Type:	G = 490/Tray F = 4000/Reel (12 mm pocket pitch) X = 4000/Reel (8 mm pocket pitch)
Finish:	6 = Pb-Free

Examples:

a) ZL40294BLDG6:

20-Output DB2000QL PCIe Buffer with Ultra-Low Additive Jitter, Leadless Chip Carrier, 80-Lead VGQFN, 490/Tray, Pb-Free

b) ZL40294BLDF6:

20-Output DB2000QL PCIe Buffer with Ultra-Low Additive Jitter, Leadless Chip Carrier, 80-Lead VGQFN, 4000/Reel, 12 mm pocket pitch, Pb-Free

c) ZL40294BLDX6:

20-Output DB2000QL PCIe Buffer with Ultra-Low Additive Jitter, Leadless Chip Carrier, 80-Lead VGQFN, 4000/Reel, 8 mm pocket pitch, Pb-Free

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.