

Product Overview

The Microchip Powermite surface mount 3.0 watt Zener package series provides power handling capabilities found in larger packages. In addition to its size advantages, the Powermite package features include a full-metallic bottom that eliminates the possibility of solder flux entrapment during assembly, and a unique locking tab design serves as an integral heat sink with very low thermal resistance junction to case (bottom). Its innovative design makes this device ideal for use with automatic insertion equipment. RoHS compliant versions are also available.

Features

- Surface mount equivalent to JEDEC registered 1N5925 through 1N5956 series except with additional power capability
- Extensive selection from 10 to 200V Zener voltage
- Regulates voltage over a broad operating current and temperature range
- Low reverse leakage current
- RoHS compliant versions are available
- Ideal for high-density and low-profile mounting

Applications/Benefits

- Available in Zener voltage tolerance of C suffix 2% and B suffix 5%
- Moisture classification Level 1 with no dry pack required per IPC/JEDEC J-STD-020F
- Non-sensitive to ESD per MIL-STD-750 method 1020
- Compatible with automatic insertion equipment
- Full metallic bottom eliminates flux entrapment

Figure 1. DO-216 Package

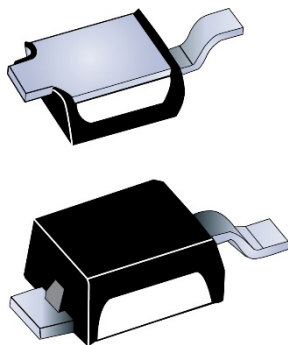


Table of Contents

Product Overview.....	1
Features.....	1
Applications/Benefits.....	1
1. Maximum Ratings.....	3
1.1. Mechanical and Packaging.....	3
2. Part Nomenclature.....	4
2.1. Symbols and Definitions.....	4
2.2. Electrical Characteristics at 25 °C Unless Otherwise Stated.....	5
3. Graphs.....	7
4. Package Dimensions.....	8
5. PAD Layout.....	9
6. Revision History.....	10
Microchip Information.....	11
Trademarks.....	11
Legal Notice.....	11
Microchip Devices Code Protection Feature.....	11

1. Maximum Ratings

Parameters/Test Conditions	Symbol	Value	Unit
Junction and Storage Temperature	T_J and T_{STG}	-55 to +150	°C
Thermal Resistance Junction-to-Ambient ⁽¹⁾	$R_{\theta JA}$	240	°C/W
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	30	°C/W
Steady-State Power Dissipation ⁽²⁾	P_D	3.0	W
Solder Temperature at 10 s	T_{SP}	260	°C

Notes:

- On FR4 PC board (1 oz copper) with recommended footprint (see [5. PAD Layout](#)).
- At $T_C < 120$ °C where T_C is case bottom temperature at mounting plane, or 0.5 watts at $T_A = 30$ °C (ambient temperature) when mounted on FR4 PC board as described for $R_{\theta JA}$ (see [Figure 3-1](#)).

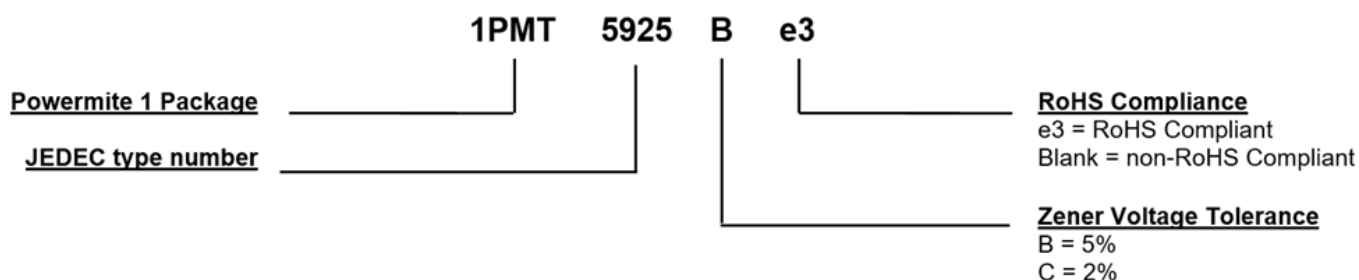
1.1. Mechanical and Packaging

- Case: Void-free transfer molded thermosetting epoxy compound meeting UL94V-0.
- Finish: Annealed matte-tin plating over copper and readily solderable per MIL-STD-750 method 2026 (consult factory for tin-lead plating).
Note: Tin-lead plated product is not RoHS compliant.
- Polarity: Cathode designated by Tab 1 (bottom).
- Tape and reel option: Standard per EIA-481-B (consult factory for quantities).
- Marking: Part number as 3 numerical digits (see [Electrical Characteristics](#)), V_Z tolerance level, a dot • if e3 RoHS compliant, date code of package seal YYWW
- Weight: Approximately 0.016 grams.

Note: See [4. Package Dimensions](#).

2. Part Nomenclature

Figure 2-1. Part Nomenclature



Note: See [Electrical Characteristics](#).

2.1. Symbols and Definitions

Symbol	Definition
I_R	Reverse Current: The maximum reverse (leakage) current that will flow at the specified voltage and temperature.
I_Z, I_{ZT}, I_{ZK}	Regulator Current: The dc regulator current (I_Z), at a specified test point (I_{ZT}), near the breakdown knee (I_{ZK})
I_{ZM}	Maximum Regulator (Zener) Current: The maximum rated dc current for the specified power rating.
I_{ZSM}	Maximum Zener Surge Current: The peak reverse current in the breakdown region including all nonrepetitive transient currents but excluding all repetitive transients.
N_D	Noise Density: The noise generated over a specified frequency bandwidth usually specified in terms of mV/√Hz
P_D	Steady-State Power Dissipation: The dc power resulting from the product of $V_Z \times I_{ZM}$
V_R	Reverse Voltage: The reverse voltage dc value, no alternating component.
V_Z	Zener Voltage: The Zener voltage the device will exhibit at a specified current (I_Z) in its breakdown region.
Z_{ZT} or Z_{ZK}	Dynamic Impedance: The small signal impedance of the diode when biased to operate in its breakdown region at a specified rms current modulation (typically 10% of I_{ZT} or I_{ZK}) and superimposed on I_{ZT} or I_{ZK} respectively.

2.2. Electrical Characteristics at 25 °C Unless Otherwise Stated

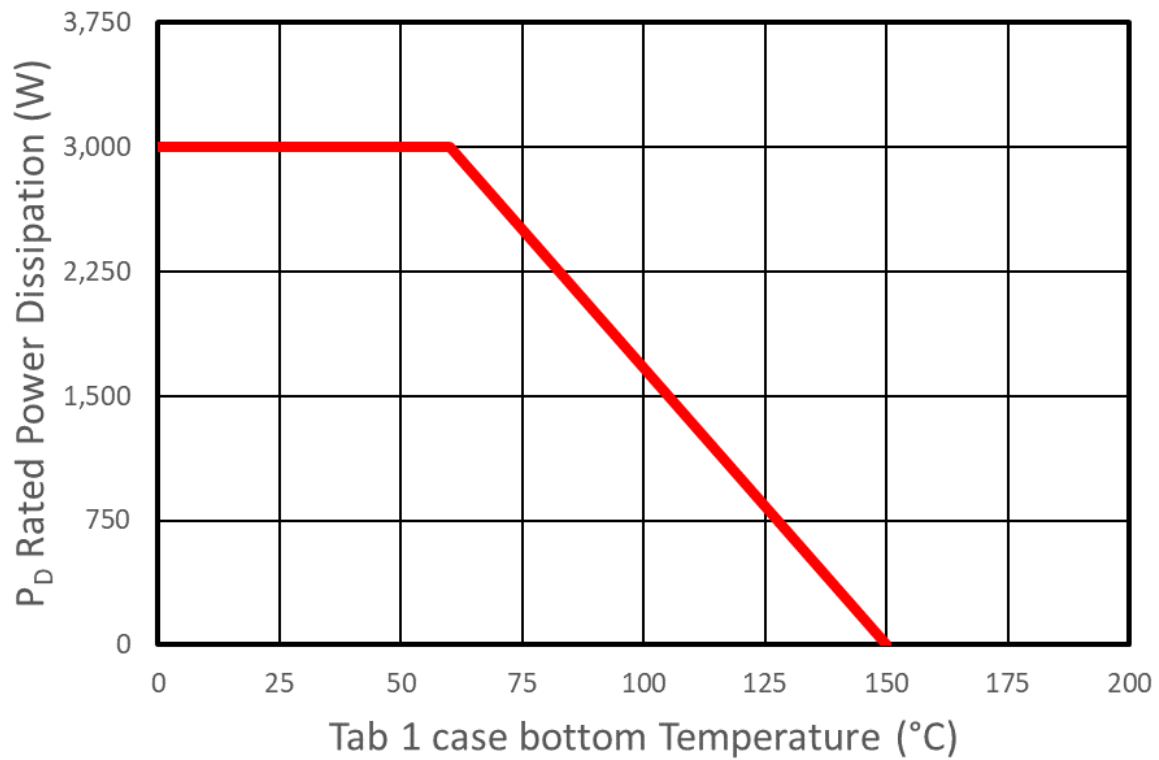
Part Number	Device Marking (1)	Nominal Zener Voltage (2)	Zener Test Current I _{ZT}	Maximum Zener Impedance ⁽³⁾ Z _{ZT} at I _{ZT}	Maximum Knee Impedance		Maximum Reverse Current I _R at V _R		Maximu Zener Current (4)
		V _Z at I _{ZT}							I _{ZM}
		Volts	mA	Ohms	mA	Ohms	μA	Volts	mA
1PMT5925B	925	10	37.5	4.5	0.25	500	5	8	247.5
1PMT5926B	926	11	34.1	5.5	0.25	550	1	8.4	224.4
1PMT5927B	927	12	31.2	6.5	0.25	550	1	9.1	206.2
1PMT5928B	928	13	28.8	7	0.25	550	1	9.9	189.8
1PMT5929B	929	15	25	9	0.25	600	1	11.4	165
1PMT5930B	930	16	23.4	10	0.25	600	1	12.2	153.5
1PMT5931B	931	18	20.8	12	0.25	650	1	13.7	68.5
1PMT5932B	932	20	18.7	14	0.25	650	1	15.2	123.8
1PMT5933B	933	22	17	17.5	0.25	650	1	16.7	112.2
1PMT5934B	934	24	15.6	19	0.25	700	1	18.2	102.3
1PMT5935B	935	27	13.9	23	0.25	700	1	20.6	90.8
1PMT5936B	936	30	12.5	28	0.25	750	1	22.8	82.5
1PMT5937B	937	33	11.4	33	0.25	800	1	25.1	74.3
1PMT5938B	938	36	10.4	38	0.25	850	1	27.4	67.7
1PMT5939B	939	39	9.6	45	0.25	900	1	29.7	62.7
1PMT5940B	940	43	8.7	53	0.25	950	1	32.7	56.1
1PMT5941B	941	47	8	67	0.25	1000	1	35.8	51.2
1PMT5942B	942	51	7.3	70	0.25	1100	1	38.8	47.9
1PMT5943B	943	56	6.7	86	0.25	1300	1	42.6	42.9
1PMT5944B	944	62	6	100	0.25	1500	1	47.1	38.6
1PMT5945B	945	68	5.5	120	0.25	1700	1	51.2	36.3
1PMT5946B	946	75	5	140	0.25	2000	1	56	33
1PMT5947B	947	82	4.6	160	0.25	2500	1	62.2	29.7
1PMT5948B	948	91	4.1	200	0.25	3000	1	69.2	26.4
1PMT5949B	949	100	3.7	250	0.25	3100	1	76	24.8
1PMT5950B	950	110	3.4	300	0.25	4000	1	83.6	21.5
1PMT5951B	951	120	3.1	380	0.25	4500	1	91.2	19.8
1PMT5952B	952	130	2.9	450	0.25	5000	1	98.8	18.1
1PMT5953B	953	150	2.5	600	0.25	6000	1	114	16.5
1PMT5954B	954	160	2.3	700	0.25	6500	1	121.6	14.9
1PMT5955B	955	180	2.1	900	0.25	7000	1	136.8	13.2
1PMT5956B	956	200	1.9	1200	0.25	8000	1	152	11.6

Notes:

1. Part numbers and marking shown have a standard tolerance of $\pm 5\%$ on the nominal Zener voltage. For $\pm 2\%$ tolerance parts C suffix in device part number and marking (for example 1PMT5925Ce3 and 925C•). Include • in marking for e3 parts.
2. V_Z is measured at I_{ZT} with T_C (TAB 1) at 30 °C. Voltage measurement to be performed 20 seconds after application of dc current.
3. Zener impedance is derived by superimposing on I_{ZT} a 60 Hz rms ac current equal to 10% of I_{ZT} (25 μ A ac).
4. Based on 3 W maximum power dissipation before any derating. Allowance has been made for higher voltage with operation at higher currents and temperature. For determination of voltage change with current deviations from I_{ZT} .
5. Forward voltage (V_F) is 1.2 volts maximum at 200 mA peak for 8.3 ms half-sine wave.

3. Graphs

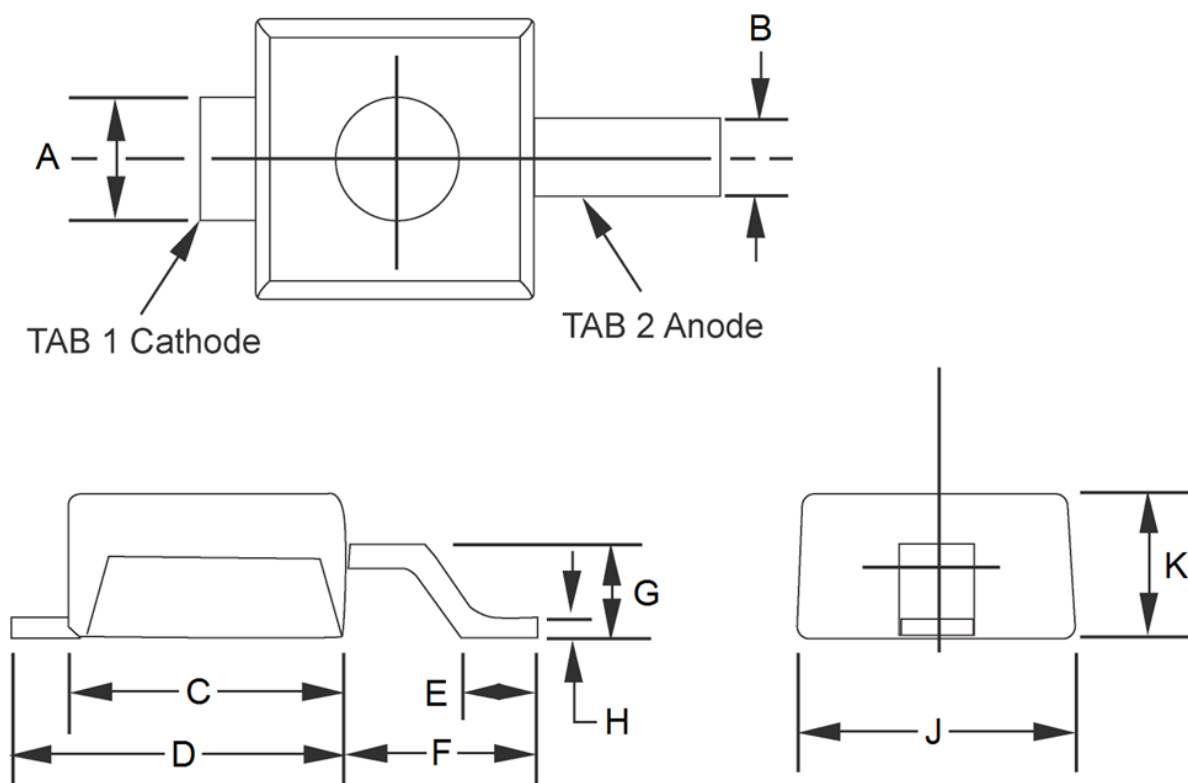
Figure 3-1. Power Derating Curve



Where T_C is case (bottom) temperature and T_A is ambient temperature on the FR4 PC board.

4. Package Dimensions

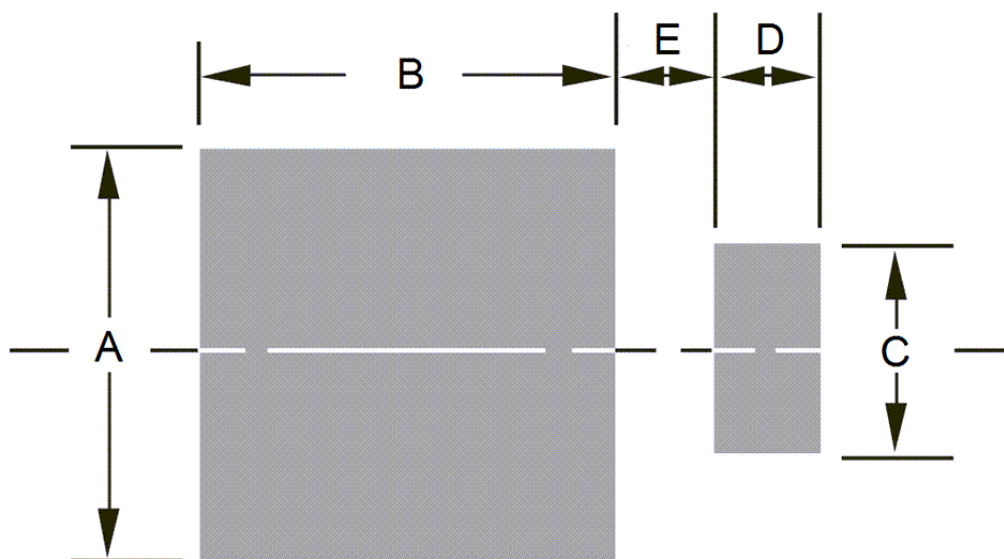
Figure 4-1. Package Dimensions



Ltr	Dimensions			
	Inch		Millimeters	
	Min	Max	Min	Max
A	0.029	0.039	0.73	0.99
B	0.016	0.026	0.40	0.66
C	0.070	0.080	1.77	2.03
D	0.087	0.097	2.21	2.46
E	0.020	0.030	0.50	0.76
F	0.051	0.061	1.29	1.54
G	0.021	0.031	0.53	0.78
H	0.004	0.008	0.10	0.20
J	0.070	0.080	1.77	2.03
K	0.035	0.045	0.89	1.14

5. PAD Layout

Figure 5-1. PAD Layout



Ltr	Dimensions	
	Inch	Millimeters
A	0.100	2.54
B	0.105	2.67
C	0.050	1.27
D	0.030	0.76
E	0.025	0.64

6. Revision History

Revision Level	Date	Description
A	4/2025	Initial version created in the Microchip template. Legacy document number is RF01311.

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