

High-Input Voltage, Adjustable 3-Terminal Linear Regulator

Features

- 13.2V to 100V Input Voltage Range
- Stable with a 100 nF Output Capacitor
- Adjustable 1.20V to 88V Output Regulation
- 5% Reference Voltage Tolerance
- 50 mA Minimum Output Current Limiting
- 10 μ A Typical ADJ Current
- Overtemperature Protection
- Available in Three Different Packages

Applications

- DC/DC SMPS Startup Circuits
- Adjustable High-Voltage Constant-Current Sources
- Industrial Controls
- Motor Controls
- Battery-Powered Systems
- Power Supplies
- Telecommunications Applications
- LED Drivers
- Automotive Applications

General Description

The LR12 is a high-voltage, low-output current and adjustable linear regulator. It has a wide operating input voltage range of 13.2V to 100V. The output voltage can be adjusted between 1.2V and 88V, provided that the input voltage is at least 12V greater than the output voltage. The output voltage can be adjusted by means of two external resistors, R_1 and R_2 , as shown in the [Typical Application Circuit](#) diagrams. The LR12 regulates the voltage difference between V_{OUT} and ADJ pins to a nominal value of 1.2V, which is amplified by the external resistor ratio, R_1 and R_2 . A typical internal constant bias current of 10 μ A is connected to the ADJ pin. This increases V_{OUT} by a constant voltage of 10 μ A times R_2 .

The LR12 is current limiting and temperature limiting. The output current limit is 100 mA maximum, and the minimum temperature limit is 125°C. An output short circuit current will therefore be limited to 100 mA maximum. When the junction temperature reaches its temperature limit, the output current and/or output voltage will decrease to keep the junction temperature from exceeding the limit. For SMPS startup circuit applications, the LR12 turns off when an external voltage greater than the output voltage of the LR12 is applied to V_{OUT} of the LR12. To maintain stability, a bypass capacitor of 100 nF or larger and a minimum DC output current of 500 μ A are required.

Package Types

3-lead TO-252
(Top View)



8-lead SOIC
(Top View)



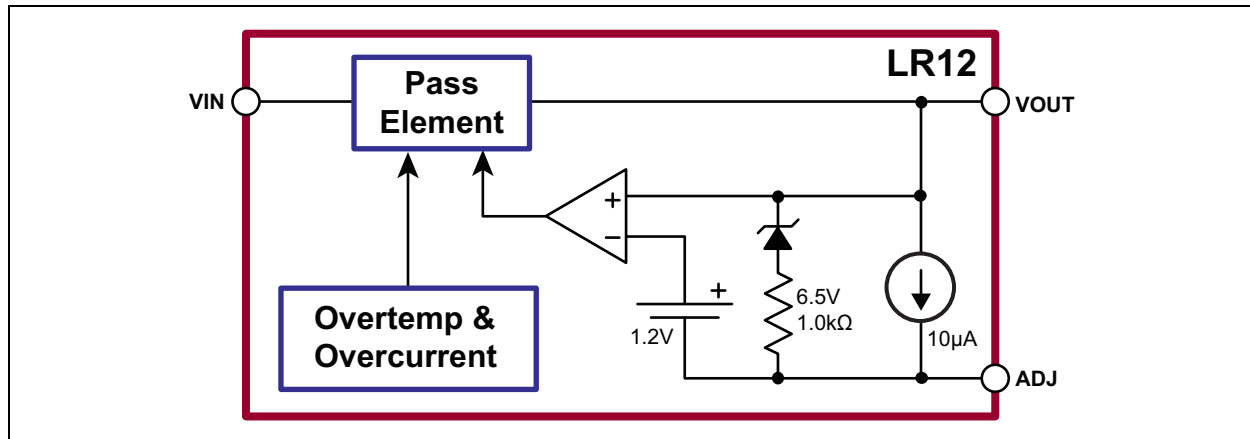
3-lead TO-92
(Top View)



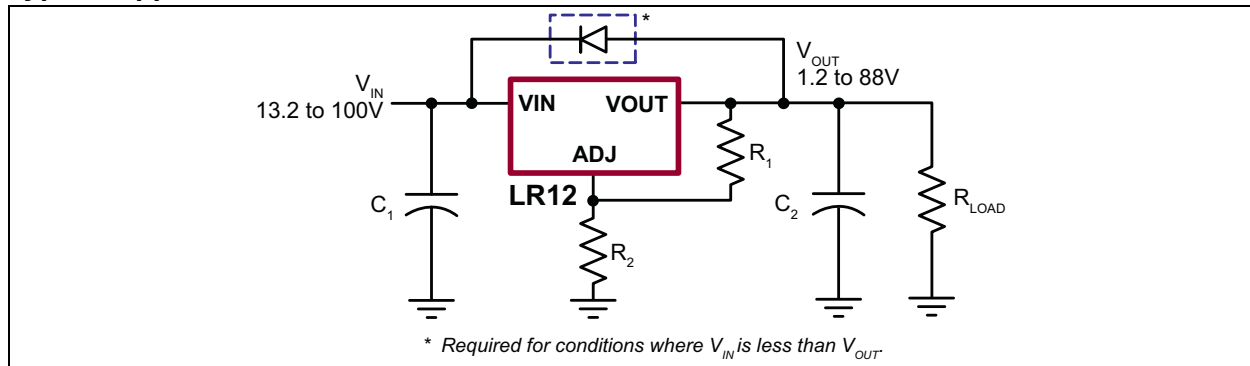
See [Table 3-1](#), [Table 3-2](#), and [Table 3-3](#) for pin information.

LR12

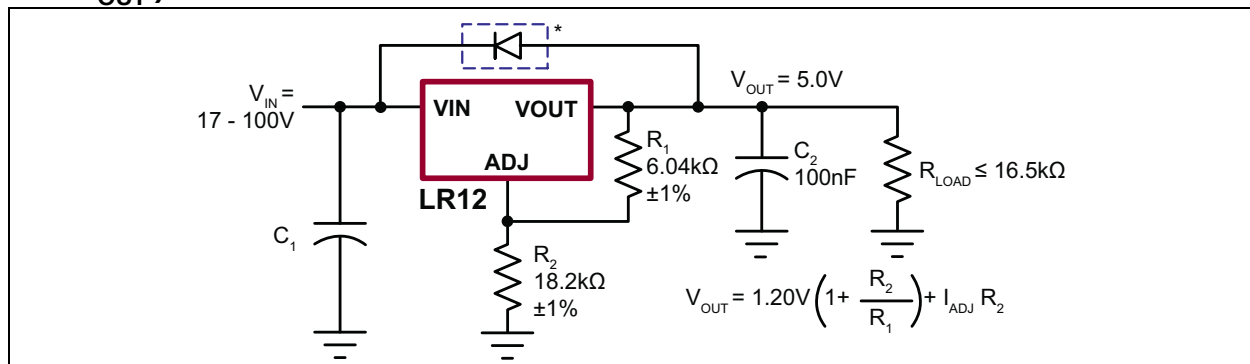
Functional Block Diagram



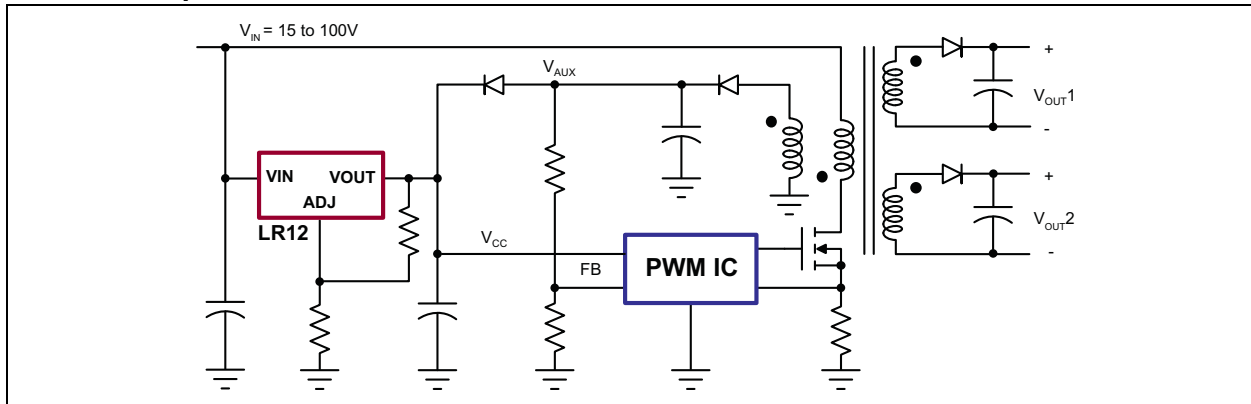
Typical Application Circuit



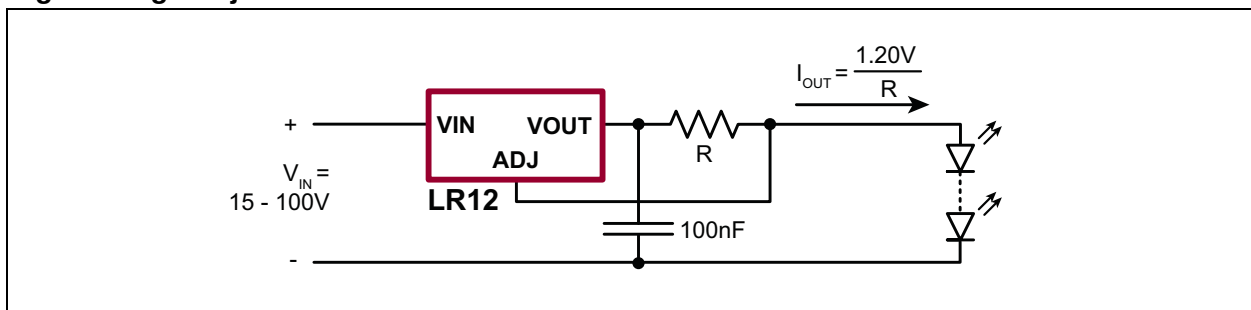
High-input Voltage, 5V Output Linear Regulator (Required for conditions where V_{IN} is less than V_{OUT}).



SMPS Startup Circuit



High-Voltage Adjustable Constant Current Source



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN-ADJ}	-0.5V to +120V
$V_{OUT-ADJ}$	-10V to +10V
$V_{IN-V_{OUT}}$	-0.5V to +120V
Operating Ambient Temperature, T_A	-40°C to +85°C
Operating Junction Temperature, T_J	-40°C to +125°C
Storage Temperature, T_S	-65°C to +150°C
Power Dissipation at $T_A = 25^\circ\text{C}$:	
3-lead TO-252 (DPAK)	2W
8-lead SOIC	1.8W
3-lead TO-92	0.6W

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Test conditions unless otherwise specified: $-40^\circ\text{C} < T_A < +85^\circ\text{C}$						
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Input-to-output Voltage Difference	$V_{IN-V_{OUT}}$	12	—	98.8	V	
Overall Output Voltage Regulation	V_{OUT}	1.14	1.2	1.26	V	$13.2\text{V} < V_{IN} < 100\text{V}$, $R_1 = 2.4\text{ k}\Omega$, $R_2 = 0$
Line Regulation	ΔV_{OUT}	—	0.003	0.03	%/V	$15\text{V} < V_{IN} < 100\text{V}$, $V_{OUT} = 5\text{V}$, $I_{OUT} = 0.5\text{A}$
Load Regulation		—	1.4	3	%	$V_{IN} = 15\text{V}$, $V_{OUT} = 5\text{V}$, $0.5\text{ mA} < I_{OUT} < 50\text{ mA}$
Temperature Regulation		-1	—	+1	%	$V_{IN} = 15\text{V}$, $V_{OUT} = 5\text{V}$, $I_{OUT} = 10\text{ mA}$, $-40^\circ\text{C} < T_A < 85^\circ\text{C}$
Output Current Limit	I_{OUT}	50	—	100	mA	$T_J < 85^\circ\text{C}$, $V_{IN-V_{OUT}} < 12\text{V}$
Minimum Output Current		—	—	-0.5		$T_J < 125^\circ\text{C}$, $V_{IN-V_{OUT}} < 100\text{V}$
Adjust Output Current	I_{ADJ}	5	10	15	μA	Includes R_1 and load current
Minimum Output Load Capacitance	C_2	100	—	—	nF	
Ripple Rejection Ratio	DV_{OUT}/DV_{IN}	50	60	—	dB	120 Hz, $V_{OUT} = 5\text{V}$

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-40	—	+85	$^\circ\text{C}$	
Operating Junction Temperature	T_J	-40	—	+125	$^\circ\text{C}$	
Storage Temperature	T_S	-65	—	+150	$^\circ\text{C}$	
PACKAGE THERMAL RESISTANCE						
3-lead TO-252 (DPAK)	θ_{JA}	—	81	—	$^\circ\text{C/W}$	
8-lead SOIC	θ_{JA}	—	101	—	$^\circ\text{C/W}$	
3-lead TO-92	θ_{JA}	—	132	—	$^\circ\text{C/W}$	

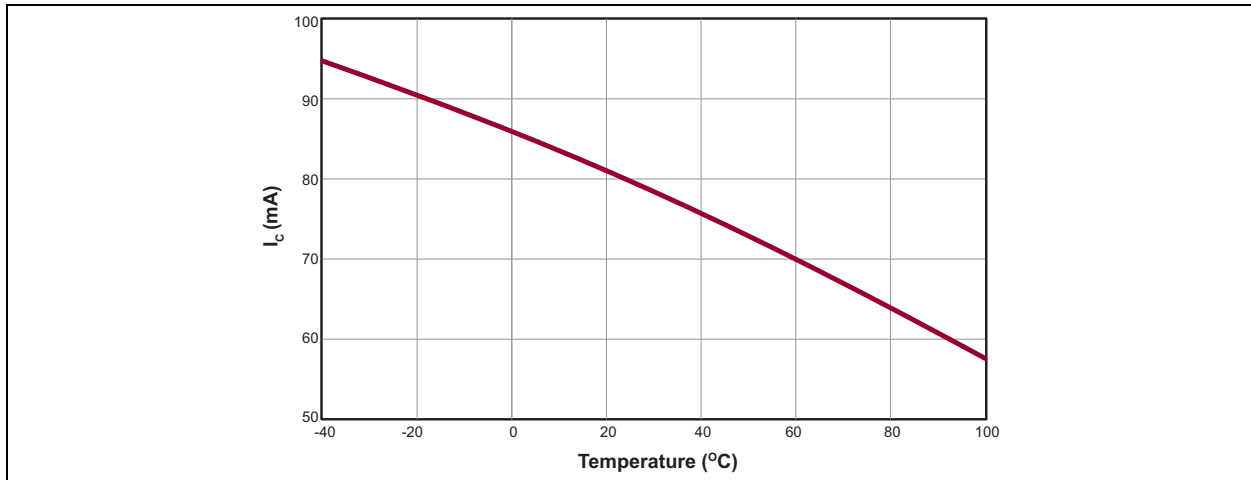


FIGURE 1-1: *Current Limit.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

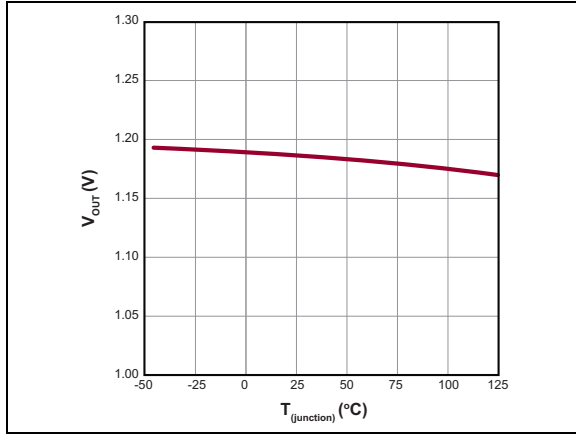


FIGURE 2-1: Temperature Variation
(See Figure 4-1).

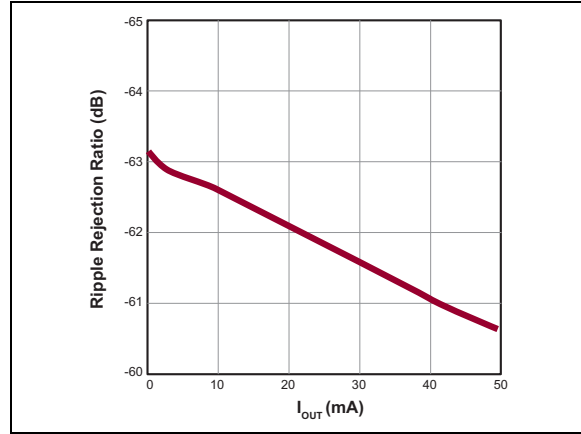


FIGURE 2-4: Ripple Rejection
(See Figure 4-4).

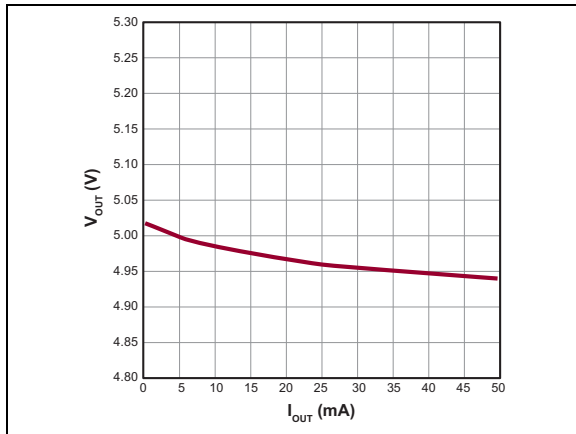


FIGURE 2-2: Load Regulation
(See Figure 4-2).

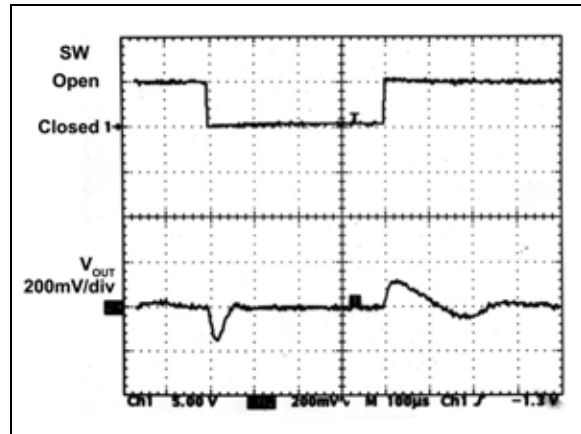


FIGURE 2-5: Load Transient Response,
Load = 509Ω (See Figure 4-5).

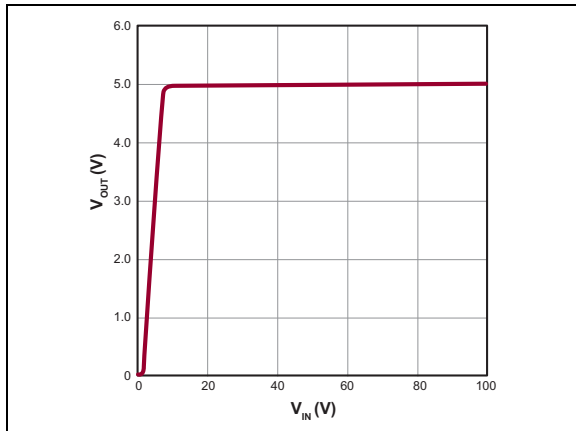


FIGURE 2-3: V_{OUT} vs. V_{IN}
(See Figure 4-3).

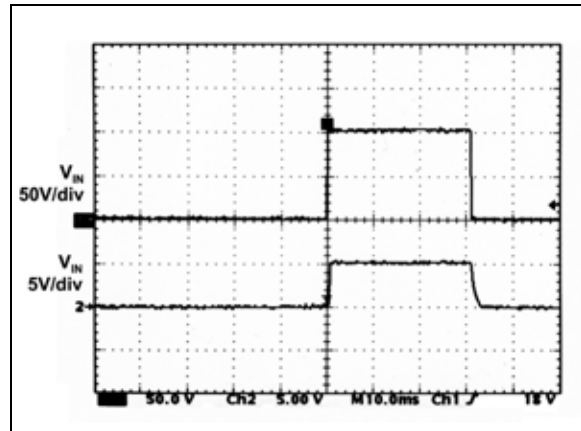


FIGURE 2-6: Line Turn-On/Off Response,
(See Figure 4-6).

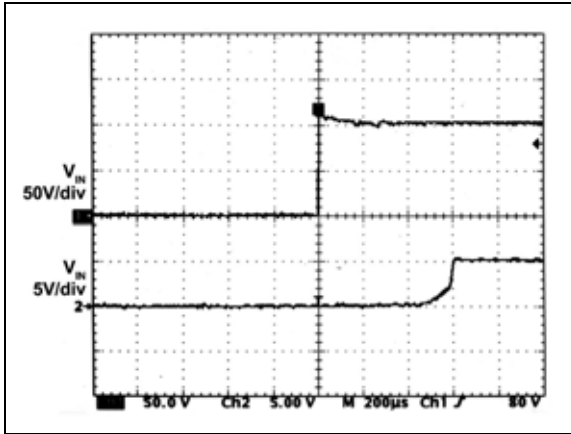


FIGURE 2-7: Line Power-Up Transient
(See [Figure 4-6](#)).

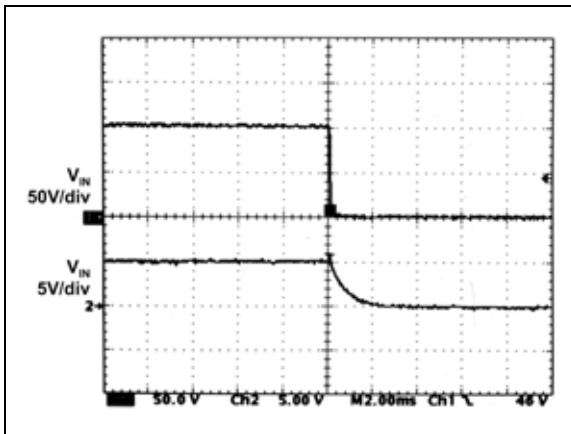


FIGURE 2-8: Line Power-Down Transient
(See [Figure 4-6](#)).

3.0 PIN DESCRIPTIONS

The details on the pins of LR12 3-lead TO-252 (DPAK), 8-lead SOIC, and 3-lead TO-92 packages are listed in [Table 3-1](#), [Table 3-2](#), and [Table 3-3](#), respectively. Refer to [Package Types](#) for the location of pins.

TABLE 3-1: 3-LEAD TO-252 (DPAK) PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VIN	Regulator Input Voltage
2	VOUT	Regulator Output Voltage
3	ADJ	Adjustment Pin
4	VOUT	Regulator Output Voltage

TABLE 3-2: 8-LEAD SOIC PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	ADJ	Adjustment Pin
2	NC	No Connection
3	NC	No Connection
4	VIN	Regulator Input Voltage
5	VOUT	Regulator Output Voltage
6	VOUT	Regulator Output Voltage
7	VOUT	Regulator Output Voltage
8	VOUT	Regulator Output Voltage

TABLE 3-3: 3-LEAD TO-92 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VIN	Regulator Input Voltage
2	VOUT	Regulator Output Voltage
3	ADJ	Adjustment Pin

4.0 APPLICATION INFORMATION

4.1 Measurement Circuits

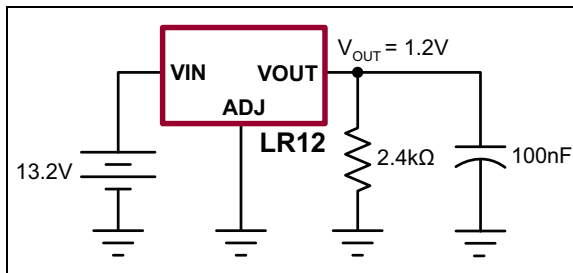


FIGURE 4-1: Temperature Variation Diagram (See [Figure 2-1](#)).

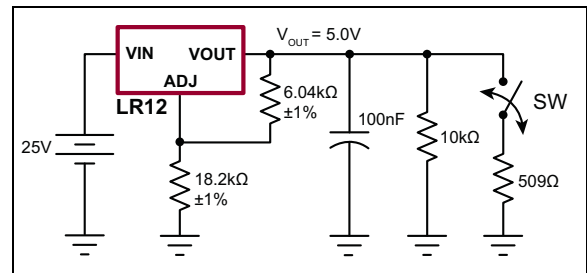


FIGURE 4-5: Load Transient Response Diagram (See [Figure 2-5](#)).

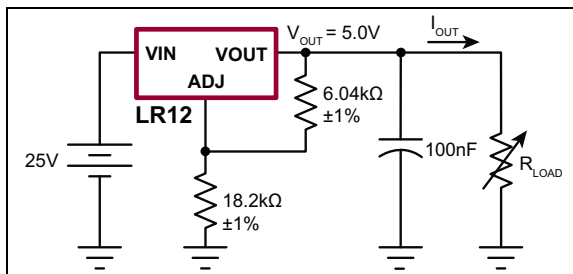


FIGURE 4-2: Load Regulation Diagram (See [Figure 2-2](#)).

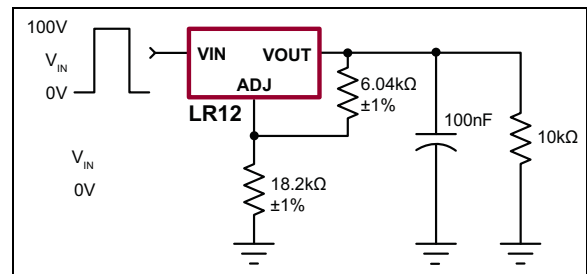


FIGURE 4-6: Line Transient Response (See [Figure 2-6](#), [Figure 2-7](#) and [Figure 2-8](#)).

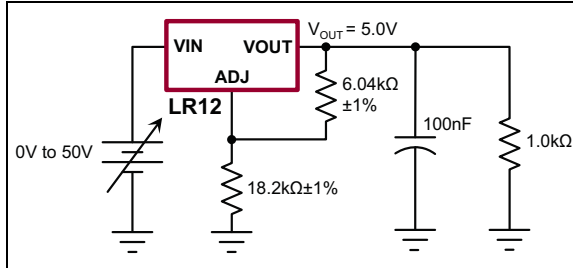


FIGURE 4-3: V_{OUT} vs. V_{IN} Diagram (See [Figure 2-3](#)).

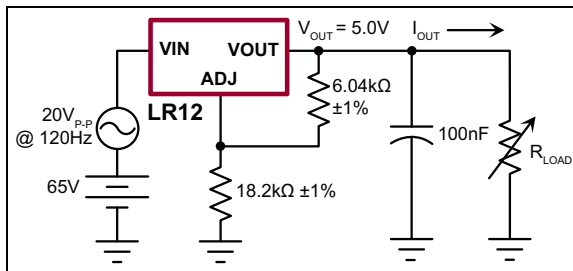
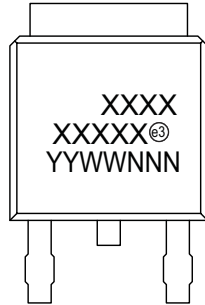


FIGURE 4-4: Ripple Rejection Diagram (See [Figure 2-4](#)).

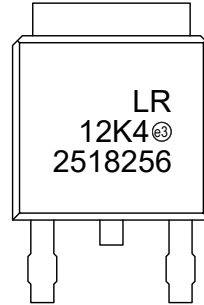
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

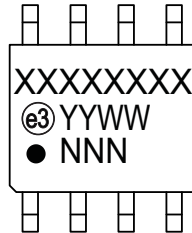
TO-252 (D-PAK)



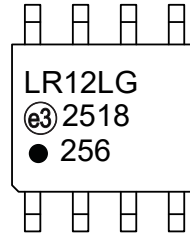
Example



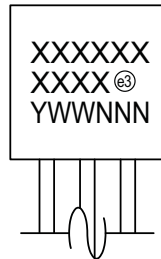
8-lead SOIC



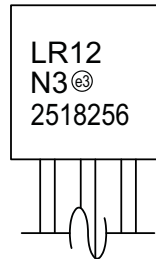
Example



3-lead TO-92



Example

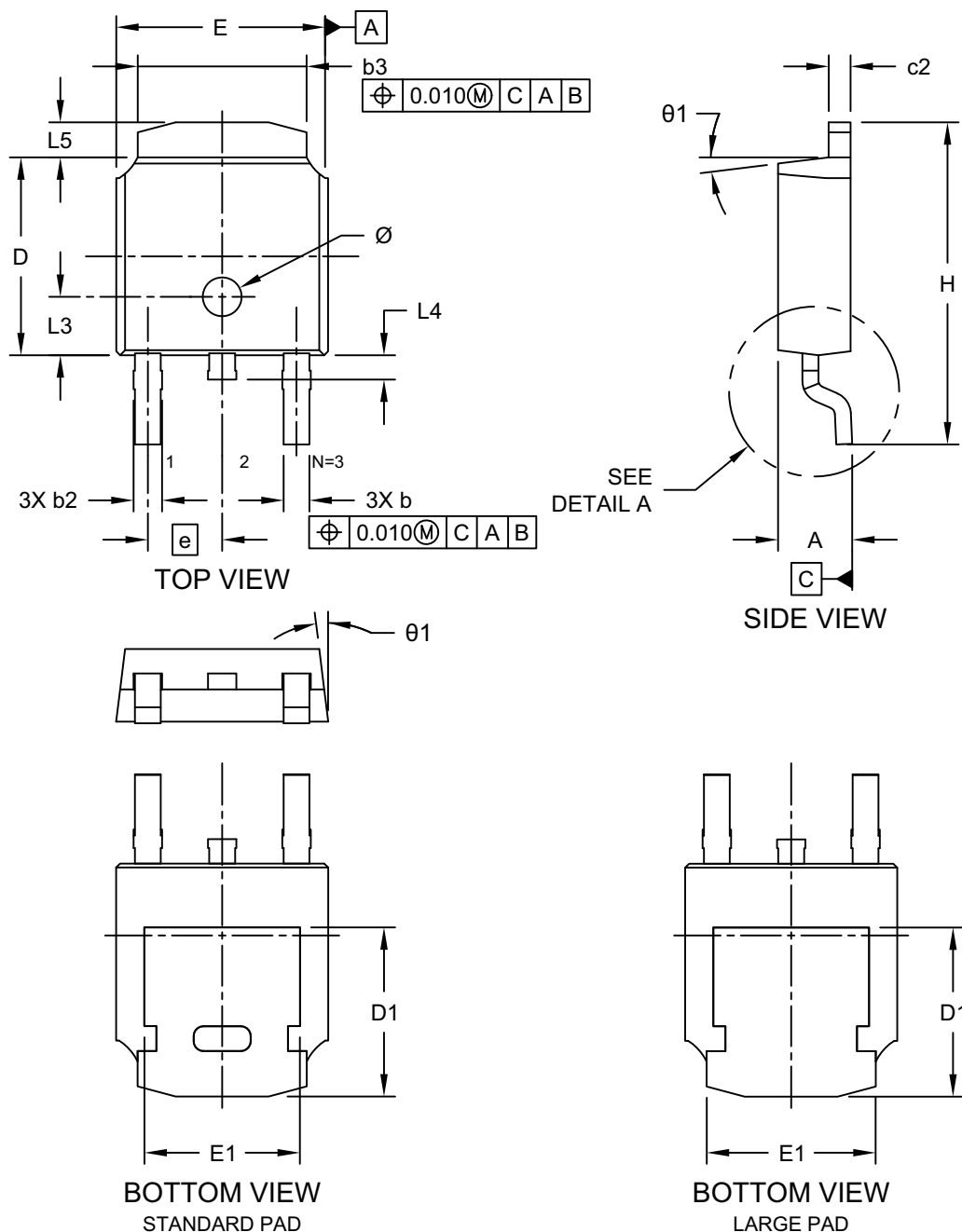


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	ⓔ	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (ⓔ) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or may not include the corporate logo.

3-Lead Deca-Watt Package, TO-252 (EA) - [DPAK]; Supertex Legacy Package Code K4

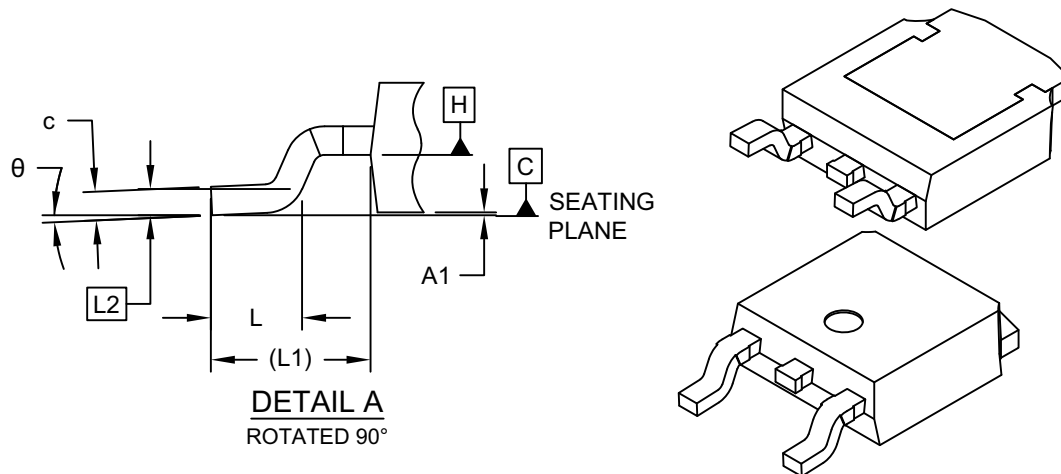
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-189 Rev C Sheet 1 of 2

3-Lead Deca-Watt Package, TO-252 (EA) - [DPAK]; Supertex Legacy Package Code K4

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units	INCHES		
	MIN	NOM	MAX
N (Leads)	3		
e	.090 BSC		
A	.086	-	.094
A1	.000	-	.005
b	.028	-	.035
b2	.030	-	.045
c	.018	-	.024
c2	.018	-	.035
D	.235	.240	.245
D1	.205	-	-
E	.250	-	.265
E1	.170	-	-
H	.370	-	.410
L	.055	.060	.070
L1	.108 REF		
L2	.020 BSC		
L3	.065	-	.077
L4	.024	-	.035
L5	.035	-	.050
theta	1°	-	5°
theta1	7° REF		

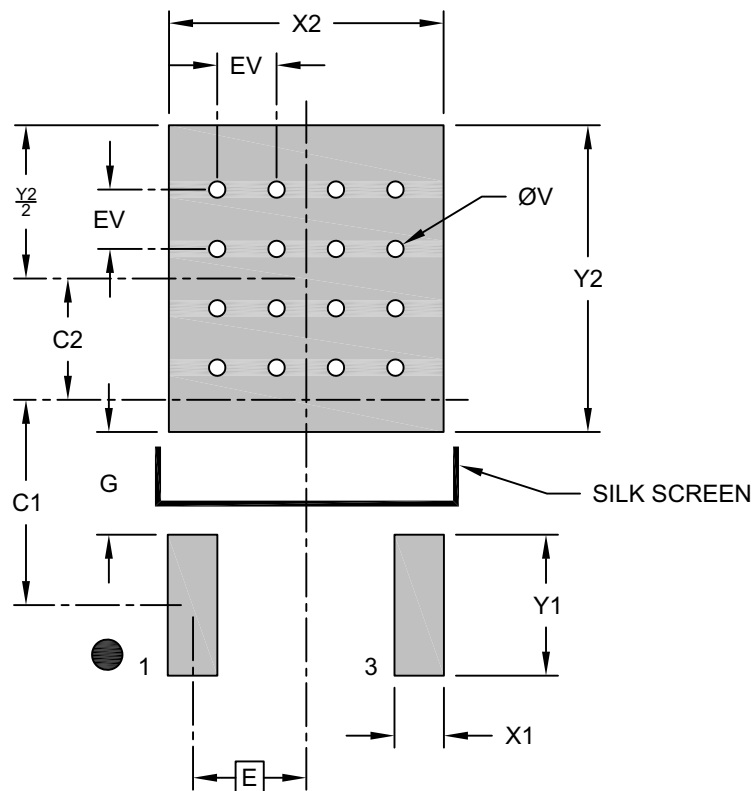
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-189 Rev C Sheet 1 of 2

3-Lead Deca-Watt Package, TO-252 (EA) - [DPAK]; Supertex Legacy Package Code K4

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Contact Pitch	E	.090 BSC		
Center Pad Width	X2			.219
Center Pad Length	Y2			.244
Contact Pad Spacing	C1		.163	
Contact Pad Spacing	C2		.096	
Contact Pad Width (Xnn)	X1			.039
Contact Pad Length (Xnn)	Y1			.112
Contact Pad to Contact Pad (Xnn)	G	.412		
Thermal Via Diameter	V		.013	
Thermal Via Pitch	EV		.047	

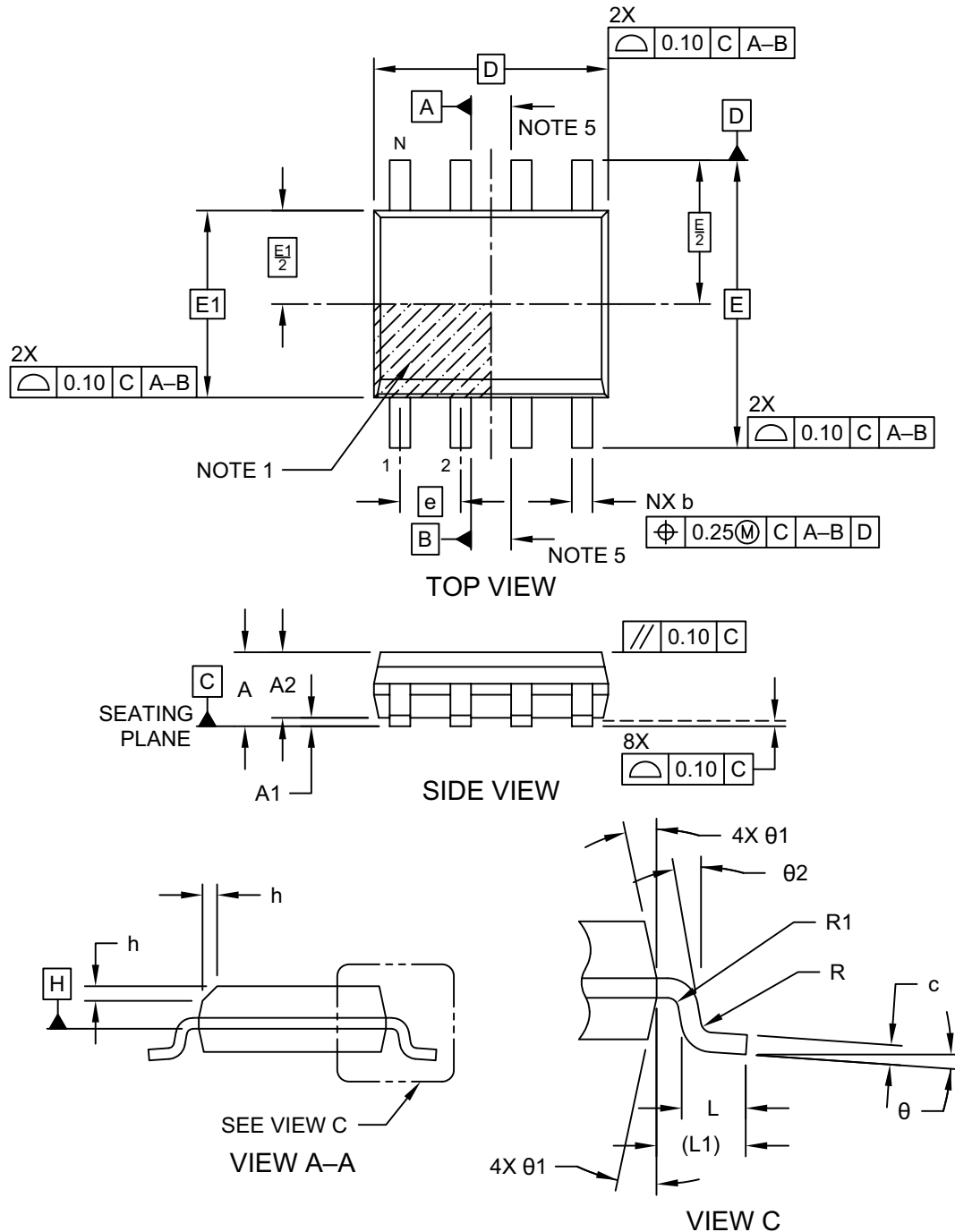
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2189 Rev C

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Atmel Legacy Global Package Code SWB

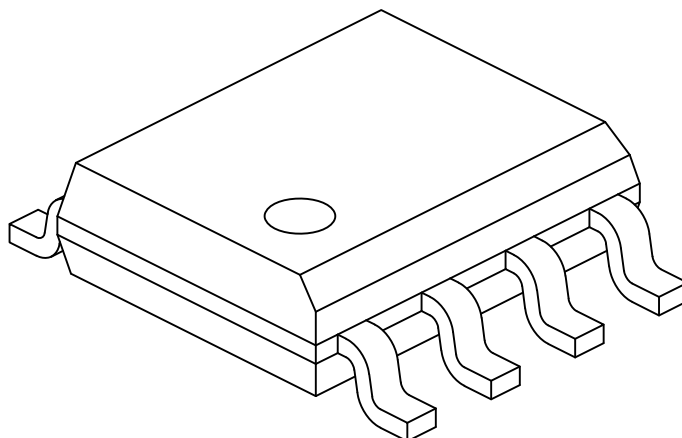
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packageing>



Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

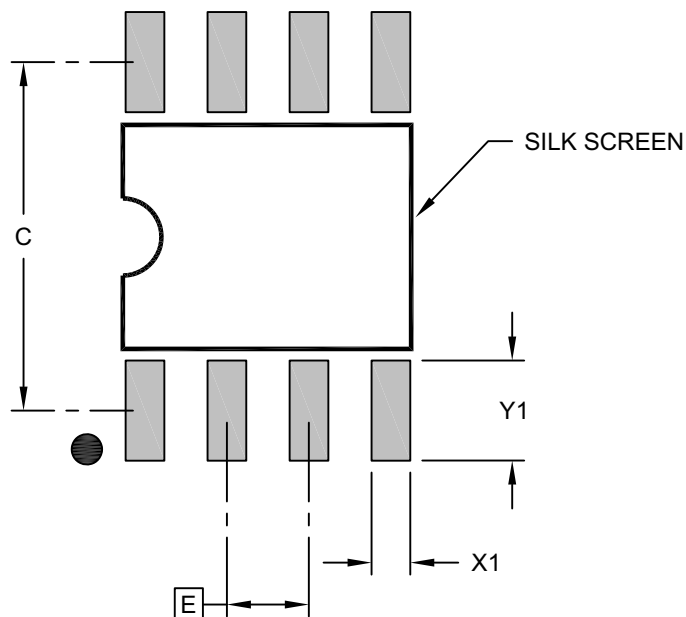
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

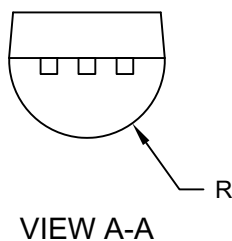
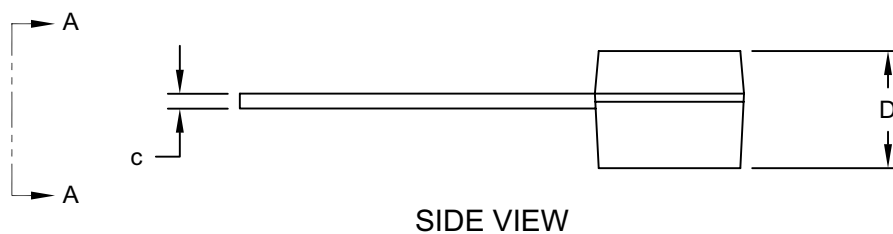
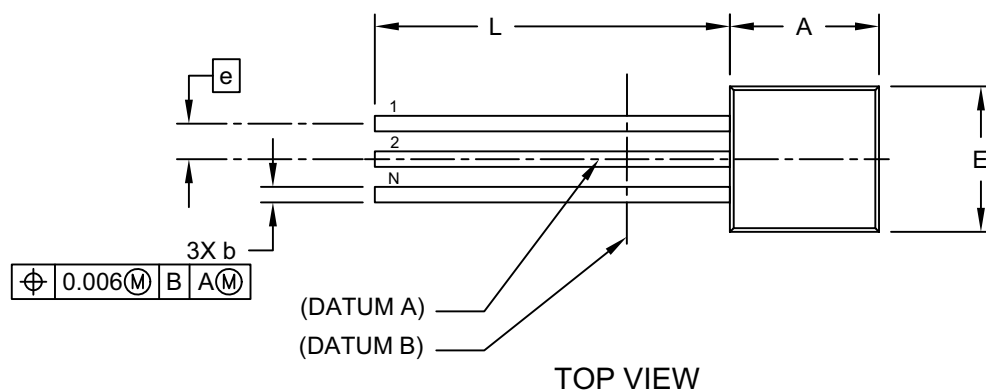
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-C2X Rev K

3-Lead Plastic Transistor Outline (TO) [TO-92]

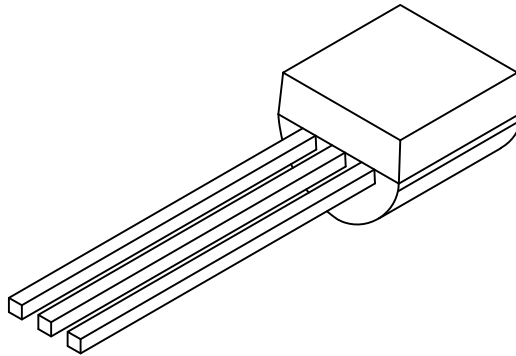
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-101-TO Rev D Sheet 1 of 2

3-Lead Plastic Transistor Outline (TO) [TO-92]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	3		
Pitch	e	.050 BSC		
Bottom to Package Flat	D	.125	-	.165
Overall Width	E	.175	-	.205
Overall Length	A	.170	-	.210
Molded Package Radius	R	.080	-	.105
Tip to Seating Plane	L	.500	-	-
Lead Thickness	c	.014	-	.021
Lead Width	b	.014	-	.022

Notes:

- Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-101-TO Rev D Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision B (July 2025)

- Removed pin labels from [Package Types](#).
- Corrected pin numbers and labels in [Table 3-2](#).
- Updated Package Drawings in [Section 5.0, Packaging Information](#)

Revision A (August 2022)

- Converted Supertex Doc# DSFP-LR12 to Microchip DS20005735A
- Updated package marking format
- Changed the quantity of the 8-lead SOIC LG package from 2500/Reel to 3300/Reel to align packaging specifications with the actual BQM
- Removed the TO-92 N3 P002,P003,P005, P013, and P014 media types to align packaging specifications with the actual BQM
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	<u>-X</u>	<u>X</u>
Device	Package Options	Environmental	Media Type
Device:	LR12 = High-Input Voltage, Adjustable 3-Terminal Linear Regulator		
Packages:	K4 = 3-lead DPAK LG = 8-lead SOIC N3 = 3-lead TO-92		
Environmental:	G = Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank) = 2000/Reel for a K4 Package = 3300/Reel for an LG Package = 1000/Bag for an N3 Package		

Examples:

 a) LR12K4-G: High-Input Voltage, Adjustable 3-Terminal Linear Regulator, 3-lead DPAK, 2000/Reel

 b) LR12LG-G: High-Input Voltage, Adjustable 3-Terminal Linear Regulator, 8-lead SOIC, 3300/Reel

 c) LR12N3-G: High-Input Voltage, Adjustable 3-Terminal Linear Regulator, 3-lead TO-92, 1000/Bag

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at <https://www.microchip.com/en-us/about/legalinformation/microchip-trademarks>.

ISBN: 979-8-3371-1536-8

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.