SY89329V

3.3V/5V 800 MHz LVTTL/LVCMOS-to-Differential LVPECL Translator

Features

- Ensured AC Performance over Temperature and Voltage:
  - DC-to-800 MHz f_{MAX}
  - <100 ps IN-to-OUT t_{PD}
- Ultra Low-Jitter Design:
  - <1 ps_{RMS} Random Jitter
  - <10 ps_{PP} Deterministic Jitter
  - <1 ps_{RMS} Cycle-to-Cycle Jitter
  - <1 ps_{PP} Total Jitter (Clock)
- Differential LVPECL Output
- Maximum I_{CC} of 20 mA
- Q Output will Default High with Inputs Open
- Power Supply: 3.3V ±10% or 5V ±10%
- –40C to +85°C Temperature Range
- Available in Ultra-Small 8-Lead (2 mm x 2 mm) VDFN Package

Applications

- High-Speed Logic
- Data Communication Systems
- Wireless Communication Systems
- Telecom Systems

General Description

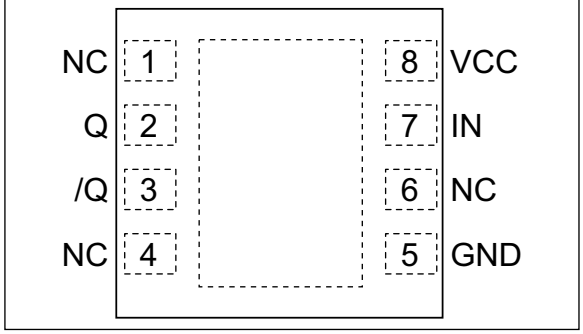
The SY89329V is a TTL/CMOS-to-differential PECL translator. Capable of running from a 3.3V or 5V supply, the part can be used in either LVTTL/LVCMOS/LVPECL or TTL/CMOS/PECL systems.

The device requires only a single positive supply of 3.3V or 5V; no negative supply is required.

The ultra-small 8-lead VDFN package of the SY89329V makes it ideal for applications where space, performance, and low power consumption are at a premium. For applications that require a dual translator in this same ultra-small VDFN package, consider the SY89322V.

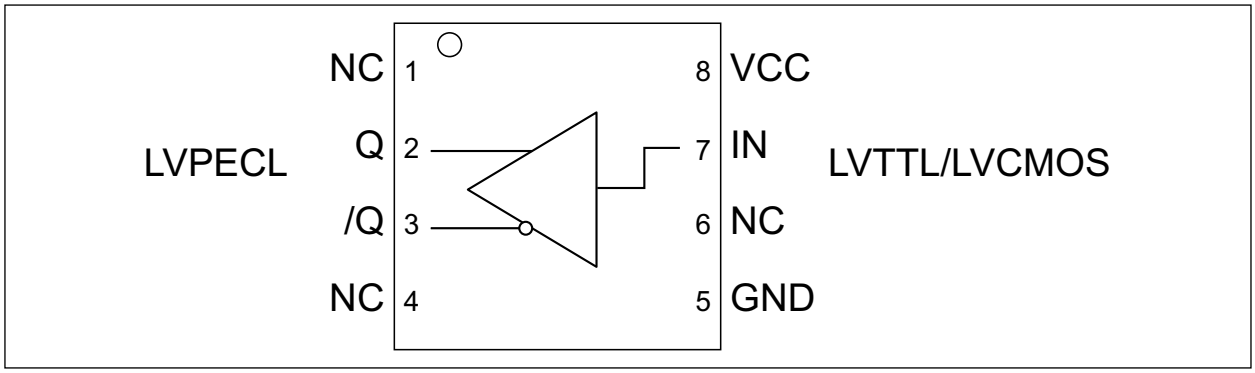
Package Type

SY89329V
8-Lead VDFN (M)
(Top View)

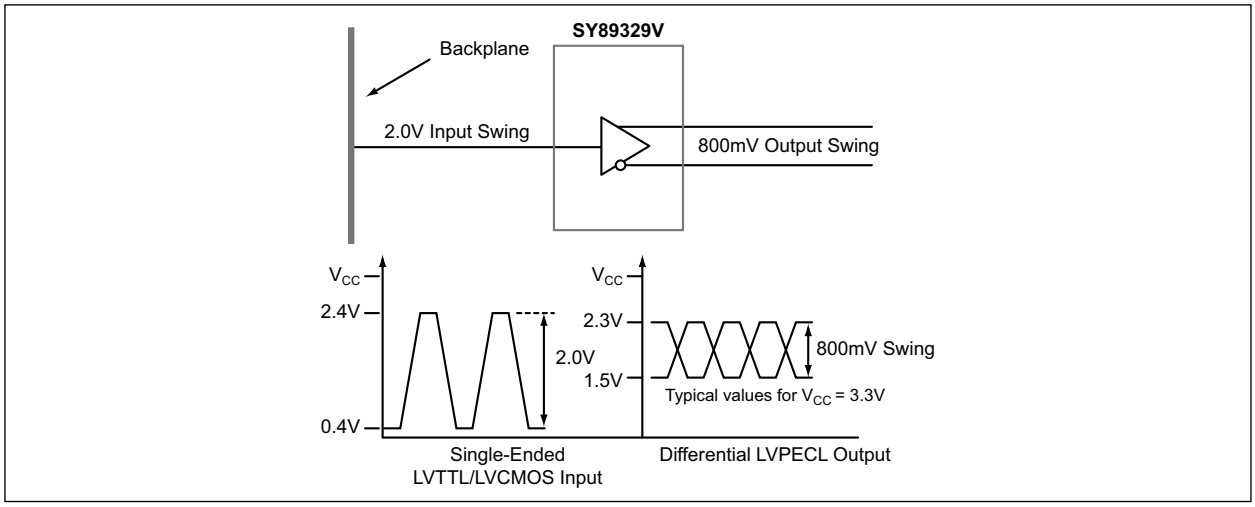


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Functional Block Diagram



Typical Application Circuit



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +6.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Voltage (V_{OUT}) ..... V_{CC} – 1.0V to V_{CC} + 0.5V
LVPECL Continuous Output Current (I_{OUT}) ..... 50 mA
LVPECL Surge Output Current (I_{OUT}) ..... 100 mA
Input Current (Source or Sink Current on IN) ..... ±50 mA

Operating Ratings ‡

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Supply Voltage (V_{CC}) ..... +4.5V to +5.5V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	—
		4.5	5.0	5.5	V	—
Power Supply Current	I_{CC}	—	—	20	mA	No load, maximum V_{CC}

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

LVTTL/LVCMOS ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage (IN, /IN)	V_{IH}	2.0	—	—	V	—
Input Low Voltage (IN, /IN)	V_{IL}	—	—	0.8	V	—
Input High Current	I_{IH}	—	—	20	µA	V_{IN} = 2.7V
		—	—	100	µA	V_{IN} = V_{CC}
Input Low Current	I_{IL}	—	—	–0.2	mA	V_{IN} = 0.5V
Input Clamp Voltage	V_{IK}	—	—	–1.2	V	I_{IN} = –18 mA

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

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LVPECL OUTPUT CHARACTERISTICS

V_{CC} = 3.3V ±10% or 5V ±10%; GND = 0V; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC} – 2V or equivalent, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage Q, /Q	V_{OH}	V_{CC} – 1.080	—	V_{CC} – 0.880	V	Note 2
Output Low Voltage Q, /Q	V_{OL}	V_{CC} – 1.830	—	V_{CC} – 1.550	V	—
Output Voltage Swing Q, /Q	V_{OUT}	600	800	—	mV	See Figure 1-1
Differential Output Voltage Swing Q, /Q	V_{DIFF_OUT}	1200	1600	—	mV	See Figure 1-2

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

2: The data sheet limits are not ensured if the device is operated beyond the operating ratings.

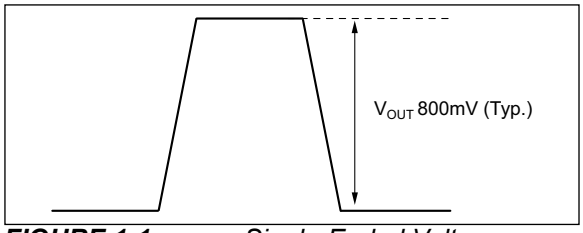


FIGURE 1-1: *Single-Ended Voltage Swing.*

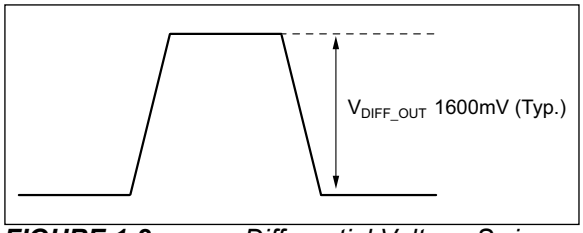


FIGURE 1-2: *Differential Voltage Swing.*

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V ±10% or 5V ±10%; T_A = –40°C to +85°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Operating Frequency	f_{MAX}	—	—	800	MHz	V_{OUT} ≥ 350 mV
Propagation Delay	t_{PD}	100	—	600	ps	IN-to-Q, /IN-to-/Q
Random Jitter (RJ)	t_{JITTER}	—	—	1	ps_{RMS}	Note 2
Deterministic Jitter (DJ)		—	—	10	ps_{PP}	Note 3
Cycle-to-Cycle Jitter		—	—	1	ps_{RMS}	Note 4
Total Jitter (TJ)		—	—	25	ps_{PP}	Note 5
Rise/Fall Time, 20% to 80% Q, /Q	t_r/t_f	200	—	500	ps	At full output swing

Note 1: Measured with outputs loaded with 50Ω to V_{CC} – 2V unless otherwise stated. See Figure 1-3 for definition of parameters. High-frequency AC-parameters are ensured by design and characterization

2: RJ is measured with a K28.7 comma detect character pattern, measured at f_{MAX}.

3: DJ is measured at f_{MAX}, with both K28.5 and 2^{23}–1 PRBS pattern.

4: Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, Tn–Tn–1 where T is the time between rising edges of the output signal.

5: Total jitter definition: with an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

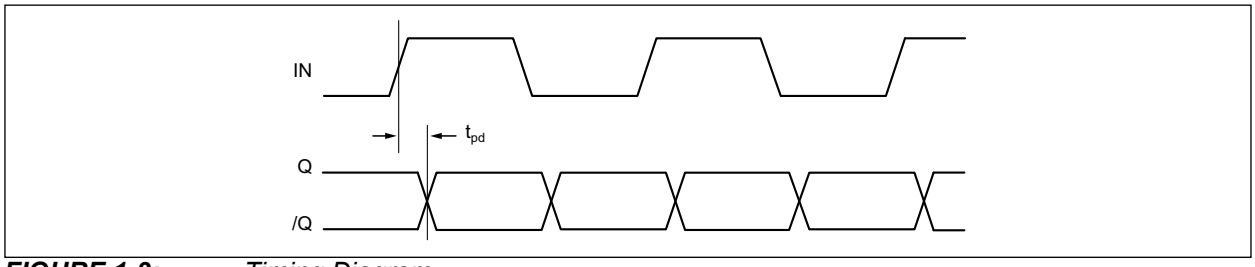


FIGURE 1-3: *Timing Diagram.*

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Package Thermal Resistances (Note 1)						
Thermal Resistance, VDFN 8-Ld	θ_{JA}	—	93	—	°C/W	Still-Air
	θ_{JA}	—	87	—	°C/W	500 lpfm
	Ψ_{JB}	—	32	—	°C/W	Junction-to-board

Note 1: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in a still air unless otherwise stated.

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 4, 6	NC	No connect.
2, 3	Q, /Q	Differential LVPECL Output: This output is the output of the device. Terminate with 50Ω to V_{CC} – 2V. See the Output Interface Applications section. Defaults HIGH if IN is floating.
5	GND Exposed Pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.
7	IN	Single-Ended Input: This is the LVTTL/LVCMOS input to the device. Input switching threshold is V_{CC}/2. If left floating, Q output will default HIGH.
8	VCC	Positive power supply. Bypass with 0.1 µF||0.01 µF low ESR capacitors.

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3.0 OUTPUT INTERFACE APPLICATIONS

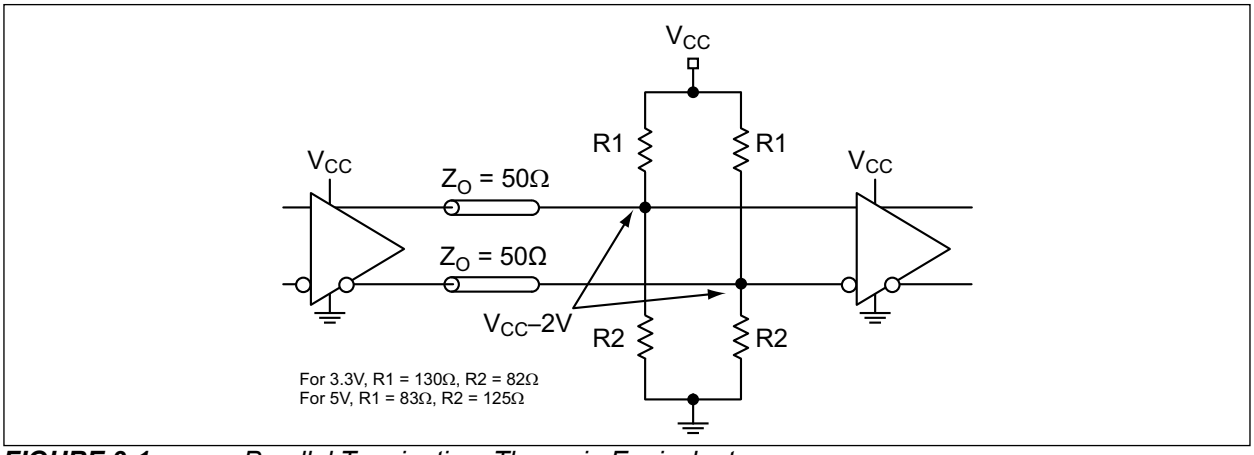


FIGURE 3-1: *Parallel Termination: Thevenin Equivalent.*

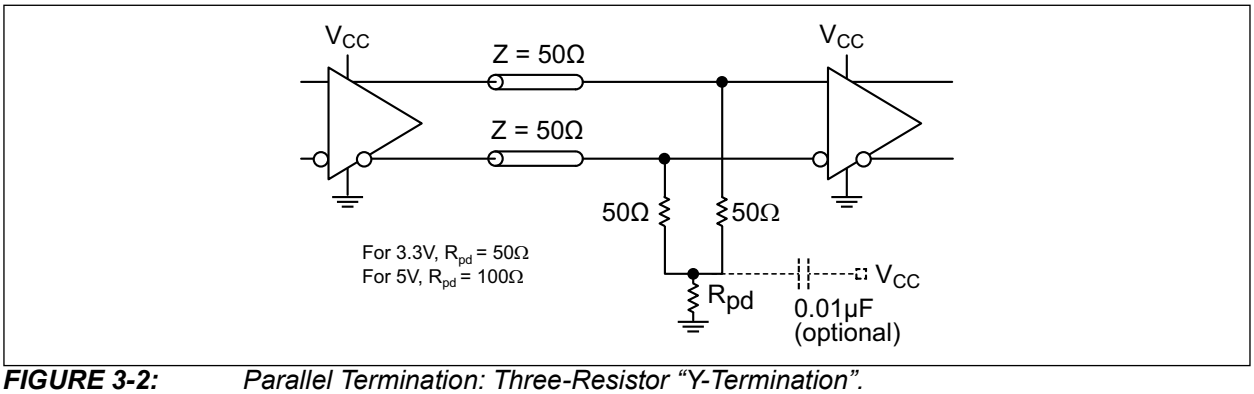


FIGURE 3-2: *Parallel Termination: Three-Resistor "Y-Termination".*

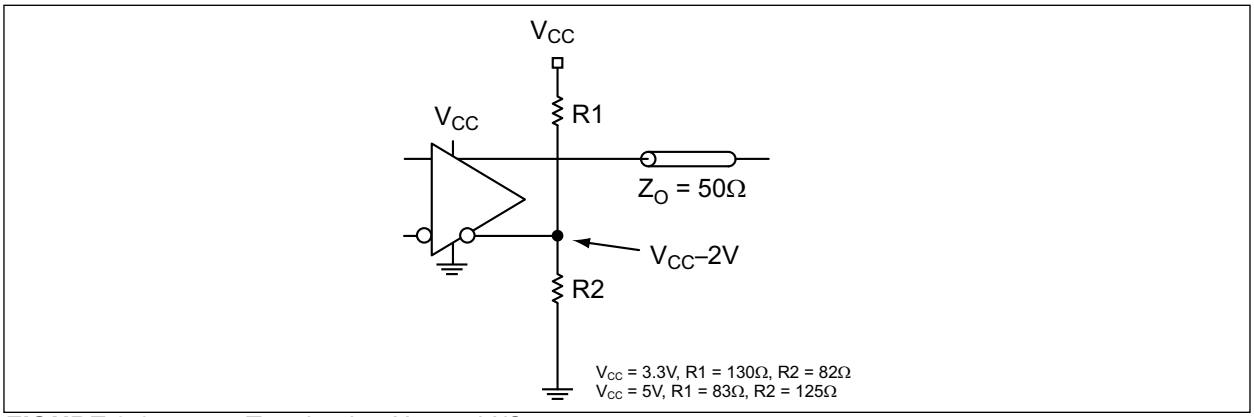


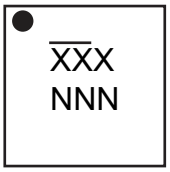
FIGURE 3-3: *Terminating Unused I/O.*

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4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-Lead VDFN*



Example

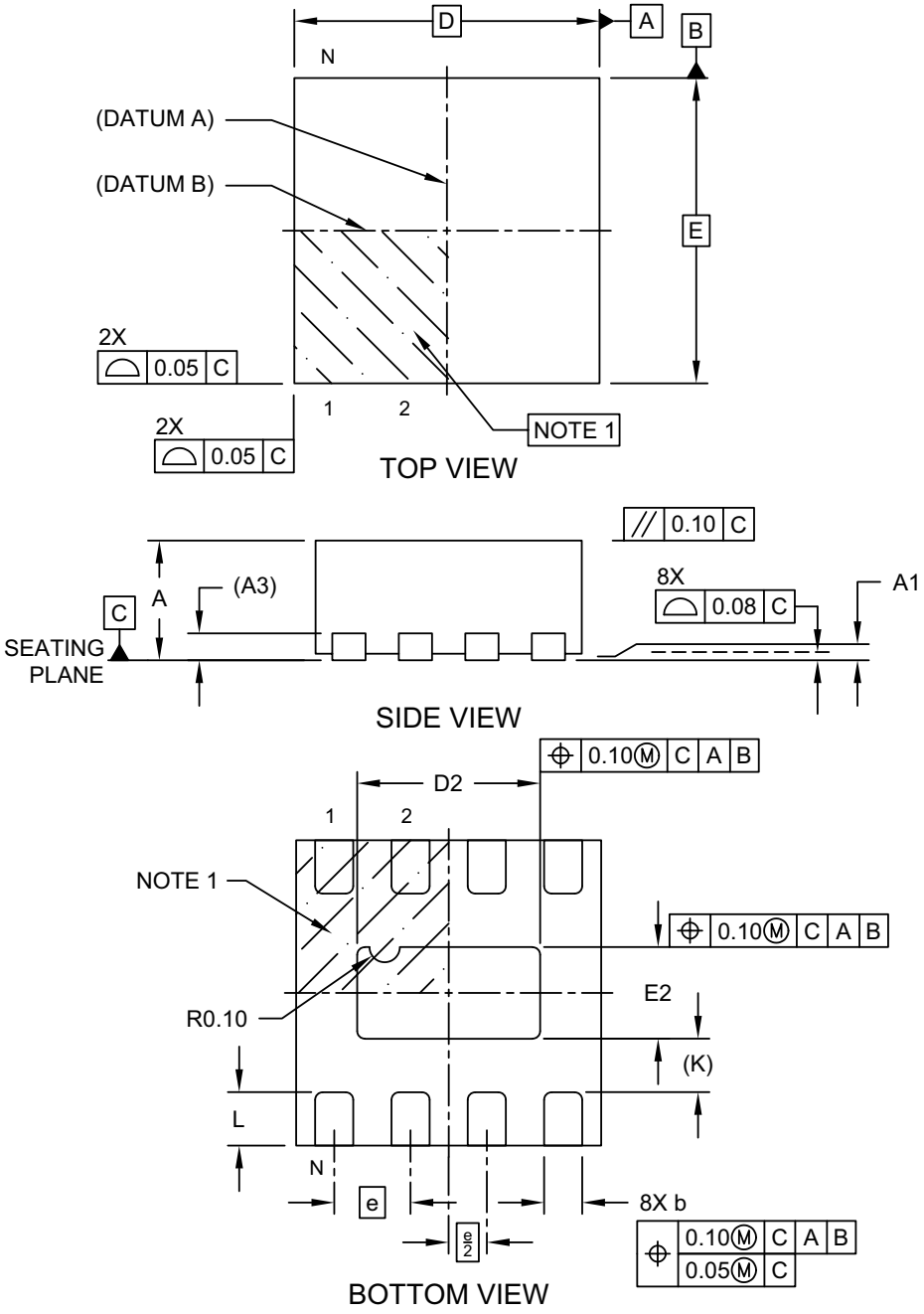


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.
		Underbar (_) and/or Overbar (‾) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

8-Lead Very Thin Plastic Dual Flat, No Lead Package (H2A) - 2x2x0.9 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

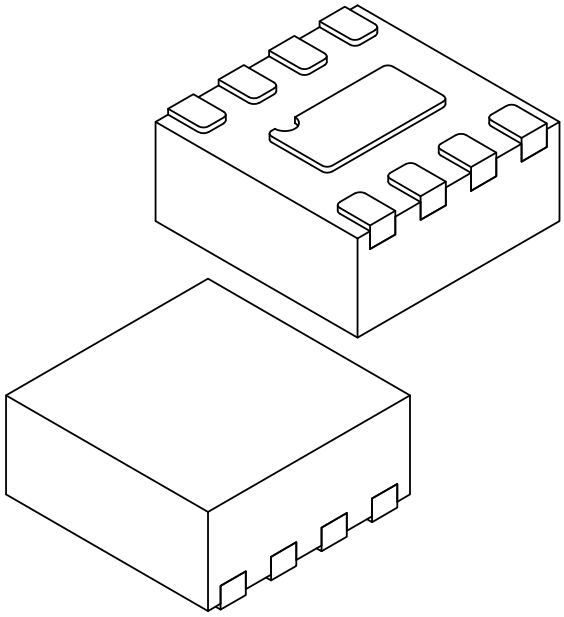
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1247 Rev B Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (H2A) - 2x2x.9 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.10	1.20	1.30
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.50	0.60	0.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K		0.35 REF	

Notes:

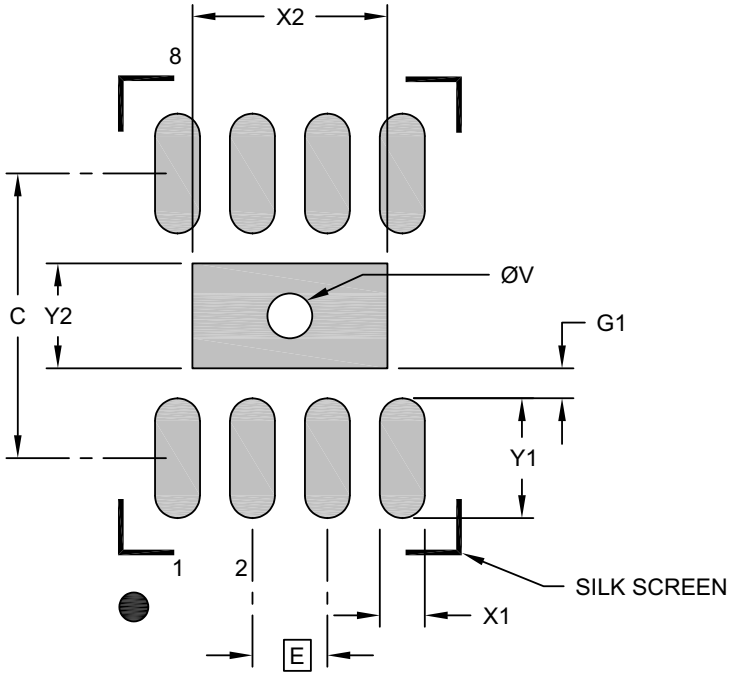
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1247 Rev B Sheet 2 of 2

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8-Lead Very Thin Plastic Dual Flat, No Lead Package (H2A) - 2x2 mm Body [VDFN] Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.30
Optional Center Pad Length	Y2			0.70
Contact Pad Spacing	C		1.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Thermal Via Diameter	V	0.27	0.30	0.33

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3247 Rev. B

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APPENDIX A: REVISION HISTORY

Revision A (May 2025)

- Converted Micrel document SY89329V to Microchip data sheet template DS20006859A.
- Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part No.	X	X	X	[-XX]
Device	Supply Voltage	Package	Temperature Range	Media Type

Device:	SY89329:	3.3V/5V 800 MHz LVTTL/LVCMOS-to-Differential LVPECL Translator	
Supply Voltage:	V	=	3.3V/5V
Package:	M	=	8-Lead 2 mm x 2 mm VDFN
Temperature Range:	G	=	–40°C to +85°C
Media Type:	TR	=	1,000/Reel

Examples:

a) SY89329VMG-TR:

SY89329, 3.3V/5V Supply Voltage, 8-Lead VDFN, –40°C to +85°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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