

Minimum Parts High-Side or Low-Side MOSFET Driver

Features

- 4.75V to 32V Operation
- Less than 1 μA Standby Current in the “Off” State
- Internal Charge Pump to Drive the Gate of an N-Channel Power FET Above Supply
- Available in Small Outline SOIC Package
- Internal Zener Clamp for Gate Protection
- Minimum External Parts Count
- Can be Used to Boost Drive to Low-Side Power FETs Operating on Logic Supplies
- 25 μs Typical Turn-On Time with Optional External Capacitors
- Implements High- or Low-Side Drivers

Applications

- Lamp Drivers
- Relay and Solenoid Drivers
- Heater Switching
- Power Bus Switching

General Description

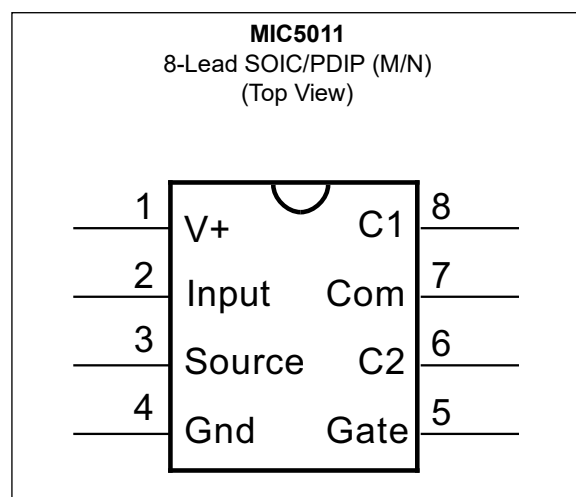
The MIC5011 is the “minimum parts count” member of the Microchip MIC501x driver family. These ICs are designed to drive the gate of an N-channel power MOSFET above the supply rail in high-side power switch applications. The 8-lead MIC5011 is extremely easy to use, requiring only a power FET and nominal supply decoupling to implement either a high- or low-side switch.

The MIC5011 charges a 1 nF load in 60 μs typical with no external components. Faster switching is achieved by adding two 1 nF charge pump capacitors. Operation down to 4.75V allows the MIC5011 to drive standard MOSFETs in 5V low-side applications by boosting the gate voltage above the logic supply. In addition, multiple paralleled MOSFETs can be driven by a single MIC5011 for ultra-high current applications.

Other members of the Microchip driver family include the MIC5013 protected 8-lead driver.

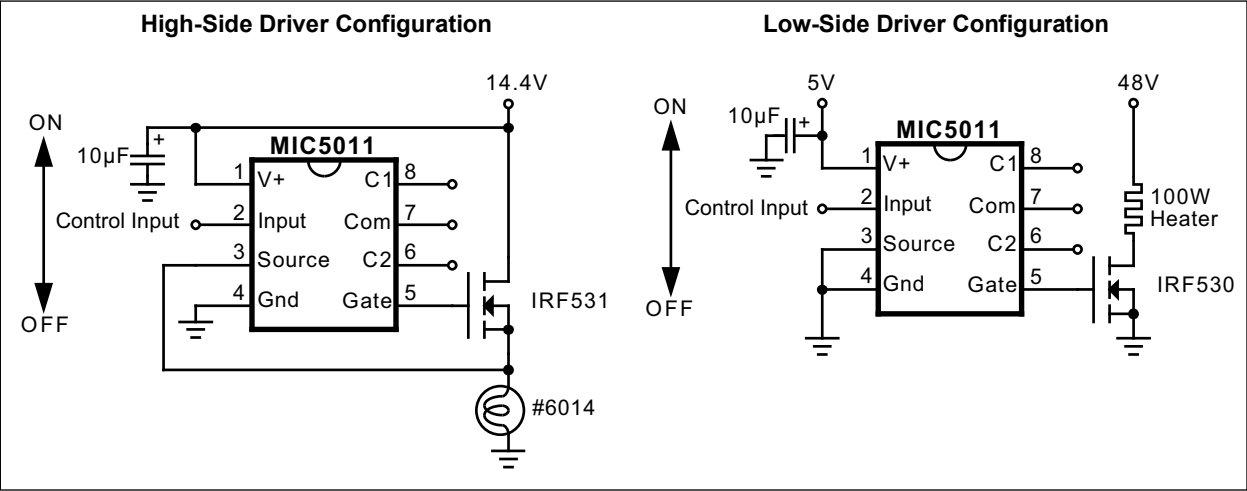
For new designs, Microchip recommends the pin-compatible MIC5014 MOSFET driver.

Package Type

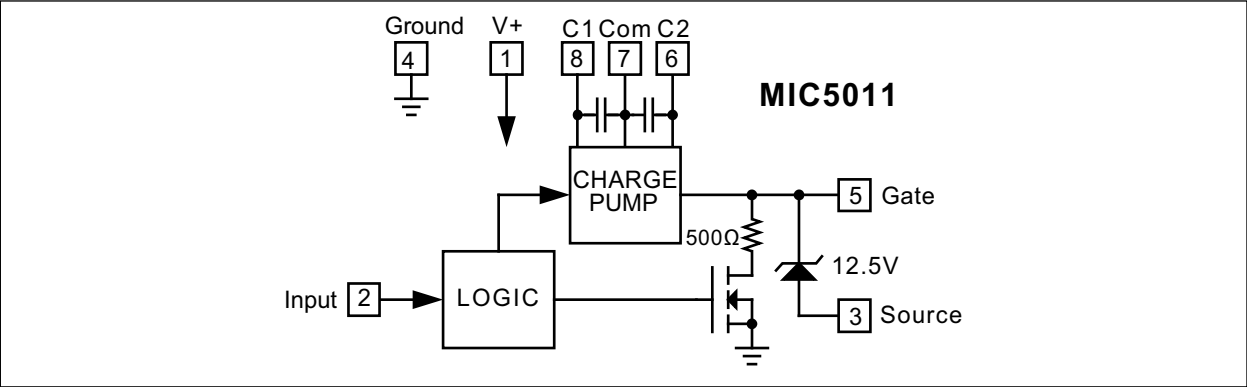


MIC5011

Typical Application Circuits



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V^+ , Pin 1)	–0.5V to +36V
Input Voltage (Pin 2)	–10V to V^+
Source Voltage (Pin 3)	–10V to V^+
Current Into Pin 3	50 mA
Gate Voltage (Pin 5)	–1V to +50V
ESD Rating	Note 1

Operating Ratings ‡

Power Dissipation	1.25W
Supply Voltage (V^+ , Pin 1 High-Side)	+4.75V to +32V
Supply Voltage (V^+ , Pin 1 Low-Side)	+4.75V to +15V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: The MIC5011 is ESD sensitive.

ELECTRICAL CHARACTERISTICS

Test Circuit. $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V^+ = 15\text{V}$, all switches open, unless otherwise specified. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current	I_1	—	0.1	10	μA	$V^+ = 32\text{V}$, $V_{\text{IN}} = 0\text{V}$, S2 closed
		—	8	20	mA	$V^+ = 32\text{V}$, $V_{\text{IN}} = V^+ = 32\text{V}$
		—	1.6	4	mA	$V^+ = 5\text{V}$, $V_{\text{IN}} = 5\text{V}$, S2 closed
Logic Input Voltage	V_{IL}	—	—	2	V	$V^+ = 4.75\text{V}$, Adjust V_{IN} for V_{GATE} low
	V_{IH}	4.5	—	—	V	$V^+ = 4.75\text{V}$, Adjust V_{IN} for V_{GATE} high
		5.0	—	—	V	$V^+ = 15\text{V}$, Adjust V_{IN} for V_{GATE} high
Logic Input Current	I_2	–1	—	—	μA	$V^+ = 32\text{V}$, $V_{\text{IN}} = 0\text{V}$
		—	—	1		$V^+ = 32\text{V}$, $V_{\text{IN}} = 32\text{V}$
Input Capacitance	C_{IN}	—	5	—	pF	Pin 2
Gate Drive	V_{GATE}	7	10	—	V	S1, S2 closed, $V_S = V^+$, $V_{\text{IN}} = 5\text{V}$, $V^+ = 4.75\text{V}$, $I_{\text{GATE}} = 0$, $V_{\text{IN}} = 4.5\text{V}$
		24	27	—	V	S1, S2 closed, $V_S = V^+$, $V_{\text{IN}} = 5\text{V}$, $V^+ = 15\text{V}$, $I_{\text{GATE}} = 100\text{ }\mu\text{A}$, $V_{\text{IN}} = 5\text{V}$
Zener Clamp ($V_{\text{GATE}} - V_{\text{SOURCE}}$)	—	11	12.5	15	V	S2 closed, $V_{\text{IN}} = 5\text{V}$, $V^+ = 15\text{V}$, $V_S = 15\text{V}$
		11	13	16		S2 closed, $V_{\text{IN}} = 5\text{V}$, $V^+ = 32\text{V}$, $V_S = 32\text{V}$

MIC5011

ELECTRICAL CHARACTERISTICS (CONTINUED)

Test Circuit. $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V^+ = 15\text{V}$, all switches open, unless otherwise specified. [Note 1](#)

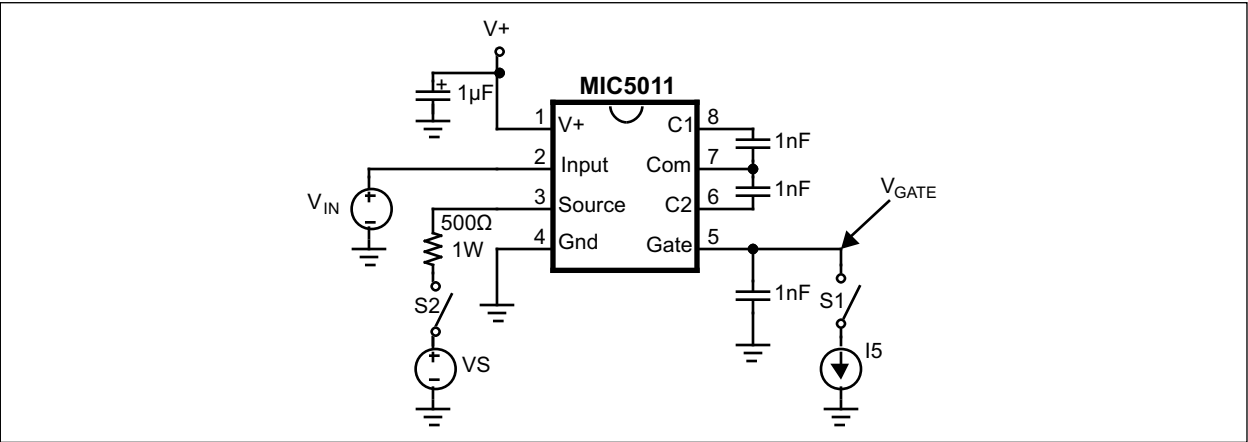
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Gate Turn-On Time	t_{ON}	—	25	50	μs	Note 2 , V_{IN} switched from 0V to 5V; measure time for V_{GATE} to reach 20V
Gate Turn-Off Time	t_{OFF}	—	4	10		V_{IN} switched from 5V to 0V; measure time for V_{GATE} to reach 1V

- Note 1:** Minimum and maximum Electrical Characteristics are 100% tested at $T_A = +25^{\circ}\text{C}$ and $T_A = +85^{\circ}\text{C}$, and 100% ensured over the entire range. Typical values are characterized at $+25^{\circ}\text{C}$ and represent the most likely parametric norm.
- 2:** Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster—see Applications Information. Maximum value of switching speed seen at $+125^{\circ}\text{C}$, units operated at room temperature will reflect the typical values shown.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	-65	—	+150	$^{\circ}\text{C}$	—
Lead Temperature	T_{LEAD}	—	—	+260	$^{\circ}\text{C}$	Soldering, 10 sec.
Maximum Junction Temperature	$T_{\text{J(MAX)}}$	—	—	+150	$^{\circ}\text{C}$	—
Junction Temperature Range	T_J	-40	—	+85	$^{\circ}\text{C}$	—
Package Thermal Resistances						
Thermal Resistance, SOIC 8-Ld	θ_{JA}	—	170	—	$^{\circ}\text{C/W}$	—
Thermal Resistance, PDIP 8-Ld	θ_{JA}	—	100	—	$^{\circ}\text{C/W}$	—

Test Circuit



2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

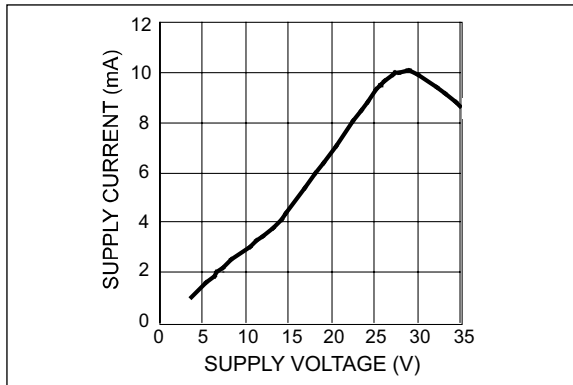


FIGURE 2-1: Supply Current vs. Supply Voltage.

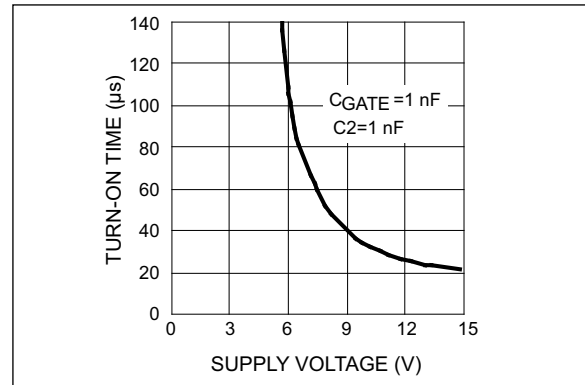


FIGURE 2-4: High-Side Turn-On Time*.

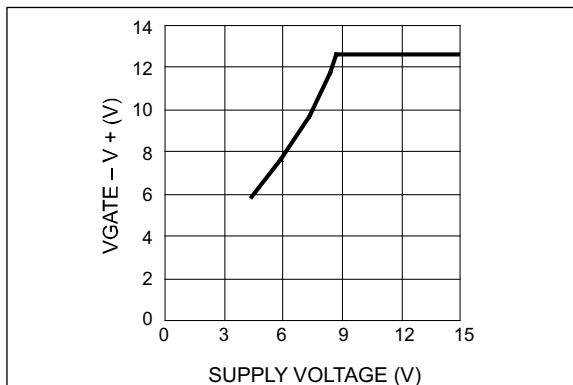


FIGURE 2-2: DC Gate Voltage Above Supply.

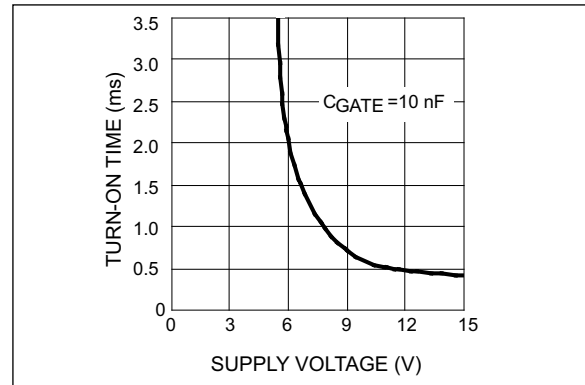


FIGURE 2-5: High-Side Turn-On Time*.

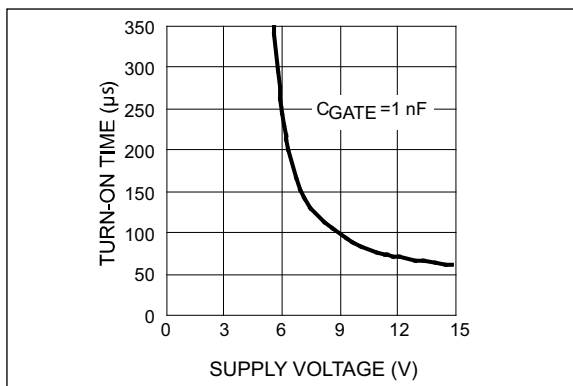


FIGURE 2-3: High-Side Turn-On Time*.

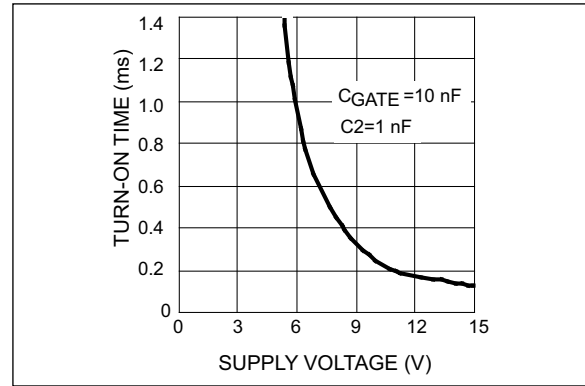


FIGURE 2-6: High-Side Turn-On Time*.

* Time for gate to reach $V^+ + 5V$ in Test Circuit with $V_S = V^+ - 5V$.

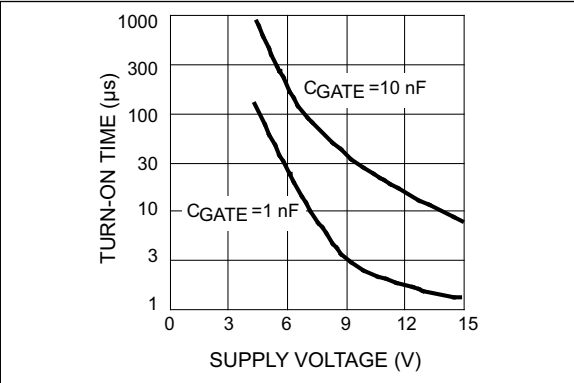


FIGURE 2-7: Low-Side Turn-On Time for Gate = 5V.

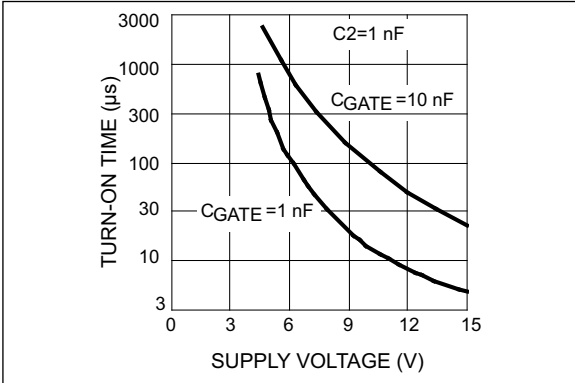


FIGURE 2-10: Low-Side Turn-On Time for Gate = 10V.

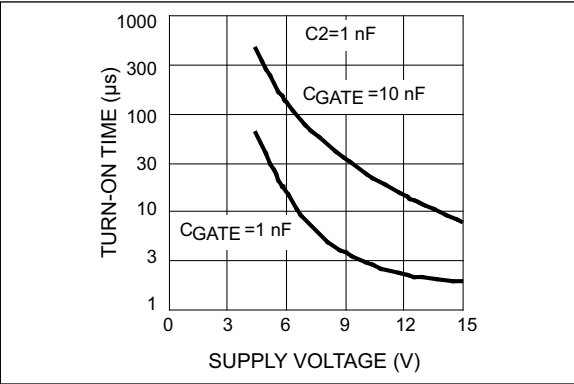


FIGURE 2-8: Low-Side Turn-On Time for Gate = 5V.

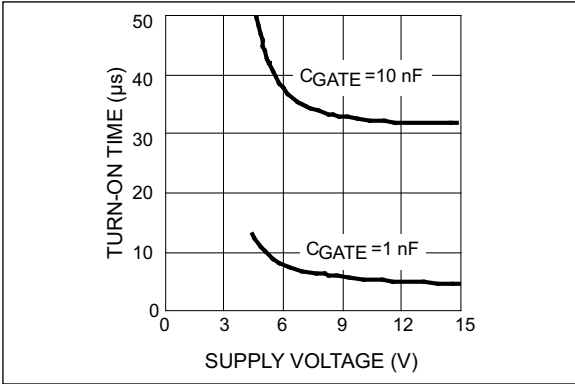


FIGURE 2-11: Turn-Off Time.

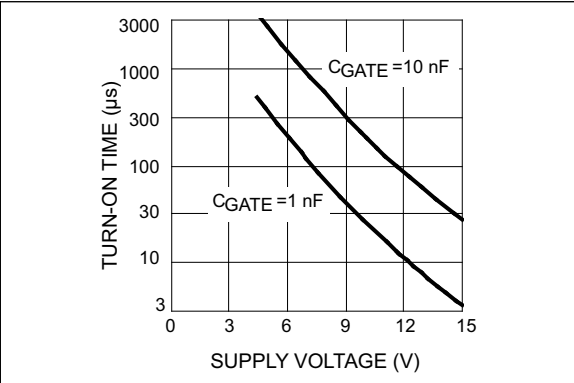


FIGURE 2-9: Low-Side Turn-On Time for Gate = 10V.

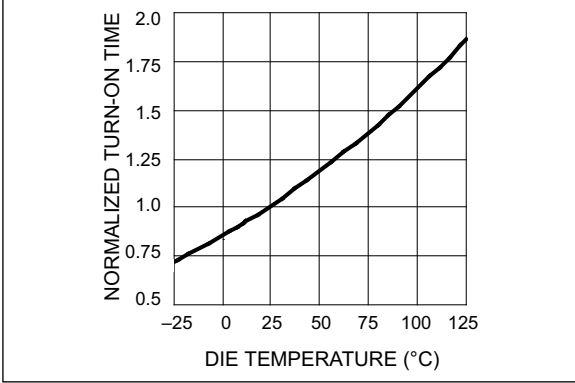


FIGURE 2-12: Turn-On Time.

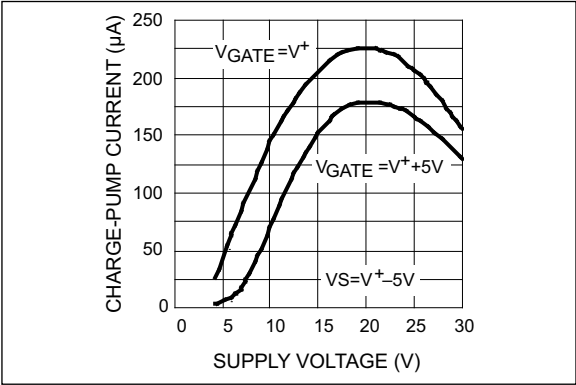


FIGURE 2-13: Charge Pump Output Current.

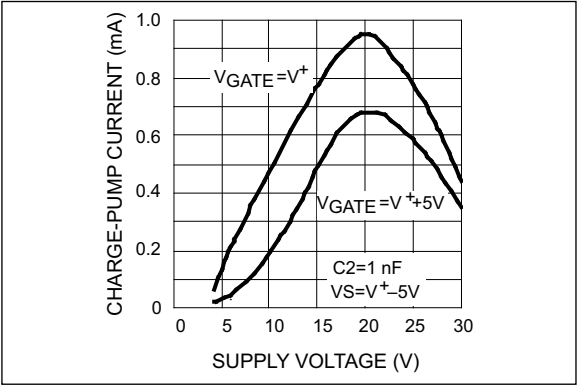


FIGURE 2-14: Charge Pump Output Current.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	V+	Supply. Must be decoupled to isolate from large transients caused by the power FET drain. 10 μ F is recommended close to Pins 1 and 4.
2	INPUT	Turns on power MOSFET when taken above threshold (3.5V typical). Requires <1 μ A to switch.
3	SOURCE	Connects to source lead of power FET and is the return for the gate clamp zener. Can safely swing to –10V when turning off inductive loads.
4	GROUND	Ground.
5	GATE	Drives and clamps the gate of the power FET. Will be clamped to approximately –0.7V by an internal diode when turning off inductive loads.
6, 7, 8	C2, COM, C1	Optional 1 nF capacitors reduce gate turn-on time; C2 has dominant effect.

4.0 APPLICATION INFORMATION

4.1 Functional Description

Refer to the [Functional Block Diagram](#). The MIC5011 functions are controlled via a logic block connected to the Input (Pin 2). When the input is low, all functions are turned off for low standby current and the gate of the power MOSFET is also held low through 500Ω to an N-channel switch. When the input is taken above the turn-on threshold (3.5V typical), the N-channel switch turns off and the charge pump is turned on to charge the gate of the power FET.

The charge pump incorporates a 100 kHz oscillator and on-chip pump capacitors capable of charging 1 nF to 5V above supply in 60 μs typical. With the addition of 1 nF capacitors at C1 and C2, the turn-on time is reduced to 25 μs typical (see [Figure 4-1](#)). The charge pump is capable of pumping the gate up to over twice the supply voltage. For this reason, a zener clamp (12.5V typical) is provided between the Gate (Pin 5) and Source (Pin 3) to prevent exceeding the V_{GS} rating of the MOSFET at high supplies.

4.2 Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal, low current lab practices. The following are the sources of pitfalls most often encountered during prototyping.

Supplies: Many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation, will produce strange results when used with a supply that has poor ripple rejection or a peaked transient response. Always monitor the power supply voltage that appears at the drain of a high-side driver (or the supply side of the load in a low-side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1 kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to over-stress various components—especially electrolytic capacitors—with possibly catastrophic results. A 10 μF supply bypass capacitor at the chip is recommended.

Residual Resistances: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50 mΩ power MOSFET for low drop, but careless construction techniques could easily add 50 mΩ to 100 mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high-current drain connections to the tab. Wiring losses have a profound effect on high-current circuits. A floating millivoltmeter can identify connections that are contributing excess drop under load.

4.3 Circuit Topologies

The MIC5011 is suited for use with standard MOSFETs in high- or low-side driver applications. In addition, the MIC5011 works well in applications where, for faster switching times, the supply is bootstrapped from the MOSFET source output. Low voltage, high-side drivers (such as shown in the [Typical Application Circuits](#)) are the slowest; their speed is reflected in the gate turn-on time specifications. The fastest drivers are the low-side and bootstrapped high-side types ([Typical Application Circuits](#) and [Figure 4-2](#)). Load current switching times are often much faster than the time to full gate enhancement, depending on the circuit type, the MOSFET, and the load. Turn-off times are essentially the same for all circuits (less than 10 μs to $V_{GS} = 1V$). The choice of one topology over another is based on a combination of considerations including speed, voltage, and desired system characteristics.

High-Side Driver ([Typical Application Circuits](#), left). The high-side topology works well down to $V^+ = 7V$ with standard MOSFETs. From 4.75V to 7V supply, a logic-level MOSFET can be substituted because the MIC5011 will not reach 10V gate enhancement (10V is the maximum rating for logic-compatible MOSFETs).

High-side drivers implemented with MIC501x drivers are self-protected against inductive switching transients. During turn-off, an inductive load will force the MOSFET source 5V or more below ground, while the MIC5011 holds the gate at ground potential. The MOSFET is forced into conduction and it dissipates the energy stored in the load inductance. The MIC5011 Source pin (Pin 3) is designed to withstand this negative excursion without damage. External clamp diodes are unnecessary.

Low-Side Driver ([Typical Application Circuits](#), right). A key advantage of the low-side topology is that the load supply is limited only by the MOSFET BVDSS rating. Clamping may be required to protect the MOSFET drain terminal from inductive switching transients. The MIC5011 supply should be limited to 15V in low-side topologies, otherwise a large current will be forced through the gate clamp zener.

Low-side drivers constructed with the MIC501x family are also fast; the MOSFET gate is driven to near supply immediately when commanded ON. Typical circuits achieve 10V enhancement in 10 μs or less on a 12V to 15V supply.

Modifying Switching Times ([Figure 4-1](#)). High-side switching times can be improved by a factor of 2 or more by adding external charge pump capacitors of 1 nF each. In cost-sensitive applications, omit C1 (C2 has a dominant effect on speed).

MIC5011

Do not add external capacitors to the MOSFET gate. Add a resistor (1 k Ω to 51 k Ω) in series with the gate to slow down the switching time.

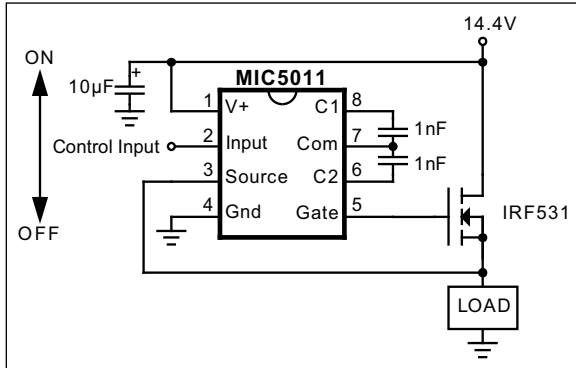


FIGURE 4-1: High-Side Driver with External Charge Pump Capacitors.

Bootstrapped High-Side Driver (Figure 4-2). The speed of a high-side driver can be increased to better than 10 μ s by bootstrapping the supply off of the MOSFET source. This topology can be used where the load is pulse-width modulated (100 Hz to 20 kHz) or where it is energized continuously. The Schottky barrier diode prevents the MIC5011 supply pin from dropping more than 200 mV below the drain supply and it also improves turn-on time on supplies of less than 10V. Because the supply current in the “off” state is only a small leakage, the 100 nF bypass capacitor tends to remain charged for several seconds after the MIC5011 is turned off. In a PWM application the chip supply is sustained at a higher potential than the system supply, which improves switching time.

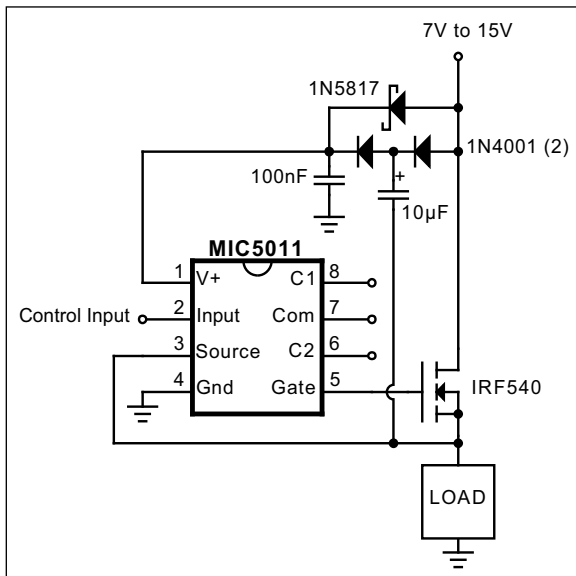


FIGURE 4-2: Bootstrapped High-Side Driver.

Opto-Isolated Interface (Figure 4-3). Although the MIC5011 has no special input slew rate requirement, the lethargic transitions provided by an opto-isolator may cause oscillations on the rise and fall of the output. The circuit shown accelerates the input transitions from a 4N35 opto-isolator by adding hysteresis. Opto-isolators are used where the control circuitry cannot share a common ground with the MIC5011 and high-current power supply, or where the control circuitry is located remotely. This implementation is intrinsically safe; if the control line is severed the MIC5011 will turn OFF.

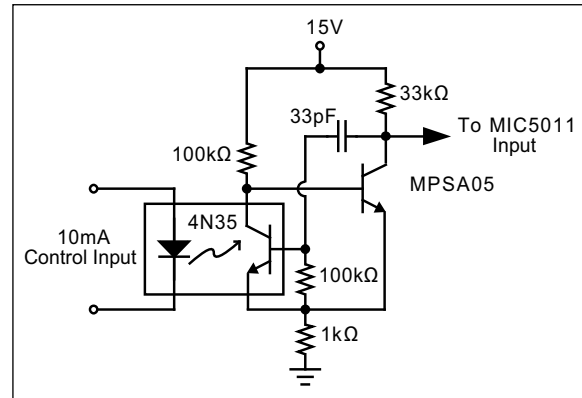


FIGURE 4-3: Improved Opto-Isolator Performance.

Industrial Switch (Figure 4-4). The most common manual control for industrial loads is a push button on/off switch. The “on” button is physically arranged in a recess so that in a panic situation the “off” button, which extends out from the control box, is more easily pressed. This circuit is compatible with control boxes such as the CR2943 series (GE). The circuit is configured so that if both switches close simultaneously, the “off” button has precedence.

This application also illustrates how two (or more) MOSFETs can be paralleled. This reduces the switch drop, and distributes the switch dissipation into multiple packages.

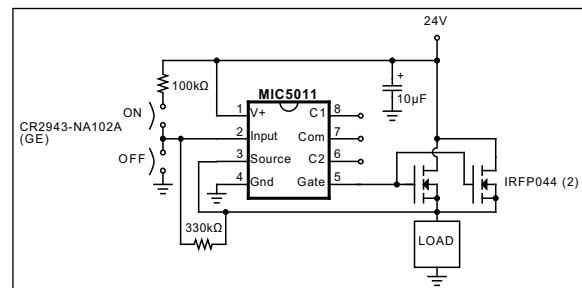


FIGURE 4-4: 50A Industrial Switch.

FIGURE 4-7: 30A Time-Delay Relay.

MIC5011

Motor Driver with Stall Shutdown (Figure 4-8).

Tachometer feedback can be used to shut down a motor driver circuit when a stall condition occurs. The control switch is a 3-way type; the "START" position is momentary and forces the driver ON. When released, the switch returns to the "RUN" position, and the tachometer's output is used to hold the MIC5011 input ON. If the motor slows down, the tachometer output is reduced, and the MIC5011 switches OFF. Resistor "R" sets the shutdown threshold.

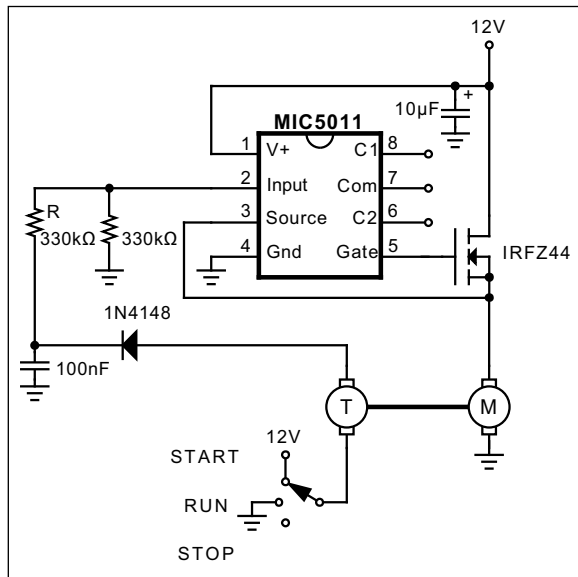


FIGURE 4-8: Motor Stall Shutdown.

Electronic Governor (Figure 4-9). The output of an AC tachometer can be used to form a PWM loop to maintain the speed of a motor. The tachometer output is rectified, partially filtered, and fed back to the input of the MIC5011. When the motor is stalled, there is no tachometer output and the MIC5011 input is pulled high, delivering full power to the motor. If the motor spins fast enough, the tachometer output is sufficient to pull the MIC5011 input low, shutting the output off. Because the rectified waveform is only partially filtered, the input oscillates around its threshold causing the MIC5011 to switch on and off at the frequency of the tachometer signal. A PWM action results because the average DC voltage at the input decreases as the motor spins faster. The 1 kΩ potentiometer is used to set the running speed of the motor. Loop gain (and speed regulation) is increased by increasing the value of the 100 nF filter capacitor.

The performance of such a loop is imprecise, but stable and inexpensive. A more elaborate loop would consist of a PWM controller and a half-bridge.

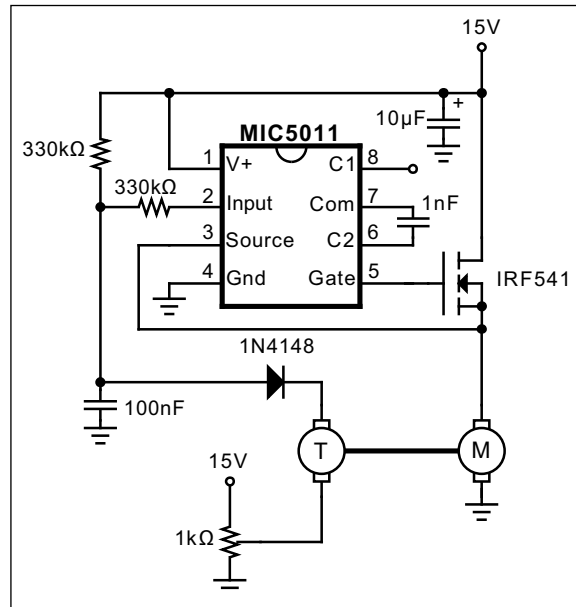


FIGURE 4-9: Electronic Governor.

Gate Control Circuit (Figure 4-10). When applying the MIC5011, it is helpful to understand the operation of the gate control circuitry. The gate circuitry can be divided into two sections: 1) charge pump (oscillator, Q1-Q5, and the capacitors) and 2) gate turn-off switch (Q6).

When the MIC5011 is in the OFF state, the oscillator is turned off, thereby disabling the charge pump. Q5 is also turned off, and Q6 is turned on. Q6 holds the gate pin (G) at ground potential which effectively turns the external MOSFET off.

Q6 is turned off when the MIC5011 is commanded on, and Q5 pulls the gate up to supply (through 2 diodes). Next, the charge pump begins supplying current to the gate. The gate accepts charge until the gate-source voltage reaches 12.5V and is clamped by the zener diode.

A 2-output, three-phase clock switches Q1-Q4, providing a quasi-tripling action. During the initial phase Q4 and Q2 are ON. C1 is discharged, and C2 is charged to supply through Q5. For the second phase Q4 turns off and Q3 turns on, pushing pin C2 above supply (charge is dumped into the gate). Q3 also charges C1. On the third phase Q2 turns off and Q1 turns on, pushing the common point of the two capacitors above supply. Some of the charge in C1 makes its way to the gate. The sequence is repeated by turning Q2 and Q4 back on, and Q1 and Q3 off.

In a low-side application operating on a 12V to 15V supply, the MOSFET is fully enhanced by the action of Q5 alone. On supplies of more than approximately 14V, current flows directly from Q5 through the zener diode to ground. To prevent excessive current flow, the MIC5011 supply should be limited to 15V in low-side applications.

The action of Q5 makes the MIC5011 operate quickly in low-side applications. In high-side applications Q5 pre-charges the MOSFET gate to supply, leaving the charge pump to carry the gate up to full enhancement 10V above supply. Bootstrapped high-side drivers are as fast as low-side drivers because the chip supply is boosted well above the drain at turn-on.

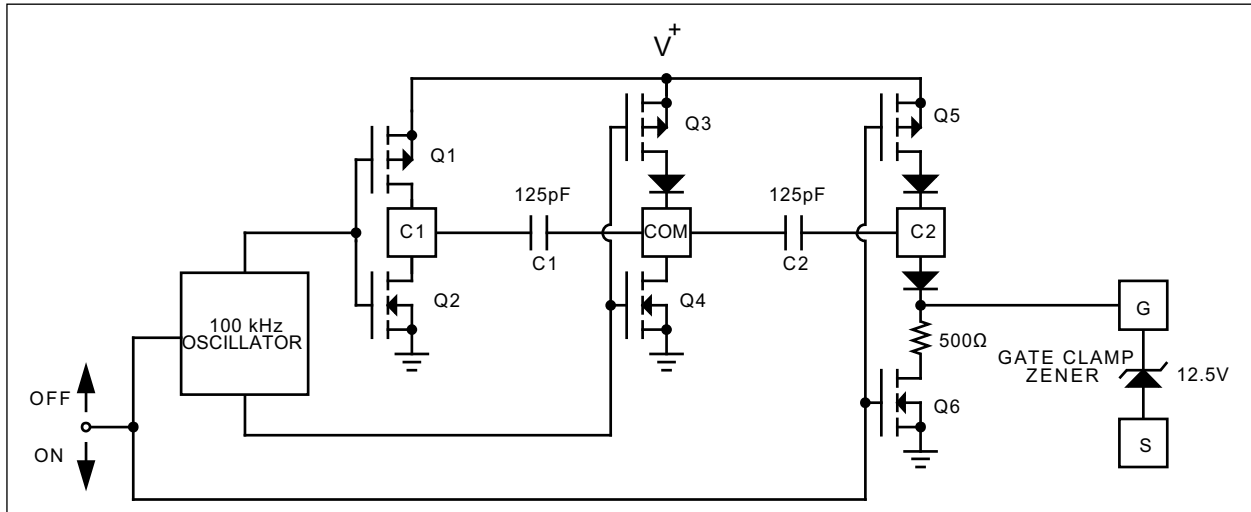


FIGURE 4-10: Gate Control Circuit Detail.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

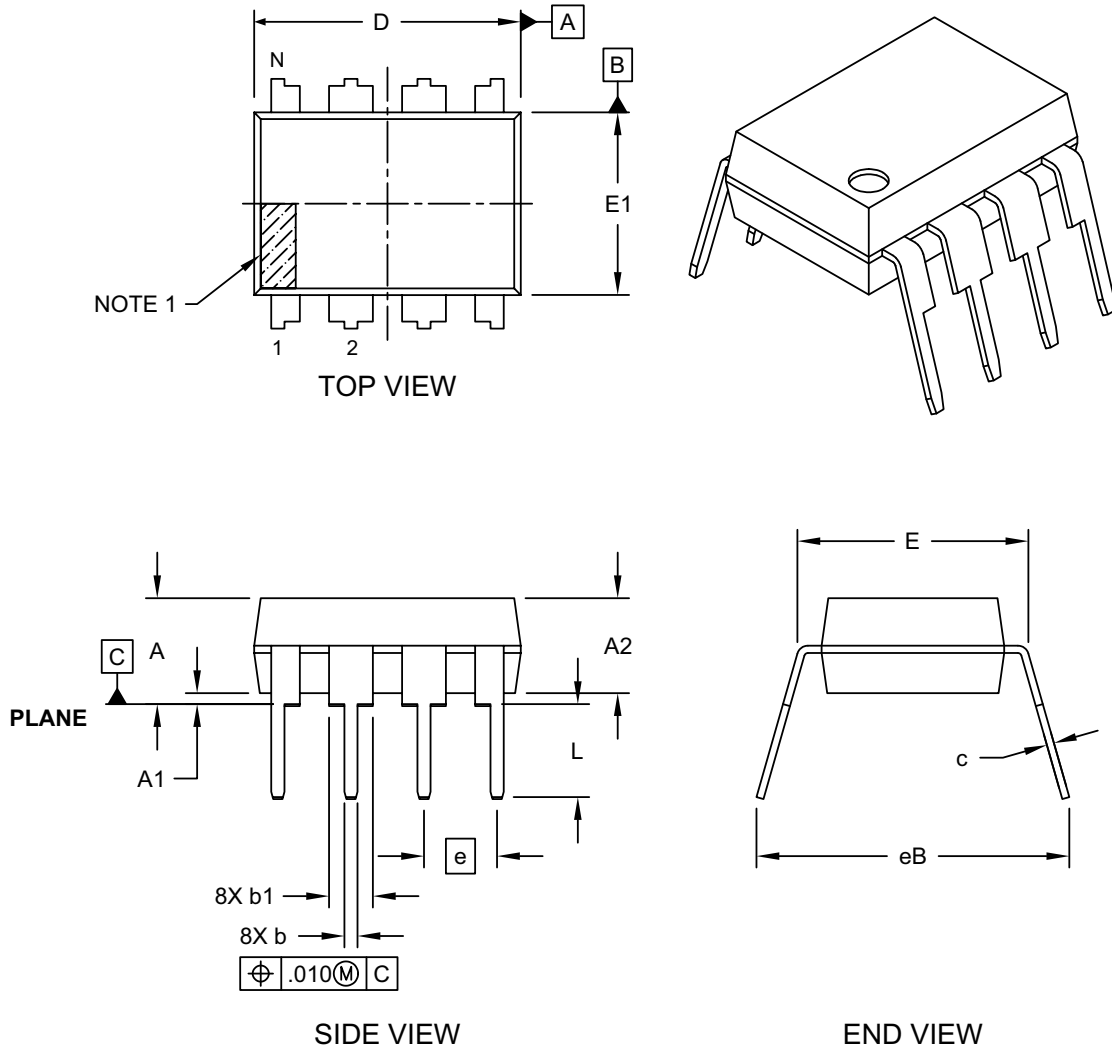
8-Lead SOIC*	Example
	
8-Lead PDIP*	Example
	

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

8-Lead Plastic Dual In-Line (C4X) - 300 mil Body [PDIP] Atmel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

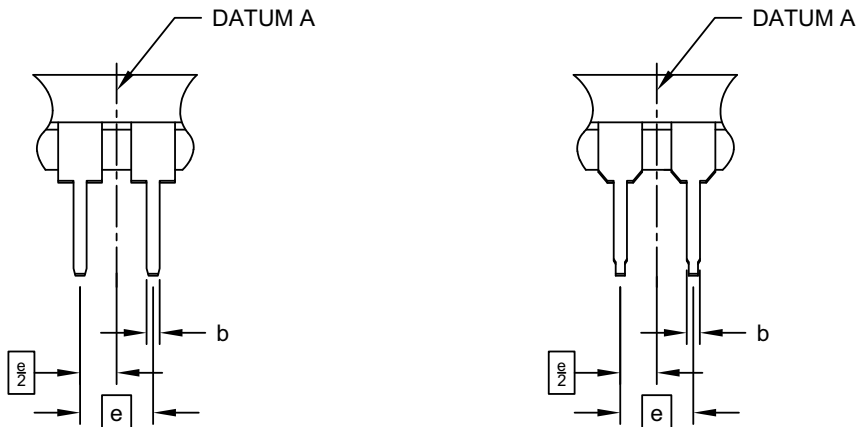


Microchip Technology Drawing No. C04-018-C4X Rev G Sheet 1 of 2

8-Lead Plastic Dual In-Line (C4X) - 300 mil Body [PDIP] Atmel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

ALTERNATE LEAD DESIGN (NOTE 5)



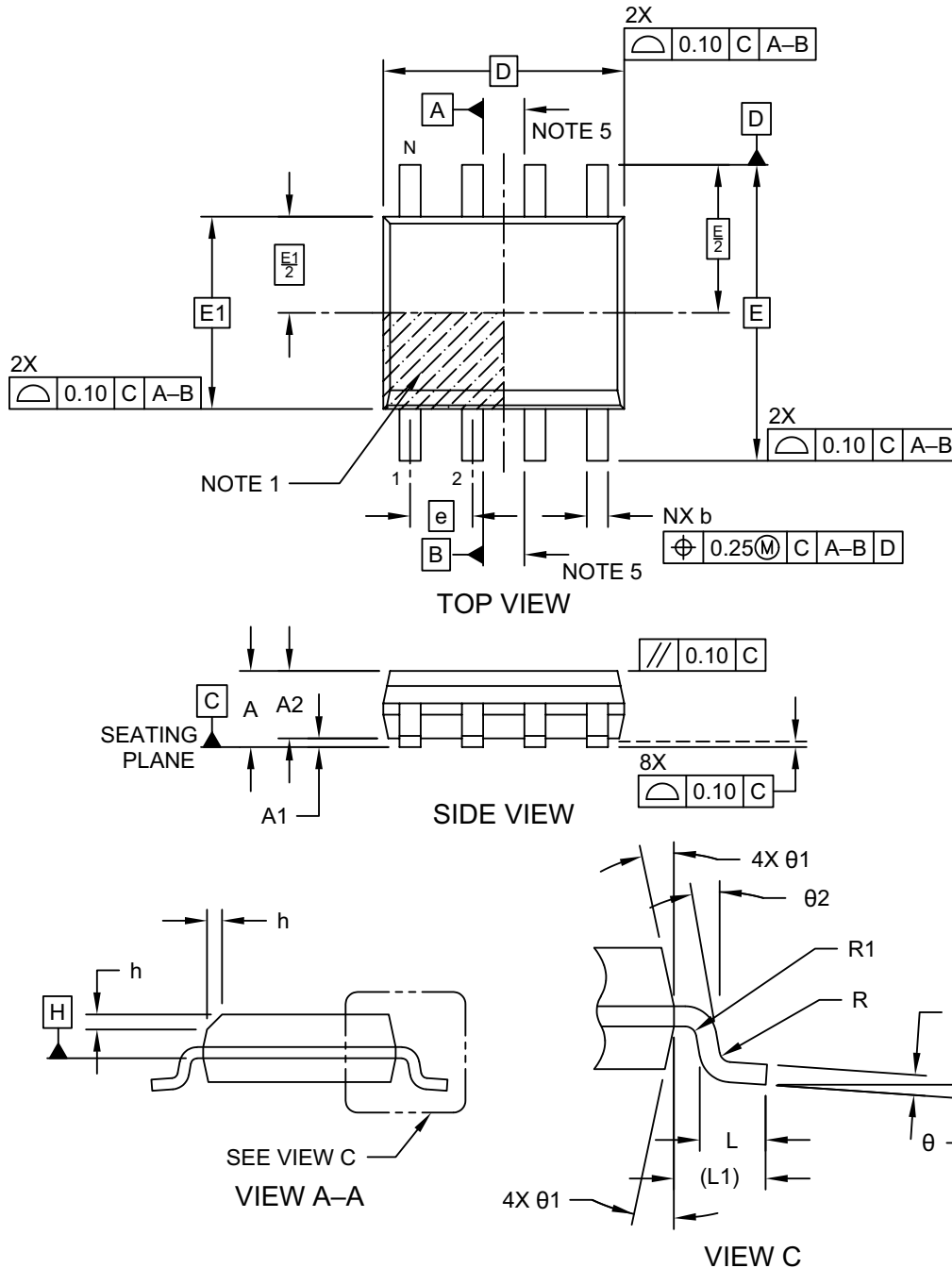
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing	§	eB	-	.430

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- Lead design above seating plane may vary, based on assembly vendor.

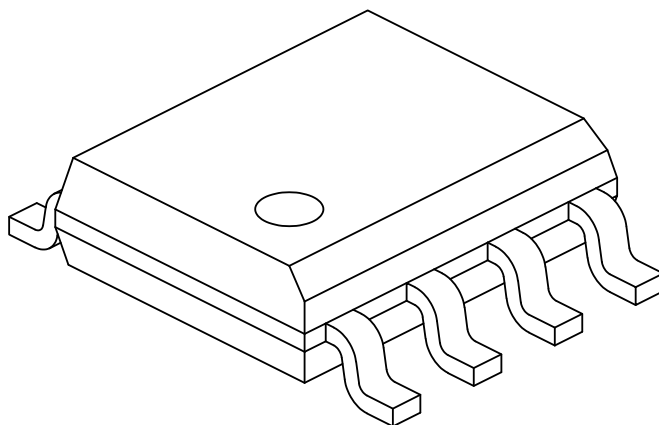
Microchip Technology Drawing No. C04-018-C4X Rev G Sheet 2 of 2

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	—	—	1.75
Molded Package Thickness	A2	1.25	—	—
Standoff §	A1	0.10	—	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	—	0.50
Foot Length	L	0.40	—	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	—	0.25
Lead Width	b	0.31	—	0.51
Lead Bend Radius	R	0.07	—	—
Lead Bend Radius	R1	0.07	—	—
Foot Angle	θ	0°	—	8°
Mold Draft Angle	θ1	5°	—	15°
Lead Angle	θ2	0°	—	—

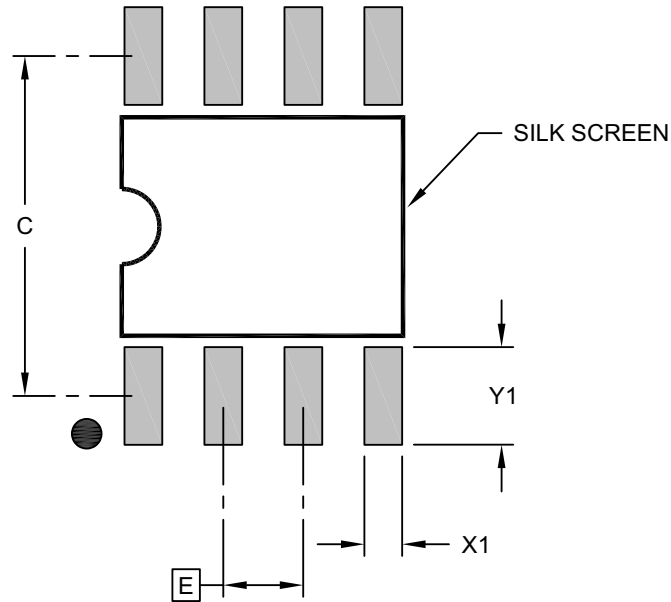
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-3BX Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-3BX Rev K

MIC5011

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (August 2024)

- Converted Micrel document MIC5011 to Microchip data sheet DS20006820A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part Number		X	X	[-XX]
Device		Temperature Range		Package
				Media Type
Device:	MIC5011:	Minimum Parts High-Side or Low-Side MOSFET Driver		
Temperature Range:	Y	=	-40°C to +85°C	
Package:	M	=	8-Lead SOIC	
	N	=	8-Lead PDIP	
Media Type:	<blank>	=	50/Tube (PDIP option)	
	<blank>	=	95/Tube (SOIC option)	
	TR	=	2,500/Reel (SOIC option only)	

Examples:

a) MIC5011YM: MIC5011, -40°C to +85°C Temp. Range, 8-Lead SOIC, 95/Tube

b) MIC5011YM-TR: MIC5011, -40°C to +85°C Temp. Range, 8-Lead SOIC, 2,500/Reel

c) MIC5011YN: MIC5011, -40°C to +85°C Temp. Range, 8-Lead PDIP, 50/Tube

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

MIC5011

NOTES:

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