AN-56

Application Note

High-Speed Design Guidelines

May 2003

Microsemi

a Microchip company

Contents

1 Revision History 1.0 1
1.1 Revision 1.0 1
2 Introduction 2
3 Power Supply Considerations 3
4 PCB LAYOUT 5
4.1 General Guidelines for Layout 5
4.2 Determining Trace Width 5
4.3 Routing Considerations 6
4.4 Additional Routing Notes 7

1 Revision History 1.0

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first release of this document. It was published in May 2003.

2 Introduction

This application note is intended to assist customers with termination and interface techniques, PCB layout (bypass capacitors and routing considerations), and power supply considerations when designing a PCB for use with high-speed (GHz range) signals.

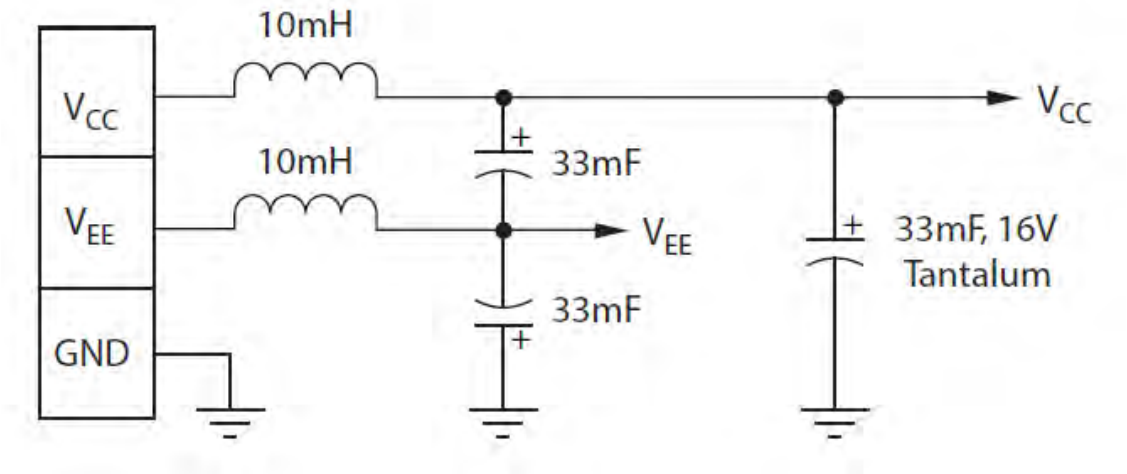
This document should be used in conjunction with the latest data sheets for specific Microchip products being used. Contact your local Microchip sales representative for application-related questions.

3 Power Supply Considerations

Many Microchip ICs operate on V_{CC} = 3.3 V and/or 2.5 V (±5%), and V_{EE} = 0 V. (Many Microchip products do not have V_{EE} and GND/V_{CC} separated; consult the data sheet of the specific product more information.) Decoupling the V_{CC} and V_{EE} power supply pins is critical in maintaining the proper operation of these devices. There are two steps involved in bypassing power supplies. Step one involves low-frequency decoupling at the power terminal where power enters the board. Use large tantalum low-inductance SMT capacitors ranging from 10 µF to 47 µF to handle low-frequency noise. These capacitors should be placed as close as possible to the supply source. Connect these capacitors to V_{CC} and V_{EE} through a 1.0 H to 10 H inductor or ferrite bead as shown in the following figure.

Note: These recommendations are general. Ideal capacitor and inductor values should be determined based on the overall power supply noise profile in your system.

Figure 1 • Bypassing Low-Frequency Power Terminal Block



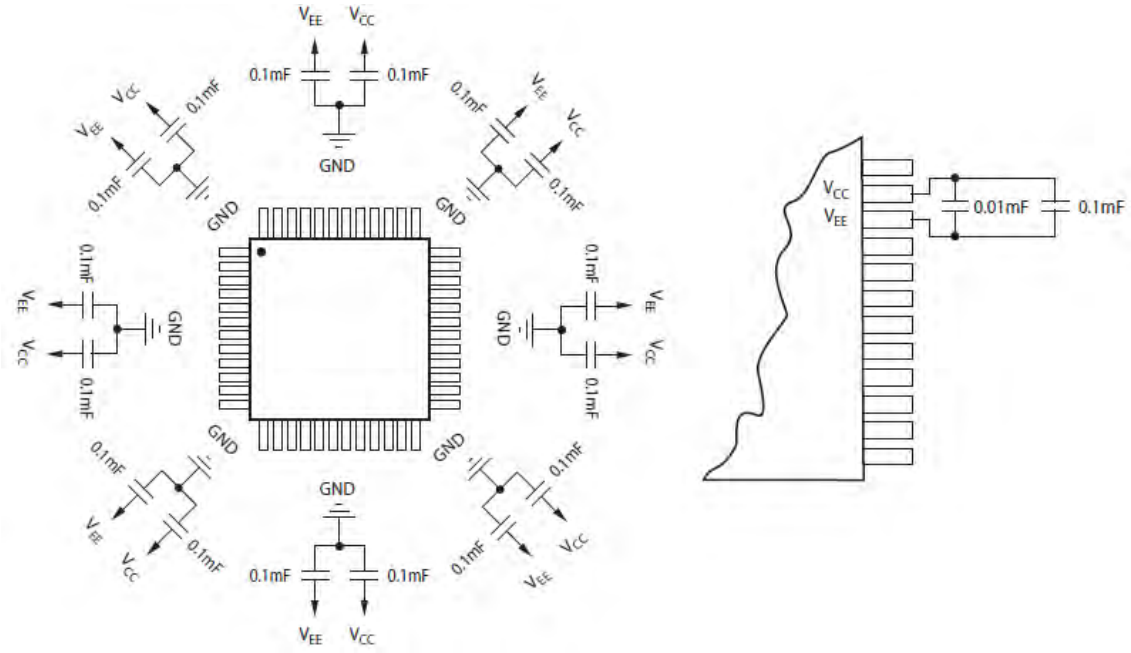
Step two involves high-frequency decoupling using 0.1 µF and 0.01 µF capacitors from the V_{CC} to V_{EE} pins, placed in parallel, or stacked on top of each other, as close as possible to the IC. (To save board space, many Vitesse products only require a 0.1 µF capacitor; consult the data sheet of the specific product for more information.) It is recommended to have separate and continuous V_{CC} and V_{EE} planes. Use 0.1 F and 0.01 F capacitor stacks arrayed around and beneath the IC to bypass any noise and facilitate an effective return current path. See the following figure.

Notes:

If one plane is used for GND and VEE in your application, your bypass array would not include a capacitor between GND and V_{EE}.

Inclusion of 0.01 µF capacitors is considered optional. Limited available board area in some applications may preclude their use.

Figure 2 • High-Frequency Bypass Array



4 PCB LAYOUT

This section discusses general guidelines for layout, covering trace width calculations, bypass capacitor locations, and routing considerations.

When implementing a high-speed system, the importance of good PCB layout cannot be ignored. Careful placement of components on the top and bottom sides of the board will ensure optimal signal integrity.

4.1 General Guidelines for Layout

Use a multi-layer board (six or more layers) and have separate V_{CC}, V_{EE} (and possibly, GND) planes. Use the highest quality dielectric allowable. Teflon® and FR4 are the two common PCB materials used in high-speed applications.

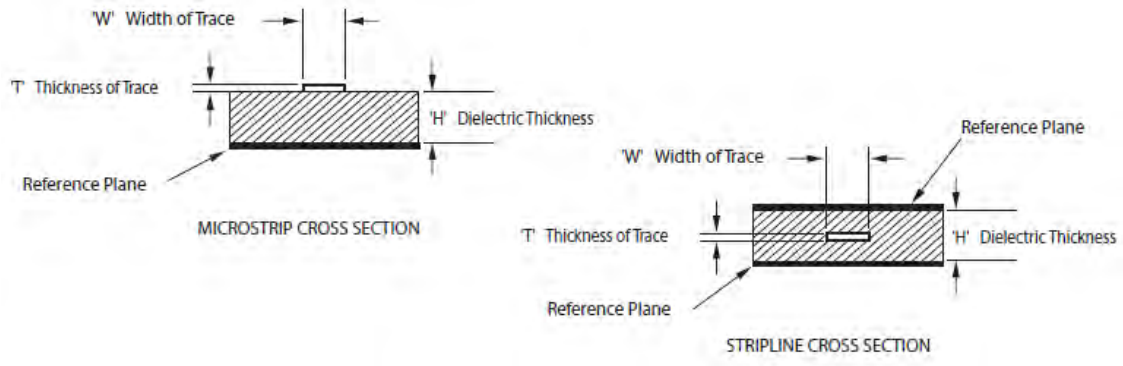
Following is the list of comparisons:

- FR4 is less expensive by a factor of 2 to 1 or 7 to 1, depending on the Teflon material (7 to 1 for Arlon, 2 to 1 for Rogers).
- Most board houses stock FR4, however, standard Teflon materials typically have a 2 to 4 week lead-time.
- FR4 comes in a greater variety of ground plane thicknesses, providing greater design flexibility to the board designer to achieve that elusive 50 Ω line impedance.
- Teflon is lower in loss and attenuation, which provides better electrical performance.
- Teflon electrical and mechanical properties are more stable over temperature.

4.2 Determining Trace Width

Careful consideration should be given for determining the trace width for the PCB transmission lines. For 40 to 50 microstrip transmission lines, a good rule of thumb is to use W/H = 2, where “W” is the width of trace and “H” is the thickness of dielectric. Stripline characteristic impedance is 0.6 times that of a microstrip line. There are several impedance calculators available on the Internet (free or for purchase). It is recommended one be used prior to board fabrication to ensure proper impedance is achieved. See the following figure.

Figure 3 • Transmission Line Cross-Section

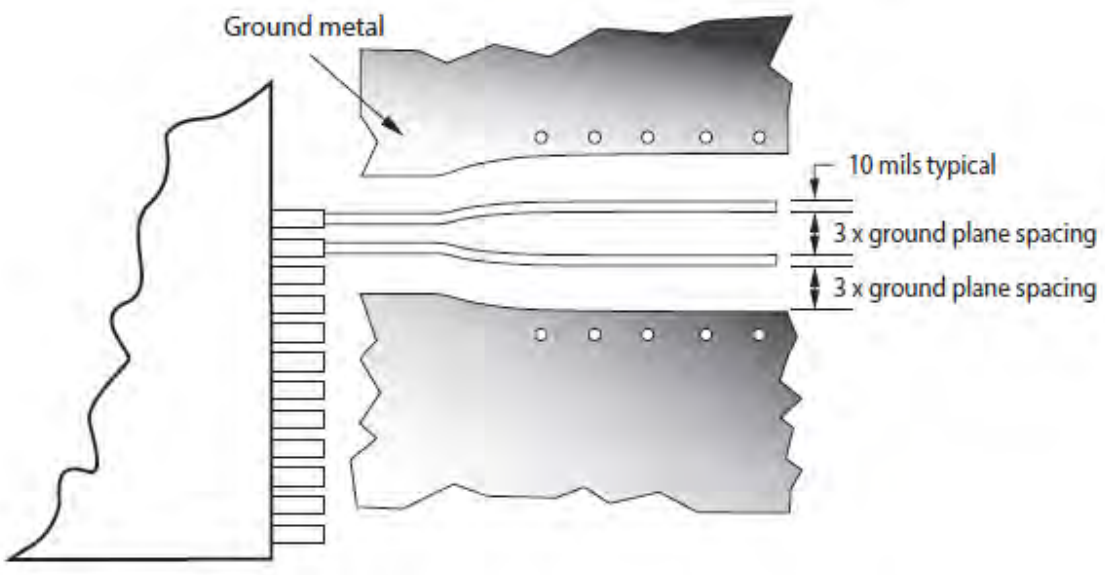


4.3 Routing Considerations

There are generally three different signal types on a PCB: low-speed/high-speed clock and data signals, control signals, and power lines/planes. Power should be connected to the ICs through vias from power planes rather than routed to pins using traces. Signals used to control various TTL functions on the chip should be kept isolated from high-speed data or clock lines with 5 mil to 10 mil wide spacing between them. Other than ensuring that control lines are isolated, they can typically be routed without special concerns for signal integrity.

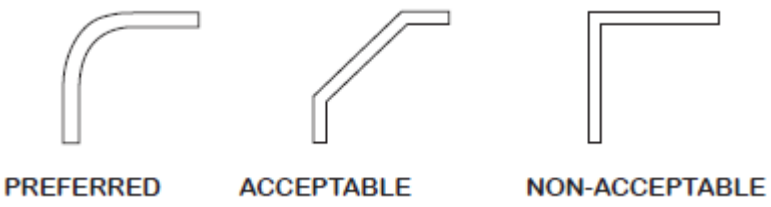
High-speed data and clock lines are more critical and do require special routing considerations. Use 3- to 4-ground plane spacing ('H' in Figure 3) between lines. Surround traces with GND metal (use multiple vias) to isolate signal lines and reduce any crosstalk.

Figure 4 • High-Speed Signal Layout



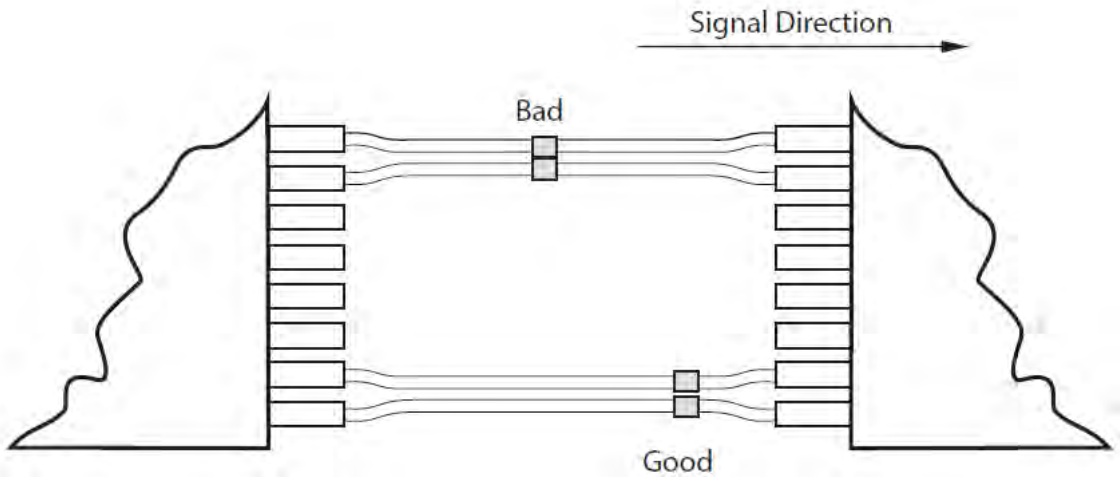
Use gradual rounded corners to avoid sharp corners. Sharp corners will cause changes in impedance and signal reflections. Smooth curves should be used for the best signal integrity effects. See the following figure.

Figure 5 • Corner Signal Routing



Do not use vias on high-speed lines to minimize impedance mismatches. Keep high-speed data lines as short as possible. Avoid routing high-speed signals under any capacitors, resistors or other ICs. Place termination or biasing components as close to the destination IC as possible, see the following figure.

Figure 6 • Location of Termination and Bias Components



4.4 Additional Routing Notes

- Care must be taken to match high-speed tracks to the same length and to follow the same path. A small mismatch in length can lead to delays between signal pairs.
- If high-speed signal traces run on the PCB surface layer, try to position a ground plane directly under these traces, and ensure that the ground plane is continuous. If a signal path crosses the edge of a plane, it will cause impedance discontinuities.
- Keep high-speed signal traces spaced well away from other traces. Separation should be greater than 5 trace widths between traces that are not of the same pair.
- Again, avoid the use of any vias in high-speed traces, as they create impedance discontinuities that lead to delays and mismatches between signal pairs. If vias in high-speed trace paths are unavoidable, then the surrounding area of the via should be cleared out on every layer of the PCB. In some cases, it may be necessary to back drill the via stubs to further reduce any impedance discontinuity.
- Specify the impedance of each trace as 50? or 75? (±10%) to ground. Also, specify an impedance relative to the other path of a differential pair as 100? or 150?, respectively. Be sure to get coupons from your board vendor so that you can verify the impedance. Loosely coupling traces is recommended to allow easier length matching.
- Avoid using lengths of 1/4th the wavelength, or multiples thereof, between impedance discontinuities.
- Connections should be point-to-point (one driver should not be routed to multiple destinations).

If there are any external bias components required, such as a bias resistor, removing the ground plane(s) from underneath the bias component can eliminate noise induction into the component. Keep the component PCB pads to their minimum size to avoid impedance discontinuities. If required, components of size 0603 or smaller should be used to minimize the impedance discontinuity impact of using the component. Locate any required termination or biasing components as close to the source or load IC as possible.

Any stub lengths on high-speed traces should be less than the result of Equation 1 to prevent negative effects of the stub on the propagation of the signal down the high-speed traces:

Max stub length = (1/6) • (t_R/D)

(EQ 1)

where,

t_R = signal rise time (ps)

D = media propagation delay (ps/in)

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

© 2003 Microsemi. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www microsemi.com.

G53065