

DC–24 GHz 0.5W GaAs Self–Biased Distributed MMIC Power Amplifier

MMA052PP45



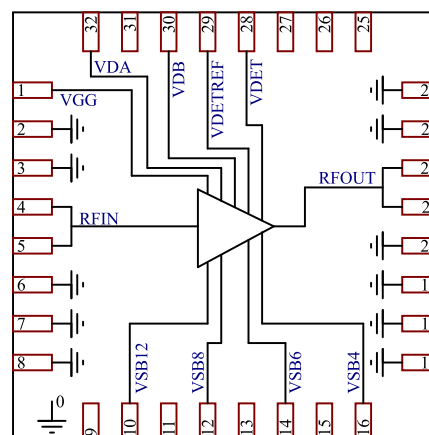
Product Overview

The MMA052PP45 is a Gallium Arsenide (GaAs) Monolithic Microwave Integrated Circuit (MMIC) Pseudomorphic High-Electron-Mobility Transistor (pHEMT) distributed self-biased amplifier. It is packaged in a 4.5 mm plastic surface-mount QFN package. The amplifier operates between DC and 24 GHz, and is ideal for transmit or receive applications in wideband military and space applications, as well as test and measurement. The amplifier is easily biased using a single positive supply, and it offers 14 dB of gain with positive gain slope, 3.5 dB noise figure, an output IP3 of 35 dBm, and 28 dBm of P3dB compressed output power. The RF I/Os are internally matched to 50Ω.

Key Features

- Broadband performance: DC to 24 GHz
- P_{sat} : 28 dBm
- Gain: 14 dB with positive gain slope
- High IP3: 35 dBm
- Single positive supply: 9V at 310 mA
- 50Ω matched I/O
- 4.5 mm × 4.5 mm, 32L plastic QFN passivated space-qualified process listed on EPPL007-38

Amplifier Functional Diagram



Applications

- Test and measurement instrumentation
- Military and space
- Wideband microwave radios
- Microwave and millimeter-wave communication systems
- A&D, Satcom, transmit and receive

Performance Overview

Parameter	Typ.	Units
Frequency range	DC – 24	GHz
P_{sat}	28	dBm
Gain	14	dB
IM3 at 20 dBm	–33	dBc
Current at +9V Supply	310	mA

Export Classification: EAR99

Performance Curves

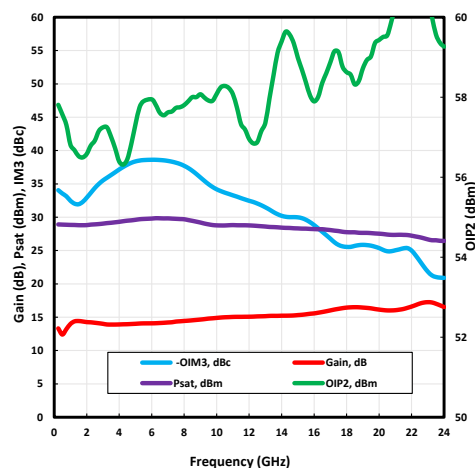


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1. Electrical Specifications

1.1 Typical Electrical Performance

Table 1-1. Typical Electrical Performance at 25 °C, $V_{DD} = 9V$, $I_{DD} = 310$ mA (Unless otherwise mentioned)

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		DC		24	GHz
Gain	DC–6 GHz	12	14		dB
	6 GHz–12 GHz	13	14.5		dB
	12 GHz–24 GHz	14	15.5		dB
Gain flatness	4 GHz–12 GHz		± 1		dB
	12 GHz–24 GHz		± 0.7		dB
Noise Figure	2 GHz–6 GHz		5		dB
	6 GHz–12 GHz		3.5		
	12 GHz–24 GHz		4.5		
Input Return Loss	DC – 6 GHz		15		dB
	6 GHz–12 GHz		15		
	12 GHz–24 GHz		12		
Output Return Loss	DC – 6 GHz		14		dB
	6 GHz–12 GHz		14		
	12 GHz–24 GHz		12		
P1dB	DC–6 GHz	25	27		dBm
	6–12 GHz	25	27		
	12 GHz–20 GHz	24.5	26		
	20 GHz–24 GHz	24	25.5		
P_{sat} (Measured at 3 dB Gain Compression)	DC–6 GHz		29		dBm
	6–12 GHz		28		
	12 GHz–20 GHz		27.5		
	20 GHz–24 GHz		27		
OIP3	DC–6 GHz		36		dBm
	6–12 GHz		35		
	12 GHz–24 GHz		32		
IM3 @ 20 dBm	DC–6 GHz		-35		dBc
	6–12 GHz		-33		
	12 GHz–24 GHz		-26		
OIP2 (low) (2–nd Order Intercept point F2–F1)			57		dBm
V_{DD} (Drain Voltage Supply)			9	11	V
I_{DD} (Drain Current)			310	400	mA

1.2 Absolute Maximum Ratings

Table 1-2 shows the absolute maximum ratings of the MMA052PP45 device at 25 °C, unless otherwise specified. Exceeding any of the maximum ratings could cause damage and/or latent defects to the device.

Table 1-2. Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (V_{DD})	12V
Gate bias voltage (V_G)	-2V to 0.5V
RF input power (P_{in})	24 dBm (or 6 dB Compression)
Channel temperature	165 °C
V_{DD} Current (I_{DD})	400 mA
DC power dissipation ($T = 85\text{ °C}$)	4.8W
Thermal resistance	15 °C/W
Storage temperature	-65 °C to +150 °C
Operating temperature	-55 °C to +85 °C



ESD Sensitive Device

1.3 Typical Performance Curves

1.3.1 Typical Performances vs. Temperature

The following graphs shown in the Figures 1-1 through 1-40 represent the Typical Performance versus Temperature curves of the MMA052PP45 device under specific bias conditions. All measurements were taken using the Eval board shown in [Figure 3-2](#).

Figure 1-1. Gain vs. Temperature @ 5V/220 mA

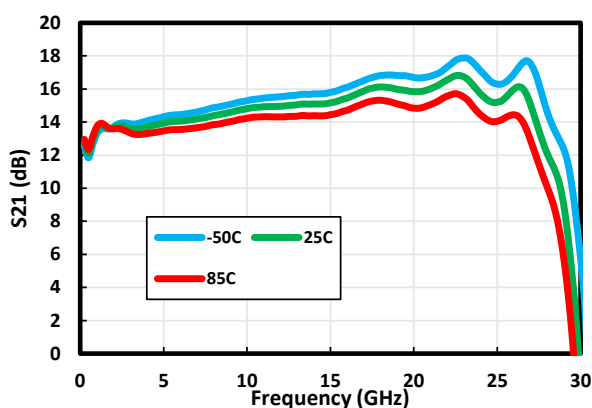


Figure 1-2. Gain vs. Temperature @ 8V/270 mA

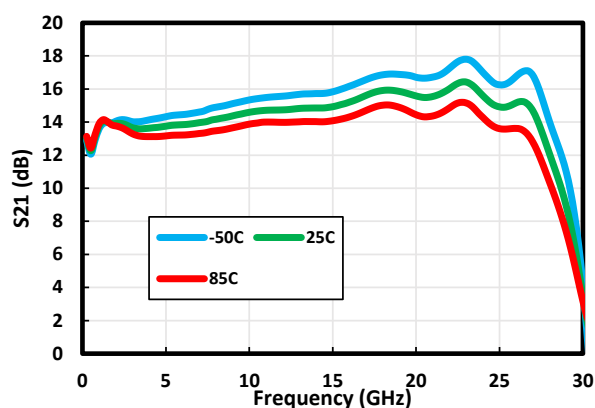


Figure 1-3. Gain vs. Temperature @ 9V/310 mA

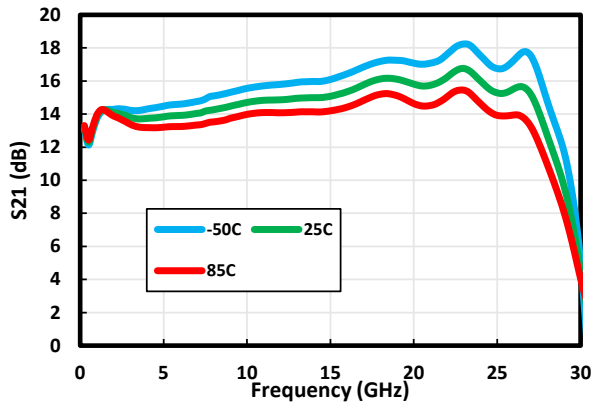


Figure 1-4. Gain vs. Temperature @ 10V/360 mA

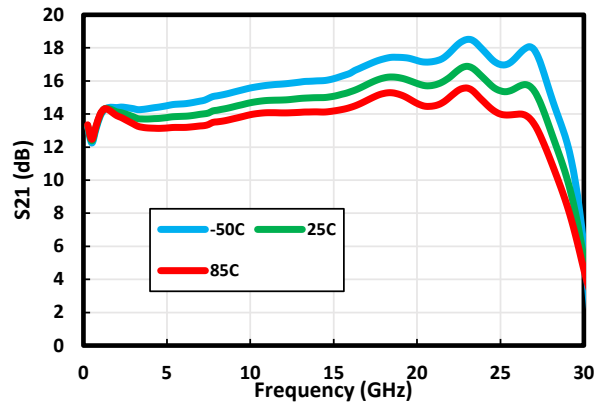


Figure 1-5. S11 vs. Temperature @ 5V/220 mA

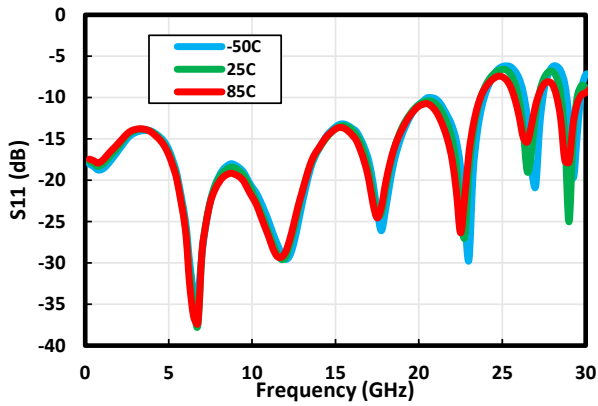


Figure 1-6. S11 vs. Temperature @ 8V/270 mA

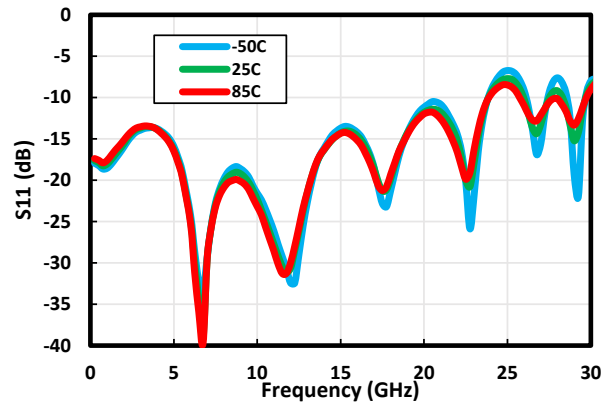


Figure 1-7. S11 vs. Temperature @ 9V/310 mA

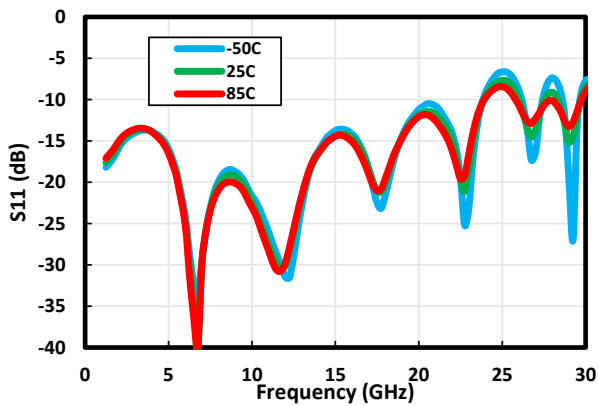


Figure 1-8. S11 vs. Temperature @ 10V/360 mA

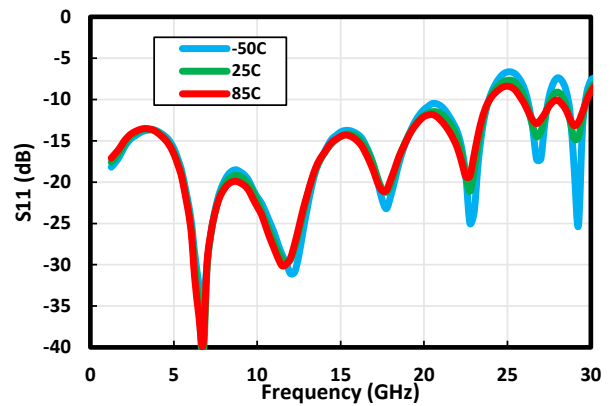


Figure 1-9. S22 vs. Temperature @ 5V/220 mA

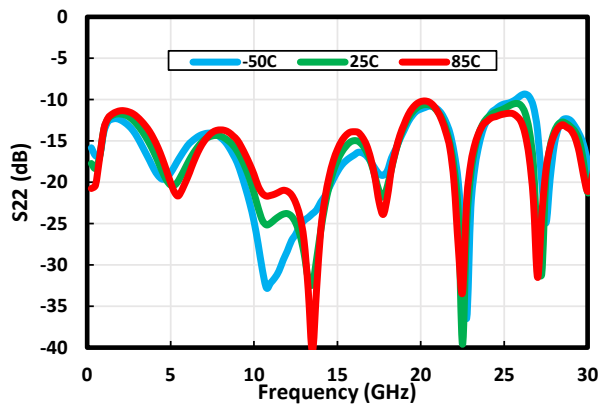


Figure 1-10. S22 vs. Temperature @ 8V/270 mA

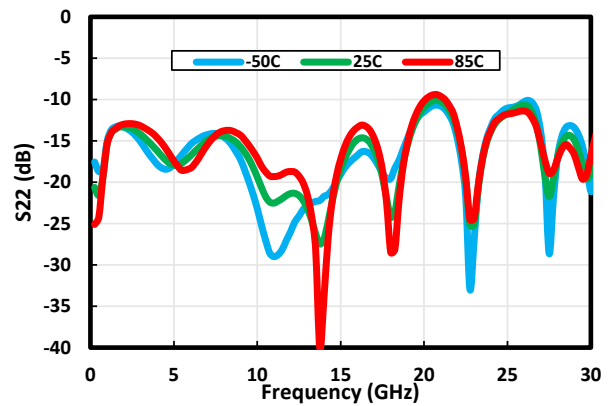


Figure 1-11. S22 vs. Temperature @ 9V/310 mA

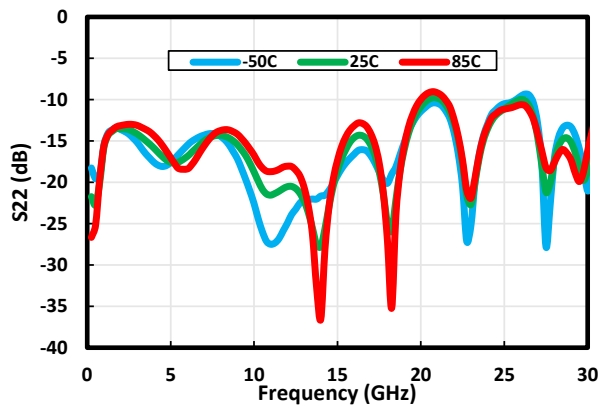


Figure 1-12. S22 vs. Temperature @ 10V/360 mA

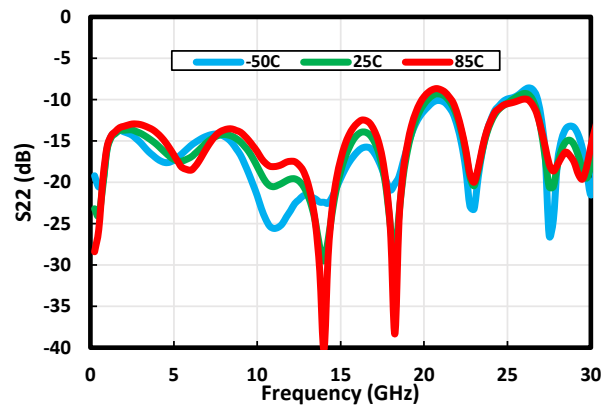


Figure 1-13. S12 vs. Temperature @ 5V/220 mA

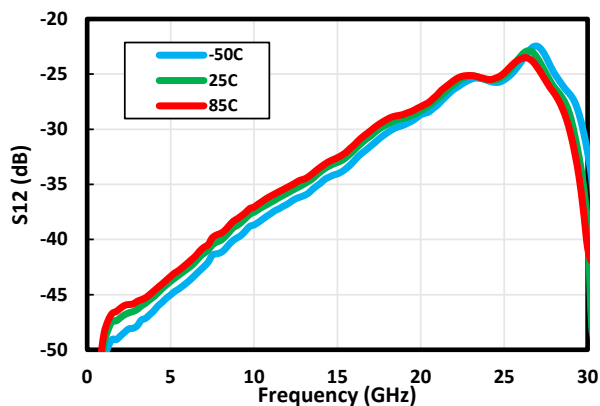


Figure 1-14. S12 vs. Temperature @ 8V/270 mA

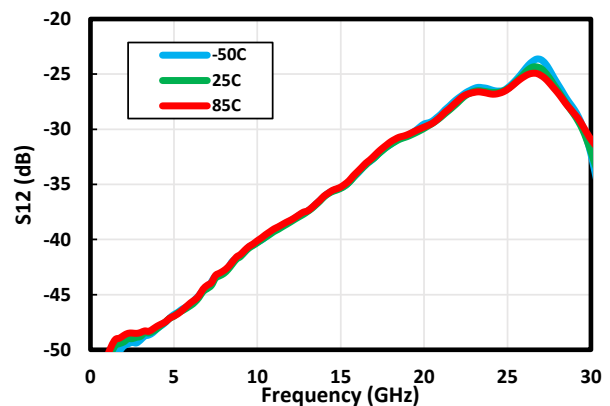


Figure 1-15. S12 vs. Temperature @ 9V/310 mA

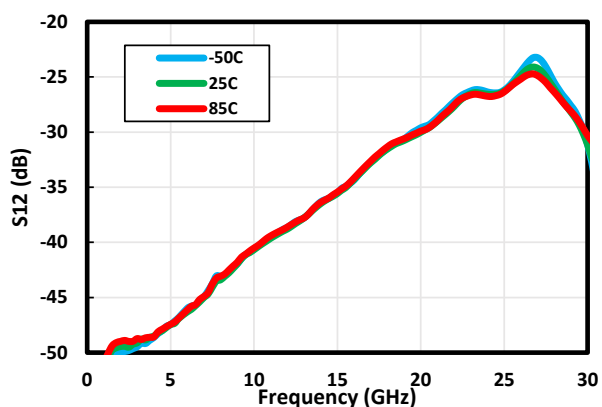


Figure 1-16. S12 vs. Temperature @ 10V/360 mA

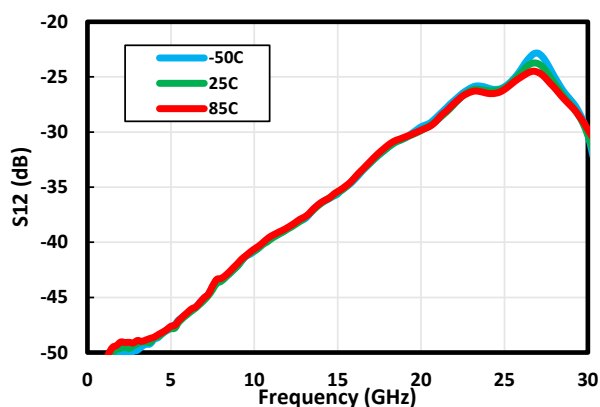


Figure 1-17. NF vs. Temperature @ 5V/220 mA

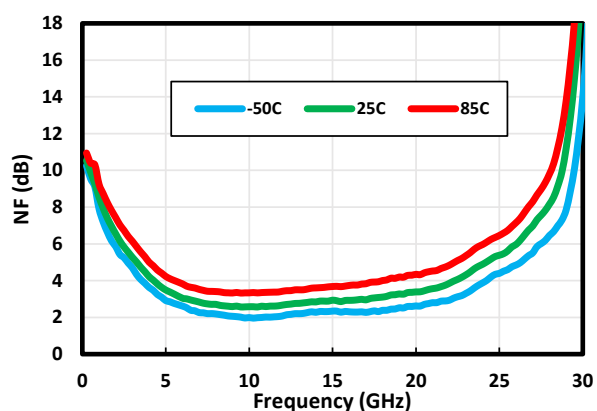


Figure 1-18. NF vs. Temperature @ 8V/270 mA

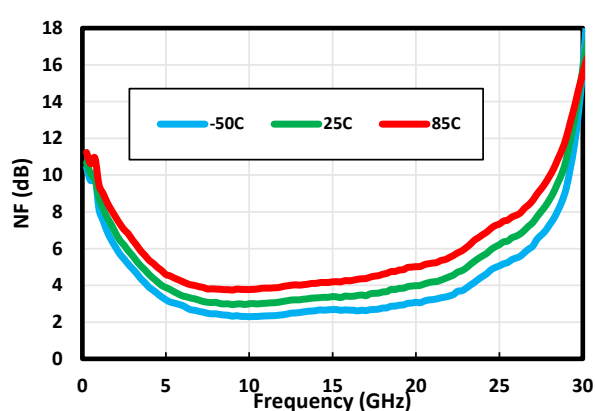


Figure 1-19. NF vs. Temperature @ 9V/310 mA

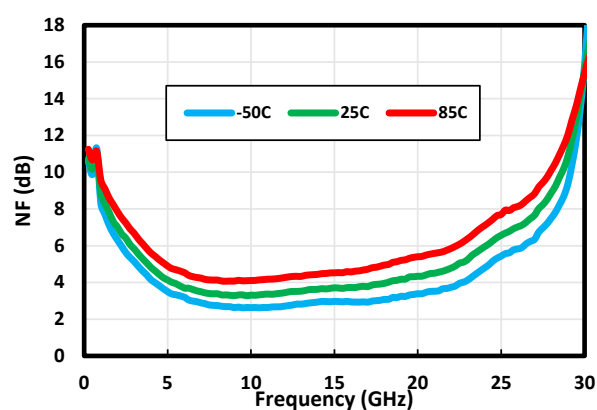


Figure 1-20. NF vs. Temperature @ 10V/360 mA

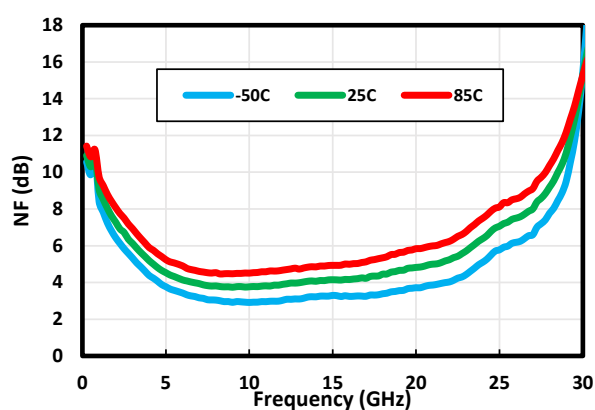


Figure 1-21. P1dB vs. Temperature @ 5V/220 mA

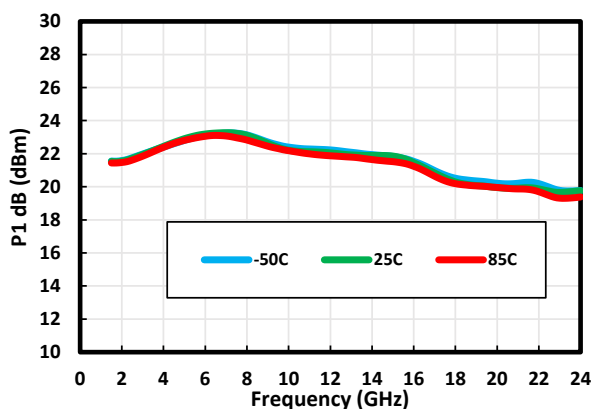


Figure 1-22. P1dB vs. Temperature @ 8V/270 mA

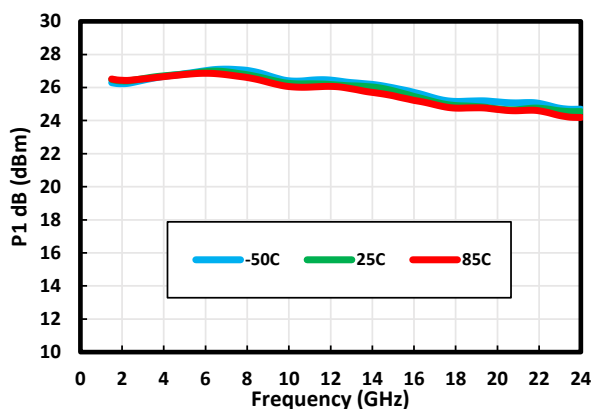


Figure 1-23. P1dB vs. Temperature @ 9V/310 mA

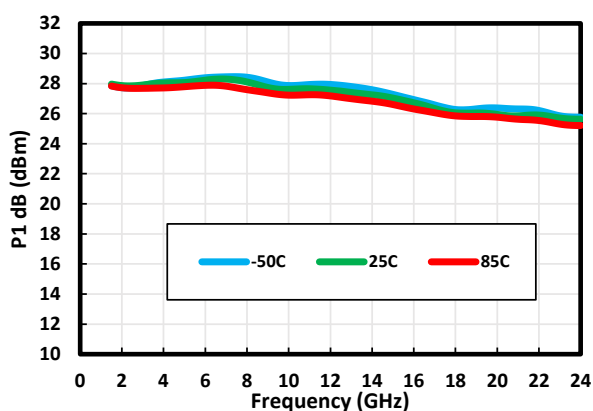


Figure 1-24. P1dB vs. Temperature @ 10V/360 mA

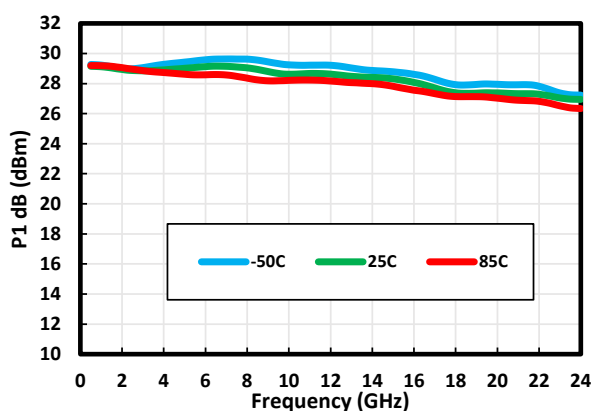


Figure 1-25. P_{sat} vs. Temperature @ 5V/220 mA

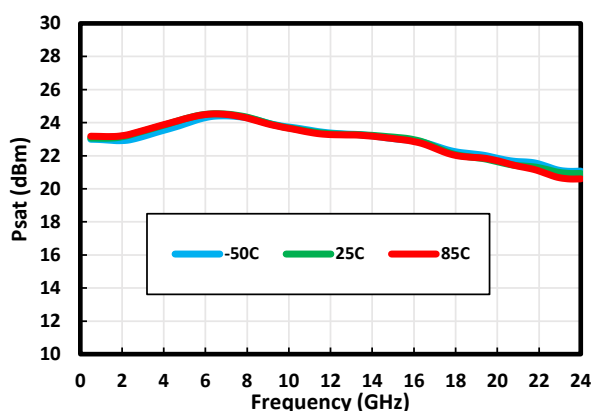


Figure 1-26. P_{sat} vs. Temperature @ 8V/270 mA

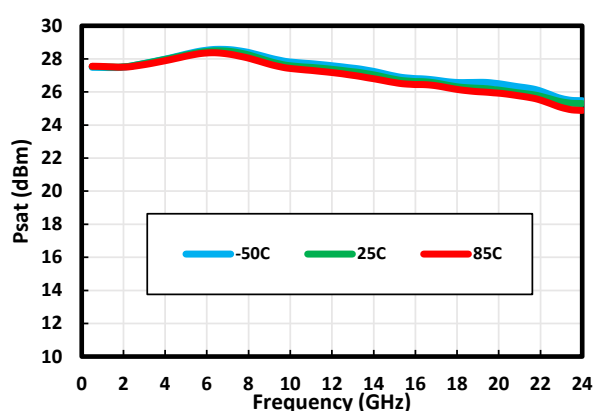


Figure 1-27. P_{sat} vs. Temperature @ 9V/310 mA

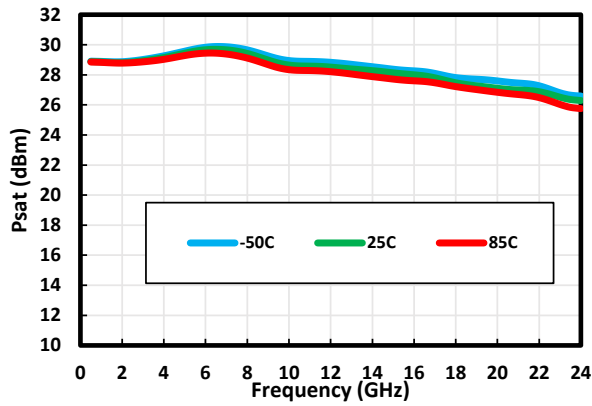


Figure 1-28. P_{sat} vs. Temperature @ 10V/360 mA

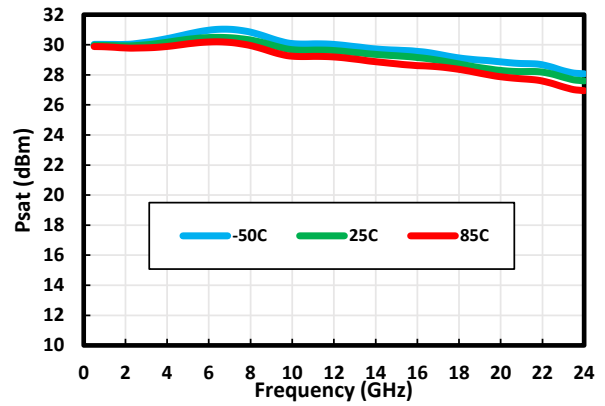


Figure 1-29. OIP3 vs. Temperature @ 5V/220 mA

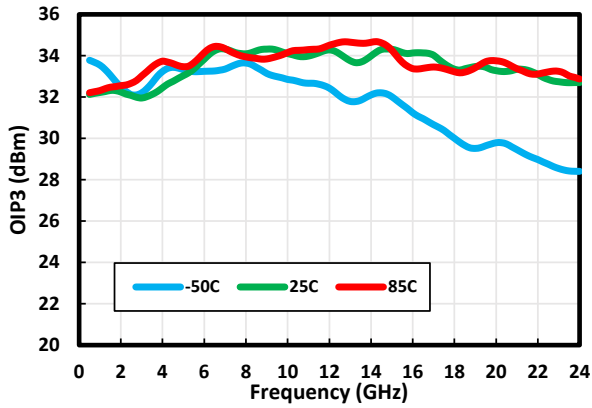


Figure 1-30. OIP3 vs. Temperature @ 8V/270 mA

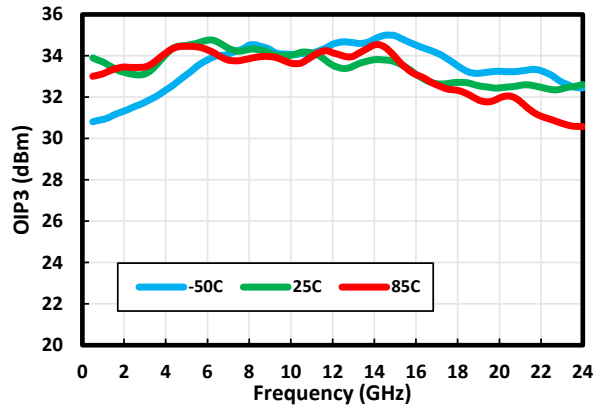


Figure 1-31. OIP3 vs. Temperature @ 9V/310 mA

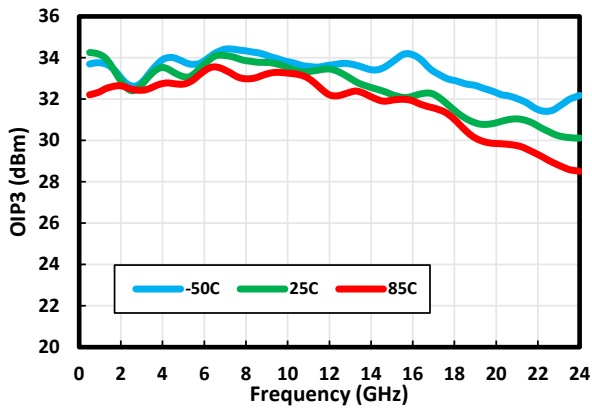


Figure 1-32. OIP3 vs. Temperature @ 10V/360 mA

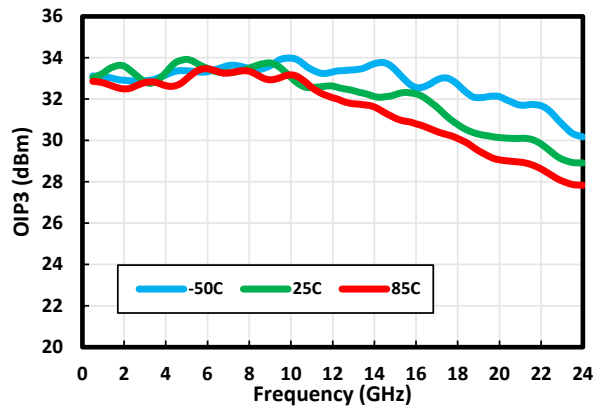


Figure 1-33. OIP2 (low) vs. Temperature @ 5V/210 mA

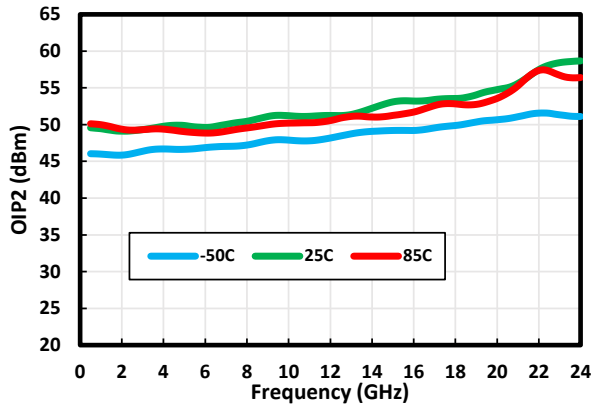


Figure 1-34. OIP2 (low) vs. Temperature @ 8V/270 mA

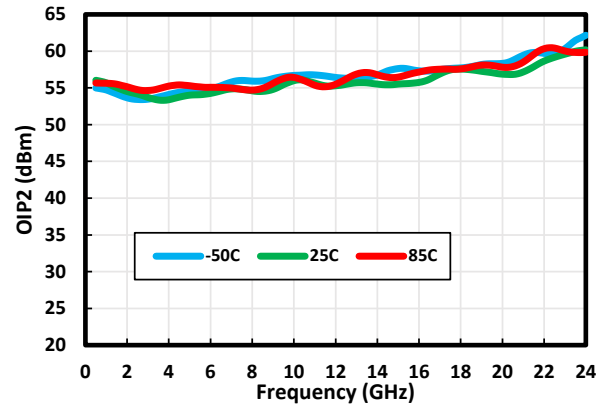


Figure 1-35. OIP2 (low) vs. Temperature @ 9V/310 mA

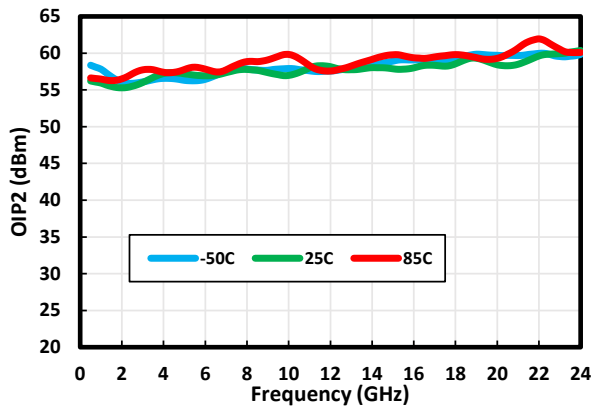


Figure 1-36. OIP2 (low) vs. Temperature @ 10V/360 mA

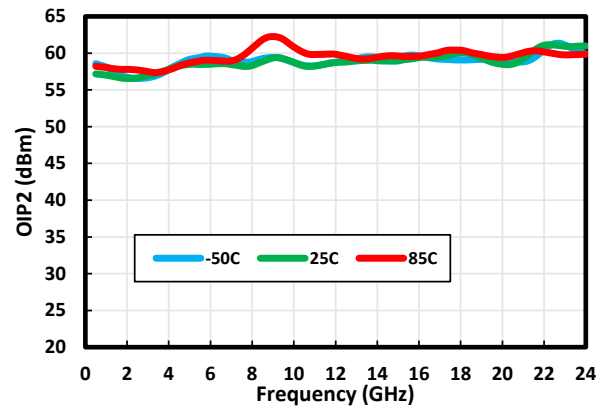


Figure 1-37. IM3 vs. Temperature @ 5V/220 mA

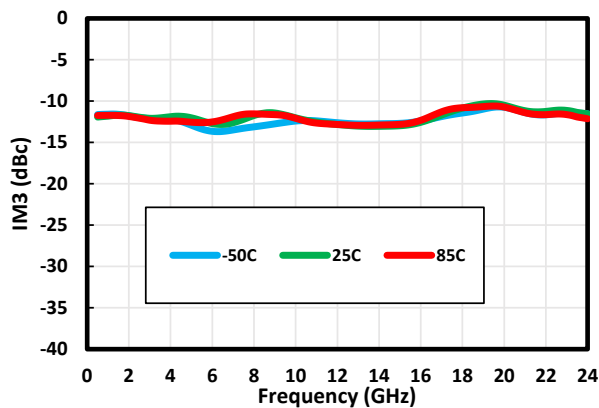


Figure 1-38. IM3 vs. Temperature @ 8V/270 mA

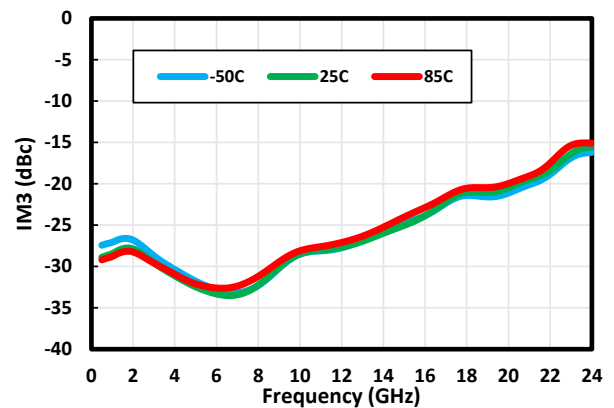


Figure 1-39. IM3 vs. Temperature @ 9V/310 mA

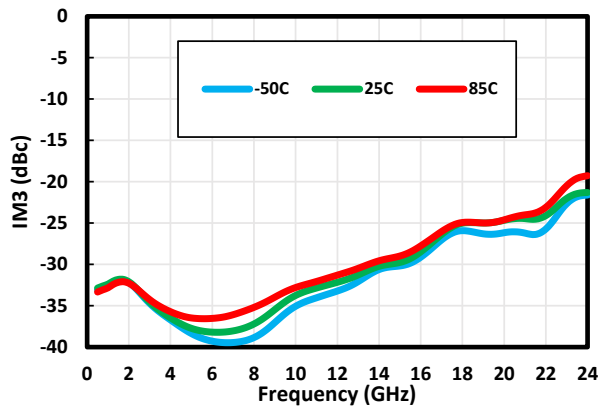
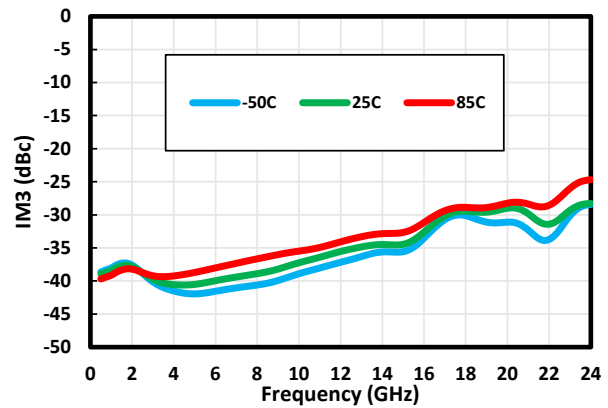


Figure 1-40. IM3 vs. Temperature @ 10V/360 mA



1.3.2 Typical Performances vs. Bias

The following graphs shown in the Figures 1-41 through 1-53 represent the Typical Performance versus Bias curves of the MMA052PP45 device under constant temperature of 25 °C. All measurements were taken using the Eval board shown in Figure 3-2. Currents were set by States according to Table 3-3.

Figure 1-41. Gain vs. V_{DD} @State 1

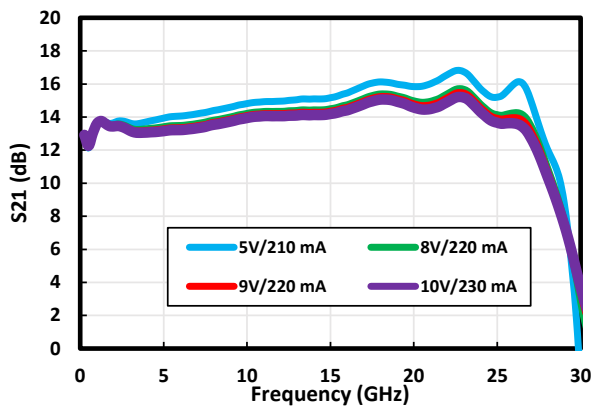


Figure 1-42. Gain vs. V_{DD} @State 5

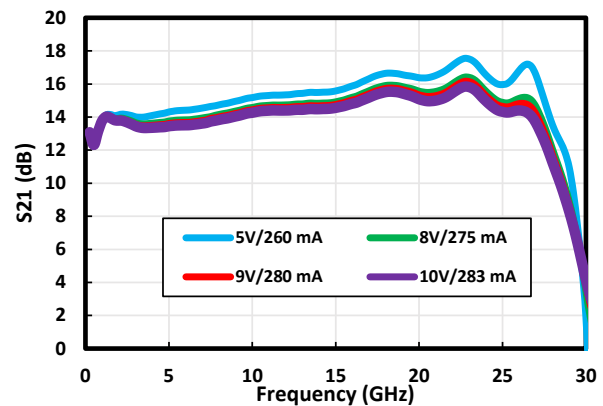


Figure 1-43. Gain vs. V_{DD} @State 8

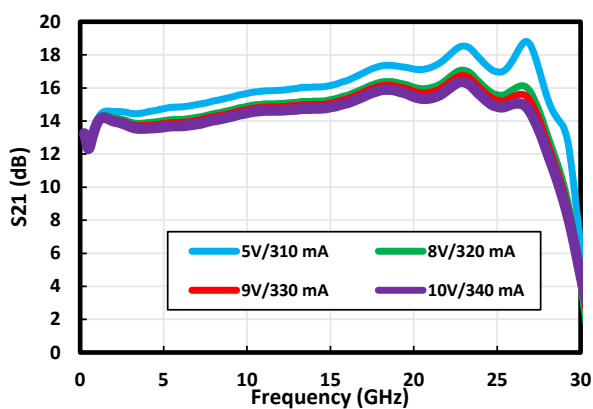


Figure 1-44. Gain vs. V_{DD} @State 16

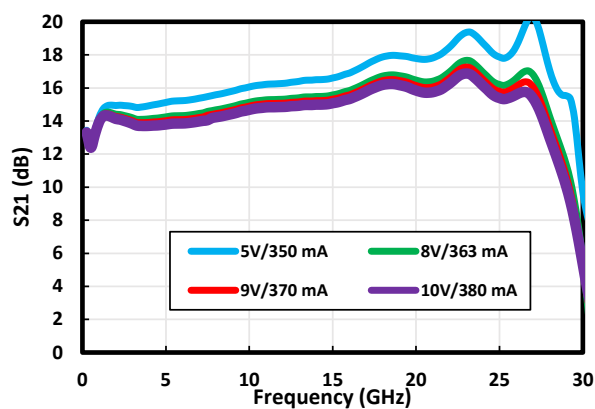


Figure 1-45. NF vs. V_{DD} @State 1

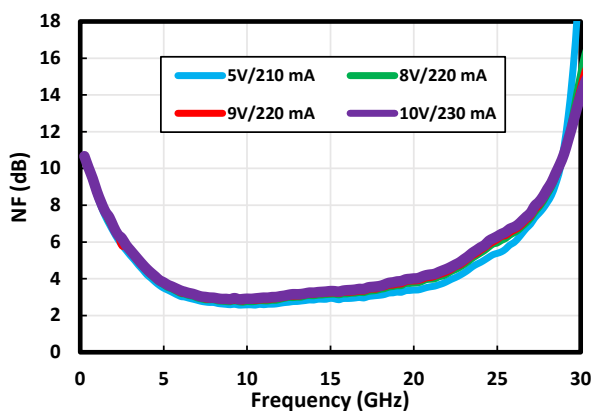


Figure 1-46. NF vs. V_{DD} @State 5

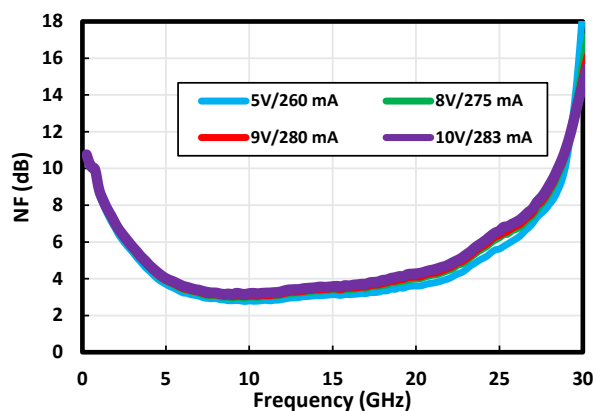


Figure 1-47. NF vs. V_{DD} @State 8

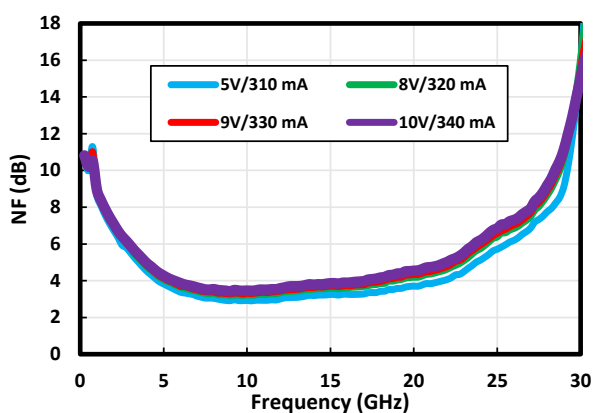


Figure 1-48. NF vs. V_{DD} @State 16

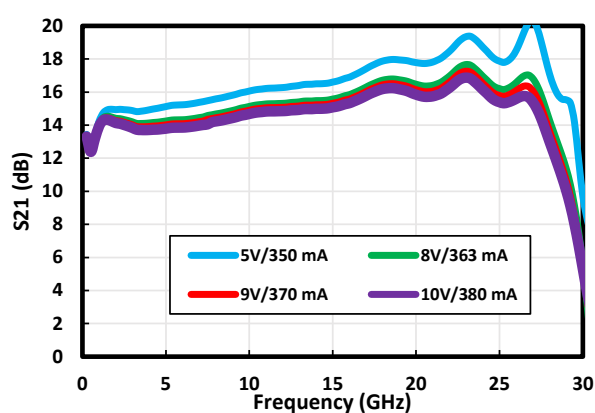


Figure 1-49. P1dB vs. V_{DD}/I_{DD}

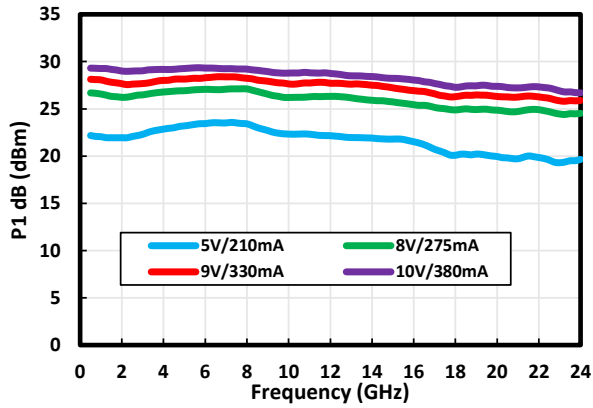


Figure 1-50. P_{sat} vs. V_{DD}/I_{DD}

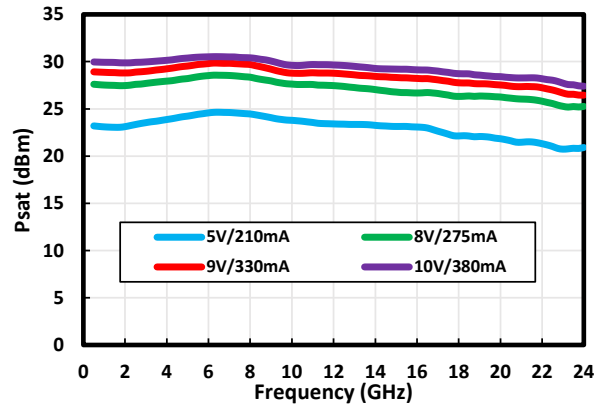


Figure 1-51. OIP3 vs. V_{DD}/I_{DD}

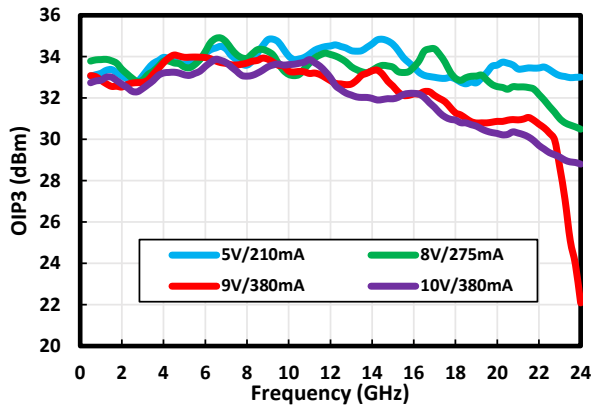


Figure 1-52. OIP2 Low at $\Delta = 10$ MHz
vs. V_{DD}/I_{DD}

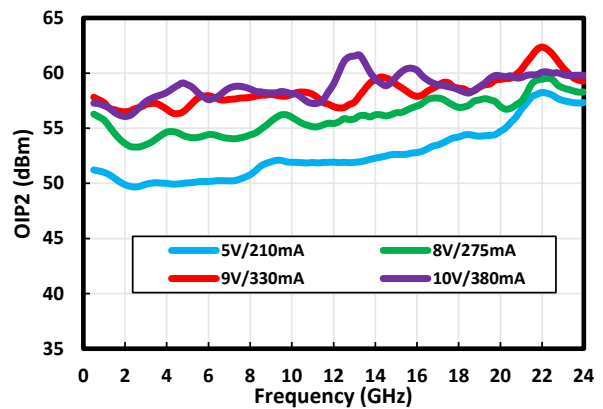
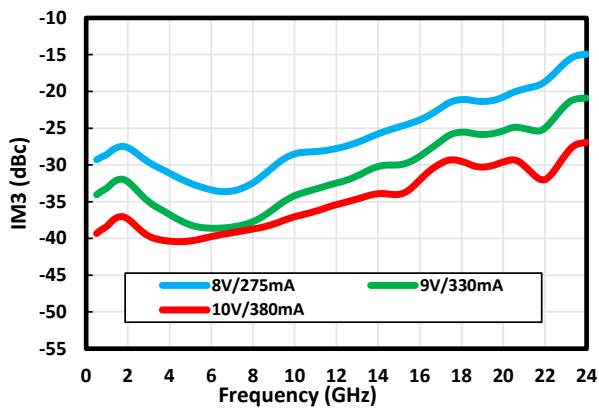


Figure 1-53. IM3 vs. V_{DD}/I_{DD} , 20 dBm (per tone)



1.3.3 Typical Performances vs. Output Power

The following graphs shown in the Figures 1-54 through 1-67 represent the Typical Performance versus Output Power curves of the MMA052PP45 device under constant temperature of 25 °C. All measurements were taken using the Eval board shown in [Figure 3-2](#).

Figure 1-54. IM2 vs. Power @ 5V/210 mA

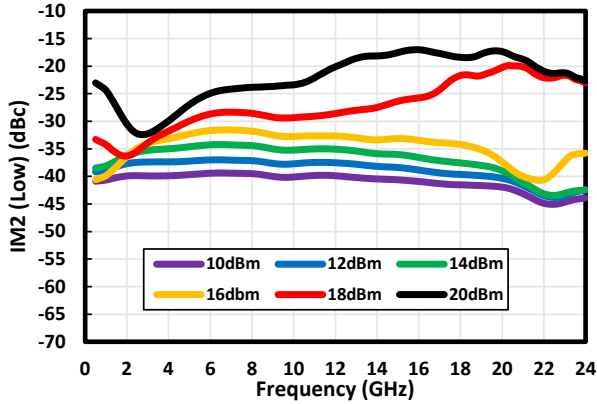


Figure 1-55. IM2 vs. Power @ 8V/275 mA

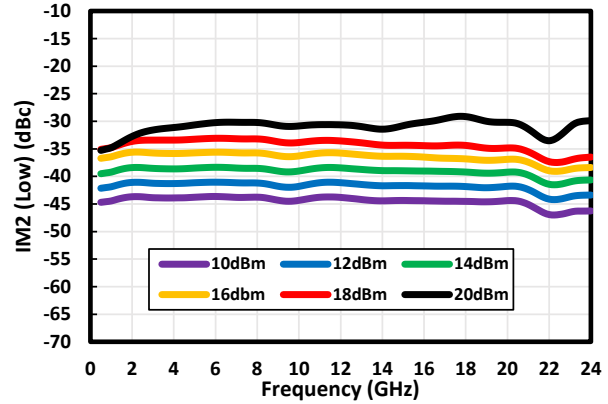


Figure 1-56. IM2 vs. Power @ 9V/330 mA

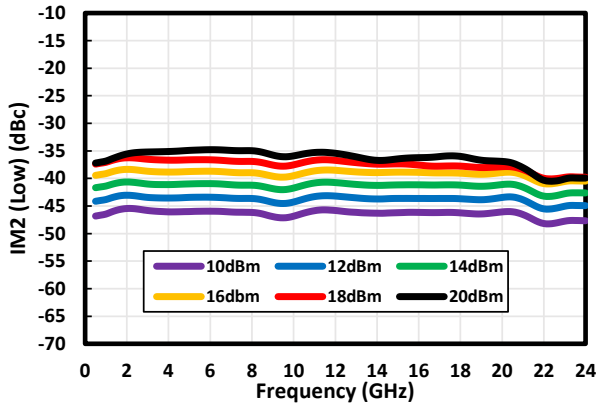


Figure 1-57. IM2 vs. Power @ 10V/380 mA

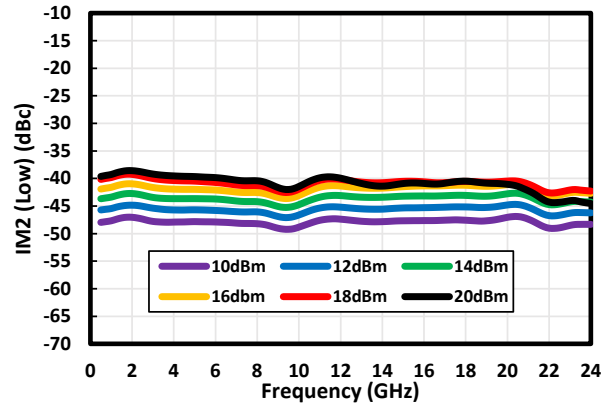


Figure 1-58. IM3 vs. Power @ 5V/210 mA

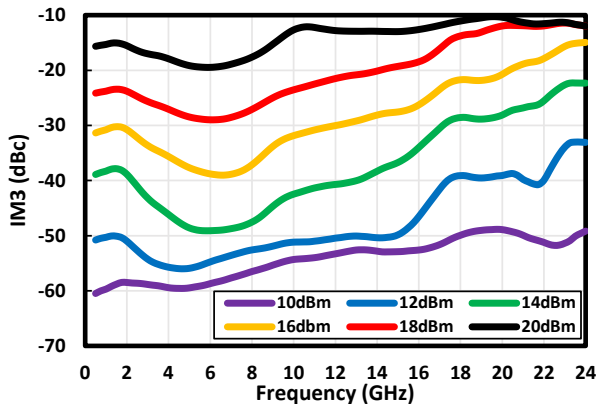


Figure 1-59. IM3 vs. Power @ 8V/275 mA

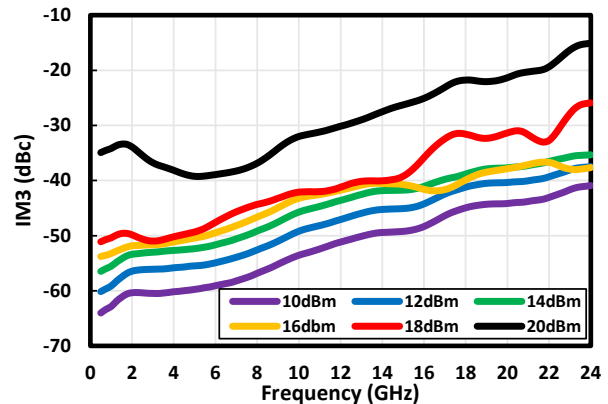


Figure 1-60. IM3 vs. Power @ 9V/330 mA

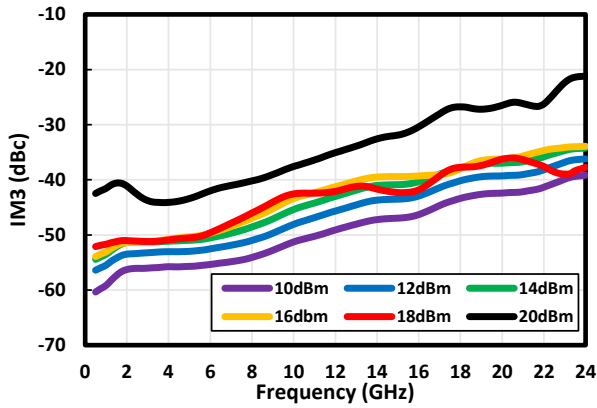


Figure 1-61. IM3 vs. Power @ 10V/380 mA

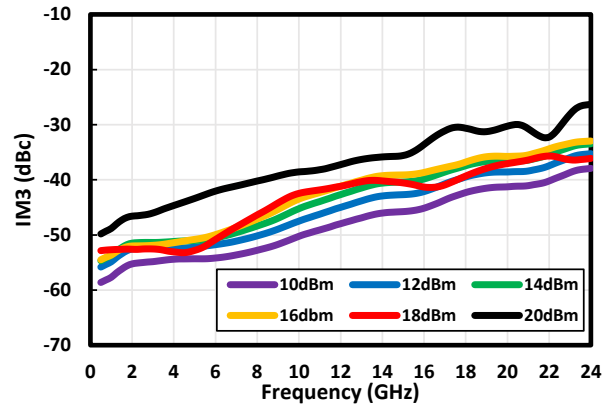


Figure 1-62. 2-ND Harmonic vs. Power @ 5V/210 mA

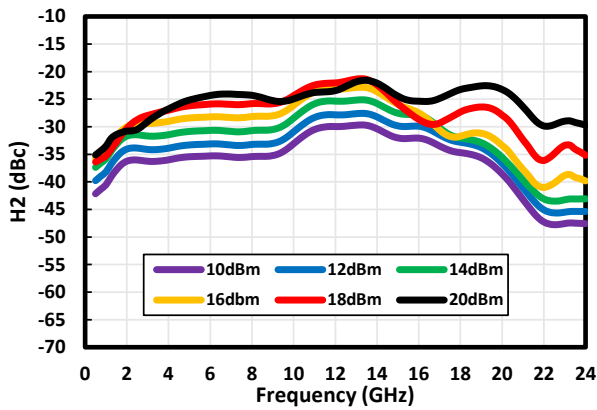


Figure 1-63. 2-ND Harmonic vs. Power @ 8V/275 mA

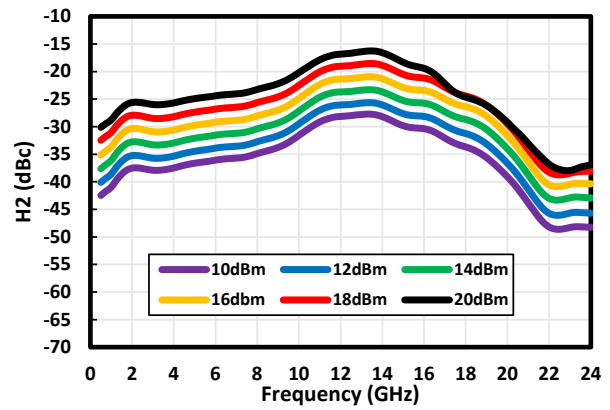


Figure 1-64. 2-ND Harmonic vs. Power @ 9V/330 mA

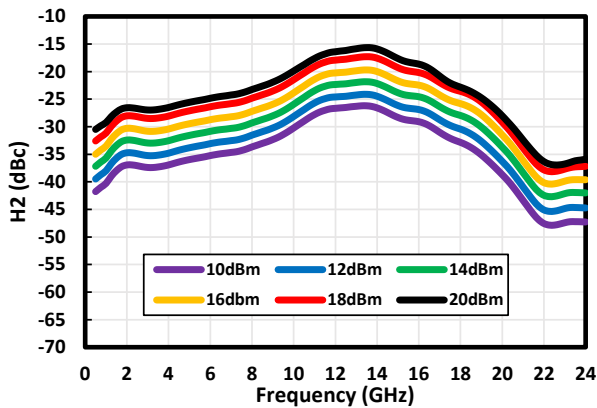


Figure 1-65. 2-ND Harmonic vs. Power @ 10V/380 mA

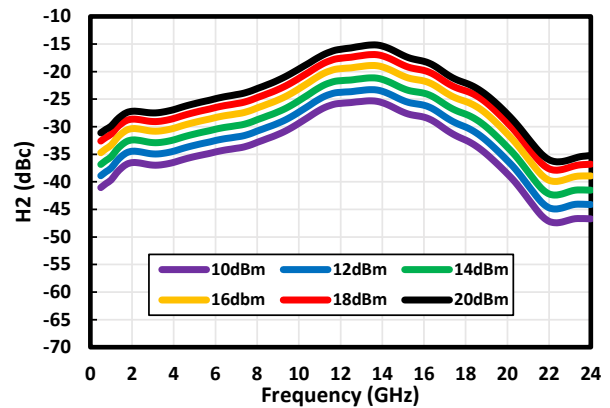


Figure 1-66. I_{DD} Current vs. Power @ 10V

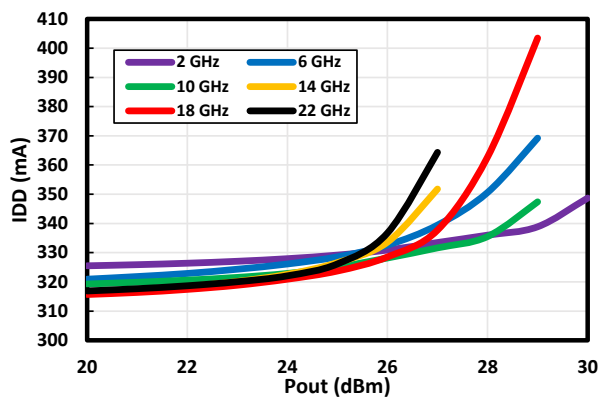
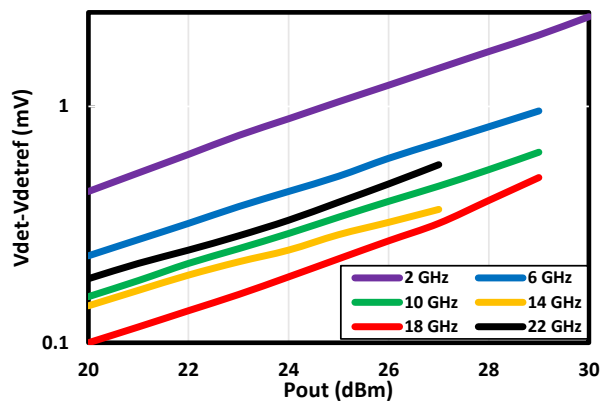


Figure 1-67. $V_{DET}-V_{DETREF}$ vs. Power



2. Package Specifications

The following illustration shows the package outline of the MMA052PP45 device. Dimensions are in millimeters [inches].

Figure 2-1. Package Outline Drawing (mm[Inches])

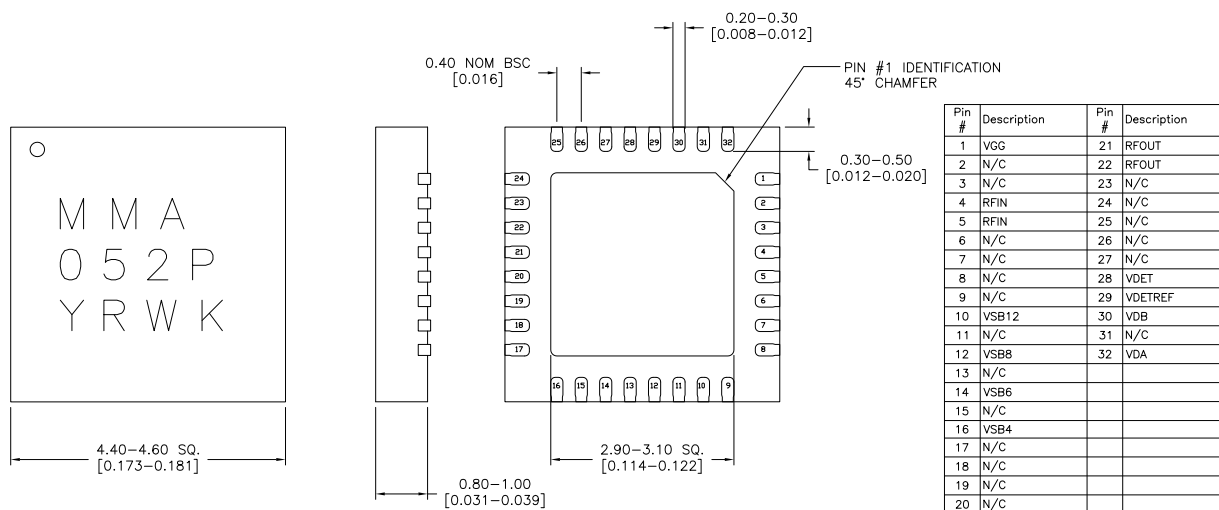


Table 2-1. Package Information

Package	4.5 mm × 4.5 mm 32L Plastic QFN
Lead Frame	C194 Cu
Plating	Ni/Pd/Au
Package Body Material	RoHS Compliant Low-stress injection molded plastic

Table 2-2. PIN Description

PIN Number	Pad Name	Pad Description
4 and 5	RF _{IN}	Pin 4 and 5 must be merged on the layout and are matched to 50Ω, and DC coupled to gate 1. (See figure 3-4 layout pattern.)
21 and 22	RF _{OUT}	Pin 21 and 22 must be merged on the layout and are matched to 50Ω. These pins are used for VDD bias. (See figure 3-4 layout pattern.)
1	V _{GG}	Bias for V _{GG} , must be coupled to VDD by connecting it to V _{DA} or V _{DB} externally for nominal operation
10, 12, 14, and 16	V _{SB}	Self-biasing resistors terminals, to adjust bias current by shorting one or several to the ground (see Table 3-3), if not used die will operate with its default current (about 200 mA)
28	V _{DET}	Detector pin, with DC voltage as function of output power, for correct operation of detector use V _{DET} -V _{DETREF} at external comparator
29	V _{DETREF}	Detector reference voltage
30 and 32	V _{DB} , V _{DA}	DC linked to VDD internally. External bypass capacitors are required to extend RF match and gain flatness below 2 GHz. Not intended for VDD bias
3, 6, 20, 23, Middle Pad	GND	Should be connected to RF/DC ground with as many vias as possible, see our recommended landing pattern as example
2, 7, 8, 9, 11, 13, 15, 17, 18, 19, 24, 25, 26, 27, and 31	N/C	These pins are not connected internally. All data was measured with these pins connected to RF/DC ground externally.

3. Evaluation PCB

Figure 3-1. Amplifier Functional Schematic

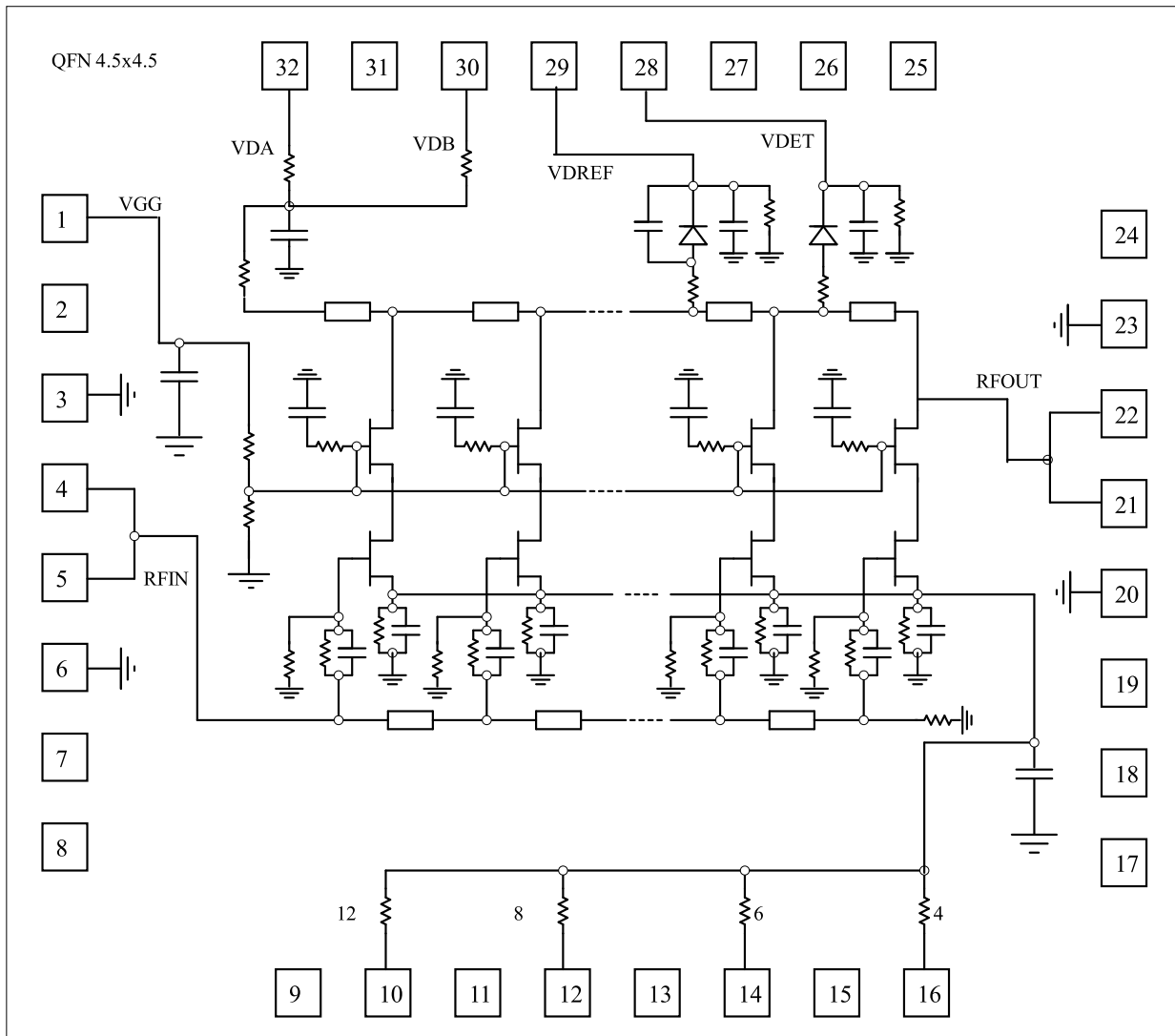
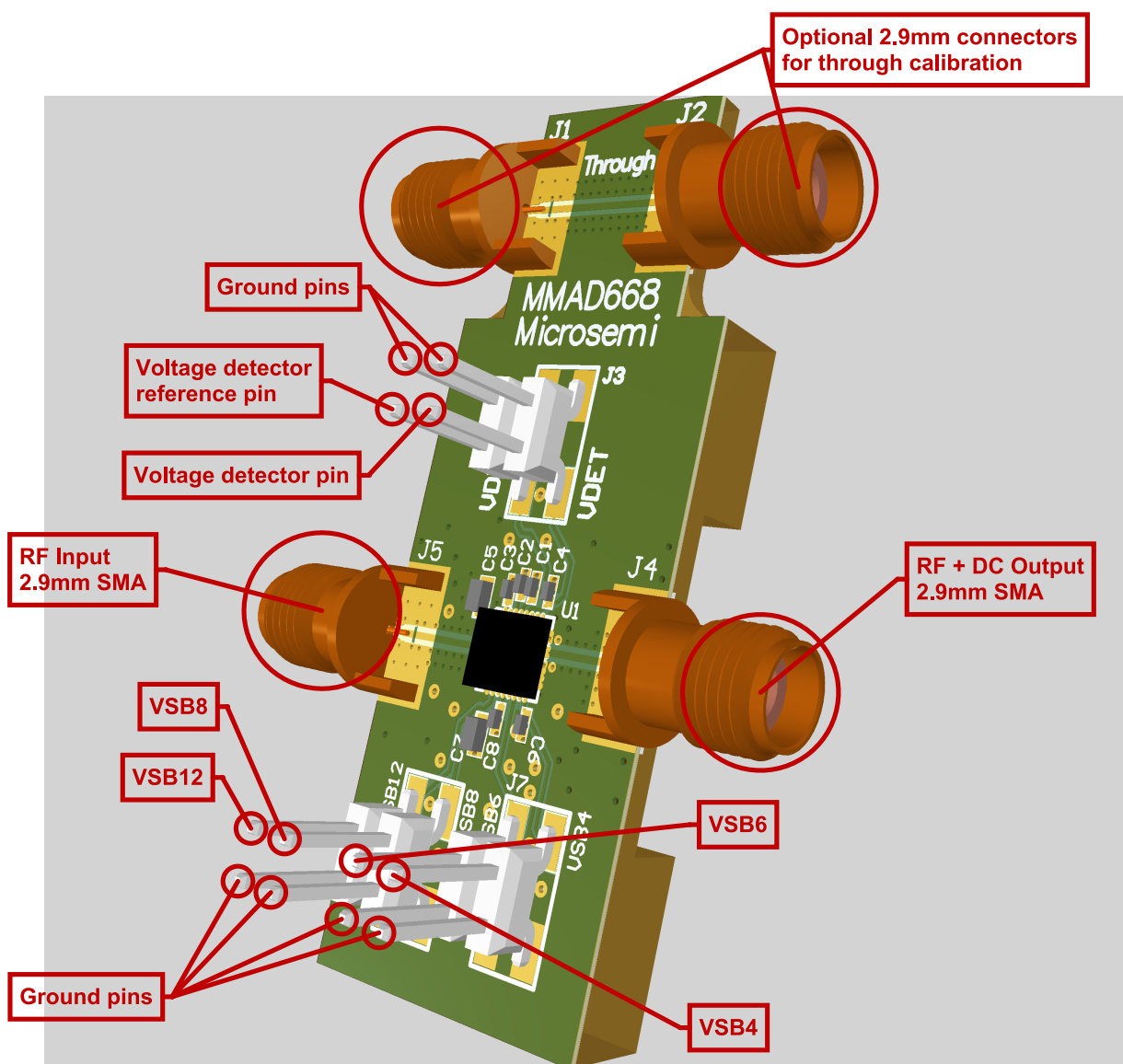


Figure 3-2. MMA052PP45E: Eval PCB



On the bottom two connectors where pins are labeled VSB12 through VSB4, the top row are connected internally to resistors that will change the drain current. The second row of pins below VSB12 through VSB4 are grounded. To use the different resistors in combinations to change the drain current jump the VSB pin to a ground pin as shown above. The average drain current values are listed below in [Table 3-3](#).

Figure 3-3. MMA052PP45E: Eval PCB Schematic

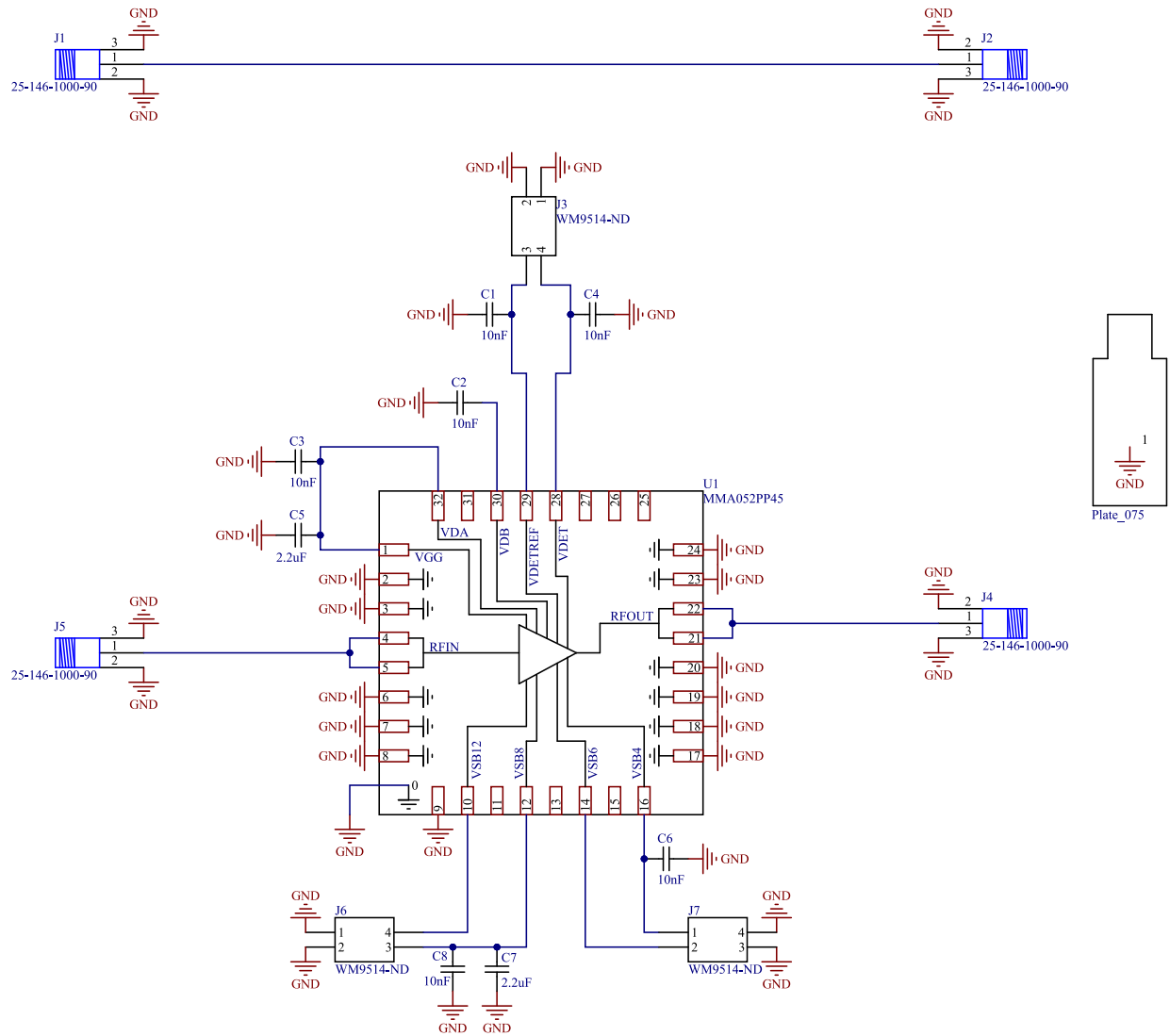


Table 3-1. MMA052PP45 Bias Sequence

Step	Bias Sequence
1	Make sure all DC and RF connections are attached before activating any DC voltage or supplies. Note: DC supply for VDD should be fed through an external bias-T on the RF+ DC output port (J4).
2	Make sure RF input port has no DC supplied to it as it will be terminated to grounded 50Ω.
3	Set VDD to desired bias voltage with current compliance within the desired current range.
4	Use short jumpers on J6 and J7 headers to set IDD using internal resistors. Note: To short a resistor pin, connect a jumper to the ground pin below it. There are five combinations (always measure IDD current). 1. No jumpers (default IDD current = 200 mA) 2. Jumper on VSB12: grounding 12Ω resistor 3. Jumper on VSB8: grounding 8Ω resistor 4. Jumper on VSB6: grounding 6Ω resistor 5. Jumper on VSB4: grounding 4Ω resistor Note: Use combination of jumpers to set required IDD current according to Absolute Maximum Ratings.



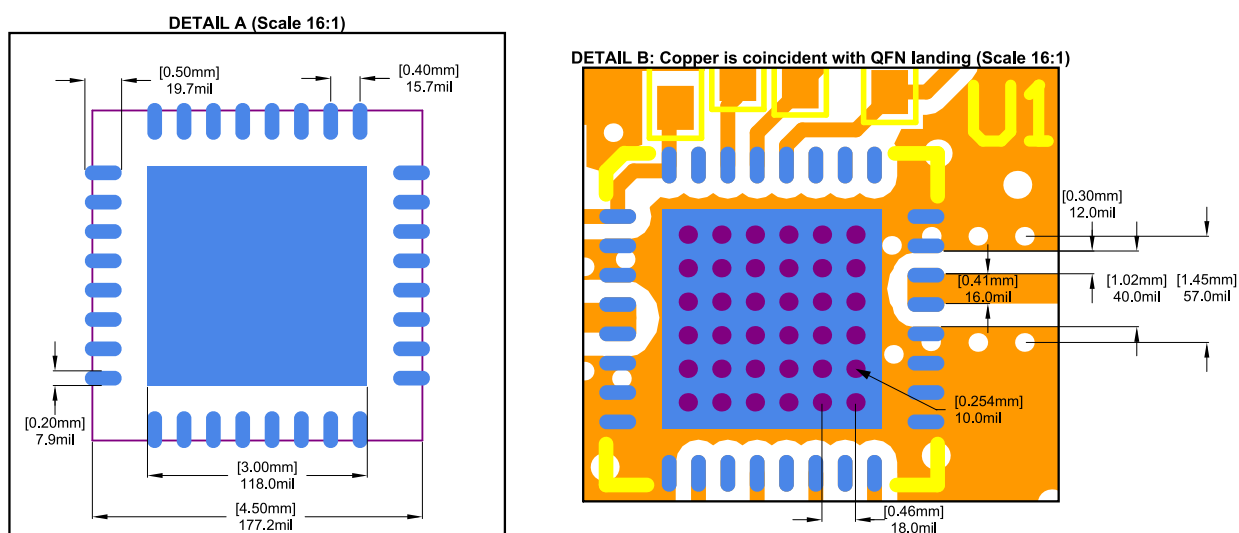
Ensure not to short VDET or VDETREF pins to avoid damage to the part.

Table 3-2. Bill of Material

Item Num.	Component designator	Description	Mnf. Part Num.	Mnf.	Qty.
1	p1	PCB Baseplate, 2.0" x 0.75"	MM-FD-0010	Poplar Hill Machine	1
2	U1	RF Power Amplifier, Self-Biased 0 GHz to 24 GHz 32-Pin QFN (4.5 x 4.5) Plastic	MMA052PP45	Microchip	1
3	C5, C7	2.2 μF ±10% 16V Ceramic Capacitor X5R 0603	GRM21BR71C225K A12L	Murata	2
4	J3, J6, J7	Header, 2-Pin, Dual row	15-91-2040	Molex	3
5	J1, J2, J4, J5	Connector, 2.9 mm Jack PCB Edge mount .012 pin	25-146-1000-90	Winchester Interconnect	4
6	C1, C2, C3, C4, C6, C8	10000 pF ±10% 50V Ceramic Capacitor X7R 0402	GRM155R71H103K A88D	Murata	6
7	SOLD1	Solder Paste, No Clean, Leadless, Sn63/Pb37	SMD291AX10T5	Chip Quik	1
8	SOLD2	Solder Wire, No Clean, Lead Free, SAC305	24-7068-7603	Kester Solder	1
9	EPOX1	Epoxy Ablefilm, ECF 563	ECF 563	Loctite	1

Table 3-3. I_{DD} currents vs. V_{SB} positioning States at different Voltages V_{DD}

State	VSB12	VSB8	VSB6	VSB4	I_{DD} at 5V (mA)	I_{DD} at 8V (mA)	I_{DD} at 9V (mA)	I_{DD} at 10V (mA)
1	Open	Open	Open	Open	208	219	223	227
2	Short	Open	Open	Open	237	249	253	258
3	Open	Short	Open	Open	250	262	267	271
4	Short	Short	Open	Open	273	285	290	295
5	Open	Open	Short	Open	262	275	279	284
6	Short	Open	Short	Open	284	296	301	306
7	Open	Short	Short	Open	293	306	311	316
8	Short	Short	Short	Open	310	322	328	334
9	Open	Open	Open	Short	283	296	301	306
10	Short	Open	Open	Short	302	315	320	326
11	Open	Short	Open	Short	310	324	329	335
12	Short	Short	Open	Short	325	339	344	351
13	Open	Open	Short	Short	318	332	337	343
14	Short	Open	Short	Short	332	346	351	358
15	Open	Short	Short	Short	339	352	357	364
16	Short	Short	Short	Short	350	364	369	376

Figure 3-4. Eval PCB Details


4. Ordering, Shipping, and Handling

4.1 Handling Recommendations

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microchip application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4.2 Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package	Note
MMA052PP45	4.5 mm × 4.5 mm, 32L Plastic QFN	
MMA052AA	Die	Refer to corresponding MMA052AA Datasheet
MMA052PP45E	Eval PCB	

4.3 Packing Information

Part Number	Description
MMA052PP45/TR	Tape and Reel

Note: Contact your Microchip sales representative for the minimum quantity order

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
B	11/2024	Updated Eval PCB drawing, layout patterns, and schematic. Added handling recommendations.
A	10/2022	Document migrated from Microsemi template to Microchip template; assigned Microchip literature number DS-00004138A, which replaces the previous Microsemi literature number MSCC-0341-DS-00114.
Previous releases (Microsemi Revisions 1.0 and 2.0)	10/2018 – 06/2019	Document created.

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