DC – 10 GHz 1 W GaAs Distributed Power MMIC Amplifier

MMA053PP5

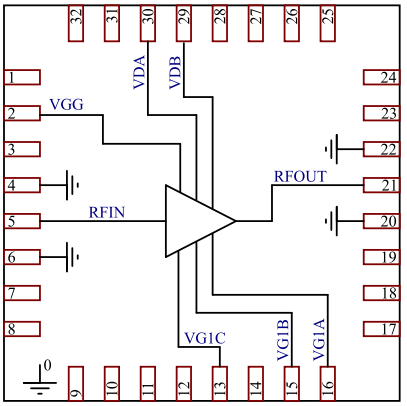
Product Overview

MMA053PP5 is a Gallium Arsenide (GaAs) Monolithic Microwave Integrated Circuit (MMIC) pHEMT distributed power amplifier in plastic QFN package that operates between DC and 10 GHz. The amplifier provides 17 dB of gain, +39 dBm output IP3, and +30 dBm of saturated output power, while requiring only 350 mA from 10V supply. Gain over DC to 6 GHz frequency range varies by only 0.2 dB, making the MMA053PP5 ideal for EW, ECM, RADAR, and test equipment application. The MMA053PP5 amplifier features plastic overmolded 5 mm × 5 mm QFN Package and I/Os that are internally matched to 50Ω.

Key Features

- Broadband performance: DC to 10 GHz
- High gain: 17 dB
- High saturated power: 30 dBm
- Supply: 10V at 350 mA
- 50Ω matched input/output
- Die size: 3 mm × 2.25 mm, 0.075 mm
- Passivated space-qualified process listed on EPPL007–38
- Packaged in overmolded 5 mm × 5 mm QFN Plastic Package

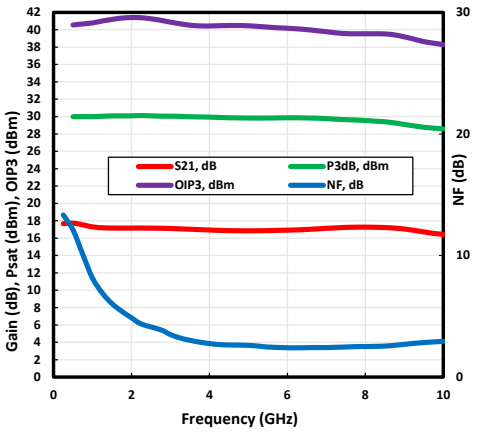
Amplifier Functional Diagram



Applications

- Test and measurement instrumentation
- Military, EW, ECM, RADAR and space
- Telecom infrastructure
- Wideband microwave radios

Performance Curves



Performance Overview

Parameter	Typ.	Units
Operational frequency range	DC – 10	GHz
Gain	17	dB
P3dB	+30	dBm
OIP3	39	dBm
Current at +10V supply	350	mA

Export Classification: EAR99

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1. Electrical Specifications

1.1 Typical Electrical Performance

Table 1-1. Typical Electrical Performance at 25 °C, V_{DD} = 10V, I_{DD} = 350 mA (Unless otherwise mentioned)

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		DC		10	GHz
Gain	DC – 6 GHz	16	17		dB
	6 GHz – 10 GHz	15.5	16.5		
Gain flatness	DC – 6 GHz		0.2		dB
	6 GHz – 10 GHz		0.5		
P1dB at 11V/420 mA	DC – 6 GHz	27	29		dBm
	6 GHz – 10 GHz	26.5	29		
	10 GHz – 12 GHz		25		
Noise figure	2 GHz – 6 GHz		3	5.5	dB
	6 GHz – 10 GHz		2.5	3.5	
Input return loss	DC – 6 GHz	13	20		dB
	6 GHz – 10 GHz	9	12		
Output return loss	DC – 6 GHz	12	15		dB
	6 GHz – 10 GHz	12	15		
P1dB	DC – 6 GHz	26	27.5		dBm
	6 GHz – 10 GHz	26	27		
P_{sat} (measured at 3 dB gain compression)	DC – 6 GHz	28	30		dBm
	10 GHz – 12 GHz	27	29		
OIP3	DC – 6 GHz		39		dBm
	6 GHz – 10 GHz		39		
IM3 at 20 dBm	DC – 6 GHz		-37		dBc
	6 GHz – 10 GHz		-35		
OIP2 (low) (2nd order point F2–F1)			45		dBm
V_{DD} (drain voltage supply)			10		V
I_{DD} (drain current)			350		mA

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1.2 Absolute Maximum Ratings

The Table 1–2 shows the absolute maximum ratings of the MMA053PP5 device at 25 °C, unless otherwise specified. Exceeding any of the maximum ratings potentially could cause damage and/or latent defects to the device.

Table 1-2. Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (V_{DD})	+12V
Gate bias voltage (V_G)	–2V to 0.5V
RF input power (Pin)	17 dBm (or 6 dB compression)
Channel temperature	165 °C
V_{DD} current (I_{DD})	520 mA
DC power dissipation (T = 85 °C)	5.7W
Thermal resistance	14 °C/W
Storage temperature	–65 °C to +150 °C
Operating temperature	–55 °C to +85 °C



ESD Sensitive Device

1.3 Typical Performance Curves

1.3.1 Typical Performances vs. Temperature

The graphs shown in Figures 1–1 through 1–40 represent the Typical Performance versus Temperature curves of the MMA053PP5 device under specific bias conditions. All measurements were taken using the test circuit shown in Figure 3-2.

Figure 1-1. Gain vs. Temperature at 5V/200 mA

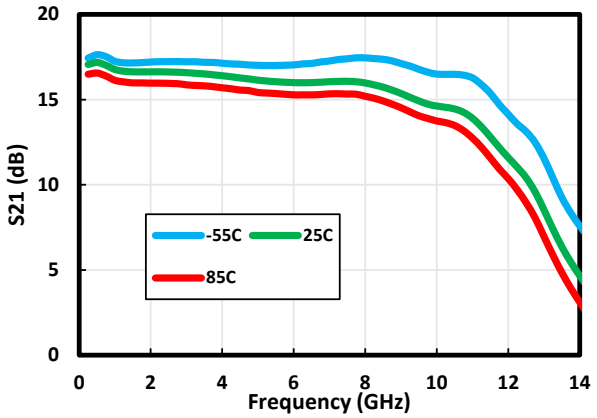

Figure 1-2. Gain vs. Temperature at 9V/300 mA

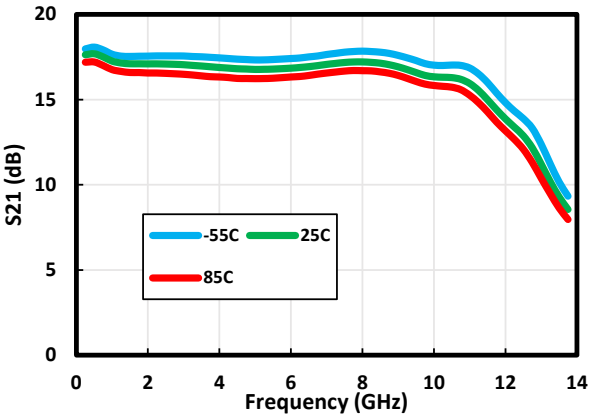

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Figure 1-3. Gain vs. Temperature at 10V/350 mA

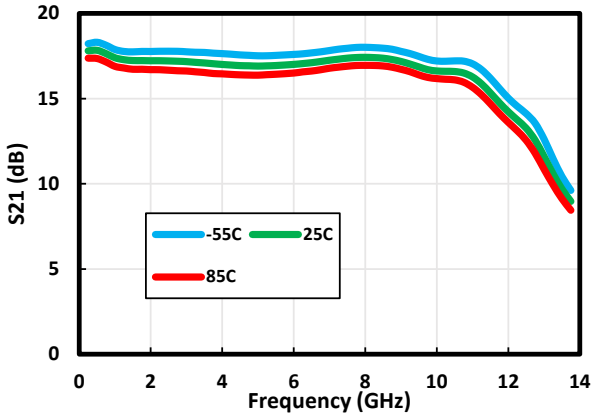

Figure 1-4. Gain vs. Temperature at 11V/400 mA

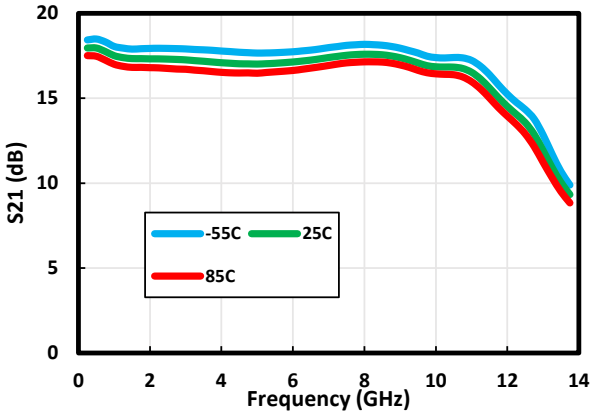

Figure 1-5. S11 vs. Temperature at 5V/200 mA

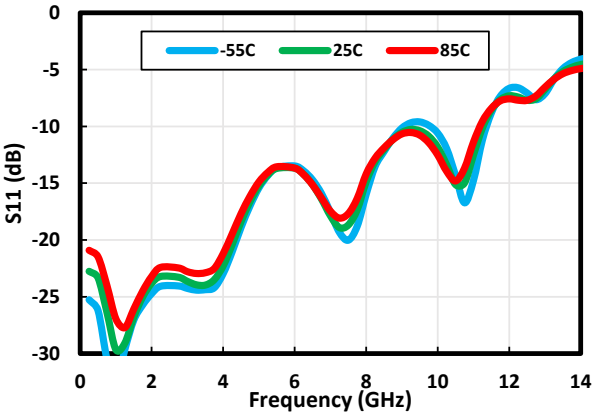

Figure 1-6. S11 vs. Temperature at 9V/300 mA

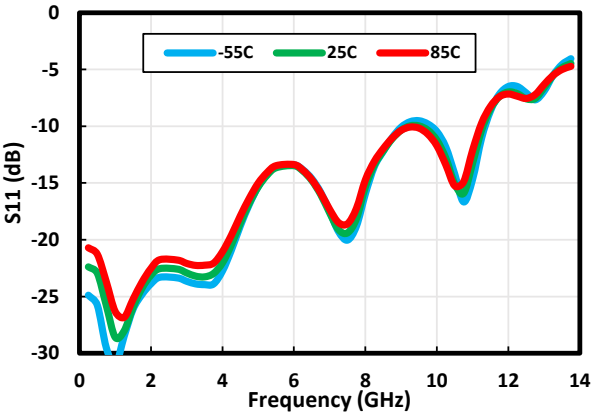

Figure 1-7. S11 vs. Temperature at 10V/350 mA

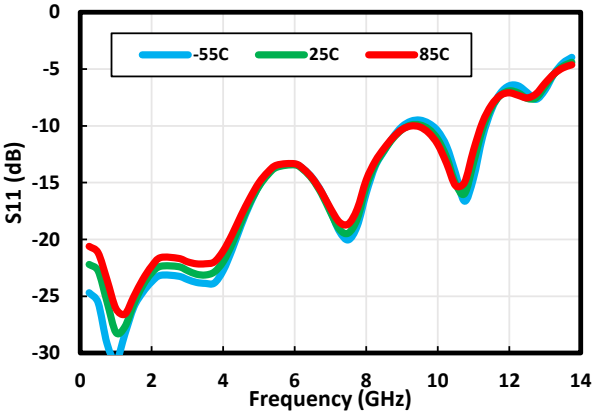

Figure 1-8. S11 vs. Temperature at 11V/400 mA

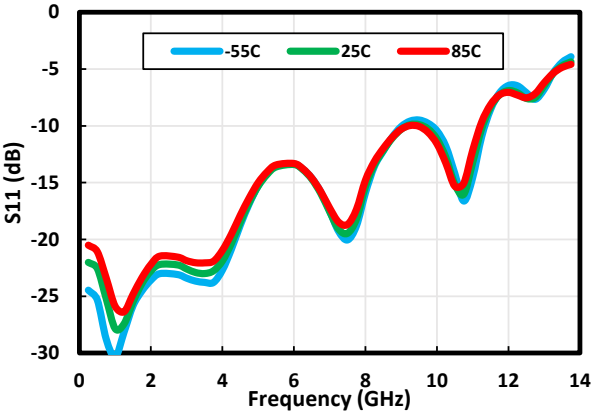

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Figure 1-9. S22 vs. Temperature at 5V/200 mA

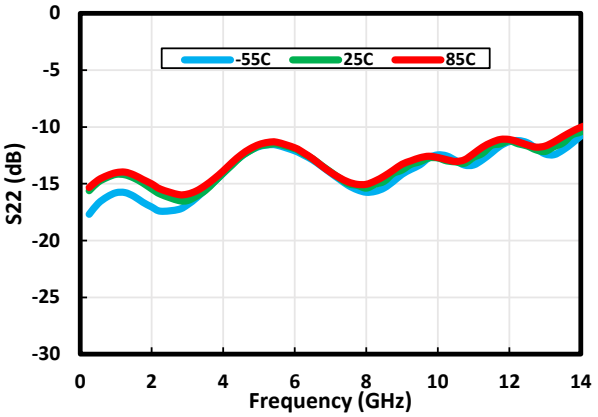

Figure 1-10. S22 vs. Temperature at 9V/300 mA

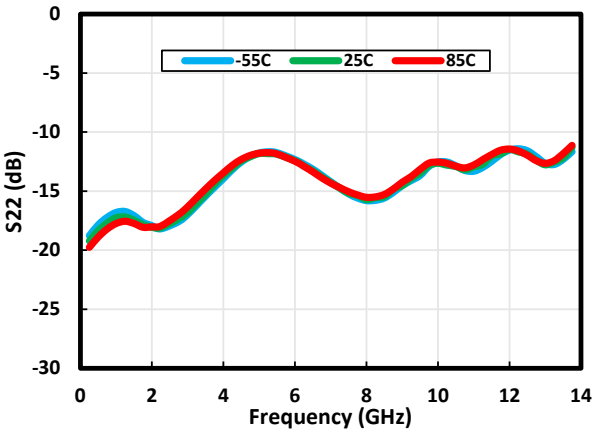

Figure 1-11. S22 vs. Temperature at 10V/350 mA

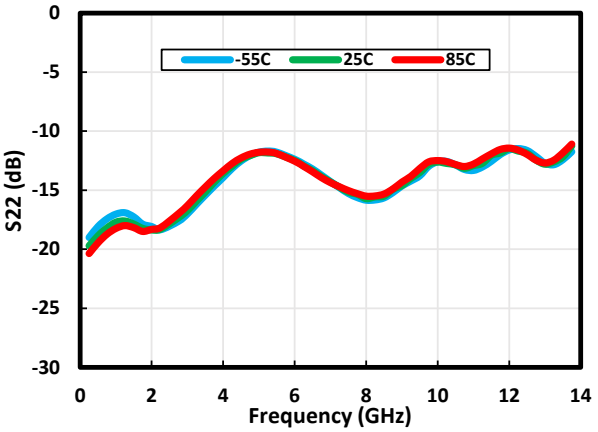

Figure 1-12. S22 vs. Temperature at 11V/400 mA

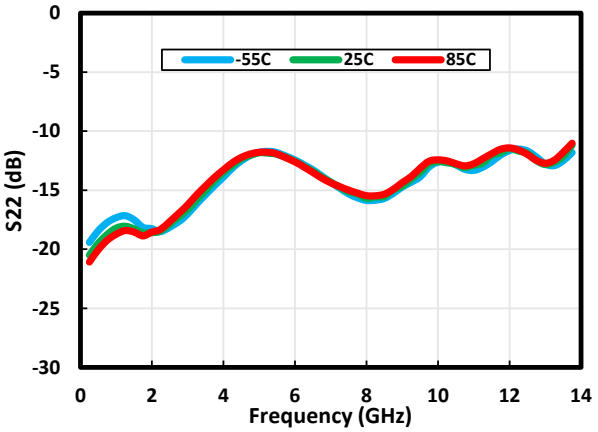

Figure 1-13. S12 vs. Temperature at 5V/200 mA

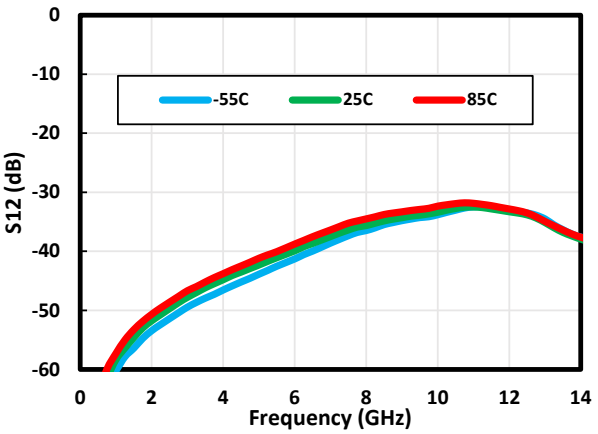

Figure 1-14. S12 vs. Temperature at 9V/300 mA

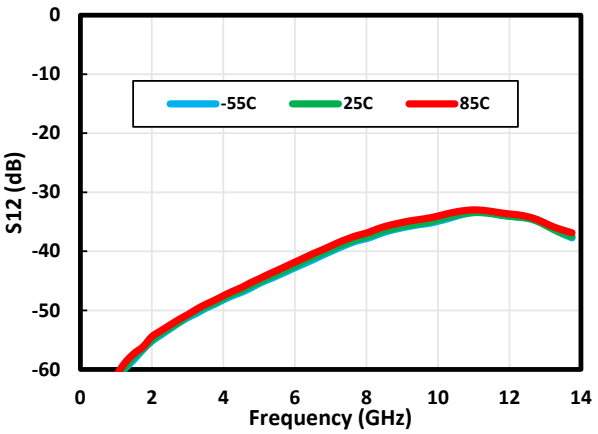

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Figure 1-15. S12 vs. Temperature at 10V/350 mA

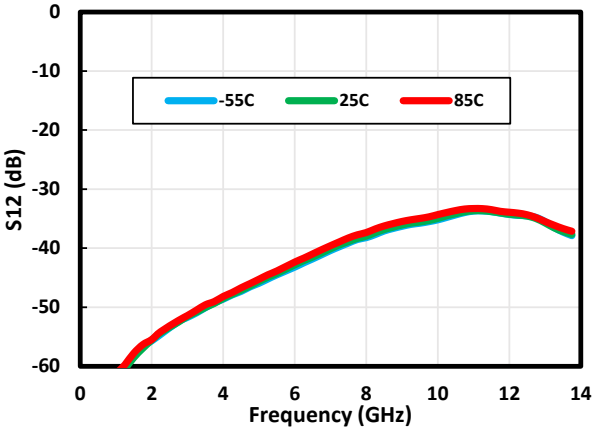

Figure 1-16. S12 vs. Temperature at 11V/400 mA

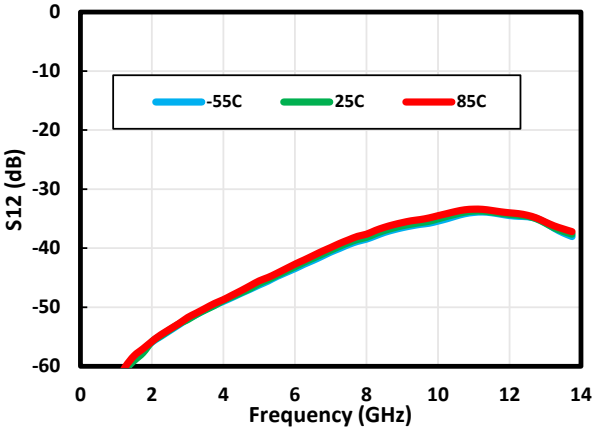

Figure 1-17. NF vs. Temperature at 5V/200 mA

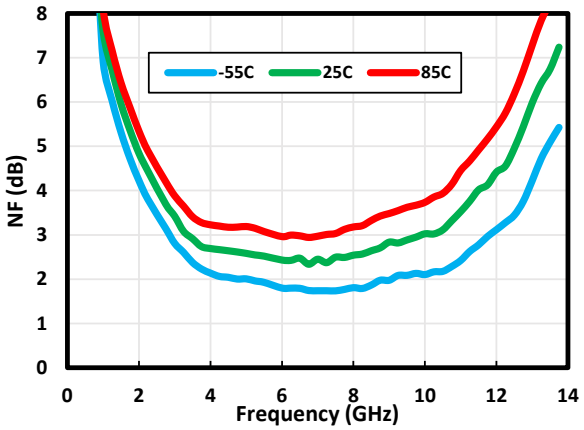

Figure 1-18. NF vs. Temperature at 9V/300 mA

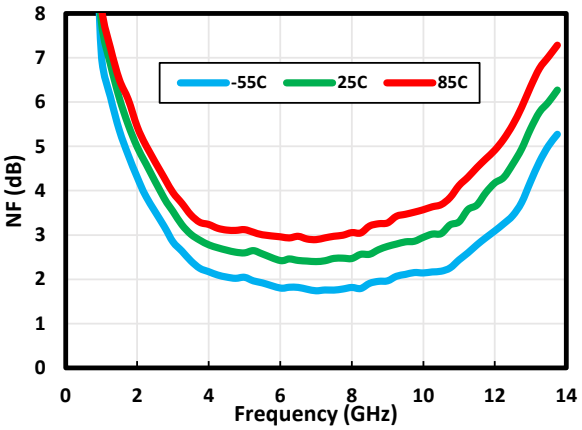

Figure 1-19. NF vs. Temperature at 10V/350 mA

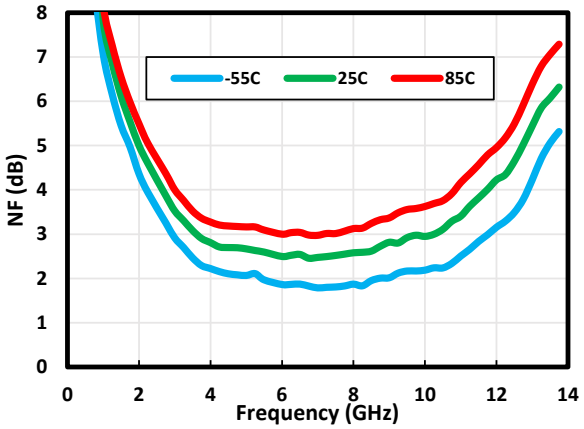

Figure 1-20. NF vs. Temperature at 11V/400 mA

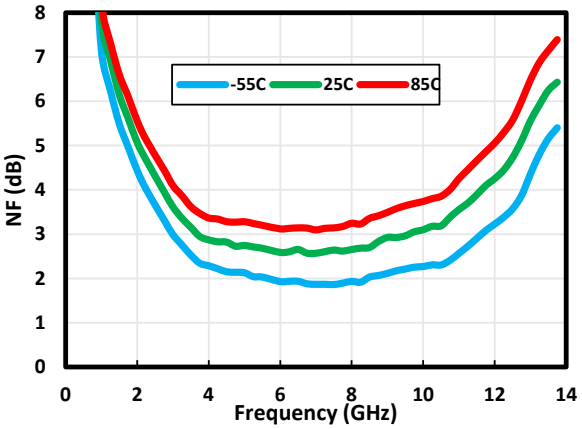

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Figure 1-21. P1dB vs. Temperature at 5V/200 mA

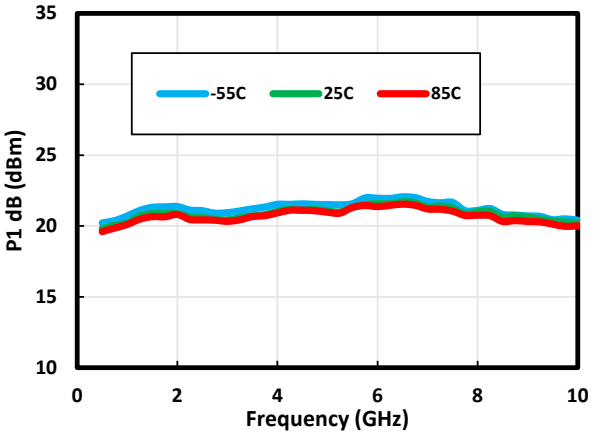

Figure 1-22. P1dB vs. Temperature at 9V/300 mA

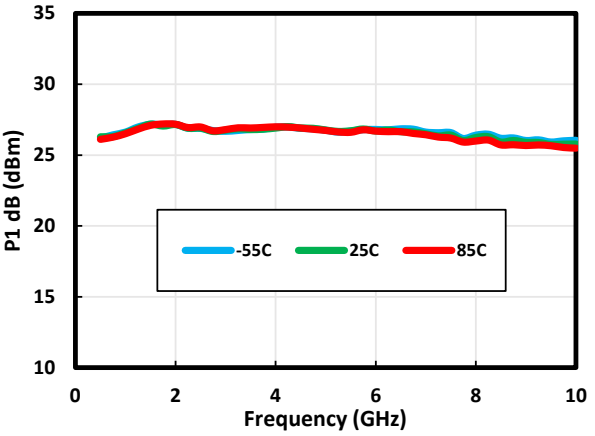

Figure 1-23. P1dB vs. Temperature at 10V/350 mA

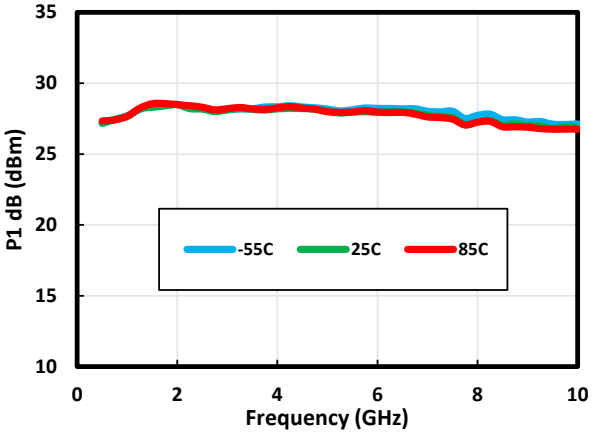

Figure 1-24. P1dB vs. Temperature at 11V/400 mA

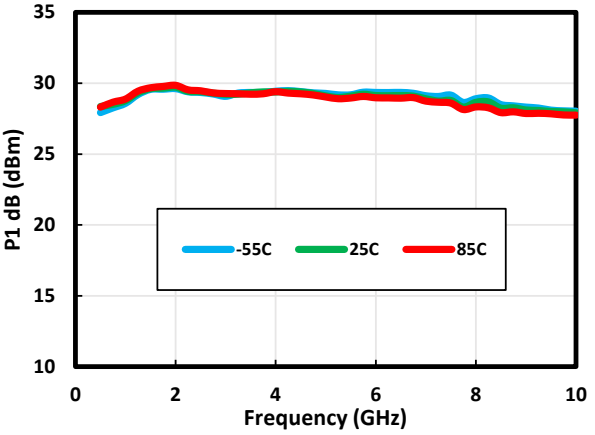

Figure 1-25. P_{sat} vs. Temperature at 5V/200 mA

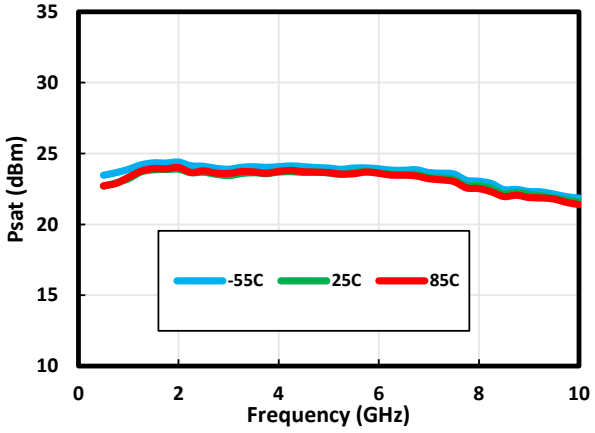

Figure 1-26. P_{sat} vs. Temperature at 9V/300 mA

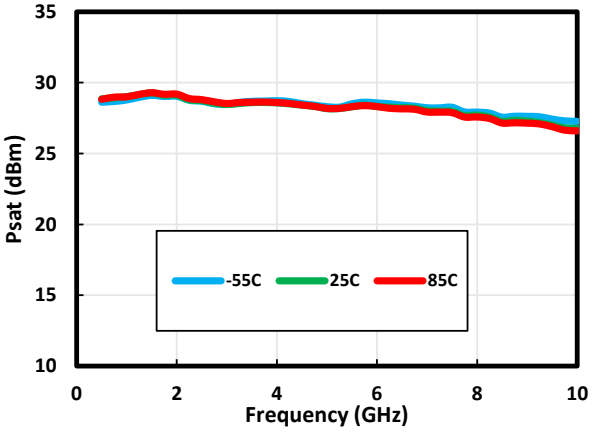

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Figure 1-27. P_{sat} vs. Temperature at 10V/350 mA

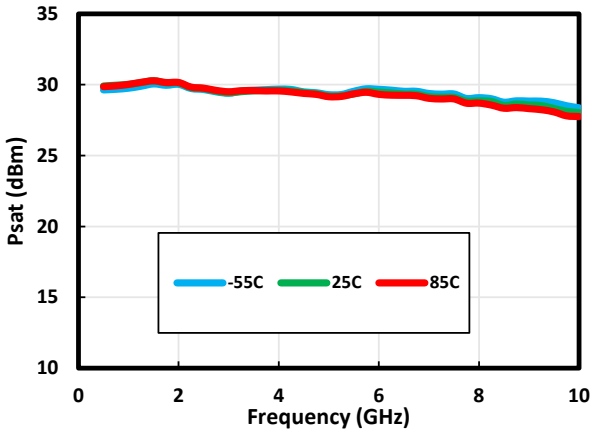

Figure 1-28. P_{sat} vs. Temperature at 11V/400 mA

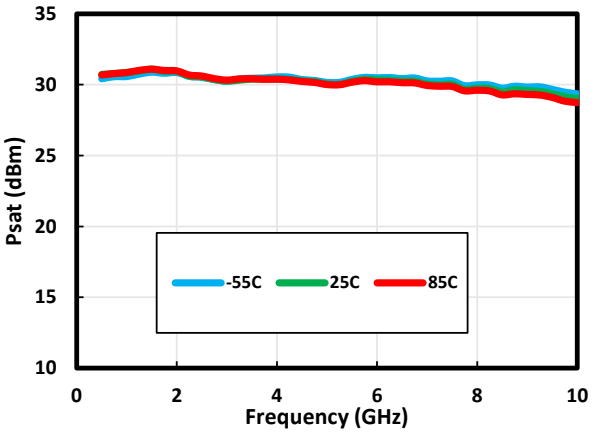

Figure 1-29. OIP3 vs. Temperature at 5V/200 mA

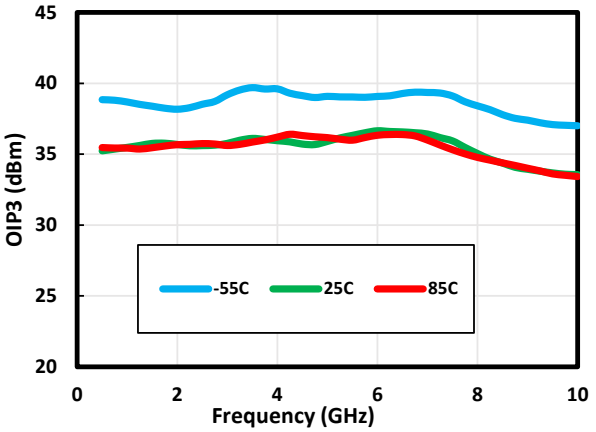

Figure 1-30. OIP3 vs. Temperature at 9V/300 mA

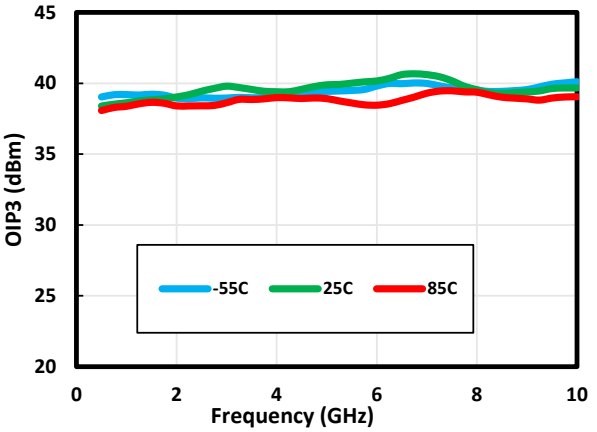

Figure 1-31. OIP3 vs. Temperature at 10V/350 mA

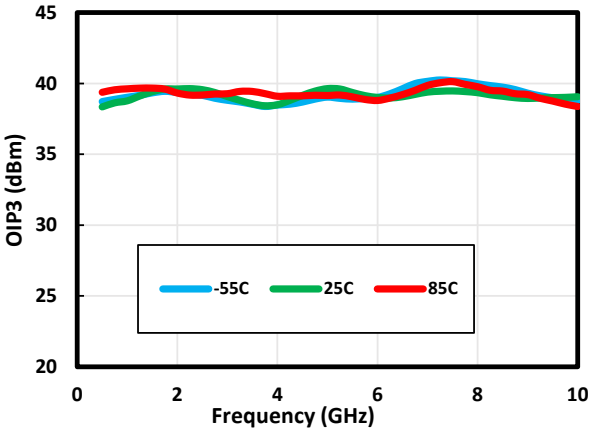

Figure 1-32. OIP3 vs. Temperature at 11V/400 mA

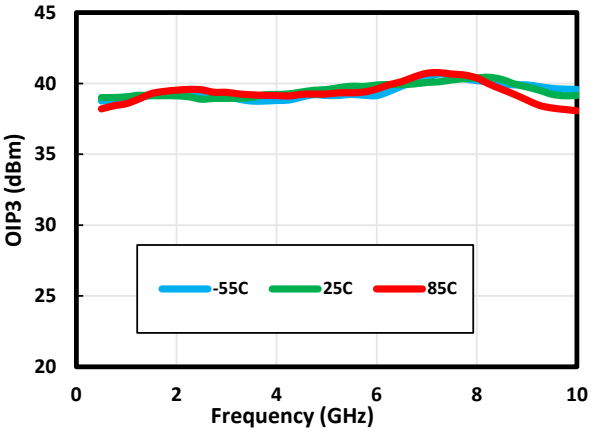

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Figure 1-33. OIP2 vs. Temperature at 5V/200 mA

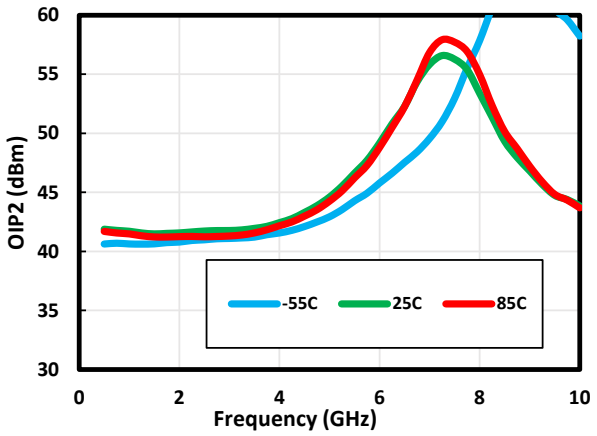

Figure 1-34. OIP2 vs. Temperature at 9V/300 mA

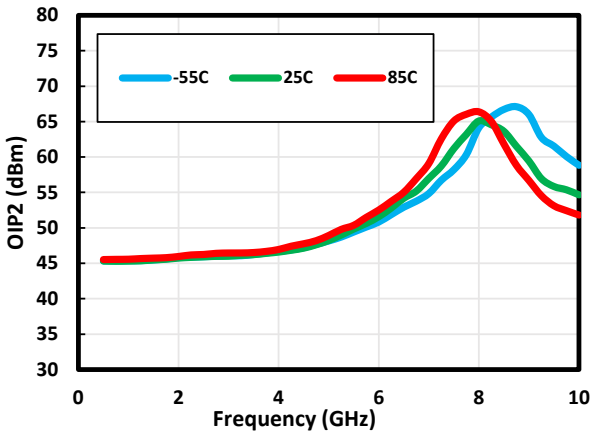

Figure 1-35. OIP2 vs. Temperature at 10V/350 mA

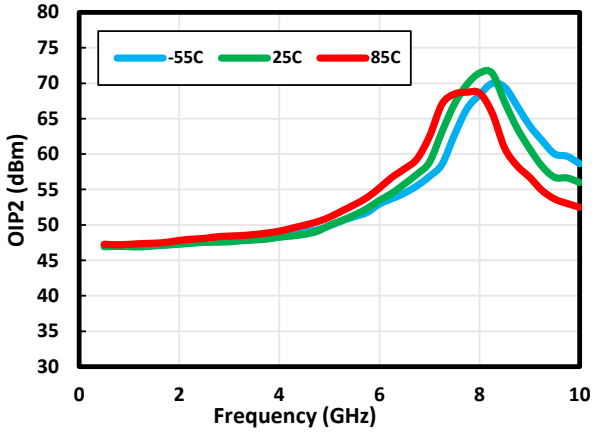

Figure 1-36. OIP2 vs. Temperature at 11V/400 mA

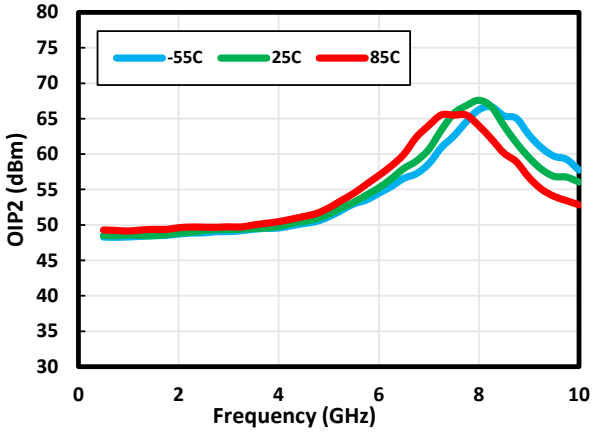

Figure 1-37. IM3 vs. Temperature at 5V/200 mA

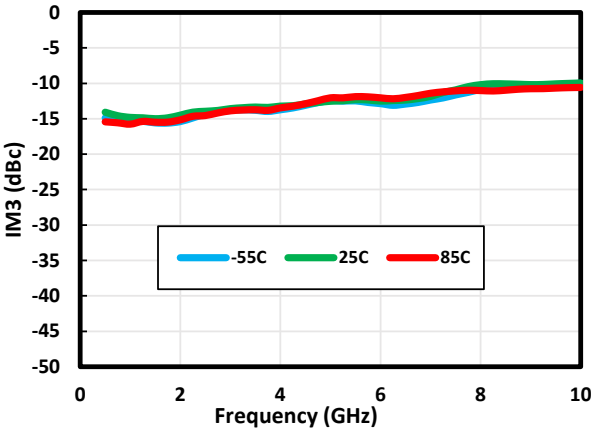

Figure 1-38. IM3 vs. Temperature at 9V/300 mA

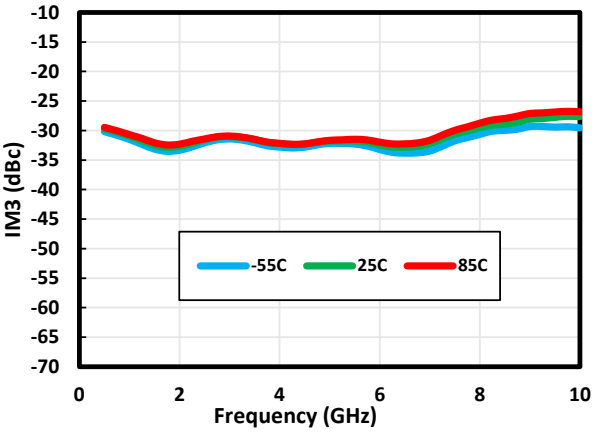

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Figure 1-39. IM3 vs. Temperature at 10V/350 mA

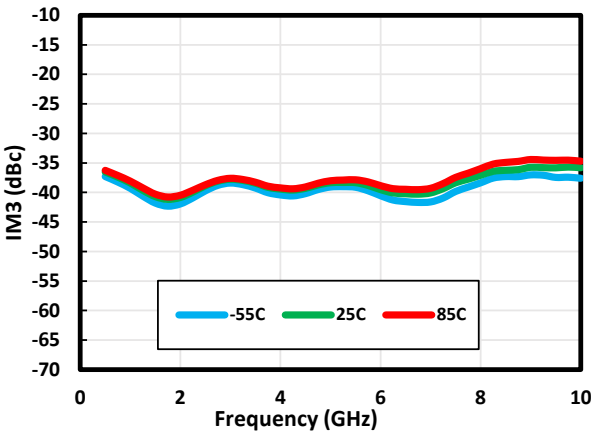
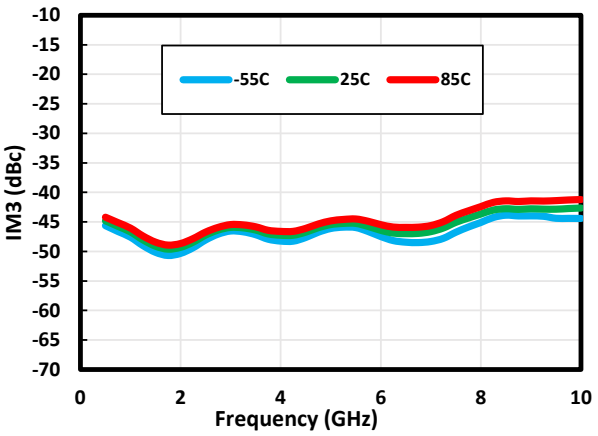


Figure 1-40. IM3 vs. Temperature at 11V/400 mA



1.3.2 Typical Performances vs. Bias

The graphs shown in Figures 1–41 through 1–59 represent the Typical Performance versus Bias curves of the MMA053PP5 under constant temperature of 25 °C. All measurements were taken using the test circuit shown in Figure 3-2.

Figure 1-41. Gain vs. V_{DD} at 200 mA

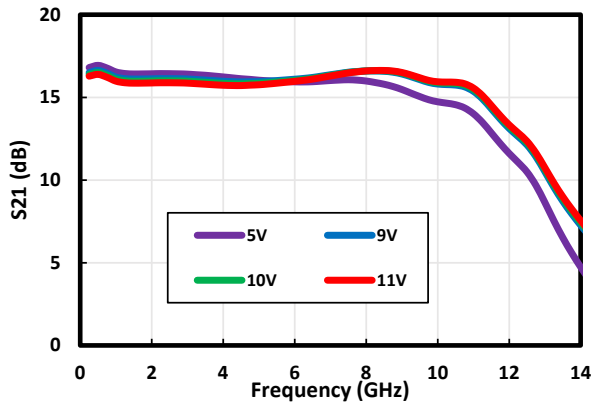


Figure 1-42. Gain vs. V_{DD} at 300 mA

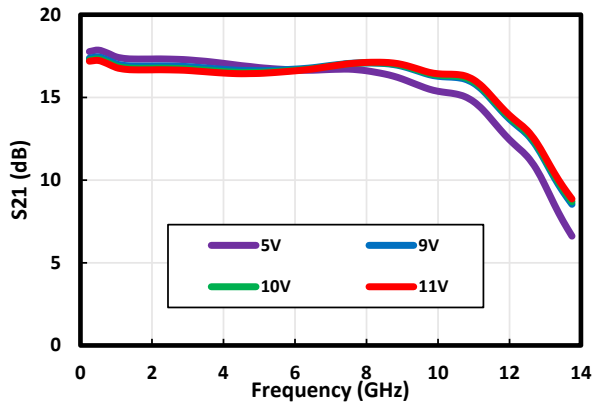


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Figure 1-43. Gain vs. V_{DD} at 350 mA

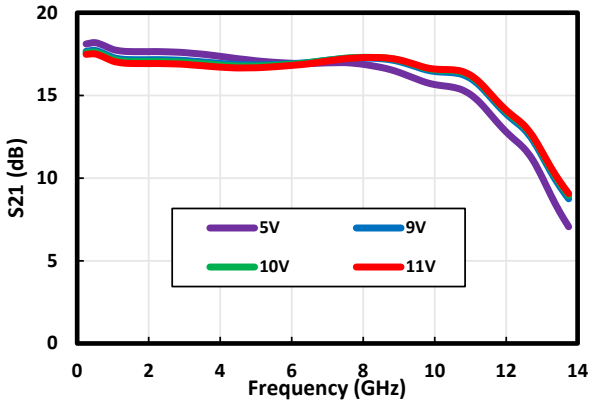

Figure 1-44. Gain vs. V_{DD} at 400 mA

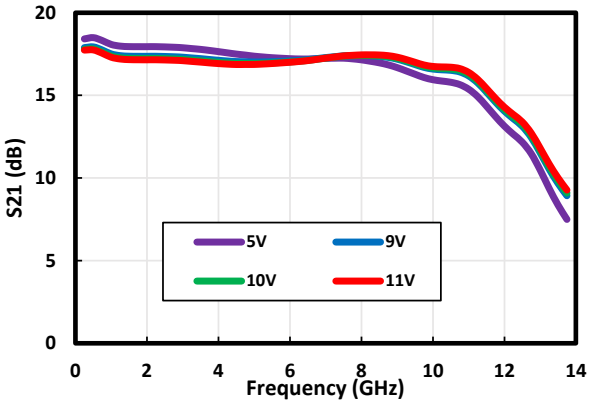

Figure 1-45. NF vs. V_{DD} at 200 mA

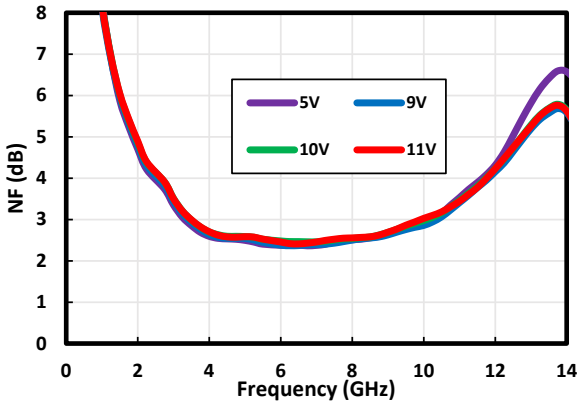

Figure 1-46. NF vs. V_{DD} at 300 mA

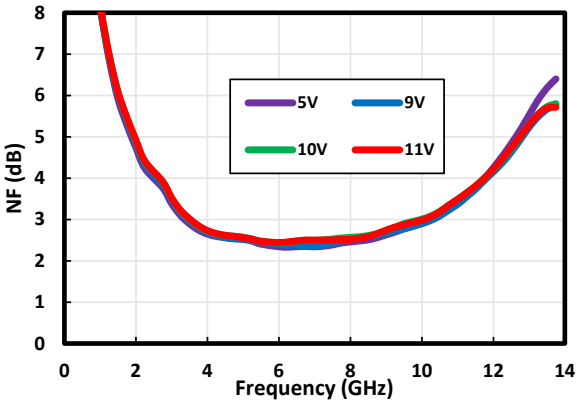

Figure 1-47. NF vs. V_{DD} at 350 mA

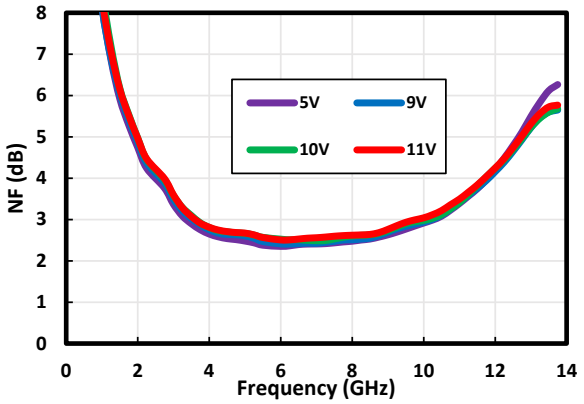

Figure 1-48. NF vs. V_{DD} at 400 mA

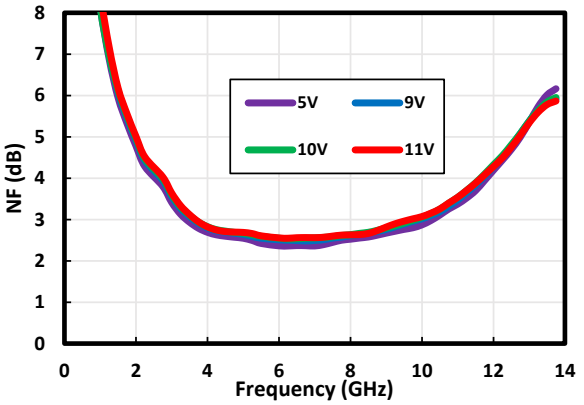

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Figure 1-49. P1dB vs. V_{DD}/I_{DD}

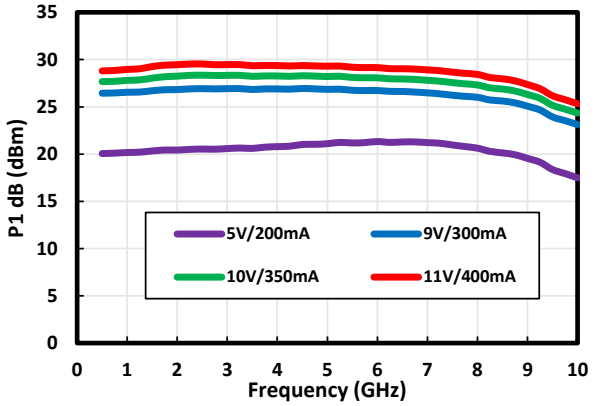


Figure 1-50. P_{sat} vs. V_{DD}/I_{DD}

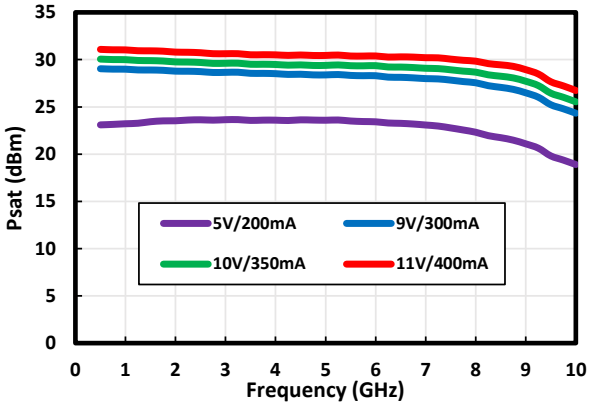


Figure 1-51. OIP3 vs. V_{DD}/I_{DD}

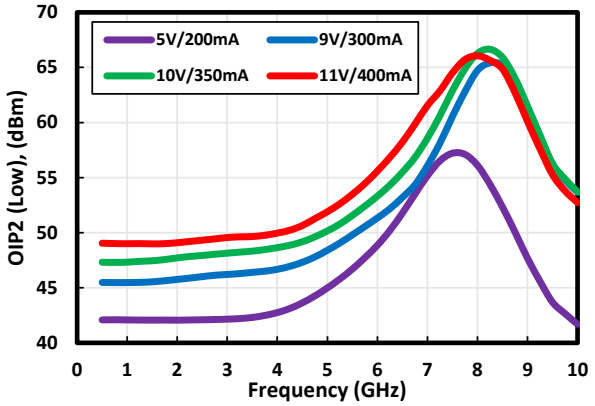


Figure 1-52. OIP2 Low at Δ = 10 MHz vs. V_{DD}/I_{DD}

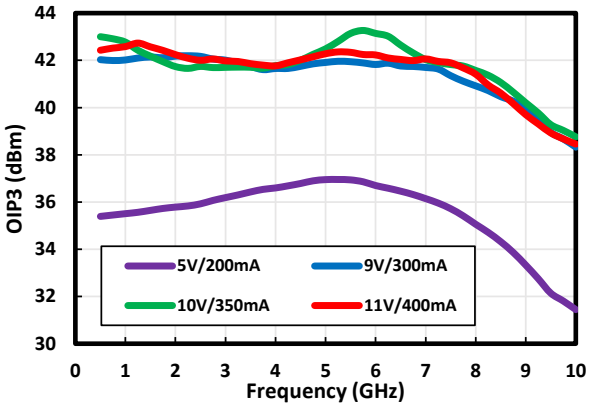
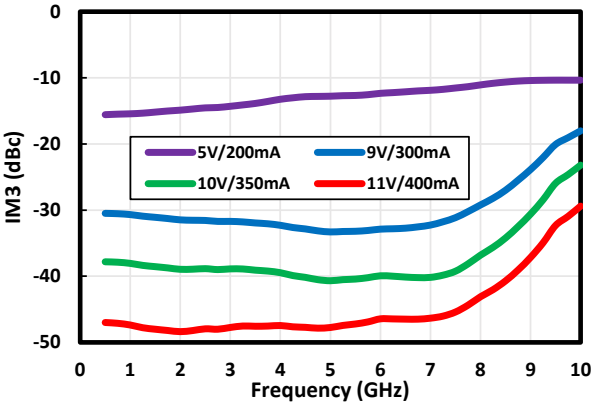


Figure 1-53. IM3 vs. V_{DD}/I_{DD} 20 dBm (per tone)



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1.3.3 Typical Performances vs. Output Power

The graphs shown in Figures 1–54 through 1–66 represent the Typical Performance versus Output power curves of the MMA053PP5 under constant temperature of 25 °C. All measurements were taken using the test circuit shown in Figure 3-2.

Figure 1-54. IM2 vs. Power at 5V/200 mA

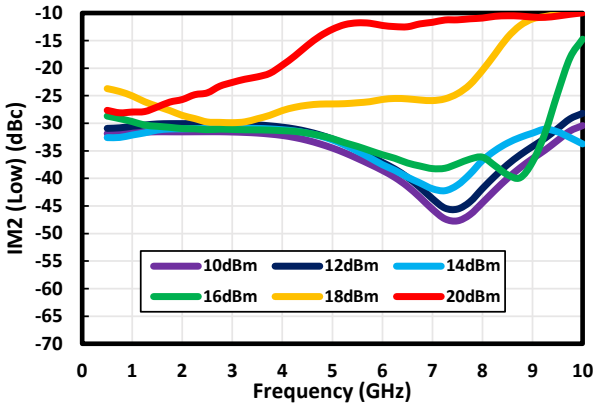

Figure 1-55. IM2 vs. Power at 9V/300 mA

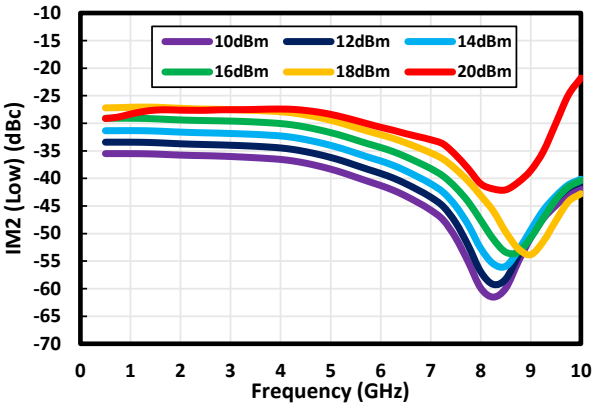

Figure 1-56. IM2 vs. Power at 10V/350 mA

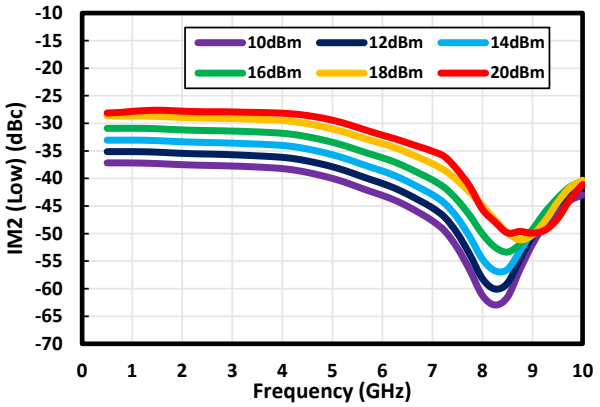

Figure 1-57. IM2 vs. Power at 11V/100 mA

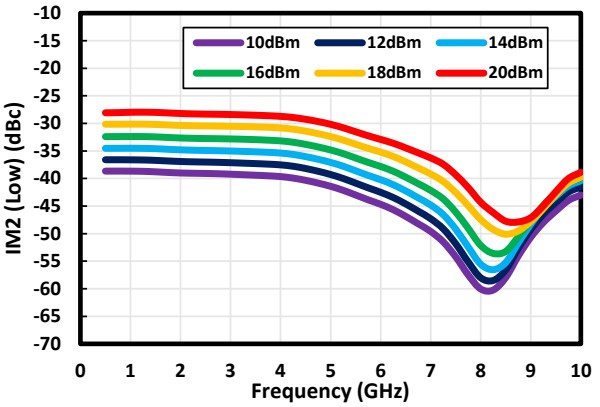

Figure 1-58. IM3 vs. Power at 5V/200 mA

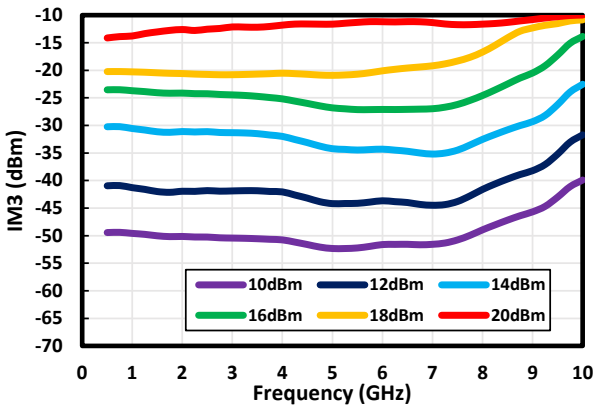

Figure 1-59. IM3 vs. Power at 9V/300 mA

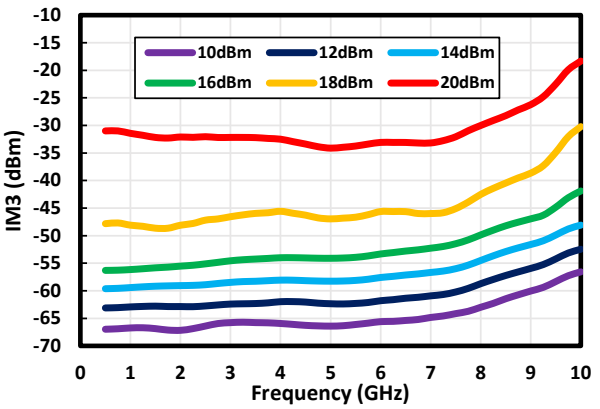

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Figure 1-60. IM3 vs. Power at 10V/350 mA

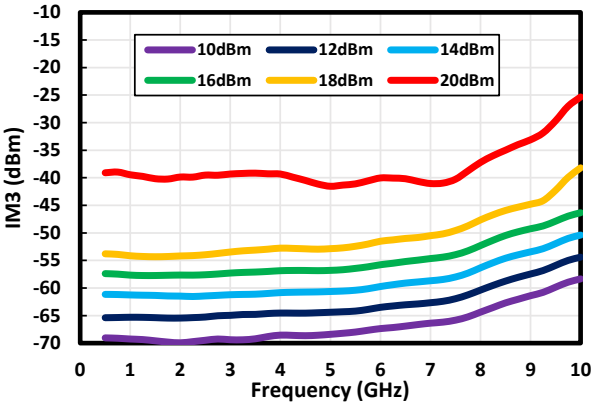

Figure 1-61. IM3 vs. Power at 11V/100 mA

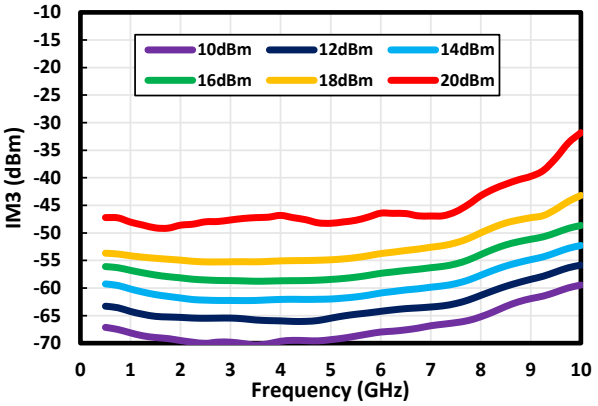

Figure 1-62. 2nd Harmonic vs. Power at 5V/200 mA

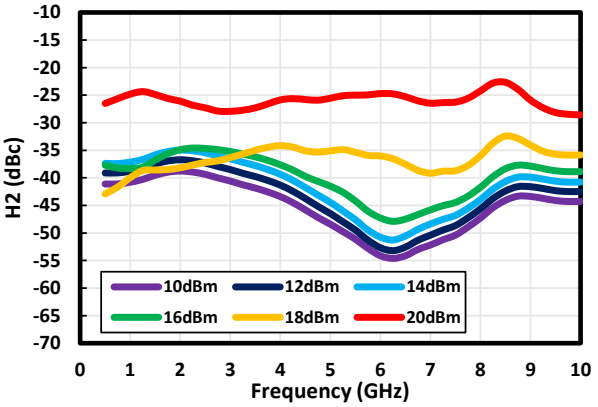

Figure 1-63. 2nd Harmonic vs. Power at 9V/300 mA

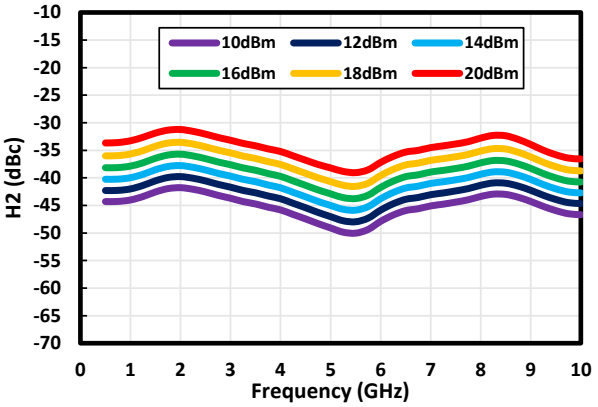

Figure 1-64. 2nd Harmonic vs. Power at 10V/350 mA

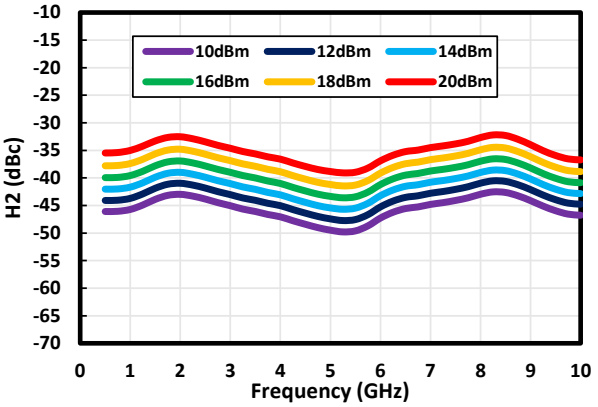

Figure 1-65. 2nd Harmonic vs. Power at 11V/100 mA

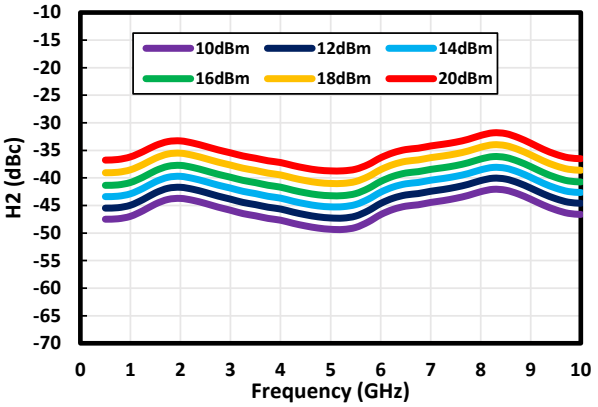

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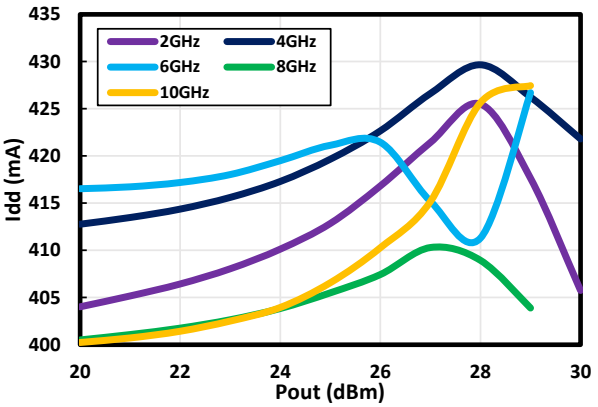
Figure 1-66. I_{DD} Current vs. Power at 11V



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2. Package Specifications

Figure 2–1 shows the package outline of the MMA053PP5 device. Dimensions are in millimeters [inches].

Figure 2-1. Package Outline Drawing (mm[inches])

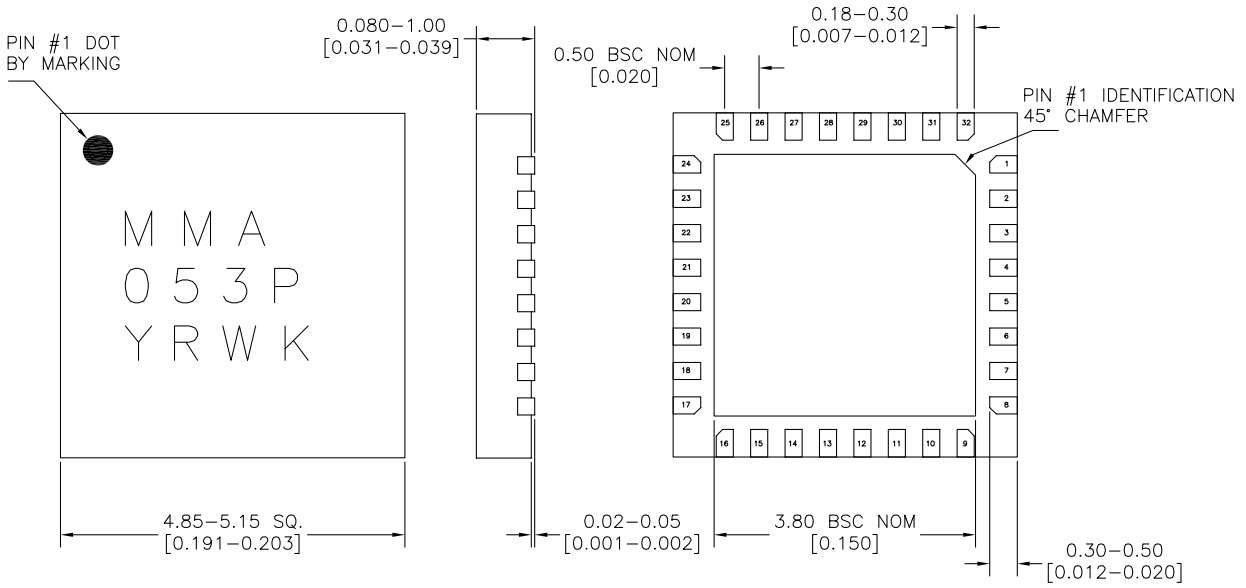

Table 2-1. Package Information

Material	Lead Frame
Package Lead frame	5 mm × 5 mm 32L Plastic QFN C194Cu
Plating	100% matte tin finish
Package body material	RoHS compliant low–stress injection molded plastic

Table 2-2. PIN Description

PIN Number	Pad Name	Pad Description
5	RF_{IN}	DC-coupled to Gate1 and matched to 50Ω.
21	RF_{OUT}	DC-coupled to V_{DD} and matched to 50Ω. V_{DD} should be biased through a Bias Tee
13	V_{G1C}	Gate1 Bias. Adjust to achieve required I_{DD}
15, 16	V_{G1B}, V_{G1A}	Low-frequency termination. Connect bypass capacitors per application circuit below.
2	V_{GG}	Low-frequency termination. Connect bypass capacitors per application circuit below.
29,30	V_{DB}, V_{DA}	DC linked V_{DD} internally. External bypass capacitors are required to extend RF match and gain flatness below 2 GHz.
4, 6, 20, 22, Middle Pad	Ground	Connected to ground per recommended layout
1, 3, 7, 8, 9, 10, 11, 12, 14, 17, 18, 19, 23, 24, 25, 26, 27, 28, 31, 32	N/C	These pins are not connected internally, but they may be connected to external RF/DC Ground on PCB.

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3. Application Circuit

Figure 3-1. Amplifier Functional Schematic

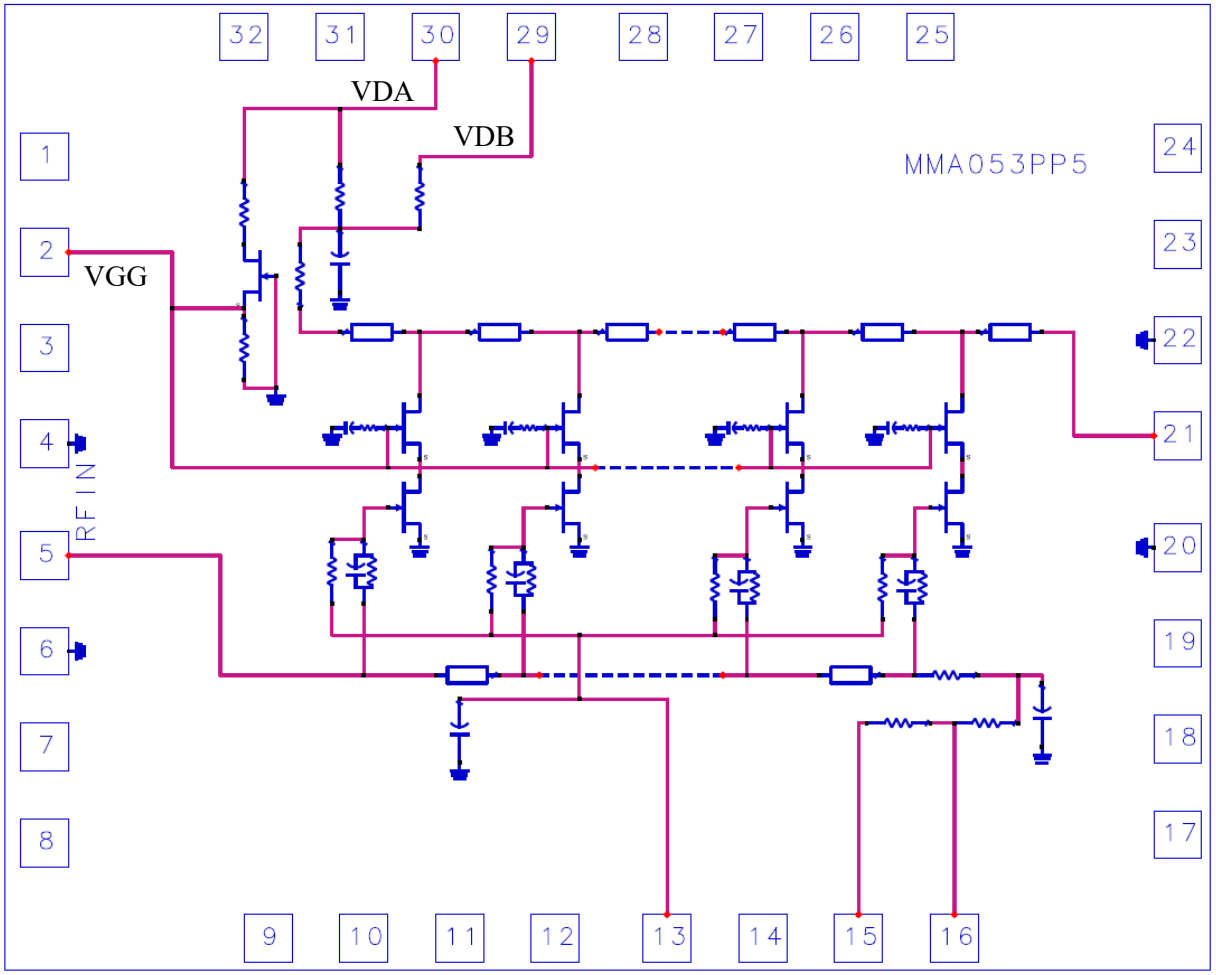

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Figure 3–2 shows the application circuit of the MMA053PP5E device. Note that there is no internal DC blocking capacitor on the input or the output, and a bias tee must be used on pin # 21 for biasing V_{DD}

Figure 3-2. Eval PCB Schematic

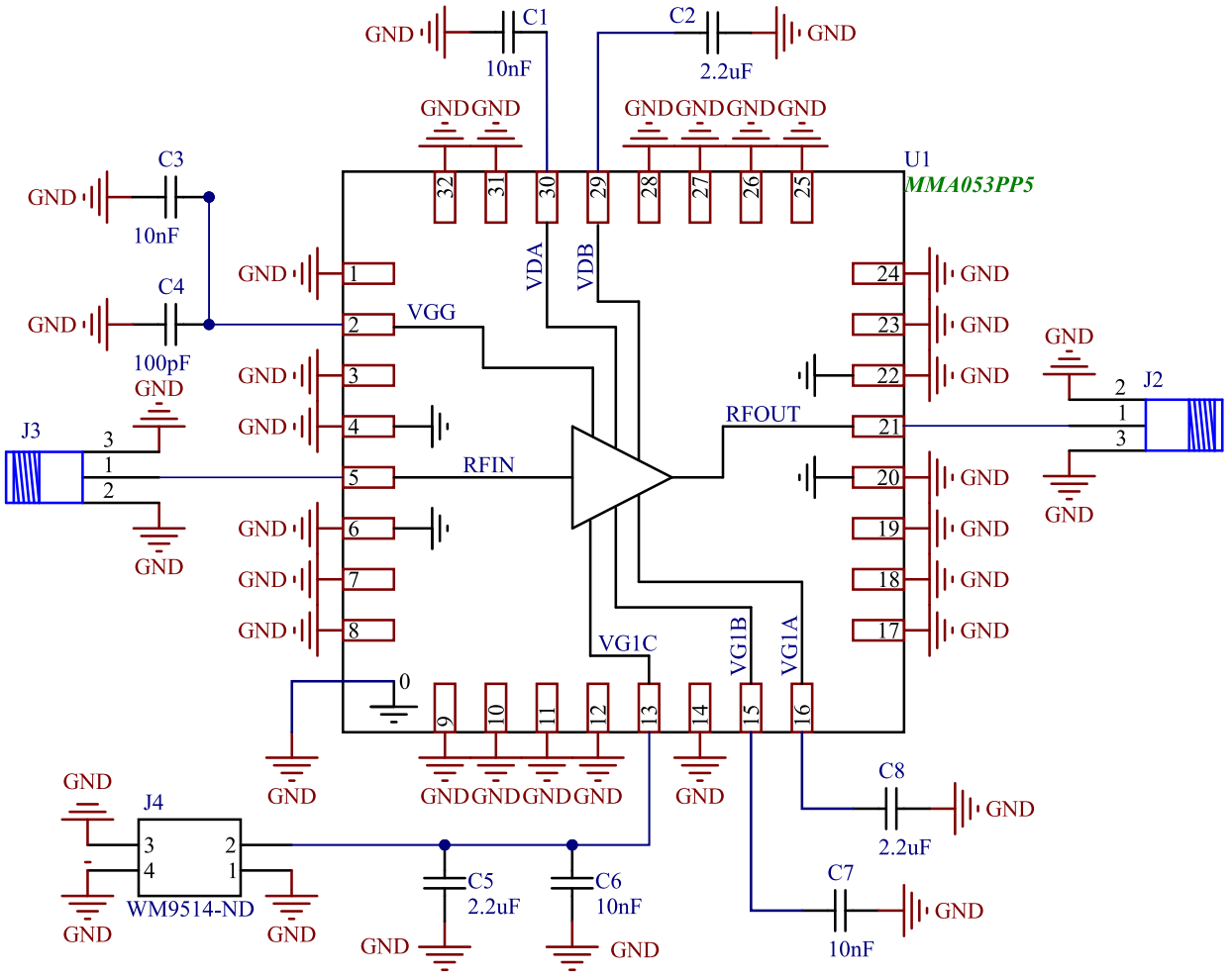

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Figure 3-3. Eval PCB

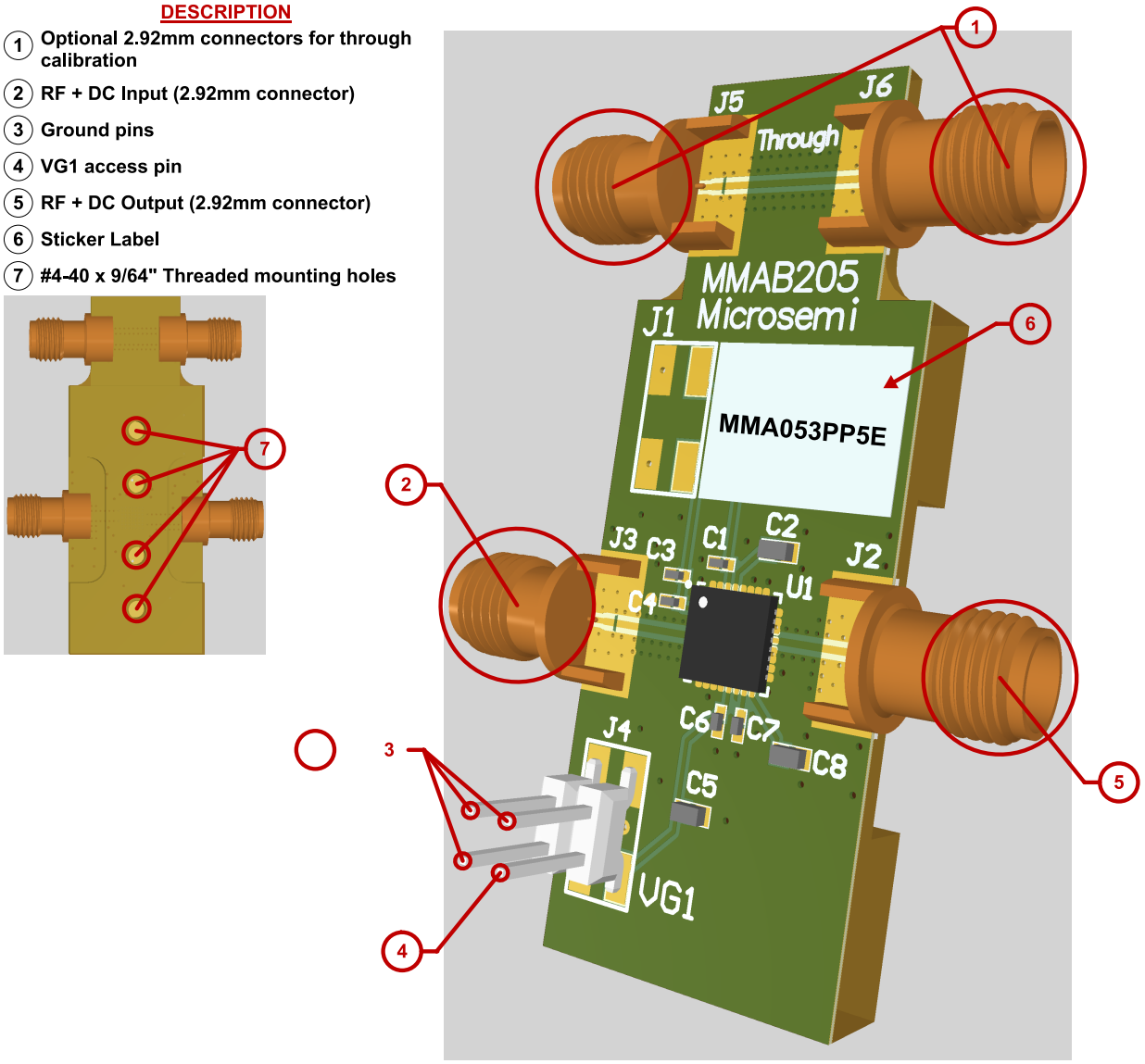

Table 3-1. Bill of Material

Item Num.	Designation	Description	Mnf. Part Num.	Qty.
1	U1	Power amp, QFN 5×5	MMA053PP5	1
2	C1, C3, C6, C7	10000 pF ±10% 50V ceramic capacitor X7R 0402	GRM155R71H103KA88D	4
3	C2, C5, C8	2.2 µF ±10% 16V ceramic capacitor X5R 0603	0603YD225KAT2A	3
4	C4	100 pF ±5% 50V Ceramic Capacitor C0G, NP0 0402	GRM1555C1H101JA01D	1
5	J2, J3, J5, J6	Connector, 2.92 mm jack PCB edge mount .012" pin	145-0701-841	4
6	J4	Header, 2-pin,dual row	15-91-2040	1

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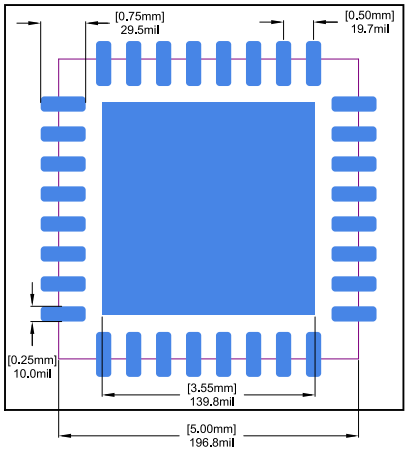
Table 3-2. MMA053PP5E Bias Sequence

Step	Bias Sequence
1	Make sure all DC and RF connections are attached before activating any DC voltage power supplies.
2	Make sure ESD precaution jumper from VG1 to GND on J4 header is removed.
3	DC supply for VDD should be fed through an external bias-T on the RF + DC output port (J2).
	Note: DC supply for VG1 could be attached either through an external bias-T on the RF + DC input port (J3) or through the marked pin on J4.
4	Set VG1 at –1.0V.
5	Set VDD according to your applications plan with current compliance at 520 mA.
6	Power supply sequencing should always be VG1 then VDD (VDD is always last on and first off).
7	Adjust VG1 gradually increasing voltage by 0.01V steps until IDD reaches desired application range.
	Note: If external bias-T used on the RF + DC Output (J2) is showing a very low cut-off frequency, precautions should be made to avoid fast changes of the IDD current otherwise DC spikes, caused by transitions, could exceed the VDD maximum level and damage the part.

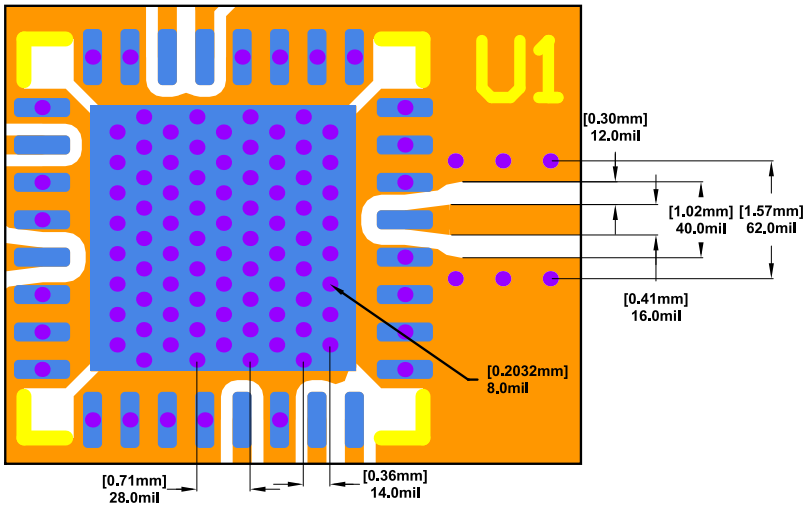
CAUTION Thermal management required. PCB assembly must be mounted on adequate heat-sink via threaded holes found on backside of base-plate (see Figure 3-5).

Figure 3-4. QFN Landing Pattern



Solder mask is coincident with QFN landing.

Figure 3-5. Eval PCB Details



Copper is coincident with QFN landing.

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4. Ordering, Shipping, and Handling

4.1 Handling Recommendations

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microchip application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4.2 Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
MMA053PP5	32 LD 5 mm × 5 mm, plastic QFN–Sn finish
MMA053PP5–NiPdAu	32 LD 5 mm × 5 mm NiPdAu finish
MMA053AA	Bare die (Refer to MMA053AA datasheet)
MMA053PP5E	Evaluation board for MMA053PP5

4.3 Packing Information

Part Number	Description
MMA053PP5/TR	Tape and reel

Note: Contact your Microchip sales representative for the minimum quantity order.

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5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
A	11/2024	Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00005742A, which replaces the previous Microsemi literature number.
Initial release (Microsemi Revision A)	01/2022	Document created.

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