VSC8487 VSC8487-15
Application Note
Migrating from VSC8487 to VSC8487-15



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first release of this document. It was published in July, 2010.

2 Introduction

VSC8487 is a two-channel XAUI to one-channel SFI fail-over PHY that supports both IEEE 802.3ae LAN and IEEE 802.3ae WIS protocols. The SFI/PCS is also enhanced to facilitate 10GBASE-KR capability on the SFI side to operate in backplane applications. At any point in time, data will flow through one channel of XAUI to SFI or vice versa. In addition to all of the features found in VSC8487, VSC8487-15 supports IEEE 1588v2. Hardware differences between VSC8487 and VSC8487-15 are listed in the following section.

This purpose of this document is to assist the customer with migration from VSC8487 to VSC8487-15, or better yet, to design a PCB that can accommodate the VSC8487 today and be upgraded to VSC8487-15 in the future without re-spinning the board.

Note: This document currently focuses on hardware differences. Software differences will exist as well since there will be additional registers dedicated to IEEE 1588v2 support. These differences will be highlighted in a later revision of this document.

3 Hardware Differences

3.1 1588v2 Support

VSC8487-15 supports 1588v2 timestamping. Tasks performed include 1588 frame detection, timestamp appending, header removal, and frame processing. While most of the tasks are self-contained within the PHY, there are some signal pins that are used by the external CPU/FPGA to interface with the 1588 engine inside the VSC8487-15. These are used to output the timestamp information and loading the time value into the PHY.

3.1.1 IEEE 1588v2 Supporting Signal Pins

While the Time of Day (TOD) registers can be written through the MDIO/I2C slave interface, there is a dedicated SPI bus for sending out the timestamps to the external CPU/FPGA if needed for a specific application. In addition, a differential clock of 125 MHz is needed for the 1588 timer, and there is an input pin to load the time and an output pin to test the timer.

- 1588_REFCLKP and 1588_REFCLKN are the 125 MHz differential clock inputs supplied to the local timer.
- 1588_Load/Save is used to synchronously load the time to the PHY.
- 1588_PPS_1 and 1588_PPS_2 are the test pins for the local time counter of the 1588 block.
- SPI_CLK, SPI_DO, and SPI_CS are the three dedicated SPI output pins to the external CPU/FPGA. SPI_CLK is the output clock, SPI_DO is the output data, and SPI_CS is the chip select. These pins are used to output the timestamps only and cannot be used to access other registers of the PHY. MDIO will be used to access the other registers. As a matter of fact, the MDIO could also be used to access the timestamp as well but due to the operating speed of the MDIO, there will be a limitation on how fast the timestamp can be read through MDIO. For faster read out of the timestamp, the SPI bus should be used. The rate of the SPI bus can be set between 10 MHz and 80 MHz.

3.1.2 Pin-out Difference Comparison

Table 1 • Pin Out Difference

Pin Number	VSC8487	VSC8487-15
D8	Reserved	1588_REFCLKP
E8	Reserved	1588_REFCLKN
K7	Reserved	SPI_CLK
L7	Reserved	SPI_DO
L10	MODE2	SI_CS
D5	GPIO_1	1588_Load/Save
D4	GPIO_0	1588_PPS_1
L6	GPIO_11	1588_PPS_2

3.2 Design Considerations

The pins D8, E8, K7, and L7 are labeled as “Reserved” pins in VSC8487, and L10 is labeled as MODE2 which is currently not used in VSC8487. These pins should be left unconnected in a VSC8487-only application. If the VSC8487-15 will ultimately be used in place of the VSC8487 in the same board design, then a 125 MHz differential clock should be provided to 1588_REFCLKP/N (pins D8 and E8) for use as the clock for the 1588 engine. The optional SPI bus (K7, L7, and L10) is used for timestamp read out only. With a SPI of push style, the read out rate could be up to ~1.45M timestamps/s. If MDIO is used, with a standard 2.5 MHz speed, the maximum output rate is ~13.2K timestamps/s. Note that often the page address will need to be changed to read the timestamps, causing four accesses to be made. This will decrease the output rate to ~10K timestamps/s. If a 12 MHz MDIO could be implemented, this results in an output rate of ~48K timestamps/s. The 12 MHz MDIO can be supported by VSC8487-15. However, in order to have the VSC8487-15 support 12 MHz, the load has to be limited by 80 pF and the pull-up has to be 200 Ω.

Interface for Time Stamp Read Out	Rate of Time Stamp Read Out
SPI—80 MHz	~1.45M/s
MDIO—12 MHz	~48K/s
MDIO—2.5 MHz	~10K/s

The 1588_Load/Save (D5), 1588_PPS_1 (D4), and 1588_PPS_2 (L6) pins should be connected to a CPU/FPGA to facilitate the load/save function and time counter check function. The 1588 engine registers are accessible through the MDIO or the slave TWS.

D4, D5, and L6 are three of the 12 GPIO pins available in both VSC8487 and VSC8487-15. Many different functions are multiplexed into these GPIO pins. The user should configure these GPIO pins according to his or her specific application. If the user plans to use some of the GPIO pins as the 1588 support interface to the 1588 engine, there will be three fewer GPIO pins available for use in other functions such as LEDs or I^2C to the SFP+ module. The details on how the GPIO pins are multiplexed to support different functions are listed in the device data sheet.

Note: The locations of the SPI pins multiplexed into the GPIO pins as indicated in the latest version of the device datasheet have been changed from that specified in the VSC8487-15 revision 1.0 datasheet.

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VPPD-02650