

9V Programmable Photoelectric Smoke Detector ASIC

Features

- 6.5-12V Operation
- Low Quiescent Current
- Programmable Internal Infrared Emitter Diode (IRED) Current
- Programmable Standby Alarm Level
- Programmable Hush[®] Alarm Level
- Programmable Hysteresis Alarm Level
- Programmable Chamber Test Alarm Level
- Programmable Low-battery Test
- Programmable Low-battery Hush
- Programmable Horn Pattern
- Horn Synchronization
- 10-year End-of-Life Indication
- Differentiated Chamber Fail and Low-battery Warnings
- Local Alarm Memory
- Interconnect up to 40 Detectors
- I/O Filter and Charge Dump
- Smart I/O for CO alarm Option
- 9-Minute or 80-Second Hush Timer
- Smart Hush[™] Option
- Automatic Alarm Locate for Interconnected Units

Description

The RE46C202 is a next generation low-power CMOS photoelectric-type smoke detector IC. With minimal external components, this circuit will provide all the required features for a photoelectric-type smoke detector.

The design incorporates a gain selectable photo amplifier for use with an infrared emitter/detector pair.

An on-chip oscillator strobes power to the smoke detection circuitry for 5 ms every 10 seconds to keep standby current to a minimum.

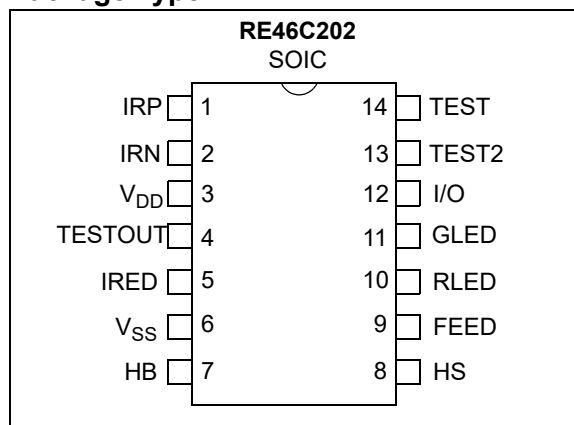
A check for a low-battery condition is performed every 80 seconds, and chamber test is performed once every 320 seconds when in standby. The temporal horn pattern supports the NFPA 72 emergency evacuation signal.

An interconnect pin allows multiple detectors to be connected such that when one unit alarms, all units will sound. A charge dump feature will quickly discharge the interconnect line when exiting a local alarm. The interconnect input is also digitally filtered.

An internal 9-minute or 80-second timer is used for a Hush operation.

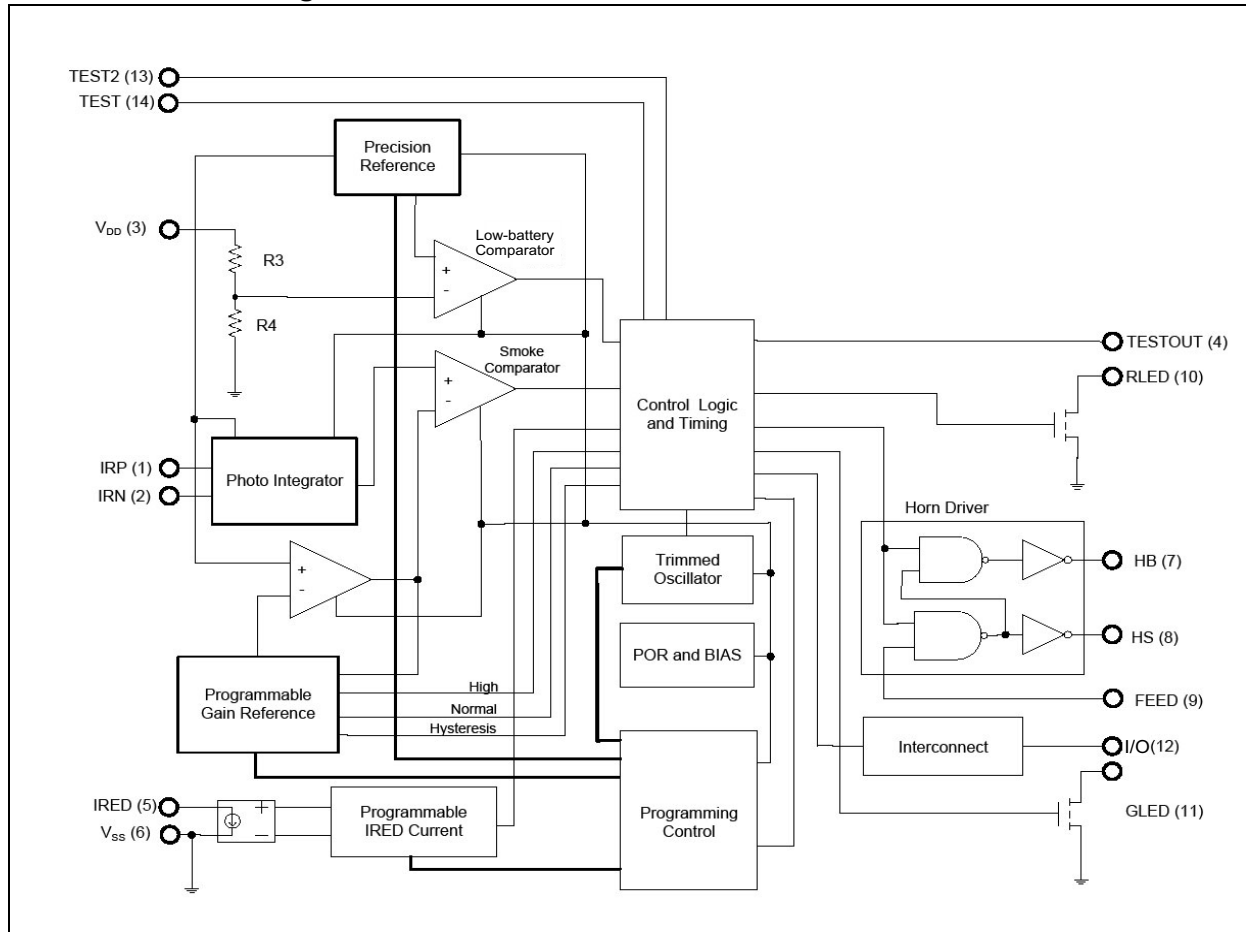
A local alarm memory feature allows the user to determine if the unit has previously entered a local alarm condition.

Package Type

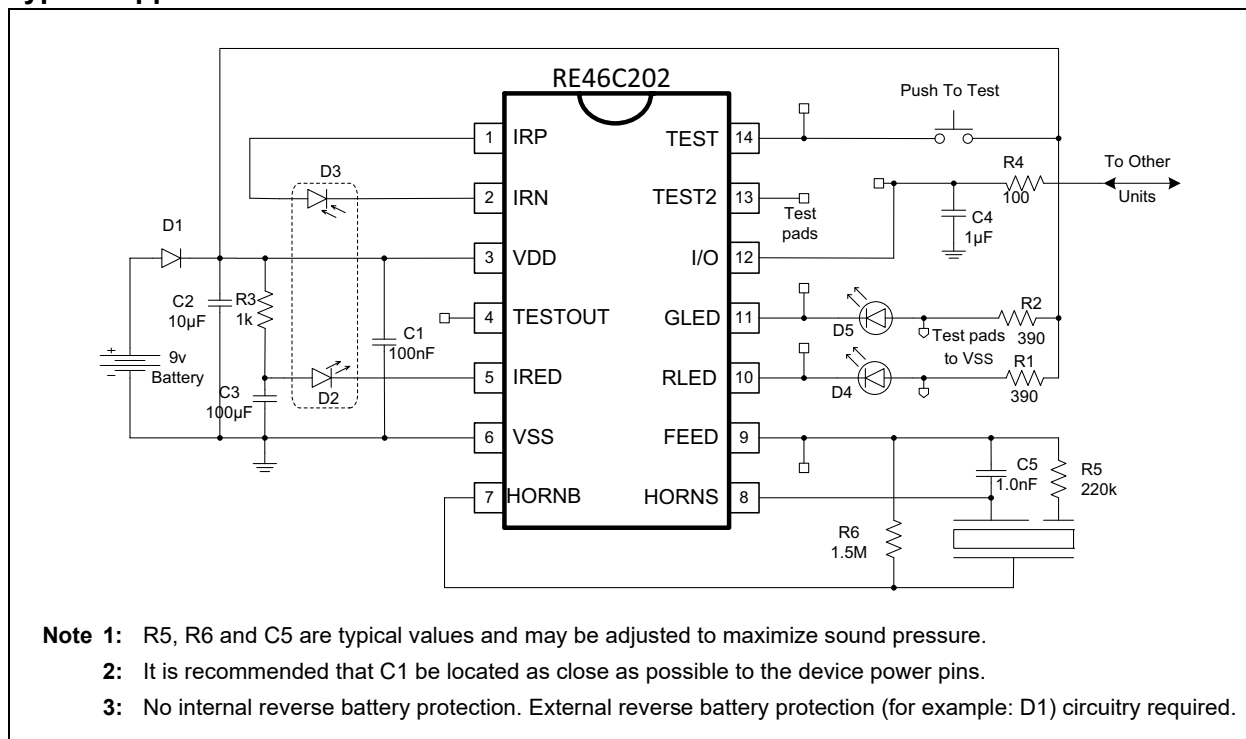


RE46C202

Functional Block Diagram



Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{DD}	12.5V
Voltage Range Except FEED, I/O, IRP, IRN	$V_{IN} = -0.3V$ to $V_{DD} + 0.3V$
FEED Input Voltage Range	$V_{INFD} = -10V$ to 22V
I/O Input Voltage Range.....	$V_{IO1} = -0.3V$ to 15V
IRP/IRN Input Voltage Range	$V_{INIRD} = -0.3V$ to 5.5V
Input Current Except FEED	$I_{IN} = 10$ mA
Storage Temperature	$T_{STG} = -55^{\circ}C$ to $+125^{\circ}C$
Maximum Junction Temperature	$T_J = +150^{\circ}C$
MM ESD.....	150V

Note: †**Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at $T_A = -10^{\circ}C$ to $+60^{\circ}C$, $V_{DD} = 9V$, $V_{SS} = 0V$ (**Note 1**)

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	3	6.5	—	12	V	Operating
Supply Current	I_{DD}	3	—	0.9	1.5	μA	Standby
Input Leakage	I_{INOP}	1	-200	—	200	pA	IRP = 5V or V_{SS}
		2	-200	—	200	pA	IRN = 5V or V_{SS}
	I_{HFD1}	9	—	20	50	μA	FEED = 22V
	I_{ILFD1}	9	-50	-15	—	μA	FEED = -10V
Input Voltage Low	V_{IL1}	9	—	—	2.7	V	FEED
	V_{IL2}	12	—	—	1	V	No local alarm, I/O as an input
	V_{IL3}	13, 14	—	—	3.4	V	TEST or TEST2
Input Voltage High	V_{IH1}	9	6.2	—	—	V	FEED, $V_{BST} = 9V$
	V_{IH2}	12	3.0	—	—	V	No local alarm, I/O as an input
	V_{IL3}	13, 14	5.6	—	—	V	TEST or TEST2
Input Pull Down Current	I_{PD1}	13, 14	20	50	80	μA	$V_{IN} = V_{DD}$
Output Voltage High	V_{OH1}	7, 8	5.5	—	—	V	$I_{OH} = -16$ mA, $V_{DD} = 6.5V$
Output Voltage Low	V_{OL1}	7, 8	—	—	1	V	$I_{OL} = 16$ mA, $V_{DD} = 6.5V$
	V_{OL2}	10, 11	—	—	0.6	V	$I_{OL} = 10$ mA, $V_{DD} = 6.5V$
Output Off Leakage High	I_{IOHZ}	10, 11	—	—	1	μA	Outputs Off, $V_{IN} = V_{DD}$

Note 1: Production tested at room temperature with temperature guard-banded limits.

2: Not production tested.

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DC ELECTRICAL CHARACTERISTICS (CONTINUED)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at $T_A = -10^{\circ}\text{C}$ to $+60^{\circ}\text{C}$, $V_{DD} = 9\text{V}$, $V_{SS} = 0\text{V}$ (**Note 1**)

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Output Current	I_{IOL1}	12	20	50	80	μA	$V_{IN} = V_{DD}$
	I_{IOL2}	12	—	—	150	μA	$V_{IN} = 15\text{V}$
	I_{IOH1}	12	-4	—	-16	mA	Alarm, $V_{IO} = 4\text{V}$ or $V_{IO} = 0\text{V}$
	I_{IODMP}	12	5	—	—	mA	At Conclusion of Local Alarm or Test, $V_{IO} = 1\text{V}$
	I_{IRED50}	5	45	50	55	mA	IRED on, $V_{IRED} = 1.5\text{V}$, (50 mA option selected; $T_A = +27^{\circ}\text{C}$)
	$I_{IRED100}$	5	90	100	110	mA	IRED on, $V_{IRED} = 1.5\text{V}$, (100 mA option selected; $T_A = +27^{\circ}\text{C}$)
	$I_{IRED150}$	5	135	150	165	mA	IRED on, $V_{IRED} = 1.5\text{V}$, (150 mA option selected, $T_A = +27^{\circ}\text{C}$)
	$I_{IRED200}$	5	180	200	220	mA	IRED on, $V_{IRED} = 1.5\text{V}$, (200 mA option selected, $T_A = +27^{\circ}\text{C}$)
IRED Temperature Coefficient	T_{CIRED}	5	—	0.5	—	$\%/^{\circ}\text{C}$	IRED Output Current Note 2
Low-battery Alarm Voltage	V_{LB}	3	6.75	6.9	7.05	V	6.9V setting
			7.05	7.2	7.35	V	7.2V setting
			7.35	7.5	7.65	V	7.5V setting
			7.65	7.8	7.95	V	7.8V setting

Note 1: Production tested at room temperature with temperature guard-banded limits.

2: Not production tested.

AC ELECTRICAL CHARACTERISTICS

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at $T_A = -10^{\circ}\text{C}$ to $+60^{\circ}\text{C}$, $V_{DD} = 9\text{V}$, $V_{SS} = 0\text{V}$.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Time Base							
Oscillator Period	T_{POSC}	—	593	625	657	μs	Operating Note 2
Oscillator Pulse Width	T_{PW}	—	296	312	329	μs	Operating
Oscillator Tolerance	T_{TOL}	—	-5%	0	5%	%	Operating
Clock Period	T_{PCLK}	—	9.5	10	10.5	ms	Operating

Note 1: Typical values are for design information and not verified.

2: TPOSC is 100% production tested. All other timing is verified by functional testing.

3: See timing diagram for CO alarm horn pattern.

4: See timing diagram for temporal and continuous horn pattern.

5: See timing diagram for horn synchronization and AAL.

6: These conditions apply to alarm memory operation.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at $T_A = -10^{\circ}\text{C}$ to $+60^{\circ}\text{C}$, $V_{DD} = 9\text{V}$, $V_{SS} = 0\text{V}$.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
RLED Indicator							
LED On Time	T _{ON1}	10	9.5	10	10.5	ms	Operating, LBSEL = 0
	T _{ON2}	10	2.37	2.5	2.63	ms	Operating, LBSEL = 1
LED Off Time	T _{LOF1}	10	304	320	336	s	Standby, No Alarm
	T _{LOF2}	10	0.94	0.99	1.04	s	Local Alarm Condition
	T _{LOF3}	10	9.5	10	10.5	s	Timer Mode, No Local Alarm
LED Period	T _{PLED0}	10	LED IS NOT ON				Remote Alarm Only
	T _{PLED1}	10	304	320	336	s	Standby, No Alarm
	T _{PLED2}	10	0.95	1	1.05	s	Local Alarm Condition
	T _{PLED3}	10	9.5	10	10.5	s	Hush Mode, No Local Alarm
GLED Indicator							
Sink Driver On Time	T _{ON4}	11	237	250	263	ms	Operating
Sink Driver Off Time	T _{OFLED1}	11	712	750	788	ms	Sink Driver Pulse Train (3x) Off Time Note 6
	T _{OFLED2}	11	35.8	37.8	39.6	s	Sink Driver Off Time Between Pulse Train (3x) Note 6
	T _{LOF4}	11	237	250	263	ms	Alarm Memory Indication in PTT
Sink Driver Period	T _{PLED4}	11	475	500	525	ms	Alarm Memory Indication in PTT
	T _{PLED5}	11	38	40	42	s	Sink Driver Timer Set Note 6
Alarm Memory Indication Time-out Period	T _{AMTO}	11	22.8	24	25.2	Hours	Alarm Memory Set, AMTO<2:1> = 00
			45.6	48	50.4	Hours	Alarm Memory Set, AMTO<2:1> = 01
			0	0	0	—	AMTO<2:1> = 10, No Alarm Memory Indication
			∞	∞	∞	—	Alarm Memory Set, AMTO<2:1> = 11
Smoke Check							
Smoke Test Period IRED	T _{STPER0}	4,5	9.5	10	10.5	s	Standby, No Alarm
	T _{STPER1}	4,5	0.95	1	1.05	s	Standby, one or more Valid Smoke Samples
	T _{STPER2}	4,5	237	250	263	ms	Push Button Test, Not in alarm
	T _{STPER3}	4,5	0.95	1	1.05	s	Local Alarm (three consecutive Valid Smoke Samples)
	T _{STPER4}	4,5	9.5	10	10.5	s	In Remote Alarm
Chamber Test Period	T _{PCT1}	4,5	304	320	336	s	Chamber Test, No Alarm

Note 1: Typical values are for design information and not verified.

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3: See timing diagram for CO alarm horn pattern.

4: See timing diagram for temporal and continuous horn pattern.

5: See timing diagram for horn synchronization and AAL.

6: These conditions apply to alarm memory operation.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at $T_A = -10^{\circ}\text{C}$ to $+60^{\circ}\text{C}$, $V_{DD} = 9\text{V}$, $V_{SS} = 0\text{V}$.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
IRED On Time	T_{IRON1}	5	—	110	—	μs	Operating/DIAG Note 1
	T_{IRON2}	5	—	220	—	μs	Operating/DIAG Note 1
	T_{IRON3}	5	—	330	—	μs	Operating/DIAG Note 1
	T_{IRON4}	5	—	440	—	μs	Operating/DIAG Note 1
Low Battery							
Low-battery Check Period	T_{PLB1}	—	76	80	84	s	Standby, no alarm, RLED off
	T_{PLB2}	—	304	320	336	s	Standby, no alarm, RLED on
Horn Operation							
Horn Startup Delay	T_{HDLY1}	7,8	475	500	525	ms	From local alarm to horn active, temporal horn pattern
Horn Period	T_{HPER1}	7,8	38	40	42	s	Low Battery, No Alarm
	T_{HPER2}	7,8	38	40	42	s	Chamber Fail, No Alarm
	T_{HPER3}	7,8	237	250	263	ms	Alarm Memory Active, Push-to-Test
	T_{HPER4}	7,8	5.5	5.8	6.1	s	CO Alarm Horn Period Note 3
	T_{HPER6}	7,8	3.8	4	4.2	s	Operating, Alarm Condition, Temporal Horn Pattern Note 4
Horn On Time	T_{HON1}	7,8	9.5	10	10.5	ms	Low-battery or Fail Chamber Test, No Alarm or Optional PTT in Alarm Memory
	T_{HON2}	7,8	475	500	525	ms	Operating, Alarm Condition, Temporal Horn Pattern Note 4
	T_{HON4}	7,8	95	100	105	ms	CO alarm Note 3
Horn Off Time	T_{HOF1}	7,8	475	500	525	ms	Operating, Alarm Condition, Temporal Horn Pattern Note 4
	T_{HOF2}	7,8	1.43	1.5	1.58	s	Operating, Alarm Condition, Temporal Horn Pattern Note 4
	T_{HOF3}	7,8	143	150	158	ms	Operating, Alarm Condition, Continuous Horn Pattern Note 4
	T_{HOF4}	7,8	37	39	41	s	Chamber Fail Horn Off Time
	T_{HOF5}	7,8	466	490	515	ms	Chamber Fail Horn Pulse Train Off Time
	T_{HOF6}	7,8	95	100	105	ms	CO Alarm Horn Off Time Between Pulses Note 3
	T_{HOF7}	7,8	4.8	5.1	5.4	s	CO Alarm Horn Off Time Between Pulses Trains Note 3
	T_{HOF8}	7,8	38	40	42	s	Low Battery, No Alarm
	T_{HOF9}	7,8	228	240	252	ms	Alarm Memory, Indication in PTT

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4: See timing diagram for temporal and continuous horn pattern.

5: See timing diagram for horn synchronization and AAL.

6: These conditions apply to alarm memory operation.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at $T_A = -10^{\circ}\text{C}$ to $+60^{\circ}\text{C}$, $V_{DD} = 9\text{V}$, $V_{SS} = 0\text{V}$.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Hush Timer Operation							
Hush Timer Period	T _{TPER}	—	8.5	9	9.5	Min	9 minute Option No Alarm Condition
		—	76	80	84	s	>1 minute Option No Alarm Condition
EOL (End-of-Life)							
End-of-Life Sample Period	T _{EOLPER}	—	346	364	382	Hours	Standby, No Alarms
End-of-Life (Time-out)	T _{EOLTO}	—	9.5	10	10.5	Years	Standby, No Alarms, Time to EOL Warning
Interconnect							
I/O Active Delay	T _{IODLY1}	12	2.8	3	3.2	s	Local Alarm Start to I/O Active
Remote Alarm Delay	T _{IODLY2}	12	0.77	0.81	0.86	s	Temporal Horn Pattern, No Local Alarm, I/O Active to Alarm
I/O Filter	T _{IOFILT}	12	—	—	290	ms	I/O Pulse Width Filtered
I/O Pulse On Time for CO Alarm	T _{IOPW1}	12	23	—	290	ms	No Local Alarm, Two Valid Pulses Required for CO
I/O Pulse Off Time for CO Alarm	T _{IOTO1}	12	—	—	5.4	s	I/O = Low
I/O Charge Dump Duration	T _{IODMP}	12	1.9	2.0	2.1	s	At Conclusion of Local Alarm or Test
Horn Synchronization							
I/O Pulse Period	T _{PIO1}	12	3.8	4	4.2	s	Local Alarm, Temporal Horn Pattern, SyncEn = 1 Note 5
I/O Pulse On Time	T _{ONIO}	12	3.41	3.59	3.77	s	Local Alarm, Temporal Horn Pattern, SyncEn = 1 Note 5
Horn Sync I/O Dump	T _{IODMP2}	12	95	100	105	ms	Local Alarm, SyncEn = 1, I/O Dump Active Note 4
Horn Sync I/O Dump Delay	T _{IODLY4}	12	285	300	315	ms	Local Alarm, SyncEn = 1 Note 5
Horn Sync Contention Window	T _{IOCW}	12	294	310	326	ms	Local Alarm, SyncEn = 1, I/O = 0, No I/O Dump, I/O Pull-down Note 5
Auto Alarm Locate (AAL)							
I/O Cycle Period	T _{PIO2}	12	15.2	16	16.8	s	Local Alarm, Temporal Horn Pattern, SyncEn = 1, NoAAL = 0 Note 5

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6: These conditions apply to alarm memory operation.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at $T_A = -10^{\circ}\text{C}$ to $+60^{\circ}\text{C}$, $V_{DD} = 9\text{V}$, $V_{SS} = 0\text{V}$.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
I/O Cycle Off Time	T_{OFIO}	12	4.19	4.41	4.63	s	Local Alarm, Temporal Horn Pattern, SyncEn = 1, NoAAL = 0, I/O Off Time between I/O Pulse Trains (3x) Note 5
Test Mode							
Input Pulse Width in Test Modes	T_{TMPW}	9, 12	10	—	—	μs	Input Pulse Width, High or Low
		13, 14		—	—		Inputs FEED, I/O, TEST2, TEST
Data Setup Time In Serial Read/Write Modes	T_{TMSU}	9, 14	10	—	—	μs	Data (TEST) Setup Time Before CLK (FEED) in TM1/3/19
Data Hold Time In Serial Read/Write Modes	T_{TMH}	9, 14	10	—	—	μs	Data (TEST) Hold Time before CLK (FEED) in TM1/3/19
Clock Period In Serial Read/Write Modes	T_{TMP}	9	30	—	—	μs	CLK (FEED) in TM1/3, with Minimum Pulse Width, Setup and Hold Times
Programming Pulse Width	T_{PROG}	12	10	—	20	ms	I/O high in TM1/3/11/15/19
Detection Enable Pulse Width	T_{DETPW}	9	2	—	—	ms	Detection Enable (FEED) High for Full Detection in TM4-7/10/12-15
Detection Enable Setup	T_{DETSU}	9	2	—	—	ms	Detection Enable (FEED) Low before Enabling Detection Measurement in TM4-7/10/12-15

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TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated.						
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-10	—	+60	$^{\circ}\text{C}$	—
Storage Temperature Range	T_{STG}	-55	—	+125	$^{\circ}\text{C}$	—
Thermal Package Resistance						
Thermal Resistance, 14L-SOIC (150 mil.)	θ_{JA}	—	90.8	—	$^{\circ}\text{C/W}$	—

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

RE46C202 SOIC	Symbol	Function
1	IRP	The anode input for the smoke chamber photo diode.
2	IRN	The cathode input for the smoke chamber photo diode.
3	V _{DD}	Connect to the positive supply voltage.
4	TESTOUT	This output is an indicator of the internal I/O dump and smoke test signals. This pin is also used for test modes.
5	IREDD	This current driver sinks a controlled pulsed current from the Infrared Emitting Diode during a smoke test sample.
6	V _{SS}	Connect to the negative supply voltage.
7	HB	This pin is connected to the metal electrode of a piezoelectric transducer.
8	HS	This pin is a complementary output to HB, connected to the ceramic electrode of the piezoelectric transducer.
9	FEED	Usually connected to the feedback electrode through a current limiting resistor. If not used, this pin must be connected to V _{DD} or V _{SS} .
10	RLED	An open drain NMOS output used to drive a visible LED. This pin provides the load current for the low-battery test and is a visual indicator for Alarm and Hush modes.
11	GLED	An open drain NMOS output used to drive a visible LED to provide a visual indication of an alarm memory condition.
12	I/O	This bidirectional pin provides the capability to interconnect many detectors in a single system. This pin has an internal pull-down device and a charge dump device.
13	TEST2	Test input to invoke test modes. This pin has an internal pull down.
14	TEST	This input is used to invoke push-to-test, Timer mode and alarm memory indication. This input has an internal pull down.

RE46C202

NOTES:

3.0 DEVICE DESCRIPTION

3.1 Standby Internal Timing

The internal oscillator is trimmed to $\pm 5\%$ tolerance. The oscillator period is 625 μs . A clock divider generates the 10 ms system clock.

In Standby, once every 10 seconds, the smoke detection circuitry is powered on for 5 ms. At the conclusion of the 5 ms, a smoke check measurement is made and the status of the smoke comparator is latched. If a smoke condition is present, the period to the next smoke check measurement decreases and additional checks are made.

In Standby, once every 80 seconds, the low-battery detection circuitry is powered on for 2.5 ms or 10 ms. At the conclusion of the 2.5 ms or 10 ms, the status of the low-battery comparator is latched. RLED is enabled for 2.5 ms or 10 ms every 320 seconds to provide a current load in the loaded battery test.

In Standby, once every 320 seconds, the chamber test circuitry is powered on for 5 ms. At the conclusion of the 5 ms, the status of the chamber test is latched (see [Section 3.4 “Chamber Test”](#) for details).

3.2 Smoke Detection Circuitry

The smoke detection circuitry consists of an integrating the photo amplifier with gain and an ADC. The ADC is composed of a DAC, comparator and counter circuitry. The counter circuitry increments the DAC output voltage until the DAC output voltage is equal to or greater than the photo amp output voltage.

A smoke check involves two steps. First, a dark integration measurement is made and digitized with the IRED off. Then a lit integration is made and digitized with the IRED on. The difference of the digitized values of the two integrations is compared to the alarm limit to determine if a smoke detection occurred. The dark integration is made to null out any offsets or leakage effects.

Three consecutive smoke detections will cause the device to go into Local Alarm and the horn circuit and interconnect will be active. If one or more valid smoke samples are detected, the RLED will turn on for 10 ms at a 1 Hz rate. When a Local Alarm occurs, the hysteresis alarm limit is selected to provide alarm hysteresis. The hysteresis limit must be lower than the Local Alarm limit. All alarm limits are user programmable.

The integrating photo amp gain and integration time are user-programmable. The combination of programmable gain and integration time allows an acceptable signal level to be achieved in different ways. The programmable integration time also sets the IRED on time. The IRED current drive is all internal and user-programmable as well.

The integrating photo amp has three separate gain modes for a selected gain:

- Normal Gain for Standby and Local Alarm
- Low Gain for Hush Timer
- Normal Gain for Chamber Test and Push-to-Test

There are four separate sets of alarm limits (all user-programmable):

- Local Alarm Limit
- Hysteresis Alarm Limit
- Hush Alarm Limit
- Chamber Test Alarm Limit

The combination of programmable gain, integration time, IRED current and alarm limits provides a high degree of flexibility when designing a smoke detector.

3.3 Photo Chamber Monitor

The Photo Chamber Monitor Function (CM) is a user selectable and programmable function (see [Register 4-1](#)). During calibration, a normal no-smoke measurement is made and stored in the CM baseline EEPROM. The user must then determine at what level the Chamber Monitor failure will occur, and this value will be stored as the CMmax limit in EEPROM.

During a normal operation, a new baseline will be calculated by making 64 integration measurements over an eight-hour period. These measurements are averaged and compared to the stored CMmax limit. If the average exceeds the CMmax limit, the Chamber Fail warning is sounded (see [Section 3.4 “Chamber Test”](#)). Chamber Monitor sampling will be suspended during Hush, Local Smoke and Remote Smoke conditions. For testing of CM levels, a special test mode is available. See [Section 4.9 “Chamber Monitor Single Sample Test Mode \(TM16\)”](#) for more details.

3.4 Chamber Test

Once every 320 seconds a smoke test with normal gain settings is performed to test the photo-chamber function. This check of the chamber is made by amplifying background reflections to simulate a smoke condition.

If two consecutive chamber tests fail to detect a simulated smoke condition, then the chamber fail latch is set and the failure warning is generated. The horn will chirp three times every 40s. Each chirp is 10 ms long and three chirps are spaced at a 0.5s interval. The chamber fail warning chirp is separated from the low-battery warning chirp by about 20s (see [Section 3.5 “Low-Battery Detection”](#)).

The horn will continue this pattern until the chamber fail latch is reset. The Reset occurs when any one of the followings is active:

- Two Consecutive Chamber Tests Pass
- Local Smoke Alarm
- PTT Smoke Alarm

A chamber test is performed approximately 140s after loaded low-battery test.

In Local Alarm, PTT Alarm or Remote Alarm condition, the chamber test is not performed and the low-battery chirping is prohibited.

3.5 Low-Battery Detection

Once every 80 seconds, the status of the battery voltage is checked by comparing a fraction of V_{DD} voltage to an internal reference voltage. In each period of 320 seconds, the battery voltage is checked four times. Of these four battery checks, three are unloaded and one is loaded with the RLED turned on which provides a current load on the battery. Low-battery status is latched at the end of the RLED pulse.

If the low-battery test fails, the horn will chirp for 10 ms every 40 seconds and will continue to chirp until the next low-battery check is passed. The unloaded low-battery checks are skipped in low-battery condition.

As a user-programmable option, a Low-Battery Hush mode can be selected. If a low-battery condition exists, upon release of PTT, the unit will enter Low-battery Hush mode and the 10ms horn chirp will be silenced for eight hours. At the conclusion of the eight hours, the audible indication will resume if the low-battery condition still exists.

3.6 Push-To-Test Operation (PTT)

PTT occurs when TEST is driven high (V_{IH3}). Release of PTT occurs when TEST is driven low (V_{IL3}).

PTT has different functions for different circumstances.

In Standby, PTT tests the unit. Upon start of PTT, the photo amplifier Normal Gain mode is selected and background reflections are used to emulate a smoke condition. The smoke detection rate increases to once every 250 ms. After three consecutive smoke detections, the unit will go into a Local Alarm condition. In alarm, the smoke detection rate decreases to once every 1s. Upon release of PTT, the photo amplifier normal gain is selected with hysteresis alarm levels. The detection rate remains at once every second until three consecutive no-smoke conditions are detected.

In Standby and if the alarm memory latch is already set, PTT does not test the unit. PTT invokes the alarm memory indication. Depending on the user selection, it can be a 4 Hz horn chirp, 4 Hz GLED pulse or both. Upon release of PTT, the alarm memory latch is reset.

In Standby and in low-battery condition, PTT tests the unit and RLED will be constantly enabled. This allows the user to easily identify the low-battery unit without waiting for 40s to hear a horn chirp. Upon release of PTT, RLED goes back to normal standby pulse rate. The Low-Battery Hush mode is then activated, if this function is enabled.

3.7 Interconnect Operation

The bidirectional I/O pin allows multiple detectors to be interconnected. In a Local Alarm condition, this pin is driven high 3.7s after a Local Alarm condition is sensed through a constant current source; this amounts to 4s of an originating alarm before remote alarms sound. Shorting this output to ground will not cause excessive current to flow. The I/O is ignored as an input during a Local Alarm.

The I/O pin also has an NMOS discharge device that is active for 2s after the conclusion of any type of local alarm. This device helps to quickly discharge any capacitance associated with the interconnect line.

If a remote, active high signal is detected, the device goes into Remote Alarm and the horn will be active. RLED will be off, indicating a Remote Alarm condition. Internal protection circuitry allows the signaling unit to have higher supply voltage than the signaled unit, without excessive current draw.

The interconnect input has a 310 ms nominal digital filter. This allows for interconnection to other types of alarms (carbon monoxide, for example) that may have a pulsed interconnect signal.

As a user-programmable option, the smart interconnect (smart I/O) function can be selected. If the I/O input is pulsed high twice with a nominal pulse on time greater than 23 ms and within 5.4s, a CO Alarm condition is detected and the CO temporal horn pattern will sound. The CO temporal horn pattern will sound at least two times if a CO Alarm condition is detected.

3.8 Hush Timer Mode

In Hush mode, the photo amp gain is reduced by one half and the Hush Alarm level, which is user-programmable, sets the smoke detection level. RLED is turned on for 10 ms every 10s while in Hush mode.

The Hush mode period is user-programmable and can be set to either 9 minutes or 80s. After this period times out, the unit goes back to standby operation.

Upon release of PTT, the unit may or may not go into a Hush mode, depending on the user selection.

If the Hush-In-Alarm-Only option is selected, then release of PTT only in a Local Alarm condition can initiate a Hush mode. Upon release of PTT, the unit is immediately reset out of alarm and the horn is silenced.

If the Hush-In-Alarm-Only option is not selected, then anytime a release of PTT occurs the Hush mode is initiated.

If the unit is currently in a Hush mode, then PTT will test the unit with the standby gain and alarm level. Upon release of PTT, a new Hush mode will be initiated.

As another user-programmable option, Hush mode can be terminated early by a Smart Hush function. This function allows the Hush mode to be canceled by either a high local smoke alarm or a remote smoke alarm. High local smoke alarm is a local smoke alarm caused by a smoke level which exceeds the Hush alarm level.

3.9 Local Alarm Memory

The Local Alarm Memory is a user-programmable option.

If a unit has entered a Local Alarm, then, when it exits the Local Alarm, the Alarm Memory latch is set. The GLED can be used to visually identify any unit that had previously been in a Local Alarm condition. The GLED sink driver is pulsed on three times every 40s. Each GLED driver pulse is 250 ms long and spaced 1s from the next pulse. This local alarm memory indication can be disabled or displayed with a period of 24 hours, 48 hours or no limit, depending on the user selection. This visual GLED indication is not displayed if a low-battery condition exists.

The user will be able to identify a unit with an active local alarm memory at any time before the Alarm Memory latch is reset. Upon start of PTT, the local alarm memory indication will be activated. Depending on the user selection, it can be a 4 Hz horn chirp, 2 Hz GLED pulse or both. A release of PTT will reset the local Alarm Memory latch. Depending on the user's programmed selection, the Alarm Memory latch can also be reset at the same time as the Alarm Memory Indication Period (24 or 48 hours). If zero or no limit is selected as the Alarm Memory Indication Period, then the Alarm Memory latch will be reset only at PTT.

3.10 End-of-Life (EOL) Indicator

The EOL Indicator is a user-programmable function.

If the EOL Indicator function is enabled, then approximately every 15 days of continuous standby operation, the design will read an age count stored in EEPROM and will then increment this age. After 10 years of operation, an audible indication will be given to signal that the unit needs to be replaced. The EOL indicator is five 10 ms horn chirps.

3.11 Horn Pattern

The temporal horn pattern supports the NFPA 72 emergency evacuation signal.

If a CO alarm is detected through the I/O, the unit will sound the CO horn pattern. The CO horn pattern consists of four horn beeps in every 5.8s. Each horn beep is 100 ms long and separated by 100 ms.

3.12 Horn Synchronization

The horn synchronization function is a user programmable function.

In an interconnected system, if one unit goes into a local alarm, then other units will go into a remote alarm. The I/O line is driven high by the origination local smoke unit and stays high during the alarm.

If the horn synchronization function is enabled, then at the end of every temporal horn pattern, and when horn is off, the origination unit will drive I/O low, then high again. This periodic I/O pulsing high and low will cause the remote smoke units to go into and out of a remote alarm repeatedly. Each time when a unit goes into a remote alarm, its timing is reset. The horn sound of all remote smoke units will be synchronized with the horn sound of the origination unit.

A protection circuit ensures that the unit that goes into a local alarm first will be the master unit which conducts the horn synchronization. The units which go into a local alarm later will not drive the I/O line. This avoids bus contention problems.

3.13 Auto Alarm Locate

Auto Alarm Locate (AAL) is also a user-programmable function. To use AAL with the temporal horn pattern, the horn synchronization function has to be selected also.

The purpose of AAL is to let users quickly find the local alarm units just by listening. The local alarm units will sound the pattern without interruption. The remote alarm units will sound the pattern with interruption. Every 16s the remote units are silenced for 4.7s.

The originating unit conducts the I/O cycling. During every fourth temporal horn pattern, the I/O is driven low for one temporal horn pattern. In the remaining three temporal horn patterns, the I/O is still pulsing to keep the horn synchronized.

The RLED of the origination unit and other local smoke units will be turned on 2.5 or 10 ms every 1s. The RLED of the remote smoke units will be off.

4.0 USER PROGRAMMING MODES

The RE46C202 provides user programming and test modes. User programming modes allow the various device options to be set and stored in EEPROM. Test modes provide a means to evaluate device performance.

Table 4-1 lists the various parametric settings provided by the RE46C202. The IRED period also sets the photo amp integration time. The photo detection limits section shows the typical maximum input current range for a given gain factor and integration time of the photo amp. The photo detection resolution section shows the step resolution for a given gain factor and integration time of the photo amp. Table 4-2 provides a list of user-selectable features such as Hush and Alarm Memory options.

TABLE 4-1: PARAMETRIC PROGRAMMING

Parametric Programming		Range		Resolution
IRED Period		100 – 400 μ s		100 μ s
IRED Current		50 – 200 mA		50 mA
Low-battery Detection Voltage		6.9 – 7.8V		300 mV
Photo Detection Limits		Input Current Range (nanoamps)		
		Normal/Hysteresis	Hush	Chamber Test
Integration Time 100 μ s	GF = 1x	61	122	61
	GF = 2x	30.5	61	30.5
	GF = 4x	15.3	30.5	15.3
	GF = 8x	7.6	15.3	7.6
Integration Time 200 μ s	GF = 1x	30.5	61	30.5
	GF = 2x	15.3	30.5	15.3
	GF = 4x	7.6	15.3	7.6
	GF = 8x	3.8	7.6	3.8
Integration Time 300 μ s	GF = 1x	20.3	40.7	20.3
	GF = 2x	10.2	20.3	10.2
	GF = 4x	5.1	10.2	5.1
	GF = 8x	2.54	5.1	2.54
Integration Time 400 μ s	GF = 1x	15.3	30.5	15.3
	GF = 2x	7.6	15.3	7.6
	GF = 4x	3.8	7.6	3.8
	GF = 8x	1.91	3.8	1.91
Photo Detection Resolution		Step Resolution (picoamps)		
		Normal/Hysteresis	Hush	Chamber Test
Integration Time 100 μ s	GF = 1x	1000	2000	1000
	GF = 2x	500	1000	500
	GF = 4x	250	500	250
	GF = 8x	125	250	125
Integration Time 200 μ s	GF = 1x	500	1000	500
	GF = 2x	250	500	250
	GF = 4x	125	250	125
	GF = 8x	63	125	63
Integration Time 300 μ s	GF = 1x	333	667	333
	GF = 2x	167	333	167
	GF = 4x	83	167	83
	GF = 8x	42	83	42
Integration Time 400 μ s	GF = 1x	250	500	250
	GF = 2x	125	250	125
	GF = 4x	63	125	63
	GF = 8x	31	63	31

TABLE 4-2: FEATURES PROGRAMMING

Features	Options
User Program Lockbit: Disables Programmability	Locked/Unlocked
Photo Chamber Monitor	Enable/Disable
Low-battery Detection Selection	6.9V, 7.2V, 7.5V, 7.8V
10 Year End-of-Life Indicator	Enable/Disable
Smart I/O with CO Alarm Sensing	Enable/Disable
Auto Alarm Locate	Enable/Disable
Horn Synchronization	Enable/Disable
Low-battery Hush	Enable/Disable
Alarm Memory Indicator at PTT: Horn Chirping	Enable/Disable
Alarm Memory Indicator at PTT: GLED Flashing	Enable/Disable
Alarm Memory Indicator at Standby Time-out Period	0/24/48 hour or no limit
Alarm Memory	Enable/Disable
Hush Time-out Period	9 minutes or 80 seconds
Smart Hush	Enable/Disable
Hush In Alarm Only	Enable/Disable
Hush	Enable/Disable
Low-battery Test RLED Pulse Width Select	10 ms or 2.5 ms

4.1 Calibration and Programming Procedures

Fifteen separate programming and test modes are available for user customization. The TEST2 input is used to enter these modes and step through these modes. To enter these modes, after power-up, TEST2 must be driven to V_{DD} and held at that level. To step through the modes, first the TEST input must be driven to V_{DD} . TEST2 is then clocked. TEST has to be high when clocking TEST2.

Anytime TEST2 and TEST are both driven to low, the unit will come out of these modes and go back to the Normal Operation mode. FEED, I/O and TEST are reconfigured to become Test mode inputs. TEST2 clock occurs on the rising edge, when it switches from V_{SS} to V_{DD} . The test mode functions are outlined in the [Table 4-3](#).

TABLE 4-3: TEST MODE FUNCTIONS

Mode	Description	TEST2 Clock	TEST	TEST2	FEED	I/O	TESTOUT	RLED	GLED	HB
M0 (1)	Normal Operation	0	PTT/Hush	0	FEED	I/O	I/O Dump or Smoke Check (2)	RLED	GLED	HB
TM0 (1)	Horn Test	1	HornEn	V_{DD}	FEED	I/O	NA	RLED	GLED	HB
TM1	Serial Read/Write	2	ProgData	V_{DD}	ProgClk	ProgEn	Serial Out	RLED	GLED	HB
TM2	Low-battery Test	3	TEST	V_{DD}	FEED	VDD	LBCompOut (3)	RLED	GLED	HB
TM3	EOL Serial Read/Write	4	ProgData	V_{DD}	ProgClk	ProgEn	Serial Out	RLED	GLED	HB
Smoke Check Test Modes										
TM4	Chamber Test Limit Check (7)	5	V_{DD}	V_{DD}	Measure Enable	V_{SS}	DCMP (4)	DAC (5)	IntegOut (6)	SCMP (4)
TM5	Standby Limit Check (8)	6	V_{DD}	V_{DD}	Measure Enable	V_{SS}	DCMP (4)	DAC (5)	IntegOut (6)	SCMP (4)
TM6	Hysteresis Limit Check (9)	7	V_{DD}	V_{DD}	Measure Enable	V_{SS}	DCMP (4)	DAC (5)	IntegOut (6)	SCMP (4)
TM7	Hush Limit Check	8	V_{DD}	V_{DD}	Measure Enable	V_{SS}	DCMP (4)	DAC (5)	IntegOut (6)	SCMP (4)

Note 1: After power-up, the unit is in M0, the Normal Operation mode. In M0, if TEST2 is driven to V_{DD} , the unit will enter TM0.

2: In M0, the digital output TESTOUT is driven to V_{DD} when the internal I/O dump signal, the smoke check signal or the POR signal occur.

3: LBCompOut – digital comparator output (high if $V_{DD} < LB$ trip point; low if $V_{DD} > LB$ trip point).

4: The Digital Compare (DCMP) asserts as high when the digitized smoke level equals or exceeds the smoke alarm limit, and SCMP is the latched DCMP value.

5: DAC – smoke level digitizer output voltage.

6: IntegOut – Integrator voltage level, including gain factor amplification

7: It is recommended that the Chamber Test Limit and PTT Limit Check be set so that the test always produces a smoke condition (=1) in clear air.

8: It is recommended that the Standby Smoke Check be set so that it always tests positive (= 1) for minimum required smoke for the alarm.

9: It is recommended that the Hysteresis Smoke Check be set so that it always produces a No Smoke (= 0) for maximum allowable smoke.

10: In CM Cal mode, a smoke measurement increments the CM counter.

11: In CM Cal mode, the CM shift register is set to the CM counter when TEST = 0 for programming in TM11.

12: In CM Cal mode, the CM_{max} shift register is set to the CM counter when TEST = 1 for programming in TM11.

13: ScmpOut asserts a high when the DAC output voltage is equal to or greater than the Integrator output voltage.

14: In Calibration modes, TEST resets the dark integration measurement, after which the first Calibration Clock (CalCLK) on FEED causes a dark integration measurement.

15: CalCLK causes an integration with IRED on, starting with the rising edge; it also increments the DAC input by 1 on the falling edge.

TABLE 4-3: TEST MODE FUNCTIONS (CONTINUED)

Mode	Description	TEST2 Clock	TEST	TEST2	FEED	I/O	TESTOUT	RLED	GLED	HB
Chamber Monitor (CM) Calibration Test Modes										
TM10	CM Baseline	11	0	V_{DD}	Measure Enable (10)	Latch (11)	ScmpOut (13)	DAC (5)	IntegOut (6)	HB
	Increment CM Counter		↑↓		V_{SS}	V_{SS}				
	CMmax		1		V_{SS}	Latch (12)				
TM11	Program CM Values	12	Not Used	V_{DD}	V_{SS}	ProgEn	NA	NA	NA	HB
Smoke Calibration Test Modes										
TM12	Chamber Test Calibration	13	Measure Enable (14)	V_{DD}	CalCLK (15)	Latch	ScmpOut (13)	DAC (5)	IntegOut (6)	HB
TM13	Standby Calibration	14	Measure Enable (14)	V_{DD}	CalCLK (15)	Latch	ScmpOut (13)	DAC (5)	IntegOut (6)	HB
TM14	Hysteresis Calibration	15	Measure Enable (14)	V_{DD}	CalCLK (15)	Latch	ScmpOut (13)	DAC (5)	IntegOut (6)	HB
TM15	Hush Calibration	16	Measure Enable (14)	V_{DD}	CalCLK (15)	Latch ProgEn	ScmpOut (13)	DAC (5)	IntegOut (6)	HB
TM19	EE Lock Bit	20	V_{DD}	V_{DD}	FEED	ProgEn	Lock Out	RLED	GLED	HB

- Note**
- 1: After power-up, the unit is in M0, the Normal Operation mode. In M0, if TEST2 is driven to V_{DD} , the unit will enter TM0.
 - 2: In M0, the digital output TESTOUT is driven to V_{DD} when the internal I/O dump signal, the smoke check signal or the POR signal occur.
 - 3: LBCompOut – digital comparator output (high if $V_{DD} < LB$ trip point; low if $V_{DD} > LB$ trip point).
 - 4: The Digital Compare (DCMP) asserts as high when the digitized smoke level equals or exceeds the smoke alarm limit, and SCMP is the latched DCMP value.
 - 5: DAC – smoke level digitizer output voltage.
 - 6: IntegOut – Integrator voltage level, including gain factor amplification
 - 7: It is recommended that the Chamber Test Limit and PTT Limit Check be set so that the test always produces a smoke condition (=1) in clear air.
 - 8: It is recommended that the Standby Smoke Check be set so that it always tests positive (= 1) for minimum required smoke for the alarm.
 - 9: It is recommended that the Hysteresis Smoke Check be set so that it always produces a No Smoke (= 0) for maximum allowable smoke.
 - 10: In CM Cal mode, a smoke measurement increments the CM counter.
 - 11: In CM Cal mode, the CM shift register is set to the CM counter when TEST = 0 for programming in TM11.
 - 12: In CM Cal mode, the CM_{max} shift register is set to the CM counter when TEST = 1 for programming in TM11.
 - 13: ScmpOut asserts a high when the DAC output voltage is equal to or greater than the Integrator output voltage.
 - 14: In Calibration modes, TEST resets the dark integration measurement, after which the first Calibration Clock (CalCLK) on FEED causes a dark integration measurement.
 - 15: CalCLK causes an integration with IRED on, starting with the rising edge; it also increments the DAC input by 1 on the falling edge.

4.1.1 PROGRAMMING IN THE TYPICAL APPLICATION

The [Typical Application](#) shows the typical application circuit with special probe pads for test modes. Logic Inputs are FEED, I/O, TEST2, and TEST. They all need to have driven inputs on these nodes in the test modes. TESTOUT is a digital output. RLED and GLED are analog outputs.

Weak signals may be multiplexed to the RLED and GLED outputs. When this occurs, it is important to ground the anodes of D4 and D5 so that they are not overdriven by the current through the LEDs.

4.2 Horn Test (TM0)

Test mode TM0 allows the horn to be enabled indefinitely for audibility testing.

To enter this mode, follow these steps:

1. Power-up with the bias condition shown in [Figure 4-1](#) to enter M0. At power-up, TEST, I/O, FEED and TEST2 should be tied to V_{SS} .
2. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} to enter TM0; the horn will be enabled.

In TM0, the TEST pin is the HornEnB control. To prevent the horn from sounding in TM0, TEST can be driven high. To prevent the horn from sounding while entering TM0, TEST may be driven high concurrently or just before TEST2 is driven to V_{DD} .

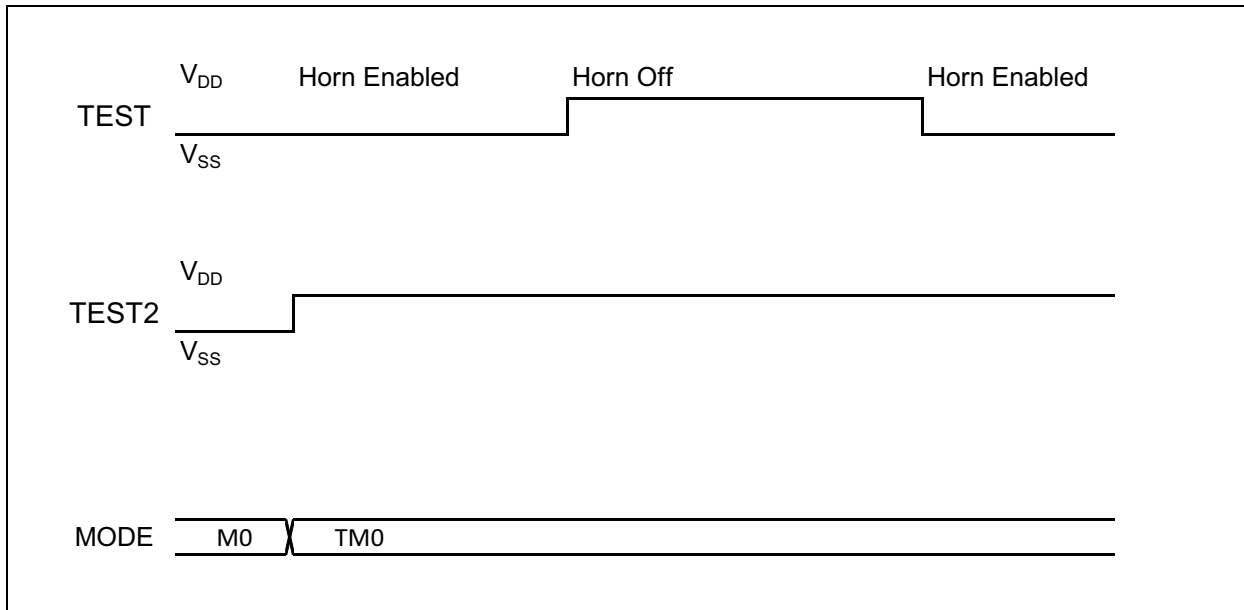


FIGURE 4-1: Timing Diagram for Horn Test in Mode TM0.

4.3 Serial Read/Write (TM1)

The feature selections and calibration values can be programmed in through the Serial Read/Write mode. Data are serially loaded into a shift register which is then used to program the EEPROM. All 60 bits must be loaded. This means temporary alarm limits and CM values must be loaded if these values are not known. Calibration and CM Test modes can be used to update these values.

To enter Test mode TM1, follow these steps:

1. Power-up with the bias condition shown in [Figure 4-1](#) to enter M0. At power-up, the four input pins TEST, I/O, FEED and TEST2 should be tied to V_{SS} . TESTOUT is the serial output.
2. Drive the TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} .
3. Drive the TEST input from V_{SS} to V_{DD} and hold at V_{DD} .
4. Apply one clock pulse to the TEST2 input (V_{DD} to V_{SS} and back to V_{DD}) to enter TM1. This enables the Serial Read/Write mode.

5. TEST now acts as a data input (1 = V_{DD} , 0 = V_{SS}), and FEED acts as the clock input (1 = V_{DD} , 0 = V_{SS}). Data are clocked in on the rising edge.
6. Shift in 60 bits of the user configuration and calibration settings. These settings are described in [Register 4-1](#).
7. After the data are entered into the shift register, pulse I/O high for a minimum of 10 ms to store the data in EEPROM. The timing diagram is shown in [Figure 4-2](#).
8. When Test mode TM1 is entered, the contents of EEPROM are loaded into the shift register. The shift register contents are read out on TESTOUT as data are clocked in. If I/O is not pulsed, the contents of the EEPROM are not changed.

REGISTER 4-1: USER CONFIGURATION SETTINGS AND CALIBRATION SETTINGS

				R/W	R/W	R/W	R/W
				CMM5	CMM4	CMM3	CMM2
bit 59				bit 56			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CMM1	CMM0	CM5	CM4	CM3	CM2	CM1	CM0
bit 55				bit 48			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	HUL5	HUL4
bit 47				bit 40			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HUL3	HUL2	HUL1	HUL0	HYL5	HYL4	HYL3	HYL2
bit 39				bit 32			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HYL1	HYL0	NL5	NL4	NL3	NL2	NL1	NL0
bit 31				bit 24			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CME _n	IRED2	IRED1	TIRON2	TIRON1	GF2	GF1	LBTR2
bit 23				bit 16			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LBTR1	EOLE _n	COE _n	NoAAL	SyncEn	LBHshEn	AMHCE _n	AMLEDE _n
bit 15				bit 8			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
AMTO2	AMTO1	AME _n	ShrtTO	Smrth	HIAO	HushEnB	LBSEL
bit 7				bit 0			

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 59-54 **CMM[5:0]:** Chamber Monitor Max Limit ([Section 3.3 “Photo Chamber Monitor”](#))
 000000 = 0
 000001 = 1
 •
 •
 •
 111110 = 62
 111111 = 63

bit 53-48 **CM[5:0]:** Chamber Monitor Baseline ([Section 3.3 “Photo Chamber Monitor”](#))
 000000 = 0
 000001 = 1
 •
 •
 •
 111110 = 62
 111111 = 63

REGISTER 4-1: USER CONFIGURATION SETTINGS AND CALIBRATION SETTINGS

bit 47-42	CTL[5:0]: Chamber Test Limit (Section 3.4 “Chamber Test”) 000000 = 0 000001 = 1 • • • 111110 = 62 111111 = 63
bit 41-36	HUL[5:0]: Hush Limit (Section 3.8 “Hush Timer Mode”) 000000 = 0 000001 = 1 • • • 111110 = 62 111111 = 63
bit 35-30	HYL[5:0]: Hysteresis Limit (Section 3.2 “Smoke Detection Circuitry”) 000000 = 0 000001 = 1 • • • 111110 = 62 111111 = 63
bit 29-24	NL[5:0]: Normal Smoke Detection Limit (Section 3.2 “Smoke Detection Circuitry”) 000000 = 0 000001 = 1 • • • 111110 = 62 111111 = 63
bit 23	CMEn: Chamber Monitor Enable 1 = Enable 0 = Disable
bit 22-21	IRED[2:1]: IRED Current Setting Select 00 = 50 mA 01 = 100 mA 10 = 150 mA 11 = 200 mA
bit 20-19	TIRON[2:1]: Integration Time Select 00 = 100 μ s 01 = 200 μ s 10 = 300 μ s 11 = 400 μ s
bit 18-17	GF[2:1]: Gain Factor Setting Select 00 = 1x 01 = 2x 10 = 4x 11 = 8x
bit 16-15	LBTR[2:1]: Low Battery Trip Point Select 00 = 7.5V 01 = 6.9V 10 = 7.8V 11 = 7.2V
bit 14	EOLEn: End-of-Life Indicator Enable 1 = Enable 0 = Disable

REGISTER 4-1: USER CONFIGURATION SETTINGS AND CALIBRATION SETTINGS

bit 13	COEn: CO Alarm Function (Smart I/O) Enable 1 = Enable 0 = Disable
bit 12	NoAAL: Auto Alarm Locate Disable 1 = AAL is disabled 0 = AAL is enabled
bit 11	SyncEn: Horn Synchronization Enable 1 = Enable 0 = Disable
bit 10	LBHshEn: Low-Battery Hush Enable 1 = Enable 0 = Disable
bit 9	AMHCEn: Alarm Memory PTT Indicator Horn Chirp Enable 1 = Enable 0 = Disable
bit 8	AMLEDEn: Alarm Memory PTT Indicator LED Flashing Enable 1 = Enable 0 = Disable
bit 7-6	AMTO[2:1]: Alarm Memory Standby LED indicator Time Out Select 00 = 24 hour 01 = 48 hour 10 = 0 11 = never time out
bit 5	AMEn: Alarm Memory Enable 1 = Enable 0 = Disable
bit 4	ShrtTO: Hush Timer Time Out Select 1 = 80s 0 = 9 minutes
bit 3	SmrthH: Smart Hush Enable 1 = Enable (Hush is canceled by either high smoke or remote smoke) 0 = Disable (Hush is never canceled until time out)
bit 2	HIAO: Hush-in-Alarm-Only Enable 1 = Enable (Hush is activated upon release of PTT during local alarm only) 0 = Disable (Hush is activated upon release of PTT at anytime)
bit 1	HushEnB: Hush Enable 1 = Hush is disabled 0 = Hush is enabled
bit 0	LBSEL: Low-battery Pulse Width Select 1 = 2.5 ms 0 = 10 ms

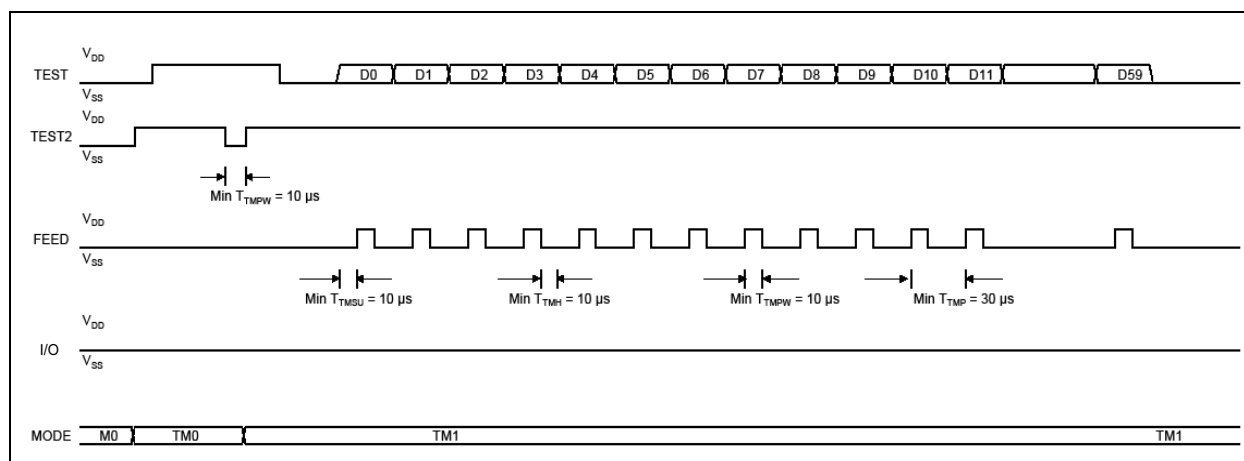


FIGURE 4-2: Timing Diagram for User Feature Selection in Serial Read/Write Mode TM1.

4.4 Low-Battery Test (TM2)

Test mode TM2 allows the low-battery trip point to be tested.

To enter this mode, follow these steps:

1. Power-up with the bias condition shown in Figure 4-1 to enter M0. At power-up, TEST, I/O, FEED and TEST2 should be tied to V_{SS} .
2. Drive TEST from V_{SS} to V_{DD} and hold at V_{DD} .
3. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} to enter TM0.
4. Apply two clock pulses to the TEST2 input (V_{DD} to V_{SS} and then back to V_{DD}) to enter in TM2 mode.
5. Drive I/O from V_{SS} to V_{DD} to enable the low-battery testing and turn on the RLED. Sweep V_{DD} from high to low and monitor TESTOUT output. The TESTOUT output will indicate the low-battery status (High = low battery detected).

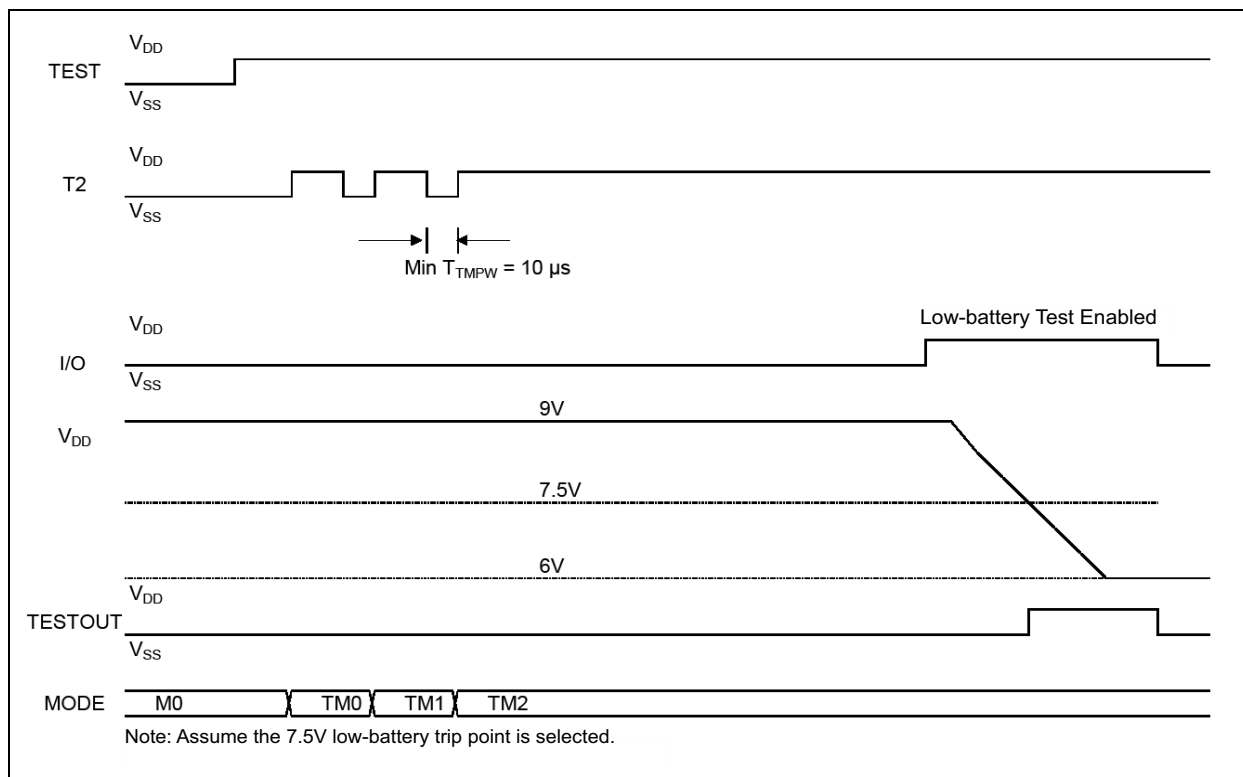


FIGURE 4-3: Timing Diagram for Low-Battery Test in Mode TM2.

4.5 End-Of-Life Serial Read/Write (TM3)

The 10-year End-of-Life feature can be read and modified through the TM3 Serial Read/Write mode. This allows for the possibility of setting shorter end-of-life values for different applications, such as three or five years. Note that the controls for data, clock and program are the same as the previous Serial Read/Write mode, but a different register is used.

To enter this mode, follow these steps:

1. Power up with the bias condition shown in Figure 4-1 to enter M0. At power-up, drive four input pins (probe pads) TEST, I/O, FEED and TEST2 should be tied to V_{SS} . TESTOUT, RLED and GLED are outputs and must not be driven.
2. Drive TEST from V_{SS} to V_{DD} and hold at V_{DD} .
3. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} to enter TM0.
4. Apply three clock pulses to the TEST2 input (V_{DD} to V_{SS} and back to V_{DD}) to enter in TM3. This enables the EOL Serial Read/Write mode.
5. Drive TEST low to V_{SS} .
6. TEST acts as a data input ($1 = V_{DD}$, $0 = V_{SS}$).
7. TESTOUT acts as the data output ($1 = V_{DD}$, $0 = V_{SS}$).
8. FEED acts as the clock input ($1 = V_{DD}$, $0 = V_{SS}$).
9. Data are clocked on the rising edge.
10. Shift in the values of the eight EOL bits, MSB first.
11. Drive I/O high for 10 ms to program the new EOL counter value.

REGISTER 4-2: END-OF-LIFE REGISTER

W	W	W	W	W	W	W	W
EOL0	EOL1	EOL2	EOL3	EOL4	EOL5	EOL6	EOL7
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 0-7

EOL[0:7]: Long Term Drift Max Limit ([Section 3.10 “End-of-Life \(EOL\) Indicator”](#))

00000000 = 0

10000000 = 1

•

•

•

01111111 = 254

11111111 = 255

4.5.1 END-OF-LIFE EXAMPLE

For a 10-year EOL time-out, the internal counter counts up to 241 clocks incremented every 364 hours (≈15 days). The counter starts at zero. To shorten the EOL time-out, the EOL register can be loaded with a non-zero value.

For a seven-year EOL time-out, start with EOL value of 72 instead of 0. [Table 4-4](#) shows the bit settings for a seven-year EOL.

TABLE 4-4: SEVEN-YEAR EOL

Data	0	0	0	1	0	0	1	0
Bit #	0	1	2	3	4	5	6	7
Value	0	0	0	8	0	0	64	0

When the part reaches a count of 241, the EOL warning will occur. In this seven-year example, the starting value was 72, so the clock will be incremented 169 (241-72) times, for a total of 169 x 364 hours, or 61516 hours or 7.0 years.

4.6 Limits Verification (TM4, TM5, TM6, TM7)

After the RE46C202 is configured, test modes are available to verify that the limits are functioning as expected. [Table 4-5](#) describes the limit verification test modes. These test modes are ordered to facilitate smoke box verification, going from no smoke to minimum smoke to maximum no smoke alarm (hysteresis) to minimum Hush smoke. Overall, this means starting with no smoke and ending with maximum smoke.

To enter these test modes, follow these steps:

1. Power-up with the bias condition shown in [Figure 4-1](#) to enter M0. At power-up, the four input pins TEST, I/O, FEED and TEST2 should be tied to V_{SS}. TESTOUT, RLED and GLED are outputs that are used to monitor the system

response.

2. Drive TEST from V_{SS} to V_{DD} and hold at V_{DD}.
3. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD}.
4. Apply four clock pulses to the TEST2 input (V_{DD} to V_{SS} and back to V_{DD}) to enter TM4.
5. With appropriate smoke level in the chamber, pull TEST low to V_{SS} and then, drive FEED to V_{DD} for at least 2 ms. TESTOUT will indicate detection status (HIGH = detection). The integrator and DAC voltages can be monitored on the GLED and RLED pins, respectively.
6. Drive TEST high to V_{DD} and clock TEST2 once. This places the RE46C202 in the next test mode.
7. Repeat Steps 5 and 6 until each verification mode is checked.

This operation causes a dark (IRED off) measurement followed by a lit (IRED on) measurement. The difference is digitized and compared to the 6-bit alarm limit. The resulting compare comes out on TESTOUT. A logic high is output as soon as the measurement digitization exceeds the smoke alarm limit.

[Figure 4-4](#) shows the timing diagram for the Limits Verification procedure.

TABLE 4-5: ALARM LIMITS VERIFICATION DESCRIPTION

Function	Mode	TEST2 Clocks (Low, then High)
PTT/Chamber Test	TM4	Clock TEST2 4x
Standby	TM5	Clock TEST2 5x
Hysteresis	TM6	Clock TEST2 6x
Hush	TM7	Clock TEST2 7x

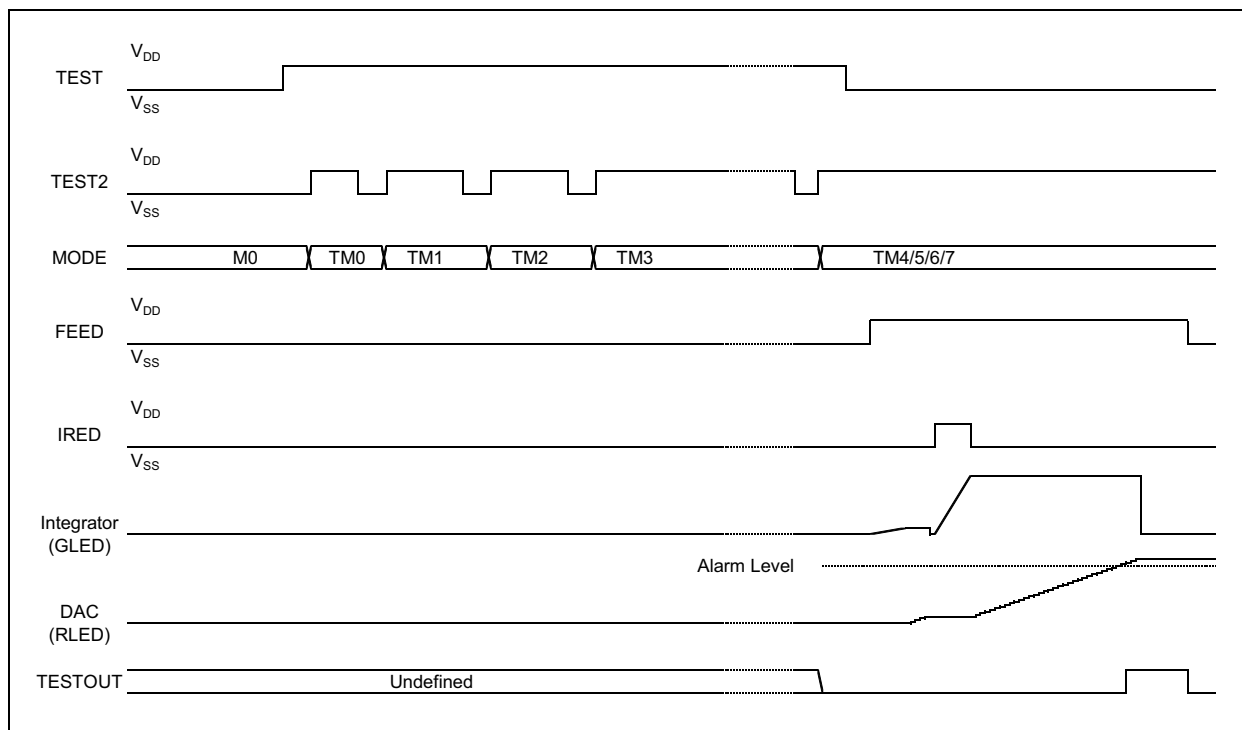


FIGURE 4-4: Timing Diagram for Limit Verification in Mode TM4 ~ TM7.

4.7 Chamber Monitor Calibration (TM10, TM11)

Measurement and programming of the Chamber Monitor baseline value is done in Test modes TM10 and TM11, respectively. Alternately, in a well-characterized system, TM1 may be used to program CM and CM_{max} without measurement. CM_{max} must be set to a value greater than the CM value.

4.7.1 BASELINE CM MEASUREMENT (TM10)

To enter this mode, follow these steps:

1. Power-up with the bias condition shown in [Figure 4-1](#) to enter M0. At power-up, drive four input pins (probe pads) TEST, I/O, FEED and TEST2 should be tied to V_{SS} . TESTOUT, RLED and GLED are outputs that are used to monitor the system response.
2. Drive TEST from V_{SS} to V_{DD} and hold at V_{DD} .
3. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} .
4. Apply 10 clock pulses to the TEST2 input (V_{DD} to V_{SS} and back to V_{DD}) to enter TM10.
5. Drive TEST from V_{DD} to V_{SS} before measuring.
6. Driving FEED high for at least 2 ms causes a baseline dark (IRED off) measurement followed by a lit (IRED on) measurement. The difference is digitized and accumulated to the CM counter.

The integrator and DAC voltages can be monitored on the GLED and RLED pins, respectively. The comparison of the DAC and the integrator voltages comes out on the TESTOUT pin.

7. The baseline CM value that is held in the CM counter is latched into the programming register by clocking I/O while TEST and FEED are low.
8. The CM value is stored in EEPROM in TM11.
9. In order to set the CM_{max} value, the value held in the CM counter can be incremented by pulsing TEST from V_{SS} to V_{DD} and back to V_{SS} . Each pulse increments the CM counter by one.
10. The CM_{max} value held in the CM counter is latched into the programming register by clocking I/O while TEST is high and FEED is low.

4.7.2 CM PROGRAMMING (TM11)

After the CM and CM_{max} values are latched in the programming register in TM10, values may be programmed into EEPROM in TM11.

1. To enter CM Programming mode TM11, with TEST high, and clock TEST2 once from TM10.
2. Drive TEST to V_{SS} .
3. Pulse I/O to V_{DD} for 10 ms minimum.
4. The CM and CM_{max} values are now stored in EEPROM.

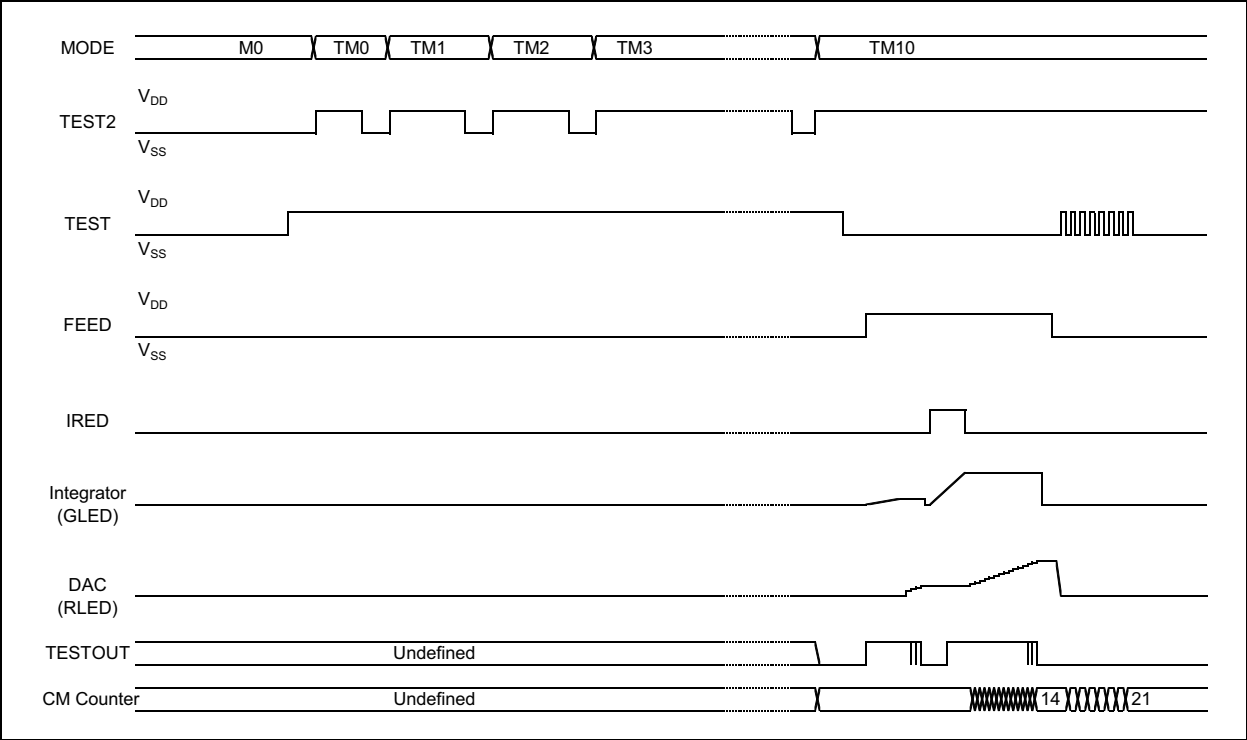


FIGURE 4-5: Timing Diagram for CM Calibration Mode in TM10.

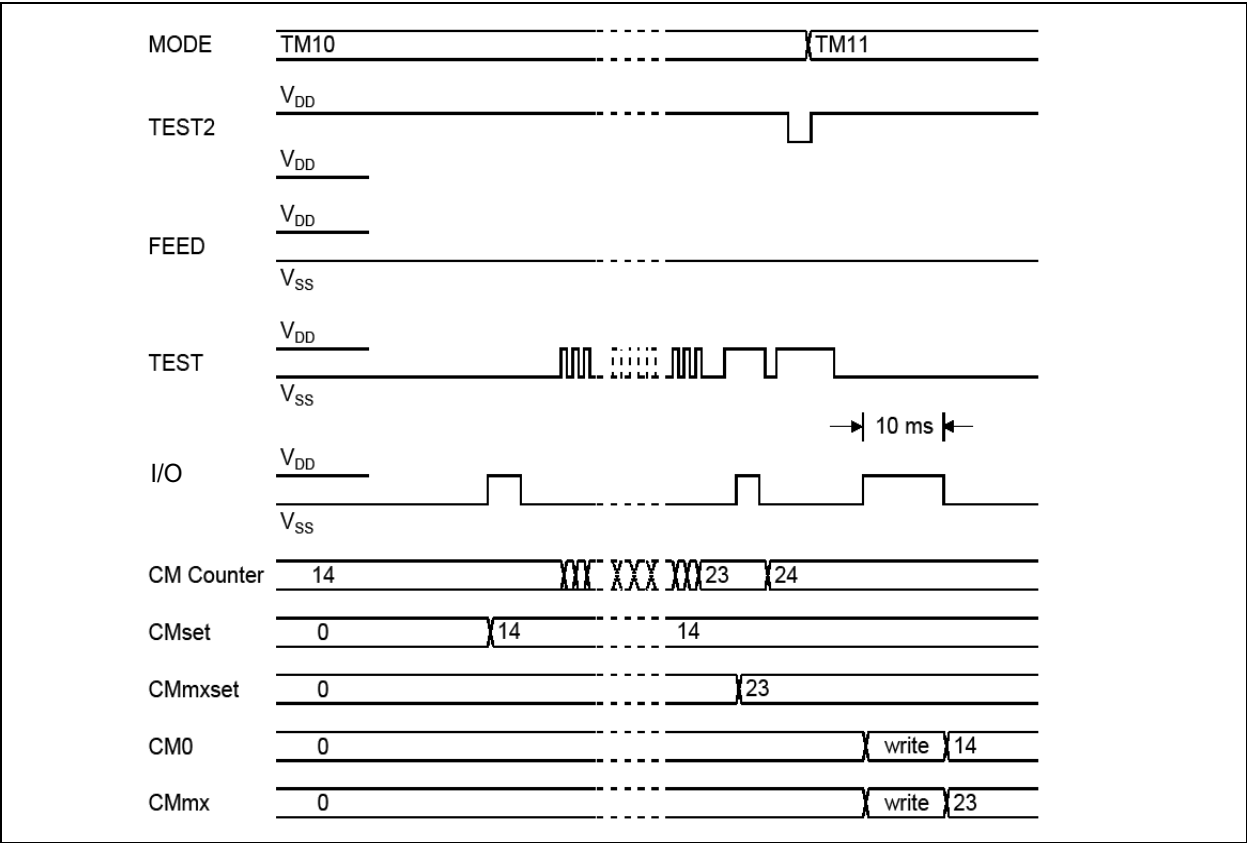


FIGURE 4-6: Timing Diagram for CM Calibration Setting and Programming in Modes TM10 ~ TM11.

4.8 Smoke Calibration (TM12, TM13, TM14, TM15)

A separate Calibration Test mode is used for each Measurement mode (PTT/Chamber Test, Normal, Hysteresis and Hush) so that alarm limits can be set for each.

The Calibration Test modes are listed in Table 4-6. In all calibration test modes, the integrator output can be accessed at the GLED output. The DAC output voltage, which represents the smoke detection level, can be accessed at the RLED output, and the comparator output can be accessed at TESTOUT.

The FEED input is clocked to step up the smoke detection level at RLED. Each FEED clock increments the DAC and initiates a smoke measurement. When the smoke detection level is less than the photo amp output voltage, TESTOUT will be asserted high. When the smoke detection level is equal to or greater than the photo amp output voltage, TESTOUT will remain low. To save this smoke alarm limit, the I/O input is pulsed low-to-high to store the result in the programming register. In TM15, when the I/O is pulsed, the result is stored in the programming register and then all four results in the programming register are programmed into the EEPROM. It is recommended that the I/O pulse in TM15 be at least 10 ms.

TABLE 4-6: ALARM LIMIT CALIBRATION MODES

Alarm Limit	Mode	TEST2 Clocks (Low, then High)
PTT/Chamber Test	TM12	Clock TEST2 12x
Standby Alarm Limit	TM13	Clock TEST2 13x
Hysteresis Alarm Limit	TM14	Clock TEST2 14x
Hush Alarm Limit	TM15	Clock TEST2 15x

4.8.1 SIMPLE ALARM LEVEL CALIBRATION

1. Power-up with the bias condition shown in Figure 4-1 to enter M0. At power-up, drive four input pins (probe pads) TEST, I/O, FEED and TEST2 should be tied to V_{SS} . TESTOUT, RLED and GLED are outputs that are used to monitor the system response.
2. Drive TEST from V_{SS} to V_{DD} and hold at V_{DD} .
3. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} .
4. To calibrate an alarm limit setting, clock TEST2 to the test mode (TM12, TM13, TM14 and TM15 as indicated above).
5. With appropriate smoke level in chamber, pull TEST low to V_{SS} , and then drive FEED to V_{DD} and hold at least for 2 ms. The integrator and DAC voltages come out on the GLED and RLED pins, respectively. This operation causes a baseline dark (no IRED) measurement followed by a lit (IRED) measurement.
6. Clock FEED (hold FEED high for at least 2 ms) until TESTOUT no longer transitions high after an integration. Unlike the Limit Verification, digitization does not occur automatically, but instead the DAC is incremented on each falling edge of FEED. The DAC voltage is shown on the RLED pin. When the DAC output is greater than the integrator output, TESTOUT will not transition high. Then, with FEED held low, pulse I/O high for 10 μ s to latch the data into the programming register.
7. To store the TM15 limit and program all the alarm limits in to EEPROM, pulse I/O high for 10 ms.

4.8.2 QUICKER ALARM LEVEL CALIBRATION

FEED can be used to skip tests the min. alarm level.

1. To calibrate a smoke detection level, clock TEST2 to the test mode (TM12, TM13, TM14, and TM15 as indicated above).
2. With appropriate smoke level in chamber, pull TEST low to V_{SS} , then drive FEED to V_{DD} and hold for at least 2 ms for the first full integration. The integrator and DAC voltages come out on the GLED and RLED pins, respectively. This operation causes a baseline dark (no IRED) measurement followed by a light (IRED) measurement.
3. Clock FEED high for 5 μ s with a 10 μ s period until the minimum of the calibration range is reached then, hold FEED low for greater than 2 ms.
4. Clock FEED high for at least 2 ms until TESTOUT no longer transitions high after an integration.

4.8.3 DECREMENTING ALARM LIMIT CALIBRATION

If the desired alarm limit is one step below the measured alarm limit, the measurement can effectively be decremented. The measurement counter rolls over at 64, so incrementing FEED 63 times is equivalent to decrementing the measurement by one.

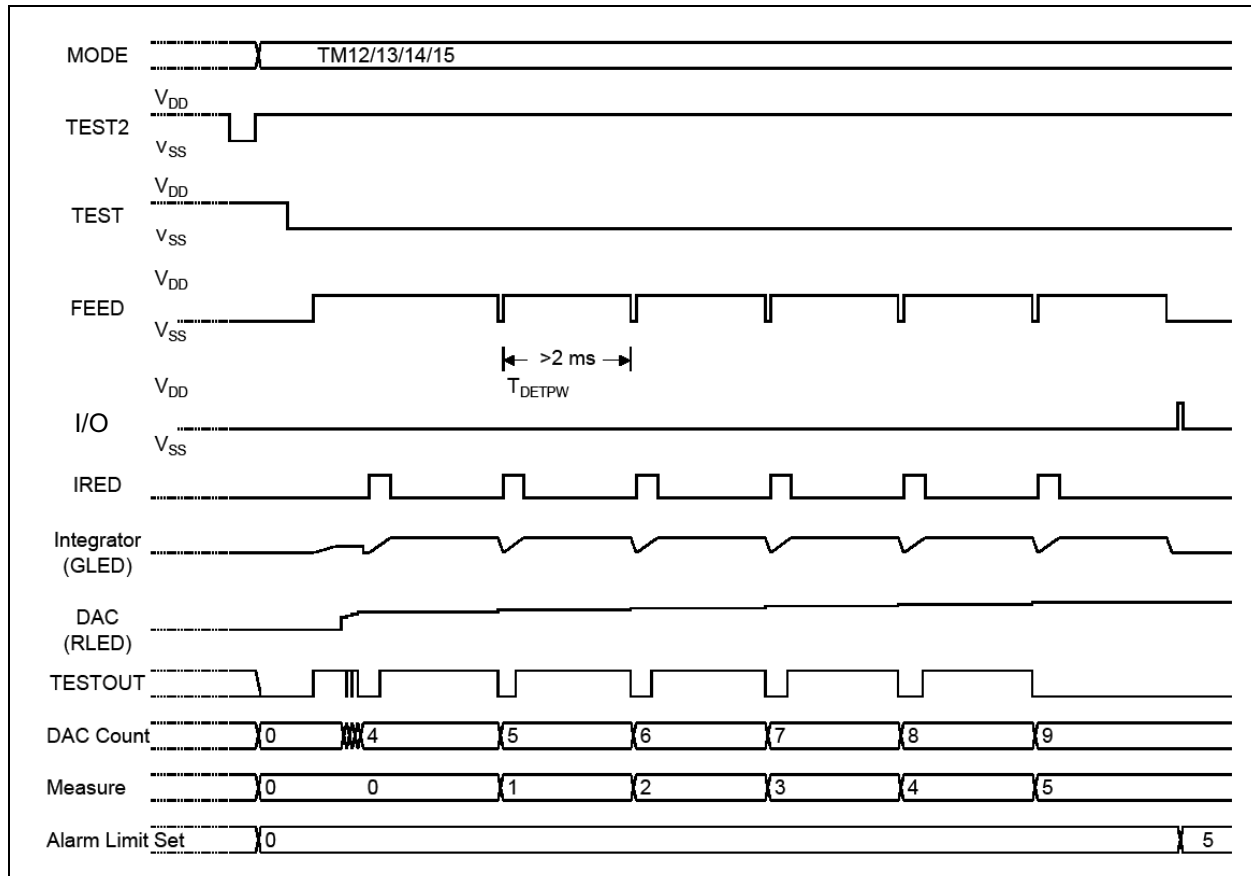


FIGURE 4-7: Timing Diagram for Simple Alarm Limit Calibration in Mode TM12 ~ TM15.

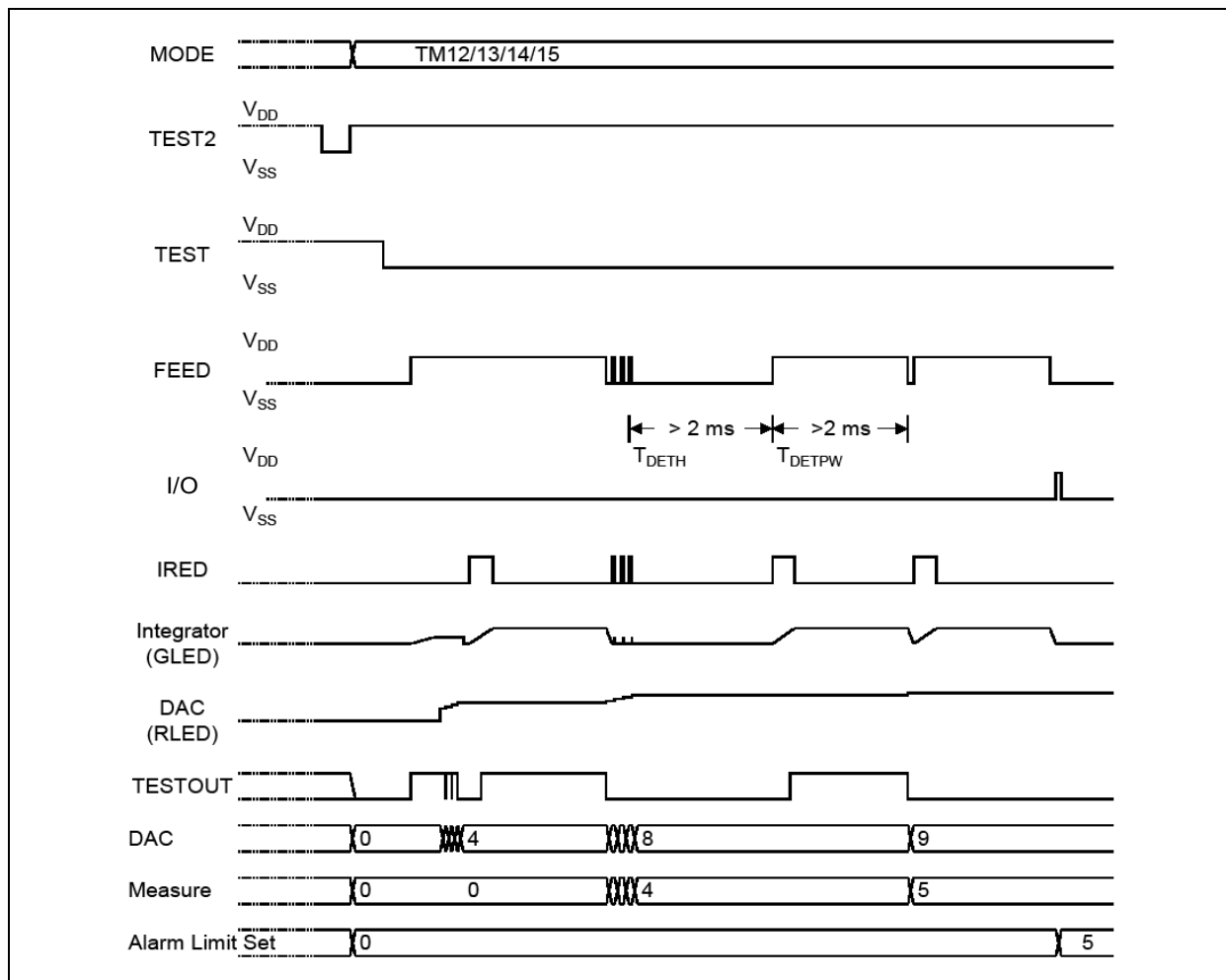


FIGURE 4-8: Timing Diagram for Quick Alarm Limit Calibration in Mode TM12 ~ TM15.

4.9 Chamber Monitor Single Sample Test Mode (TM16)

Test mode TM16 allows users to enable the Chamber Monitor Fast Single Sample mode. Instead of taking 64 samples over eight hours and dividing by 64, it takes a single sample within eight minutes. If this sample is greater than CMmax, the chamber monitor will chirp.

To enable the Chamber Monitor Fast Single Sample mode, follow these steps:

1. Wait until at least one detection (TO pulses high).
2. Drive TEST2 from V_{SS} to V_{DD} .
3. Drive TEST from V_{SS} to V_{DD} .
4. Apply 16 clock pulses to TEST2 (V_{DD} to V_{SS} & then back to V_{DD}) to enter TM16.
5. Pulse I/O > 3V for at least 10 μ s; this sets the Chamber Monitor Fast Single Sample mode.
6. Drop out of TM16 and into Normal Operating mode:
 - a. TEST = V_{SS}
 - b. TEST2 = V_{SS}

In this mode, the CM sample will be accompanied by a 10 ms GLED flash. After the single CM sample, the chamber monitor will revert to a normal operation.

4.10 Lock Bit Programming (TM19)

Test mode TM19 allows users to program the EE lock bit. Once the EE lock bit is set, the programmed user EE data cannot be changed, unless the lock bit is reset.

To enter this mode, follow these steps:

1. Power-up with the bias condition shown in [Figure 4-1](#) to enter M0. At power-up, TEST, I/O, FEED and TEST2 should be tied to V_{SS} .
2. Drive TEST from V_{SS} to V_{SS} and hold at V_{DD} .
3. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} to enter TM0.

4. Apply 19 clock pulses to the TEST2 input (V_{DD} to V_{SS} and then back to V_{DD}) to enter in TM19 mode.
5. Hold TEST at V_{DD} and pulse I/O once to set the lock bit and store it into EEPROM memory.
6. To reset the lock bit in step 5, drive TEST to V_{SS} and pulse I/O once to reset the lock bit.

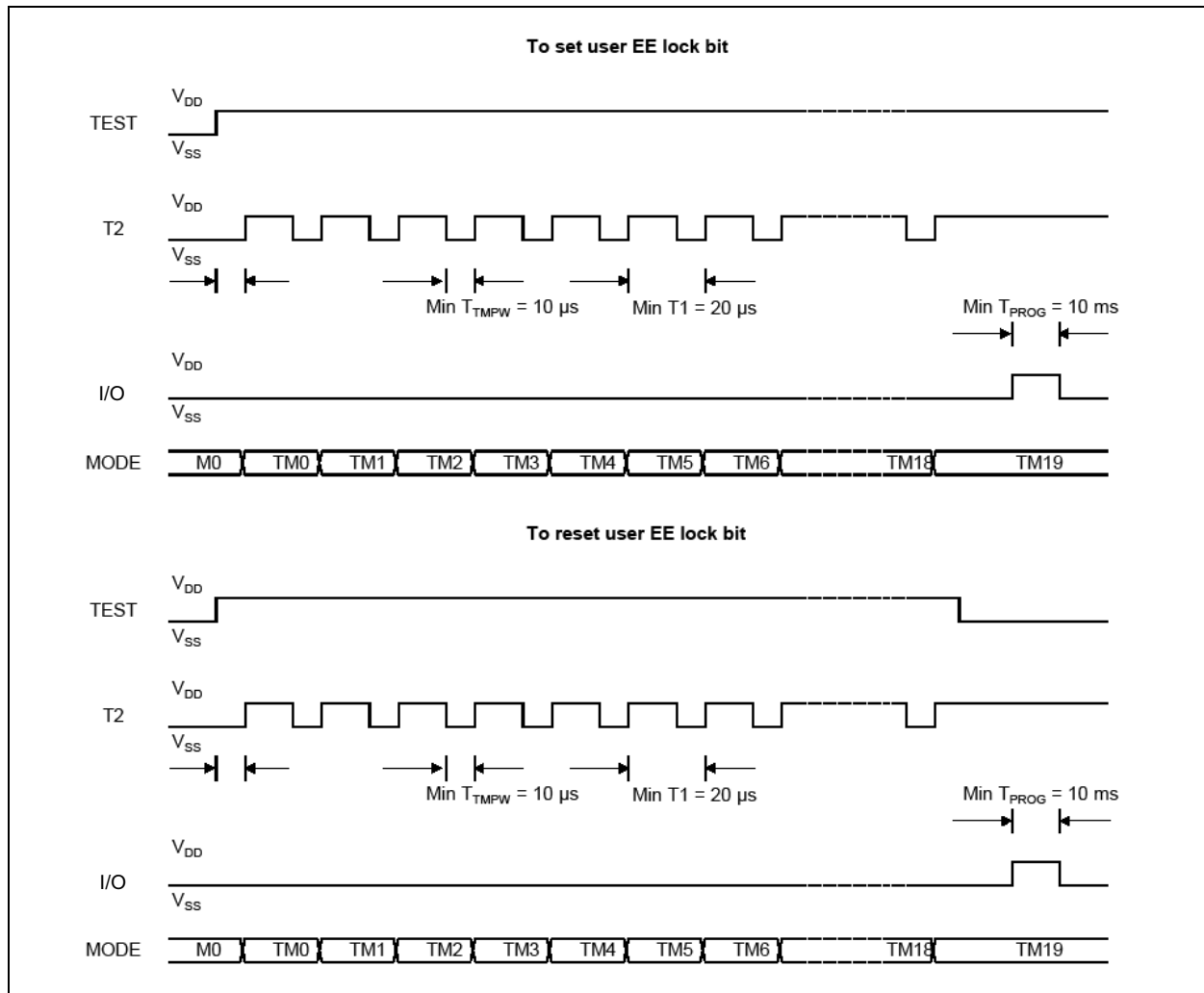


FIGURE 4-9: Timing Diagram for User Lock Bit Programming in Mode TM19.

NOTES:

5.0 APPLICATION NOTES

5.1 Standby Current Calculation

A calculation of the standby current is shown in [Table 5-1](#), which is based on the [Typical Application](#) and the following conditions:

V_{DD}	= 9V
LED Current in Loaded Battery	= 16.7 mA
Check ($V_{fLED}=2.0V$, $V_{DS}=0.5V$, $R1$ = 390)	
End-of-Life Enabled	= (EOLEn = 1)
Detection Integration Time	= 220 μs
IRED Current	= 200 mA

TABLE 5-1: STANDBY CURRENT CALCULATION

I_{DD} Component	Current (μA)	Duration (s)	Period (s)	Duty Cycle	Average Current (μA)
Fixed IDD	0.9	Always	Always	1	0.9
Photo Detection Current					
Smoke Detection					
Excluding IR Drive	170	5.00E-03	10	500E-6	86E-3
IR drive During Detection	200E+3	220E-6	10	20E-6	4.4
Subtotal					4.5
Chamber Test					
Excluding IR Drive	170	5.00E-03	320	16E-6	2.7E-3
IR drive During Detection	200E+3	220E-6	320	625E-9	138E-3
Subtotal					140E-3
Low-battery Check					
Unloaded	20	10E-3	80	125E-6	2.5E-3
Loaded	16.7E+3	10E-3	320	231E-6	522E-3
Subtotal					524E-3
End-of-Life					5E-6
Total					6.1

The following sections explain the current components in [Table 5-1](#).

5.1.1 FIXED IDD

This is the current draw from the internal oscillator, which is constantly running in a normal operation.

5.1.2 SMOKE DETECTION

This is the current draw from the smoke detection circuitry during the 5 ms smoke check period. This is done every 10s in normal standby operation.

The IR drive component of smoke detection typically is the biggest factor in the overall smoke detector current budget. Careful selection of integration time and IRED current can maximize detector battery life.

For the IR drive in [Table 5-1](#), the setting of 200 mA and 220 μs was selected, which reflects an average of 4 μA .

Reducing the integration time or the IRED current will decrease the IR drive component proportionately. For example, halving the integration time from 220 μs to 120 μs will halve the average current from 4.4 μA to 2.2 μA ; using a 100 μA IRED current and 100 μs integration time will reduce the average current to 1.1 μA .

Likewise, increasing to maximum settings will increase the current draw. Using a 440 μs integration time and 200 mA IRED yields a maximum (nominal) average current draw of 8.8 μA .

5.1.3 CHAMBER TEST

This is the current draw from the smoke detection circuitry during the 5 ms chamber test. This is done every 320s in normal standby operation.

The integration time, IRED current and gain factor settings also apply to the chamber test. However, since the check is less frequent, the average current contribution is relatively small. At most, this test will add around 0.3 μ A to the overall current budget.

5.1.4 LOW-BATTERY CHECK (UNLOADED)

This is the current draw from the low-battery detection circuitry during the 10 ms unloaded low-battery check period.

5.1.5 LOW-BATTERY CHECK (LOADED)

This is the current draw from the RLED during the 10 ms loaded low-battery check period. The 16.7 mA current load is based on an LED forward diode voltage of 2.0V, a driver $V_{DS(on)} = 0.5V$ and $R1 = 390\Omega$. This current will degrade as the battery voltage drops, eventually reducing to around 12 mA at a low-battery voltage of 7.2V.

Proper selection of a battery test load is needed to adequately test for a low-battery condition. Likewise, the selection of a low-battery voltage is also important to ensure sufficient horn levels in alarm and battery life.

5.1.6 END-OF-LIFE

This is the current draw to read EOL bits from EE and then increase by one, followed by writing the EOL bits back to EE. The average 5 pA cost of operating end-of-life is inconsequential to the overall current usage.

5.1.7 TOTAL CURRENT

This is the average total current draw in standby.

5.2 FUNCTIONAL TIMING DIAGRAMS

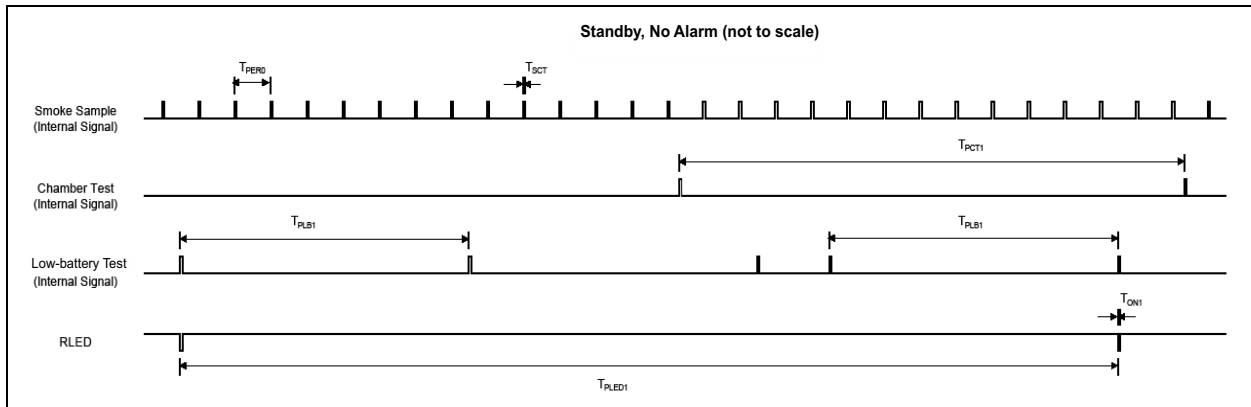


FIGURE 5-1: Timing Diagram – Standby, No Alarm.

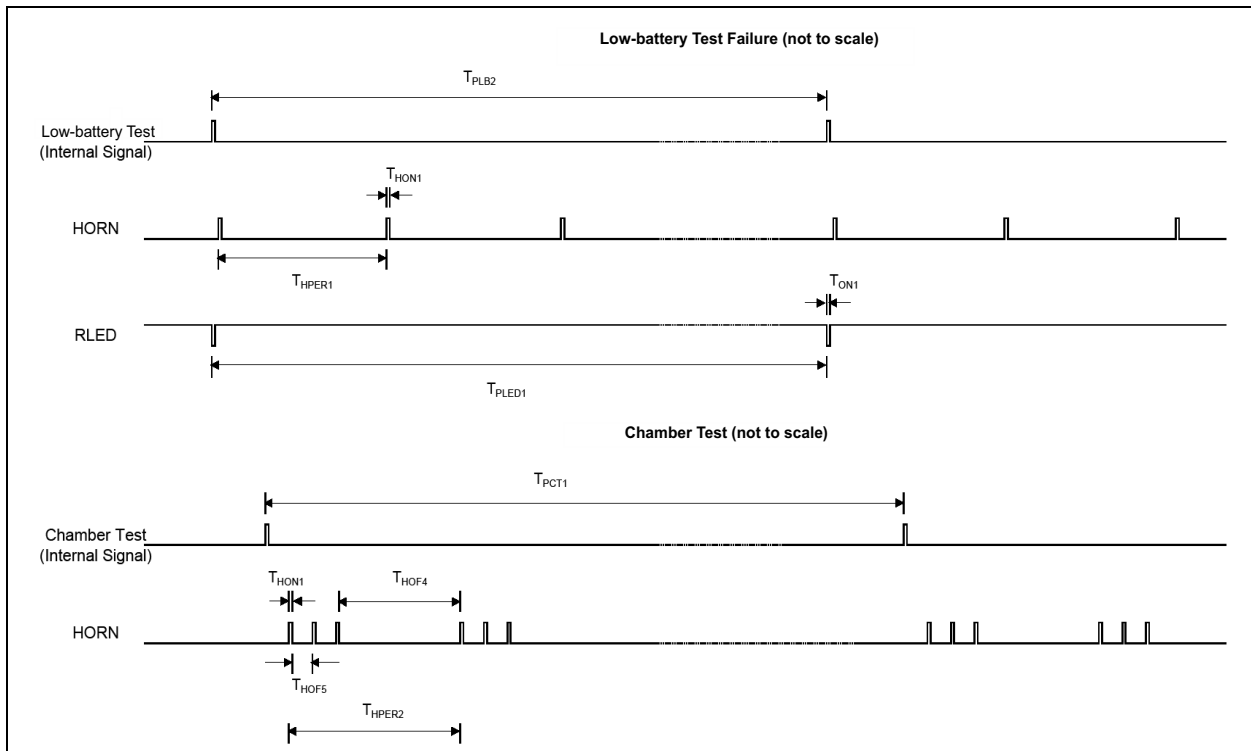


FIGURE 5-2: Timing Diagram – Low-Battery Test Failure and Chamber Test Failure.

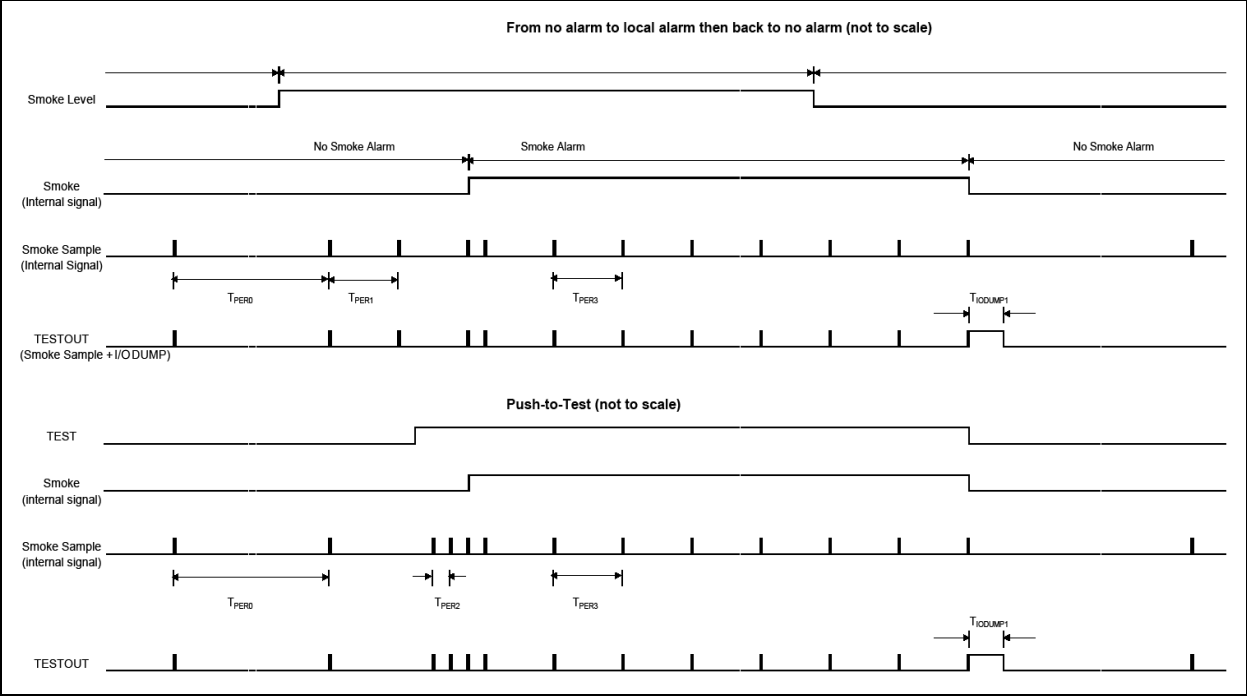


FIGURE 5-3: Timing Diagram – From Standby to Local Smoke and Push-To-Test.

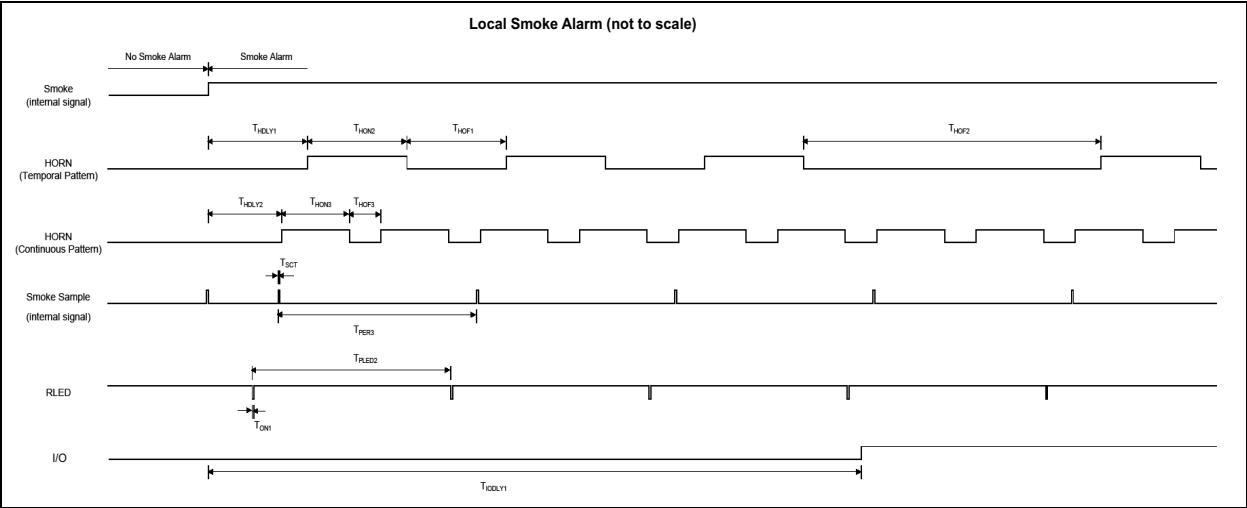


FIGURE 5-4: Timing Diagram – Local Smoke Alarm.

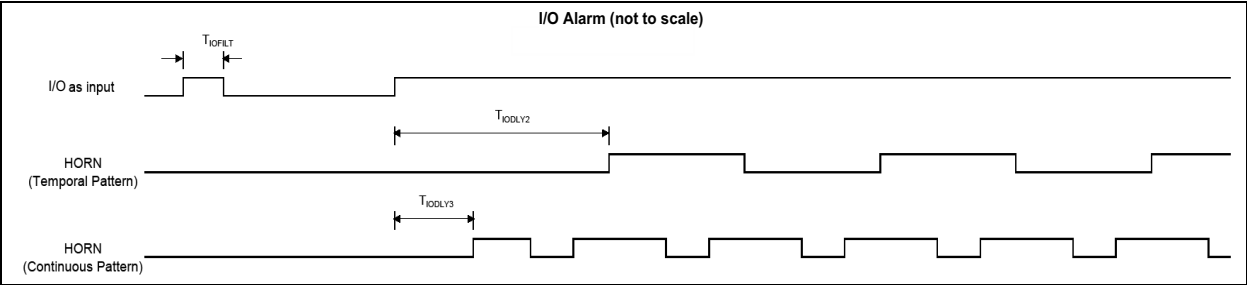


FIGURE 5-5: Timing Diagram – I/O Smoke Alarm.

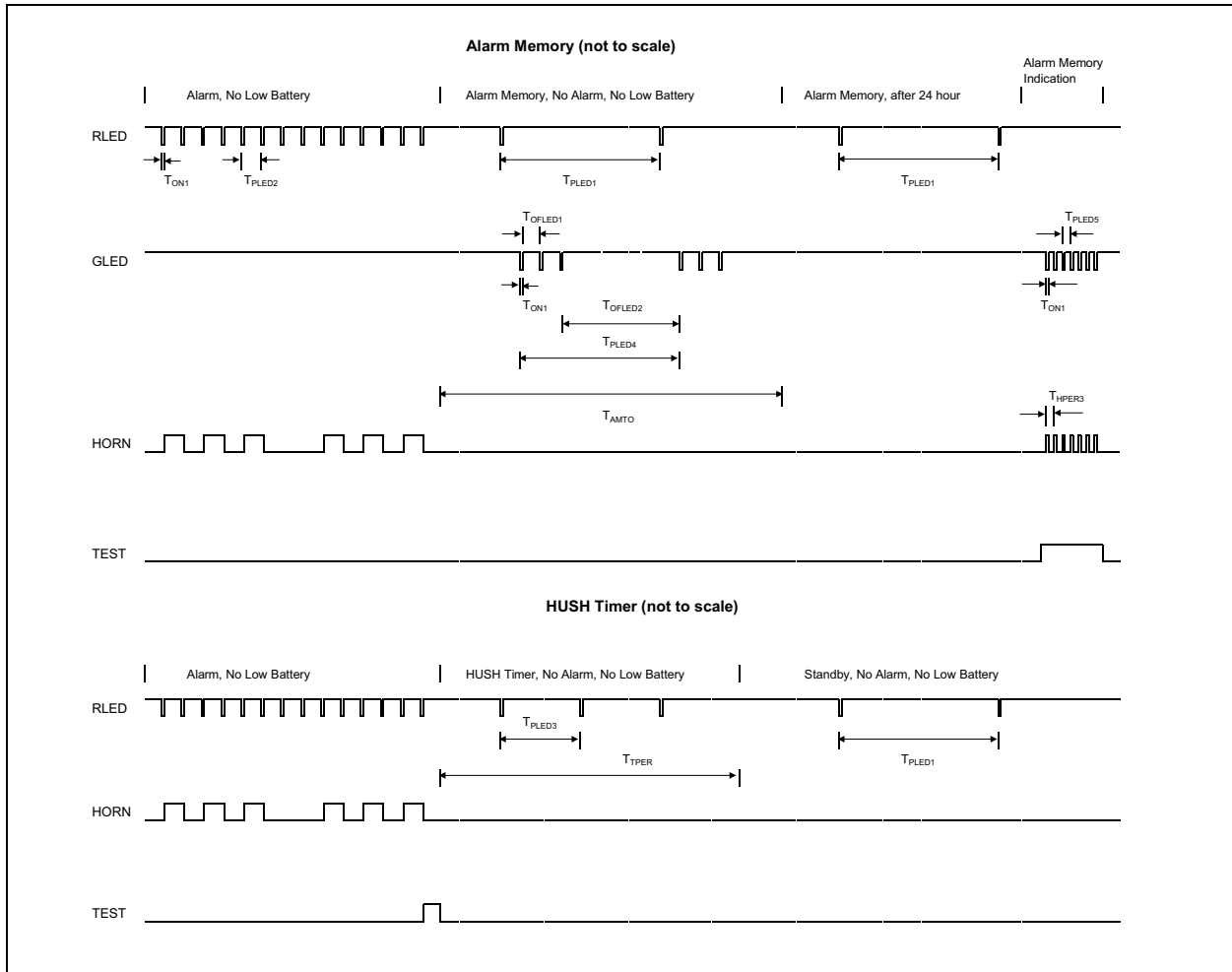


FIGURE 5-6: Timing Diagram – Alarm Memory and Hush Timer.

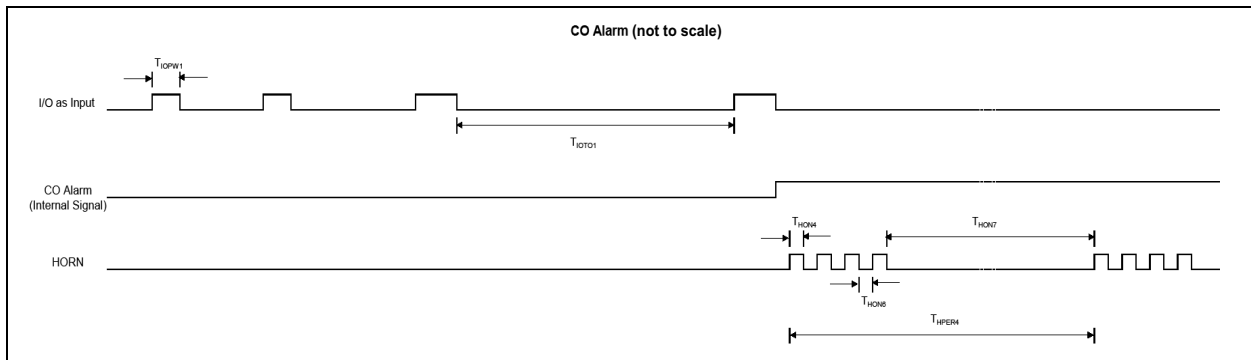


FIGURE 5-7: Timing Diagram – CO Alarm.

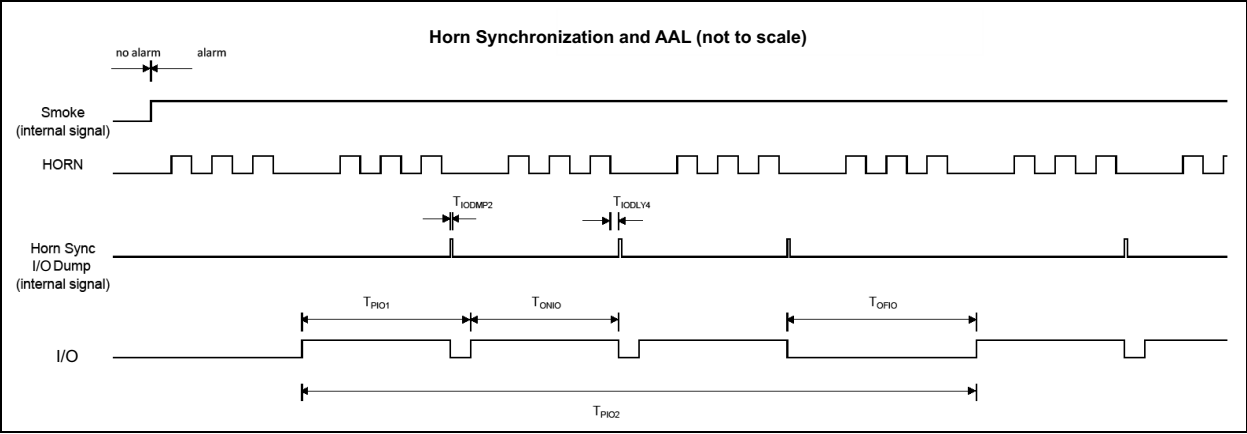
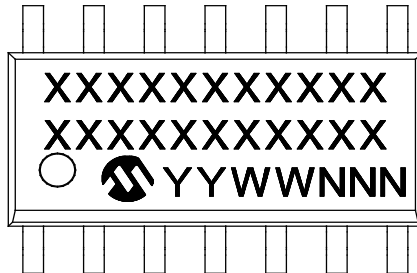


FIGURE 5-8: *Timing Diagram – Horn Synchronization and AAL.*

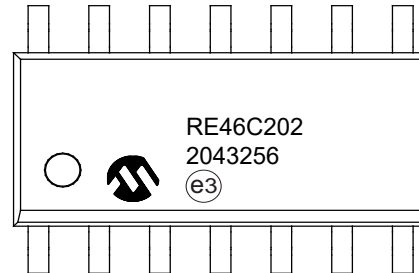
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

14-Lead SOIC (3.90 mm)



Example

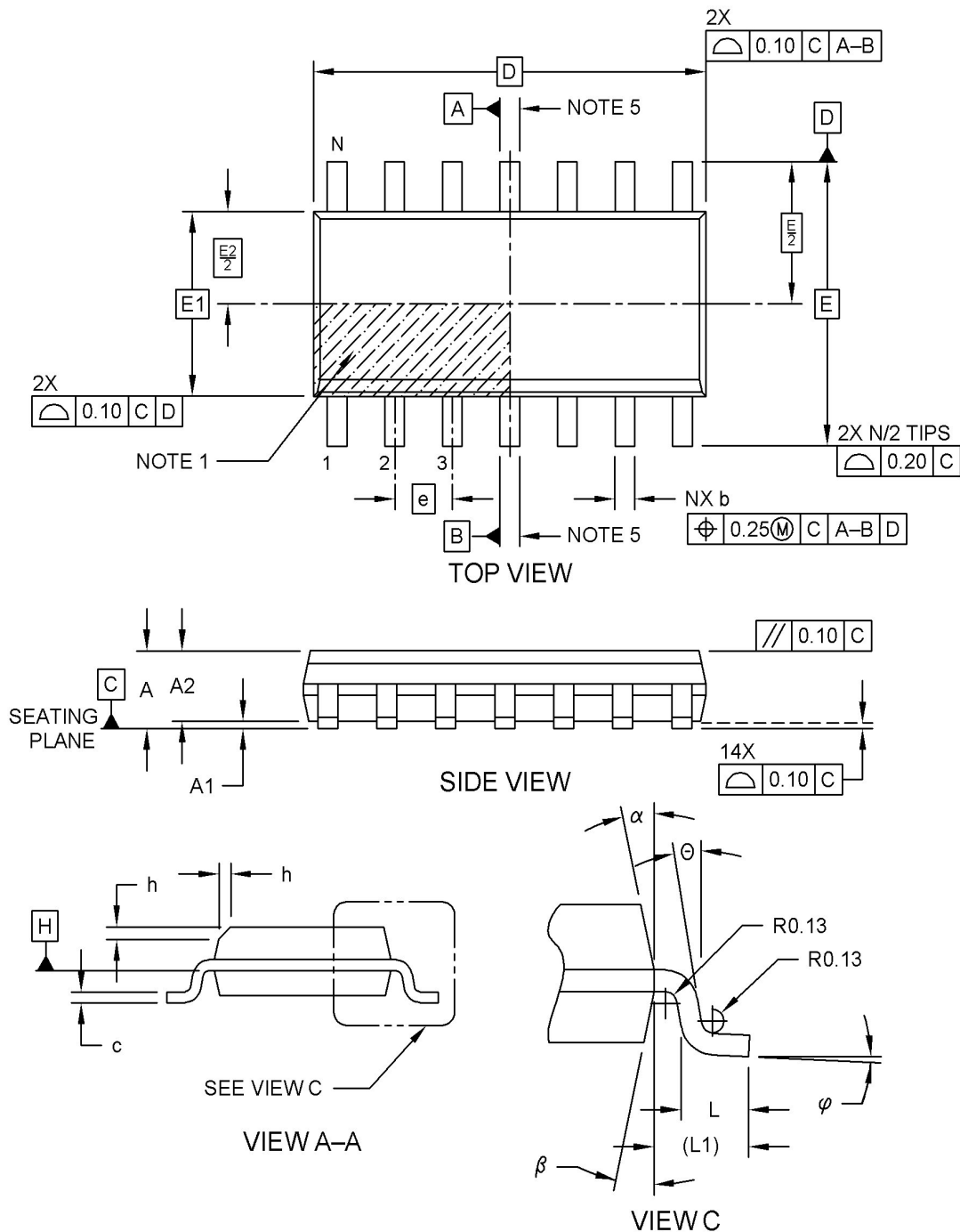


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

14-Lead Plastic Small Outline (D3X) - Narrow, 3.90 mm Body [SOIC]

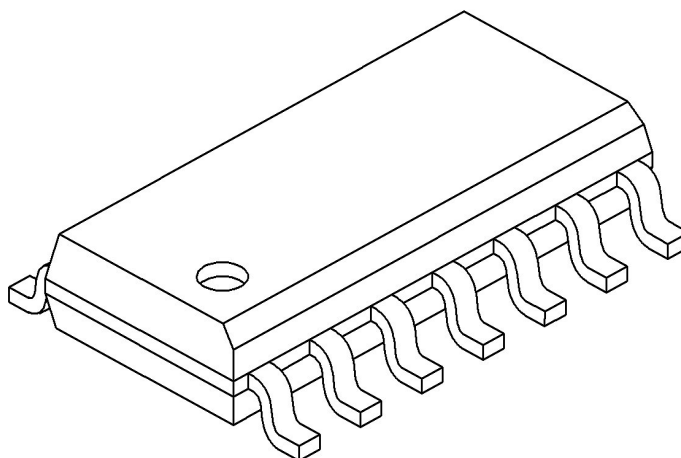
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-065-D3X Rev E Sheet 1 of 2

14-Lead Plastic Small Outline (D3X) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		14		
Pitch	e		1.27 BSC		
Overall Height	A		-	-	1.75
Molded Package Thickness	A2		1.25	-	-
Standoff §	A1		0.10	-	0.25
Overall Width	E		6.00 BSC		
Molded Package Width	E1		3.90 BSC		
Overall Length	D		8.65 BSC		
Chamfer (Optional)	h		0.25	-	0.50
Foot Length	L		0.40	-	1.27
Footprint	L1		1.04 REF		
Lead Angle	Ø		0°	-	-
Foot Angle	φ		0°	-	8°
Lead Thickness	c		0.10	-	0.25
Lead Width	b		0.31	-	0.51
Mold Draft Angle Top	α		5°	-	15°
Mold Draft Angle Bottom	β		5°	-	15°

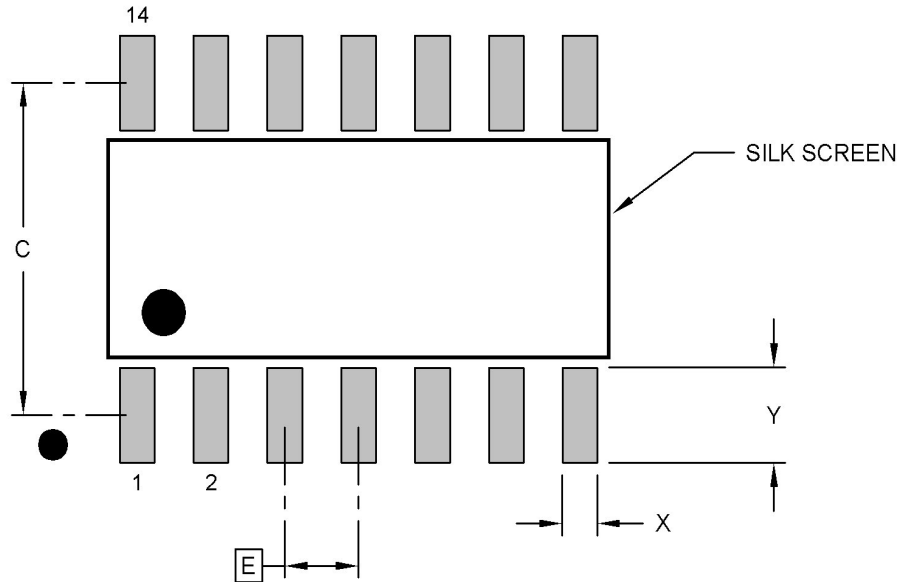
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-D3X Rev E Sheet 2 of 2

14-Lead Plastic Small Outline (D3X) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

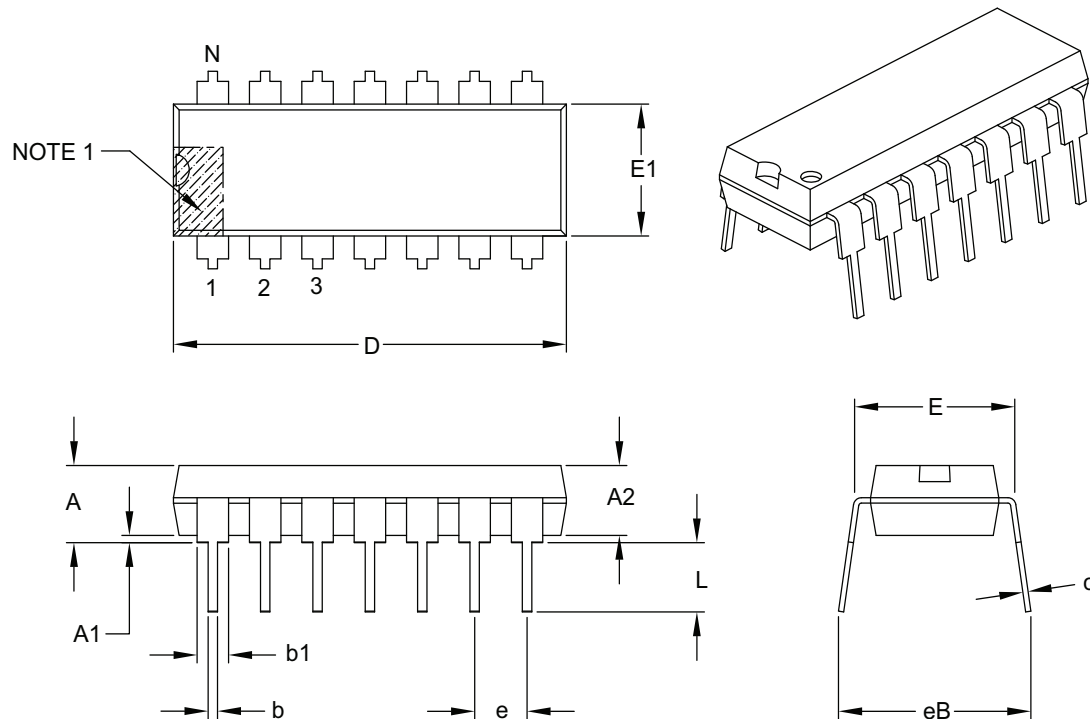
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-D3X Rev E

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

APPENDIX A: REVISION HISTORY

Revision B (April 2025)

The following is a list of modifications:

- Removed UL reference from [Section “Description”](#).
- Updated [Section 6.0, Packaging Information](#).
- Minor editorial corrections

Revision A (May 2022)

- Original release of this document

RE46C202

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>X</u>	<u>IXI</u> ⁽¹⁾	<u>X</u>
Device	Package	Number of Pins	Tape and Reel Option	Lead Free
Device:	RE46C202: Programmable Photoelectric Smoke Detector ASIC			
Package:	S14	=	Small Plastic Outline - Narrow, 3.90 mm Body (SOIC)	
Number of Pins:	14	=	14-Lead	
Tape and Reel Option:	Blank	=	Standard packaging (tube or tray)	
	T	=	Tape and Reel ⁽¹⁾	
Lead Free:	F	=	Lead Free	

Examples:
a) RE46C202S14: Programmable Photoelectric Smoke Detector ASIC, 14-Lead SOIC package, Lead Free
b) RE46C202S14T: Programmable Photoelectric Smoke Detector ASIC, 14-Lead SOIC package, Tape and Reel, Lead Free

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

RE46C202

NOTES:

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ISBN: 979-8-3371-0202-3

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