SN65DSI83 MIPI® DSI 桥转 FlatLink™ LVDS 单通道 DSI 转单链路 LVDS 桥接器

1 特性

- 实现了 MIPI® D-PHY 版本 1.00.00 物理层前端和显示串行接口 (DSI) 版本 1.02.00
- 单通道 DSI 接收器可配置为每通道 1、2、3 或 4 个 D-PHY 数据通道，运行速度高达 1Gbps/通道
- 支持格式为 RGB666 和 RGB888 的 18bpp 和 24bpp DSI 视频数据包
- 最大分辨率高达 60fps WUXGA 1920×1200（18bpp 和 24bpp 彩色），缩短消隐时间。适合 60fps 1366×768/1280×800（18bpp 和 24bpp）
- 单链路 LVDS 的 FlatLink™ 输出
- 支持单通道 DSI 至单链路 LVDS 运行模式
- LVDS 输出时钟范围为 25MHz 至 154MHz
- LVDS 像素时钟可采用自由运行持续 D-PHY 时钟或外部基准时钟 (REFCLK)
- 1.8V 主 V_{CC} 电源
- 低功耗特性包括关断模式、精简 LVDS 输出电压摆幅、共模和 MIPI 超低功耗状态 (ULPS) 支持
- 支持 LVDS 通道交换和 LVDS 引脚顺序反转功能，以方便 PCB 布线
- ESD 等级 ±2kV (HBM)
- 采用 64 引脚 5mm × 5mm nFBGA (ZXH) 封装
- 温度范围：–40°C 至 85°C

2 应用

- PC 和笔记本电脑
- 平板电脑
- 联网外设和打印机

3 说明

SN65DSI83 DSI 至 FlatLink 桥接器件特有一个单通道 MIPI D-PHY 接收器前端配置，此配置中在每个通道上具有 4 条信道，每条信道的运行速率为 1Gbps，最大输入带宽为 4Gbps。该桥接器可解码 MIPI DSI 18bpp RGB666 和 24bpp RGB888 视频流，并将格式化视频数据流转换为兼容 FlatLink 的 LVDS 输出（像素时钟范围为 25MHz 至 154MHz），从而提供单链路 LVDS（每个链路具有 4 个数据信道）。

SN65DSI83 器件可支持高达 WUXGA 1920 × 1200（每秒 60 帧，24bpp，采用简化消隐）的分辨率。此外，SN65DSI83 也适合采用 60fps 1366 × 768/1280 × 800（18bpp 和 24bpp）分辨率的应用。该器件实现了部分线路缓冲以适应 DSI 与 LVDS 接口间的数据流不匹配。

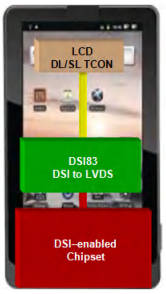
SN65DSI83 采用符合工业标准的接口技术设计，能够与多种微处理器兼容，并且具有多种功耗管理特性，包括低摆幅 LVDS 输出和 MIPI 定义的超低功耗状态 (ULPS) 支持。

SN65DSI83 器件采用小外形尺寸 5mm × 5mm nFBGA（0.5mm 间距）封装，工作温度范围为 –40ºC 至 85ºC。

器件信息(1)

器件型号	封装	封装尺寸
SN65DSI83	nFBGA (64)	5.00mm × 5.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



典型应用

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。
English Data Sheet: SLLSEC1

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (June 2018) to Revision I (October 2020) — **Page**

- 将 u*jrBGA ZQE 更改为 nFBGA ZXH 1
- Changed u*jr ZQE to nFBGA ZXH 4
- Changed u*jr ZQE to nFBGA ZXH. Updated thermal information 6
- Changed u*jr ZQE to nFBGA ZXH 39

Changes from Revision G (June 2015) to Revision H (June 2018) — **Page**

- Deleted figure *RESET and Initialization Timing Definition While V_{CC} is High* 10
- Changed the paragraph following 图 7-3 15
- Changed *Recommended Initialization Sequence* To: *Initialization Sequence* 16
- Changed 表 7-2 16
- Changed item 3 in *Video Stop and Restart Sequence* From: Drive all DSI input lanes including DSI CLK lane to LP11. To: Drive all DSI data lanes to LP11, but keep the DSI CLK lanes in HS. 31

Changes from Revision F (May 2015) to Revision G (June 2015) — **Page**

- Moved *Recommended Initialization Setup Sequence* 16
- Changed *SN65DSI83 DSI Lane Merging Illustration* back to original image 19

Changes from Revision E (October 2013) to Revision F (May 2015) — **Page**

- 添加了*引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- 根据全新 TI 标准更新了数据表，添加了章节并重新编排了内容 1
- Updated the *SN65DSI83 FlatLink Timing Definitions* diagram 10
- Changed *Functional Block Diagram* 13
- Changed *SN65DSI83 DSI Lane Merging Illustration* 19
- Changed from: 1366 × 768 WXGA to:1280 × 800 WXGA 32
- Changed *Design Parameters* table values 32
- Changed *Detailed Design Procedure* values and text 33

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- Changed *Example Script* subsection 36

Changes from Revision D (December 2012) to Revision E (October 2013) **Page**

- 将状态从“产品预发布”更改为“量产数据” 1

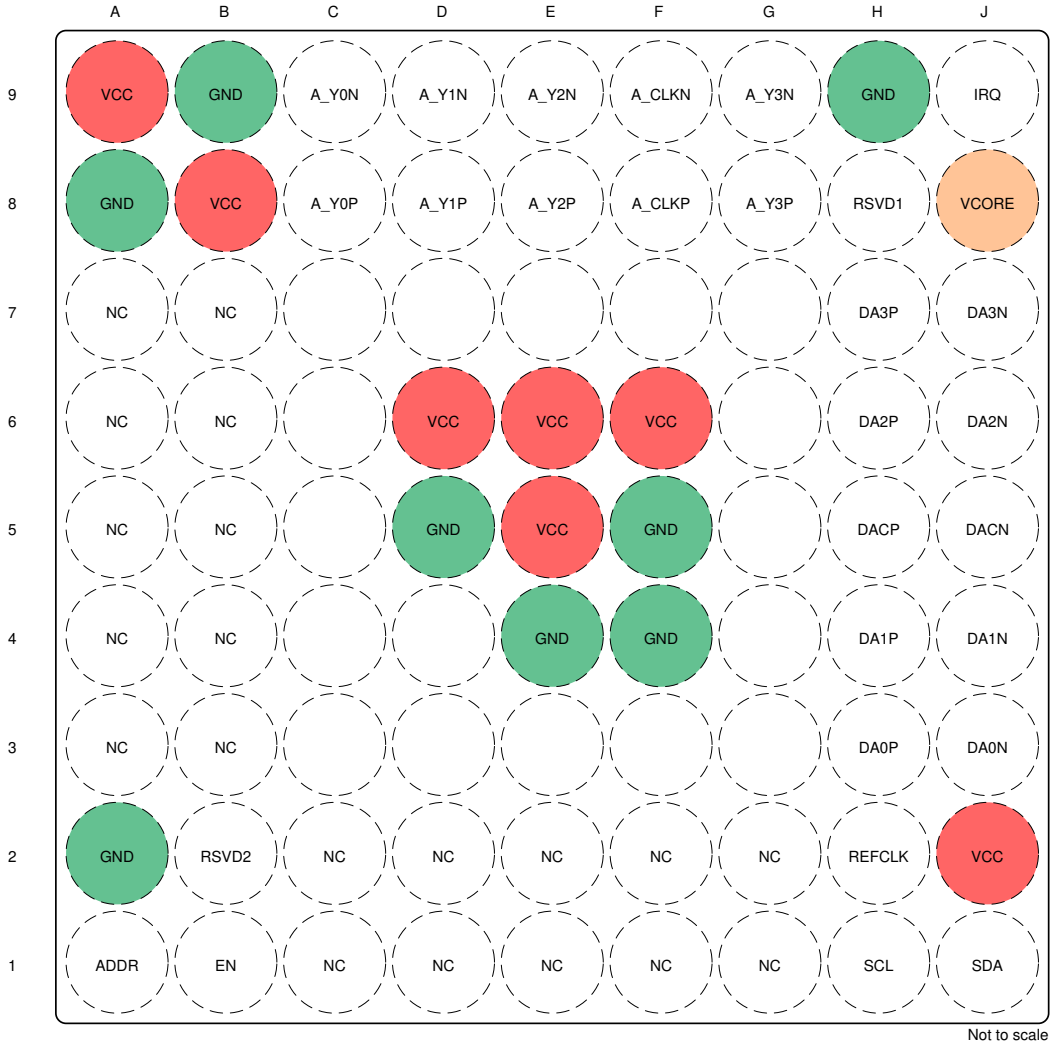
Changes from Revision A (September 2012) to Revision B (December 2012) **Page**

- Changed the value of V_{OH} From: 1.3 MIN To: 1.25 MIN 7
- Changed the I_{CC} TYP value From: TBD To: 77 and MAX value From: TBD To: 112 7
- Added a TYP value of 7.7 to I_{ULPS} 7
- Changed the I_{RST} TYP value From: 0.05 To: 0.04 and MAX value From: 0.2 To: 0.06 7
- changed the values of |VOD| 7
- Changed the values of $V_{OC(SS)}$ for test conditions CSR 0x19.6 = 0 7
- Added table note 2 7
- Added table note 3 7
- Changed the t_{setup} and t_{hold} NOM value of 1.5 to a MIN value of 1.5 8
- Changed the SWITCHING CHARACTERISTICS table 10
- Changed the description of CHA_LVDS_VOD_SWING 24

Changes from Revision * (August 2012) to Revision A (September 2012) **Page**

- 将“特性”从“最大分辨率高达 60fps WUXGA 1920 × 1200（18bpp 和 24bpp 彩色），缩短消隐时间。适合 60fps 1366 × 768（18bpp 和 24bpp）”更改为“最大分辨率高达 60fps WUXGA 1920 × 1200（18bpp 和 24bpp 彩色），缩短消隐时间。适合 60fps 1366 × 768/1280 × 800（18bpp 和 24bpp）” 1
- 更改了“说明”部分第二段中的文本，从“使用 60fps 1366 × 768（18bpp 和 24bpp）的应用。”修改为“使用 60fps 1366 × 768/1280 × 800（18bpp 和 24bpp）的应用。” 1

5 Pin Configuration and Functions



ZXH Package 64-Pin nFBGA (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A_CLKN	F9	LVDS output	FlatLink Channel A LVDS clock
A_CLKP	F8		
ADDR	A1	CMOS I/O	Local I^{2}C Interface Target Address Select. See 表 7-3. In normal operation, this pin is an input. When the ADDR pin is programmed high, it must be tied to the same 1.8-V power rails where the SN65DSI83 VCC 1.8-V power rail is connected.
A_Y0N	C9	LVDS output	FlatLink Channel A LVDS data output 0
A_Y0P	C8		
A_Y1N	D9		FlatLink Channel A LVDS data output 1
A_Y1P	D8		
A_Y2N	E9		FlatLink Channel A LVDS data output 2
A_Y2P	E8		
A_Y3N	G9		FlatLink Channel A LVDS data output 3. A_Y3P and A_Y3N shall be left NC for 18 bpp panels
A_Y3P	G8		

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表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DA0N	J3	LVDS Input (HS) CMOS Input (LS) (failsafe)	MIPI D-PHY Channel A Data Lane 0; data rate up to 1 Gbps
DA0P	H3		
DA1N	J4		MIPI D-PHY Channel A Data Lane 1; data rate up to 1 Gbps
DA1P	H4		
DA2N	J6		MIPI D-PHY Channel A Data Lane 2; data rate up to 1 Gbps
DA2P	H6		
DA3N	J7		MIPI D-PHY Channel A Data Lane 3; data rate up to 1 Gbps
DA3P	H7		
DACN	J5		MIPI D-PHY Channel A Clock Lane; operates up to 500 MHz
DACP	H5		
EN	B1	CMOS Input with pullup (failsafe)	Chip enable and reset. Device is reset (shutdown) when EN is low.
GND	A2, A8, B9, D5, E4, F4, F5, H9	Power Supply	Reference ground
IRQ	J9	CMOS Output	Interrupt signal
NC	B3, A3, B4, A4, B5, A5, B6, A6, B7, A7, C2, C1, D2, D1, F2, F1, G2, G1, E2, E1	No connects	These pins must not be connected to any signal, power or ground.
REFCLK	H2	CMOS Input (Failsafe)	Optional external reference clock for LVDS pixel clock. If an external reference clock is not used, this pin must be pulled to GND with an external resistor. The source of the reference clock must be placed as close as possible with a series resistor near the source to reduce EMI.
RSVD1	H8	CMOS Input/Output with pulldown	Reserved. This pin must be left unconnected for normal operation.
RSVD2	B2	CMOS Input with pulldown	Reserved. This pin must be left unconnected for normal operation.
SCL	H1	CMOS Input (Failsafe)	Local I^2C interface clock
SDA	J1	Open Drain I/O (failsafe)	Local I^2C interface bidirectional data signal
VCC	A9, B8, D6, E5, E6, F6, J2	Power Supply	1.8-V power supply
VCORE	J8		1.1-V output from voltage regulator. This pin must have a 1-μF external capacitor to GND.

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{CC}		– 0.3	2.175	V
Input voltage	CMOS input pins	– 0.5	2.175	V
	DSI input pins (DA × P/N, DB × P/N)	– 0.4	1.4	V
Storage temperature, T_{stg}		– 65	105	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	VCC power supply	1.65	1.8	1.95	V
V_{PSN}	Supply noise on any V_{CC} pin	$f_{(noise)}$ > 1 MHz		0.05	V
T_A	Operating free-air temperature	– 40		85	°C
T_{CASE}	Case temperature			92.2	
V_{DSI_PIN}	DSI input pin voltage range	– 50		1350	mV
Z_L	LVDS output differential impedance	90		132	Ω

6.4 Thermal Information

THERMAL METRIC[1]		SN65DSI83 ZXH (nFBGA) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.0	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	30.8	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IL}	Low-level control signal input voltage				0.3 × VCC	V
V_{IH}	High-level control signal input voltage		0.7 × VCC			V
V_{OH}	High-level output voltage	I_{OH} = –4 mA	1.25			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
I_{LKG}	Input failsafe leakage current	V_{CC} = 0; $V_{CC(PIN)}$ = 1.8 V			±30	µA
I_{IH}	High-level input current	Any input pin			±30	µA
I_{IL}	Low-level input current	Any input pin			±30	µA
I_{OZ}	High-impedance output current	Any output pin			±10	µA
I_{OS}	Short-circuit output current	Any output driving GND short			±20	mA
I_{CC}	Device active current	See [2]		77	112	mA
I_{ULPS}	Device standby current	All data and clock lanes are in ultra-low power state (ULPS)		7.7	10	mA
I_{RST}	Shutdown current	EN = 0		0.04	0.06	mA
R_{EN}	EN control input resistor			200		kΩ
MIPI DSI INTERFACE						
V_{IH-LP}	LP receiver input high threshold	See 图 6-2	880			mV
V_{IL-LP}	LP receiver input low threshold	See 图 6-2			550	mV
$\|V_{ID}\|$	HS differential input voltage		70		270	mV
$\|V_{IDT}\|$	HS differential input voltage threshold				50	mV
$V_{IL-ULPS}$	LP receiver input low threshold; ultra-low power state (ULPS)				300	mV
V_{CM-HS}	HS common mode voltage; steady-state		70		330	mV
ΔV_{CM-HS}	HS common mode peak-to-peak variation including symbol delta and interference				100	mV
V_{IH-HS}	HS single-ended input high voltage	See 图 6-2			460	mV
V_{IL-HS}	HS single-ended input low voltage	See 图 6-2	–40			mV
$V_{TERM-EN}$	HS termination enable; single-ended input voltage (both Dp and Dn apply to enable)	Termination is switched simultaneous for Dn and Dp			450	mV
$R_{DIFF-HS}$	HS mode differential input impedance		80		125	Ω

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
FlatLink LVDS OUTPUT						
$\|V_{OD}\|$	Steady-state differential output voltage for A_Y x P/N and B_Y x P/N	CSR 0x19.3:2 = 00 100-Ω near-end termination	180	245	313	mV
		CSR 0x19.3:2 = 01 100-Ω near-end termination	215	293	372	
		CSR 0x19.3:2 = 10 100-Ω near-end termination	250	341	430	
		CSR 0x19.3:2 = 11 100-Ω near-end termination	290	389	488	
		CSR 0x19.3:2 = 00 200-Ω near-end termination	150	204	261	
		CSR 0x19.3:2 = 01 200-Ω near-end termination	200	271	346	
		CSR 0x19.3:2 = 10 200-Ω near-end termination	250	337	428	
		CSR 0x19.3:2 = 11 200-Ω near-end termination	300	402	511	
	Steady-state differential output voltage for A_CLKP/N and B_CLKP/N	CSR 0x19.3:2 = 00 100-Ω near-end termination	140	191	244	mV
		CSR 0x19.3:2 = 01 100-Ω near-end termination	168	229	290	
		CSR 0x19.3:2 = 01 100-Ω near-end termination	195	266	335	
		CSR 0x19.3:2 = 11 100-Ω near-end termination	226	303	381	
		CSR 0x19.3:2 = 00 200-Ω near-end termination	117	159	204	
		CSR 0x19.3:2 = 01 200-Ω near-end termination	156	211	270	
		CSR 0x19.3:2 = 10 200-Ω near-end termination	195	263	334	
		CSR 0x19.3:2 = 11 200-Ω near-end termination	234	314	399	
$\Delta\|V_{OD}\|$	Change in steady-state differential output voltage between opposite binary states	RL = 100 Ω			35	mV
$V_{OC(SS)}$	Steady state common-mode output voltage (3)	CSR 0x19.6 = 1 and CSR 0x1B.6 = 1 (see 图 6-3)	0.8	0.9	1	V
		CSR 0x19.6 = 0 (see 图 6-3)	1.15	1.25	1.35	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See 图 6-3			35	mV
R_{LVDS_DIS}	Pulldown resistance for disabled LVDS outputs			1		kΩ

(1) All typical values are at V_{CC} = 1.8 V and T_A = 25°C.
(2) SN65DSI83: SINGLE Channel DSI to SINGLE Channel DSI, 1280 × 800
- Number of LVDS lanes = 3 data lanes + 1 CLK lane
- Number of DSI lanes = 4 data lanes + 1 CLK lane
- LVDS CLK OUT = 83 M
- DSI CLK = 500 M
- RGB888, LVDS 18 bpp

Maximum values are at V_{CC} = 1.95 V and T_A = 85°C
(3) Tested at V_{CC} = 1.8 V , T_A = –40°C for MIN, T_A = 25°C for TYP, T_A = 85°C for max.

6.6 Timing Requirements

		MIN	TYP	MAX	UNIT
$f_{(I2C)}$	Local I^2C input frequency			400	kHz

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		MIN	TYP	MAX	UNIT
f_{HS_CLK}	DSI HS clock input frequency	40		500	MHz
t_{setup}	DSI HS data to clock setup time	0.15			UI[(1)]
t_{hold}	DSI HS data to clock hold time; see 图 6-1	0.15			

(1) The unit interval (UI) is one half of the period of the HS clock; at 500 MHz the minimum setup and hold time is 150 ps.

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
DSI						
t_{GS}	DSI LP glitch suppression pulse width				300	ps
LVDS						
t_c	Output clock period		6.49		40	ns
t_w	High-level output clock (CLK) pulse duration			4 / 7 t_c		ns
t_0	Delay time, CLK ↑ to 1st serial bit position	t_c = 6.49 ns; Input clock jitter < 25 ps (REFCLK)	–0.15		0.15	ns
t_1	Delay time, CLK ↑ to 2nd serial bit position		1 / 7 t_c – 0.15		1 / 7 t_c + 0.15	ns
t_2	Delay time, CLK ↑ to 3rd serial bit position		2 / 7 t_c – 0.15		2 / 7 t_c + 0.15	ns
t_3	Delay time, CLK ↑ to 4th serial bit position		3 / 7 t_c – 0.15		3 / 7 t_c + 0.15	ns
t_4	Delay time, CLK ↑ to 5th serial bit position		4 / 7 t_c – 0.15		4 / 7 t_c + 0.15	ns
t_5	Delay time, CLK ↑ to 6th serial bit position		5 / 7 t_c – 0.15		5 / 7 t_c + 0.15	ns
t_6	Delay time, CLK ↑ to 7th serial bit position		6 / 7 t_c – 0.15		6 / 7 t_c + 0.15	ns
t_r	Differential output rise time	See 图 6-4	180		500	ps
t_f	Differential output fall time					
EN, ULPS, RESET						
t_{en}	Enable time from EN or ULPS	$t_{c(o)}$ = 12.9 ns			1	ms
t_{dis}	Disable time to standby				0.1	
t_{reset}	Reset Time		10			ms
REFCLK						
F_{REFCLK}	REFCLK freqeuncy. Supported frequencies: 25 MHz to 154 MHz		25		154	MHz
t_r, t_f	REFCLK rise and fall time		100 ps		1 ns	s
t_{pj}	REFCLK peak-to-peak phase jitter				50	ps
Duty	REFCLK duty cycle		40%	50%	60%	
REFCLK or DSI CLK (DACP/N, DBCP/N)						
SSC_CLKIN	SSC enabled input CLK center spread depth [2]		0.5%	1%	2%	
	Modulation frequency range		30		60	kHz

(1) All typical values are at V_{CC} = 1.8 V and T_A = 25°C
(2) For EMI reduction purpose, the SN65DSI83 device supports the center spreading of the LVDS CLK output through the REFCLK or DSI CLK input. The center spread CLK input to the REFCLK or DSI CLK is passed through to the LVDS CLK output A_CLKP and A_CLKN, or B_CLKP and B_CLKN, or both.

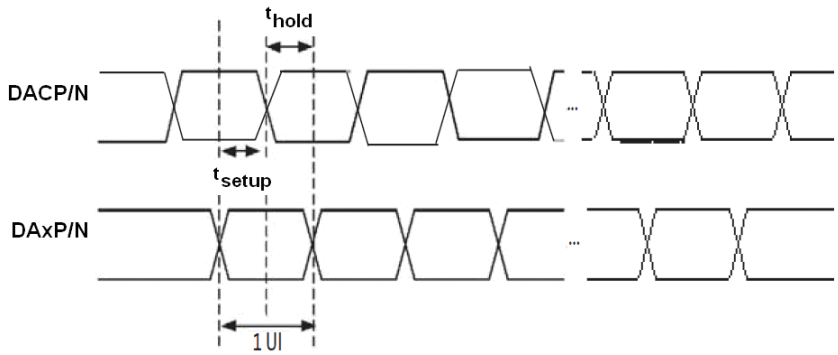

图 6-1. DSI HS Mode Receiver Timing Definitions

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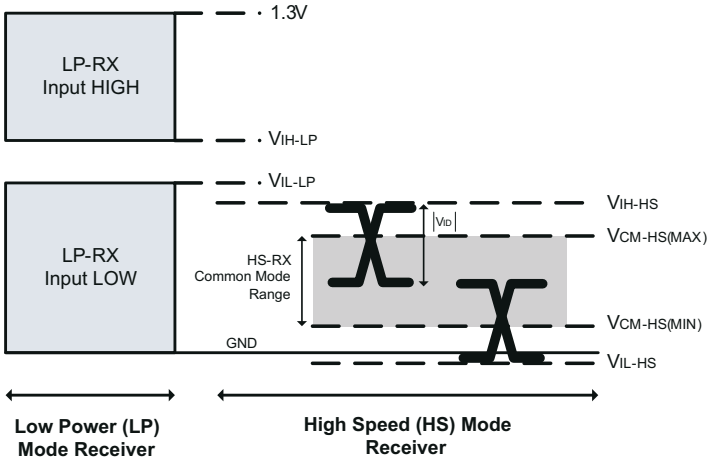


图 6-2. DSI Receiver Voltage Definitions

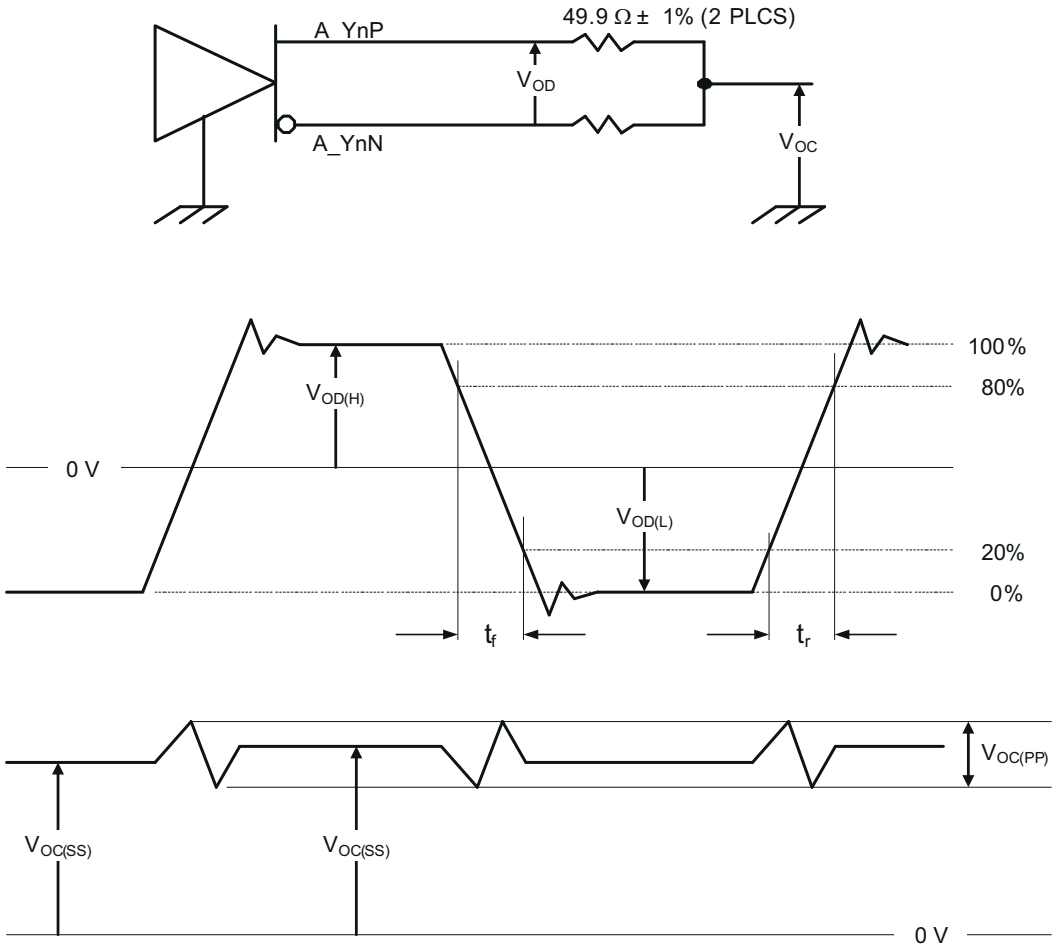


图 6-3. Test Load and Voltage Definitions for FlatLink Outputs

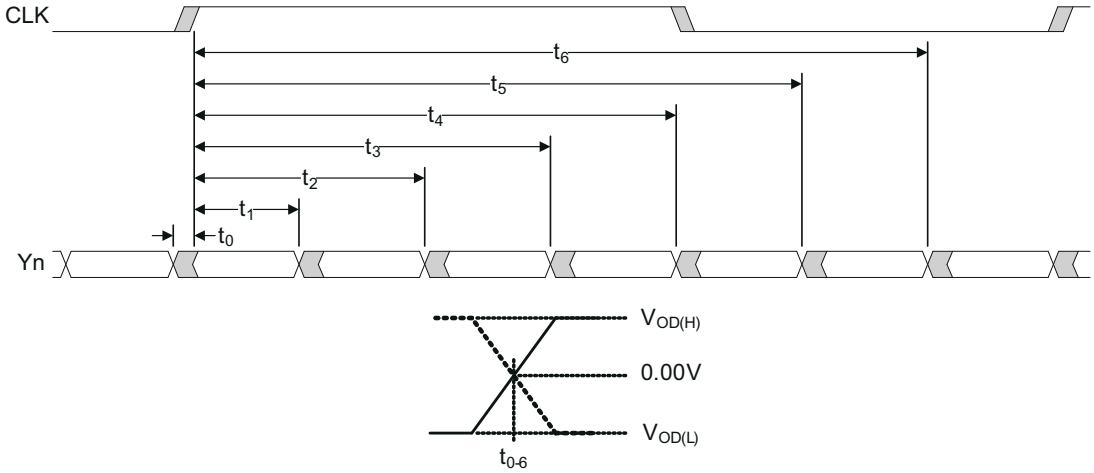
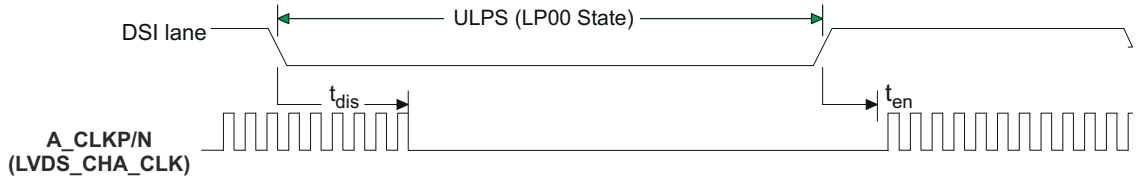


图 6-4. SN65DSI83 FlatLink Timing Definitions



A. See 节 7.3.2 for the ULPS entry and exit sequence.
B. ULPS entry and exit protocol and timing requirements must be met per MIPI DPHY specification.

图 6-5. ULPS Timing Definition

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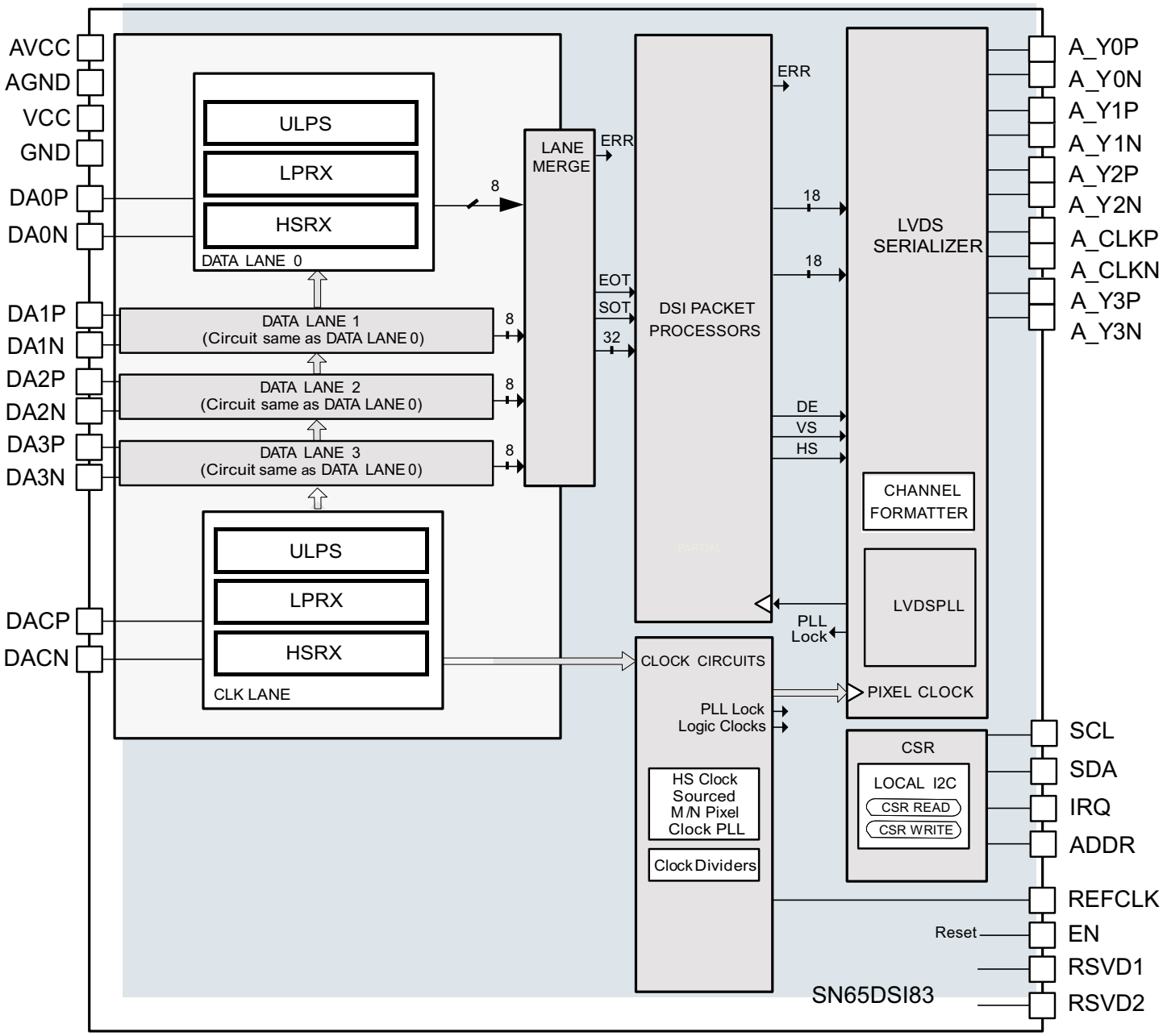
7 Detailed Description

7.1 Overview

The SN65DSI83 DSI to FlatLink bridge device features a single-channel MIPI® D-PHY receiver front-end configuration with four lanes per channel operating at 1 Gbps per lane; a maximum input bandwidth of 4 Gbps. The bridge decodes MIPI DSI 18 bpp RGB666 and 24 bpp RGB888 packets and converts the formatted video data stream to a FlatLink compatible LVDS output operating at pixel clocks operating from 25 MHz to 154 MHz, offering a Single-Link LVDS with four data lanes per link.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Clock Configurations and Multipliers

The FlatLink LVDS clock may be derived from the DSI channel A clock, or from an external reference clock source. When the MIPI D-PHY channel A HS clock is used as the LVDS clock source, the D-PHY clock lane must operate in HS free-running (continuous) mode. This feature eliminates the need for an external reference clock reducing system costs

The reference clock source is selected by HS_CLK_SRC (CSR 0x0A.0) programmed through the local I^2C interface. If an external reference clock is selected, it is multiplied by the factor in REFCLK_MULTIPLIER (CSR 0x0B.1:0) to generate the FlatLink LVDS output clock. When an external reference clock is selected, it must be between 25 MHz and 154 MHz. If the DSI channel A clock is selected, it is divided by the factor in DSI_CLK_DIVIDER (CSR 0x0B.7:3) to generate the FlatLink LVDS output clock. Additionally, LVDS_CLK_RANGE (CSR 0x0A.3:1) and CH_DSI_CLK_RANGE(CSR 0x12) must be set to the frequency range of the FlatLink LVDS output clock and DSI Channel A input clock respectively for the internal PLL to operate correctly. After these settings are programmed, PLL_EN (CSR 0x0D.0) must be set to enable the internal PLL.

7.3.2 ULPS

The SN65DSI83 device supports the MIPI defined ULPS. While the device is in the ULPS, the CSR registers are accessible via I^2C interface. ULPS sequence must be issued to all active DSI CLK and, or DSI data lanes of the enabled DSI channels for the SN65DSI83 device to enter the ULPS. The following sequence must be followed to enter and exit the ULPS.

1. The host issues a ULPS entry sequence to all DSI CLK and data lanes enabled.
2. When the host is ready to exit the ULPS mode, the host issues a ULPS exit sequence to all DSI CLK and data lanes that need to be active in normal operation.
3. Wait for the PLL_LOCK bit (CSR 0x0A.7) to be set.
4. Set the SOFT_RESET bit (CSR 0x09.0).
5. Device resumes normal operation (that is, video streaming resumes on the panel).

7.3.3 LVDS Pattern Generation

The SN65DSI83 device supports a pattern generation feature on LVDS channels. This feature can be used to test the LVDS output path and LVDS panels in a system platform. The pattern generation feature can be enabled by setting the CHA_TEST_PATTERN bit at address 0x3C. No DSI data is received while the pattern generation feature is enabled.

There are three modes available for LVDS test pattern generation. The mode of test pattern generation is determined by register configuration, as shown in 表 7-1.

表 7-1. Video Registers

ADDRESS BIT	REGISTER NAME
0x20.7:0	CHA_ACTIVE_LINE_LENGTH_LOW
0x21.3:0	CHA_ACTIVE_LINE_LENGTH_HIGH
0x24.7:0	CHA_VERTICAL_DISPLAY_SIZE_LOW
0x25.3:0	CHA_VERTICAL_DISPLAY_SIZE_HIGH
0x2C.7:0	CHA_HSYNC_PULSE_WIDTH_LOW
0x2D.1:0	CHA_HSYNC_PULSE_WIDTH_HIGH
0x30.7:0	CHA_VSYNC_PULSE_WIDTH_LOW
0x31.1:0	CHA_VSYNC_PULSE_WIDTH_HIGH
0x34.7:0	CHA_HORIZONTAL_BACK_PORCH
0x36.7:0	CHA_VERTICAL_BACK_PORCH
0x38.7:0	CHA_HORIZONTAL_FRONT_PORCH

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表 7-1. Video Registers (continued)

ADDRESS BIT	REGISTER NAME
0x3A.7:0	CHA_VERTICAL_FRONT_PORCH

7.4 Device Functional Modes

7.4.1 Reset Implementation

When EN is deasserted (low), the SN65DSI83 device is in shutdown or reset state. In this state, CMOS inputs are ignored, the MIPI D-PHY inputs are disabled and outputs are high impedance. It is critical to transition the EN input from a low level to a high level after the V_{CC} supply has reached the minimum operating voltage, as shown in 图 7-1. This is achieved by a control signal to the EN input, or by an external capacitor connected between EN and GND.

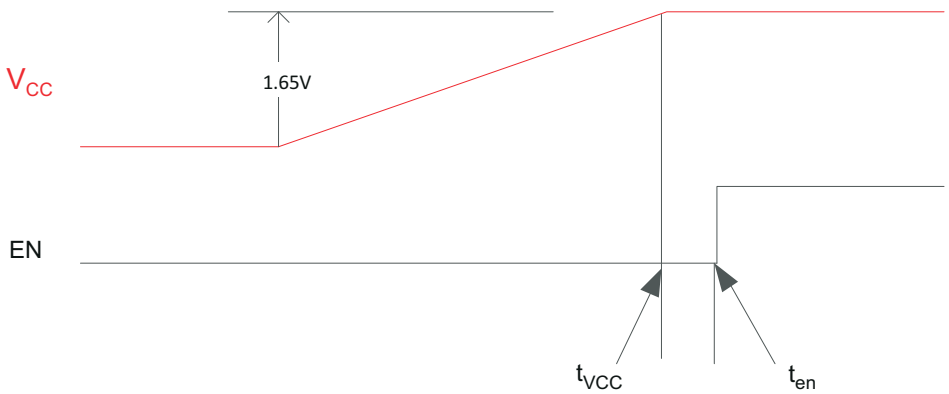

图 7-1. Cold Start V_{CC} Ramp up to EN

When implementing the external capacitor, the size of the external capacitor depends on the power-up ramp of the V_{CC} supply, where a slower ramp-up results in a larger value external capacitor. See the latest reference schematic for the SN65DSI83 device and, or consider approximately 200-nF capacitor as a reasonable first estimate for the size of the external capacitor.

Both EN implementations are shown in 图 7-2 and 图 7-3.

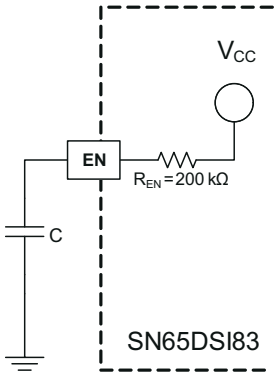

图 7-2. External Capacitor Controlled EN

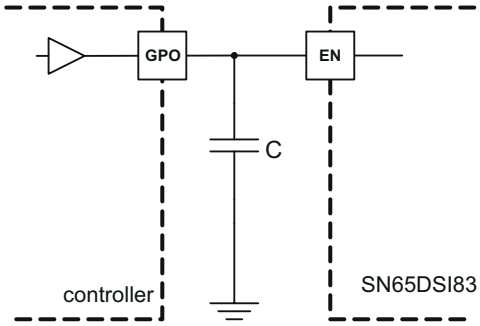

图 7-3. EN Input from Active Controller

When the SN65DSI83 is reset while V_{CC} is high, the EN pin must be held low for at least 10 ms before being asserted high as described in 表 7-2 to be sure that the device is properly reset. The DSI CLK lane MUST be in HS and the DSI data lanes MUST be driven to LP11 while the device is in reset before the EN pin is asserted per the timing described in 表 7-2.

7.4.2 Initialization Sequence

Use the following initialization sequence to setup the SN65DSI83. This sequence is required for proper operation of the device. Steps 9 through 11 in the sequence are optional.

表 7-2. Initialization Sequence

INITIALIZATION SEQUENCE NUMBER	INITIALIZATION SEQUENCE DESCRIPTION
Init seq 1	Power on
Init seq 2	After power is applied and stable, the DSI CLK lanes MUST be in HS state and the DSI data lanes MUST be driven to LP11 state
Init seq 3	Set EN pin to Low
Wait 10 ms (1)	
Init seq 4	Tie EN pin to High
Wait 10 ms (1)	
Init seq 5	Initialize all CSR registers to their appropriate values based on the implementation (The SN65DSI8x is not functional until the CSR registers are initialized)
Init seq 6	Set the PLL_EN bit (CSR 0x0D.0)
Wait 10 ms (1)	
Init seq 7	Set the SOFT_RESET bit (CSR 0x09.0)
Wait 10 ms (1)	
Init seq 8	Change DSI data lanes to HS state and start DSI video stream
Wait 5 ms (1)	
Init seq 9	Read back all resisters and confirm they were correctly written
Init seq 10	Write 0xFF to CSR 0xE5 to clear the error registers
Wait 1 ms (1)	
Init seq 11	Read CSR 0xE5. If CSR 0xE5!= 0x00, then go back to step #2 and re-initialize

(1) Minimum recommended delay. It is fine to exceed these.

7.4.3 LVDS Output Formats

The SN65DSI83 device processes DSI packets and produces video data driven to the FlatLink LVDS interface in an industry standard format. Single-Link LVDS is supported by the SN65DSI83 device. During conditions such as the default condition, and some video synchronization periods, where no video stream data is passing from the DSI input to the LVDS output, the SN65DSI83 device transmits zero value pixel data on the LVDS outputs while maintaining transmission of the vertical sync and horizontal sync status.

图 7-4 illustrates a Single-Link LVDS 18 bpp application.

图 7-5 illustrates a Single-Link 24 bpp application using Format 2, controlled by CHA_24BPP_FORMAT1 (CSR 0x18.1). In data Format 2, the two MSB per color are transferred on the Y3P/N LVDS lane.

图 7-6 illustrates a 24 bpp Single-Link application using Format 1. In data Format 1, the two LSB per color are transferred on the Y3P/N LVDS lane.

图 7-7 illustrates a Single-Link LVDS application where 24 bpp data is received from DSI and converted to 18 bpp data for transmission to an 18 bpp panel. This application is configured by setting CHA_24BPP_FORMAT1 (CSR 0x18.1) to 1 and CHA_24BPP_MODE (CSR 0x18.3) to 0. In this configuration, the SN65DSI83 device does not transmit the 2 LSB per color since the Y3P and Y3N LVDS lane is disabled.

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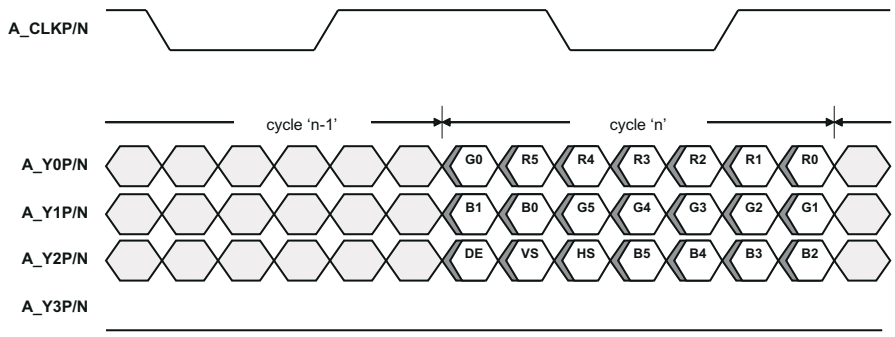
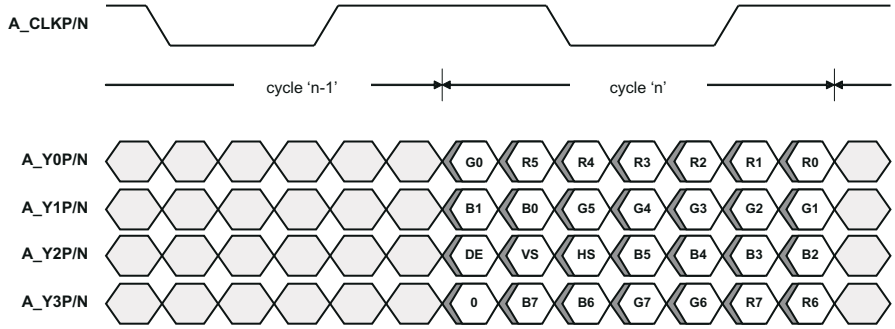
备注

图 7-4, 图 7-5, 图 7-6, and 图 7-7 only illustrate a few example applications for the SN65DSI83 device. Other applications are also supported.



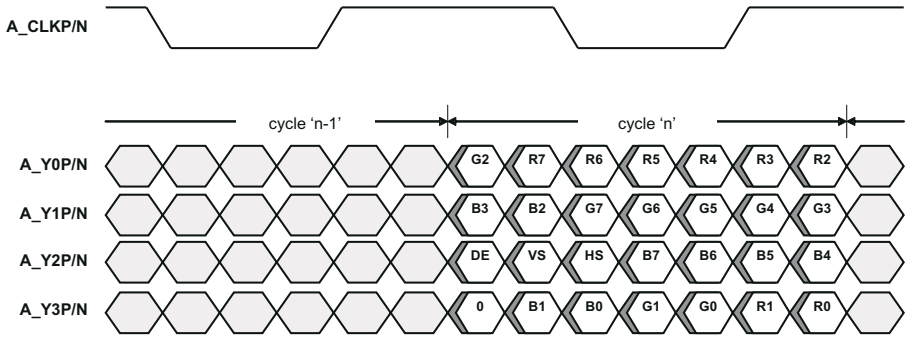
DE = Data Enable; A_Y3P/N are Output Low

图 7-4. FlatLink Output Data; Single-Link 18 bpp



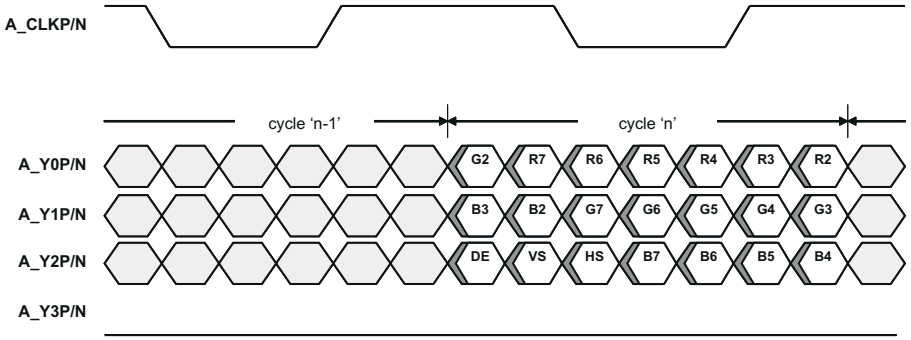
DE = Data Enable

图 7-5. FlatLink Output Data (Format 2); Single-Link 24 bpp



DE = Data Enable

图 7-6. FlatLink Output Data (Format 1); Single-Link 24 bpp



DE = Data Enable; A_Y3P and A_Y3N are output low; A_Y3P and A_Y3N are output low

图 7-7. FlatLink Output Data (Format 1); 24 bpp to Single-Link 18 bpp Conversion

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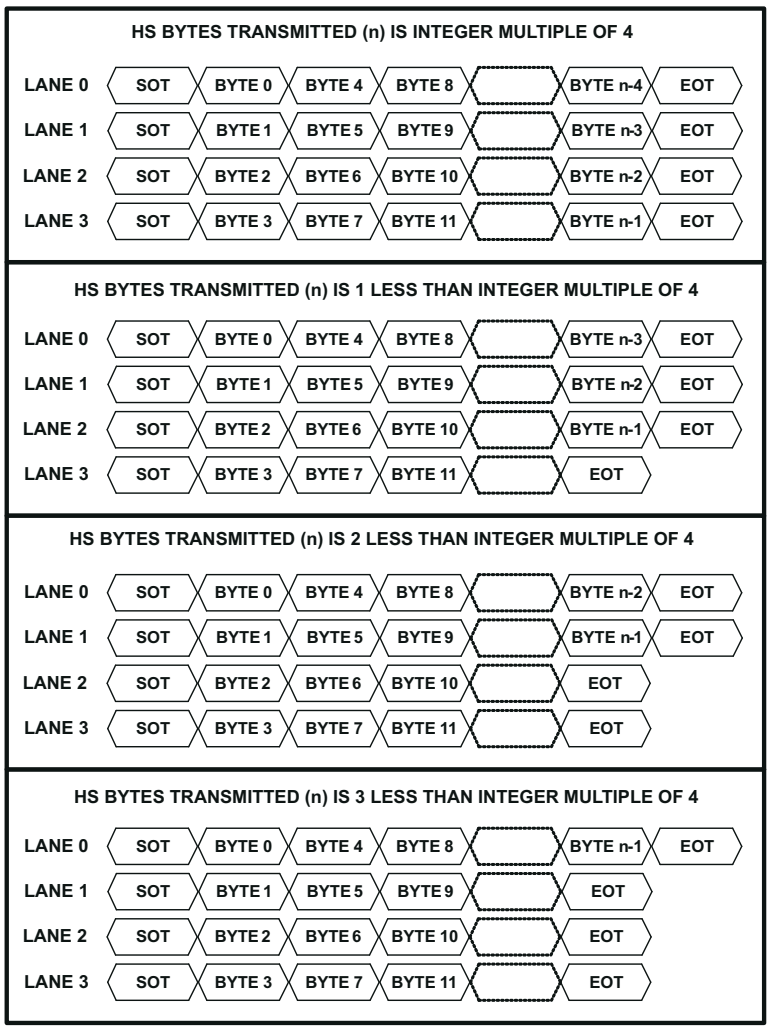
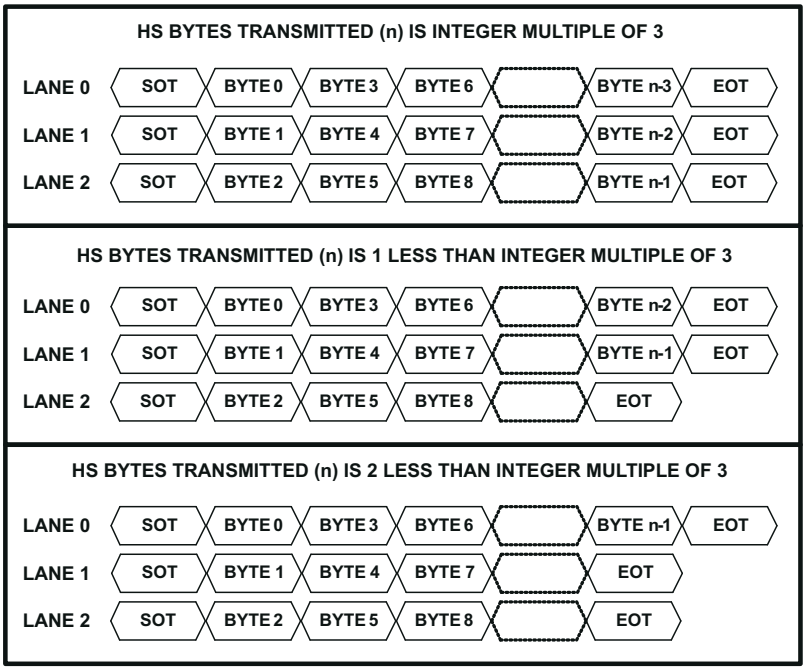
7.4.4 DSI Lane Merging

The SN65DSI83 device supports four DSI data lanes, and may be configured to support 1, 2, or 3 DSI data lanes per channel. Unused DSI input pins on the SN65DSI83 device must be left unconnected or driven to LP11 state. The bytes received from the data lanes are merged in HS mode to form packets that carry the video stream. DSI data lanes are bit and byte aligned.

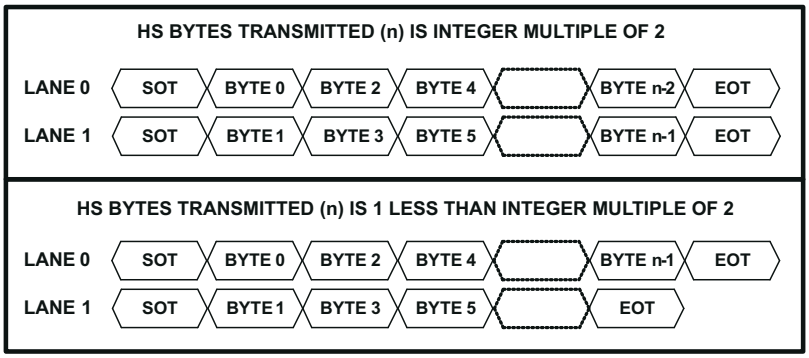
图 7-8 shows the lane merging function for each channel; 4-, 3-, and 2-lane modes.



4 DSI Data Lane Configuration (default)



3 DSI Data Lane Configuration



2 DSI Data Lane Configuration

图 7-8. SN65DSI83 DSI Lane Merging Illustration

7.4.5 DSI Pixel Stream Packets

The SN65DSI83 device processes 18 bpp (RGB666) and 24 bpp (RGB888) DSI packets on each channel, as shown in 图 7-9, 图 7-10, and 图 7-11.

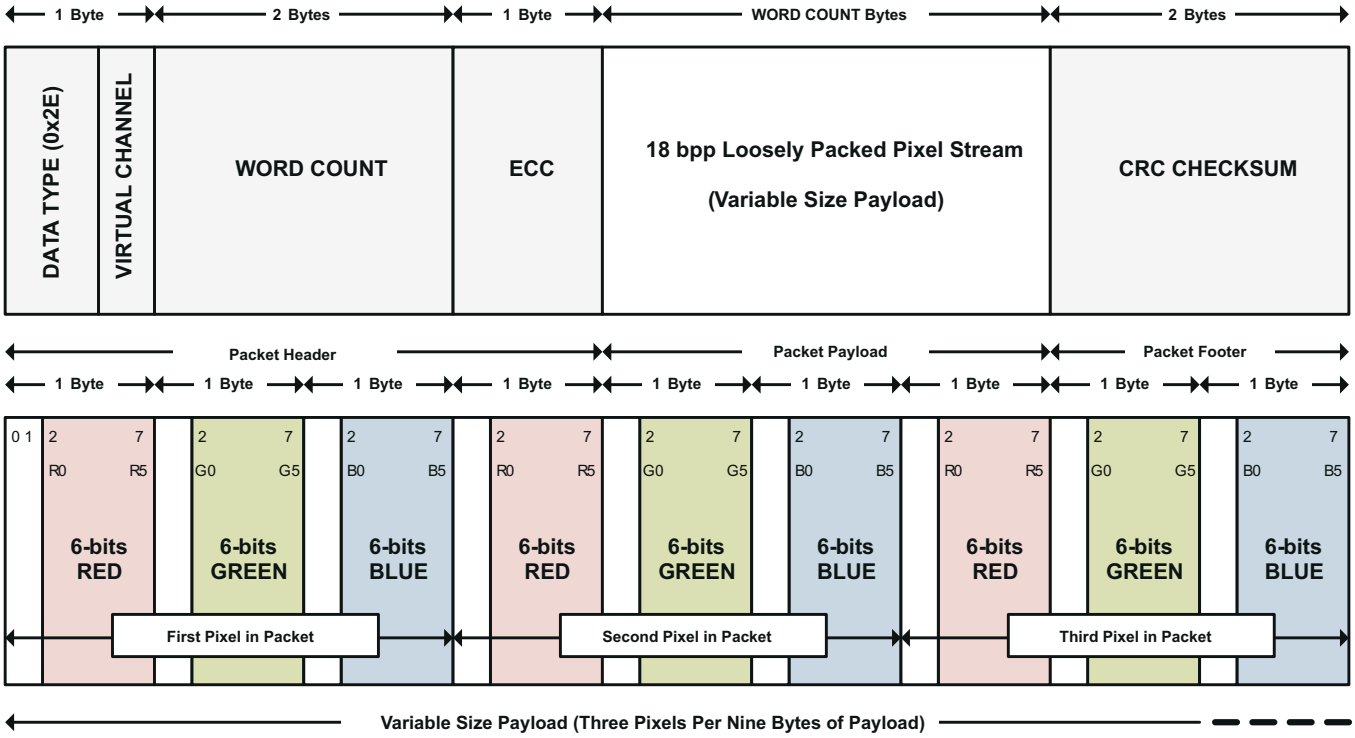


图 7-9. 18 bpp (Loosely Packed) DSI Packet Structure

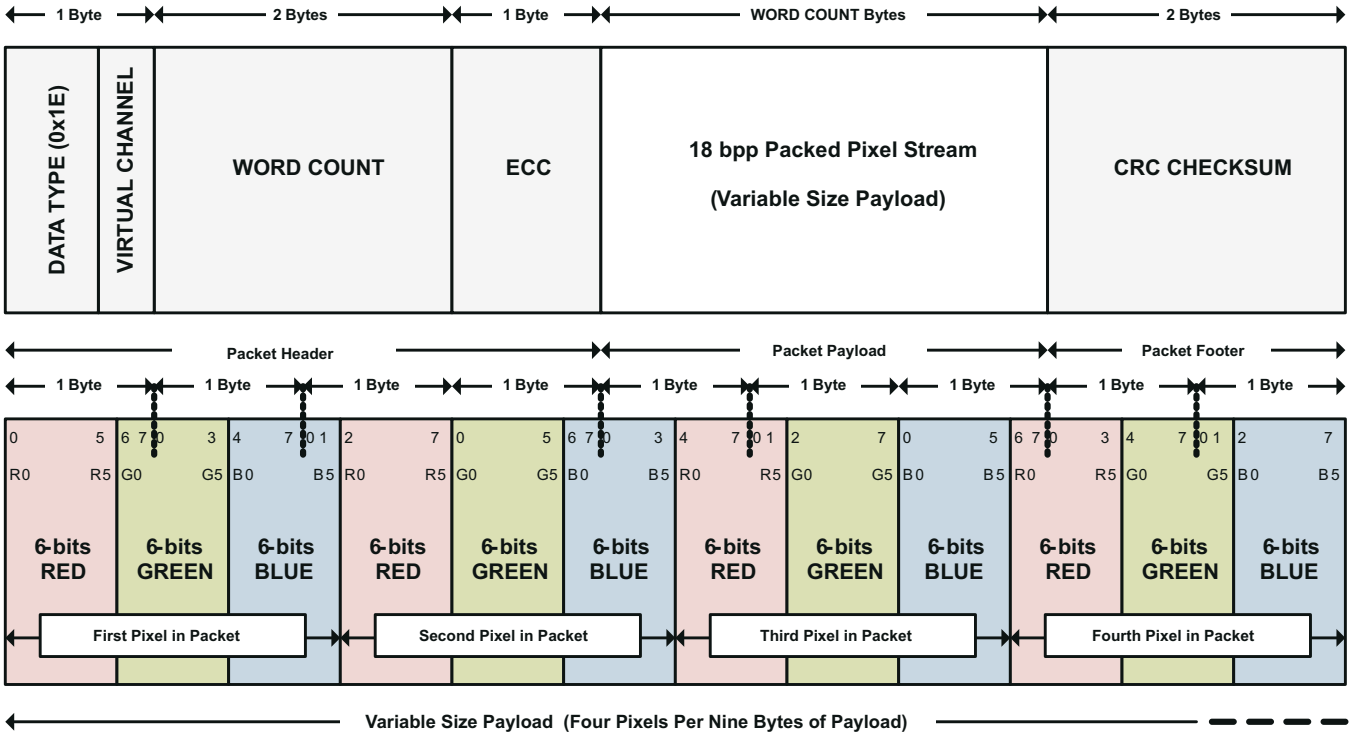


图 7-10. 18 bpp (Tightly Packed) DSI Packet Structure

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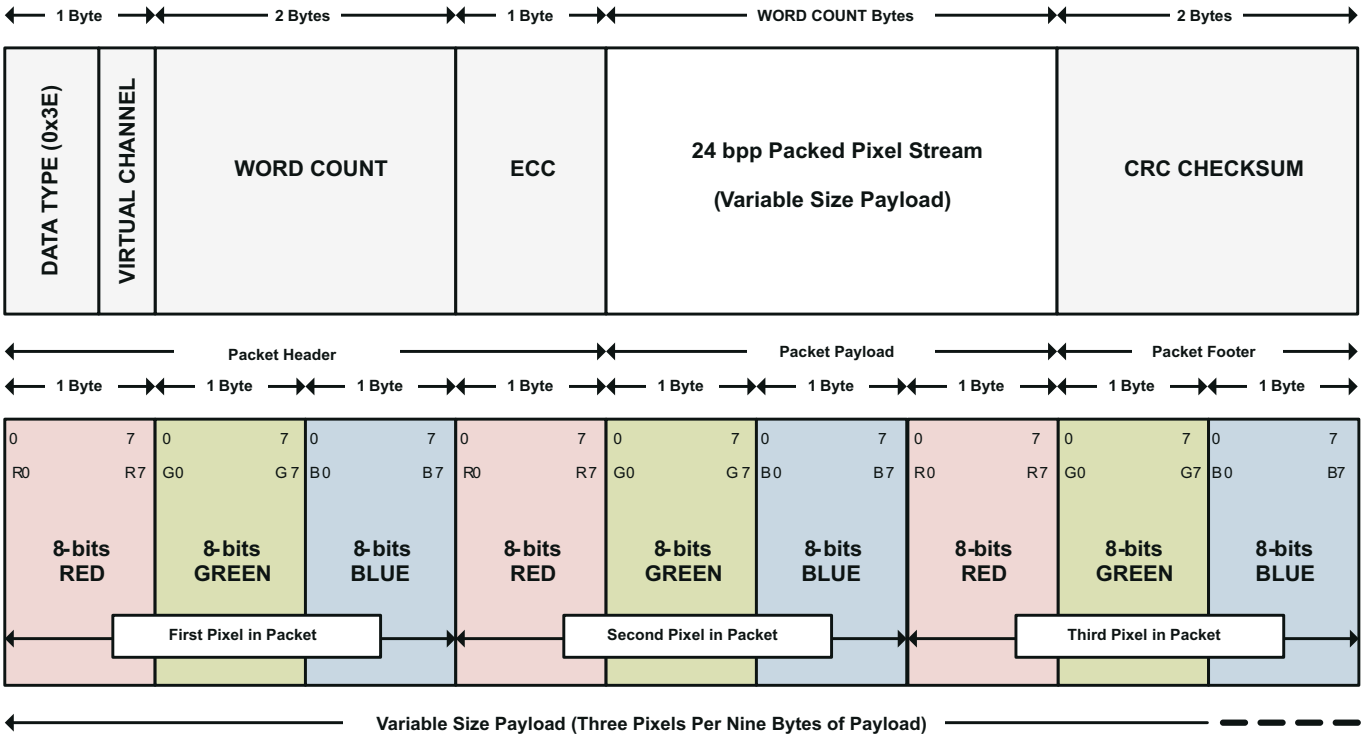


图 7-11. 24 bpp DSI Packet Structure

7.4.6 DSI Video Transmission Specifications

The SN65DSI83 device supports burst video mode and non-burst video mode with sync events or with sync pulses packet transmission as described in the DSI specification. The burst mode supports time-compressed pixel stream packets that leave added time per scan line for power savings LP mode. The SN65DSI83 device requires a transition to LP mode once per frame to enable PHY synchronization with the DSI host processor; however, for a robust and low-power implementation, the transition to LP mode is recommended on every video line.

图 7-12 shows the DSI video transmission applied to SN65DSI83 device applications. In all applications, the LVDS output rate must be less than or equal to the DSI input rate. The first line of a video frame shall start with a VSS packet, and all other lines start with VSE or HSS. The position of the synchronization packets in time is of utmost importance since this has a direct impact on the visual performance of the display panel; that is, these packets generate the HS and VS (horizontal and vertical sync) signals on the LVDS interface after the delay programmed into CHA_SYNC_DELAY_LOW/HIGH (CSR 0x28.7:0 and 0x29.3:0).

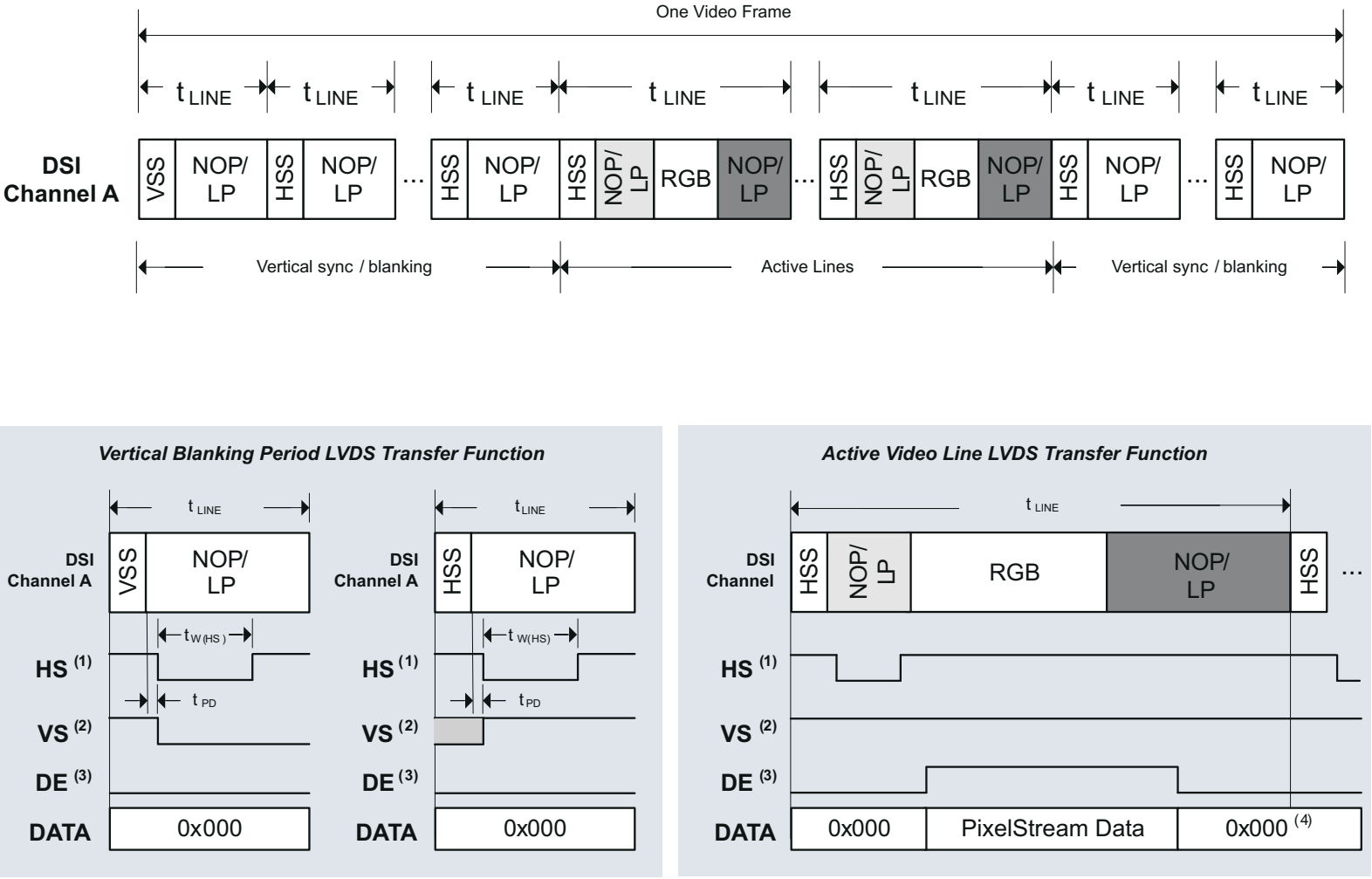
As required in the DSI specification, the SN65DSI83 device requires that pixel stream packets contain an integer number of pixels (that is, end on a pixel boundary); TI recommends to transmit an entire scan line on one pixel stream packet. When a scan line is broken in to multiple packets, inter-packet latency shall be considered such that the video pipeline (that is, pixel queue or partial line buffer) does not run empty (under-run); during scan line processing, if the pixel queue runs empty, the SN65DSI83 device transmits zero data (18’b0 or 24’b0) on the LVDS interface.

备注

When the HS clock is used as a source for the LVDS pixel clock, the LP mode transitions apply only to the data lanes, and the DSI clock lane remains in the HS mode during the entire video transmission.

备注

The SN65DSI83 device does not support the DSI virtual channel capability or reverse direction (peripheral to processor) transmissions.



(1) The assertion of HS is delayed (t_{PD}) by a programmable number of pixel clocks from the last bit of VSS/HSS packet received on DSI. The HS pulse width ($t_{W(HS)}$) is also programmable. The illustration shows HS active low.

(2) VS is signaled for a programmable number of lines (t_{LINE}) and is asserted when HS is asserted for the first line of the frame . VS is de -asserted when HS is asserted after the number of lines programmed has been reached. The illustration shows VS active low

(3) DE is asserted when active pixel data is transmitted on LVDS, and polarity is set independent to HS/VS. The illustration shows DE active high

(4) After the last pixel in an active line is output to LVDS, the LVDS data is output zero

LEGEND

VSS	**DSI Sync Event Packet: V Sync Start**
HSS	**DSI Sync Event Packet: H Sync Start**
RGB	**A sequence of DSI Pixel Stream Packets and Null Packets**
NOP/LP	**DSI Null Packet , Blanking Packet , or a transition to LP Mode**

图 7-12. DSI Channel Transmission and Transfer Function

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7.5 Programming

7.5.1 Local I²C Interface Overview

The SN65DSI83 device local I²C interface is enabled when EN is input high, access to the CSR registers is supported during ULPS. The SCL and SDA pins are used for I²C clock and I²C data respectively. The SN65DSI83 device I²C interface conforms to the 2-wire serial interface defined by the I²C Bus Specification, Version 2.1 (January 2000) and supports fast mode transfers up to 400 kbps.

The device address byte is the first byte received following the start condition from the master device. The 7-bit device address for SN65DSI83 device is factory preset to 010110X with the least significant bit being determined by the ADDR control input. 表 7-3 clarifies the SN65DSI83 device target address.

表 7-3. SN65DSI83 I²C Target Address Description (1) (2)

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (W/R)
0	1	0	1	1	0	ADDR	0/1

(1) When ADDR = 1, Address cycle is 0x5A (write) and 0x5B (read)
(2) When ADDR = 0, Address cycle is 0x58 (write) and 0x59 (read)

The following procedure is followed to write to the SN65DSI83 device I²C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSI83 device 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The SN65DSI83 device acknowledges the address cycle.
3. The master presents the subaddress (I²C register within SN65DSI83 device) to be written, consisting of one byte of data, MSB-first.
4. The SN65DSI83 device acknowledges the subaddress cycle.
5. The master presents the first byte of data to be written to the I²C register.
6. The SN65DSI83 device acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the SN65DSI83 device.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure is followed to read the SN65DSI83 I²C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the SN65DSI83 device 7-bit address and a one-value W/R bit to indicate a read cycle.
2. The SN65DSI83 device acknowledges the address cycle.
3. The SN65DSI83 device transmits the contents of the memory registers MSB-first starting at register 00h. If a write to the SN65DSI83 I²C register occurred prior to the read, then the SN65DSI83 device starts at the subaddress specified in the write.
4. The SN65DSI83 device waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I²C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the SN65DSI83 device transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure is followed for setting a starting subaddress for I²C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSI83 device 7-bit address and a zero-value W/R bit to indicate a write cycle
2. The SN65DSI83 device acknowledges the address cycle.
3. The master presents the subaddress (I²C register within the SN65DSI83 device) to be written, consisting of one byte of data, MSB first.
4. The SN65DSI83 device acknowledges the subaddress cycle.
5. The master terminates the write operation by generating a stop condition (P).

7.6 Register Maps

7.6.1 Control and Status Registers Overview

Many of the SN65DSI83 device functions are controlled by the control and status registers (CSR). All CSR registers are accessible through the local I^2C interface.

See 表 7-4 through 表 7-9 for the SN65DSI83 CSR descriptions. Reserved or undefined bit fields must not be modified. Otherwise, the device may operate incorrectly.

表 7-4. CSR Bit Field Definitions – ID Registers

ADDRESS	BIT	DESCRIPTION	DEFAULT	ACCESS(1)
0x00 – 0x08	7:0	Reserved Addresses 0x08 – 0x00 = {0x01, 0x20, 0x20, 0x20, 0x44, 0x53, 0x49, 0x38, 0x35}	Reserved	R/O

(1) R/O = Read only; R/W = Read/write; R/W1C = Read/write 1 to clear; W/O = Write only (reads return undetermined values)

表 7-5. CSR Bit Field Definitions – Reset and Clock Registers

ADDRESS	BIT	DESCRIPTION	DEFAULT	ACCESS (1)
0x09	0	SOFT_RESET This bit automatically clears when set to 1 and returns 0s when read. This bit must be set after the CSR’s are updated. This bit must also be set after making any changes to the DIS clock rate or after changing between DSI burst and nonburst modes. 0 – No action (default) 1 – Reset device to default condition excluding the CSR bits	0	W/O
0x0A	7	PLL_EN_STAT After PLL_EN_STAT = 1, wait at least 3 ms for PLL to lock 0 – PLL not enabled (default) 1 – PLL enabled	0	R/O
	3:1	LVDS_CLK_RANGE This field selects the frequency range of the LVDS output clock. 000 – 25 MHz ≤ LVDS_CLK < 37.5 MHz 001 – 37.5 MHz ≤ LVDS_CLK < 62.5 MHz 010 – 62.5 MHz ≤ LVDS_CLK < 87.5 MHz 011 – 87.5 MHz ≤ LVDS_CLK < 112.5 MHz 100 – 112.5 MHz ≤ LVDS_CLK < 137.5 MHz 101 – 137.5 MHz ≤ LVDS_CLK ≤ 154 MHz (default) 110 – Reserved 111 – Reserved	101	R/W
	0	HS_CLK_SRC 0 – LVDS pixel clock derived from input REFCLK (default) 1 – LVDS pixel clock derived from MIPI D-PHY channel A HS continuous clock	0	R/W

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表 7-5. CSR Bit Field Definitions – Reset and Clock Registers (continued)

ADDRESS	BIT	DESCRIPTION	DEFAULT	ACCESS (1)
0x0B	7:3	DSI_CLK_DIVIDER When CSR 0x0A.0 = 1, this field controls the divider used to generate the LVDS output clock from the MIPI D-PHY Channel A HS continuous clock. When CSR 0x0A.0 = 0, this field must be programmed to 00000. 00000 – LVDS clock = source clock (default) 00001 – Divide by 2 00010 – Divide by 3 00011 – Divide by 4 … 10111 – Divide by 24 11000 – Divide by 25 11001 through 11111 – Reserved	00000	R/W
	1:0	REFCLK_MULTIPLIER When CSR 0x0A.0 = 0, this field controls the multiplier used to generate the LVDS output clock from the input REFCLK. When CSR 0x0A.0 = 1, this field must be programmed to 00. 00 – LVDS clock = source clock (default) 01 – Multiply by 2 10 – Multiply by 3 11 – Multiply by 4	00	R/W
0x0D	0	PLL_EN When this bit is set, the PLL is enabled with the settings programmed into CSR 0x0A and CSR 0x0B. The PLL must be disabled before changing any of the settings in CSR 0x0A and CSR 0x0B. The input clock source must be active and stable before the PLL is enabled. 0 – PLL disabled (default) 1 – PLL enabled	0	R/W

(1) R/O = Read Only; R/W = Read/write; R/W1C = Read/write 1 to Clear; W/O = Write only (reads return undetermined values)

表 7-6. CSR Bit Field Definitions – DSI Registers

ADDRESS	BIT	DESCRIPTION	DEFAULT	ACCESS (1)
0x10	7	Reserved. Do not write to this field. Must remain at default.	0	R/W
	6:5	Reserved. Do not write to this field. Must remain at default.	01	R/W
	4:3	CHA_DSI_LANES This field controls the number of lanes that are enabled for DSI channel A. 00 – Four lanes are enabled 01 – Three lanes are enabled 10 – Two lanes are enabled 11 – One lane is enabled (default) Note: Unused DSI input pins on the SN65DSI83 must be left unconnected.	11	R/W
	0	SOT_ERR_TOL_DIS 0 – Single bit errors are tolerated for the start of transaction SoT leader sequence (default) 1 – No SoT bit errors are tolerated	0	R/W
0x11	7:6	CHA_DSI_DATA_EQ This field controls the equalization for the DSI channel A data lanes 00 – No equalization (default) 01 – 1 dB equalization 10 – Reserved 11 – 2 dB equalization	00	R/W
	3:2	CHA_DSI_CLK_EQ This field controls the equalization for the DSI channel A clock 00 – No equalization (default) 01 – 1-dB equalization 10 – Reserved 11 – 2-dB equalization	00	R/W

表 7-6. CSR Bit Field Definitions – DSI Registers (continued)

ADDRESS	BIT	DESCRIPTION	DEFAULT	ACCESS (1)
0x12	7:0	CHA_DSI_CLK_RANGE This field specifies the DSI clock frequency range in 5-MHz increments for the DSI channel A clock 0x00 through 0x07 – Reserved 0x08 – 40 ≤ frequency < 45 MHz 0x09 – 45 ≤ frequency < 50 MHz … 0x63 – 495 ≤ frequency < 500 MHz 0x64 – 500 MHz 0x65 through 0xFF – Reserved	0	R/W

(1) R/O = Read only; R/W = Read/write; R/W1C = Read/write 1 to clear; W/O = Write only (reads return undetermined values)

表 7-7. CSR Bit Field Definitions – LVDS Registers

ADDRESS	BIT	DESCRIPTION	DEFAULT	ACCESS (1)
0x18	7	DE_NEG_POLARITY 0 – DE is positive polarity driven 1 during active pixel transmission on LVDS (default) 1 – DE is negative polarity driven 0 during active pixel transmission on LVDS	0	R/W
	6	HS_NEG_POLARITY 0 – HS is positive polarity driven 1 during corresponding sync conditions 1 – HS is negative polarity driven 0 during corresponding sync (default)	1	R/W
	5	VS_NEG_POLARITY 0 – VS is positive polarity driven 1 during corresponding sync conditions 1 – VS is negative polarity driven 0 during corresponding sync (default)	1	R/W
	4	Reserved. Do not write to this field. Must remain at default.	1	R/W
	3	CHA_24BPP_MODE 0 – Force 18 bpp; LVDS channel A lane 4 (A_Y3P or A_Y3N) is disabled (default) 1 – Force 24 bpp; LVDS channel A lane 4 (A_Y3P or A_Y3N) is enabled	0	R/W
	1	CHA_24BPP_FORMAT1 This field selects the 24 bpp data format 0 – LVDS channel A lane A_Y3P or A_Y3N transmits the 2 MSB per color; format 2 (default) 1 – LVDS channel A lane A_Y3P or A_Y3N transmits the 2 LSB per color; format 1 Note1: This field must be 0 when 18bpp data is received from DSI. Note2: If this field is set to 1 and CHA_24BPP_MODE is 0, the SN65DSI83 device will convert 24-bpp data to 18-bpp data for transmission to an 18-bpp panel. In this configuration, the SN65DSI83 device will not transmit the 2 LSB per color on LVDS channel A, since LVDS channel A lane 4 is disabled.	0	R/W
0x19	6	CHA_LVDS_VOCM This field controls the common mode output voltage for LVDS channel A 0 – 1.2 V (default) 1 – 0.9 V (CSR 0x1B.5:4 CHA_LVDS_CM_ADJUST must be set to 01b)	0	R/W
	3:2	CHA_LVDS_VOD_SWING This field controls the differential output voltage for LVDS channel A. See the Electrical Characteristics table for $\lvert V_{OD} \rvert$ for each setting: 00, 01 (default), 10, 11	01	R/W

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表 7-7. CSR Bit Field Definitions – LVDS Registers (continued)

ADDRESS	BIT	DESCRIPTION	DEFAULT	ACCESS (1)
0x1A	5	CHA_REVERSE_LVDS This bit controls the order of the LVDS pins for channel A. 0 – Normal LVDS channel A pin order. LVDS channel A pin order is the same as listed in the Pin Assignments Section. (default) 1 – Reversed LVDS channel A pin order. LVDS channel A pin order is remapped as follows: • A_Y0P → A_Y3P • A_Y0N → A_Y3N • A_Y1P → A_CLKP • A_Y1N → A_CLKN • A_Y2P → A_Y2P • A_Y2N → A_Y2N • A_CLKP → A_Y1P • A_CLKN → A_Y1N • A_Y3P → A_Y0P • A_Y3N → A_Y0N	0	R/W
	1	CHA_LVDS_TERM This bit controls the near end differential termination for LVDS channel A. This bit also affects the output voltage for LVDS Channel A. 0 – 100-Ω differential termination 1 – 200-Ω differential termination (default)	1	R/W
0x1B	5:4	CHA_LVDS_CM_ADJUST This field can be used to adjust the common mode output voltage for LVDS channel A. 00 – No change to common mode voltage (default) 01 – Adjust common mode voltage down 3% 10 – Adjust common mode voltage up 3% 11 – Adjust common mode voltage up 6%	00	R/W

(1) R/O = Read only; R/W = Read/write; R/W1C = Read/write 1 to clear; W/O = Write only (reads return undetermined values)

备注

For all video registers:

TEST PATTERN GENERATION PURPOSE ONLY registers are for test pattern generation use only. Others are for normal operation unless the test pattern generation feature is enabled.

表 7-8. CSR Bit Field Definitions – Video Registers

ADDRESS	BIT	DESCRIPTION	DEFAULT	ACCESS (1)
0x20	7:0	CHA_ACTIVE_LINE_LENGTH_LOW This field controls the length in pixels of the active horizontal line that are received on DSI channel A and output to LVDS channel A.. The value in this field is the lower 8 bits of the 12-bit value for the horizontal line length.	0	R/W
0x21	3:0	CHA_ACTIVE_LINE_LENGTH_HIGH This field controls the length in pixels of the active horizontal line that are received on DSI channel A and output to LVDS channel A.. The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length.	0	R/W
0x24	7:0	CHA_VERTICAL_DISPLAY_SIZE_LOW TEST PATTERN GENERATION PURPOSE ONLY. This field controls the vertical display size in lines for LVDS channel A. The value in this field is the lower 8 bits of the 12-bit value for the vertical display size. The value in this field is only used for channel A test pattern generation.	0	R/W

表 7-8. CSR Bit Field Definitions – Video Registers (continued)

ADDRESS	BIT	DESCRIPTION	DEFAULT	ACCESS [1]
0x25	3:0	CHA_VERTICAL_DISPLAY_SIZE_HIGH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the vertical display size in lines for LVDS channel A. The value in this field is the upper 4 bits of the 12-bit value for the vertical display size. The value in this field is only used for channel A test pattern generation.	0	R/W
0x28	7:0	CHA_SYNC_DELAY_LOW This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for channel A. The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI83 device. The additional delay is approximately 10 pixel clocks. The sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the lower 8 bits of the 12-bit value for the sync delay.	0	R/W
0x29	3:0	CHA_SYNC_DELAY_HIGH This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for channel A. The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI83 device. The additional delay is approximately 10 pixel clocks. The sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the lower 4 bits of the 12-bit value for the sync delay.	0	R/W
0x2C	7:0	CHA_HSYNC_PULSE_WIDTH_LOW This field controls the width in pixel clocks of the HSync pulse duration for LVDS channel A. The value in this field is the lower 8 bits of the 10-bit value for the HSync pulse duration. The value in this field is used for channel A test pattern generation when test pattern generation feature is enabled by programming bit 4 at 0x3C.	0	R/W
0x2D	1:0	CHA_HSYNC_PULSE_WIDTH_HIGH This field controls the width in pixel clocks of the HSync pulse duration for LVDS channel A. The value in this field is the upper 2 bits of the 10-bit value for the HSync pulse duration. The value in this field is used for channel A test pattern generation when test pattern generation feature is enabled by programming bit 4 at 0x3C.	0	R/W
0x30	7:0	CHA_VSYNC_PULSE_WIDTH_LOW This field controls the length in lines of the VSync pulse duration for LVDS channel A. The value in this field is the lower 8 bits of the 10-bit value for the VSync pulse duration. The value in this field is used for channel A test pattern generation when test pattern generation feature is enabled by programming bit 4 at 0x3C.	0	R/W
0x31	1:0	CHA_VSYNC_PULSE_WIDTH_HIGH This field controls the length in lines of the VSync pulse duration for LVDS channel A. The value in this field is the upper 2 bits of the 10-bit value for the VSync pulse duration. The value in this field is used for channel A test pattern generation when test pattern generation feature is enabled by programming bit 4 at 0x3C.	0	R/W
0x34	7:0	CHA_HORIZONTAL_BACK_PORCH This field controls the time in pixel clocks between the end of the HSync pulse and the start of the active video data for LVDS channel A. The value in this field is used for channel A test pattern generation when test pattern generation feature is enabled by programming bit 4 at 0x3C.	0	R/W
0x36	7:0	CHA_VERTICAL_BACK_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the number of lines between the end of the VSync pulse and the start of the active video data for LVDS channel A. The value in this field is only used for channel A test pattern generation.	0	R/W
0x38	7:0	CHA_HORIZONTAL_FRONT_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the time in pixel clocks between the end of the active video data and the start of the HSync pulse for LVDS channel A. The value in this field is only used for channel A test pattern generation.	0	R/W

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表 7-8. CSR Bit Field Definitions – Video Registers (continued)

ADDRESS	BIT	DESCRIPTION	DEFAULT	ACCESS (1)
0x3A	7:0	CHA_VERTICAL_FRONT_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the number of lines between the end of the active video data and the start of the VSync pulse for LVDS channel A. The value in this field is only used for channel A test pattern generation.	0	R/W
0x3C	4	CHA_TEST_PATTERN TEST PATTERN GENERATION PURPOSE ONLY. When this bit is set, the SN65DSI83 device will generate a video test pattern for LVDS channel A based on the values programmed into the video registers for channel A.	0	R/W

(1) R/O = Read only; R/W = Read/write; R/W1C = Read/write 1 to clear; W/O = Write only (reads return undetermined values)

表 7-9. CSR Bit Field Definitions – IRQ Registers

ADDRESS	BIT	DESCRIPTION	DEFAULT	ACCESS (1)
0xE0	0	IRQ_EN When enabled by this field, the IRQ output is driven high to communicate IRQ events. 0 – IRQ output is high-impedance (default) 1 – IRQ output is driven high when a bit is set in registers 0xE5 that also has the corresponding IRQ_EN bit set to enable the interrupt condition	0	R/W
0xE1	7	CHA_SYNCH_ERR_EN 0 – CHA_SYNCH_ERR is masked 1 – CHA_SYNCH_ERR is enabled to generate IRQ events	0	R/W
	6	CHA_CRC_ERR_EN 0 – CHA_CRC_ERR is masked 1 – CHA_CRC_ERR is enabled to generate IRQ events	0	R/W
	5	CHA_UNC_ECC_ERR_EN 0 – CHA_UNC_ECC_ERR is masked 1 – CHA_UNC_ECC_ERR is enabled to generate IRQ events	0	R/W
	4	CHA_COR_ECC_ERR_EN 0 – CHA_COR_ECC_ERR is masked 1 – CHA_COR_ECC_ERR is enabled to generate IRQ events	0	R/W
	3	CHA_LLP_ERR_EN 0 – CHA_LLP_ERR is masked 1 – CHA_ LLP_ERR is enabled to generate IRQ events	0	R/W
	2	CHA_SOT_BIT_ERR_EN 0 – CHA_SOT_BIT_ERR is masked 1 – CHA_SOT_BIT_ERR is enabled to generate IRQ events	0	R/W
	0	PLL_UNLOCK_EN 0 – PLL_UNLOCK is masked 1 – PLL_UNLOCK is enabled to generate IRQ events	0	R/W
0xE5	7	CHA_SYNCH_ERR When the DSI channel A packet processor detects an HS or VS synchronization error, that is, an unexpected sync packet; this bit is set; this bit is cleared by writing a 1 value.	0	R/W1C
	6	CHA_CRC_ERR When the DSI channel A packet processor detects a data stream CRC error, this bit is set; this bit is cleared by writing a 1 value.	0	R/W1C
	5	CHA_UNC_ECC_ERR When the DSI channel A packet processor detects an uncorrectable ECC error, this bit is set; this bit is cleared by writing a 1 value.	0	R/W1C
	4	CHA_COR_ECC_ERR When the DSI channel A packet processor detects a correctable ECC error, this bit is set; this bit is cleared by writing a 1 value.	0	R/W1C
	3	CHA_LLP_ERR When the DSI channel A packet processor detects a low level protocol error, this bit is set; this bit is cleared by writing a 1 value. Low-level protocol errors include SoT and EoT sync errors, Escape Mode entry command errors, LP transmission sync errors, and false control errors. Lane merge errors are reported by this status condition.	0	R/W1C
	2	CHA_SOT_BIT_ERR When the DSI channel A packet processor detects an SoT leader sequence bit error, this bit is set; this bit is cleared by writing a 1 value.	0	R/W1C
	0	PLL_UNLOCK This bit is set whenever the PLL Lock status transitions from LOCK to UNLOCK.	1	R/W1C

(1) R/O = Read only; R/W = Read/write; R/W1C = Read/write 1 to clear; W/O = Write only (reads return undetermined values)

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8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN65DSI83 device is primarily targeted for portable applications such as tablets and smart phones that utilize the MIPI DSI video format. The SN65DSI83 device can be used between a GPU with DSI output and a video panel with LVDS inputs.

8.1.1 Video STOP and Restart Sequence

When the system requires to stop outputting video to the display, TI recommends to use the following sequence for the SN65DSI83 device:

1. Clear the PLL_EN bit to 0 (CSR 0x0D.0).
2. Stop video streaming on DSI inputs.
3. Drive all DSI data lanes to LP11, but keep the DSI CLK lanes in HS.

When the system is ready to restart the video streaming.

1. Start video streaming on DSI inputs.
2. Set the PLL_EN bit to 1 (CSR 0x0D.0).
3. Wait for minimum of 3 ms.
4. Set the SOFT_RESET bit (0x09.0).

8.1.2 Reverse LVDS Pin Order Option

For ease of PCB routing, the SN65DSI83 device supports reversing the pin order via configuration register programming. The order of the LVDS pin for LVDS channel A can be reversed by setting the address 0x1A bit 5 CHA_REVERSE_LVDS. See the corresponding register bit definition for details.

8.1.3 IRQ Usage

The SN65DSI83 device provides an IRQ pin that can be used to indicate when certain errors occur on DSI. The IRQ output is enabled through the IRQ_EN bit (CSR 0xE0.0). The IRQ pin will be asserted when an error occurs on DSI, the corresponding error enable bit is set, and the IRQ_EN bit is set. An error is cleared by writing a 1 to the corresponding error status bit.

备注

If the SOFT_RESET bit is set while the DSI video stream is active, some of the error status bits may be set.

备注

If the DSI video stream is stopped, some of the error status bits may be set. These error status bits must be cleared before restarting the video stream.

备注

If the DSI video stream starts before the device is configured, some of the error status bits may be set. TI recommends to start streaming after the device is correctly configured as recommended in the initialization sequence in 节 7.4.2.

8.2 Typical Application

图 8-1 shows a typical application using the SN65DSI83 device for a single channel DSI receiver to interface a single-channel DSI application processor to an LVDS single-link 18 bit-per-pixel panel supporting 1280 × 800 WXGA resolutions at 60 frames per second.

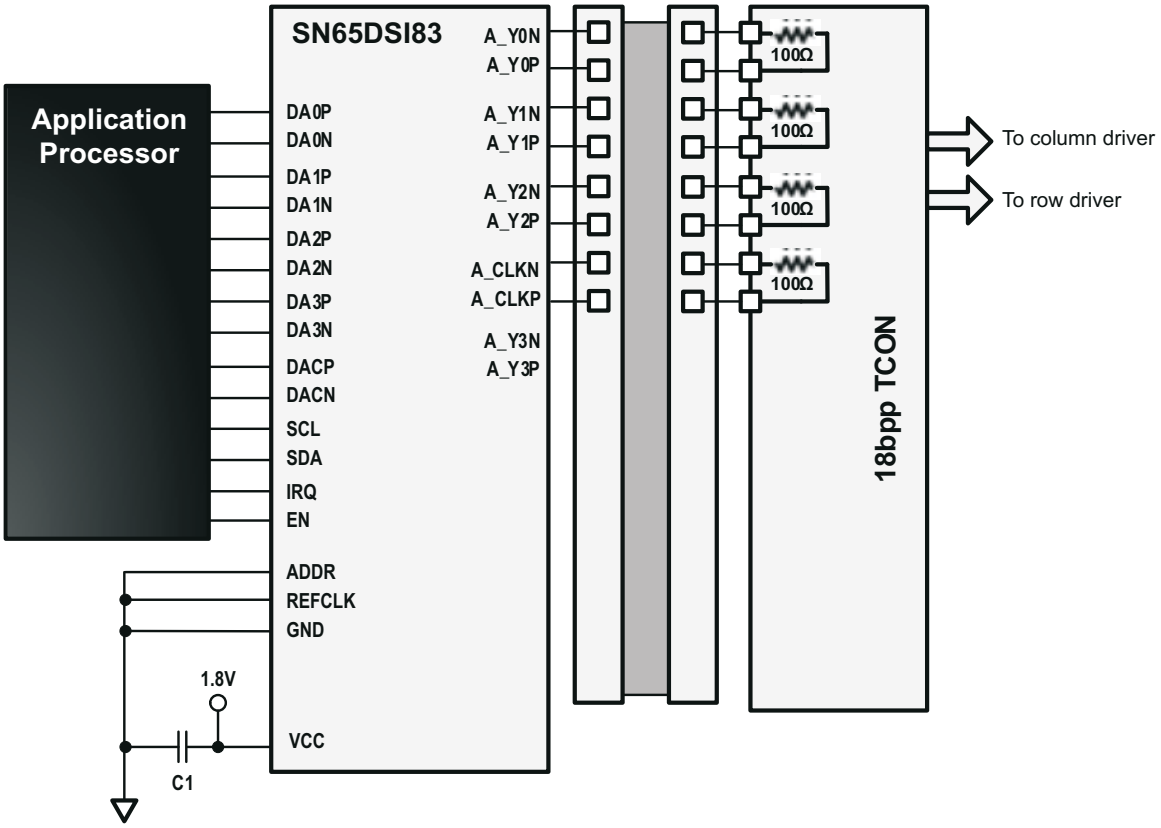

图 8-1. Typical WXGA 18-bpp Panel Application

8.2.1 Design Requirements

表 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
VCC	1.8 V (±5%)
Clock Source (REFCLK or DSIA_CLK)	DSIA_CLK
REFCKL Frequency	N/A
DSIA Clock Frequency	500 MHz
PANEL INFORMATION	
Pixel Clock (MHz)	83 MHz
Horizontal Active (pixels)	1280
Horizontal Blanking (pixels)	384
Vertical Active (lines)	800
Vertical Blanking (lines)	30
Horizontal Sync Offset (pixels)	64
Horizontal Sync Pulse Width (pixels)	128
Vertical Sync Offset (lines)	3
Vertical Sync Pulse Width (lines)	7

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表 8-1. Design Parameters (continued)

DESIGN PARAMETERS	EXAMPLE VALUE
PANEL INFORMATION (continued)	
Horizontal Sync Pulse Polarity	Negative
Vertical Sync Pulse Polarity	Negative
Color Bit Depth (6 bpc or 8 bpc)	6-bit
Number of LVDS Lanes	1 × [3 Data Lanes + 1 Clock Lane]
DSI INFORMATION	
Number of DSI Lanes	1 × [4 Data Lanes + 1 Clock Lane]
DSI Clock Frequency(MHz)	500 MHz
Dual DSI Configuration(Odd/Even or Left/Right)	N/A

8.2.2 Detailed Design Procedure

The video resolution parameters required by the panel need to be programmed into the SN65DSI83 device. For this example, the parameters programmed would be the following:

Horizontal Active = 1280 or 0x500

CHA_ACTIVE_LINE_LENGTH_LOW = 0x00

CHA_ACTIVE_LINE_LENGTH_HIGH = 0x05

Vertical Active = 800 or 0x320

CHA_VERTICAL_DISPLAY_SIZE_LOW = 0x20

CHA_VERTICAL_DISPLAY_SIZE_HIGH = 0x03

Horizontal Pulse Width = 128 or 0x80

CHA_HSYNC_PULSE_WIDTH_LOW = 0x80

CHA_HSYNC_PULSE_WIDTH_HIGH = 0x00

Vertical Pulse Width = 7

CHA_VSYNC_PULSE_WIDTH_LOW = 0x07

CHA_VSYNC_PULSE_WIDTH_HIGH = 0x00

Horizontal Backporch = HorizontalBlanking – (HorizontalSyncOffset + HorizontalSyncPulseWidth)

Horizontal Backporch = 384 – (64 + 128)

Horizontal Backporch = 192 or 0xC0

CHA_HORIZONTAL_BACK_PORCH = 0xC0

Vertical Backporch = VerticalBlanking – (VerticalSyncOffset +VerticalSyncPulseWidth)

Vertical Backporch = 30 – (3 + 7)

Vertical Backporch = 20 or 0x14

CHA_VERTICAL_BACK_PORCH = 0x14

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Horizontal Frontporch = HorizontalSyncOffset

Horizontal Frontporch = 64 or 0x40

CHA_HORIZONTAL_FRONT_PORCH = 0x40

Vertical Frontporch = VerticalSyncOffset

Vertical Frontporch = 3

CHA_VERTICAL_FRONT_PORCH = 0x03

The pattern generation feature can be enabled by setting the CHA_TEST_PATTERN bit at address 0x3C and configuring the TEST PATTERN GENERATION PURPOSE ONLY register as shown in 表 7-8.

LVDS clock is derived from the DSI channel A clock. When the MIPI D-PHY channel A HS clock is used as the LVDS clock source, it is divided by the factor in DSI_CLK_DIVIDER (CSR 0x0B.7:3) to generate the FlatLink LVDS output clock. Additionally, LVDS_CLK_RANGE (CSR 0x0A.3:1) and CH_DSI_CLK_RANGE(CSR 0x12) must be set to the frequency range of the FlatLink LVDS output clock and DSI Channel A input clock respectively for the internal PLL to operate correctly. After these settings are programmed, PLL_EN (CSR 0x0D.0) must be set to enable the internal PLL.

LVDS_CLK_RANGE = 2 – 62.5 MHz ≤ LVDS_CLK < 87.5 MHz

HS_CLK_SRC = 1 – LVDS pixel clock derived from MIPI D-PHY channel A

DSI_CLK_DIVIDER = 00101 – Divide by 6

CHA_DSI_LANES = 00 – Four lanes are enabled

CHA_DSI_CLK_RANGE = 0x64 – 500 MHz

8.2.2.1 Example Script

This example configures the SN65DSI83 device for the following configuration:

```
<aardvark>
<configure i2c="1" spi="1" gpio="0" tpower="1" pullups="1"/>
<i2c_bitrate khz="100"/>
=====SOFTRESET=======
<i2c_write addr="0x2D" count="1" radix="16">09 01</i2c_write> <sleep ms="10"/>
======PLL_EN(bit 0) - Enable LAST after addr 0A and 0B configured======
<i2c_write addr="0x2D" count="1" radix="16">0D 00</i2c_write> <sleep ms="10"/>
======HS_CLK_SRC bit0===
======LVDS_CLK_Range bit 3:1======
<i2c_write addr="0x2D" count="1" radix="16"> 0A 05</i2c_write> <sleep ms="10"/>
======DSI_CLK_DIVIDER bit7:3=====
======RefCLK multiplier(bit1:0)======
======00 - LVDSclk=source clk, 01 - x2, 10 -x3, 11 - x4======
<i2c_write addr="0x2D" count="1" radix="16">0B 28</i2c_write> <sleep ms="10"/>
======DSI Ch Confg Left_Right Pixels(bit7 - 0 for A ODD, B EVEN, 1 for the other config)======
======DSI Ch Mode(bit6:5) 00 - Dual, 01 - single, 10 - two single =======
======SOT_ERR_TOL_DIS(bit0)=======
<i2c_write addr="0x2D" count="1" radix="16">10 26</i2c_write> <sleep ms="10"/>
====500M====
<i2c_write addr="0x2D" count="1" radix="16">12 64</i2c_write> <sleep ms="10"/>
======bit7: DE_Pol, bit6:HS_Pol, bit5:VS_Pol, bit4: LVDS Link Cfg, bit3:CHA 24bpp, bit2: CHB 24bpp,
bit1: CHA 24bpp fmt1, bit0: CHB 24bpp fmt1======
<i2c_write addr="0x2D" count="1" radix="16">18 72</i2c_write> <sleep ms="10"/>
<i2c_write addr="0x2D" count="1" radix="16">19 00</i2c_write> <sleep ms="10"/>
======CHA_LINE_LENGTH_LOW========
<i2c_write addr="0x2D" count="1" radix="16">20 00</i2c_write> <sleep ms="10"/>
======CHA_LINE_LENGTH_HIGH========
<i2c_write addr="0x2D" count="1" radix="16">21 05</i2c_write> <sleep ms="10"/>
======CHA_VERTICAL_DISPLAY_SIZE_LOW========
<i2c_write addr="0x2D" count="1" radix="16">24 00</i2c_write> <sleep ms="10"/>
======CHA_VERTICAL_DISPLAY_SIZE_HIGH========
<i2c_write addr="0x2D" count="1" radix="16">25 04</i2c_write> <sleep ms="10"/>
======CHA_SYNC_DELAY_LOW========
<i2c_write addr="0x2D" count="1" radix="16">28 20</i2c_write> <sleep ms="10"/>
======CHA_SYNC_DELAY_HIGH========
<i2c_write addr="0x2D" count="1" radix="16">29 01</i2c_write> <sleep ms="10"/>
======CHA_HSYNC_PULSE_WIDTH_LOW========
<i2c_write addr="0x2D" count="1" radix="16">2C 80</i2c_write> <sleep ms="10"/>
======CHA_HSYNC_PULSE_WIDTH_HIGH========
<i2c_write addr="0x2D" count="1" radix="16">2D 00</i2c_write> <sleep ms="10"/>
======CHA_VSYNC_PULSE_WIDTH_LOW========
<i2c_write addr="0x2D" count="1" radix="16">30 07</i2c_write> <sleep ms="10"/>
======CHA_VSYNC_PULSE_WIDTH_HIGH========
<i2c_write addr="0x2D" count="1" radix="16">31 00</i2c_write> <sleep ms="10"/>
======CHA_HOR_BACK_PORCH========
<i2c_write addr="0x2D" count="1" radix="16">34 C0</i2c_write> <sleep ms="10"/>
======CHA_VER_BACK_PORCH========
<i2c_write addr="0x2D" count="1" radix="16">36 00</i2c_write> <sleep ms="10"/>
======CHA_HOR_FRONT_PORCH========
<i2c_write addr="0x2D" count="1" radix="16">38 00</i2c_write> <sleep ms="10"/>
======CHA_VER_FRONT_PORCH========
<i2c_write addr="0x2D" count="1" radix="16">3A 00</i2c_write> <sleep ms="10"/>
======CHA/CHB TEST PATTERN(bit4 CHA, bit0 CHB)========
<i2c_write addr="0x2D" count="1" radix="16">3C 00</i2c_write> <sleep ms="10"/>
======PLL_EN(bit 0) - Enable LAST after addr 0A and 0B configured======
<i2c_write addr="0x2D" count="1" radix="16">0D 01</i2c_write> <sleep ms="10"/>
======Read======
<i2c_write addr="0x2D" count="1" radix="16">00</i2c_write> <sleep ms="10"/>
======Read======
<i2c_write addr="0x2D" count="256" radix="16">00</i2c_write> <sleep ms="10"/>
</aardvark>
```


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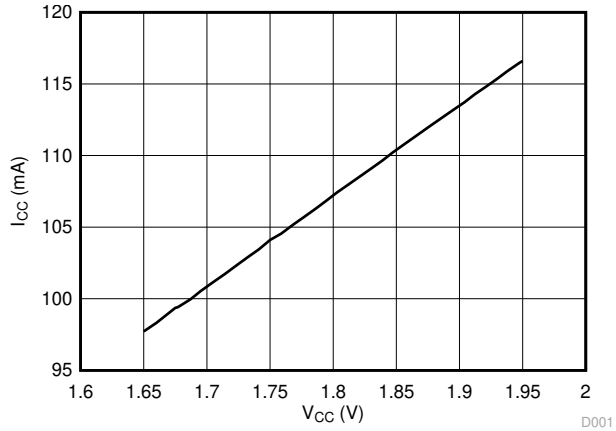
8.2.3 Application Curve



A. All typical values are at T_A = 25°C.
B. SN65DSI83: SINGLE Channel DSI to SINGLE Channel DSI, 1280 × 800
   1. number of LVDS lanes = 3 data lanes + 1 CLK lane
   2. number of DSI lanes = 4 data lanes + 1 CLK lane
   3. LVDS CLK OUT = 83 M
   4. DSI CLK = 500 M
   5. RGB666, LVDS 18 bpp

图 8-2. Power Consumption

9 Power Supply Recommendations

9.1 V_{CC} Power Supply

Each VCC power supply pin must have a 100-nF capacitor to ground connected as close as possible to the SN65DSI83 device. It is recommended to have one bulk capacitor (1 µF to 10 µF) on it. It is also recommended to have the pins connected to a solid power plane.

9.2 VCORE Power Supply

This pin must have a 100-nF capacitor to ground connected as close as possible to the SN65DSI83 device. It is recommended to have one bulk capacitor (1 µF to 10 µF) on it. It is also recommended to have the pins connected to a solid power plane.

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10 Layout

10.1 Layout Guidelines

10.1.1 Package Specific

For the ZXH package, to minimize the power supply noise floor, provide good decoupling near the SN65DSI83 device power pins. The use of four ceramic capacitors (2 × 0.1 μF and 2 × 0.01 μF) provides good performance. At the least, TI recommends to install one 0.1-μF and one 0.01-μF capacitor near the SN65DSI83 device. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized. Placing the capacitor underneath the SN65DSI83 device on the bottom of the PCB is often a good choice.

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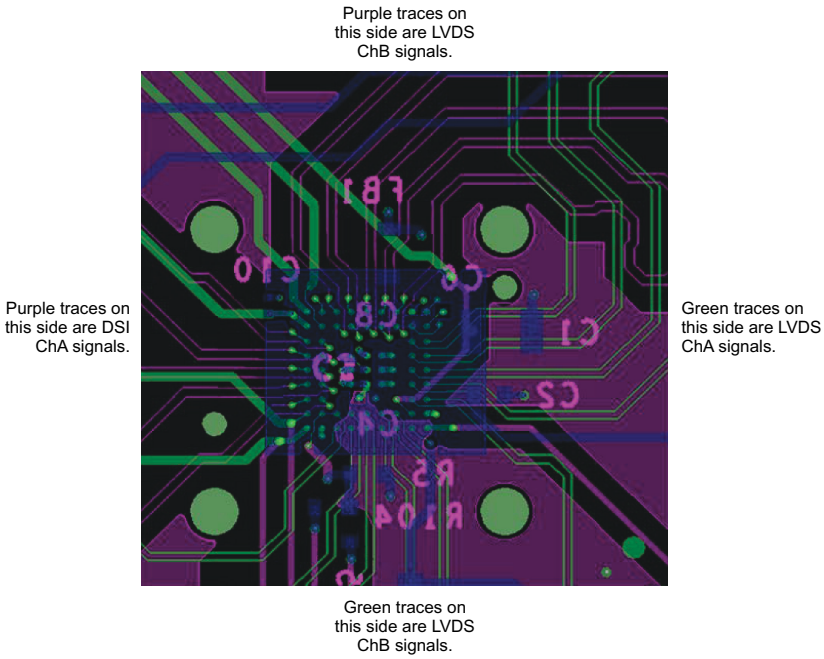
10.1.2 Differential Pairs

- Differential pairs must be routed with controlled 100-Ω differential impedance (± 20%) or 50-Ω single-ended impedance (±15%).
- Keep away from other high speed signals
- Keep lengths to within 5 mils of each other.
- Length matching must be near the location of mismatch.
- Each pair must be separated at least by 3 times the signal trace width.
- The use of bends in differential traces must be kept to a minimum. When bends are used, the number of left and right bends must be as equal as possible and the angle of the bend must be ⩾ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
- Route all differential pairs on the same of layer.
- The number of vias must be kept to a minimum. It is recommended to keep the via count to 2 or less.
- Keep traces on layers adjacent to ground plane.
- Do NOT route differential pairs over any plane split.
- Adding Test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test points are used, they must be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

10.1.3 Ground

TI recommends that only one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the SN65DSI83 must be connected to this plane with vias.

10.2 Layout Example



Green - Top Layer, Purple - Layer 3, Blue - Bottom Layer

图 10-1. SN65DSI8x Layout Example

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11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

11.3 Trademarks

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Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65DSI83ZXHR	Active	Production	NFBGA (ZXH) | 64	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DSI83
SN65DSI83ZXHR.A	Active	Production	NFBGA (ZXH) | 64	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DSI83
SN65DSI83ZXHR.B	Active	Production	NFBGA (ZXH) | 64	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DSI83

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN65DSI83 :

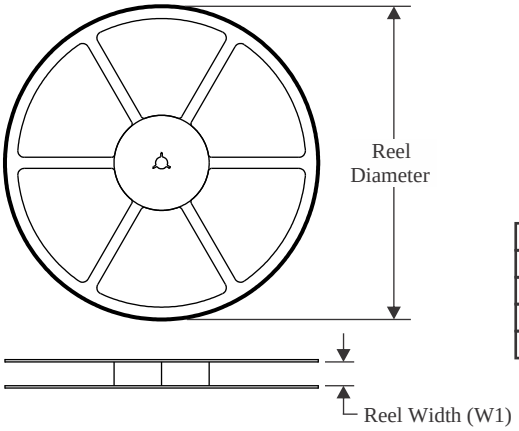
- Automotive : SN65DSI83-Q1

NOTE: Qualified Version Definitions:

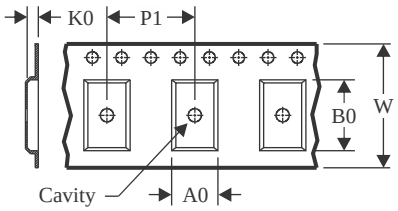
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

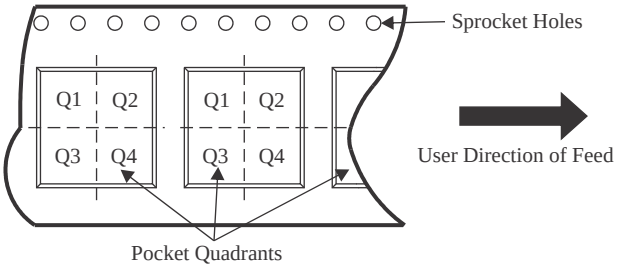


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

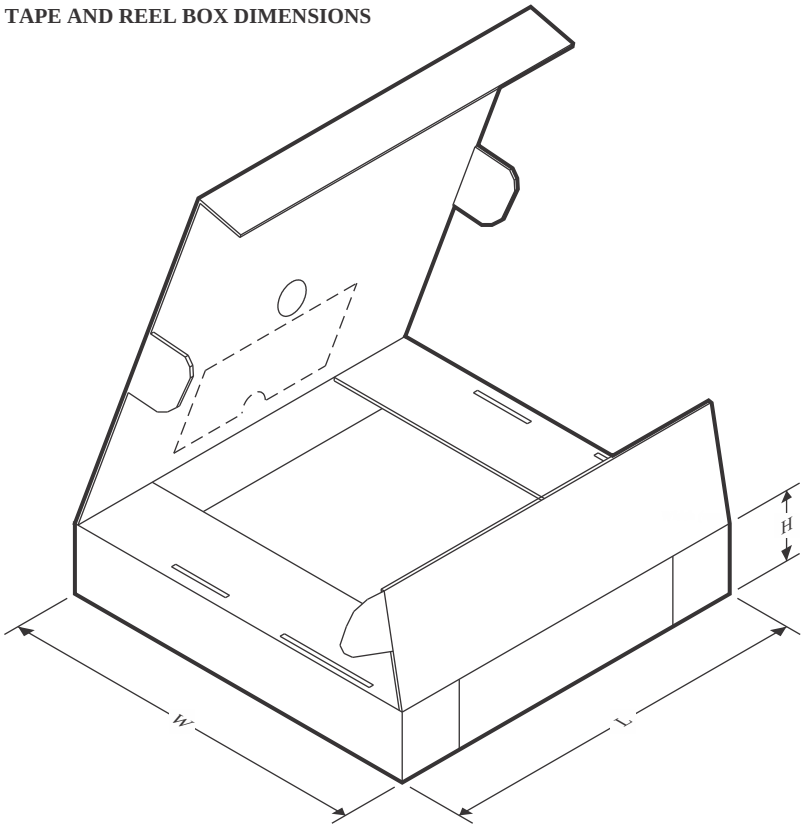
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

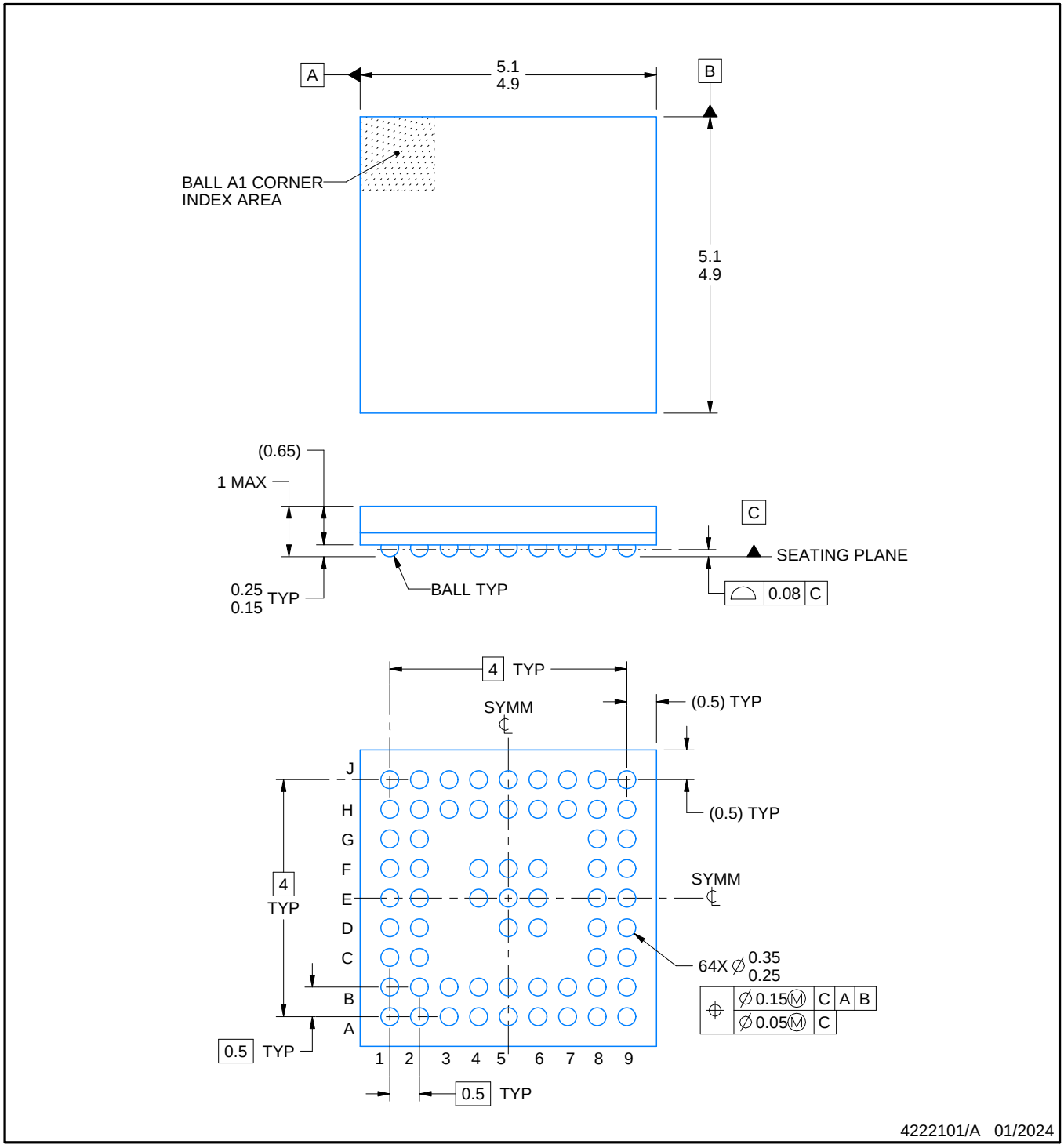
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65DSI83ZXHR	NFBGA	ZXH	64	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



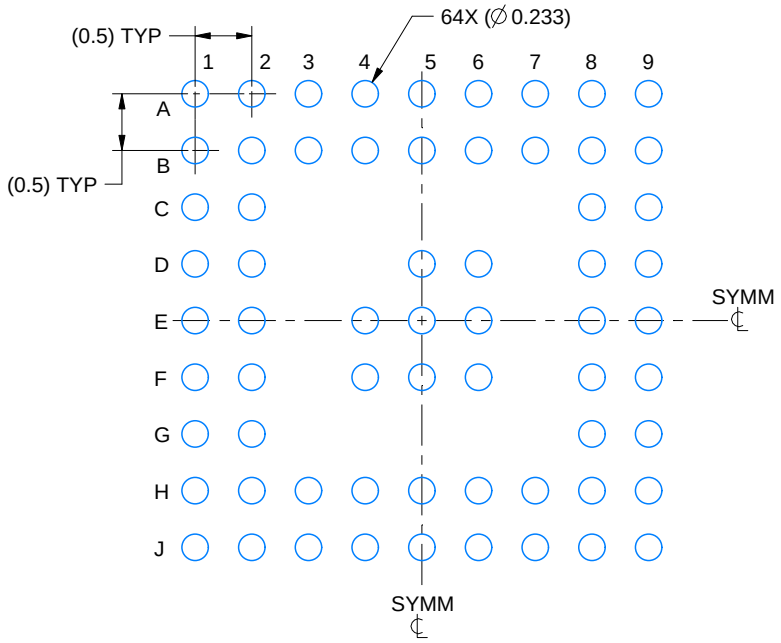
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65DSI83ZXHR	NFBGA	ZXH	64	2500	336.6	336.6	31.8

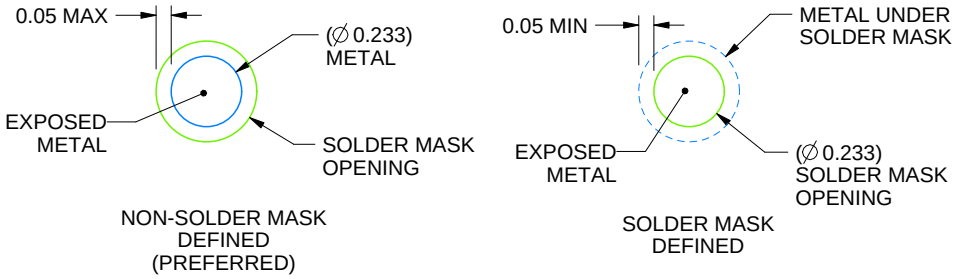


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

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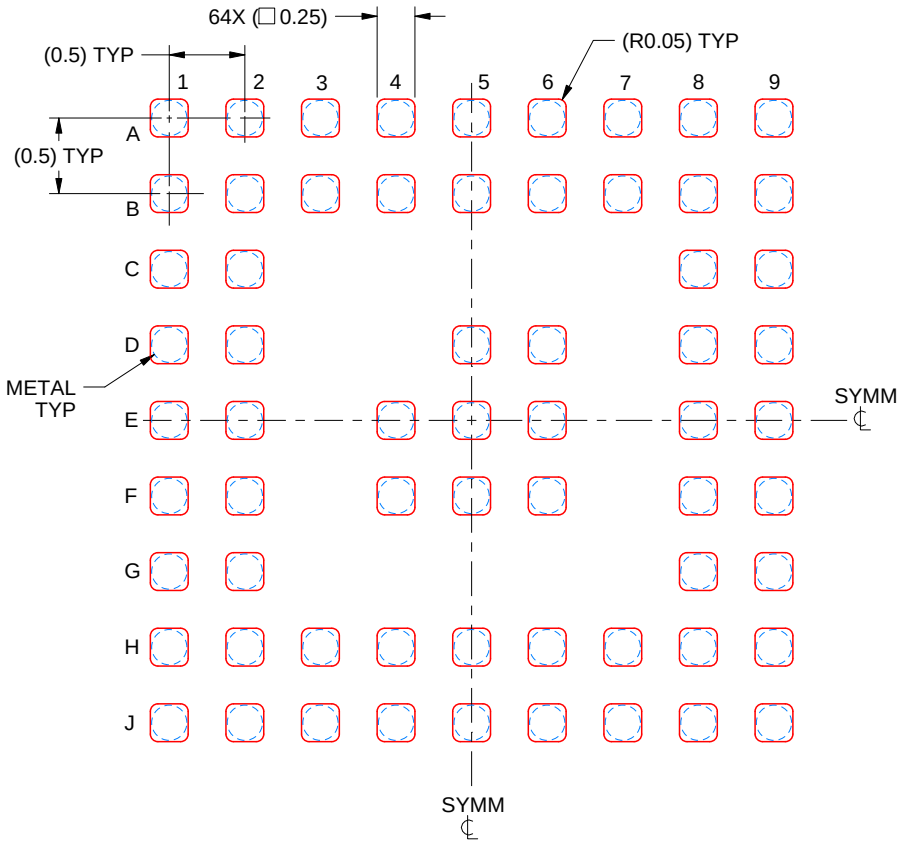
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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