UCC28610 绿色模式反激式控制器

1 特性

- 级联配置可实现完全集成式电流控制而无需外部传感电阻器
- 具有由共源共栅配置实现的低待机功耗的快速启动
- 针对整个运行范围内最优效率的频率和峰值电流调制
- 绿色环保模式 (GM) 突发开关数据包提升无负载效率
- 高级过流保护限制均方根 (RMS) 输入和输出电流
- 热关断
- 支持重试或锁存响应的定时过载
- 可编程无光耦输出过压保护
- 快速闭锁故障恢复
- 8 引脚小外形尺寸集成电路 (SOIC) 封装以及 8 引脚塑料双列直插 (PDIP) 无铅封装

2 应用

- 通用输入交流和直流适配器，12 至 65W
- 高效内务处理和辅助电源
- 离线电池充电器
- 消费类电子产品（DVD 播放器、机顶盒、数字电视、游戏机和打印机）

3 说明

UCC28610 将交流和直流消费类电源解决方案的性能和可靠性水平提高到全新的水平。

一个脉宽调制 (PWM) 调制算法在整个运行范围内保持断续或转换模式运行的同时，变化开关频率和初级电流。与一个共源共栅架构组合在一起，这些技术创新在一个传统反激式架构中改进了效率、可靠性和系统成本。

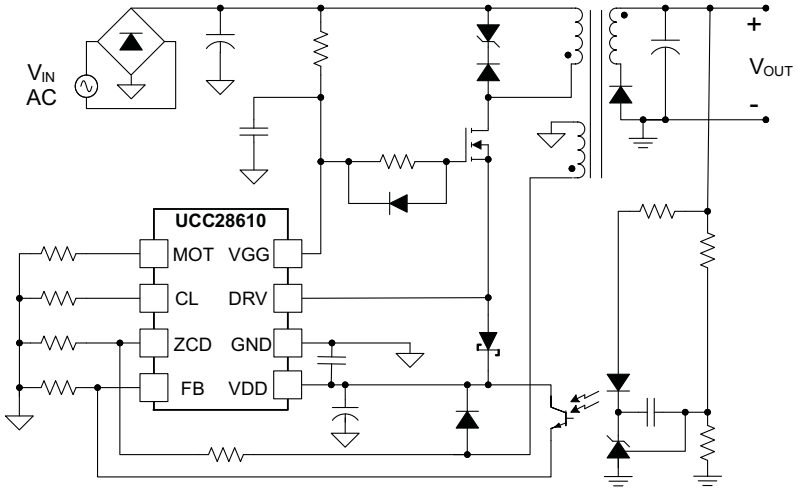
UCC28610 提供一个可预期的最大功率阈值，以及一个针对过载的定时响应，从而实现对浪涌功率要求的安全处理。对于重试或锁存模式，过载故障响应是可由用户设定的。额外保护 功能 包括输出过压检测、可编程最大导通时间和热关断。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC28610	SOIC (8)	4.90mm x 3.91mm
	PDIP (8)	9.81mm x 6.35mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化应用电路原理图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (November 2014) to Revision G — **Page**

- 已添加 *引脚配置和功能* 部分、*ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1

Changes from Revision E (September 2012) to Revision F — **Page**

- 已更改 更改了首页上的已更新典型应用图。 ... 1
- Added Thermal Information Section. ... 5
- Changed ESD Rating, Human Body Model from 2000 V to 1500 V. ... 5
- Changed *Electrical Characteristics* FB = 0 V to IFB = 10 µA. ... 6
- Changed Voltage of CL pin max value from 1.05 V to 1.10 V. ... 7
- Changed I_{FB} range for Green Mode (GM) modulation min value from 50 µA to 45 µA. ... 7
- Changed ZCD low clamp voltage min value from -200 mV to -220 mV. ... 7
- Changed Figure 1. ... 8
- Changed Symplified Block Diagram ... 11
- Changed Figure 20. ... 16
- Changed High Frequency Ringing Solutions, (a) ferrite chip, (b) CDRV and (c) RG-OFF drawing. ... 17
- Changed Basic Flyback Converter and Waveforms at Peak Load and Minimum V_{BULK} Voltage drawing. ... 19
- Changed Start-Up Currents for the Cascode Architecture drawing. ... 22
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Changes from Revision D (January 2011) to Revision E **Page**

- Changed Symplified Block Diagram 11

Changes from Revision C (January 2009) to Revision D **Page**

- Deleted Equation 7 20
- Deleted Equation 7 34

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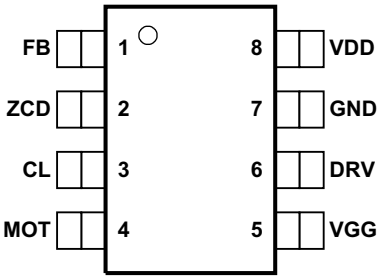
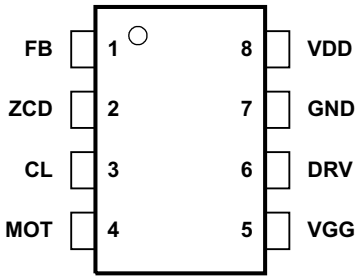
5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



P Package
8-Pin PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CL	3	I	**(Current Limit)** This pin programs the peak primary inductor current that is reached each switching cycle. Program with a resistor between CL and GND.
DRV	6	O	**(DRiVe)** This pin drives the source of an external high voltage power MOSFET. The DRV pin carries the full primary current of the converter. Connect a Schottky diode between DRV and VDD to provide initial bias at start up.
FB	1	I	**(FeedBack)** The FB current, I_{FB}, commands the operating mode of the UCC28610. The FB voltage is always 0.7 V. This pin only detects current.
GND	7	—	**(GrouND)** This pin is the current return terminal for both the analog and power signals in the UCC28610. This terminal carries the full primary current of the converter. Separate the return path of the bulk capacitor from the return path of FB, ZCD, MOT, and CL.
MOT	4	I	**(Maximum On Time)** This pin has three functions: 1. MOT programs the allowed maximum on-time, t_{MOT}, of the internal driver. 2. MOT programs the converter's reaction to overload and power input under-voltage conditions with either a shutdown/retry response or a latch-off response. 3. MOT can be used to externally shut down the power supply by pulling MOT to GND. When the pin is released, the converter will start after a restart delay, t_{RETRY}. Functions 1 and 2 are programmed with a resistor between MOT and GND.
VDD	8	—	This is the bias supply pin for the UCC28610. It can be derived from an external source or an auxiliary winding. This pin must be decoupled with a 0.1-μF ceramic capacitor placed between VDD and GND, as close to the device as possible.
VGG	5	—	This pin provides a DC voltage for the gate of the external high voltage MOSFET. This pin must be decoupled with a 0.1-μF ceramic capacitor placed between VGG and GND, as close to the device as possible. This pin also initiates start-up bias through a large value resistor that is connected to the input bulk voltage.
ZCD	2	I	**(Zero Current Detection)** This pin has two functions: 1. ZCD senses the transformer reset based on a valid zero current detection signal. 2. ZCD programs the output Over Voltage Protection (OVP) feature using a resistive divider on the primary side bias winding of the Flyback transformer.

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6 Specifications

6.1 Absolute Maximum Ratings

All voltages are with respect to GND, –40°C < T_J = T_A < 125°C, all currents are positive into and negative out of the specified terminal (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage range	VDD	–0.5	25	V
	DRV, during conduction	–0.5	2.0	
	DRV, during non-conduction		20	
	VGG (2)	–0.5	16	
	ZCD, MOT, CL (3)	–0.5	7	
	FB (3)	–0.5	1.0	
	VDD – VGG	–7	10	
Continuous input current	I_{VGG} (2)		10	mA
Input current range	I_{ZCD}, I_{MOT}, I_{CL}, I_{FB} (3)	–3	1	
Peak output current	DRV		-5	A
	DRV, pulsed 200ns, 2% duty cycle	–5	1.5	
T_J	Operating junction temperature,	–40	150	°C
	Lead Temperature (soldering, 10 sec.)		260	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) These are stress ratings only. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability
(2) Voltage on VGG is internally clamped. The clamp level varies with operating conditions. In normal use, VGG is current fed with the voltage internally limited
(3) In normal use, MOT, CL, ZCD, and FB are connected to resistors to GND and internally limited in voltage swing

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	1500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Unless otherwise noted, all voltages are with respect to GND, -40°C < T_J = T_A < 125°C. Components reference, Figure 34.

			MIN	MAX	UNIT
VDD	Input voltage		9	20	V
VGG	Input voltage from low-impedance source		9	13	V
I_{VGG}	Input current from a high-impedance source		10	2000	µA
R_{MOT}	Resistor to GND	Shutdown/Retry mode	25	100	kΩ
		Latch-off mode	150	750	kΩ
R_{CL}	Resistor to GND		24.3	100	kΩ
R_{ZCD1}	Resistor to auxiliary winding		50	200	kΩ
C_{VGG}	VGG capacitor		33	200	nF
C_{BP}	VDD bypass capacitor, ceramic		0.1	1	µF

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6.4 Thermal Information

THERMAL METRIC (1)		UCC28610 D (SOIC) 8 PINS	UCC28610 P (PDIP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.5	56.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.7	45.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.8	33.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.3	22.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.3	33.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise stated: VDD = 12 V, VGG = 12 V, ZCD = 1 V, I_{FB} = 10 µA, GND = 0 V, a 0.1-µF capacitor between VDD and GND, a 0.1-µF capacitor between VGG and GND, R_{CL} = 33.2 kΩ, R_{MOT} = 380 kΩ, –40°C < T_A < +125°C, T_J = T_A

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD and VGG SUPPLY						
$VGG_{(OPERATING)}$	VGG voltage, operating	VDD = 14 V, I_{VGG} = 2.0 mA	13	14	15	V
$VGG_{(DISABLED)}$	VGG voltage, PWM disabled	VDD = 12 V, I_{VGG} = 15 µA, I_{FB} = 350 µA	15	16	17	V
ΔVGG	Rise in VGG clamping voltage during UVLO, GM, or Fault	$VGG_{(DISABLED)}$ – $VGG_{(OPERATING)}$	1.75	2.00	2.15	V
$I_{VGG(SREG)}$	VGG shunt regulator current	VGG = $VGG_{(DISABLED)}$ -100 mV, VDD = 12 V		6	10	µA
$\Delta VGG_{(SREG)}$	VGG shunt load regulation	10 µA ≤ I_{VGG} ≤ 5 mA, I_{FB} = 350 µA		125	200	mV
$VGG_{(LREG)}$	VGG LDO regulation voltage	VDD = 20 V, I_{VGG} = – 2 mA		13		V
$VGG_{(LREG,\ DO)}$	VGG LDO Dropout Voltage	VDD – VGG, VDD = 11 V, I_{VGG} = – 2 mA	1.5	2	2.5	V
$VDD_{(ON)}$	UVLO turn-on threshold		9.7	10.2	10.7	V
$VDD_{(OFF)}$	UVLO turn-off threshold		7.55	8	8.5	V
$\Delta VDD_{(UVLO)}$	UVLO hysteresis		1.9	2.2	2.5	V
$I_{VDD(OPERATING)}$	Operating current	VDD = 20 V	2.5	3	3.7	mA
$I_{VDD(GM)}$	Idle current between bursts	I_{FB} = 350 µA		550	900	µA
$I_{VDD(UVLO)}$	Current for VDD < UVLO	VDD = $VDD_{(ON)}$ – 100 mV, increasing		225	310	µA
$R_{DS,ON(VDD)}$	VDD Switch on resistance, DRV to VDD	VGG = 12 V, VDD = 7V, I_{DRV} = 50 mA		4	10	Ω
$VDD_{(FAULT\ RESET)}$	VDD for fault latch reset		5.6	6	6.4	V
MODULATION						
$t_{S(HF)}$ (1)	Minimum switching period, frequency modulation (FM) mode	I_{FB} = 0 µA, (1)	7.125	7.5	7.875	µs
$t_{S(LF)}$ (1)	Maximum switching period, reached at end of FM modulation range	I_{FB} = $I_{FB,\ CNR3}$ – 20 µA, (1)	31	34	38	µs
$I_{DRVpk(max)}$	Maximum peak driver current over amplitude modulation(AM) range	I_{FB} = 0 µA, R_{CL} = 33. 2 kΩ	2.85	3	3.15	A
		I_{FB} = 0 µA, R_{CL} = 100 kΩ	0.80	0.90	1.0	
$I_{DRVpk(min)}$	Minimum peak driver current reached at end of AM modulation range	$I_{FB,\ CNR2}$ + 10 µA, R_{CL} = 33.2 kΩ	0.7	0.85	1.1	A
		$I_{FB,\ CNR2}$ + 10 µA, R_{CL} = 100 kΩ	0.2	0.33	0.5	
K_P	Maximum power constant	$I_{DRVpk(max)}$ = 3 A	0.54	0.60	0.66	W/µH
$I_{DRVpk(absmin)}$	Minimum peak driver independent of R_{CL} or AM control	R_{CL} = OPEN	0.3	0.45	0.6	A

(1) t_S sets a minimum switching period. Following the starting edge of a PWM on time, under normal conditions, the next on time is initiated following the first zero crossing at ZCD after t_S. The value of t_S is modulated by I_{FB} between a minimum of $t_{S(HF)}$ and a maximum of $t_{S(LF)}$ In normal operation, $t_{S(HF)}$ sets the maximum operating frequency of the power supply and $t_{S(LF)}$ sets the minimum operating frequency of the power supply.

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Electrical Characteristics (continued)

Unless otherwise stated: VDD = 12 V, VGG = 12 V, ZCD = 1 V, I_{FB} = 10 µA, GND = 0 V, a 0.1-µF capacitor between VDD and GND, a 0.1-µF capacitor between VGG and GND, R_{CL} = 33.2 kΩ, R_{MOT} = 380 kΩ, –40°C < T_A < +125°C, T_J = T_A

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{BLANK(Ilim)}$	Leading edge current limit blanking time	I_{FB} = 0 µA, R_{CL} = 100 kΩ, 1.2-A pull-up on DRV	120	220	450	ns
V_{CL}	Voltage of CL pin	I_{FB} = 0 µA	2.94	3	3.06	V
		I_{FB} = ($I_{FB,CNR3}$ – 20 µA) (1)	0.95	1.00	1.10	
$I_{FB,CNR1}$ (2)	I_{FB} range for FM modulation	I_{FB} increasing, t_S = $t_{S(LF)}$, I_{DRVpk} = $I_{DRVpk(max)}$	145	165	195	µA
$I_{FB,CNR2}$ – $I_{FB,CNR1}$ (2)	I_{FB} range for AM modulation	t_S = $t_{S(LF)}$, I_{DRVpk} ranges from $I_{DRVpk(max)}$ to $I_{DRVpk(min)}$	35	45	65	µA
$I_{FB,CNR3}$ – $I_{FB,CNR2}$ (2)	I_{FB} range for Green Mode (GM) modulation	I_{FB} increasing until PWM action is disabled entering a burst-off state	45	70	90	µA
$I_{FB,\ GM\text{-}HYST}$ (2)	I_{FB} hysteresis during GM modulation to enter burst on and off states	I_{FB} decreasing from above $I_{FB,CNR3}$	10	25	40	µA
V_{FB}	Voltage of FB pin	I_{FB} = 10 µA	0.34	0.7	0.84	V
ZERO CROSSING DETECTION						
$ZCD_{(TH)}$	ZCD zero crossing threshold	ZCD high to low generates switching period (t_S has expired)	5	20	50	mV
$ZCD_{(CLAMP)}$	ZCD low clamp voltage	I_{ZCD} = –10 µA	-220	-160	-100	mV
$ZCD_{(START)}$	ZCD voltage threshold to enable the internal start timer	Driver switching periods generated at start timer rate	0.1	0.15	0.2	V
$t_{DLY(ZCD)}$	Delay from zero crossing to Driver turn-on	150-Ω pull-up to 12-V on DRV		150		ns
$t_{WAIT(ZCD)}$	Wait time for zero crossing detection	Driver turn-on edge generated following t_S with previous zero crossing detected	2	2.4	2.8	µs
t_{ST}	Starter time-out period	ZCD = 0 V	150	240	300	
DRIVER						
$R_{DS(on)(DRV)}$	Driver on-resistance	I_{DRV} = 4.0 A		90	190	mΩ
$I_{DRV(OFF)}$	Driver off-leakage current	DRV = 12 V		1.5	20	µA
$R_{DS(on)(HSDRV)}$	High-side driver on-resistance	I_{DRV} = –50 mA		6	11	Ω
$I_{DRV(DSCH)}$	DRV bulk discharge current	VDD open, DRV= 12 V, Fault latch set	2	2.8	3.6	mA
OVERVOLTAGE FAULT						
$ZCD_{(OVP)}$	Overvoltage fault threshold at ZCD	Fault latch set	4.85	5	5.15	V
$t_{BLANK(OVP)}$	ZCD blanking and OVP sample time from the turn-off edge of DRV		0.6	1	1.7	µs
$I_{ZCD(bias)}$	ZCD Input bias current	ZCD = 5 V	-0.1	-0.05	0.1	µA
OVERLOAD FAULT						
$I_{FB(OL)}$	Current to trigger overload delay timer		0	1.5	3	µA
t_{OL}	Delay to overload fault	I_{FB} = 0 A continuously	200	250	325	ms
t_{RETRY}	Retry delay in retry mode or after shutdown command	R_{MOT} = 76 kΩ		750		ms
$R_{MOT(TH)}$	Boundary R_{MOT} between latch-off and retry modes	See (3)	100	120	150	kΩ
SHUTDOWN THRESHOLD						
$MOT_{(SR)}$	Shutdown-Retry threshold	MOT high to low	0.7	1	1.3	V
I_{MOT}	MOT current when MOT is pulled low	MOT = 1 V	–600	–450	–300	µA

(2) Refer to Figure 1.
(3) A latch-off or a shutdown and retry fault response to a sustained overload is selected by the range of R_{MOT}.
To select the latch-off mode, R_{MOT} should be greater than 150 kΩ and t_{MOT} is given by $R_{MOT} \times (1.0 \times 10^{-11})$.
To select the shutdown-retry mode, R_{MOT} should be less than 100 kΩ and t_{MOT} is given by $R_{MOT} \times (5.0 \times 10^{-11})$.

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Electrical Characteristics (continued)

Unless otherwise stated: VDD = 12 V, VGG = 12 V, ZCD = 1 V, I_{FB} = 10 µA, GND = 0 V, a 0.1-µF capacitor between VDD and GND, a 0.1-µF capacitor between VGG and GND, R_{CL} = 33.2 kΩ, R_{MOT} = 380 kΩ, –40°C < T_A < +125°C, T_J = T_A

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MAXIMUM ON TIME						
t_{MOT}	Latch-OFF	R_{MOT} = 383 kΩ	3.43	3.83	4.23	µs
	Shutdown-retry	R_{MOT} = 76 kΩ	3.4	3.8	4.2	
MOT	MOT voltage		2.7	3	3.3	V
THERMAL SHUTDOWN						
T_{SD} (4)	Shutdown temperature	T_J, temperature rising (4)		165		°C
T_{SD_HYS} (4)	Hysteresis	T_J, temperature falling, degrees below T_{SD} (4)		15		°C

(4) Thermal shutdown occurs at temperatures higher than the normal operating range. Device performance at or near thermal shutdown temperature is not specified or assured.

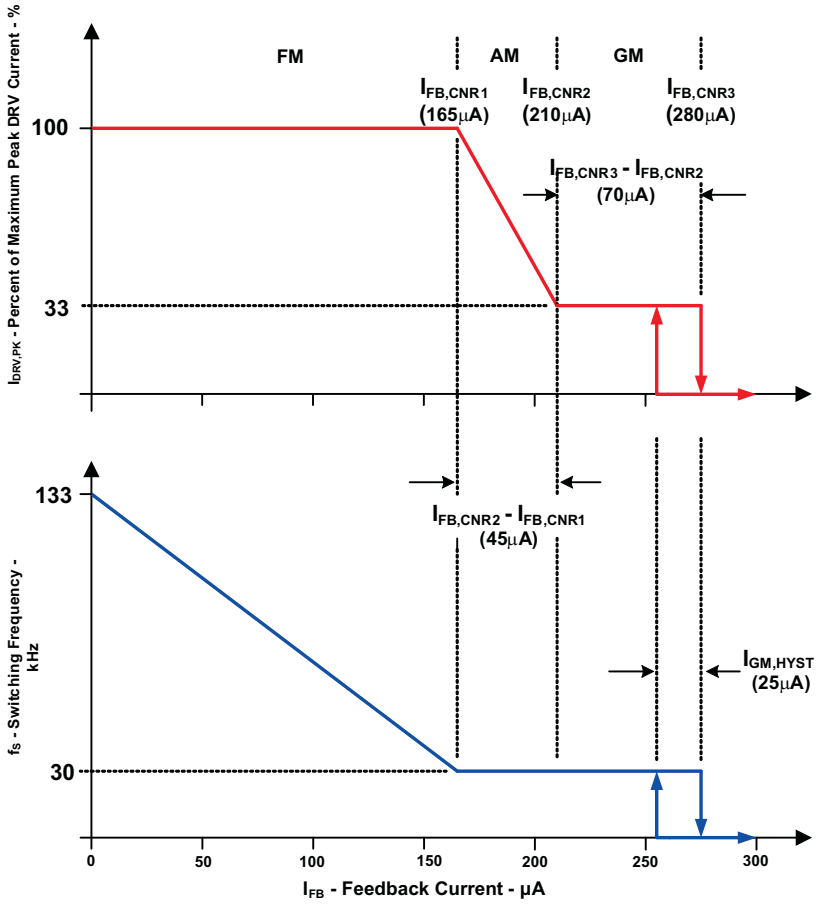

Figure 1. FB Electrical Condition Detail

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6.6 Typical Characteristics

Unless otherwise stated: VDD = 12 V, VGG = 12 V, ZCD = 1 V, I_{FB} = 10 µA, GND = 0 V, a 0.1-µF capacitor between VDD and GND, a 0.1-µF capacitor between VGG and GND, R_{CL} = 33.2 kΩ, R_{MOT} = 380 kΩ, –40°C < T_A < +125°C, T_J = T_A

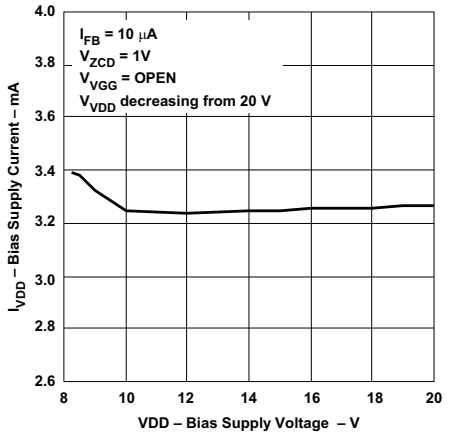

Figure 2. Bias Supply Current vs Bias Supply Voltage During Operation

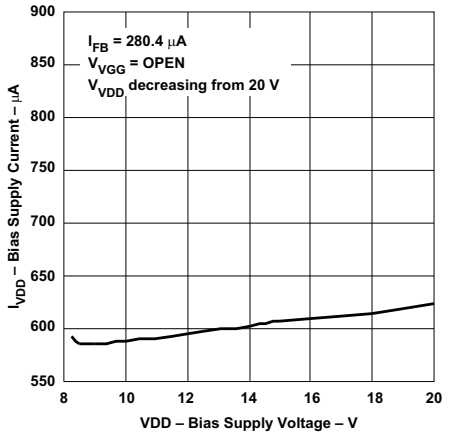

Figure 3. Bias Supply Current vs Bias Supply Voltage During Green Mode

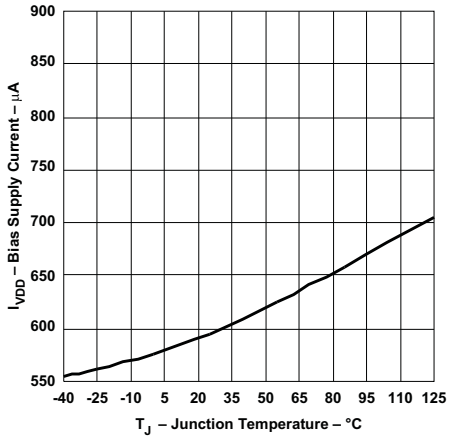

Figure 4. Bias Supply Current vs Temperature During Green Mode

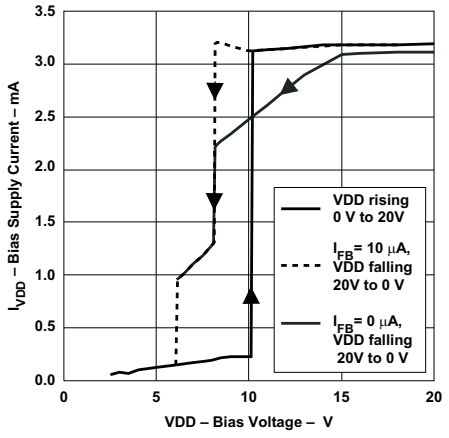

Figure 5. Operational I_{VDD} – Bias Current vs Bias Voltage

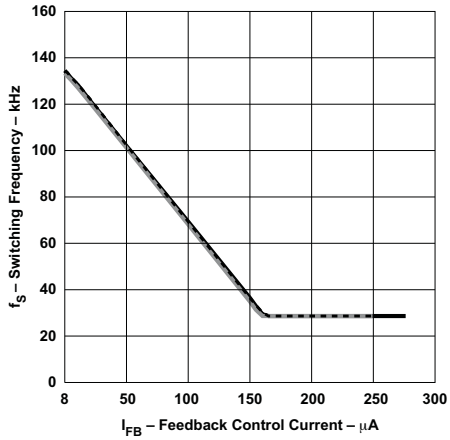

Figure 6. Oscillator Frequency vs Feedback Current

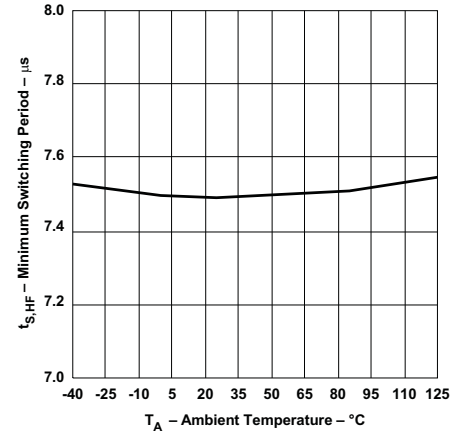

Figure 7. Minimum Switching Period vs Temperature

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Typical Characteristics (continued)

Unless otherwise stated: VDD = 12 V, VGG = 12 V, ZCD = 1 V, I_{FB} = 10 µA, GND = 0 V, a 0.1-µF capacitor between VDD and GND, a 0.1-µF capacitor between VGG and GND, R_{CL} = 33.2 kΩ, R_{MOT} = 380 kΩ, –40°C < T_A < +125°C, T_J = T_A

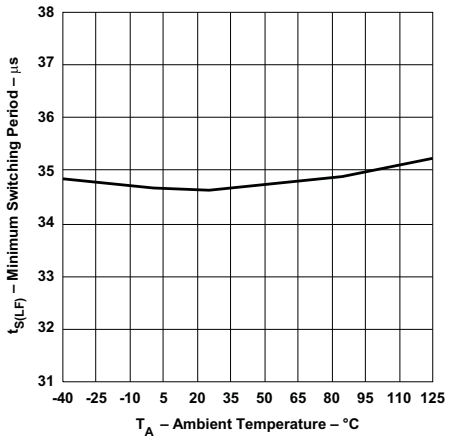

Figure 8. Switching Period During Amplitude Modulaltion vs Ambient Temperature

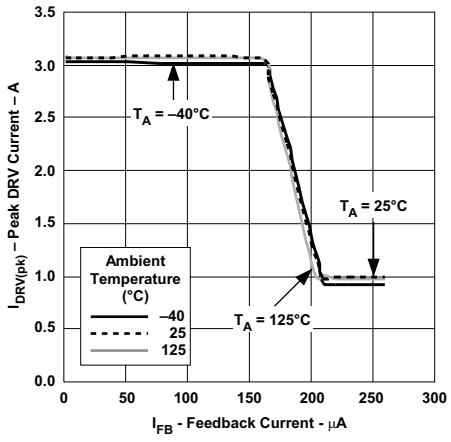

Figure 9. Peak DRV Current vs Feedback Current

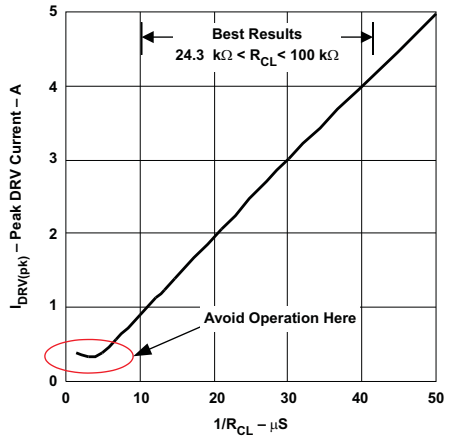

Figure 10. Peak DRV Current vs Transconductance (1/R_{CL})

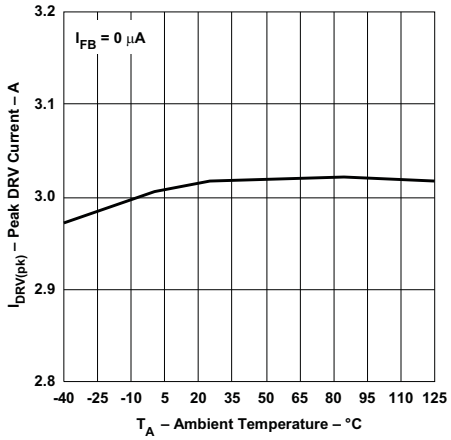

Figure 11. Peak DRV Current vs Ambient Temperature

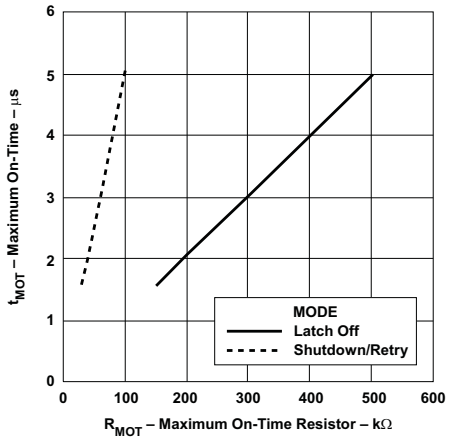

Figure 12. Maximum On Time vs Maximum On-Time Resistance

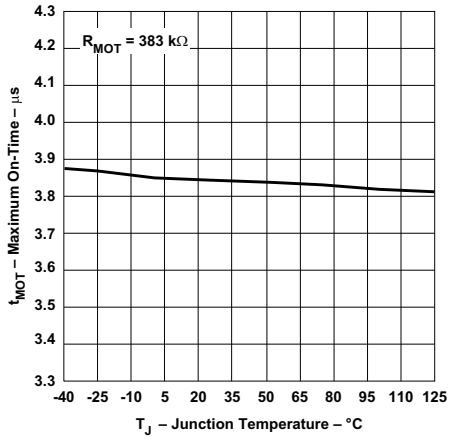

Figure 13. Maximum On Time vs Junction Temperature

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Typical Characteristics (continued)

Unless otherwise stated: VDD = 12 V, VGG = 12 V, ZCD = 1 V, I_{FB} = 10 µA, GND = 0 V, a 0.1-µF capacitor between VDD and GND, a 0.1-µF capacitor between VGG and GND, R_{CL} = 33.2 kΩ, R_{MOT} = 380 kΩ, –40°C < T_A < +125°C, T_J = T_A

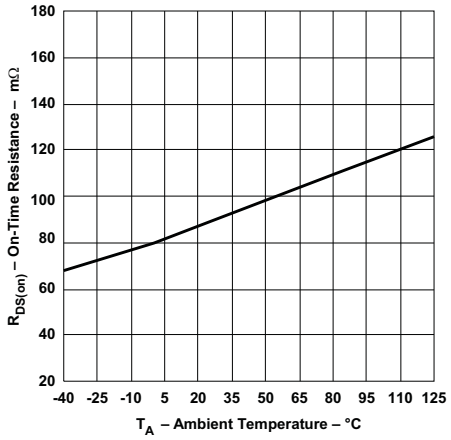

Figure 14. Driver $R_{DS(on)}$ vs Ambient Temperature

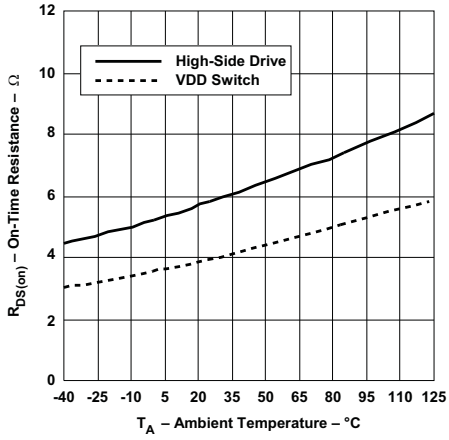

Figure 15. $R_{DS(on)}$ of High Side Drive and VDD Switch vs Temperature

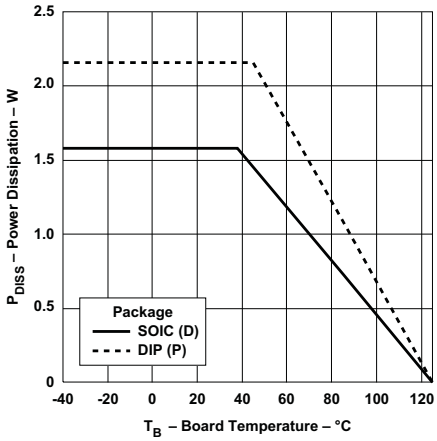

Figure 16. Safe Operating Area vs Board Temperature

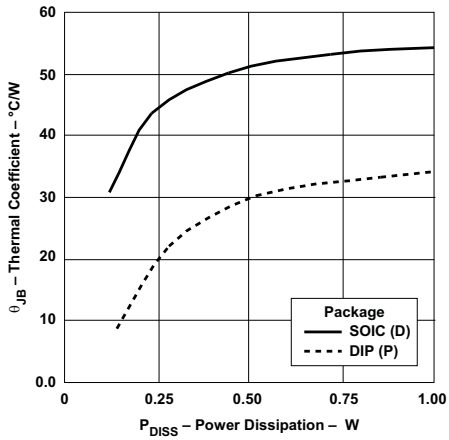

Figure 17. Thermal Coefficient – θ_{JB} vs Power Dissipation

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7 Detailed Description

7.1 Overview

The flyback converter is attractive for low power AC/DC applications because it provides output isolation and wide input operating abilities using a minimum number of components. Operation of the flyback converter in Discontinuous Conduction Mode (DCM) is especially attractive because it eliminates reverse recovery losses in the output rectifier and it simplifies control.

The UCC28610 is a flyback controller for 12-W to 65-W, peak AC/DC power supply applications that require both low AC line power during no-load operation and high average efficiency. This controller limits the converter to DCM operation. It does not allow Continuous Conduction Mode (CCM) operation. Forced DCM operation results in a uniquely safe current limit characteristic that is insensitive to AC line variations. The peak current mode modulator does not need slope compensation because the converter operates in DCM.

The operation of the UCC28610 is facilitated by driving the external high voltage MOSFET through the source. This configuration is called a cascode driver. It features fast start-up and low input power under no-load conditions without having high voltage connections to the control device. The cascode driver has no effect on the general operation of the flyback converter.

The feedback pin uses current rather than voltage. This unique feature minimizes primary side power consumption during no-load operation by avoiding external resistive conversion from opto-coupler current to voltage.

Average efficiency is optimized by the UCC28610 between peak power and 22% peak power with constant peak current, variable off-time modulation. This modulation tends to make the efficiency constant between 22% and 100% peak load, eliminating the need to over-design to meet average efficiency levels that are required by EnergyStar™.

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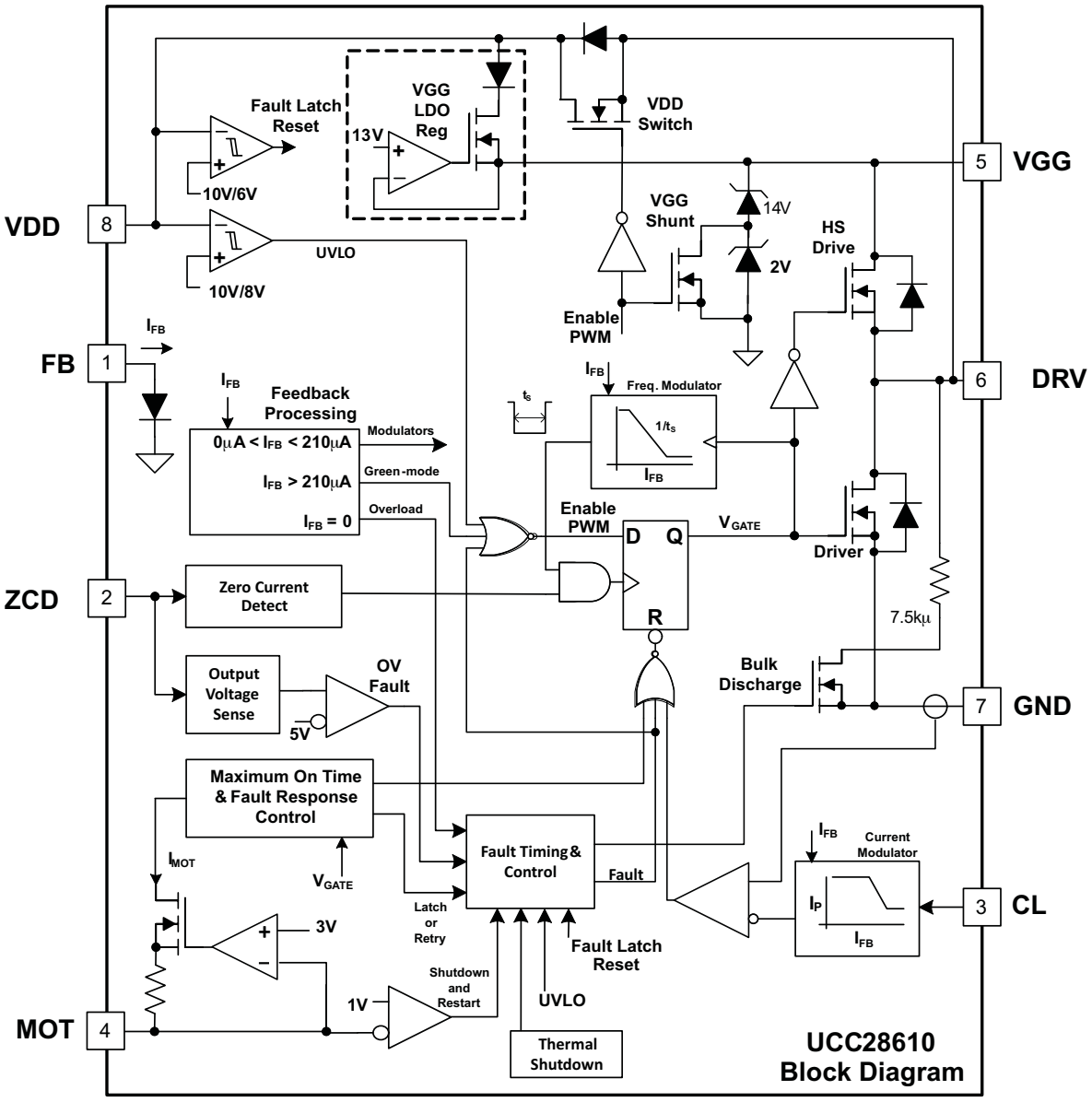
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fault Recovery

The UCC28610 reacts with the programmed overload response if the overload lasts longer than t_{OL} (nominally 250 ms). The overload fault responses are either (1) latch-off or (2) shutdown/retry after a retry delay of 750 ms. The overload response is programmed with the MOT pin. The forced DCM feature prevents transformer saturation and limits the average and RMS output currents of the secondary winding of the transformer. Even under short circuit load conditions, the output current of the transformer is limited to the levels that are shown in Equation 1, where N_{PS} is the primary-to-secondary turns ratio. Typical behavior for a shorted load is shown in Figure 18.

Feature Description (continued)

$$I_{SECONDARY,AVG(SHORTEDLOAD)} = \frac{N_{PS} \times I_{DRV(PEAK)}}{2}$$

$$I_{SECONDARY,RMS(SHORTEDLOAD)} = \frac{N_{PS} \times I_{DRV(PEAK)}}{\sqrt{3}} \quad (1)$$

In shutdown/retry mode switching will be re-enabled after the 750-ms retry delay. In latch-off mode, a 7.5-kΩ load is activated at the DRV pin upon the activation by a fault condition. The internal 7.5-kΩ load draws current from the bulk capacitor through the HVMOSFET and the transformer primary winding. The bias voltage, VDD, is also regulated by the HVMOSFET during the latch-off state. Once the AC line is removed, a 2.8-mA current, $I_{DRV,DSCH}$, will discharge the bulk capacitor. Ultimately, VDD will discharge when the bulk voltage becomes sufficiently low. A normal start-up cycle can occur if the input voltage is applied after VDD falls below the fault reset level, $VDD_{(FAULT\ RESET)}$, which is approximately equal to 6 V.

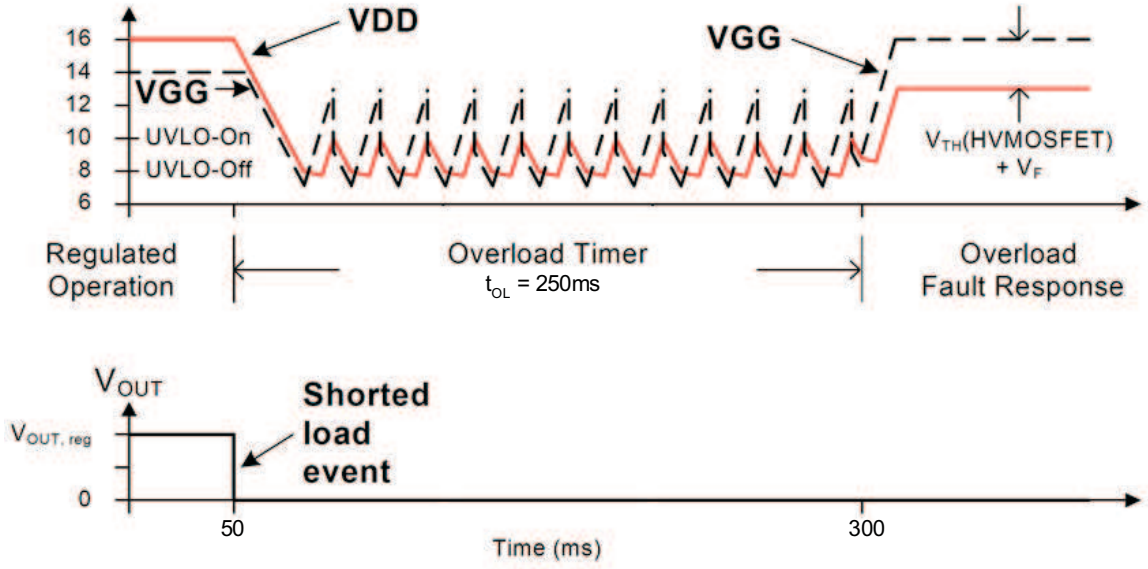


Figure 18. Overload Behavior with a Shorted Output

7.3.2 Maximum On-Time and Brown Out

The forced DCM feature provides protection against excessive primary currents in the event that the input voltage becomes very low. The highest possible secondary currents can be described by Equation 1. The UCC28610 adds further protection by allowing the user to program the maximum on-time.

The Maximum On-Time (MOT) function causes the converter to react as if there is an overload condition if the load is sufficiently large during a line sag condition. During low line conditions the MOT function limits the on-time of the primary switch which limits the peak current in the primary power stage. Figure 19 shows how the MOT period, t_{MOT}, is programmed over the range of 1.5 µs to 5 µs for either range of programming resistors. The resistor range determines the controller's response to a sustained overload fault – to either Latch-off or to Shutdown/Retry, which is the same response for a line-sag, or brown out, condition.

7.3.3 External Shutdown Using the MOT Pin

Many applications require the ability to shutdown the power supply with external means. This feature is easily implemented by connecting the collector and emitter of an NPN transistor between MOT and GND, respectively. The NPN transistor can be the photo-transistor of an opto-isolator for isolated applications.

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Feature Description (continued)

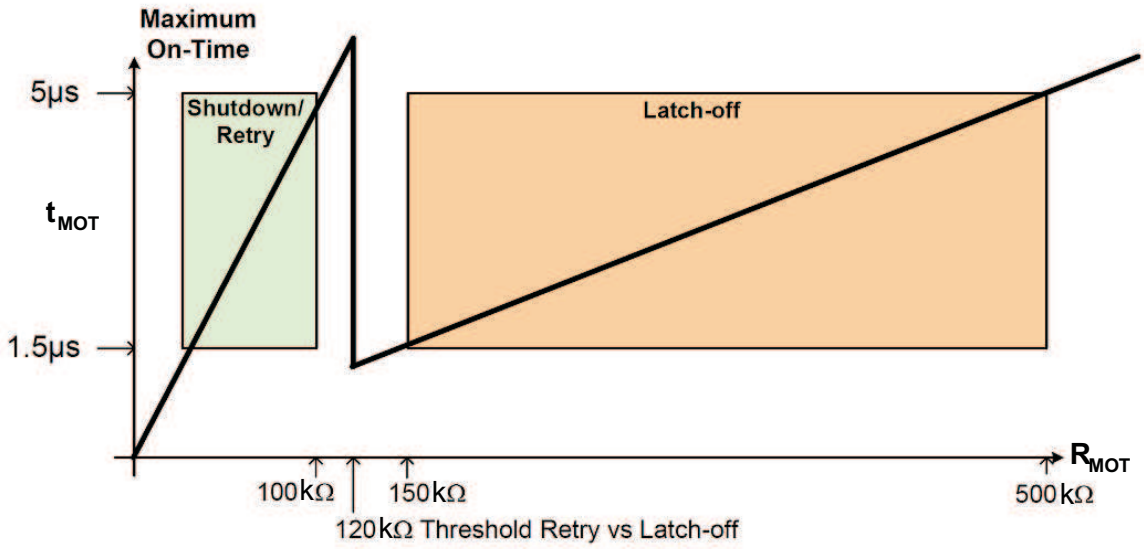

Figure 19. Programming MOT and Overload Fault Response

For latch-off response to over-current or brownout:

$$R_{MOT} = t_{MOT} \times \left(1 \times 10^{11} \frac{\Omega}{s}\right) \quad (2)$$

where:

$$150\ k\Omega \le R_{MOT} \le 500\ k\Omega$$
$$1.5\ \mu s \le t_{MOT} \le 5\ \mu s \quad (3)$$

For shut-down/retry response to over-current or brownout:

$$R_{MOT} = t_{MOT} \times \left(2 \times 10^{10} \frac{\Omega}{s}\right) \quad (4)$$

where:

$$25\ k\Omega \le R_{MOT} \le 100\ k\Omega$$
$$1.5\ \mu s \le t_{MOT} \le 5\ \mu s \quad (5)$$

7.3.4 Overvoltage Detection

The UCC28610 controller monitors the output voltage by sampling the voltage at the auxiliary winding. The sampling time has a fixed delay of 1 µs, $t_{BLANK,OVP}$, after the internal driver turns off. This allows the auxiliary winding to be sampled after the bias winding voltage settles from the transient. This same delay is used to blank the ZCD input to avoid unintended zero crossing detection should the ringing be large enough to cross the ZCD zero crossing threshold.

The output over-voltage (OV) threshold is set using the turn ratio of the auxiliary winding to the output secondary and a resistive divider into the ZCD input pin. The UCC28610 will always enter a latched-off state if it detects an OV condition. The VDD supply must cycle below the fault reset threshold to re-start in order to recover. The functionality of the over-voltage detection function is shown in Figure 20.

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Feature Description (continued)

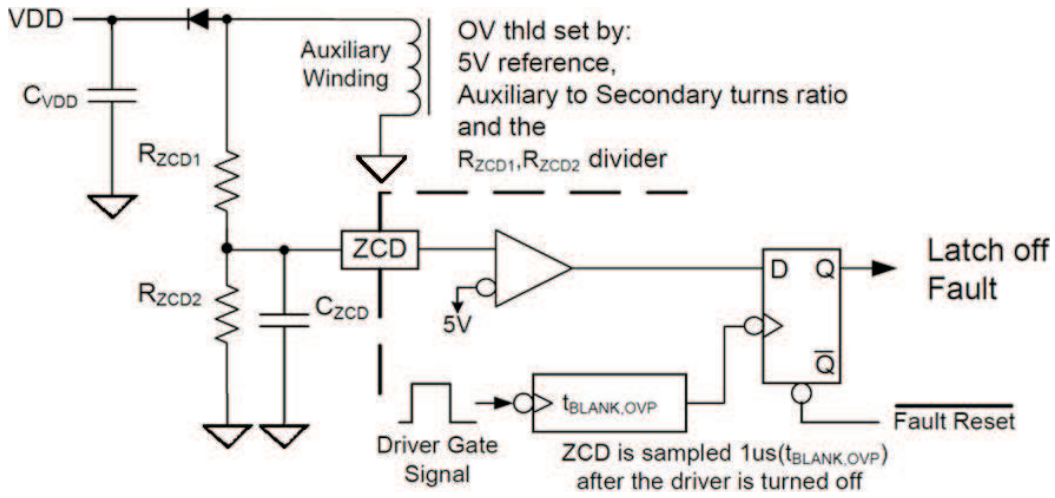

Figure 20. Output Over-Voltage Protection with ZCD Pin

7.3.5 Solving for High Frequency Ringing

Cascode drive circuits are well known for high speed voltage gain. This topology can have small signal bandwidth well over 100 MHz and it can exhibit high frequency ringing. The internal HS Drive MOSFET shorts the gate to source of the external HVMOSFET during the turn-off interval of the switch cycle. This prevents the HVMOSFET from undesirably exciting the LC resonant circuit in the converter (the magnetizing inductance of the transformer and the stray drain capacitance). High frequency ringing can appear within the built-in dead-time between the turn-off of DRV and the turn-on of the HS Drive. A large amount of energy is transferred through the power components during this dead-time. Excessive high frequency ringing can cause EMI problems and become destructive in some situations.

7.3.5.1 Identification of High Frequency Ringing

The high frequency ringing is the result of stray capacitances ringing with the stray inductance between the source of the HVMOSFET and the DRV pin. Low threshold voltage of the high voltage MOSFET and large peak DRV current can make the ringing worse. In destructive ringing situations, the converter may easily power up and attain regulation the first time, never to start-up again.

The ringing can be observed in either or both of the following conditions:

- The very first HVMOSFET turn-off event during a cold start of the converter (VGG > VDD).
- HVMOSFET turn-off edge under steady state, where the converter switches the HVMOSFET at the programmed $I_{DRV,PK}$ level (VDD > VGG).

7.3.5.2 Avoid HF Ringing

High frequency ringing problems with cascode MOSFET drives can often be avoided. Many converters will not have this problem because they use an HVMOSFET with a large V_{th}, large $R_{DS(on)}$, low transconductance gain, or operate at low current. Ringing problems can also be avoided by minimizing stray inductance. The trace between the HVMOSFET source and the DRV pin must be kept very short, less than 1 cm. Do not add current probe loops to the source lead of the HVMOSFET. Do not place ferrite beads on the source lead of the HVMOSFET.

If ringing cannot be avoided, the most efficient and effective methods to solve ringing during switching transients are:

1. A ferrite chip or bead connected to the gate of the HVMOSFET,
2. A small capacitor connected from DRV to GND and
3. A gate turn-off resistor. These three techniques can be used separately or combined, as shown in Figure 21.

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Feature Description (continued)

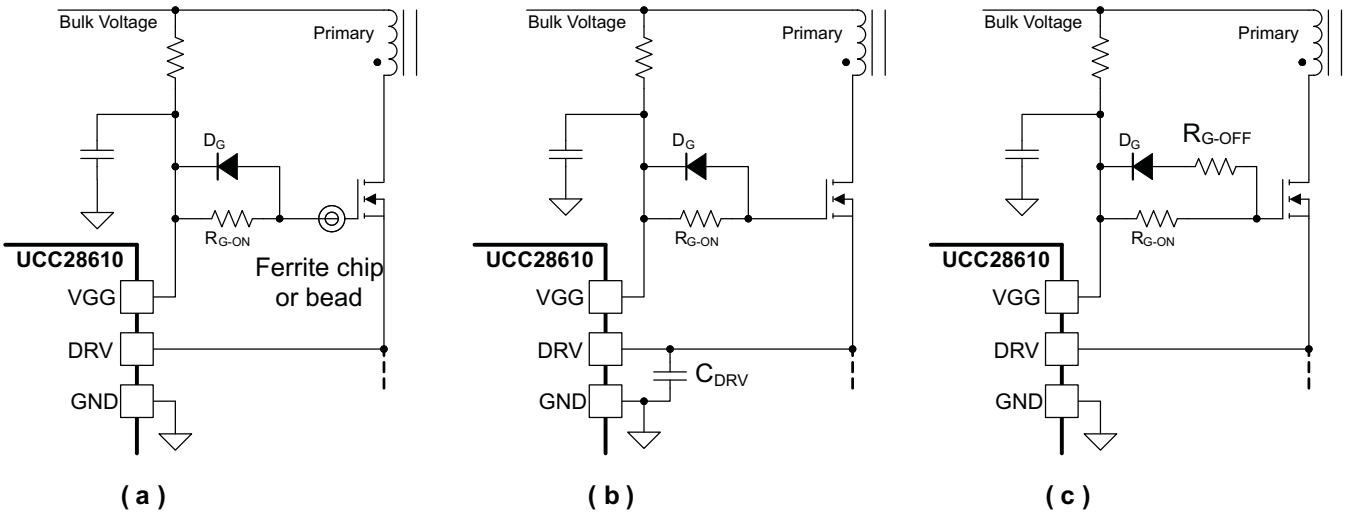

Figure 21. High Frequency Ringing Solutions, (a) ferrite chip, (b) CDRV and (c) RG-OFF

7.3.5.3 Ferrite Chip or Bead Solution

The ferrite chip or bead connected to the gate of the HVMOSFET provides the best result because it suppresses ringing in the gate, source, and drain circuits of the HVMOSFET with minimal added losses. Select the ferrite chip for its resistance value in the ringing frequency range (for example, 60 Ω at 100 MHz). The peak current rating of the ferrite chip or bead must be sufficient for the drain – gate discharge current that occurs during the turn-off transient. Excessively large bead reactance can result in low frequency surges of VGG at peak load. Normally, good results can be achieved with a 0603 ferrite chip device.

7.3.5.4 DRV Capacitor Solution

A capacitor between DRV and GND can reduce ringing on VGG. Select the DRV capacitor experimentally by observing the effect on the VGG pin during the first turn-off edge and during the turn-off edge at full load operation. The capacitor should be less than 3.3 nF so that it does not significantly reduce efficiency. Use a capacitor with a low Q, such as one with Y5V dielectric. This technique will not completely damp the ringing yet it can provide sufficient protection against stray inductance between the source of the HVMOSFET and the DRV pin.

7.3.5.5 Gate Turn-Off Resistor Solution

A gate turn-off resistor in the range 0 Ω < R_{G-OFF} < 5 Ω can damp ringing. The turn-off resistance is limited in order to prevent the stray source inductance of the HVMOSFET from over charging VGG through the body diode of the HS Drive MOSFET, in addition to any peak current error problems that would be caused by additional delay. The damping effect of the gate resistor works better in applications with low current and small source inductance.

A much larger resistance can be tolerated during the HVMOSFET turn-on transition due to DCM operation. The recommended turn-on resistance range is 0 Ω <R_{G-ON} < 200 Ω in order to prevent the turn-on delay from interfering with valley switching.

7.3.6 Thermal Shutdown

The UCC28610 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown point, T_{SD}, the UCC28610 initiates a shutdown event and permits retry after the retry time, t_{RETRY}. Shutdown/Retry cycles continue if the junction temperature is not less than T_{SD} minus T_{SD_HYST}.

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7.4 Device Functional Modes

According to the voltage and current among IC pins and the input voltage, output loading conditions, UCC28610 operates in different functional modes.

1. At startup, when VDD is below turn on threshold $VDD_{(ON)}$, VGG is clamped at $VGG_{(DISABLED)}$. Flyback MOSFET becomes a source follower with $VGG_{(DISABLED)}$ on its gate. This arrangement allows the VDD capacitor charge up till turn on threshold $VGG_{(ON)}$.
2. Once VDD exceed the turn on threshold $VGG_{(ON)}$, the IC start to switching and deliver power to the load. Before IC starts to switching, MOT pin detects its resistor value and set the fault response. Also, the VGG clamp is reduced from $VGG_{(DISABLED)}$ to $VGG_{(OPERATING)}$ to disable the startup operation mode.
3. When UCC28610 is switching and deliver power to the load, its switching frequency and peak current are modulated based on FB pin current. The FB pin current is determined by the feedback loop design and output loading condition. During normal operation, the valley switching is
   (a) At heavy load, UCC28610 control the Flyback converter operate at constant peak current with frequency modulation mode (FM) to regulate output voltage.
   (b) In the medium to light load, the converter operate in fixed switching frequency with peak current modeulation mode (AM) to regulate the output voltage.
   (c) Once the load becomes too light, the converter operates in fixed frequency and fixed peak current mode. The output voltage is regulated through burst mode operation.
4. UCC28610 can be shut down under different conditions.
   (a) Once the VDD voltage drops below turn off threshold $VDD_{(OFF)}$, UCC28610 shuts down and returns to start up mode.
   (b) If MOT is pulled below 1V externally, UCC28610 shuts down and VDD recycles until MOT pin becomes above 1V to restart.
   (c) If the FB pin current is continuously below $I_{FB(OL)}$ for longer than t_{OL}, UCC28610 shuts down because of over load fault. Depending on the fault response setting, converter either latches off or tries to restart. This fault can be introduced by over load condition or input voltage becomes too low that system loses its capability to regulate output voltage.
   (d) When ZCD pin senses over voltage condition, UCC28610 shuts down. Depending on the fault response setting, UCC28610 enters latch off mode or tries to restart.
   (e) Once internal junction temperature is higher than T_{SD}, UCC28610 shuts down because of over temperature protection. Depending on the fault response setting, UCC28610 latches off or tries to restart after junction temperature drops below T_{SD}-T_{SD_HYS}.
5. Once UCC28610 latches off, VDD voltage needs to drop below $VDD_{(FAULT_RESET)}$ to release the latch. During fault reset, input voltage must be disconnected from the source to allow VDD voltage to drop.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Transformer Selection

To begin a power supply design, the power supply designer needs to know the peak power to be delivered by the converter, the input voltage range, the output voltage, and an estimate of the maximum allowable bulk voltage ripple. Select the maximum allowable stress voltage for the external power MOSFET. The stress voltage, V_{DS}, determines the reflected secondary voltage that resets the flyback transformer and the turn ratio between primary and secondary. A simplified diagram of the converter and its waveforms are shown in Figure 22.

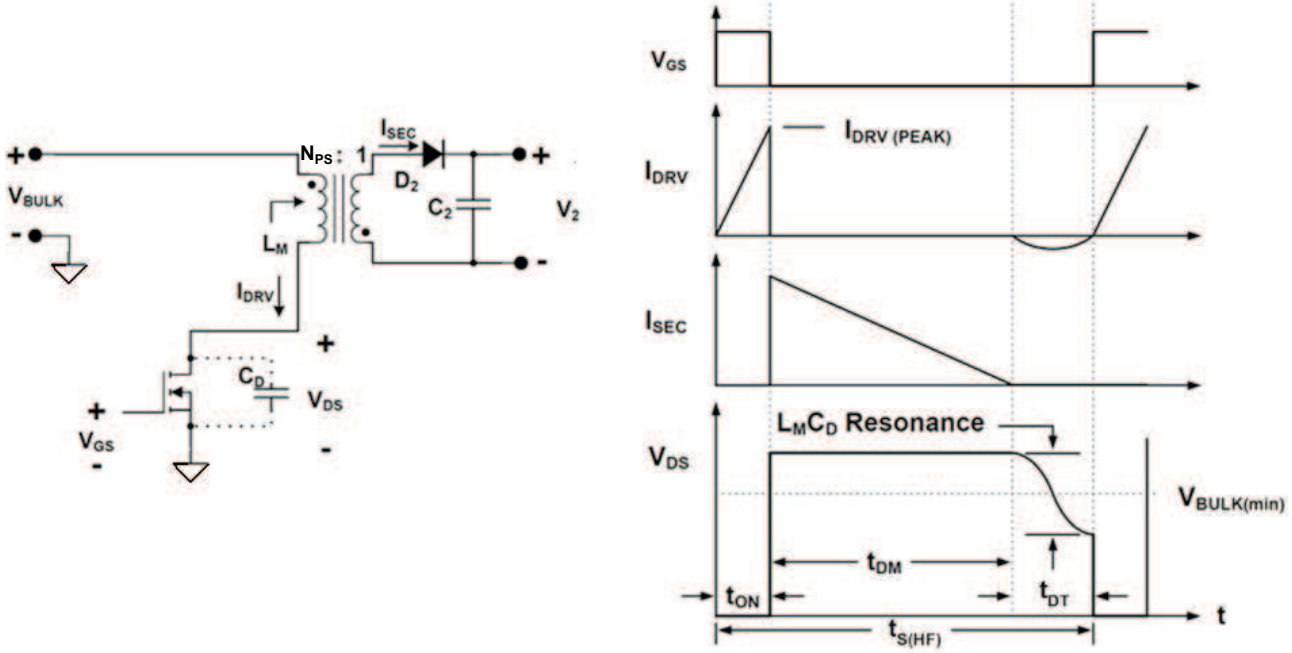

Figure 22. Basic Flyback Converter and Waveforms at Peak Load and Minimum V_{BULK} Voltage

Peak power is the maximum power level that must be regulated by the converter control system. Loads that last longer than the control loop time constant (100 μs - 300 μs) are directly considered "peak power". Loads lasting less than the control loop time constant can be averaged over the control loop time constant.

The minimum switching period is when the converter is operating in the Frequency Modulation (FM) mode, referred to as $t_{S(HF)}$. This switching period must equal the sum of the switching intervals at minimum input voltage, maximum load, as shown in Figure 22 and described in Equation 6. The switching intervals are t_{ON}, the conduction time of the MOSFET; t_{DM} the demagnetization time of the transformer and t_{DT}, the duration of the deadtime, equal to half of the resonant cycle, after the transformer is de-energized.

$$t_{S(HF)} = t_{ON} + t_{DM} + t_{DT} \tag{6}$$

Solve for the primary to secondary turn ratio, N_{PS}, using the maximum allowable V_{DS}, the maximum input line voltage, the predicted voltage spike due to leakage inductance and the desired regulated output voltage of the converter, V_{OUT}.

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Application Information (continued)

$$N_{PS} = \frac{V_{DS} - \sqrt{2}\, V_{IN(max)} - V_{leakage_spike}}{V_{OUT}} \quad (7)$$

Assume a deadtime, t_{DT}, of 5% of the total minimum switching period to allow for variations in the output capacitance of the HVMOSFET and the leakage inductance value:

$$t_{DT} = 0.05 \times t_{S(HF)} \quad (8)$$

Using volt-seconds balance, set the volt-seconds on equal to the volt-seconds for demagnetizing and solve for the on-time:

$$V_{BULK(min)} \times t_{ON} = V_{OUT} \times N_{PS} \times t_{DM} \quad (9)$$

$$t_{DM} = t_{S(HF)} - t_{ON} - t_{DT} \quad (10)$$

$$t_{ON} = \frac{V_{OUT} \times N_{PS} \times (t_{S(HF)} - t_{DT})}{V_{BULK(min)} + (V_{OUT} \times N_{PS})} \quad (11)$$

The maximum input power, P_{IN}, to the converter, in addition to being equal to the output power divided by the overall efficiency, is always equal to:

$$P_{IN} = \frac{P_{OUT}}{\text{efficiency}} = \frac{\left(V_{BULK(min)} \times t_{ON}\right)^2}{2 \times L_M \times t_{S(HF)}} \quad (12)$$

Solve for the primary inductance value:

$$L_M = \frac{\left(V_{BULK(min)} \times t_{ON}\right)^2}{2 \times P_{IN} \times t_{S(HF)}} \quad (13)$$

This equation is an approximation of the primary inductance value that is the best choice to minimize the primary side RMS current. In the actual circuit, when the resonance and delay due to leakage inductance can be measured, the magnetizing inductance value may need to be iterated for optimized low voltage switching.

Select the CL resistor, R_{CL}, based upon the maximum power constant of the controller, K_P, The tolerance of L_M should be considered (such as 10% lower for a typical inductor) and the minimum value of L_M should be used to calculate the value of the CL resistor.

To avoid tripping the overload protection feature of the controller during the normal operating range, use the minimum value of K_P from the Electrical Characteristics Table:

$$R_{CL} = 33.2\text{k}\Omega \times \sqrt{\frac{K_P \times L_M}{P_{IN}}} \quad (14)$$

Once R_{CL} is selected, the peak DRV current is calculated using Equation 10:

$$I_{DRV(PK)} = \frac{100\text{kV}}{R_{CL}} \quad (15)$$

For high efficiency, the bias winding turn ratio, N_{PB}, should be designed to maintain the VDD voltage above the VGG clamp, which is equal to $VGG_{(DISABLED)}$, when the converter is in burst mode. If VDD discharges below this value, minus the threshold voltage of the HVMOSFET, the HVMOSFET will turn on and linearly supply the VDD current from the high voltage rail instead of from the bias windings. Adding a zener diode on VDD will protect VDD from exceeding its absolute maximum rating in the event of a spike due to excess leakage inductance.

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Application Information (continued)

8.1.2 Cascode Bias and Start-Up

The UCC28610 uses a cascode drive and bias to control the high voltage power MOSFET and provide initial bias at start-up. Thus, the external high voltage power MOSFET provides the start-up function in addition to the power switching function during converter operation. The cascode architecture utilizes a low voltage switch operating between ground and the source of a high voltage MOSFET (HVMOSFET) configured in a common gate configuration, as shown in Figure 23. There are some key points to note.

1. The gate of the external HVMOSFET is held at a DC voltage.
2. The HVMOSFET is driven through the source, not the gate.
3. The entire primary winding current passes through the internal low voltage Driver MOSFET (both DRV and GND pins).

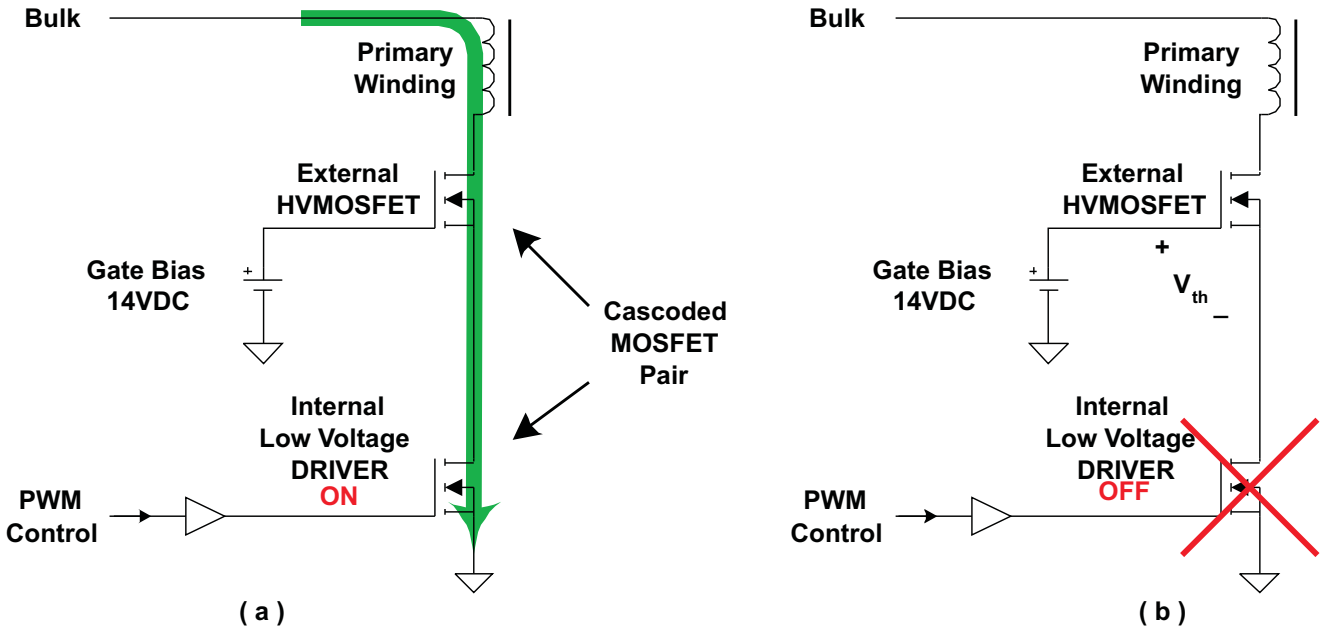

Figure 23. Cascoded Architecture

The UCC28610 integrates the low voltage switch in the form of a 90-mΩ FET along with all associated current sensing and drive. The HVMOSFET is forced to track the fast internal low voltage driver. The drain-gate charge in the HVMOSFET does not affect the turn-off speed because the gate is connected to a low impedance DC source. The cascode configuration results in very fast turn-off of the HVMOSFET, which keeps MOSFET switching losses low.

Cascode drive circuits are well known for high speed voltage gain. This topology can have small signal bandwidth over 100 MHz and it can exhibit high frequency ringing. High frequency ringing can cause EMI problems and become destructive in some situations. The sub-intervals during and immediately following the turn-on and turn-off transients are particularly susceptible to oscillation. For avoidance or solutions, see the application section, Solving High Frequency Ringing.

The cascode configuration permits a unique start-up sequence that is fast yet low-loss. Start-up bias uses a low level bleed current from either the AC line or the rectified and filtered AC line, or bulk voltage (via R_{START}) as shown in Figure 24. This current charges a small VGG capacitor, C_{VGG}, raising the HVMOSFET gate. The VGG pin will typically draw approximately 6 μA ($I_{VGG(SREG)}$) during this time, allowing the bulk bias current to be small and still charge the VGG capacitor. The HVMOSFET acts as a source follower once VGG reaches the threshold voltage of the HVMOSFET. Then, the HVMOSFET will bring up the DRV voltage as VGG continues to rise. During this time the UCC28610 is in UVLO and the Enable PWM signal is low. This turns on the VDD switch connecting VDD to DRV, allowing VDD to rise with the source of the HVMOSFET and charging C_{VDD}. An external Schottky diode, D1, is required between DRV and VDD. This diode passes potentially high switching currents that could otherwise flow through the body diode of the internal VDD Switch.

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Application Information (continued)

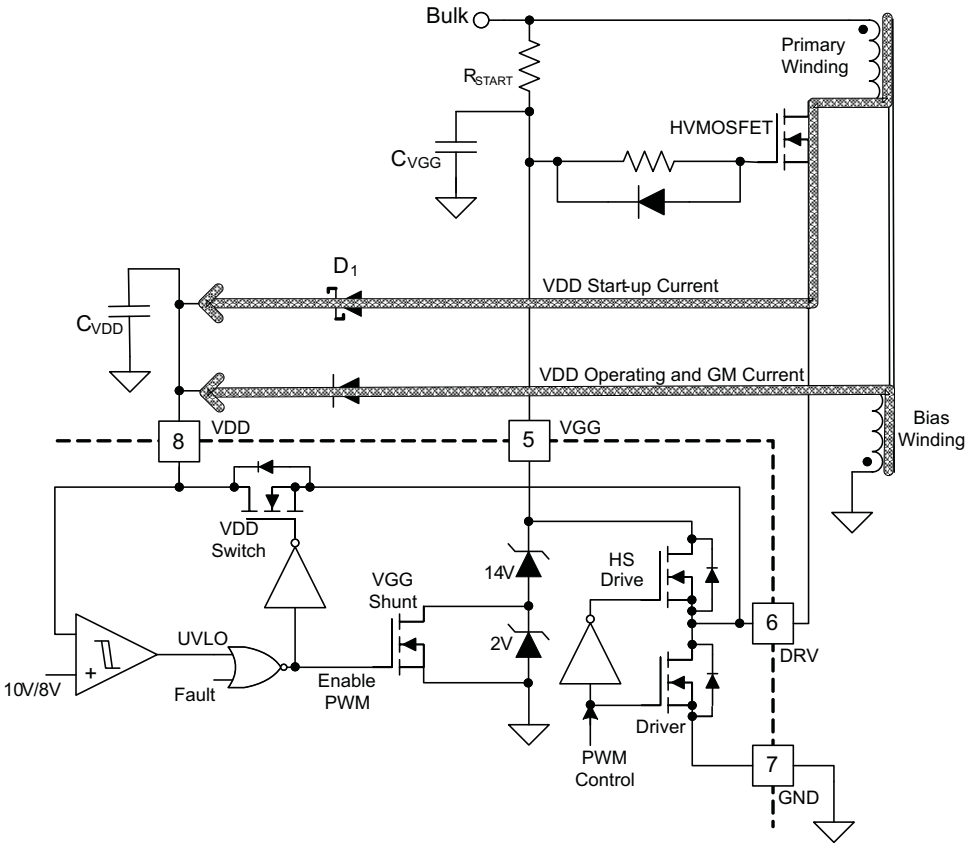

Figure 24. Start-Up Currents for the Cascode Architecture

In order to achieve the lowest possible no-load power, select the number of turns in the bias winding so that VDD is higher than 16 V – V_{TH} of the HVMOSFET. A bias winding voltage between 17 V and 20 V usually achieves minimum loss. The bias winding often tracks the primary leakage inductance turn-off voltage spike. Place a 20-V Zener diode between VDD and GND in applications where heavy loads cause excessive VDD voltage.

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Application Information (continued)

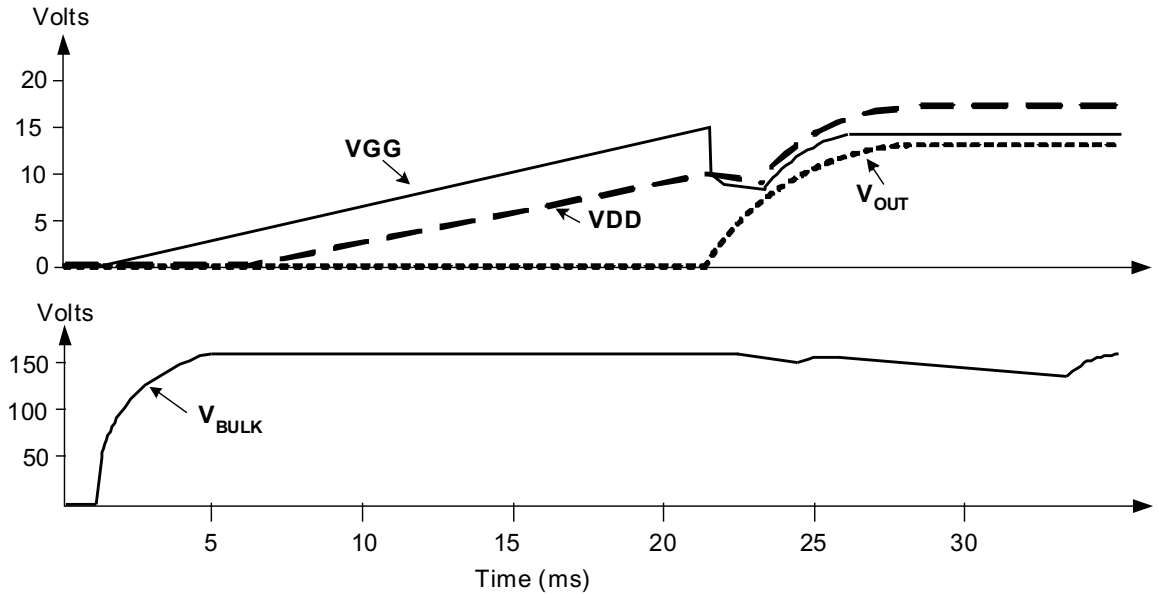

Figure 25. Typical Start-Up Waveforms for a 17-V Bias Winding Voltage

Typical start-up waveforms are shown in Figure 25. As VGG rises, VDD will follow, minus the threshold voltage of the HVMOSFET. When VDD reaches approximately 10 V, the UCC28610 initiates switching. The bias supply current, I_{VDD}, rises to its operating level and it is supplied from the VDD capacitor. Start-up times can be kept under 200 ms by selecting the VGG capacitor in the range of 33 nF to 1000 nF and selecting R_{START} to have a current of 15 μA at the minimum AC line voltage. Select capacitor C_{VDD} to have enough capacitance to provide operating bias current to the controller for the time it takes the auxiliary winding to take over. No-load burst operation may impose a requirement for additional C_{VDD} capacitance.

The voltage on VGG is shunt regulated to 16 V whenever the PWM action is disabled. This is reduced to 14 V during switching to limit voltage stress on the gate of the external HVMOSFET. The external HVMOSFET should have a threshold voltage of less than 6 V in order to permit proper starting.

8.1.3 Feedback Function

Modulation and modes are controlled by applying current to the FB pin. The FB pin is usually used to feed back the output error signal to the modulator. The UCC28610 uses internal current mirrors to apply the FB current to the Feedback Processing block, and then to the Frequency Modulator and Current Modulator blocks. The voltage of the FB pin is a constant 0.7 V. AC filtering of the output of the opto-coupler must be applied at the FB pin, as shown in Figure 26. The corner frequency of the filter in Figure 26 should be at least a decade above the maximum switching frequency of the converter, as given in Equation 16. A 100-kΩ resistor, R_{FB}, between the opto-coupler emitter and GND prevents ground noise from resetting the overload timer by biasing the FB pin with a negative current. An opto-coupler with a low Current Transfer Ratio (CTR) is required to give better no-load performance than a high CTR device due to the bias current of the secondary reference. The low CTR also offers better noise immunity than a high CTR device.

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Application Information (continued)

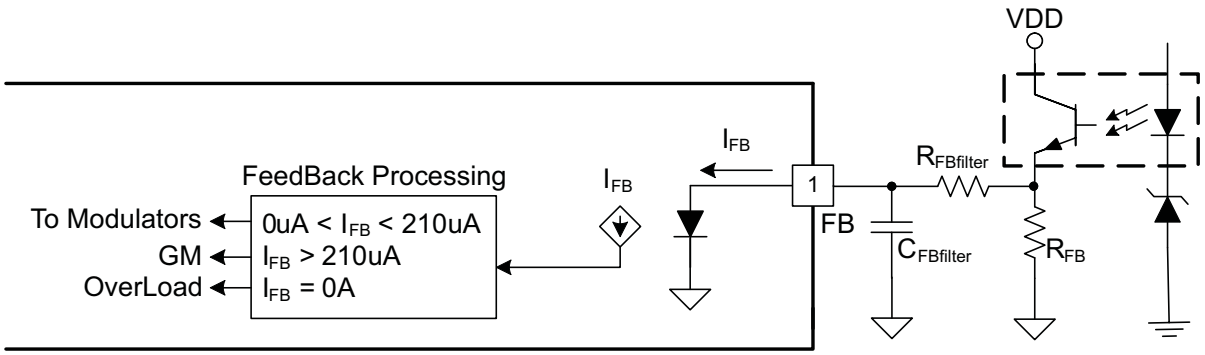

Figure 26. FB Details

$$f_{FB} = \frac{1}{2 \times \pi \times R_{FBfilter} \times C_{FBfilter}} \tag{16}$$

8.1.4 Modulation Modes

Under normal operating conditions, the FB current commands the operating mode of the UCC28610, as shown in Figure 27 and Figure 28. The FB current commands the UCC28610 to operate the converter in one of three modes: Frequency Modulation (FM) mode, Amplitude Modulation (AM) mode, and Green Mode (GM).

The converter operates in FM mode with a large power load (22% to 100% the peak regulated power). The peak HVMOSFET current reaches its maximum programmed value and FB current regulates the output voltage by varying the switching frequency, which is inversely proportional to t_S. The switching frequency is modulated from 30 kHz (22% peak power) to 133 kHz (100% peak power), the on time is constant, and the I_{DRV} peak current is constant. The maximum programmable HVMOSFET current, $I_{DRV,PK(max)}$, is set by a resistor on the CL pin, as described in Equation 15.

The converter operates in AM mode at moderate power levels (2.5% to 22% of the peak regulated power). The FB current regulates the output voltage by modulating the amplitude of the peak HVMOSFET current from 33% to 100% of the maximum programmed value while the switching frequency is fixed at approximately 30 kHz. The UCC28610 modulates the voltage on the CL pin from 3 V to 1 V to vary the commanded peak current, as shown in Figure 27 and Figure 28.

The converter operates in GM at light load (0% to 2.5% of the peak regulated power). The FB current regulates the output voltage in the Green Mode with hysteretic bursts of pulses using FB current thresholds. The peak HVMOSFET current is 33% of the maximum programmed value. The switching frequency within a burst of pulses is approximately 30 kHz. The duration between bursts is regulated by the power supply control dynamics and the FB hysteresis. The UCC28610 reduces internal bias power between bursts in order to conserve energy during light-load and no-load conditions.

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Application Information (continued)

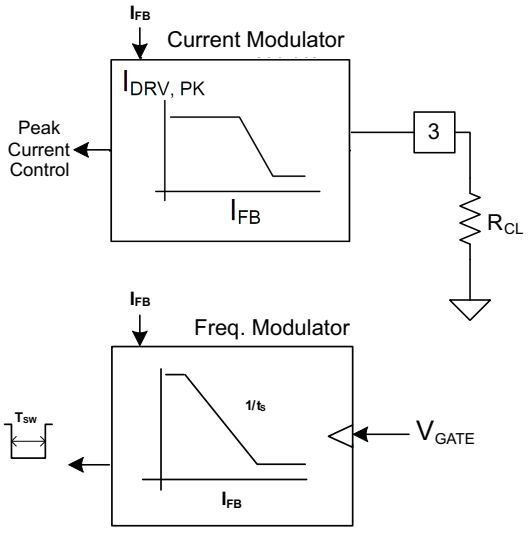

Figure 27. Modulation Control Blocks

Application Information (continued)

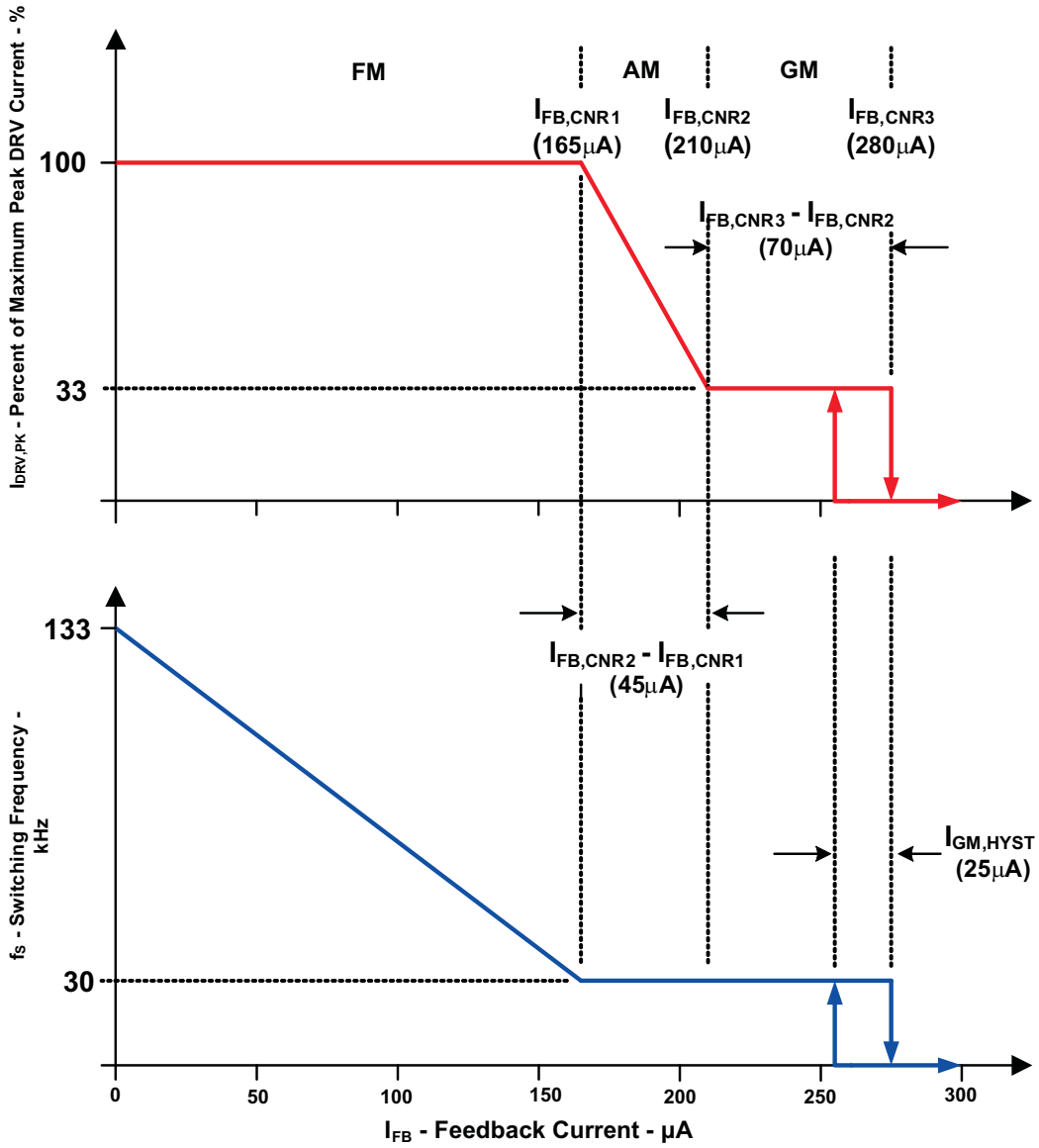

Figure 28. Control Diagram with Operating Modes

8.1.5 Primary Current Sense

The UCC28610 uses a current mirror technique to sense primary current in the Current Modulator. See Figure 29 for details. All of the primary current passes into the DRV pin, through the Driver MOSFET and out of the GND pin. The Driver MOSFET current is scaled and reflected to the PWM Comparator where it is compared with the CL current. At the beginning of each switching cycle a blanking pulse, $t_{BLANK,(Ilim)}$, of approximately 220 ns is applied to the internal current limiter to allow the driver to turn on without false limiting on the leading edge capacitive discharge currents normally present in the circuit.

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Application Information (continued)

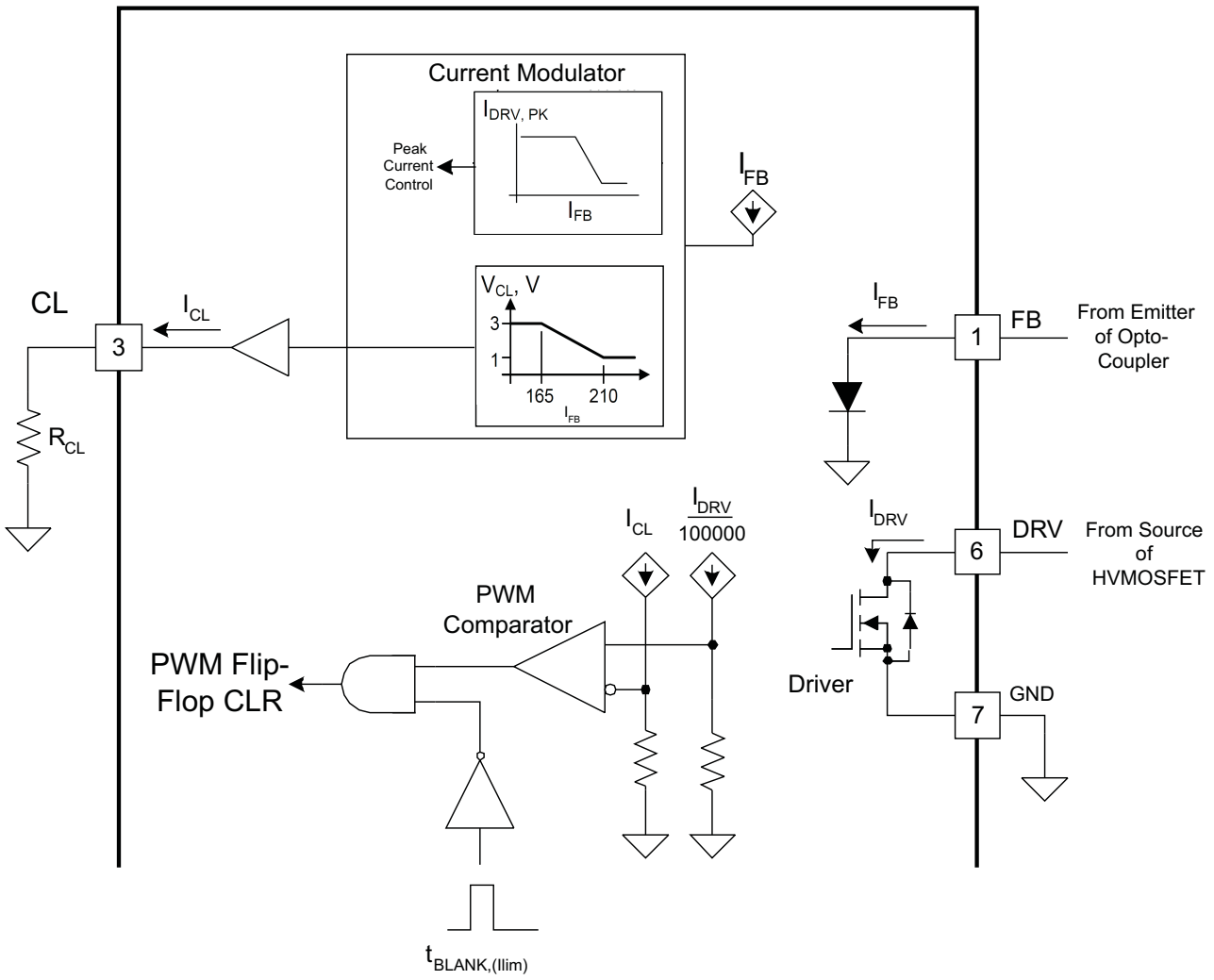

Figure 29. CL pin and DRV Current Sense

8.1.6 Zero Crossing Detection

The modulator requires three conditions in order to initiate the next switching cycle:

1. The time since the last turn-on edge must be equal to or greater than the time that is requested by the Feedback Processor as determined by the feedback current, I_{FB}.
2. The time since the last turn-on edge must be longer than the minimum period that is built into the UCC28610 (nominally 7.5 μs which equals 133 kHz).
3. Immediately following a high-to-low zero crossing of the ZCD voltage. Or, it has been longer than $t_{WAIT,ZCD}$ (~2.4 μs) since the last zero crossing has been detected.

Every switching cycle is preceded by at least one zero crossing detection by the ZCD pin. The modulator allows the resonant ring to damp between pulses if the period needs to exceed the damping limit, allowing long pauses between pulses during no-load operation.

The switching frequency is not allowed to exceed 133 kHz (nominally). This sets the maximum power limit so that it will be constant for all bulk voltages that exceed the minimum line voltage value.

Figure 30 illustrates a set of switching cycle waveforms over a range of operating conditions. The UCC28610 is designed to always keep the inductor current discontinuous. This prevents current tailing during start-up or short circuit conditions and accommodates control of the maximum power delivered.

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Application Information (continued)

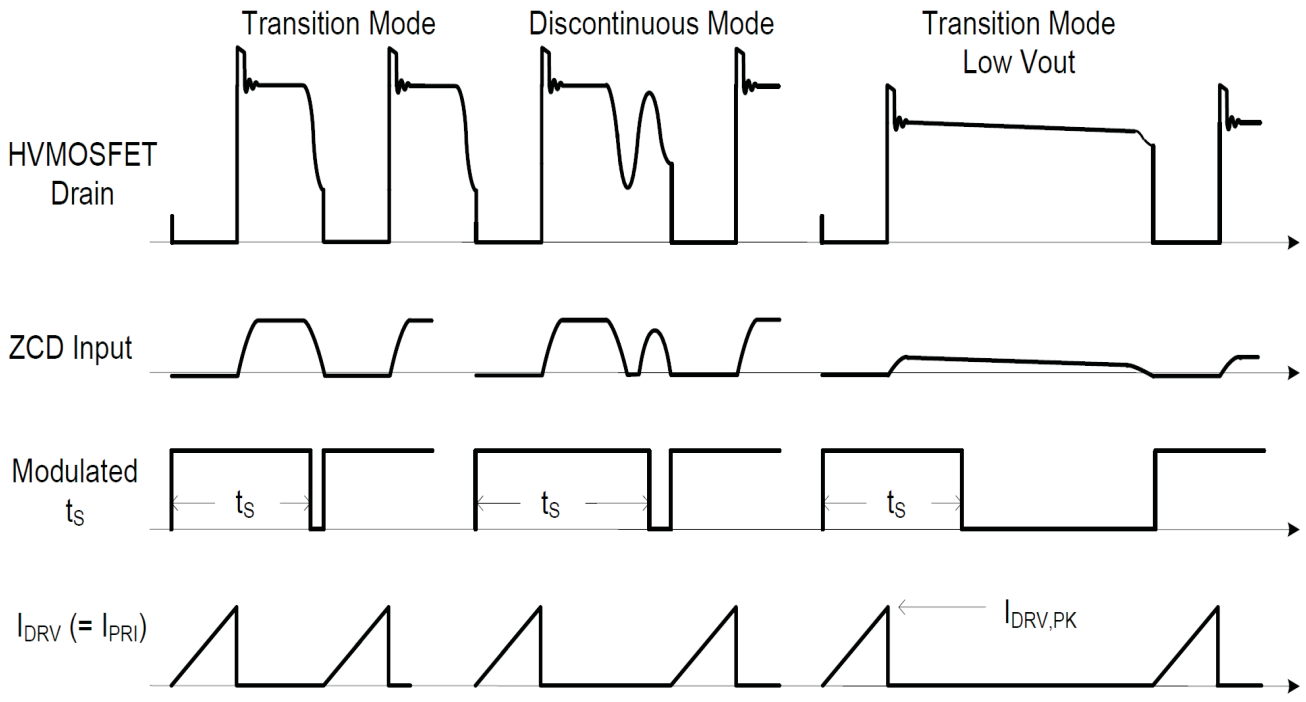

Figure 30. Switching Cycle Waveforms

Zero crossing is detected using a resistive divider across the bias winding, as shown in Figure 31. The bias winding operates in phase with the output winding. The ZCD function detects transformer demagnetization when the ZCD voltage has a high to low crossing of the 20-mV ZCD threshold, ZCD_{TH}. The voltage at the ZCD pin is internally clamped to contain negative excursions at -160mV (ZCD_{CLAMP}). A small delay, 50 ns to 200 ns, can be added with C_{ZCD} to align the turn-on of the primary switch with the resonant valley of the primary winding waveform.

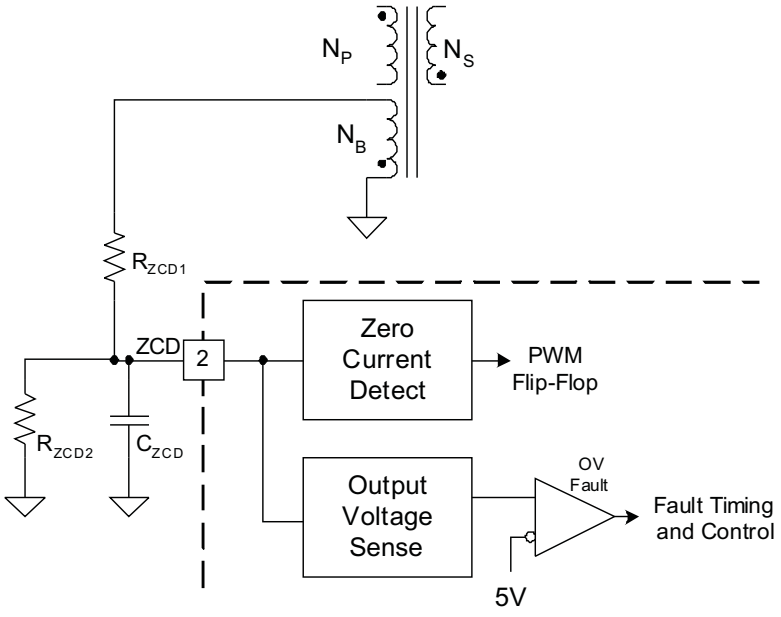

Figure 31. Zero Crossing Detection

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Application Information (continued)

$$R_{ZCD1} = \frac{V_{OUT} + V_F}{100\mu A} \times \frac{N_B}{N_S} \quad (17)$$

$$R_{ZCD2} = \frac{ZCD_{(ovp)} \times R_{ZCD1}}{\left(V_{OUT(pk)} \times \frac{N_B}{N_S}\right) - ZCD_{(ovp)}} \quad (18)$$

8.1.7 Green Mode Operation

During light load operation the UCC28610 cycles between two states: GM-on and GM-off. The details are shown in Figure 32. During the GM-on state, the controller is active while the modulator issues a burst of one or more pulses. During the GM-off state the controller reduces its operating current and switching action is inhibited. The rate and duration of the on and off states are controlled by the current into the FB pin as it cycles between the two hysteretic thresholds separated by $I_{FB,\ GM_HYST}$, the load current, the output filter capacitor, and the details of the feedback circuit.

During the GM-off state the VDD supply current is reduced to approximately 550 μA, $I_{VDD(GM)}$. The Enable PWM signal goes low which inhibits switching, sets the VGG shunt regulation to ~16 V, $VGG_{(DISABLED)}$, and turns on the VDD switch. The VGG node quickly charges to 16V and the low VDD current is supplied from the VDD capacitor.

During the GM-on state the UCC28610 controls the peak primary current to 33% of $I_{DRV,PK(max)}$, at a 30-kHz rate. When switching, the VGG shunt regulator pulls the VGG voltage down to ~14 V. VDD is charged by the auxiliary winding during this time as long as VDD does not discharge below 14 V. The converter's output voltage is charged until the feedback network forces the FB current to the GM off threshold, $I_{FB,CNR3}$, and puts the controller back into the GM off state.

At very light loads the time between PWM bursts can be long. To obtain the lowest no-load power, it is important that VDD not discharge below 16 V by more than the threshold voltage of the HVMOSFET or the HVMOSFET will turn-on and linearly supply the VDD current from the high-voltage bulk rail. The VDD voltage can be extended by increasing the C_{VDD} capacitance without significant impact on start-up time.

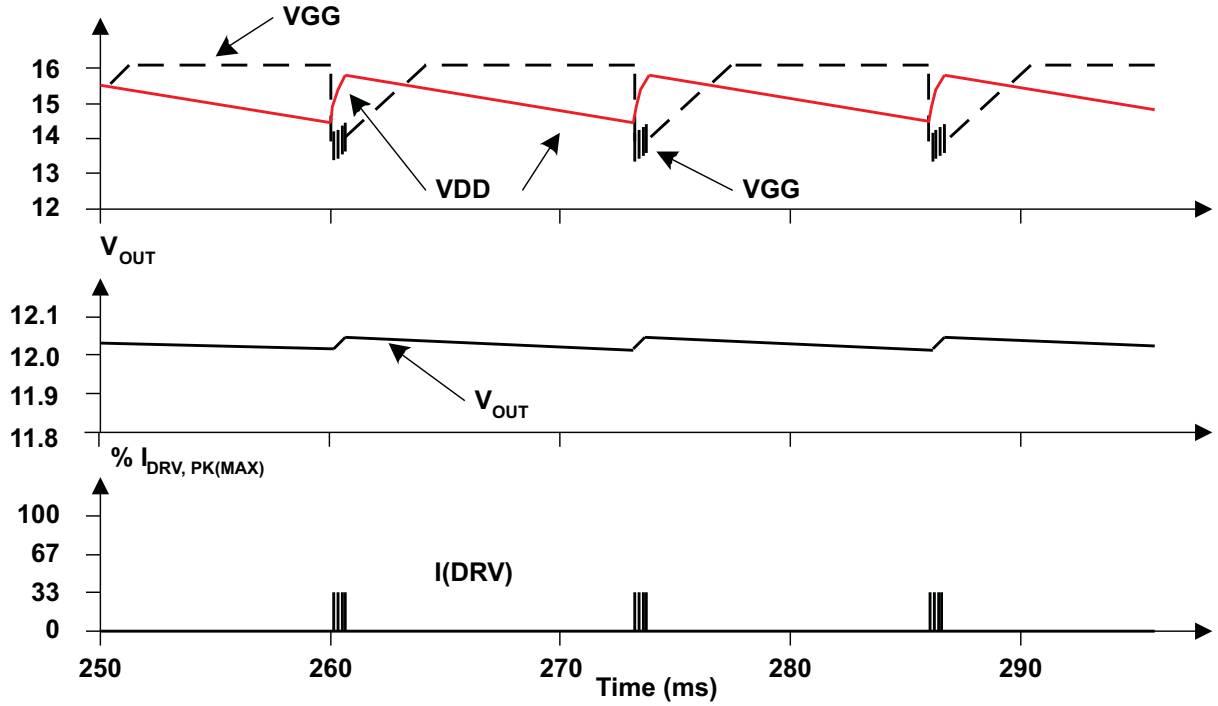

Figure 32. Green Mode Operation

Application Information (continued)

8.1.8 Maximum Converter Power Limitation

The suggested peak power range of the UCC28610 is 12 W to 65 W based on a universal AC line converter (90-VAC to 265-VAC input line voltage), using an external high voltage MOSFET with a voltage rating of 600 V. This power range may depend on application and external MOSFET stress voltage. Ultimately, the peak primary current is the limiting factor because this current must pass through the UCC28610. The limit on the peak primary current imposes a limit on the peak primary power. The peak power must be less than 65 W, not the average power. The peak power is defined as the highest power level where the controller must maintain regulation.

At all power levels, program the UCC28610 to control the power limit with the primary inductance, peak current and maximum switching frequency (133 kHz). The maximum peak input power level is given by Equation 19. The accuracy of the power limit is twice as sensitive to $I_{DRV(PK)}$ errors than L_M errors and $f_{S(max)}$ errors. If the load demands more power than the programmed level, the power supply output voltage sags and the overload timer is initiated.

$$P_{IN(max)} = \frac{L_m \times I_{DRV(pk)}^2 \times f_{S(max)}}{2} \tag{19}$$

8.1.9 Minimum Converter Power Limitation

The dynamics of the DRV current sense imposes the 12-W minimum power level limit for this controller. The power level limits are found from DRV current estimates for typical universal AC adapters that use a 600-V MOSFET. The power range and its associated peak current range are given in Equation 20.

$$P_{IN} \geq 12W$$
$$I_{DRV,PK(min)} \geq 1A \tag{20}$$

The minimum power level is due to a loss of linearity of the current mirror, as shown in Figure 33. A programmed $I_{DRV,PK}$ level between 0.66 A and 1 A (by using 100 kΩ ≤ R_{CL} ≤ 150 kΩ) allows only a 2:1 amplitude modulation range of the peak DRV current. The amplitude of I_{DRV} modulates linearly if $I_{DRV,PK}$ is programmed within its recommended operating range (1.0 A < $I_{DRV,PK}$ < 4.1 A, corresponding to 100 kΩ > R_{CL} > 24.3 kΩ respectively.

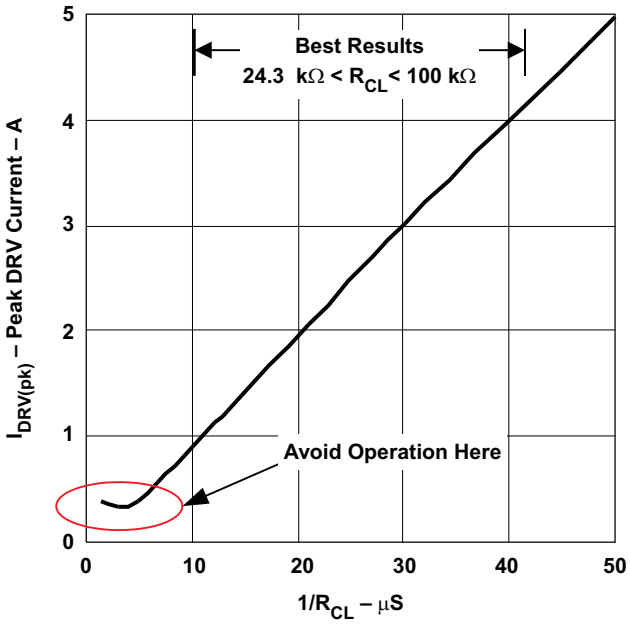

Figure 33. Dynamic Operating Range

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8.2 Typical Application

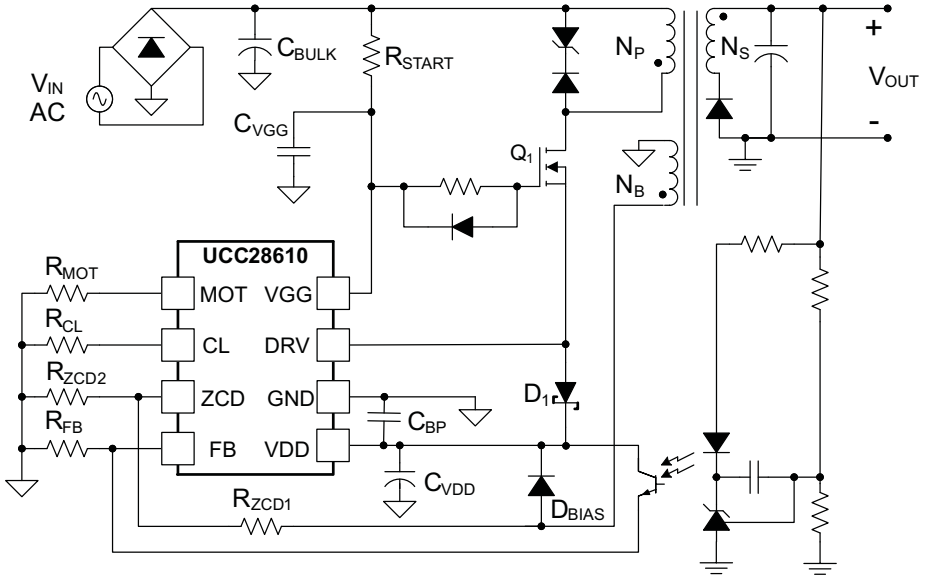

Figure 34. Recommended Operating Conditions Application

8.2.1 Design Requirements

Table 1 illustrates a typical subset of high-level design requirements. Many of these parameter values are used in the design equations contained in Table 2.

Table 1. UCC28610EVM-474 Electrical Performance Specifications

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		85		265	VRMS
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage	V_{IN} = min to max, I_{OUT} = min to max	10.8	12	13.2	V
V_{ripple}	Output voltage ripple	V_{IN} = 115 V_{RMS}, I_{OUT} = max		80	120	mVpp
I_{OUT}	Output current	V_{IN} = min to max	0		2.1	A
I_{OCP}	Output over current inception point	V_{IN} = max		3		A
V_{OVP}	Output OVP	I_{OUT} = min to max			16	V
	Transient response voltage over shoot	I_{OUT} = min to max		500		mV
SYSTEM CHARACTERISTICS						
h_{PEAK}	Peak efficiency	V_{IN} = 115 V_{RMS}, I_{OUT} = 1.05 A		85.7%		
	No load power consumption	V_{IN} = 115 V_{RMS}		67		mW
		V_{IN} = 230 V_{RMS}		107		

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For reference designators refer to Figure 34.

8.2.2 Detailed Design Procedure

Table 2. Pin Components(1)(2)

NAME	PIN	DESCRIPTION
CL	3	$R_{CL} = 33.2k\Omega \times \sqrt{\frac{K_P \times L_M}{P_{IN}}}$ $I_{DRV(PK)} = \frac{100\ kV}{R_{CL}}$ Where K_P = 0.54W/ μH L_M is the minimum value of the primary inductance $P_{IN} = P_{OUT}/\eta$ η = efficiency
DRV	6	Q_1, power MOSFET with adequate voltage and current ratings, V_{VGS} must have at least 20-V static rating.
		D_1, Schottky diode, rated for at least 30 V, placed between DRV and VDD
FB	1	R_{FB} = 100 kΩ
GND	7	Bypass capacitor to VDD, C_{BP} = 0.1-μF, ceramic
MOT	4	For latch-off response to overcurrent faults: t_{MOT} = user programmable maximum on-time after 250-ms delay. $R_{MOT} = t_{MOT} \times \left(1 \times 10^{11}\ \frac{\Omega}{s}\right)$ where • 150 kΩ ≤ R_{MOT} ≤ 500 kΩ For shutdown-retry response to overcurrent faults: $R_{MOT} = t_{MOT} \times \left(2 \times 10^{10}\ \frac{\Omega}{s}\right)$ • 25 kΩ ≤ R_{MOT} ≤ 100 kΩ and t_{MOT} ≤ 5 μs
VDD	8	$C_{VDD} = \frac{I_{VDD(GM)} \times t_{BURST}}{\Delta VDD_{(BURST)}}$ where: $\Delta VDD_{(BURST)}$ is the allowed VDD ripple during burst operation t_{BURST} is the estimated burst period, The typical C_{VDD} value is approximately 47 μF D_{BIAS} must have a voltage rating greater than: $V_{DBIAS} \geq V_{OUT} \frac{N_{PS}}{N_{PB}} + \frac{V_{BULK(max)}}{N_{PB}}$ where: V_{DBIAS} is the reverse voltage rating of diode D_2 $V_{BULK(max)}$ is the maximum rectified voltage of C_{BULK} at the highest line voltage

(1) Refer to the *Electrical Characteristics* table for all constants and measured values, unless otherwise noted.
(2) Refer to Figure 34 for all component locations in the Table 2.

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Table 2. Pin Components(1)(2) (continued)

NAME	PIN	DESCRIPTION
VGG	5	minimize the length of the C_{VGG} connection to GND C_{VGG} = at least 10x C_{GS} of HVMOSFET, usually C_{VGG} = 0.1 µF.
ZCD	2	$R_{ZCD1} = \frac{V_{OUT} + V_F}{100\ \mu A} \times \frac{N_{PS}}{N_{PB}}$ $R_{ZCD2} = \frac{ZCD_{(ovp)} \times R_{ZCD1}}{\left(V_{OUT(pk)} \times \frac{N_{PS}}{N_{PB}}\right) - ZCD_{(ovp)}}$
		where: $ZCD_{(ovp)}$ is the overvoltage fault threshold at ZCD N_{PS} is the primary to secondary turns ratio N_{PB} is the primary to bias turns ratio V_{OUT} is the average output voltage of the secondary V_F is the forward bias voltage of the secondary rectifier $V_{OUT,PEAK}$ is the desired output overvoltage fault level

8.2.2.1 Input Bulk Capacitance and Minimum Bulk Voltage

Bulk capacitance may consist of one or more capacitors connected in parallel. The input power of the converter based on target full-load efficiency, minimum input RMS voltage, minimum AC input frequency, and minimum bulk capacitor voltage are used to determine the bulk capacitor value. Maximum input power is used in the C_{BULK} calculation and is determined by:

$$P_{in(max)} = \frac{V_{OUT} \times I_{OUT}}{\eta} \tag{21}$$

Assume 30% voltage ripple on the bulk capacitor, the minimum bulk capacitor voltage is 70% of the minimum input AC voltage at its peak value.

$$V_{BULK(min)} = 0.7 \times \sqrt{2} \times V_{in(min)} \tag{22}$$

Equation 23 provides an accurate solution for input capacitance needed to achieve a minimum bulk valley voltage target $V_{BULK(min)}$, accounting for hold-up during any loss of AC power for a certain number of half cycles, N_{HC}, by an AC-line drop-out condition. Alternatively, if a given input capacitance value is prescribed, iterate the $V_{BULK(min)}$ value until that target capacitance is obtained, which determines the $V_{BULK(min)}$ expected for that capacitance.

$$C_{BULK} \geq \frac{2P_{in(max)} \times \left(0.25 + 0.5N_{HC} + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{in(min)}}\right)\right)}{(2V^2_{IN(min)} - V^2_{BULK(min)}) \times f_{LINE(min)}} \tag{23}$$

8.2.2.2 Transformer Selection

To begin a power supply design, the power supply designer needs to know the peak power to be delivered by the converter, the input voltage range, the output voltage, and an estimate of the maximum allowable bulk voltage ripple. Select the maximum allowable stress voltage for the external power MOSFET. The stress voltage, V_{DS}, determines the reflected secondary voltage that resets the flyback transformer and the turn ratio between primary and secondary. A simplified diagram of the converter and its waveforms are shown in Figure 22.

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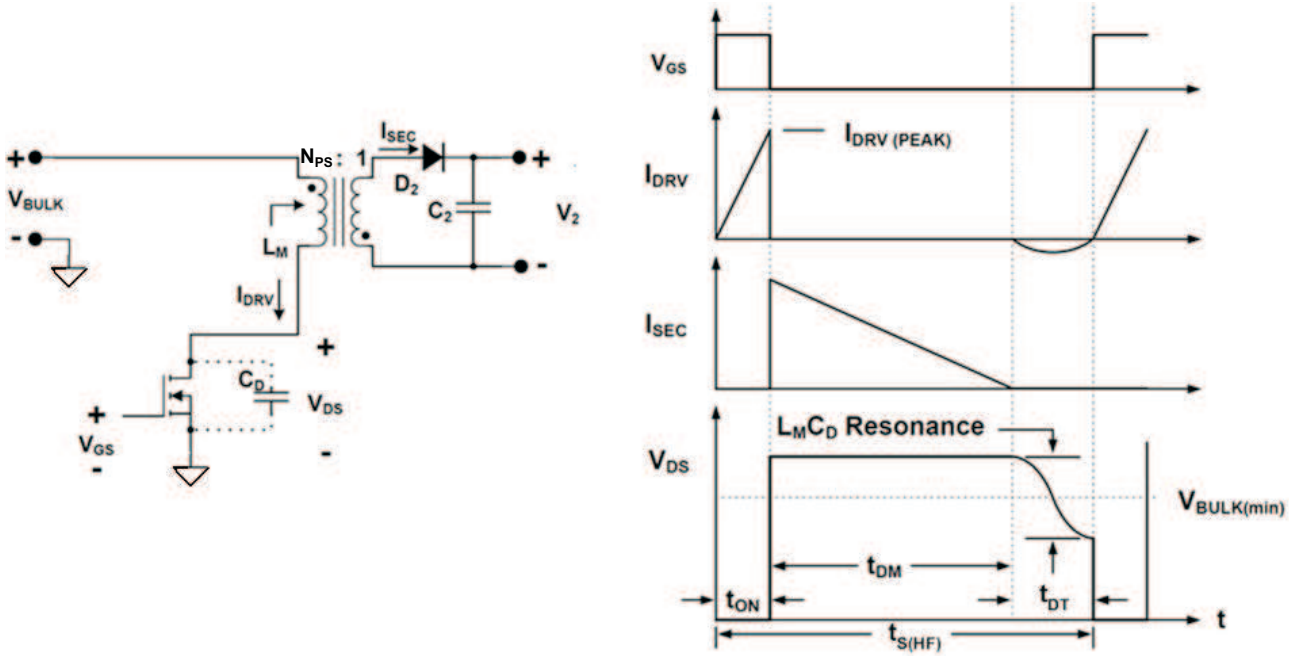

Figure 35. Basic Flyback Converter and Waveforms at Peak Load and Minimum V_{BULK} Voltage

Peak power is the maximum power level that must be regulated by the converter control system. Loads that last longer than the control loop time constant (100 μs - 300 μs) are directly considered “peak power”. Loads lasting less than the control loop time constant can be averaged over the control loop time constant.

The minimum switching period is when the converter is operating in the Frequency Modulation (FM) mode, referred to as $t_{S(HF)}$. This switching period must equal the sum of the switching intervals at minimum input voltage, maximum load, as shown in Figure 35 and described in Equation 24. The switching intervals are t_{ON}, the conduction time of the MOSFET; t_{DM} the demagnetization time of the transformer and t_{DT}, the duration of the deadtime, equal to half of the resonant cycle, after the transformer is de-energized.

$$t_{S(HF)} = t_{ON} + t_{DM} + t_{DT} \tag{24}$$

Solve for the primary to secondary turn ratio, N_{PS}, using the maximum allowable V_{DS}, the maximum input line voltage, the predicted voltage spike due to leakage inductance and the desired regulated output voltage of the converter, V_{OUT}.

$$N_{PS} = \frac{V_{DS} - \sqrt{2}\, V_{IN(max)} - V_{leakage_spike}}{V_{OUT}} \tag{25}$$

Assume a deadtime, t_{DT}, of 5% of the total minimum switching period to allow for variations in the output capacitance of the HVMOSFET and the leakage inductance value:

$$t_{DT} = 0.05 \times t_{S(HF)} \tag{26}$$

Using volt-seconds balance, set the volt-seconds on equal to the volt-seconds for demagnetizing and solve for the on-time:

$$V_{BULK(min)} \times t_{ON} = V_{OUT} \times N_{PS} \times t_{DM} \tag{27}$$

$$t_{DM} = t_{S(HF)} - t_{ON} - t_{DT} \tag{28}$$

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$$t_{ON} = \frac{V_{OUT} \times N_{PS} \times (t_{S(HF)} - t_{DT})}{V_{BULK(min)} + (V_{OUT} \times N_{PS})} \quad (29)$$

The maximum input power, P_{IN}, to the converter, in addition to being equal to the output power divided by the overall efficiency, is always equal to:

$$P_{IN} = \frac{P_{OUT}}{\text{efficiency}} = \frac{\left(V_{BULK(min)} \times t_{ON}\right)^2}{2 \times L_M \times t_{S(HF)}} \quad (30)$$

Solve for the primary inductance value:

$$L_M = \frac{\left(V_{BULK(min)} \times t_{ON}\right)^2}{2 \times P_{IN} \times t_{S(HF)}} \quad (31)$$

This equation is an approximation of the primary inductance value that is the best choice to minimize the primary side RMS current. In the actual circuit, when the resonance and delay due to leakage inductance can be measured, the magnetizing inductance value may need to be iterated for optimized low voltage switching.

Select the CL resistor, R_{CL}, based upon the maximum power constant of the controller, K_P, The tolerance of L_M should be considered (such as 10% lower for a typical inductor) and the minimum value of L_M should be used to calculate the value of the CL resistor.

To avoid tripping the overload protection feature of the controller during the normal operating range, use the minimum value of K_P from the Electrical Characteristics Table:

$$R_{CL} = 33.2k\Omega \times \sqrt{\frac{K_P \times L_M}{P_{IN}}} \quad (32)$$

Once R_{CL} is selected, the peak DRV current is calculated using Equation 10:

$$I_{DRV(PK)} = \frac{100kV}{R_{CL}} \quad (33)$$

For high efficiency, the bias winding turn ratio, N_{PB}, should be designed to maintain the VDD voltage above the VGG clamp, which is equal to $VGG_{(DISABLED)}$, when the converter is in burst mode. If VDD discharges below this value, minus the threshold voltage of the HVMOSFET, the HVMOSFET will turn on and linearly supply the VDD current from the high voltage rail instead of from the bias windings. Adding a zener diode on VDD will protect VDD from exceeding its absolute maximum rating in the event of a spike due to excess leakage inductance.

8.2.2.3 Feedback Function

Modulation and modes are controlled by applying current to the FB pin. The FB pin is usually used to feed back the output error signal to the modulator. The UCC28610 uses internal current mirrors to apply the FB current to the Feedback Processing block, and then to the Frequency Modulator and Current Modulator blocks. The voltage of the FB pin is a constant 0.7 V. AC filtering of the output of the opto-coupler must be applied at the FB pin, as shown in Figure 36. The corner frequency of the filter in Figure 36 should be at least a decade above the maximum switching frequency of the converter, as given in Equation 34. A 100-kΩ resistor, R_{FB}, between the opto-coupler emitter and GND prevents ground noise from resetting the overload timer by biasing the FB pin with a negative current. An opto-coupler with a low Current Transfer Ratio (CTR) is required to give better no-load performance than a high CTR device due to the bias current of the secondary reference. The low CTR also offers better noise immunity than a high CTR device.

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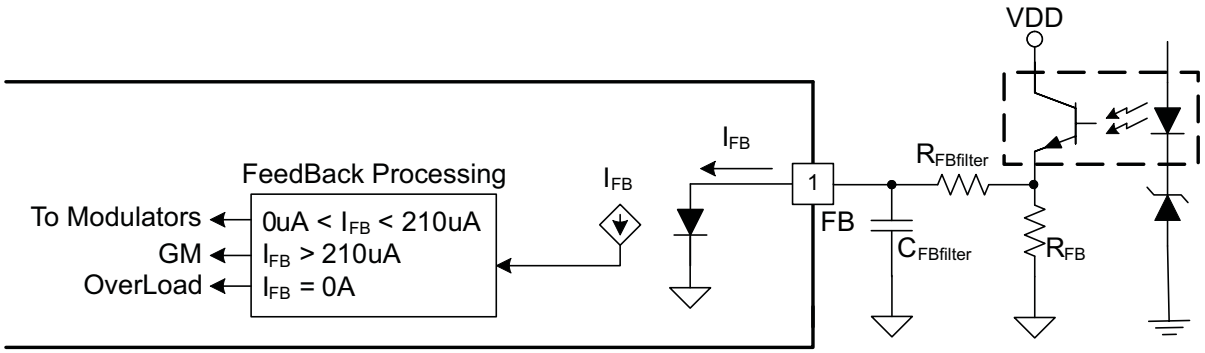

Figure 36. FB Details

$$f_{FB} = \frac{1}{2 \times \pi \times R_{FBfilter} \times C_{FBfilter}} \tag{34}$$

Zero crossing is detected using a resistive divider across the bias winding, as shown in Figure 37. The bias winding operates in phase with the output winding. The ZCD function detects transformer demagnetization when the ZCD voltage has a high to low crossing of the 20-mV ZCD threshold, ZCD_{TH}. The voltage at the ZCD pin is internally clamped to contain negative excursions at -160mV (ZCD_{CLAMP}). A small delay, 50 ns to 200 ns, can be added with C_{ZCD} to align the turn-on of the primary switch with the resonant valley of the primary winding waveform.

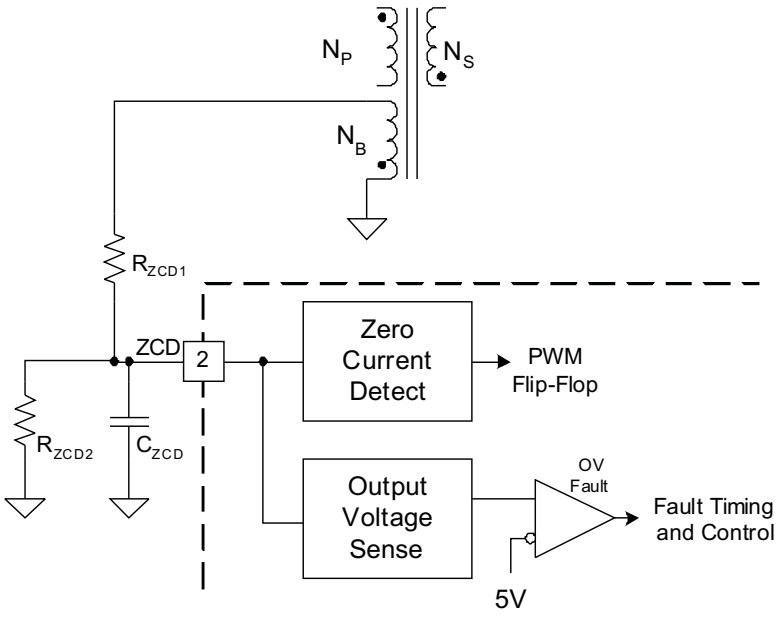

Figure 37. Zero Crossing Detection

$$R_{ZCD1} = \frac{V_{OUT} + V_F}{100\mu A} \times \frac{N_B}{N_S} \tag{35}$$

$$R_{ZCD2} = \frac{ZCD_{(ovp)} \times R_{ZCD1}}{\left(V_{OUT(pk)} \times \frac{N_B}{N_S}\right) - ZCD_{(ovp)}} \tag{36}$$

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8.2.3 Application Curves

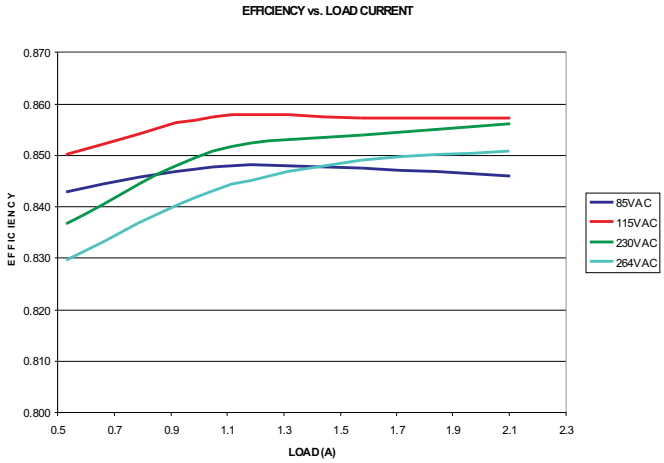


Figure 38. Efficiency as a Function of Load Current and Input Voltage

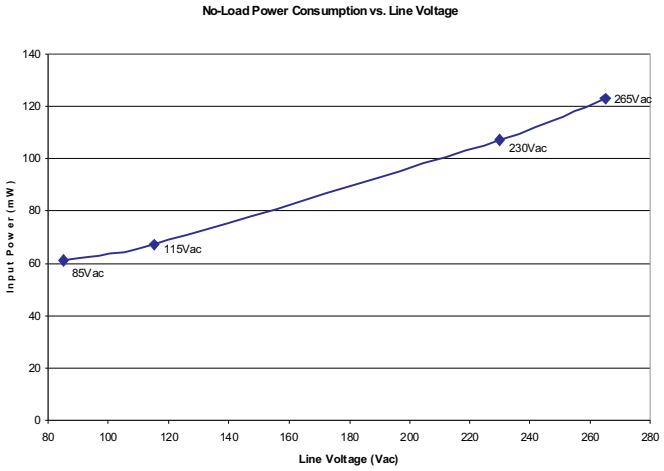
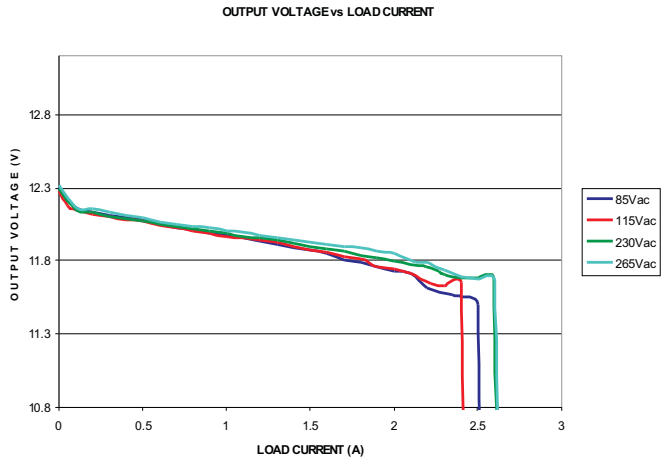
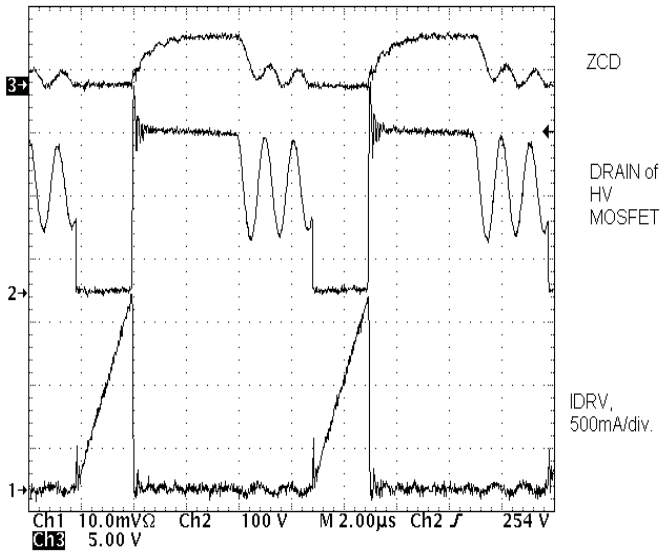


Figure 39. No-Load Input Power as a Function of Input Voltage



Note the Shutdown/Retry Threshold for Each Line Voltage

Figure 40. Output Voltage as a Function of Load Current and Line Voltage



Input voltage = V_{AC}, Full Load, f_{SW} = 112 kHz. Ch.1 = I_{DRV}, 500 mA/div., I_{DRV} = 1.53 A, Ch. 2 = Drain of HV MOSFET, 100 V/div., Ch.3 = ZCD, 5V/div.

Figure 41. FM Mode Switching Cycle Waveform

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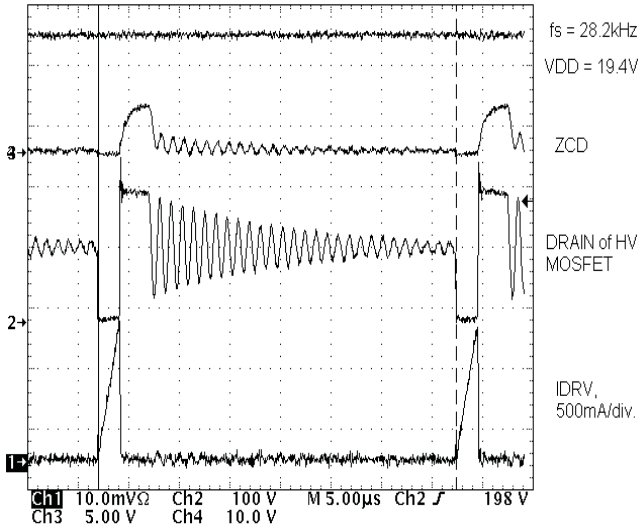

(Input voltage = 85 V_{AC} , 0.3-A load, f_{SW} = 28.2 kHz, Ch.1 = I_{DRV}, 500 mA/div., I_{DRV} = 1.1 A, Ch.2 = Drain of HV MOSFET, 100 V/div., Ch.3 = ZCD, 5 V/div., Ch. 4 = VDD, 10 V/div.)

Figure 42. AM Mode Switching Cycle Waveform

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9 Power Supply Recommendations

The UCC28610 VDD can be charged through high-voltage MOSFET directly from the high-voltage bus at startup. Due to the nature of high loss, this charging path is intended for startup operation only. During normal operation, the VDD voltage should be high enough to avoid this high-loss charging path.

In order to achieve the lowest possible no-load power, select the number of turns in the bias winding so that VDD is higher than 16V-V_{TH} of the high voltage MOSFET. A bias winding voltage between 17 V and 20 V usually achieves minimum loss. The bias winding often tracks the primary leakage inductance turn-off voltage spike. Place a 20-V Zener diode between VDD and GND in applications where the heavy loads cause excessive VDD voltage.

10 Layout

10.1 Layout Guidelines

It is possible to design a power supply on a single layer board using the UCC28610. Figure 43 and Figure 44 show an example of a typical layout and design, respectively. Proper use of ground planes can solve EMI and thermal problems. For best results, create a quiet ground plane for the components associated with pins 1 through 4. This offers shielding for the control signals. Also, do not extend the ground plane under heat sinks, thermistors or snubbers so that these components do not heat the UCC28610.

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10.2 Layout Example

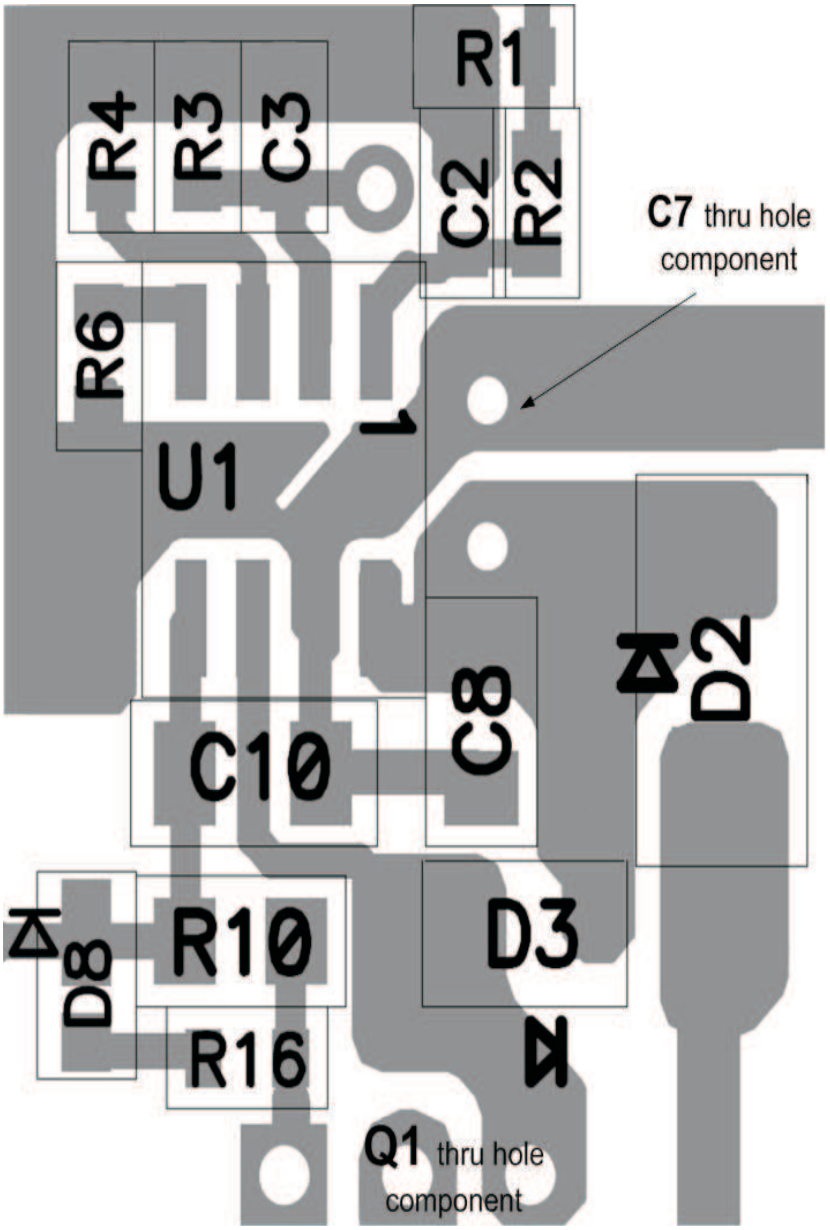

Figure 43. Typical Layout of the Device on a Single Layer PCB

NOTE

The reference designators correspond to the components shown in the schematic of Figure 44.

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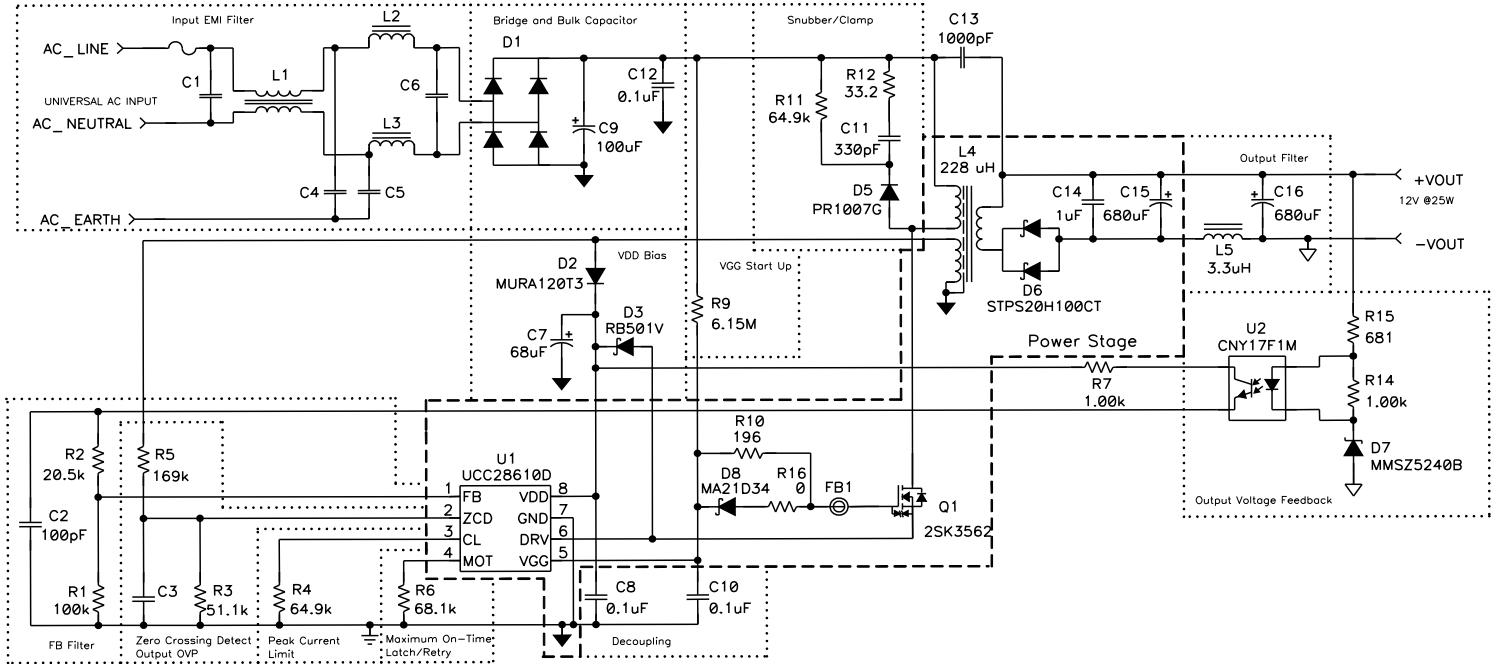

Figure 44. Typical Design Schematic

11 器件和文档支持

11.1 社区资源

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TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

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11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28610D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28610
UCC28610D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28610
UCC28610D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28610
UCC28610DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28610
UCC28610DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28610
UCC28610DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28610

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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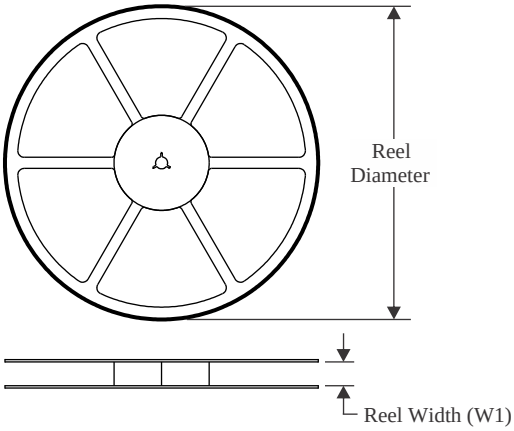
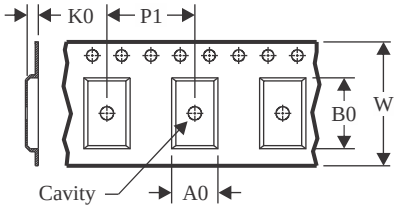
TAPE AND REEL INFORMATION

REEL DIMENSIONS

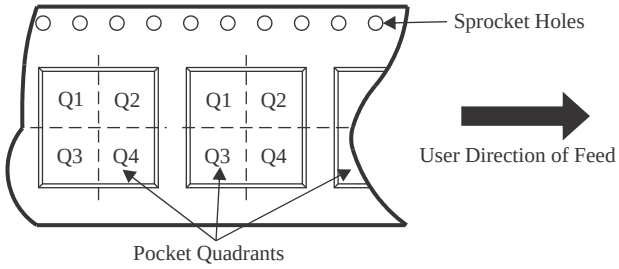


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

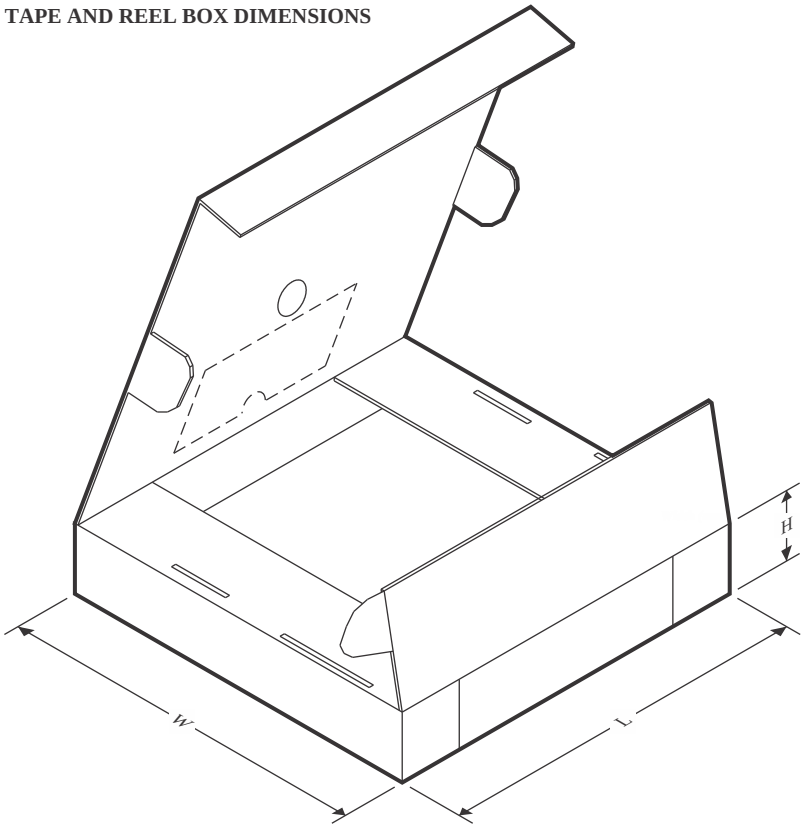
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28610DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

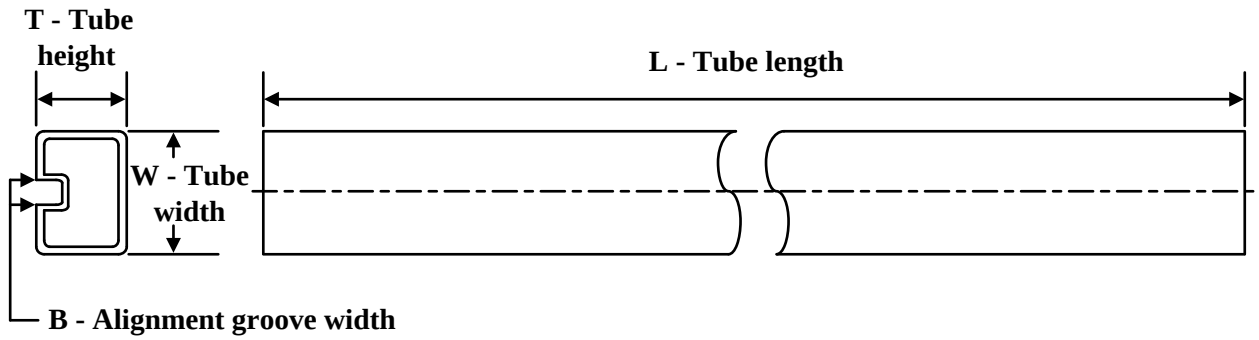
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

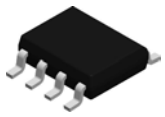
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28610DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28610D	D	SOIC	8	75	507	8	3940	4.32
UCC28610D.A	D	SOIC	8	75	507	8	3940	4.32
UCC28610D.B	D	SOIC	8	75	507	8	3940	4.32

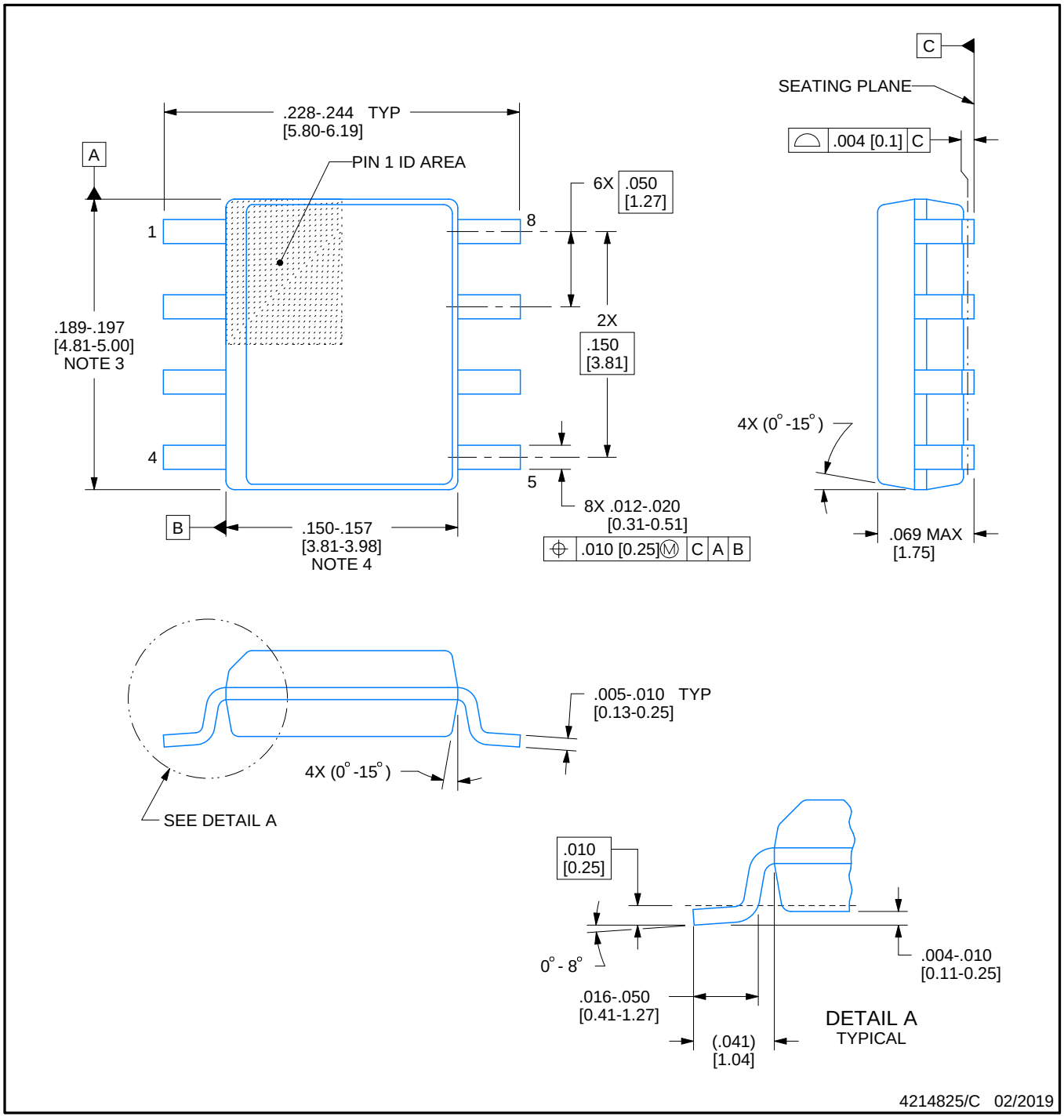


PACKAGE OUTLINE

D0008A

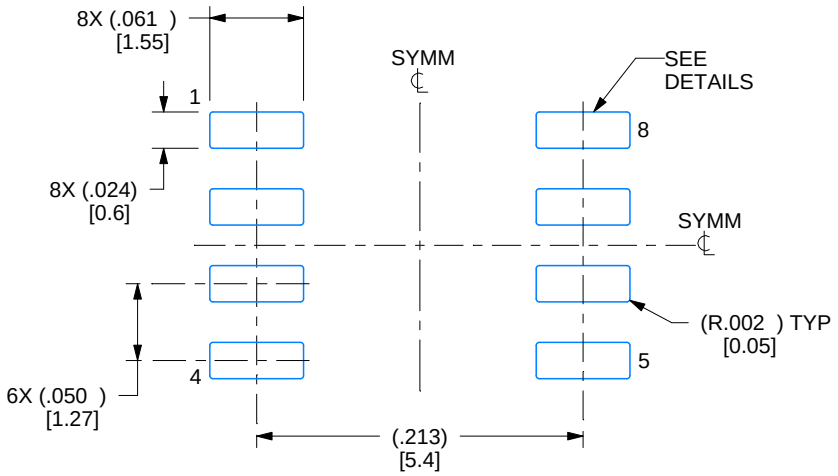
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

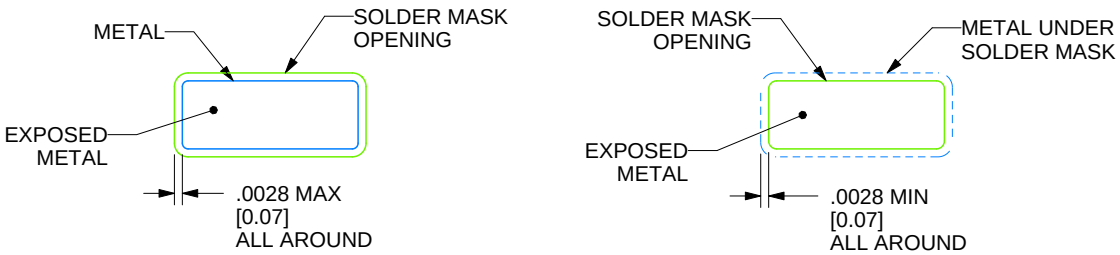


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

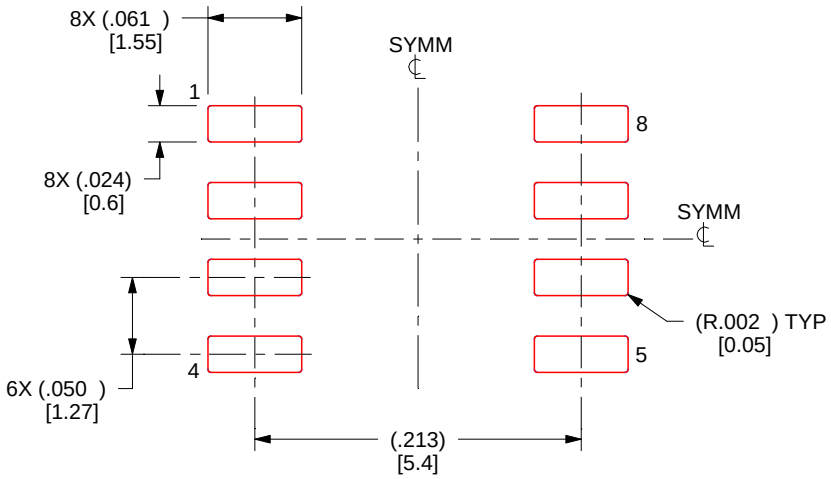
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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