MP28167-A

2.8V to 22V V_{IN}, 3A I_{OUT}, 4-Switch, Integrated Buck-Boost Converter with FB Pin

DESCRIPTION

The MP28167-A is a synchronous, four-switch, integrated buck-boost converter capable of regulating the output voltage across a wide 2.8V to 22V input voltage range with high efficiency. The integrated output voltage scaling and adjustable output current limit functions meet USB power delivery (PD) requirements.

The MP28167-A uses constant-on-time (COT) control in buck mode and constant-off-time control in boost mode, providing fast load transient response and smooth buck-boost mode transient. The MP28167-A provides auto-PFM/PWM or forced PWM switching modes. It also provides configurable output constant current (CC) current limit, which supports flexible design for different applications.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), configurable soft start, and thermal shutdown.

The MP28167-A is available in a QFN-16 (3mmx3mm) package.

FEATURES

- Configurable Output Voltage via FB Pin
- Wide 2.8V to 22V Operating Input Voltage Range
- 0.08V to 1.637V Reference Voltage Range with 0.8mV Resolution through I^2C (1) (Default 1V Reference Voltage)
- 3A Output Current or 4A Input Current
- Four Low $R_{DS(ON)}$ Internal Buck Power MOSFETs
- Adjustable Accurate CC Output Current Limit with Internal Sensing MOSFET via I^2C
- 500kHz/750kHz Selectable Switching Frequency
- Output Over-Voltage Protection (OVP) with Hiccup
- Output Short-Circuit Protection (SCP) with Hiccup
- Over-Temperature Warning and Shutdown
- I^2C Interface with ALT Pin
- One-Time Programmable (OTP) Non-Volatile Memory
- I^2C-Configurable Line Drop Compensation, PFM/PWM Mode, Soft Start, OCP, and OVP
- Configurable EN Shutdown Discharge
- Available in a QFN-16 (3mmx3mm) Package
- The MPL-AL Inductor Series Matches the Best Performance

APPLICATIONS

- USB PD Sourcing Ports
- Buck-Boost Bus Supplies

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Note:

1) For applications where V_{OUT} is below 3V, the switching frequency decreases.

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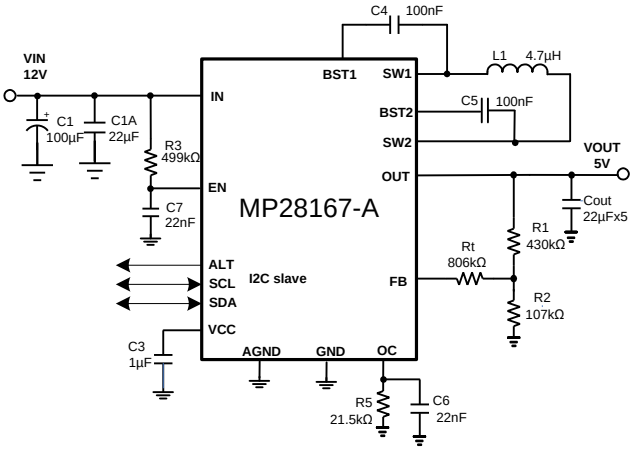
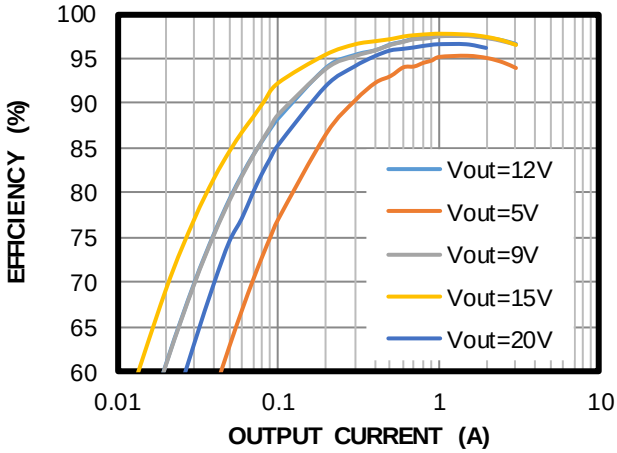
TYPICAL APPLICATION



Efficiency vs. Output Current

V_{IN} = 12V, V_{OUT} = 5V to 20V, L = 4.7µH, f_{SW} = 500kHz, R_{DC} = 16.5mΩ, forced PWM mode



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP28167GQ-A	QFN-16 (3mmx3mm)	*See below*	1
EVKT-MP28167-A	Evaluation kit		

* For Tape & Reel, add suffix –Z (e.g. MP28167GQ-A–Z).

TOP MARKING

BKNY
LLL

BKN: Product code of MP28167GQ-A
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-MP28167-A

EVKT-MP28167-A kit contents (items below can be ordered separately, and the GUI installation file and supplemental documents can be downloaded from the MPS website):

#	Part Number	Item	Quantity
1	EV28167-A-Q-00A	MP28167-A evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I^2C communication interface, one USB cable, and one ribbon cable	1

Order directly from MonolithicPower.com or our distributors.

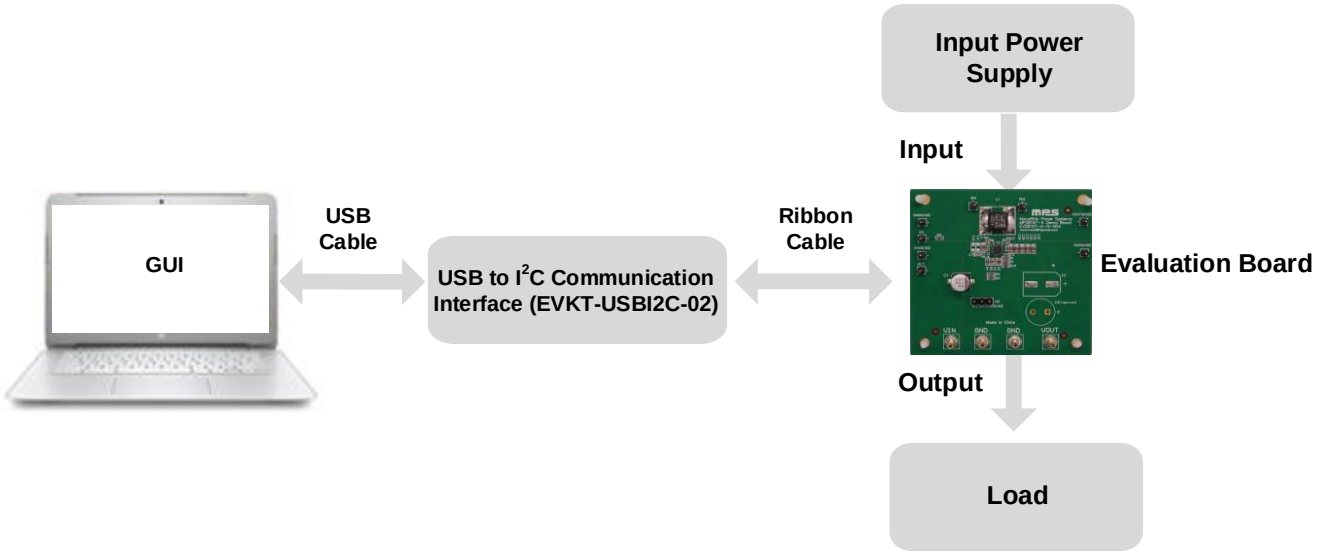

Figure 1: EVKT-MP28167-A Evaluation Kit Set-Up

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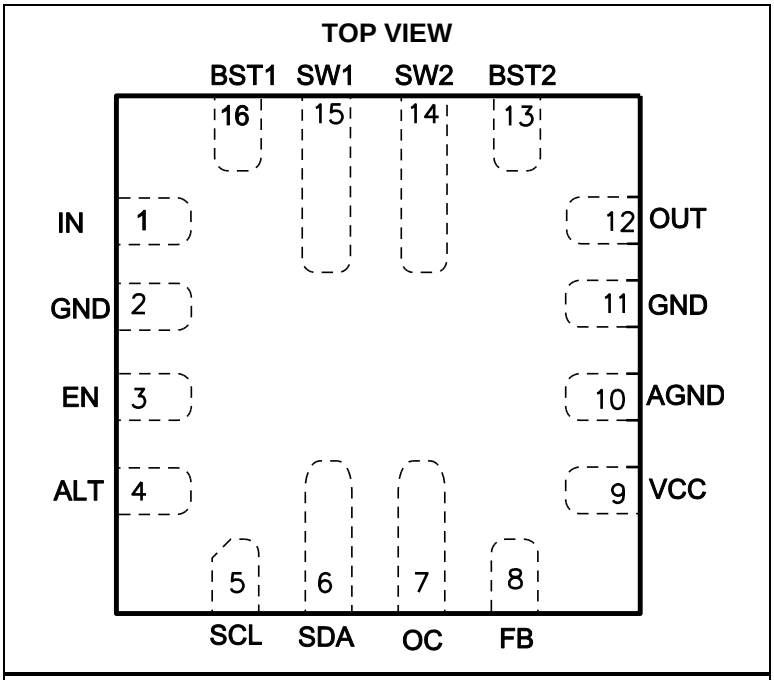
PACKAGE REFERENCE



QFN-16 (3mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	IN	**Supply voltage.** IN is the drain of the internal power device, and provides power to the entire chip. The MP28167-A operates from a 2.8V to 22V input voltage. A capacitor (C_{IN}) is required to prevent large voltage spikes from appearing at the input. Place C_{IN} as close to the IC as possible.
2, 11	GND	**Power ground.** GND is the reference ground of the regulated output voltage. GND requires extra consideration during PCB layout. Connect GND with copper traces and vias.
3	EN	**On/off control for entire chip.** Drive EN high to turn the device on. Drive EN low or float EN to turn it off. EN has an internal 2MΩ pull-down resistor to ground.
4	ALT	**Alert output.** If ALT pulls to logic low, a fault or warning has occurred.
5	SCL	**Clock pin of the I^2C interface.** SCL can support an I^2C clock up to 3.4MHz. If not used, SCL should be pulled up to VCC.
6	SDA	**Data pin of the I^2C interface.** If not used, SDA should be pulled up to VCC.
7	OC	**Output constant current limit set pin.**
8	FB	**Feedback.** Sets the output voltage when connected to the tap of an external resistor divider that is connected between output and GND.
9	VCC	**Internal 3.65V LDO regulator output.** Decouple VCC with a 1µF capacitor.
10	AGND	**Analog ground.** Connect AGND to GND.
12	OUT	**Output power pin.** Place the output capacitor close to OUT and GND.
13	BST2	**Bootstrap.** Connect a 0.1µF capacitor between SW2 and BST2 to form a floating supply across the high-side switch driver.
14	SW2	**Switching node of the second half bridge.** Connect one end of the inductor to SW2 for the current to run through the bridge.
15	SW1	**Switching node of the first half bridge.** Connect one end of the inductor to SW1 for the current to run through the bridge.
16	BST1	**Bootstrap.** Connect a 0.1µF capacitor between SW1 and BST1 to form a floating supply across the high-side switch driver.

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ABSOLUTE MAXIMUM RATINGS (2)

Supply voltage (V_{IN}) 26V
V_{OUT} 24V
$V_{SW1, SW2 (DC)}$ .....-0.3V to +24.3V
$V_{SW1, SW2 (10ns)}$ .....-7V to +26V
$V_{BST1, BST2}$ ..... V_{SWx} + 4V
V_{EN} .....-0.3V to +26V
V_{ALT} .....-0.3V to +5.5V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (3) (6)
..... 4.8W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Rating (4)

All pins (HBM) ..... ±2kV
All pins (CDM).....±2kV

Recommended Operating Conditions (5)

Operation input voltage range .....2.8V to 22V
Output voltage range .....1V to 20.47V
Output current.....3A continuous current or 4A input current
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-16 (3mmx3mm)
EV28167-A-Q-00A (6)..... 26..... 3.... °C/W
JESD51-7 (7) ..... 50..... 12... °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on EV28167-A-Q-00A, 4-layer PCB, 64mmx64mm.
7) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C [8], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{IN}	V_{EN} = 0V		0	3	μA
Quiescent supply current	I_Q	Non-switching, I^2C sets PFM mode		1		mA
EN rising threshold	V_{EN_RISING}		1.00	1.10	1.20	V
EN hysteresis	V_{EN_HYS}			110		mV
EN to ground resistance	R_{EN}	V_{EN} = 2V		2		MΩ
EN on to V_{OUT} > 90% delay	t_{DELAY}	See Figure 7 on page 19		3.6		ms
VCC regulator	V_{CC}		3.3	3.65	4	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 10mA		1		%
V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO}		2.50	2.65	2.8	V
V_{IN} under-voltage lockout threshold hysteresis	V_{UVLO_HYS}			160		mV
Power Converter						
HS switch on resistance	R_{DSON_HS}	Switch A, D		25	40	mΩ
LS switch on resistance	R_{DSON_LSB}	Switch B, C		21	35	mΩ
Feedback voltage	V_{FB}	T_J = 25°C	-1%	1000	+1%	mV
		T_J = -40°C to +125°C	-1.5%	1000	+1.5%	mV
Feedback current	I_{FB}	V_{FB} = 1.05V		10		nA
Output discharge resistance	R_{DIS}			60	100	Ω
Switch leakage	SW_{LKG}	V_{EN} = 0V, $V_{SW1, SW2}$ = 22V, T_J = 25°C			1	μA
		V_{EN} = 0V, $V_{SW1, SW2}$ = 22V, T_J = -40°C to +125°C			5	μA
Oscillator frequency	f_{S1}	Set FREQ = 500kHz by I^2C, T_J = 25°C	-20%	520	+20%	kHz
	f_{S2}	Set FREQ = 750kHz by I^2C, T_J = 25°C		750		kHz
Minimum on time [9]	t_{ON_MIN1}	Switch A, B, C, D		160		ns
Maximum duty cycle	D_{MAX}	Buck mode, FREQ = 500kHz		85		%
Minimum duty cycle [9]	D_{MIN}	Boost mode, FREQ = 500kHz		15		%
Soft-start time	t_{SS}	Can be changed by I^2C, V_{REF} from 0V to 1V, default SS time		3.5		ms
Protection						
Output over-voltage protection	V_{OVP_R}		150%	160%	170%	V_{REF}
Output OVP recovery	V_{OVP_F}		130%	140%	150%	V_{REF}
Low-side B valley limit	I_{LIMIT2}	Switch B	6	8	10	A
Low-side C peak current limit	I_{LIMIT3}	Switch C		10		A

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C [8], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output average current [9]	I_{OUT_LIM1}	V_{OUT} = 5V, across 0°C to 125°C temp range	0.85	1	1.15	A
	I_{OUT_LIM2}	V_{OUT} = 5V, across 0°C to 125°C temp range	-5%	3.5	+5%	A
Output UV threshold	V_{UVP}	20µs deglitch, UV falling	45%	50%	55%	V_{REF}
ALT sink current capability	$ALT_{_LOW}$	Sink 4mA		0.2	0.4	V
ALT leakage	$ALT_{_LKG}$	V_{PULL} = 5V			1	µA
Thermal shutdown rising threshold [9]	T_{STD}			150		°C
Thermal hysteresis [9]	T_{STD_HYS}			20		°C
I^2C Specification [9]						
Input logic high	V_{IH}	I^2C pull-up VDD can be 1.8V to 5V	1.4			V
Input logic low	V_{IL}				0.4	V
Output voltage logic low	V_{OUT_L}				0.4	V
SCL clock frequency	f_{SCL}			400	3400	kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}		0	60		ns
Set-up time for (repeated) start condition	t_{SU_STA}		160			ns
Hold time for (repeated) start condition	t_{HD_STA}		160			ns
Bus free time between a start and a stop condition	t_{BUF}		160			ns
Set-up time for stop condition	t_{SU_STO}		160			ns
SCL and SDA rising time	t_R		10		300	ns
SCL and SDA falling time	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				400	pF

Notes:

8) All min/max parameters are tested at T_J = 25°C. Over-temperature limits are guaranteed by design, characterization, and correlation.
9) Guaranteed by engineering sample characterization.

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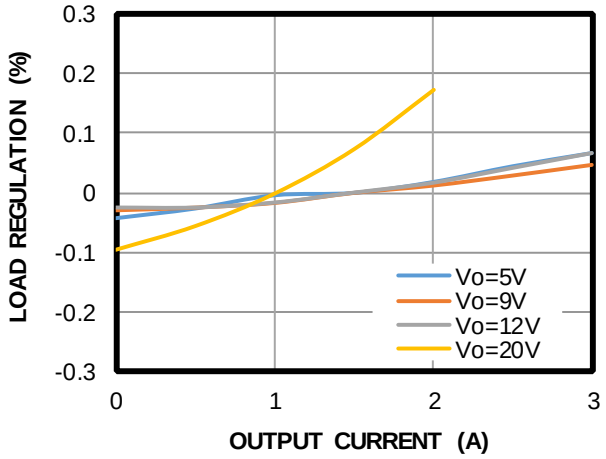
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

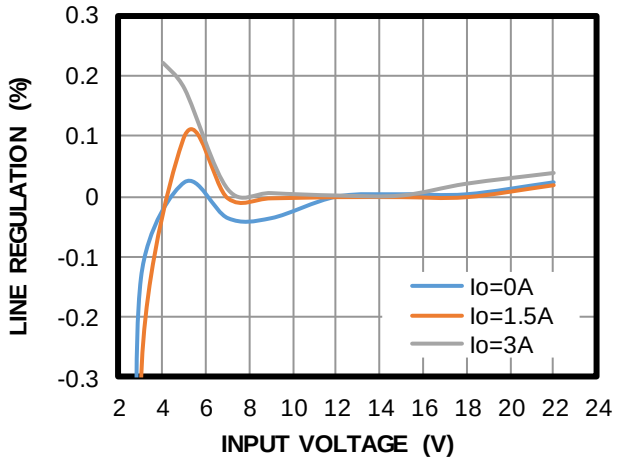
Load Regulation

V_{IN} = 12V, V_{OUT} = 5V/9V/12V/20V,
I_{OUT} = 0A to 3A, no line drop compensation



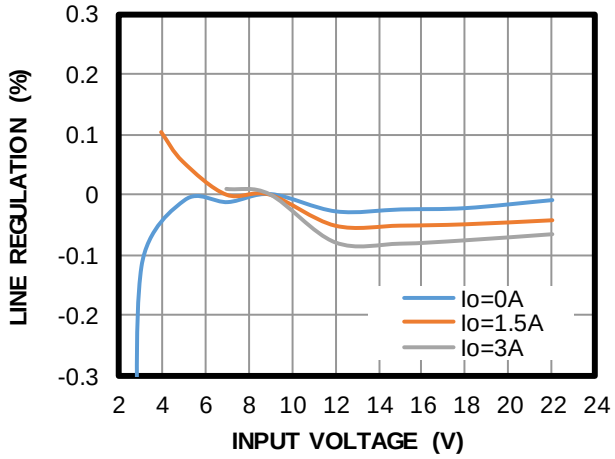
Line Regulation vs. Input Voltage

V_{OUT} = 5V



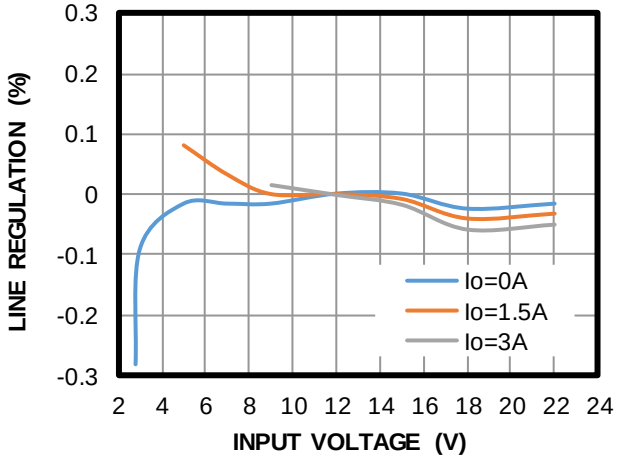
Line Regulation vs. Input Voltage

V_{OUT} = 9V



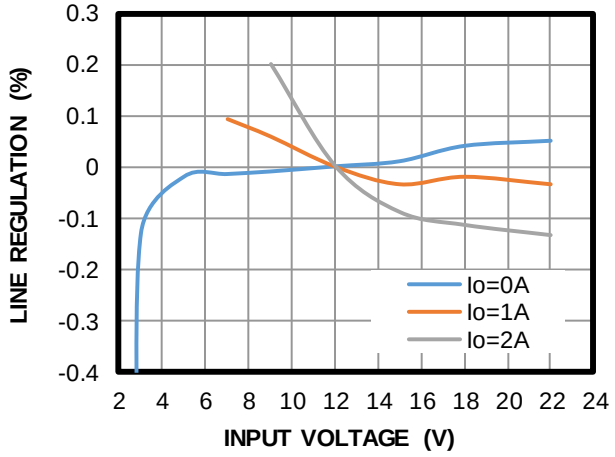
Line Regulation vs. Input Voltage

V_{OUT} = 12V



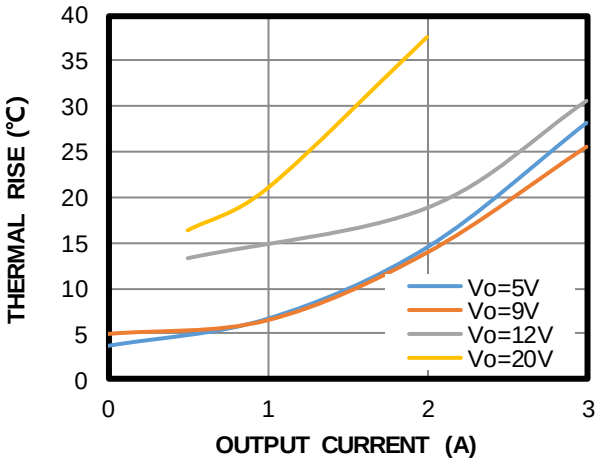
Line Regulation vs. Input Voltage

V_{OUT} = 20V



Thermal Rise vs. Output Current

V_{IN} = 12V, V_{OUT} = 5V to 20V, I_{OUT} = 0A to 3A



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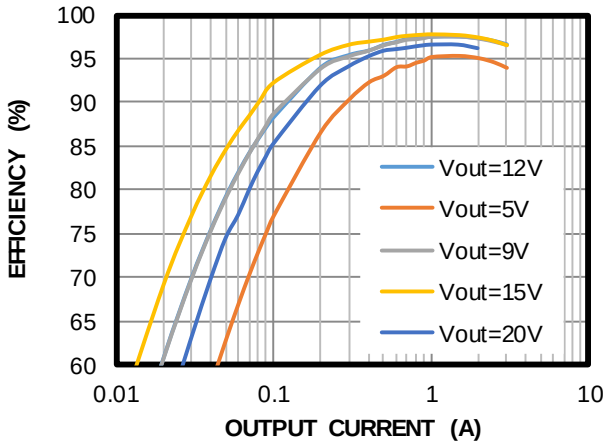
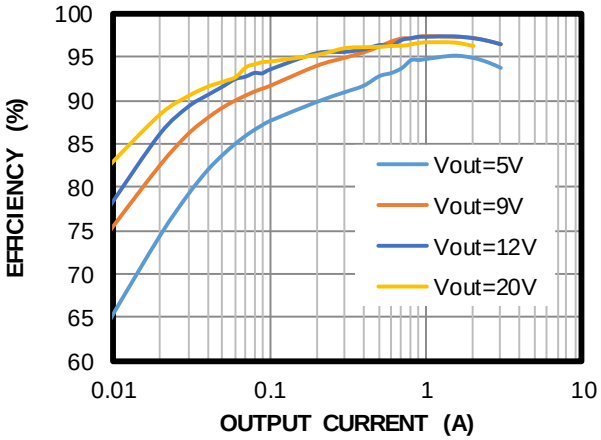
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

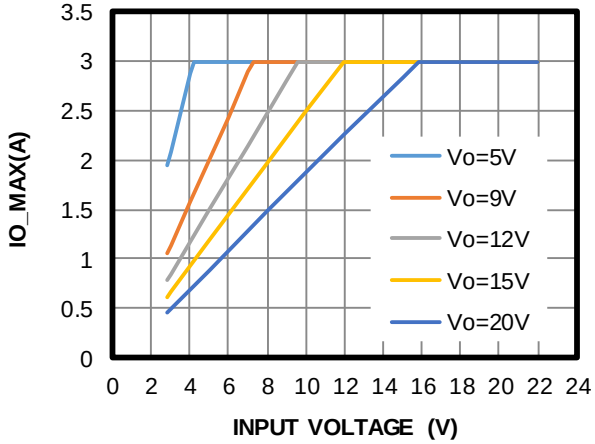
Efficiency vs. Output Current
V_{OUT} = 5V to 20V, R_{DC} = 16.5mΩ, forced PWM mode



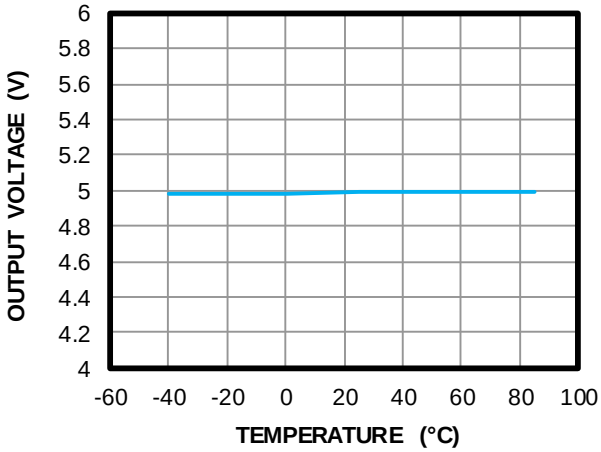
Efficiency vs. Output Current
V_{OUT} = 5V to 20V, R_{DC} = 16.5mΩ, PFM mode



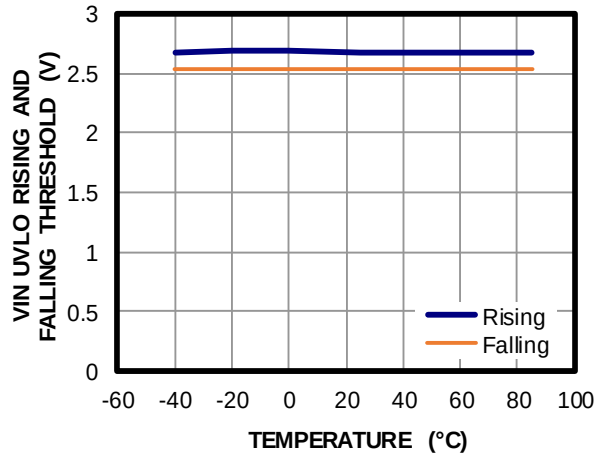
Recommended V_{IN}, V_{OUT}, I_{OUT} Operation Range
22µF x 5 ceramic C_{OUT} capacitor



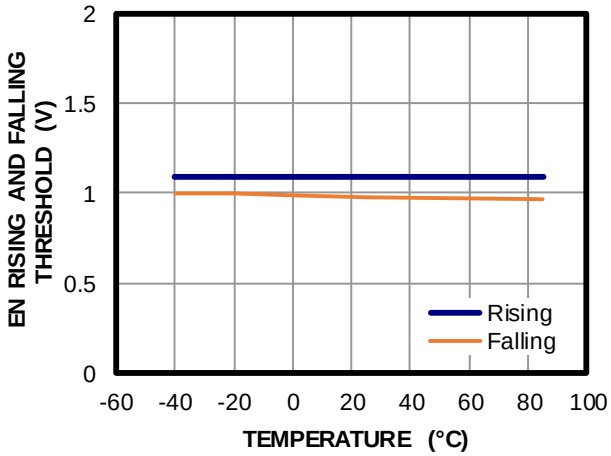
Output Voltage vs. Temperature



VIN UVLO Rising and Falling Threshold vs. Temperature



EN Rising and Falling Threshold vs. Temperature



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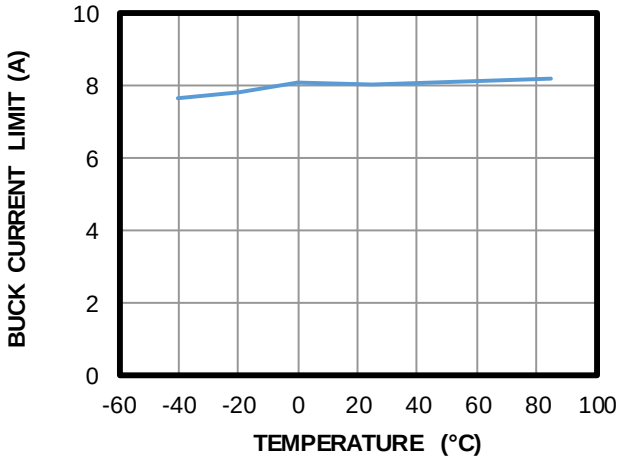
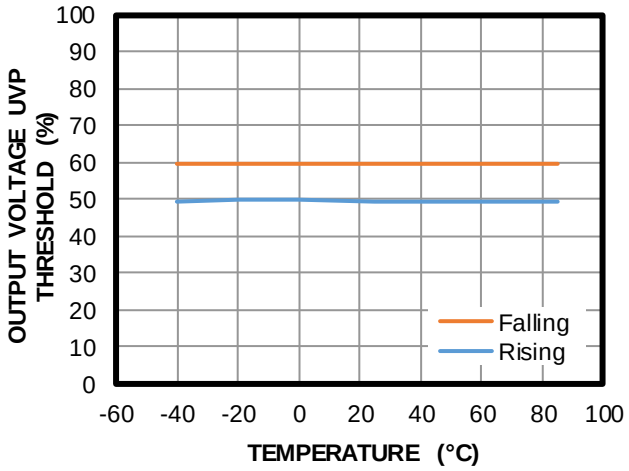
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

Buck Current Limit vs. Temperature



Output Voltage UVP Threshold vs. Temperature



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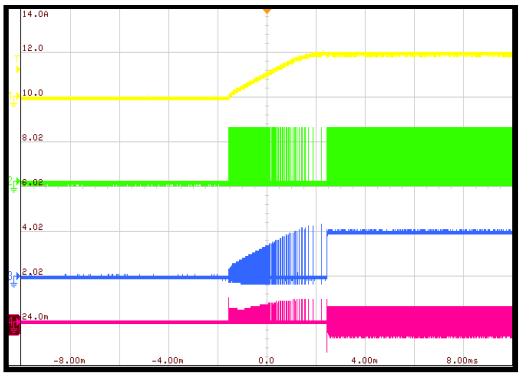
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 500kHz, T_A = 25°C, test waveform is based on Figure 17, unless otherwise noted.

EN Bit Enabled through I²C Command

Load = 0A

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 2A/div.

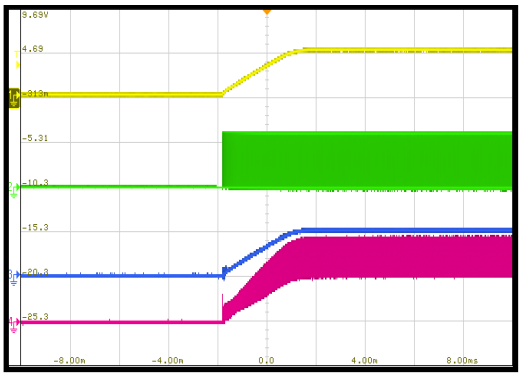


2ms/div.

EN Bit Enabled through I²C Command

Load = 3A

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 2A/div.

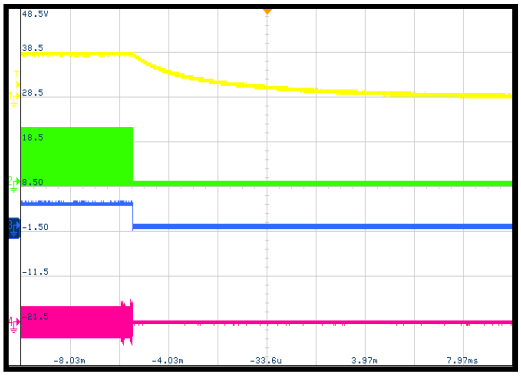


2ms/div.

EN Bit Shutdown through I²C Command

Load = 0A

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 10V/div.
CH4: I_L 2A/div.

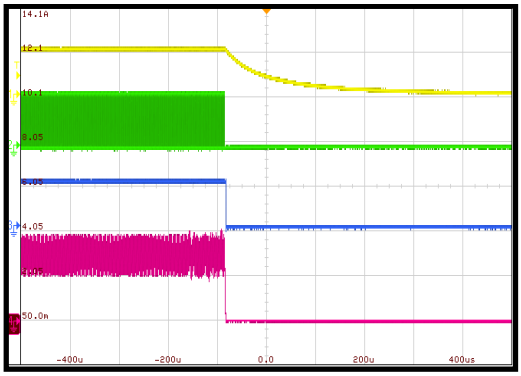


2ms/div.

EN Bit Shutdown through I²C Command

Load = 3A

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 2A/div.

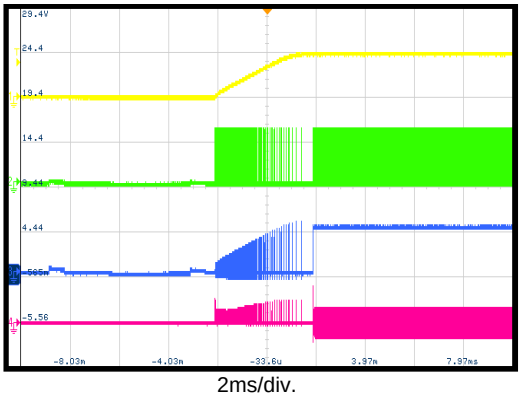


100μs/div.

EN Pin Enabled

Load = 0A

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 2A/div.

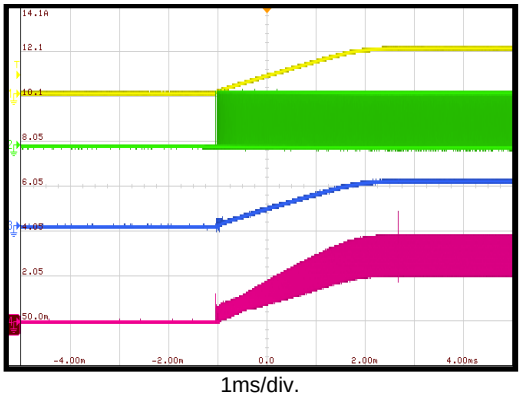


2ms/div.

EN Pin Enabled

Load = 3A

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 2A/div.



1ms/div.

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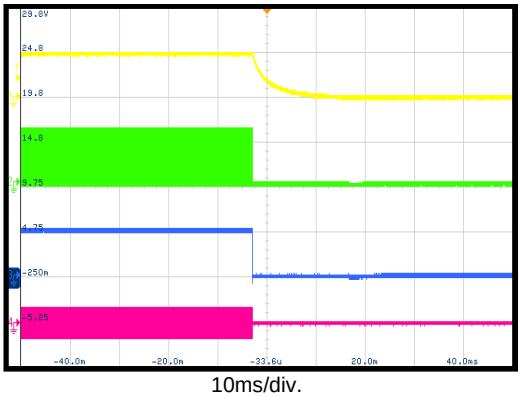
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 500kHz, T_A = 25°C, test waveform is based on Figure 17, unless otherwise noted.

EN Pin Disabled
Load = 0A

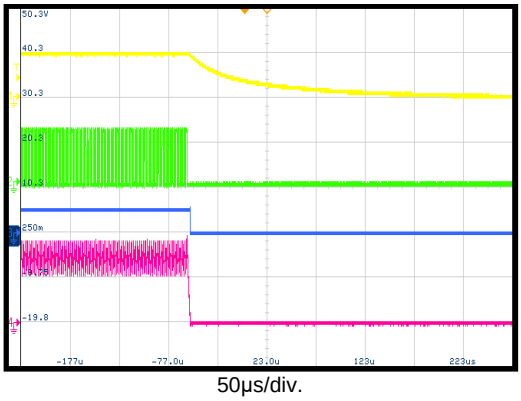
CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 2A/div.



10ms/div.

EN Pin Disabled
Load = 3A

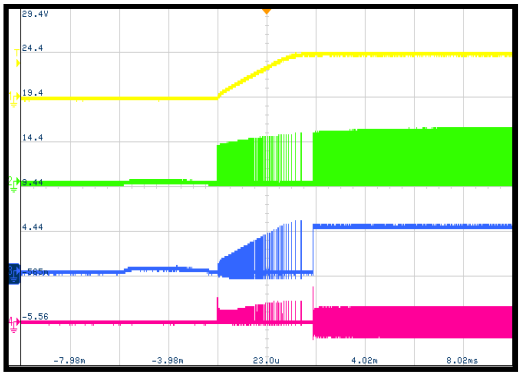
CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 10V/div.
CH4: I_L 2A/div.



50μs/div.

VIN Start-Up
Load = 0A

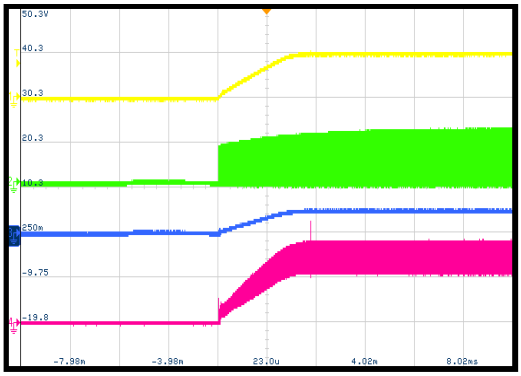
CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 2A/div.



2ms/div.

VIN Start-Up
Load = 3A

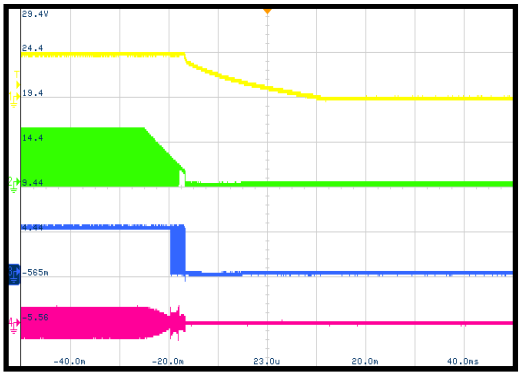
CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 10V/div.
CH4: I_L 2A/div.



2ms/div.

VIN Shutdown
Load = 0A

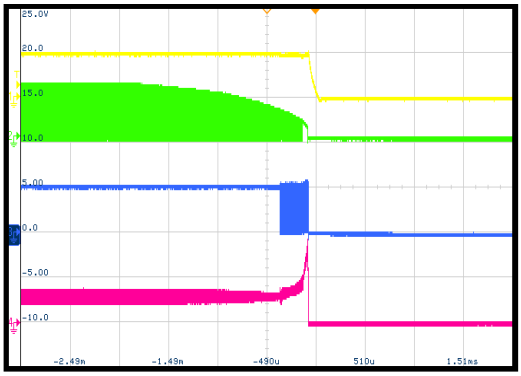
CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 2A/div.



10ms/div.

VIN Shutdown
Load = 3A

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 5A/div.



500μs/div.

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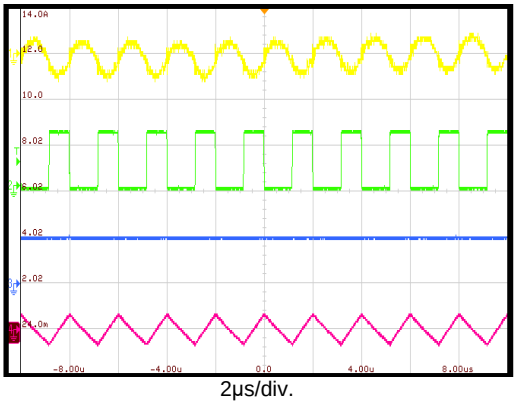
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 500kHz, T_A = 25°C, test waveform is based on Figure 17, unless otherwise noted.

Steady State

V_{OUT} = 5V, load = 0A, f_{SW} = 500kHz

CH1: V_{OUT} 20mV/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 2A/div.

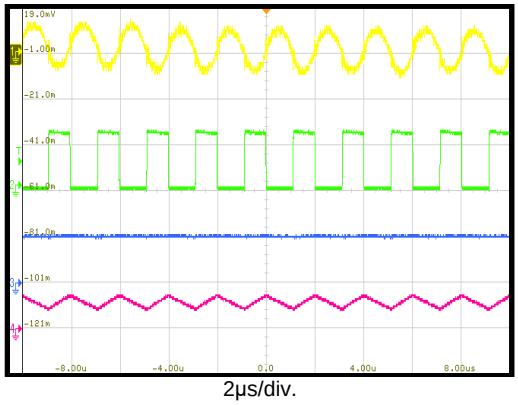


2μs/div.

Steady State

V_{OUT} = 5V, load = 3A, f_{SW} = 500kHz

CH1: V_{OUT} 20mV/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 5A/div.

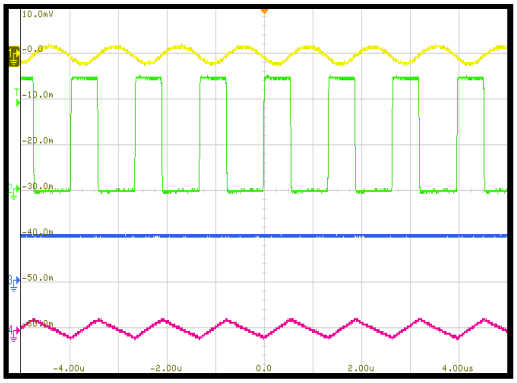


2μs/div.

Steady State

V_{OUT} = 5V, load = 0A, f_{SW} = 750kHz

CH1: V_{OUT}/AC 10mV/div.
CH2: V_{SW1} 5V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 2A/div.

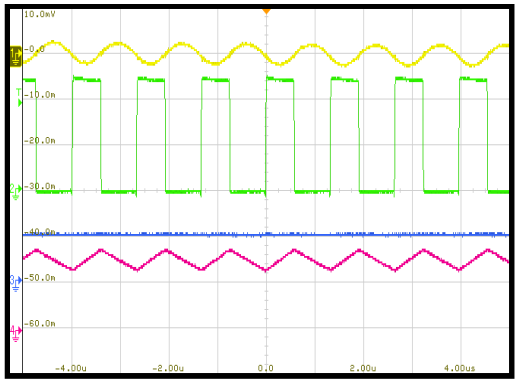


1μs/div.

Steady State

V_{OUT} = 5V, load = 3A, f_{SW} = 750kHz

CH1: V_{OUT}/AC 10mV/div.
CH2: V_{SW1} 5V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 2A/div.

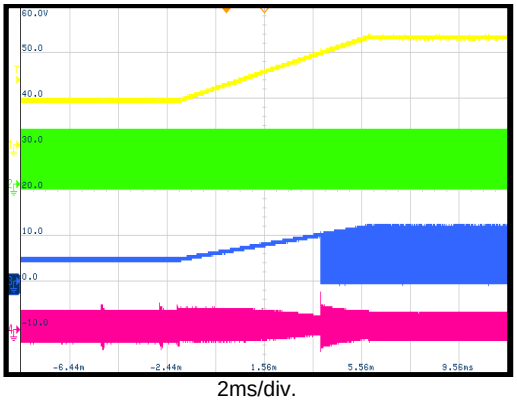


1μs/div.

I^2C VID

V_{OUT} = 5V to 12V, I_{OUT} = 0A, R1 = 430kΩ, R2 = 53.6kΩ

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 10V/div.
CH4: I_L 2A/div.

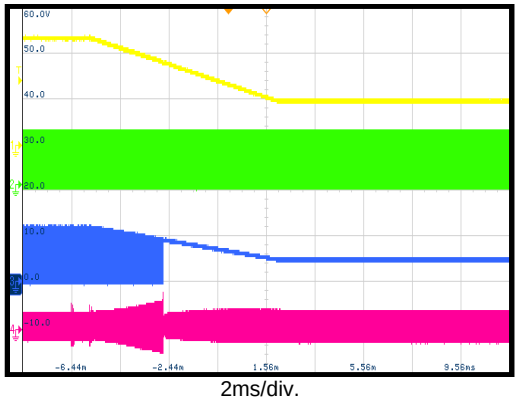


2ms/div.

I^2C VID

V_{OUT} = 12V to 5V, I_{OUT} = 0A, R1 = 430kΩ, R2 = 53.6kΩ

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 10V/div.
CH4: I_L 2A/div.



2ms/div.

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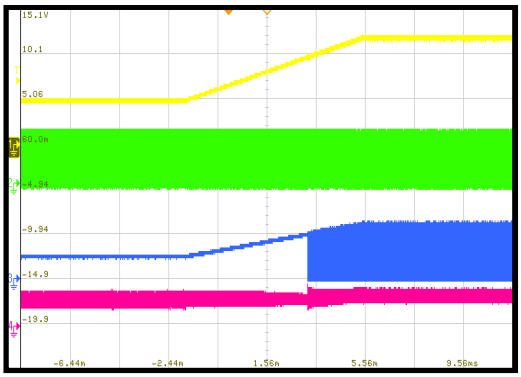
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 500kHz, T_A = 25°C, test waveform is based on Figure 17, unless otherwise noted.

I²C VID

V_{OUT} = 5V to 12V, I_{OUT} = 3A, R1 = 430kΩ, R2 = 53.6kΩ

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 10V/div.
CH4: I_L 5A/div.

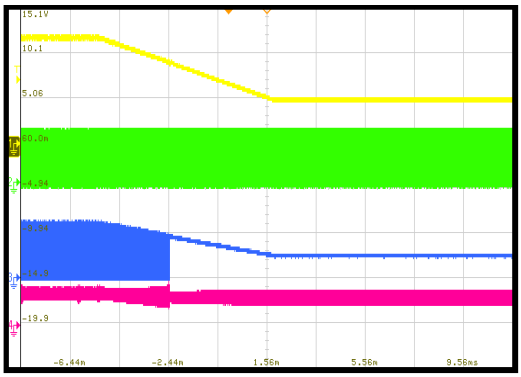


2ms/div.

I²C VID

V_{OUT} = 12V to 5V, I_{OUT} = 3A, R1 = 430kΩ, R2 = 53.6kΩ

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 10V/div.
CH4: I_L 5A/div.

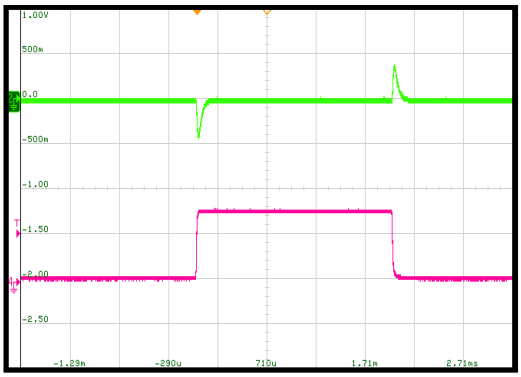


2ms/div.

Load Transient

V_{IN} = 12V, V_{OUT} = 5V, no line drop compensation, 0A to 1.5A, 150mA/μs

CH2: V_{OUT}/AC 500mV/div.
CH4: I_{OUT} 1A/div.

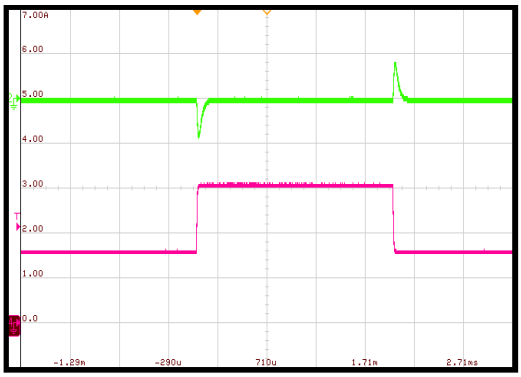


500μs/div.

Load Transient

V_{IN} = 12V, V_{OUT} = 5V, no line drop compensation, 1.5A to 3A, 150mA/μs

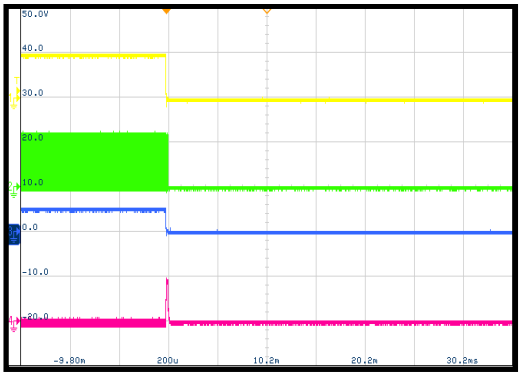
CH2: V_{OUT}/AC 500mV/div.
CH4: I_{OUT} 1A/div.



500μs/div.

Short-Circuit Protection Entry with Latch-Off Mode

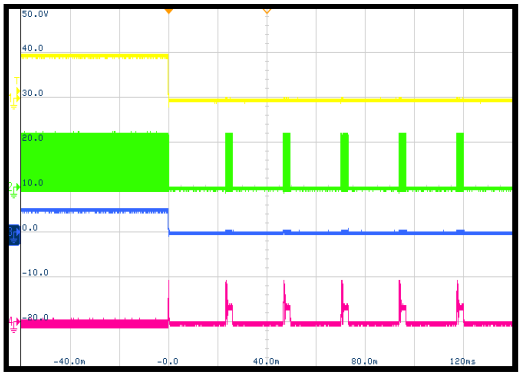
CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 10V/div.
CH4: I_L 10A/div.



5ms/div.

Short-Circuit Protection Entry with Hiccup Mode

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 10V/div.
CH4: I_L 10A/div.



20ms/div.

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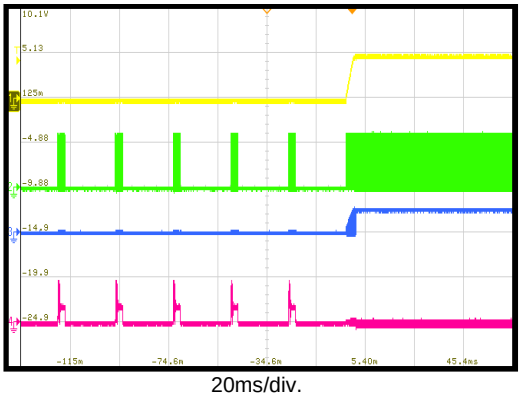
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 500kHz, T_A = 25°C, test waveform is based on Figure 17, unless otherwise noted.

Short-Circuit Protection Recovery with Hiccup Mode

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 10V/div.
CH4: I_L 10A/div.

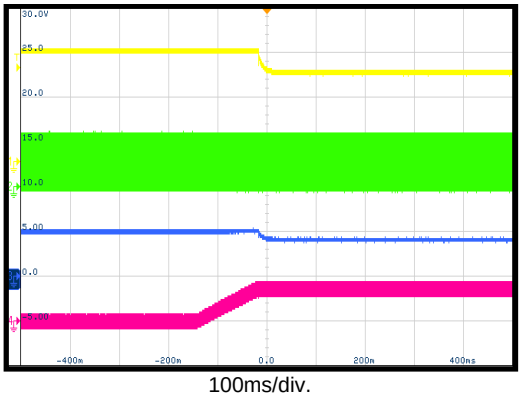


20ms/div.

CC Current Limit Entry

(Test with CV mode of electronic load)

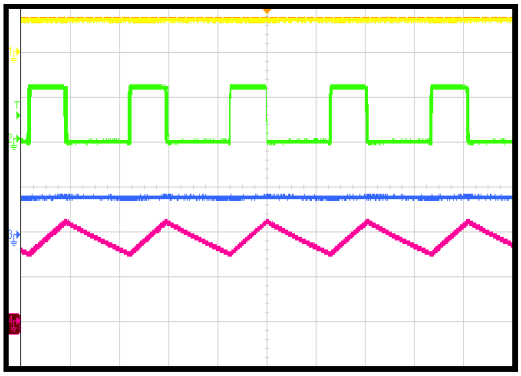
CH1: V_{OUT} 2V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 5A/div.



100ms/div.

CC Current Limit Steady State

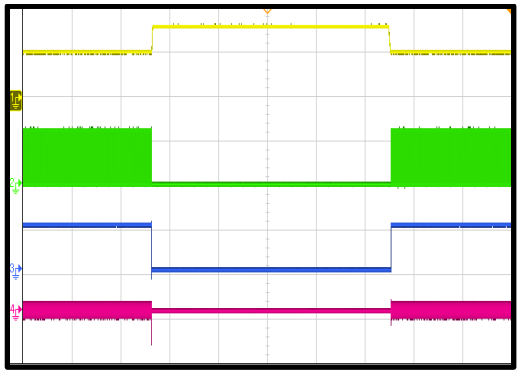
CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 2A/div.



1μs/div.

V_{OUT} OVP with Hiccup Mode

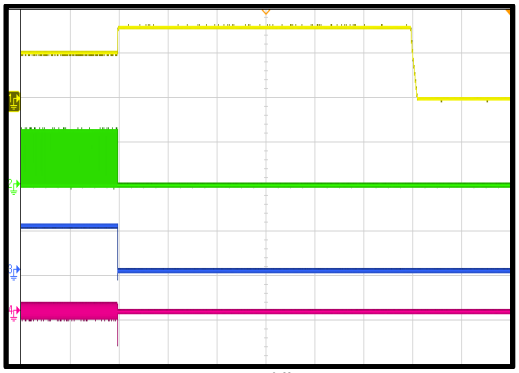
CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 5A/div.



500ms/div.

V_{OUT} OVP with Latch-Off Mode

CH1: V_{OUT} 5V/div.
CH2: V_{SW1} 10V/div.
CH3: V_{SW2} 5V/div.
CH4: I_L 5A/div.



500ms/div.

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FUNCTIONAL BLOCK DIAGRAM

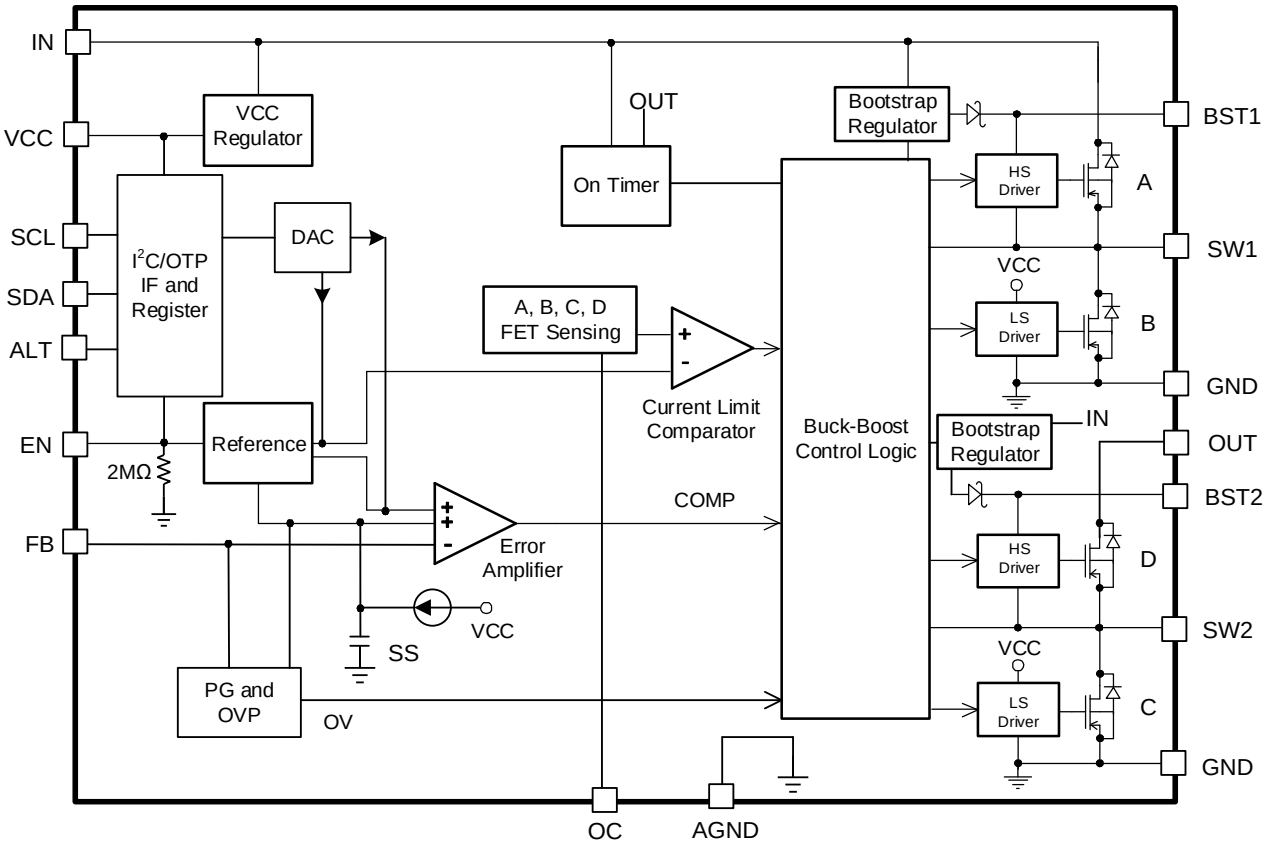

Figure 1: Functional Block Diagram

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OPERATION

The MP28167-A is a four-switch, integrated buck-boost converter that can work in constant-on-time (COT) control mode with a fixed frequency. This provides fast transient response for the buck, boost, and buck-boost modes. A special buck-boost control strategy provides high efficiency over the full input range, and smooth transient between different modes.

Buck-Boost Operation

The MP28167-A can regulate the output voltage (V_{OUT}) to be above, equal to, or below the input voltage (V_{IN}). Figure 2 shows a power structure with one inductor and the four switches.

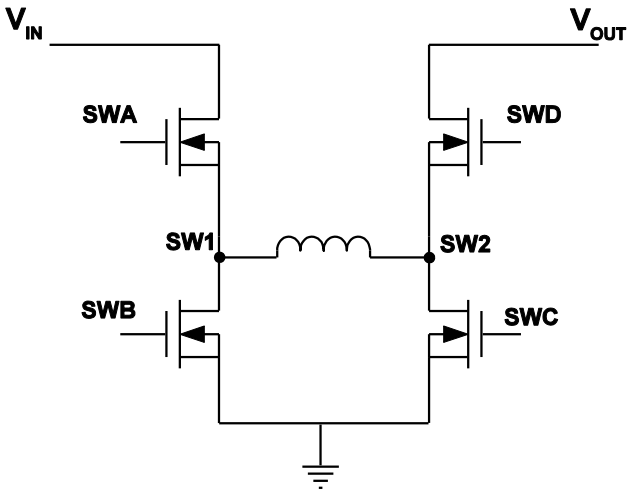

Figure 2: Buck-Boost Topology

The MP28167-A can operate in buck mode, boost mode, or buck-boost mode with different V_{IN} inputs (see Figure 3).

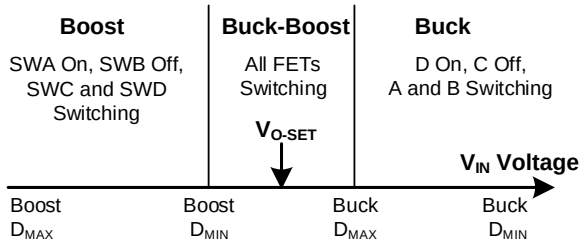

Figure 3: Buck-Boost Operation Range

Buck Mode

When V_{IN} is significantly higher than V_{OUT}, the MP28167-A works in buck mode. In buck mode, SWA and SWB switch for buck regulation. SWC is off, and SWD remains on to conduct the inductor current.

SWA works with COT control logic, and SWB turns on as a complement of SWA. In each cycle, SWB turns on to conduct the inductor current.

When the inductor current drops to the COMP voltage (V_{COMP}), SWB turns off and SWA turns on. SWA turns on for a fixed on time before turning off. Then SWB turns on again, and the operation repeats. The COMP signal is the error amplifier (EA) output from the V_{OUT} feedback and internal FB reference voltage (see Figure 4).

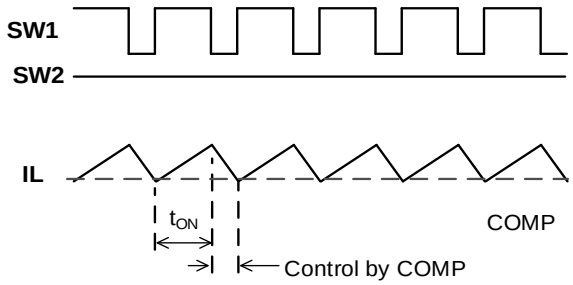

Figure 4: Buck Waveform

Boost Mode

When V_{IN} is significantly lower than V_{OUT}, the MP28167-A works in boost mode. In boost mode, SWC and SWD switch for the boost regulation. SWB is off, and SWA remains on to conduct the inductor current.

During each period, SWC remains off with COT control, while SWD turns on as a complement of SWC to boost the inductor current to the output. In each cycle, SWC turns on to conduct the inductor current. When the inductor current rises and reaches V_{COMP}, SWC turns off and SWD turns on. SWC turns off with a fixed off time before turning on again. During this period, SWD turns on for the current freewheel (see Figure 5).

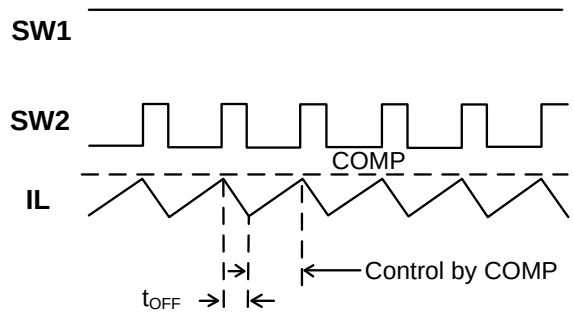

Figure 5: Boost Waveform

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Buck-Boost Mode

When V_{IN} is almost equal to V_{OUT}, the MP28167-A cannot provide enough energy to operate in buck mode due to SWA's minimum off time, or it supplies too much power to V_{OUT} in boost mode due to SWC's minimum on time. The IC uses buck-boost control to regulate V_{OUT} in these conditions.

If V_{IN} drops and the SWA off period is close to the minimum buck off time in buck mode, buck-boost mode is engaged. When the next cycle starts after the SWA and SWD on time (the buck high-side MOSFET [HS-FET] on period), the boost starts with SWA and SWC on (boost low-side MOSFET [LS-FET] on).

SWA and SWD turn on again for the resting period of boost mode (boost HS-FET on). After the boost period elapses, the buck period starts, and SWB and SWD remain on until the inductor current drops to V_{COMP}. Then SWA and SWD turn on until the next boost period begins. Buck and boost switching work with a one-interval period. This is called buck-boost mode.

If V_{IN} rises, and the SWC on period is close to the boost minimum on time in boost mode, buck-boost mode is enabled. After the boost constant-off-time period (SWA and SWD on), SWB and SWD remain on until the inductor current signal drops to V_{COMP}, just like a buck off-time period control.

After the inductor current signal triggers V_{COMP}, SWA and SWD turn on for the buck on time, which is followed by boost switching (SWA and SWC on). Buck and boost switching work with a one-interval period. Figure 6 shows the buck-boost waveform when V_{IN} exceeds V_{OUT}.

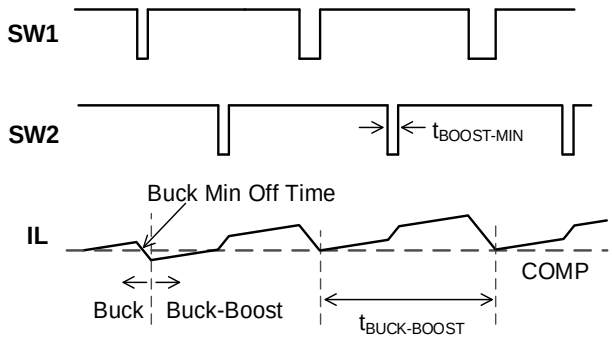

Figure 6: Buck to Buck-Boost Transient

Figure 7 shows the buck-boost waveform when V_{OUT} exceeds V_{IN}.

If V_{IN} exceeds 130% of V_{OUT} in buck-boost mode, the MP28167-A switches from buck-boost mode to buck mode. If V_{IN} drops below 20% of V_{OUT}, the MP28167-A switches from buck-boost mode to boost mode.

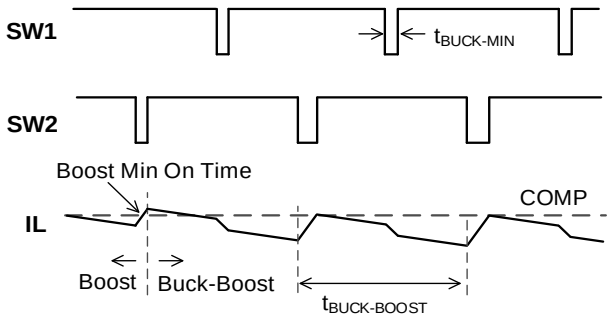

Figure 7: Buck-Boost Waveform

Working Mode Selection

The MP28167-A works with a fixed frequency under heavy-load conditions. When the load current decreases, the MP28167-A can work in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM) based on the MODE register setting.

FCCM (or Forced PWM)

In forced continuous conduction mode (FCCM), the buck on time and boost off time are determined by the internal circuit. This achieves a fixed frequency based on the V_{IN} / V_{OUT} ratio. When the load decreases, the average input current drops, and the inductor current may go negative from V_{OUT} to V_{IN} during the off time (SWD on). This forces the inductor current to work in continuous mode with a fixed frequency, producing a lower V_{OUT} ripple than in PSM mode.

PSM (Auto-PFM/PWM Mode)

If the inductor current drops to 0A in PSM, SWD turns off to prevent the current from flowing from V_{OUT} to V_{IN}, forcing the inductor current to work in discontinuous conduction mode (DCM). Meanwhile, the internal off time clock stretches once the MP28167-A enters DCM mode. The frequency drops when the inductor current conduction period decreases, which helps save power loss and reduce the V_{OUT} ripple.

If V_{COMP} drops to the PSM threshold (even if the IC stretches the frequency), the MP28167-A stops switching to further decrease the switching power loss.

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The MP28167-A recovers switching once V_{COMP} exceeds the PSM threshold. The switching pulse skips based on V_{COMP} in very light-load conditions. PSM has a much higher efficiency than FCCM mode in light load, but the V_{OUT} ripple may be higher due to the group switching pulse.

Internal VCC Regulator

The 3.65V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 3.65V, the output of the regulator is in full regulation. If V_{IN} drops below 3.65V, the output decreases with V_{IN}. VCC requires an external 1µF ceramic capacitor for decoupling.

Enable (EN) Control

The MP28167-A has an enable (EN) control pin. Pull EN high to enable the IC. Pull EN low or float EN to disable the IC.

If EN is pulled down when the output discharge function is enabled, the MP28167-A shuts down after 55ms. The MP28167-A's I^2C register value is reset to default only after the MP28167-A experiences this type of shutdown. If EN is pulled high within 55ms, the I^2C register is not reset, and the MP28167-A enables the output with the previous register setting.

If the output discharge function is disabled, the MP28167-A shuts down once EN is pulled down for more than 100µs, and the MP28167-A I^2C register is reset after a 100µs delay.

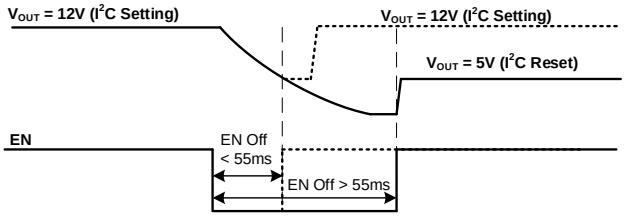

Figure 8: EN On/Off Logic for I^2C Register Reset

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage and enables or disables the entire IC.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates an SS voltage that ramps up from 0V to 3.65V. If the SS voltage (V_{SS}) is below V_{REF}, the error amplifier uses V_{SS} as the reference. If V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

If the output of the MP28167-A is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor exceeds the internal feedback voltage (see Figure 8).

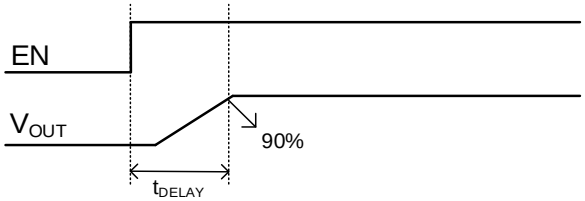

Figure 9: EN On to V_{OUT} > 90% Delay

Over-Current Protection (OCP)

The MP28167-A has a constant-current limit control loop to limit the output average current. The current information is sensed from switches A, B, C, and D. Then an average algorithm calculates the output current.

When the output current exceeds the current-limit threshold, the output voltage starts to drop.

There are two conditions that activate this condition:

1. The first is if V_{OUT} exceeds 3V, V_{FB} drops below 50% of V_{REF}, and V_{OUT} drops below 3V. The MP28167-A then enters hiccup mode or latch off mode according to the I^2C setting.
2. The second is if V_{OUT} is set below or equal to 3V, and V_{OUT} drops below the under-voltage (UV) threshold (typically 50% below V_{REF}). The MP28167-A then enters hiccup mode or latch-off mode according to the I^2C setting.

In hiccup mode, the MP28167-A stops switching and recovers automatically with 12.5% duty cycles. In latch-off mode, the MP28167-A stops switching until the IC restarts (power cycling on VIN or EN, or EN bit toggling).

Over-Voltage Protection (OVP)

The MP28167-A monitors a resistor-divided feedback voltage to detect output over-voltage (OV) conditions. When the feedback voltage exceeds 160% of the target voltage, the over-voltage protection (OVP) comparator output

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goes high. The output-to-ground discharge resistor turns on.

The OUT pin has an absolute OVP function. Once V_{OUT} exceeds the absolute OVP threshold (23V), the MP28167-A stops switching and turns on the OUT-to-ground discharge resistor.

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid fault triggers. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Output Discharge

The MP28167-A has an output discharge function that provides a resistive discharge path for the external output capacitor. The function is active when the part is disabled (input voltage is under UVLO or enable off), the discharge path is turned off when V_{OUT} < 50mV or waits for the 50ms maximum timer to pass. This function can also be disabled via the I²C.

Thermal Warning (TSW) and Shutdown (TSD)

Thermal warning and thermal shutdown prevent the part from operating at exceedingly high temperatures. When the silicon die temperature exceeds 120°C, the MP28167-A sets the OTW bit [D5] to 1. When the temperature falls below its lower threshold (typically 100°C), the OTW bit [D5] is set to 0.

When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled. This is a non-latch protection.

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence.

The MP28167-A interface is an I²C slave that supports fast mode (400kHz) and high-speed mode (3.4MHz). The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled instantaneously via the I²C interface.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by a 0 to indicate a write operation, or 1 to indicate a read operation.

Start and Stop Conditions

The start and stop conditions are signaled by the master device, which signifies the beginning and end of an I²C transfer. The start (S) condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop (P) condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 9).

The master then generates the SCL clocks and transmits the device address and the read/write direction bit (R/W) on the SDA line.

Transfer Data

Data is transferred in 8-bit bytes by an SDA line. Each byte of data should be followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MP28167-A requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. The MP28167-A acknowledges that it has received each byte by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP28167-A. The MP28167-A performs an update on the falling edge of the LSB byte. See Figure 11, Figure 12, and Figure 13 for examples I²C write and read sequences.

I²C Start-Up Timing

I²C functionality is enabled once EN is active and VIN exceeds the under-voltage lockout (UVLO) threshold. The I²C works during over-current protection (OCP), over-voltage protection (OVP), and thermal shutdown.

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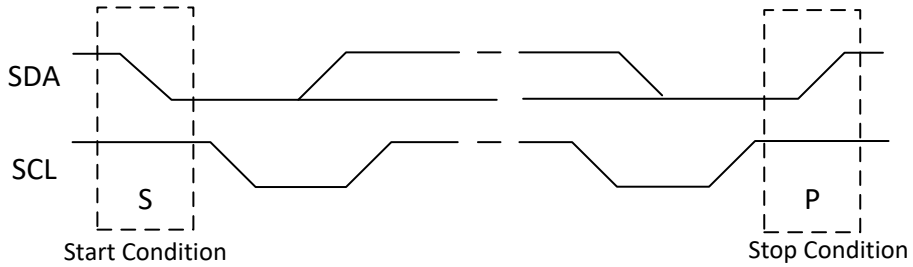

Figure 10: Start and Stop Conditions

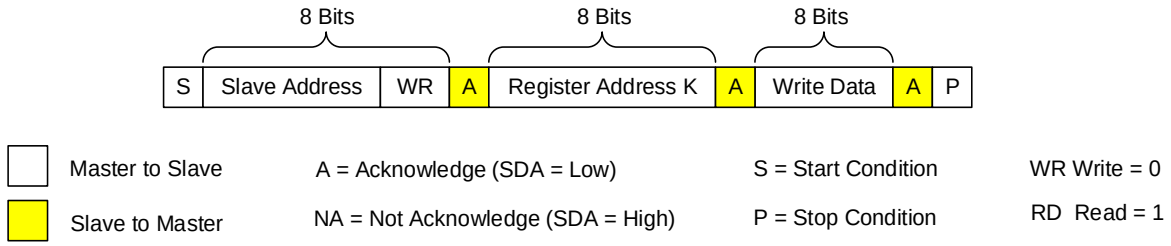

Figure 11: I²C Write Example (Write Single Register)

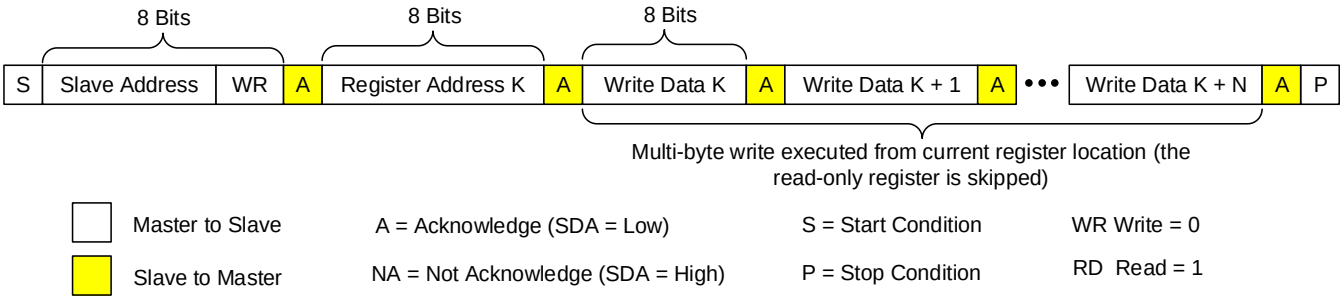

Figure 12: I²C Write Example (Write Multi-Register)

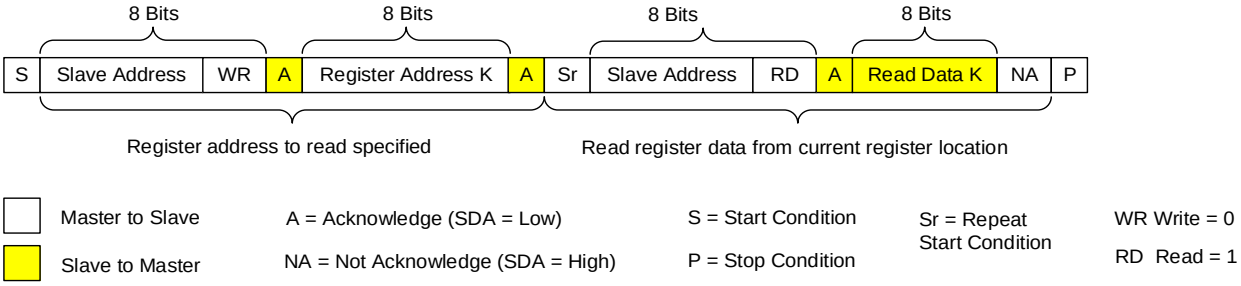

Figure 13: I²C Read Example (Read Single Register)

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I²C REGISTER MAP

Add (Hex)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VREF_L	R/W	RESERVED					VREF DATA BIT LOW [2:0] (10)		
01	VREF_H	R/W	VREF DATA BIT HIGH [10:3] (10)							
02	VREF_GO	R/W	RESERVED						PG_ DELAY_ EN (10)	GO_ BIT
03	IOUT_LIM	R/W	RESERVED	Output current limit threshold (0A to 6.35A/50mA step for 21.5kΩ OC resistor) (10)						
04	CTL1	R/W	EN (10)	HICCUP OCP_OVP (10)	DISCHG _EN (10)	MODE (10)	FREQ (10)		RESERVED	
05	CTL2	R/W	LINE DROP COMP (10)		SS (10)		RESERVED			
06	RESERVED	R	RESERVED, ALL “0”						RESERVED	
07	RESERVED	R	RESERVED							
08	RESERVED	R	RESERVED							
09	Status	R	PG	OTP	OTW	CC_CV	RESERVED			
0A	INTERRUPT	W1C	OTEMPP_ ENTER	OT WARNING_ ENTER	OC_ ENTER	OC_ RECOVER	UVP_ FALLING	OTEMPP _EXIT	OT WARNING _EXIT	PG_ RISING
0B	MASK	R/W	RESERVED			OTPMSK (10)	OTWMSK (10)	OC_ MSK (10)	UVP_ MSK (10)	PG_ MSK (10)
0C	ID1	R	OTP Configure Code. “0x00” means the standard MP28167-A							
27	MFR_ID	R	Manufacturer ID: b ‘0000 1001’							
28	DEV_ID	R	Device ID: b ‘0101 1000’							
29	IC_REV	R	IC revision: b ‘0000 0001’							

Note:

10) These items have one-time programmable (OTP) non-volatile memory. The OTP is reloaded to the I²C register when V_{IN} exceeds the under-voltage lockout (UVLO) threshold, or during EN shutdown.

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REGISTER DESCRIPTION

I²C Bus Slave Address

The MP28167-A I²C slave address is fixed as 60H.

Output Reference Voltage Setting

The registers VREF_L and VREF_H set the reference voltage and follow 11-bit direct format.

Name	VREF															
Format	Direct, unsigned binary integer															
Register Name	N/A					VREF_H D[7:0]								VREF_L D[2:0]		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	N/A					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	N/A					Data bit high								Data bit low		
Default Value (1000mV)	N/A					1250 integer										

The reference voltage can be calculated with Equation (1):

$$V_{REF}\ (mV) = V \times 0.8 \quad (1)$$

Where V is an 11-bit unsigned binary integer of VREF[10:0] that ranges from 0 to 2047. The V_{REF} resolution is 0.8mV/LSB. The reference voltage changing slew rate is fixed at 1mV/µs. See the GO_BIT section below to change the reference voltage.

VREF_GO Register

GO_BIT D[0]

The MP28167-A can be controlled when V_{REF} begins to change. Set GO_BIT to 1 to start the output reference change based on the V_{REF} register. When the V_{REF} change is complete (internal V_{REF} reaches its target value), GO_BIT auto-resets to 0. This prevents a false operation of V_{REF} scaling.

Write the reference voltage (0x00 and 0x01 registers) first, and then write GO_BIT = 1. V_{REF} changes based on the new register setting. GO_BIT resets to 0 when V_{REF} reaches a new value. The host can read GO_BIT to determine whether V_{REF} scaling has completed.

The VOUT-to-ground discharge function is enabled when GO_BIT = 1. This can ramp V_{OUT} from high to low under light-load conditions.

When GO_BIT = 0, V_{REF} does not change. When GO_BIT = 1, V_{REF} changes based on the V_{REF} register setting. After V_{REF} scaling finishes, GO_BIT is automatically reset to 0.

PG_DELAY_EN D[1]

When PG_DELAY_EN D[1] = 0, there is no delay on PG. When PG_DELAY_EN D[1] = 1, PG experiences a 100µs rising delay. The default value is 0.

IOUT_LIM Register

Sets the output current limit threshold.

Name	IOUT_LIM							
Format	Direct, unsigned binary integer							
Bit	7	6	5	4	3	2	1	0
Access	N/A	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value (3.5A)	N/A	70 integer						

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IOUT_OC can be calculated with Equation (2):

$$IOUT_OC\ (A) = IOUT_LIM \times 0.05 \quad (2)$$

Where IOUT_LIM is a 7-bit unsigned binary integer of IOUT_LIM D[6:0], and the IOUT_OC resolution is 50mA/LSB (maximum value is 6.35A).

The resistor connected from the OC pin to ground should be 21.5kΩ when using the IOUT_LIM register. Add a 22nF (C6) filter capacitor on OC to keep the CC loop stable. The MP28167-A allows IOUT_LIM to be directly changed using the I^2C. If the CC threshold must be changed after the MP28167-A has already entered the CC limit operation state, it is recommended to change the CC threshold step by step (e.g. 50mA per step) instead of changing the current value to the final value.

CTL1 Register

Bits	Bit Name	Default	Description
D[7]	EN	1	I^2C-controlled bit to turn the part on and off. When the external EN pin is low, the converter is off, and the I^2C shuts down. When EN is high, the EN bit takes over. 1: Enable the part 0: Disable the part
D[6]	HICCUP OCP_OVP	1	Over-current (OC) and over-voltage protection (OVP) mode selection. 1: Hiccup mode 0: Latch-off mode
D[5]	DISCHG_EN	1	Output discharge enable bit. 1: Output discharge occurs during EN or VIN shutdown 0: No output discharge occurs during shutdown
D[4]	MODE	1	Enable PFM/PWM mode bit. The default is PWM mode under light-load conditions. 0: Enables auto-PFM/PWM mode 1: Sets forced PWM mode
D[3:2]	FREQ	00	Sets the switching frequency. 00: 500kHz 01: 750kHz 10: Reserved 11: Reserved

CTL2 Register

Bits	Bit Name	Default	Description
D[7:6]	LINE DROP COMP	00	Sets the output voltage compensation (V_{LINE} vs. the load feature). 00: No compensation 01: V_{OUT} compensates 60mV when I_{OUT} = 3A 10: V_{OUT} compensates 120mV when I_{OUT} = 3A 11: V_{OUT} compensates 200mV when I_{OUT} = 3A V_{OUT} compensation is based on R1 and R2. V_{LINE} = (1 + R1 / R2) x $V_{REFLINE}$. Where $V_{REFLINE}$ is 0mV/12mV/24mV/40mV when the D[7:6] bits are 00/01/10/11, respectively. V_{LINE} is the compensated voltage.
D[5:4]	SS	10	Sets the output start-up soft-start timer (from 0% to 100%). If the reference voltage is 1V: 00: 1.1ms 01: 2.2ms 10: 3.5ms 11: 4.4ms The SS slew rate is constant, but SS time changes with different V_{REF} values. For example, the SS time = 3.5ms for 1V V_{REF}, and the SS time = 5.25ms for 1.5V V_{REF}.

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Status Register

Bit	Bit Name	Default	Description	Notes
D[7]	PG	N/A	Output power good indication. 0: Output power is not good 1: Output power is good	These status bits indicate instantaneous values.
D[6]	OTP	N/A	Over temperature protection (OTP) indication. 0: OTP has not occurred 1: OTP has occurred	
D[5]	OTW	N/A	Over-temperature warning (OTW) indication. 0: OTW has not occurred 1: OTW has occurred	
D[4]	CC_CV	N/A	Enable bit for constant-current (CC) output mode or constant-voltage (CV) output mode. 0: CV mode 1: CC mode	

Interrupt Register

Bits	Bit Name	Description	Notes
D[7]	OTEMPP_ ENTER	Over-temperature protection entry indication. When this bit is high, the IC enters thermal shutdown. This bit is not masked, even if OTPMSK = 1. Setting OTPMSK to 1 only masks the interrupt pin's output (ALT).	This bit is latched once triggered. Write 0xFF to this register to reset the interrupt and ALT pin's state.
D[6]	OTWARNING_ ENTER	Die temperature early warning enter bit. When this bit is high, the die temperature exceeds 120°C. This bit is not masked, even if OTWMSK = 1. Setting OTWMSK to 1 only masks the interrupt pin's output (ALT).	
D[5]	OC_ENTER	Entry of over-current (OC) or constant-current (CC) current-limit mode. THE OC_MSK bit can enable or disable the OC_ENTER and OC_RECOVER ALERT outputs.	
D[4]	OC_RECOVER	Recovery from constant-current (CC) current-limit mode. If the device recovers from a hiccup, it does not trigger this interrupt signal.	
D[3]	UVP_FALLING	Reference voltage is in under-voltage protection (UVP) threshold.	
D[2]	OTEMPP_EXIT	Over-temperature protection (OTP) ends. OTPMSK can mask off the ALT signals of this bit.	
D[1]	OTWARNING_ EXIT	Die temperature early warning exit bit. When the die temperature is below 100°C, this bit is set to 1. This bit is not masked, even if OTWMSK = 1. Setting OTWMSK to 1 only masks the interrupt pin's output (ALT).	
D[0]	PG_RISING	Output power good rising edge.	

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MSK Register

Bit	Bit Name	Default	Description
D[4]	OTPMSK	0	Set OTPMSK to 1 to mask off the over-temperature protection (OTP) alert. Setting OTPMSK to 1 only masks the interrupt pin's output (ALT). This is not the interrupt register, but it is similar for other mask bits.
D[3]	OTWMSK	0	Masks off the over-temperature warning.
D[2]	OC_MSK	0	Masks off both over-current (OC) and constant current (CC) entry and recovery.
D[1]	UVP_MSK	0	Masks off the output under-voltage protection (UVP) interrupt.
D[0]	PG_MSK	0	Masks off the PG indication function on ALT. 1: The ALT pin does not indicate a PG event 0: The ALT indicates a PG rising event

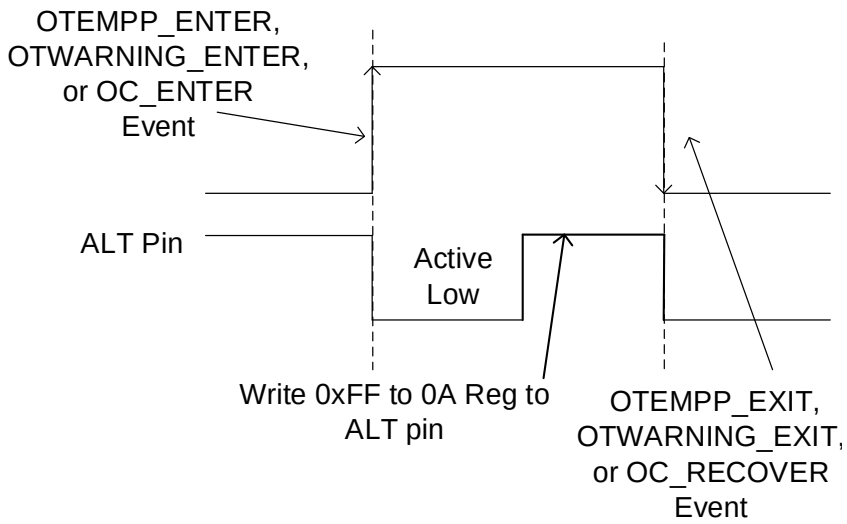

Figure 14: ALT Behavior of OTP, OT Warning, and OC Recovery

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. R1 can be calculated with Equation (1):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (1)$$

Figure 11 shows the feedback circuit.

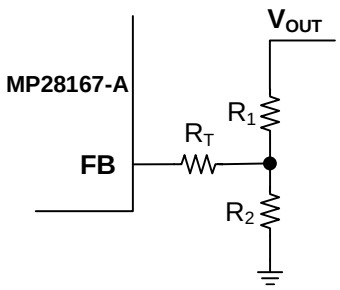

Figure 15: Feedback Network

Table 1 lists the recommended resistors and inductor values for common output voltages. If the I²C is not used to set the output voltage, it can be set using the resistors below.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	L (µH)
5	430	107	806	4.7
9	430	53.6	787	4.7
12	430	39.2	787	4.7
15	402	28.7	402	4.7
20	390	20.5	200	3.3

Selecting the Inductor

The inductor selection is based on which mode the device operates in. The inductance for buck mode (L_{BUCK}) can be estimated with Equation (2):

$$L_{BUCK} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (2)$$

Where ΔI_L is the peak-to-peak inductor ripple current, and is 30% to 50% of the maximum load current.

In boost mode, the inductor selection is based on limiting the peak-to-peak current ripple (ΔI_L) between 30% and 50% of the maximum input current.

The target inductance for boost mode can be estimated with Equation (3):

$$L_{BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (3)$$

Choosing a larger-value inductor reduces the ripple current but increases the physical size of the inductor. A larger-value inductor also reduces the converter's bandwidth by moving the right half-plane zero to lower frequencies. This tradeoff should be determined based on the application requirements.

In addition to the inductance value, the inductor must support the peak current to avoid saturation. The peak current can be calculated with Equation (4) and Equation (5) for buck and boost mode, respectively:

$$I_{PEAK-BUCK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{2 \times V_{IN(MAX)} \times f_{REQ} \times L} \quad (4)$$

$$I_{PEAK-BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{2 \times V_{OUT} \times f_{REQ} \times L} \quad (5)$$

Where η is the estimated efficiency of the MP28167-A.

For most applications, a 4.7µH inductor is recommended for 500kHz switching frequency applications, and a 3.3µH inductor is recommended for 750kHz switching frequency applications.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists recommended power inductors.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
Select family series (MPL-AL)	2.2µH to 4.7µH	MPS
MPL-AL6050-4R7	4.7µH	MPS
MPL-AL6050-3R3	3.3µH	MPS
MPL-AL5030-2R2	2.2µH	MPS

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Input and Output Capacitor Selection

It is recommended to use ceramic capacitors with an electrolytic capacitor at the input to filter the input ripple current and achieve stable operation.

Since the input capacitor absorbs the input switching current, it requires sufficient capacitance. For most applications, a 100µF electrolytic capacitor and a 22µF ceramic capacitor are sufficient.

The output capacitor stabilizes the DC output voltage. A sufficient capacitor value is recommended to limit the output voltage ripple. The minimum ceramic C_{OUT} should be 22µF x 5.

The input and output ceramic capacitors must be placed as close as possible to the device.

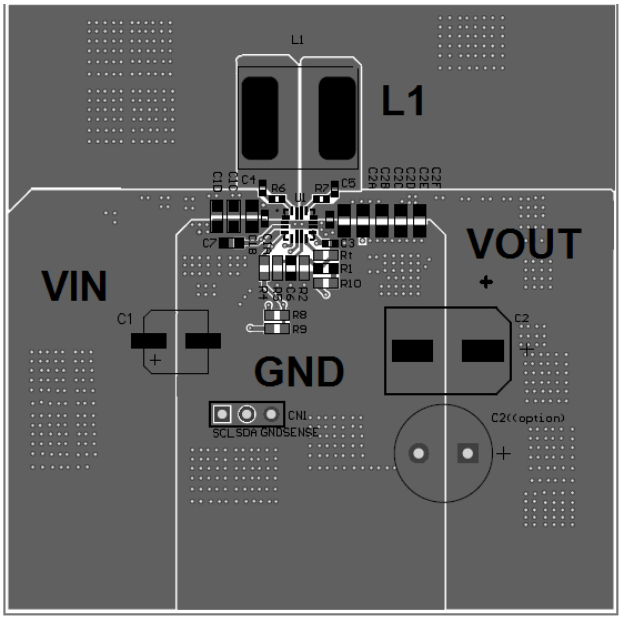
PCB Layout Guidelines (11)

Efficient PCB layout is critical for stable operation and thermal dissipation. For the best results, refer to Figure 16 and follow the guidelines below:

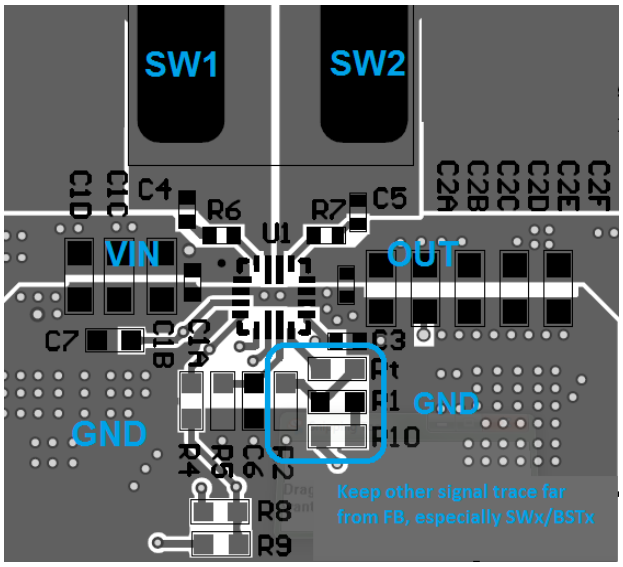
1. Place the ceramic C_{IN} and C_{OUT} capacitors close to the IC's VIN-to-GND and OUT-to-GND pins, respectively.
2. Use a large copper plane for PGND.
3. Add multiple vias to improve thermal dissipation.
4. Connect AGND to PGND.
5. Use short, direct, and wide traces to connect OUT.
6. Add vias under the IC and route the OUT trace on both PCB layers (highly recommended).
7. Use a large copper plane for SW1 and SW2.
8. Place the VCC decoupling capacitor as close to VCC as possible.
9. The FB trace requires special consideration. Use a GND copper to cover this trace, and route other signal traces far from FB, such as SWx/BSTx.

Note:

11) The recommended layout is based on the Typical Application Circuit (see Figure 17).



Top Layer



Close-Up of Layout

Figure 16: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

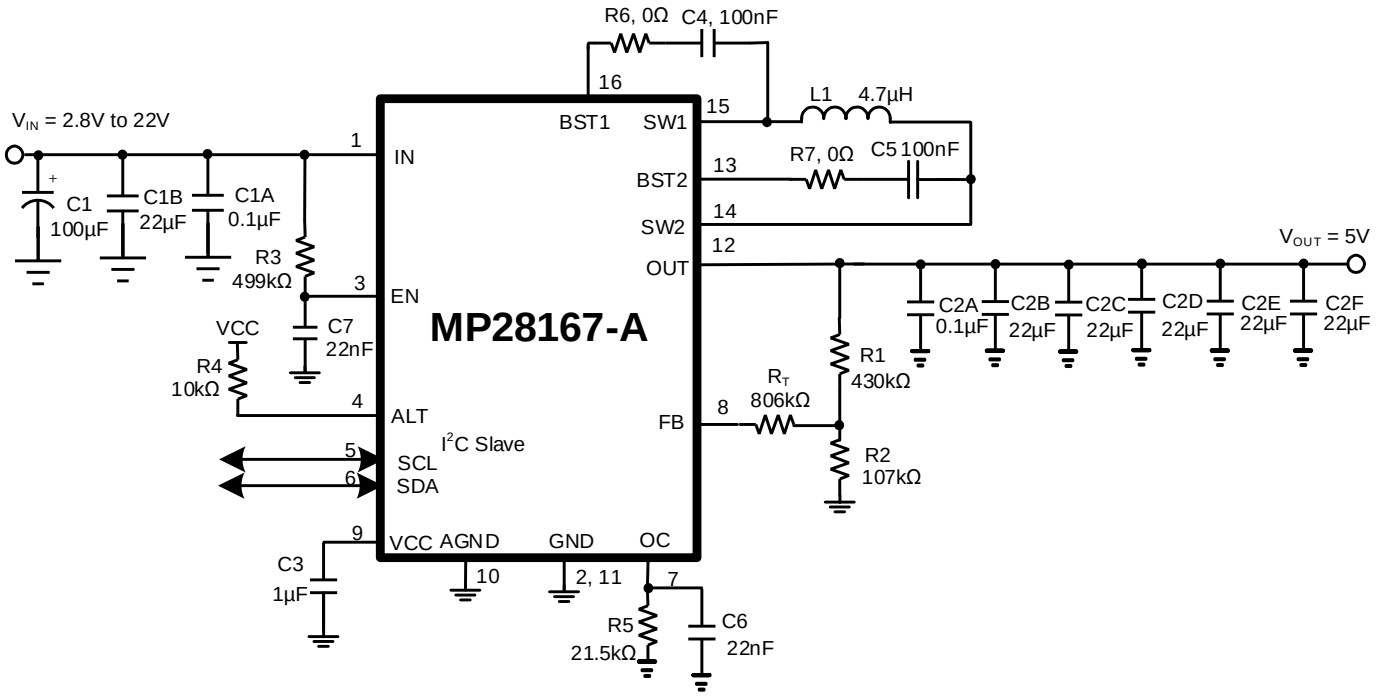

Figure 17: Typical Application Circuit for 5V V_{OUT}

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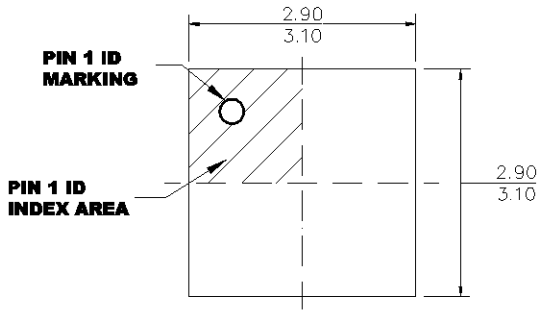
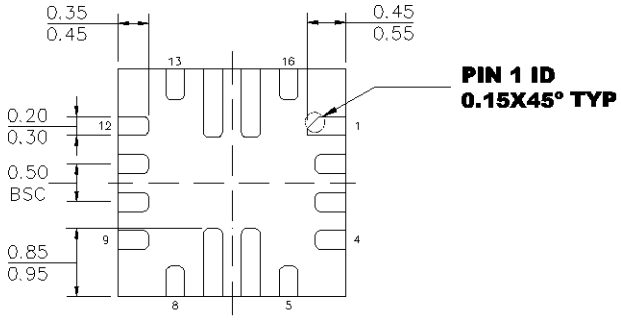
PACKAGE INFORMATION

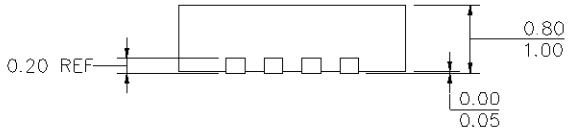
QFN-16 (3mmx3mm)



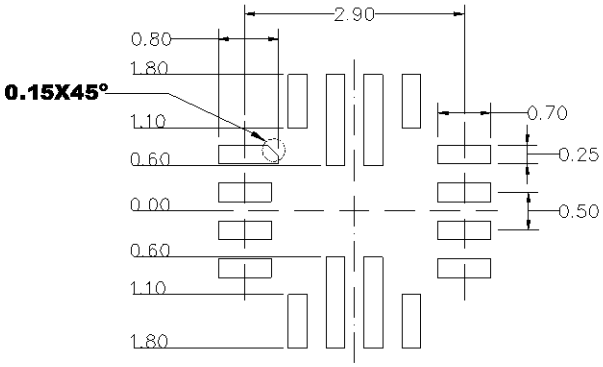
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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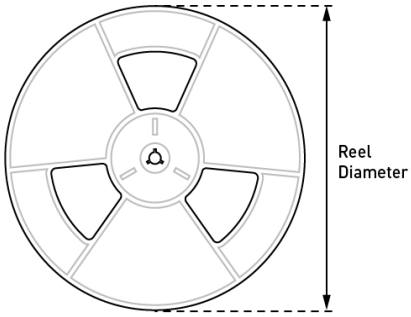
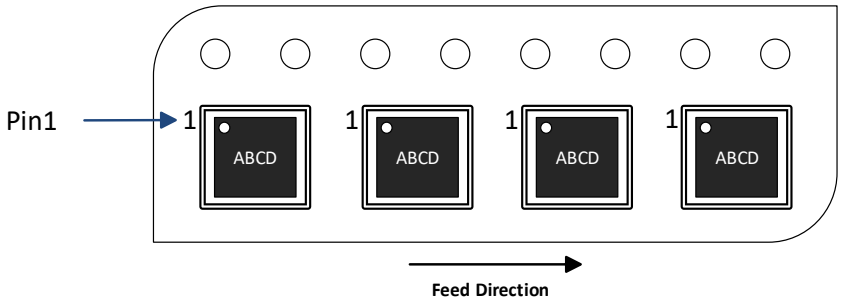
CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP28167GQ-A–Z	QFN-16 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

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