



# MPQ4321

## 42V Load Dump Tolerant, 1A, Ultra-Compact, Low Quiescent Current, Synchronous Step-Down Converter, AEC-Q100 Qualified

### DESCRIPTION

The MPQ4321 is a frequency-configurable (350kHz to 2.5MHz), synchronous, step-down switching converter with integrated internal high-side and low-side power MOSFETs. The device provides 1A of highly efficient output current with peak current mode control.

The wide 3.3V to 36V input range with 42V load dump tolerance accommodates a variety of step-down applications in automotive input environments. A 1 $\mu$ A shutdown mode quiescent current allows the device to be used in battery-powered applications.

High power conversion efficiency across the wide load range is achieved by scaling down the switching frequency under light-load conditions to reduce the switching and gate driving losses.

An open drain power good signal indicates that the output is within 94.5% to 105.5% of its nominal voltage.

Frequency foldback helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

A high-duty cycle and low-dropout mode are provided for automotive cold-crank conditions.

The MPQ4321 is available in a QFN-12 (2mmx3mm) package or a QFN-12 (3mmx4mm) package with wettable flanks.

### FEATURES

- Designed for Automotive Applications:
  - Survives 42V Load Dump
  - Supports 3.1V Cold Crank
  - Low-Dropout Mode
  - 1A of Continuous Output Current
  - Continuous Operation up to 36V
  - Operating Junction Temperature: -40°C to +150°C
  - 65ns Minimum On Time and 50ns Minimum Off Time
- Increases Battery Life:
  - 1 $\mu$ A Shutdown Supply Current
  - 20 $\mu$ A Sleep Mode Quiescent Current
  - Advanced Asynchronous Mode (AAM) Increases Efficiency under Light Loads
- High Performance for Improved Thermal Performance:
  - Integrated 70m $\Omega$  High-Side and 50m $\Omega$  Low-Side MOSFETs
- Optimized for EMC/EMI:
  - Frequency Spread Spectrum Modulation
  - Symmetric VIN Pinout
  - CISPR25 Class 5 Compliant
  - 350kHz to 2.5MHz Configurable Switching Frequency
  - MeshConnect™ Flip-Chip Package
- Additional Features:
  - Power Good Output
  - Hiccup Over-Current Protection (OCP)
  - Available in a QFN-12 (2mmx3mm) Package or a QFN-12 (3mmx4mm) Package with Wettable Flanks
  - Available in AEC-Q100 Grade-1

### APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver Assistance Systems
- Industrial Power Systems

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## TYPICAL APPLICATION

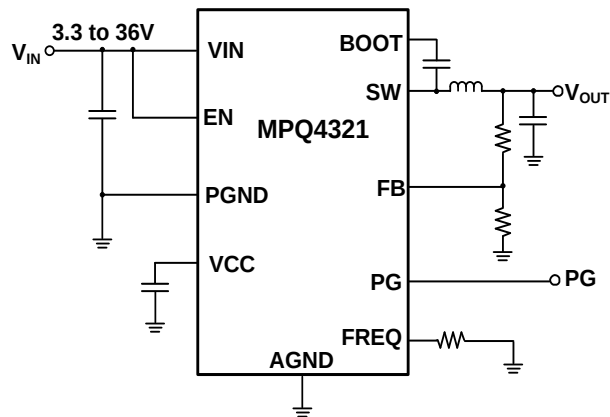


Figure 1: Adjustable Output

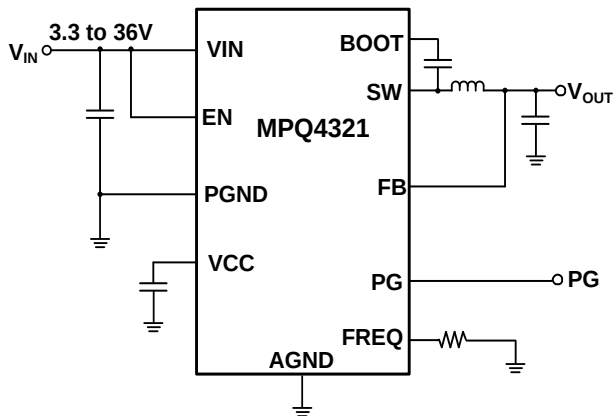
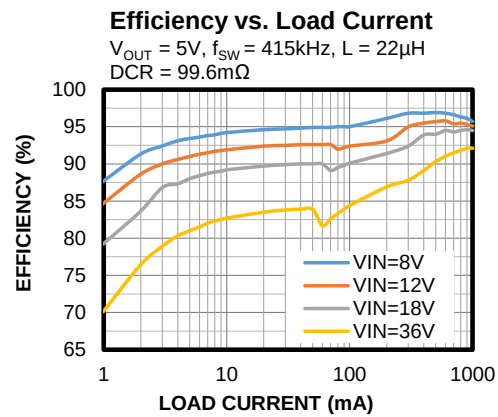


Figure 2: Fixed Output

## ORDERING INFORMATION

| Part Number* <sup>(1)</sup> | Package          | Top Marking | MSL Rating** |
|-----------------------------|------------------|-------------|--------------|
| MPQ4321GDE-AEC1***          | QFN-12 (2mmx3mm) | See Below   | 1            |
| MPQ4321GDE-5-AEC1***        | QFN-12 (2mmx3mm) | See Below   | 1            |
| MPQ4321GLE-AEC1***          | QFN-12 (3mmx4mm) | See Below   | 1            |

\* For Tape & Reel, add suffix -Z (e.g. MPQ4321GDE-AEC1-Z).

\*\*Moisture Sensitivity Level Rating

\*\*\*Wettable flank

**Note:**

1) Contact MPS for the details regarding additional versions with a fixed output.

## TOP MARKING (MPQ4321GDE-AEC1 and MPQ4321GDE-5-AEC1)

**BRJ**

**YWW**

**LLLL**

BRJ: Production code

Y: Year code

WW: Week code

LLLL: Lot number

## TOP MARKING (MPQ4321GLE-AEC1)

**MPYW**

**4321**

**LLL**

**E**

MP: MPS prefix

Y: Year code

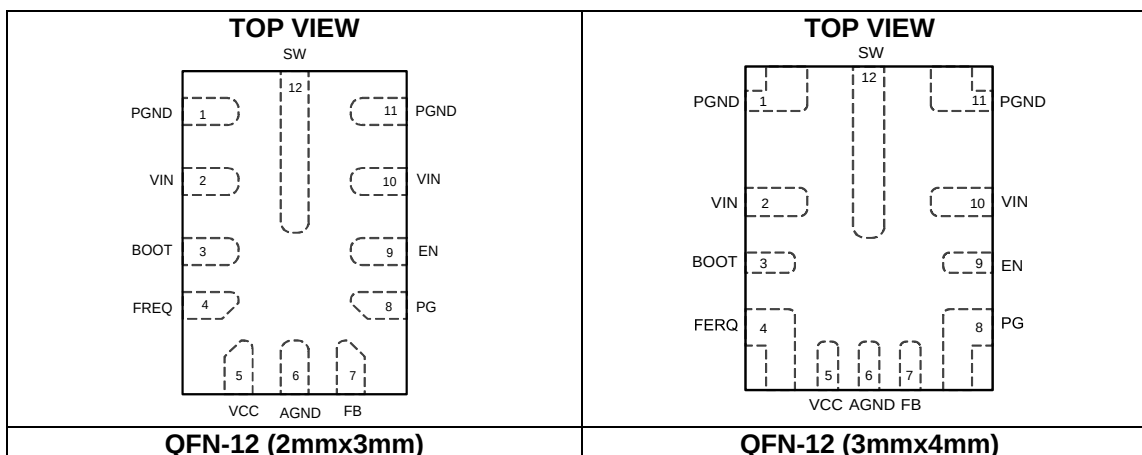
W: Week code

4321: Part number

LLL: Lot number

E: Wettable flank

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin # | Name | Description                                                                                                                                                                                                                                                                                                                                           |
|-------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 11 | PGND | <b>Power ground.</b>                                                                                                                                                                                                                                                                                                                                  |
| 2, 10 | VIN  | <b>Input supply.</b> VIN supplies power to all the internal control circuitry, as well as the power switch connected to SW. The two VIN pins are connected internally. To minimize switching spikes, place a decoupling capacitor from each VIN pin to ground, as close to each VIN pin as possible.                                                  |
| 3     | BOOT | <b>Bootstrap.</b> BOOT is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between BOOT and SW.                                                                                                                                                                                                  |
| 4     | FREQ | <b>Switching frequency configuration.</b> Connect a resistor from this pin to ground to set the switching frequency.                                                                                                                                                                                                                                  |
| 5     | VCC  | <b>Bias supply.</b> VCC is the output of the internal regulator that supplies power to the internal control circuit and gate drivers. Place a decoupling capacitor (greater than 1 $\mu$ F) from ground, and place the capacitor close to VCC.                                                                                                        |
| 6     | AGND | <b>Analog ground.</b>                                                                                                                                                                                                                                                                                                                                 |
| 7     | FB   | <b>Feedback input.</b> FB is the negative input of the error amplifier, which is typically 0.8V. If this device has a fixed output, connect this pin directly to the output voltage. If this device has an adjustable output, connect this pin to the middle point the external feedback divider, between output and AGND, to set the output voltage. |
| 8     | PG   | <b>Power good output.</b> The output of PG is open drain. If PG is used, attached PG to a power source using a pull-up resistor. PG goes high if the output voltage is within 94.5% to 105.5% of the nominal voltage. PG goes low if the output voltage is above 107% or below 93% of the nominal voltage. Float the PG pin if it is not used.        |
| 9     | EN   | <b>Enable.</b> Pull EN below the specified threshold (about 0.85V) to shut the chip down. Pull EN above the specified threshold (about 1.02V) to enable the chip. There is no internal pull-up or pull-down resistor connected to EN. Do not float the EN pin.                                                                                        |
| 12    | SW   | <b>Switch node.</b> SW is the source of the high-side MOSFET, and the drain of the low-side MOSFET.                                                                                                                                                                                                                                                   |

## ABSOLUTE MAXIMUM RATINGS <sup>(2)</sup>

|                                                                    |                                             |
|--------------------------------------------------------------------|---------------------------------------------|
| VIN, EN.....                                                       | 42V for automotive load dump <sup>(3)</sup> |
| VIN, EN.....                                                       | -0.3V to +40V                               |
| SW.....                                                            | -0.3V to $V_{IN(MAX)} + 0.3V$               |
| BOOT.....                                                          | $V_{SW} + 5.5V$                             |
| FREQ, VCC.....                                                     | 5.5V                                        |
| All other pins.....                                                | -0.3V to +6V                                |
| Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(4)</sup> |                                             |
| QFN-12 (2mmx3mm) .....                                             | 3.5W <sup>(8)</sup>                         |
| QFN-12 (3mmx4mm) .....                                             | 3.6W <sup>(9)</sup>                         |
| Operating junction temperature .....                               | +150°C                                      |
| Lead temperature.....                                              | +260°C                                      |
| Storage temperature.....                                           | -65°C to +150°C                             |

## Electrostatic Discharge (ESD) Rating

|                                 |                          |
|---------------------------------|--------------------------|
| Human body model (HBM) .....    | Class 2 <sup>(5)</sup>   |
| Charged device model (CDM)..... | Class C2b <sup>(6)</sup> |

## Recommended Operating Conditions

|                                         |                              |
|-----------------------------------------|------------------------------|
| Supply voltage ( $V_{IN}$ ).....        | 3.3V to 36V                  |
| Minimum $V_{IN}$ for start-up .....     | 3.9V                         |
| Minimum $V_{IN}$ after start-up .....   | 3.1V                         |
| Output Voltage ( $V_{OUT}$ ).....       | 0.8V to $0.95 \times V_{IN}$ |
| Operating junction temp ( $T_J$ ) ..... |                              |
| .....                                   | -40°C to +150°C              |

## Thermal Resistance $\theta_{JA}$ $\theta_{JC}$

|                     |           |           |
|---------------------|-----------|-----------|
| QFN-12 (2mmx3mm)    |           |           |
| JESD51-7 .....      | 60.....   | 7.3 ..... |
| EVQ4321-D-00A ..... | 35.5..... | 3.5.....  |
| QFN-12 (3mmx4mm)    |           |           |
| JESD51-7.....       | 50.....   | 7.5.....  |
| EVQ4321-L-00A ..... | 34.3..... | 3.7.....  |

### Notes:

- 2) The absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
- 3) Refer to ISO16750.
- 4) The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J(MAX)$ , the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D (MAX) = (T_J (MAX) - T_A) / \theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 5) Per AEC-Q100-002.
- 6) Per AEC-Q100-011.
- 7) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of  $\theta_{JC}$  shows the thermal resistance from the junction-to-case bottom.
- 8) Measured on MPS MPQ4321GDE standard EVB, 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB. The value of  $\theta_{JC}$  shows the thermal resistance from the junction-to-case top.
- 9) Measured on MPS MPQ4321GLE standard EVB, 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB. The value of  $\theta_{JC}$  shows the thermal resistance from the junction-to-case top.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                              | Symbol                 | Condition                                                                                        | Min  | Typ      | Max  | Units      |
|--------------------------------------------------------|------------------------|--------------------------------------------------------------------------------------------------|------|----------|------|------------|
| <b>Input Supply</b>                                    |                        |                                                                                                  |      |          |      |            |
| $V_{IN}$ under-voltage lockout rising threshold        | $V_{INUVLO\_RISING}$   |                                                                                                  | 3.4  | 3.65     | 3.9  | V          |
| $V_{IN}$ under-voltage lockout falling threshold       | $V_{INUVLO\_FALLING}$  |                                                                                                  | 2.6  | 2.9      | 3.1  | V          |
| $V_{IN}$ under-voltage lockout hysteresis              | $V_{INUVLO\_HYS}$      |                                                                                                  |      | 750      |      | mV         |
| $V_{IN}$ quiescent current                             | $I_Q$                  | $V_{FB} = 0.85V$ , no load, $T_J = 25^{\circ}C$                                                  |      | 20       | 28   | $\mu A$    |
|                                                        |                        | $V_{FB} = 0.85V$ , no load, $T_J = -40^{\circ}C$ to $+125^{\circ}C$ <sup>(10)</sup>              |      |          | 34   | $\mu A$    |
|                                                        |                        | $V_{FB} = 0.85V$ , no load, $T_J = -40^{\circ}C$ to $+150^{\circ}C$                              |      |          | 80   | $\mu A$    |
| $V_{IN}$ quiescent current (switching) <sup>(10)</sup> | $I_{Q\_SWITCHING}$     | Switching, $R_{FB1} = 1M\Omega$ , $R_{FB2} = 191k\Omega$ , no load                               |      | 25       |      | $\mu A$    |
| $V_{IN}$ shutdown current                              | $I_{SHDN}$             | $V_{EN} = 0V$                                                                                    |      | 1        | 10   | $\mu A$    |
| $V_{IN}$ over-voltage protection rising threshold      | $V_{INOV\_P\_RISING}$  |                                                                                                  | 35.5 | 37.5     | 40   | V          |
| $V_{IN}$ over-voltage protection falling threshold     | $V_{INOV\_P\_FALLING}$ |                                                                                                  | 34.5 | 36.5     | 39   | V          |
| $V_{IN}$ over-voltage protection hysteresis            | $V_{INOV\_P\_HYS}$     |                                                                                                  |      | 1        |      | V          |
| <b>Switches and Frequency</b>                          |                        |                                                                                                  |      |          |      |            |
| Switching frequency without frequency spread spectrum  | $f_{SW}$               | $R_{FREQ} = 86.6k\Omega$                                                                         | 332  | 415      | 498  | kHz        |
|                                                        |                        | $R_{FREQ} = 34.8k\Omega$                                                                         | 900  | 1000     | 1100 | kHz        |
|                                                        |                        | $R_{FREQ} = 15k\Omega$                                                                           | 1980 | 2200     | 2420 | kHz        |
| Frequency spread spectrum span                         |                        |                                                                                                  |      | $\pm 10$ |      | %          |
| Frequency spread spectrum modulation frequency         |                        |                                                                                                  |      | 15       |      | kHz        |
| Minimum on time <sup>(10)</sup>                        | $t_{ON\_MIN}$          |                                                                                                  |      | 65       | 80   | ns         |
| Minimum off time <sup>(10)</sup>                       | $t_{OFF\_MIN}$         |                                                                                                  |      | 50       | 70   | ns         |
| Maximum duty cycle                                     | $D_{MAX}$              |                                                                                                  | 98   | 99.5     |      | %          |
| Switch leakage current                                 | $I_{SW\_LKG}$          | $V_{EN} = 0V$ , $V_{SW} = V_{BOOT} = 0V$ or $V_{IN}$ ( $T_J = 25^{\circ}C$ )                     |      | 0.01     | 1    | $\mu A$    |
|                                                        |                        | $V_{EN} = 0V$ , $V_{SW} = V_{BOOT} = 0V$ or $V_{IN}$ ( $T_J = -40^{\circ}C$ to $+150^{\circ}C$ ) |      | 0.01     | 5    | $\mu A$    |
| HS switch on resistance                                | $R_{ON\_HS}$           | $V_{BOOT} - V_{SW} = 5V$                                                                         |      | 70       | 130  | m $\Omega$ |
| LS switch on resistance                                | $R_{ON\_LS}$           | $V_{CC} = 5V$                                                                                    |      | 50       | 90   | m $\Omega$ |
| <b>EN</b>                                              |                        |                                                                                                  |      |          |      |            |
| EN rising threshold                                    | $V_{EN\_RISING}$       |                                                                                                  | 0.97 | 1.02     | 1.07 | V          |
| EN falling threshold                                   | $V_{EN\_FALLING}$      |                                                                                                  | 0.8  | 0.85     | 0.9  | V          |
| EN threshold hysteresis                                | $V_{EN\_HYS}$          |                                                                                                  |      | 170      |      | mV         |

# ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>EN</sub> = 2V, T<sub>J</sub> = -40°C to +150°C, typical values are at T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameter                                                        | Symbol                    | Condition                                     | Min   | Typ   | Max   | Units |
|------------------------------------------------------------------|---------------------------|-----------------------------------------------|-------|-------|-------|-------|
| Output and Regulation                                            |                           |                                               |       |       |       |       |
| FB voltage<br>(adjustable output version)                        | V <sub>FB</sub>           | T <sub>J</sub> = 25°C                         | 0.794 | 0.8   | 0.806 | V     |
|                                                                  |                           | T <sub>J</sub> = -40°C to +150°C              | 0.790 | 0.8   | 0.810 | V     |
| FB input current                                                 | I <sub>FB</sub>           | adjustable output                             |       | 0     | 100   | nA    |
|                                                                  |                           | fixed output                                  |       | 3.8   |       | μA    |
| V <sub>OUT</sub> discharge current                               | I <sub>DISCHARGE</sub>    | V <sub>EN</sub> = 0V, V <sub>OUT</sub> = 0.3V | 2     | 4     |       | mA    |
| Output voltage accuracy of 5V fixed output version               | V <sub>OUT</sub>          | T <sub>J</sub> = 25°C                         | 4925  | 5000  | 5075  | mV    |
|                                                                  |                           | T <sub>J</sub> = -40°C to +150°C              | 4900  | 5000  | 5100  | mV    |
| BOOT                                                             |                           |                                               |       |       |       |       |
| BOOT-SW refresh rising                                           | V <sub>BOOT_RISING</sub>  |                                               |       | 2.5   | 2.9   | V     |
| BOOT-SW refresh falling                                          | V <sub>BOOT_FALLING</sub> |                                               |       | 2.3   | 2.7   | V     |
| BOOT-SW refresh hysteresis                                       | V <sub>BOOT_HYS</sub>     |                                               |       | 0.2   |       | V     |
| Soft Start and VCC                                               |                           |                                               |       |       |       |       |
| Soft-start time                                                  | t <sub>SS</sub>           | EN High to SS finishes                        | 3     | 5     | 7     | ms    |
| VCC voltage                                                      | V <sub>CC</sub>           | I <sub>VCC</sub> = 0A                         | 4.7   | 5     | 5.3   | V     |
| VCC regulation                                                   |                           | I <sub>VCC</sub> = 30mA                       |       | 1     |       | %     |
| VCC current Limit                                                | I <sub>LIMIT_VCC</sub>    | V <sub>CC</sub> = 4V                          | 50    | 70    |       | mA    |
| PG                                                               |                           |                                               |       |       |       |       |
| PG rising threshold<br>(V <sub>FB</sub> / V <sub>REF</sub> )     | PG <sub>VTH_RISING</sub>  | V <sub>OUT</sub> rising, adjustable output    | 93    | 94.5  | 96    | %     |
|                                                                  |                           | V <sub>OUT</sub> rising, fixed output         | 93    | 94.5  | 96.5  |       |
|                                                                  |                           | V <sub>OUT</sub> falling, adjustable output   | 104   | 105.5 | 107   |       |
|                                                                  |                           | V <sub>OUT</sub> falling, fixed output        | 104   | 105.5 | 108   |       |
| PG falling threshold<br>(V <sub>FB</sub> / V <sub>REF</sub> )    | PG <sub>VTH_FALLING</sub> | V <sub>OUT</sub> falling, adjustable output   | 91.5  | 93    | 94.5  |       |
|                                                                  |                           | V <sub>OUT</sub> falling, fixed output        | 91.5  | 93    | 95    |       |
|                                                                  |                           | V <sub>OUT</sub> rising, adjustable output    | 105.5 | 107   | 108.5 |       |
|                                                                  |                           | V <sub>OUT</sub> rising, fixed output         | 105.5 | 107   | 109.5 |       |
| PG threshold hysteresis<br>(V <sub>FB</sub> / V <sub>REF</sub> ) | PG <sub>VTH_HYS</sub>     |                                               |       | 1.5   |       |       |
| PG output voltage low                                            | V <sub>PG_LOW</sub>       | I <sub>SINK</sub> = 1mA                       |       | 0.1   | 0.3   | V     |
| PG rising deglitch time                                          | t <sub>PG_R</sub>         |                                               |       | 70    |       | μs    |
| PG falling deglitch time                                         | t <sub>PG_F</sub>         |                                               |       | 60    |       | μs    |

## ELECTRICAL CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                   | Symbol          | Condition        | Min   | Typ  | Max   | Units       |
|---------------------------------------------|-----------------|------------------|-------|------|-------|-------------|
| <b>Protections</b>                          |                 |                  |       |      |       |             |
| HS peak current limit                       | $I_{LIMIT\_HS}$ | Duty cycle = 20% | 1.5   | 2    | 2.6   | A           |
| LS valley current limit                     | $I_{LIMIT\_LS}$ |                  | 1     | 1.5  | 2     | A           |
| ZCD current                                 | $I_{ZCD}$       |                  | -0.05 | 0.05 | +0.15 | A           |
| Thermal shutdown <sup>(10)</sup>            | $T_{SD}$        |                  | 160   | 175  | 185   | $^{\circ}C$ |
| Thermal shutdown hysteresis <sup>(10)</sup> | $T_{SD\_HYS}$   |                  |       | 20   |       | $^{\circ}C$ |

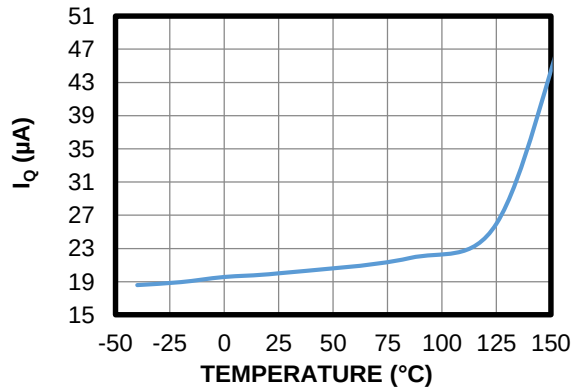
**Note:**

10) Not tested in production. Guaranteed by design and characterization.

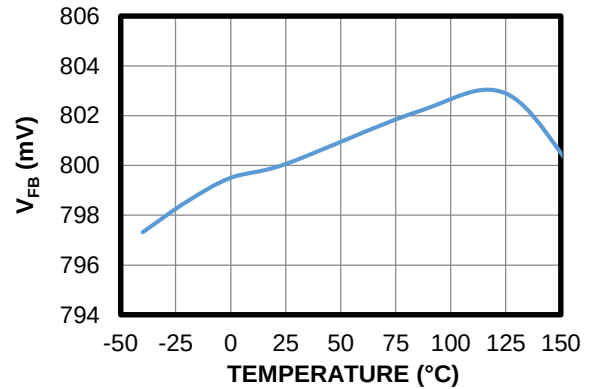
## TYPICAL CHARACTERISTICS

$V_{IN} = 12V$ , unless otherwise noted.

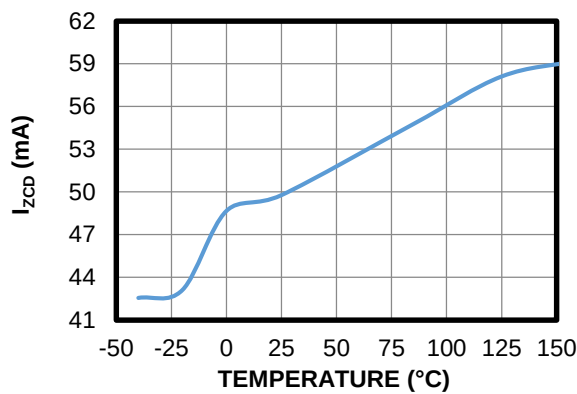
$I_Q$  vs. Temperature



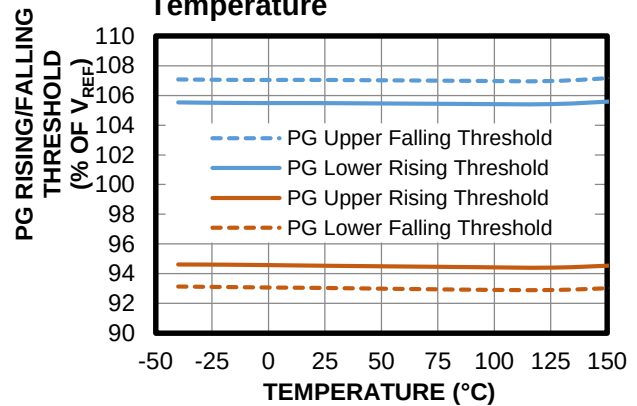
$V_{FB}$  vs. Temperature



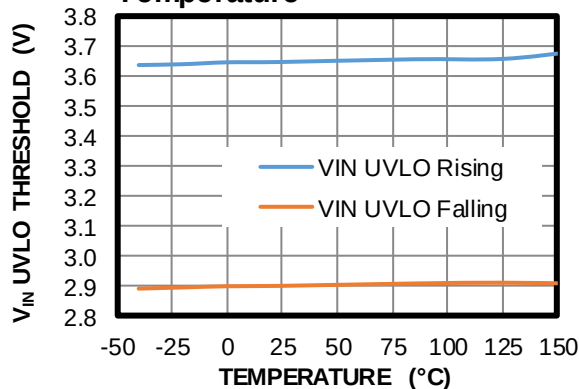
$I_{ZCD}$  vs. Temperature



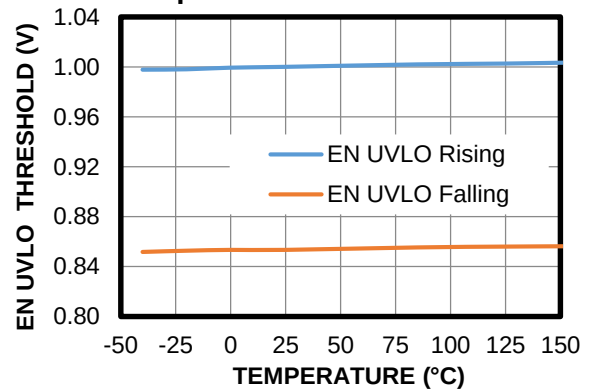
PG Rising/Falling Threshold vs. Temperature



$V_{IN}$  UVLO Threshold vs. Temperature

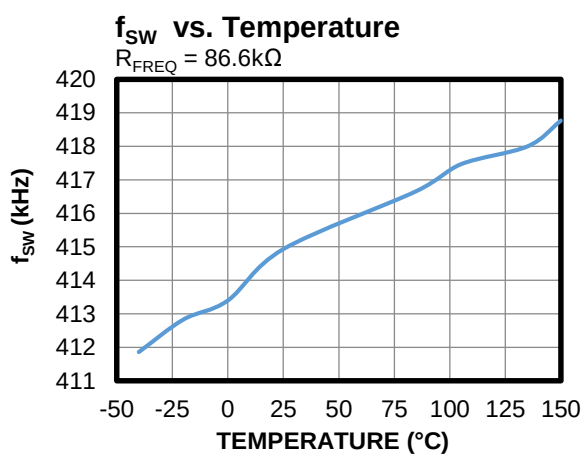
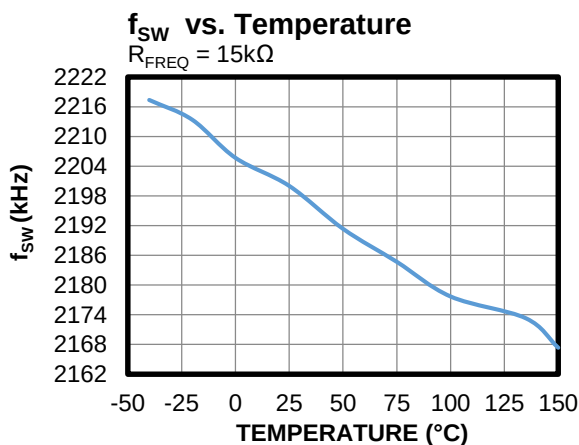
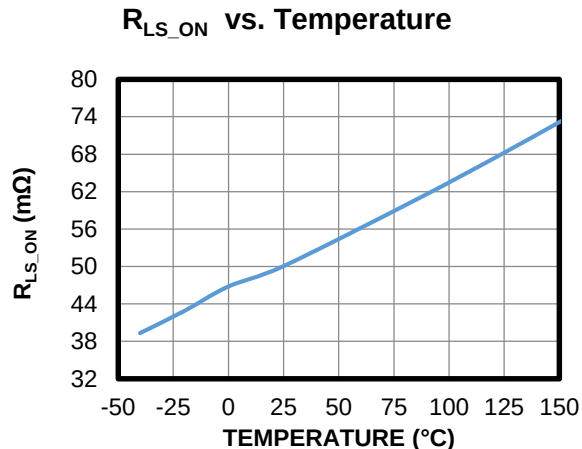
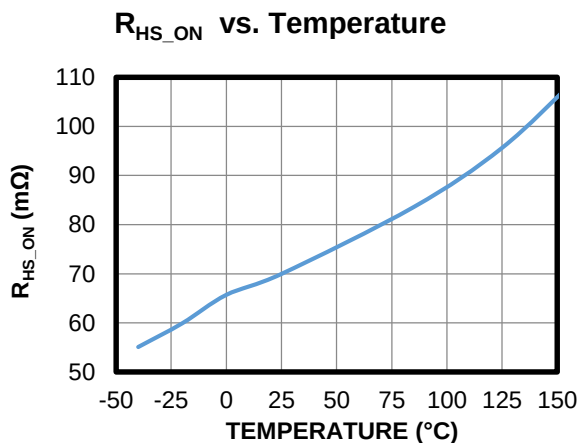
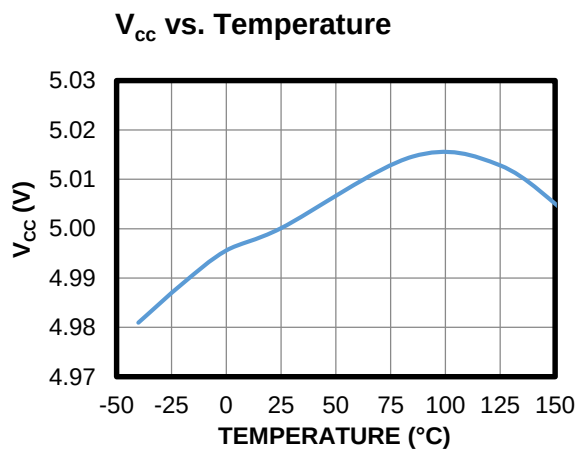
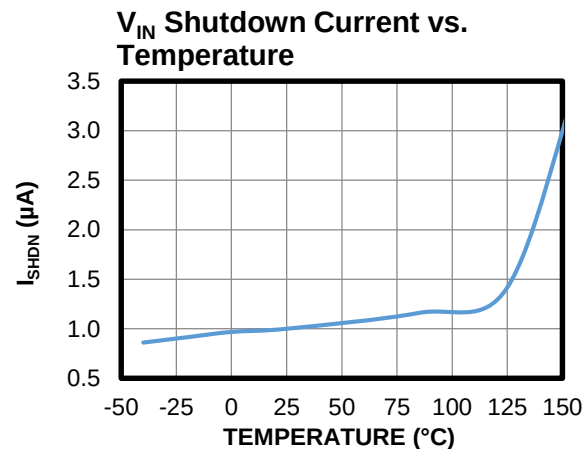


EN UVLO Threshold vs. Temperature



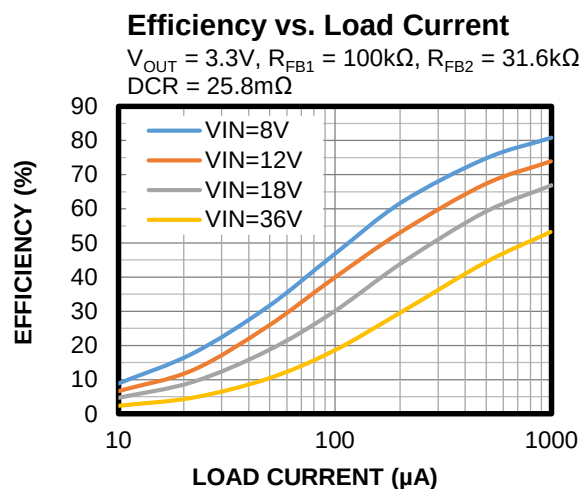
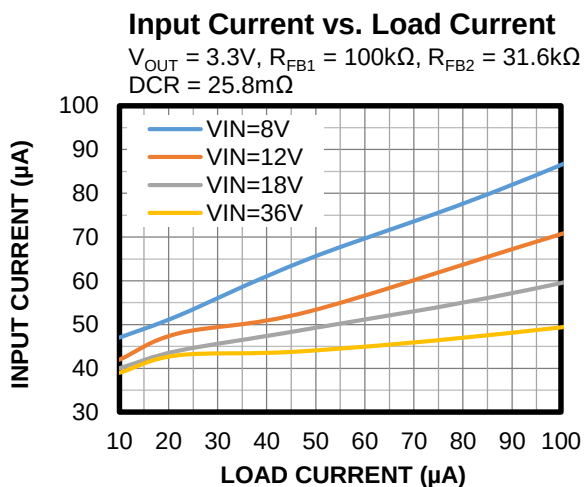
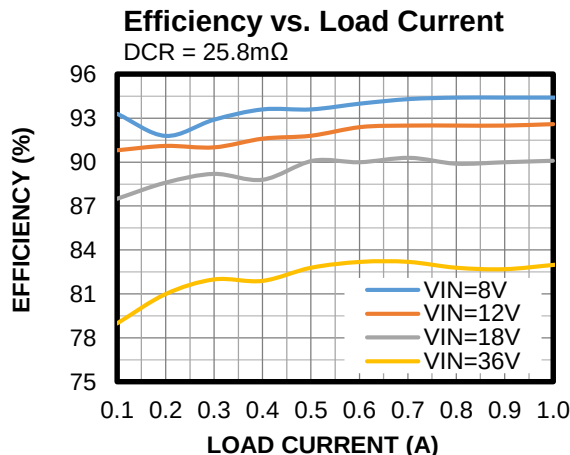
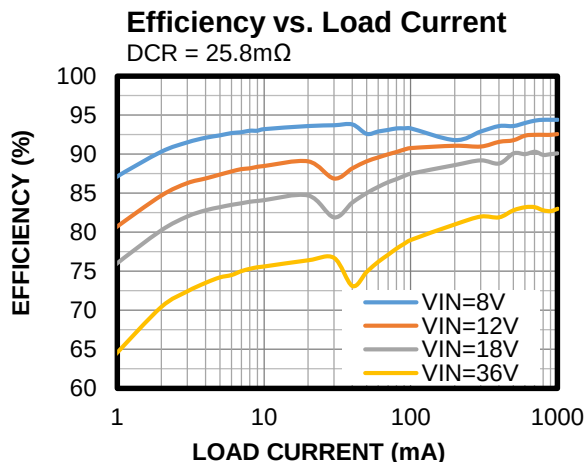
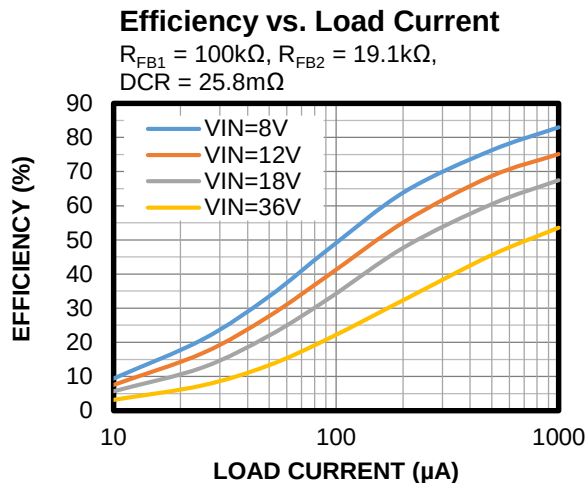
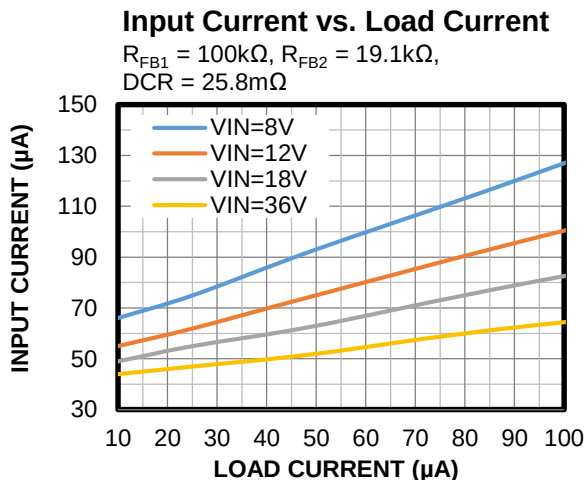
# TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ , unless otherwise noted.



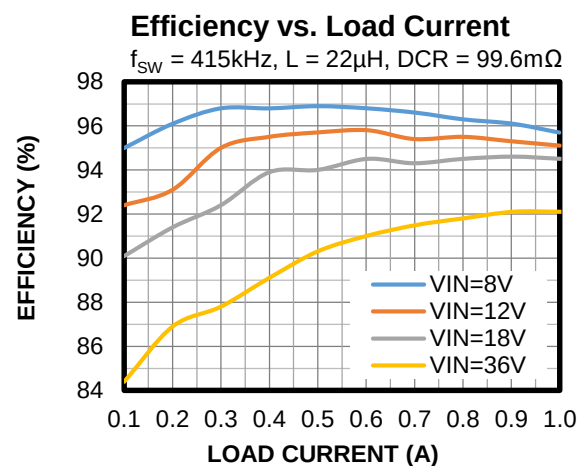
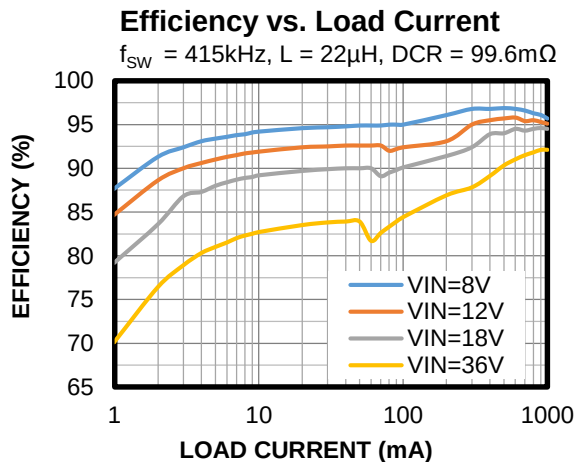
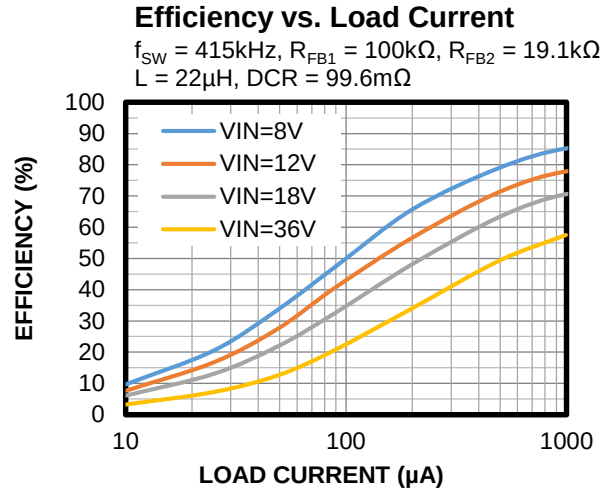
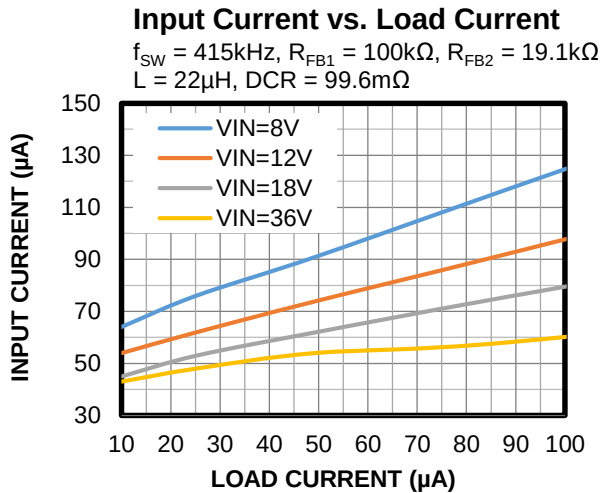
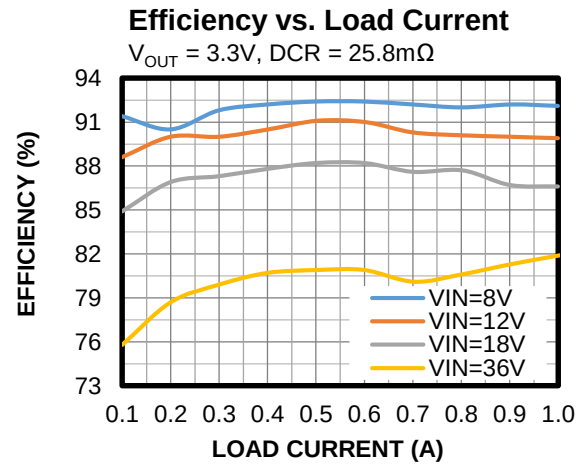
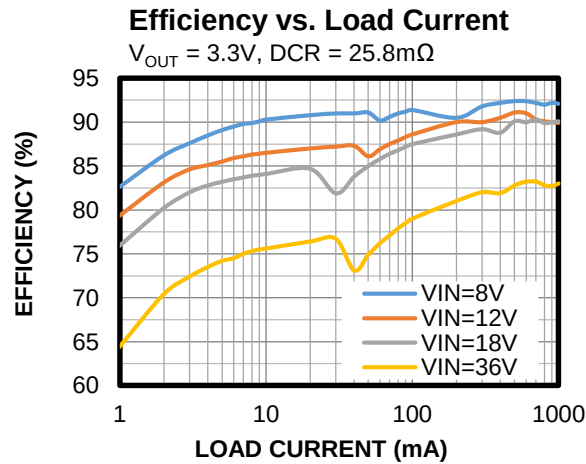
# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

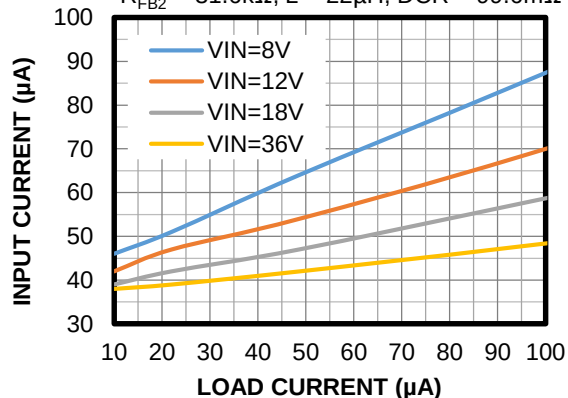


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

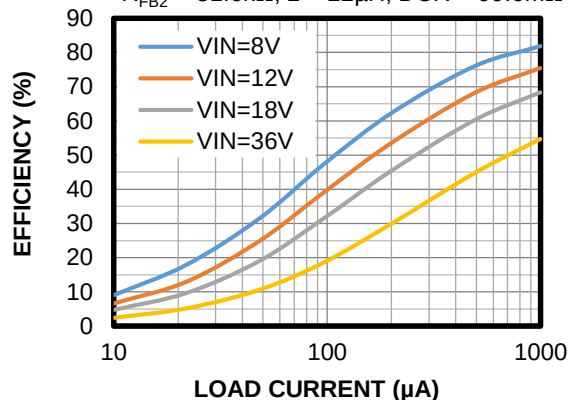
## Input Current vs. Load Current

$V_{OUT} = 3.3V$ ,  $f_{SW} = 415kHz$ ,  $R_{FB1} = 100k$   
 $R_{FB2} = 31.6k\Omega$ ,  $L = 22\mu H$ ,  $DCR = 99.6m\Omega$



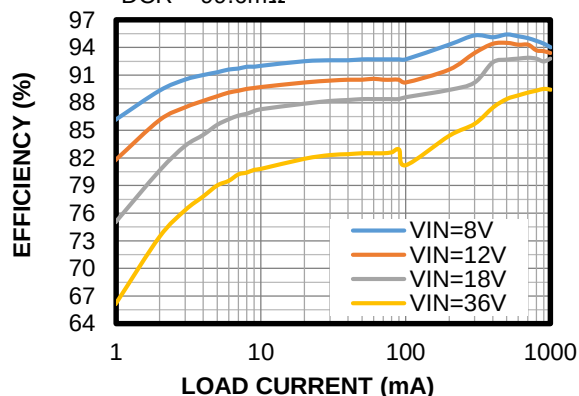
## Efficiency vs. Load Current

$V_{OUT} = 3.3V$ ,  $f_{SW} = 415kHz$ ,  $R_{FB1} = 100k$   
 $R_{FB2} = 31.6k\Omega$ ,  $L = 22\mu H$ ,  $DCR = 99.6m\Omega$



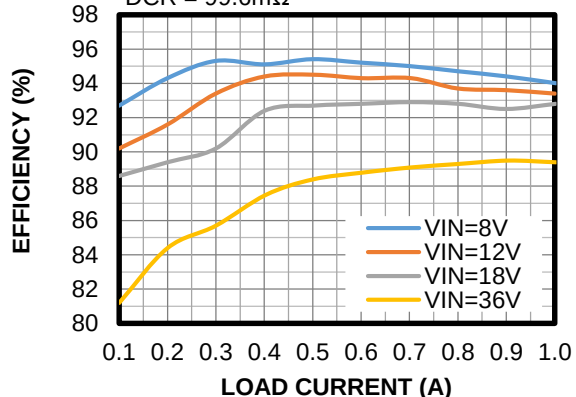
## Efficiency vs. Load Current

$V_{OUT} = 3.3V$ ,  $f_{SW} = 415kHz$ ,  $L = 22\mu H$   
 $DCR = 99.6m\Omega$



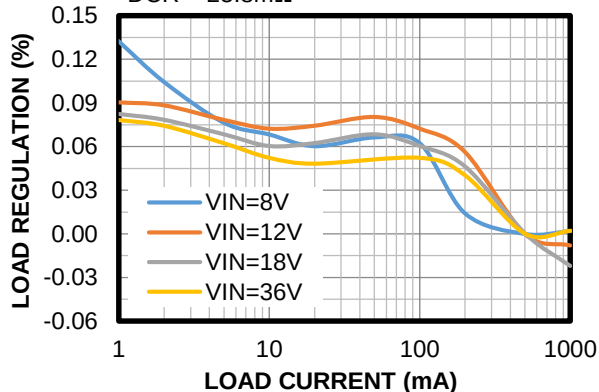
## Efficiency vs. Load Current

$V_{OUT} = 3.3V$ ,  $f_{SW} = 415kHz$ ,  $L = 22\mu H$   
 $DCR = 99.6m\Omega$



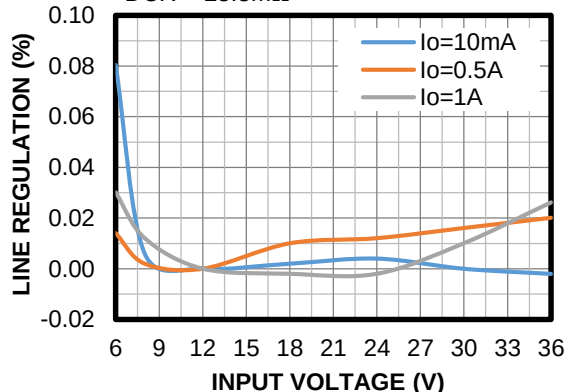
## Load Regulation

$DCR = 25.8m\Omega$



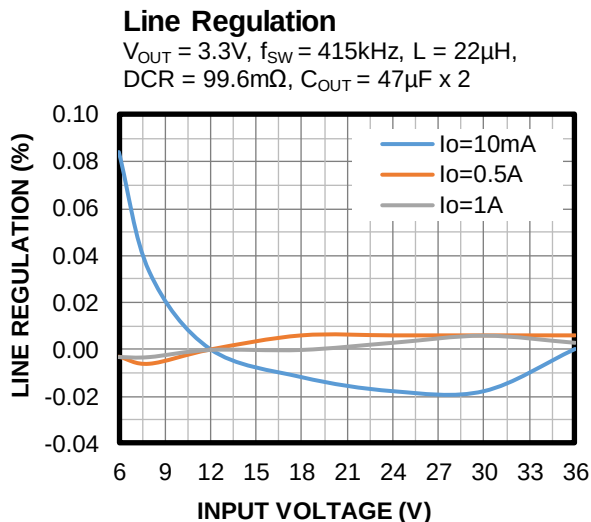
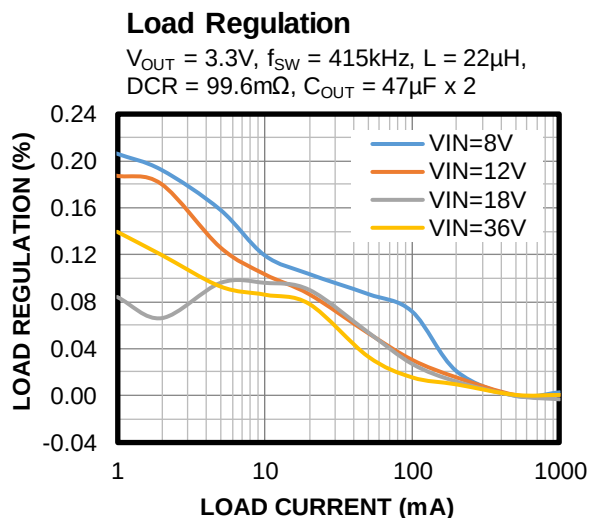
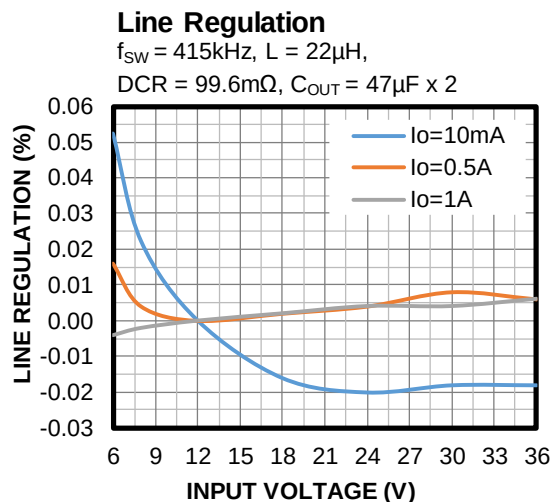
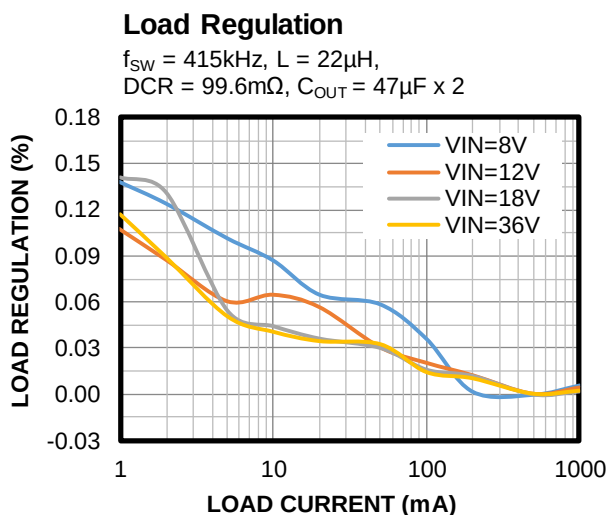
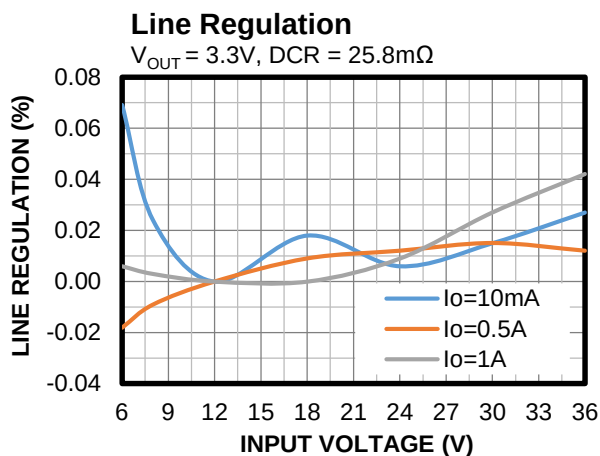
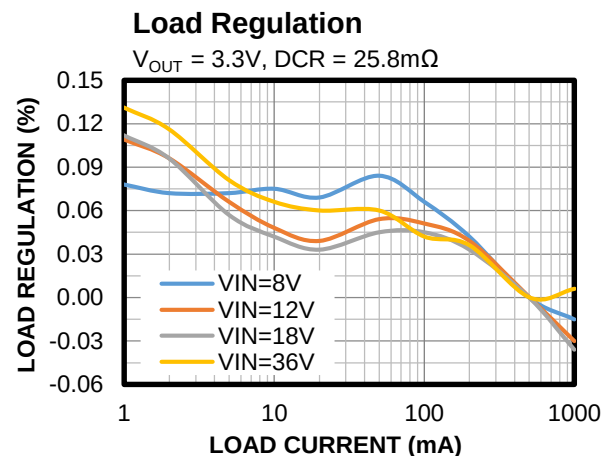
## Line Regulation

$DCR = 25.8m\Omega$



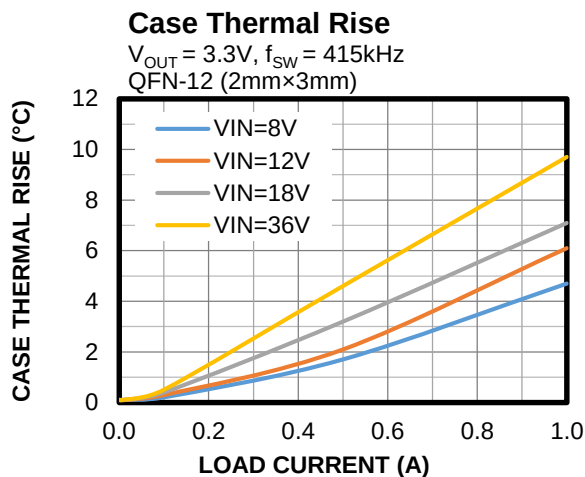
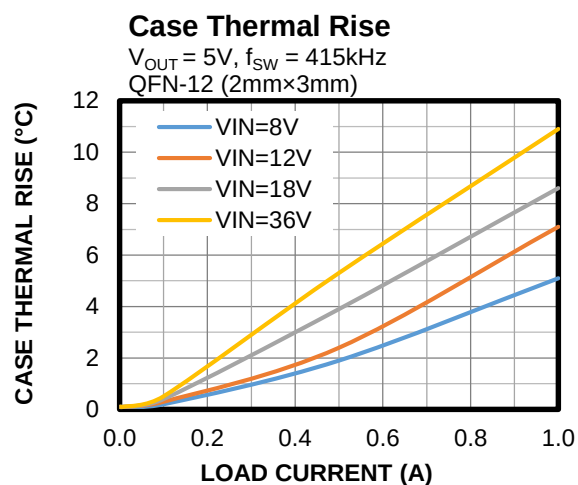
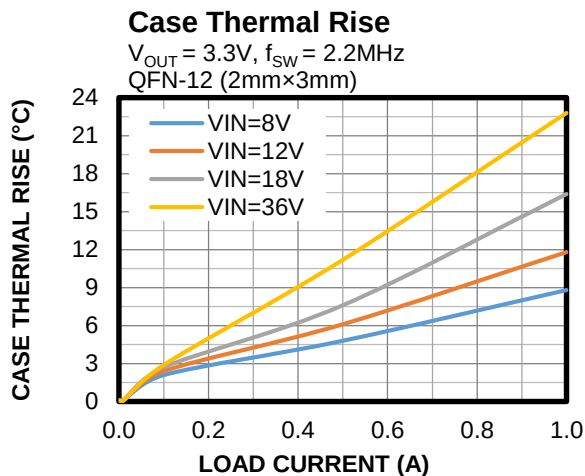
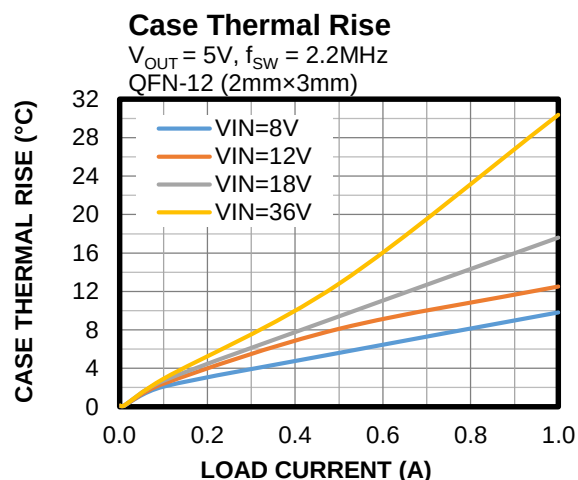
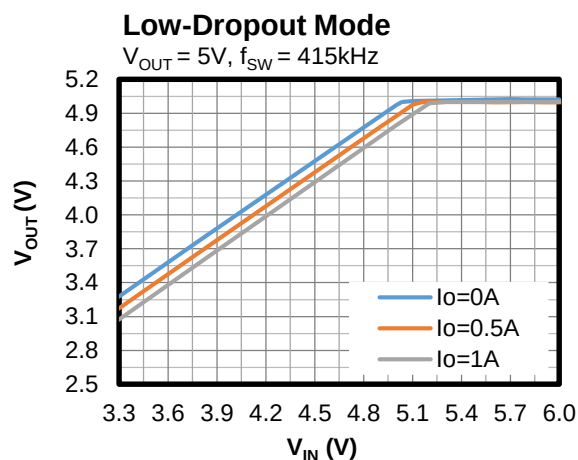
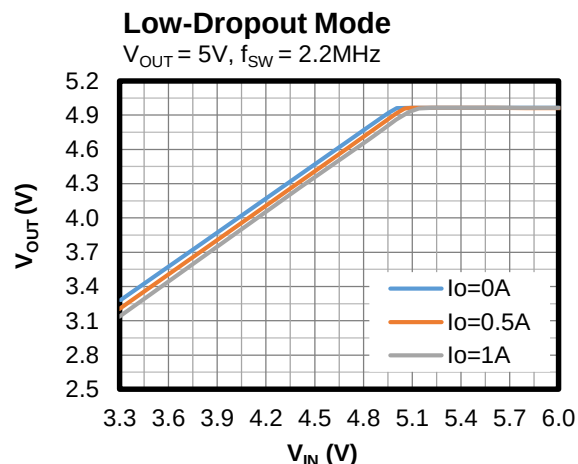
# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



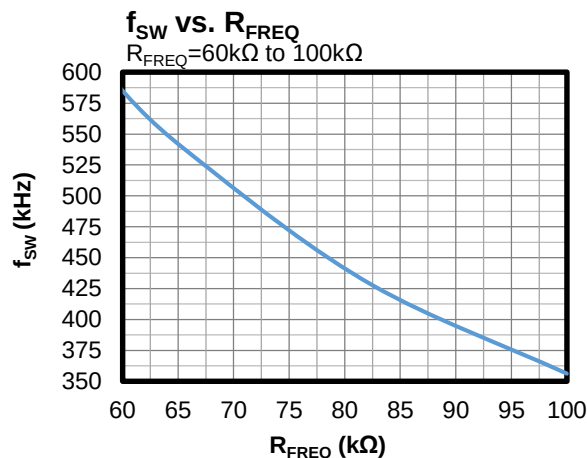
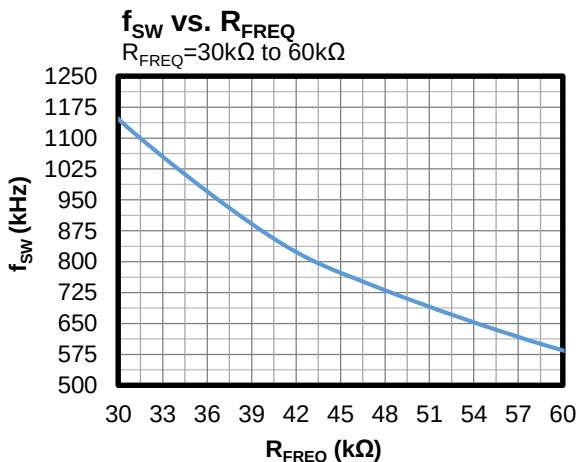
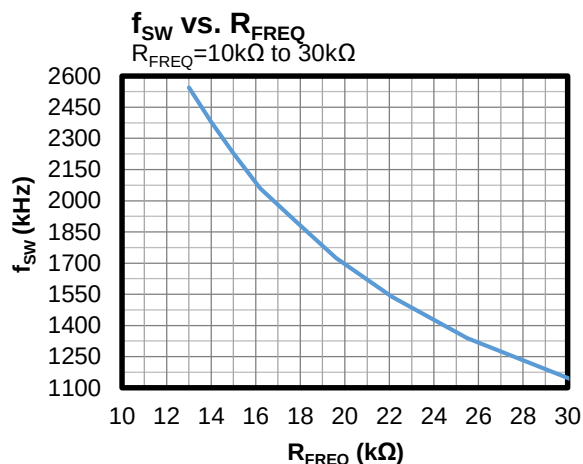
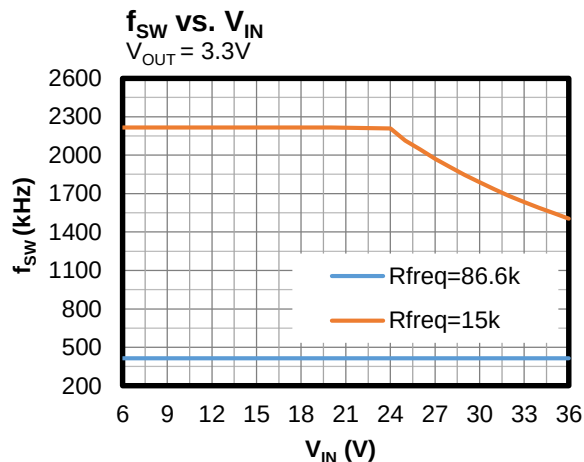
# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

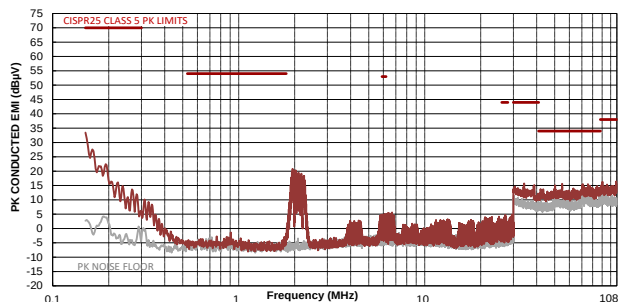


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.<sup>(11)</sup>

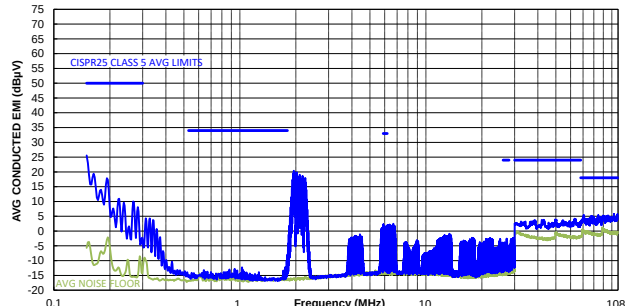
### CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



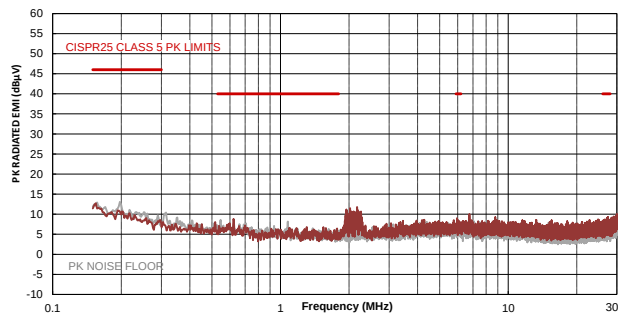
### CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



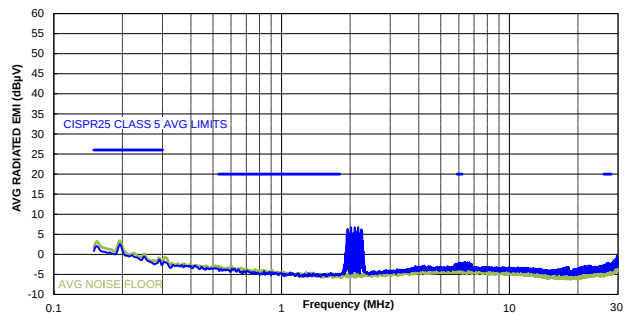
### CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



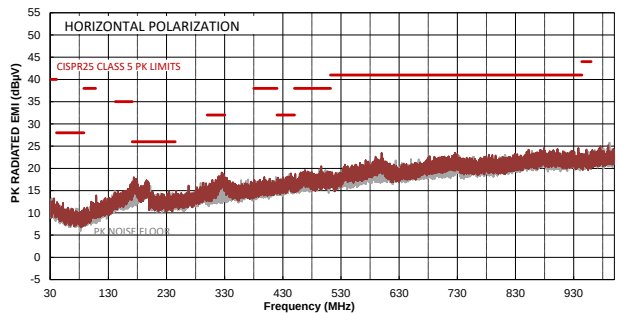
### CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



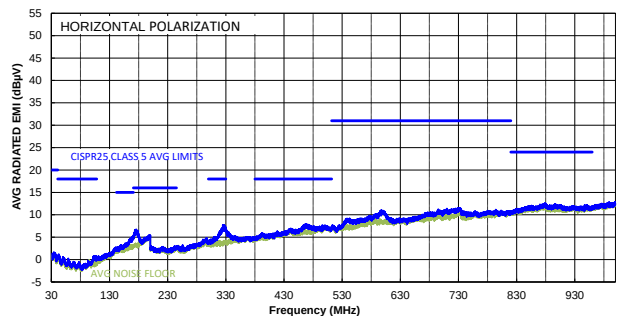
### CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



### CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

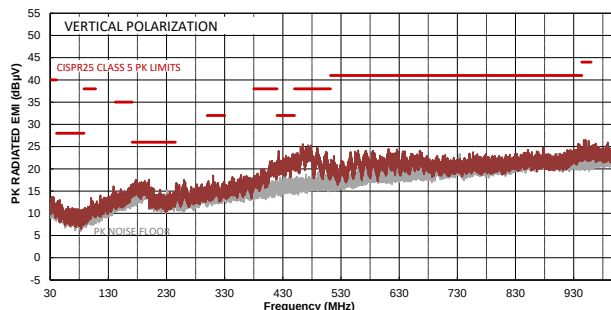


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.<sup>(11)</sup>

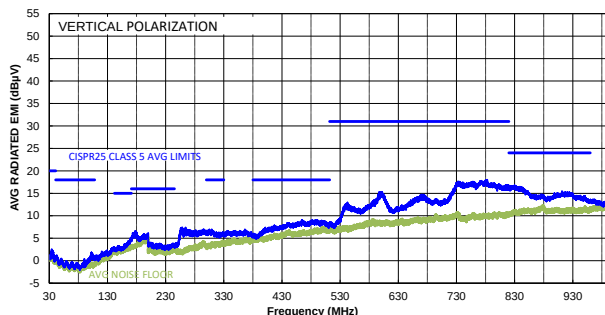
### CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



### CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



#### Note:

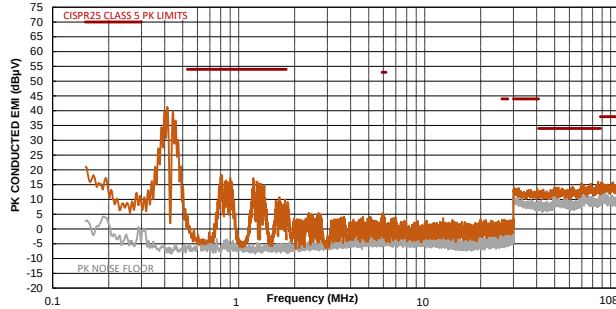
11) The EMC test results are based on the application circuit with EMI filters (see Figure 16 on page 38).

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 415kHz$ ,  $L = 22\mu H$ ,  $C_{OUT} = 47\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.<sup>(12)</sup>

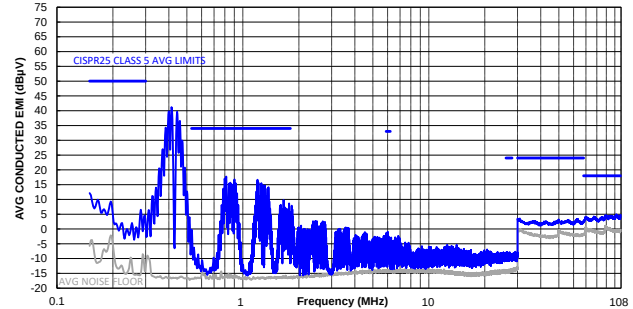
### CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



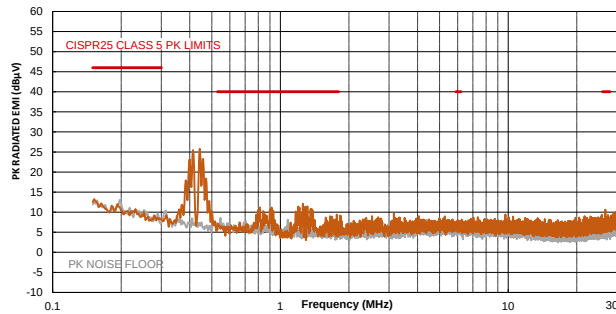
### CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



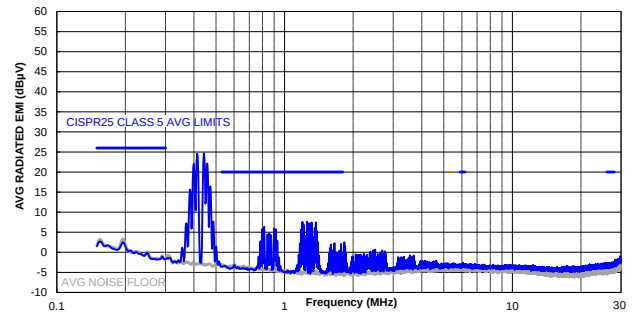
### CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



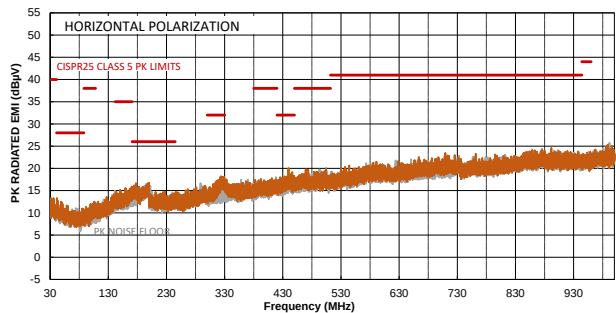
### CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



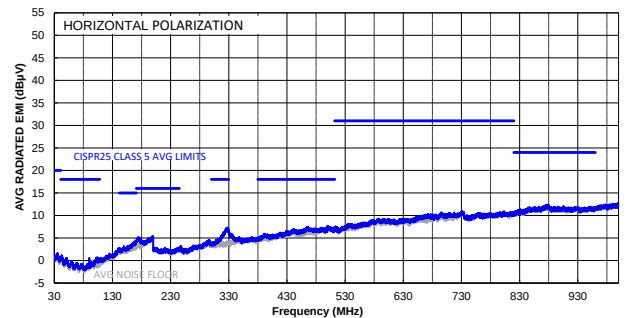
### CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



### CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

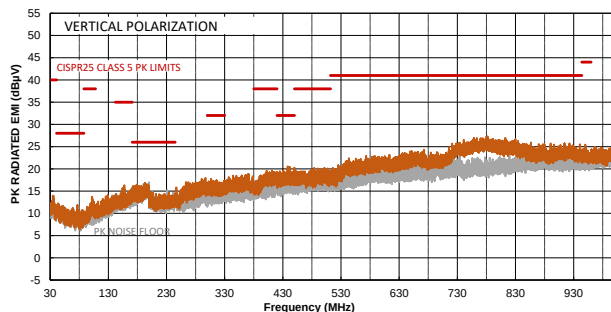


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 415kHz$ ,  $L = 22\mu H$ ,  $C_{OUT} = 47\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.<sup>(12)</sup>

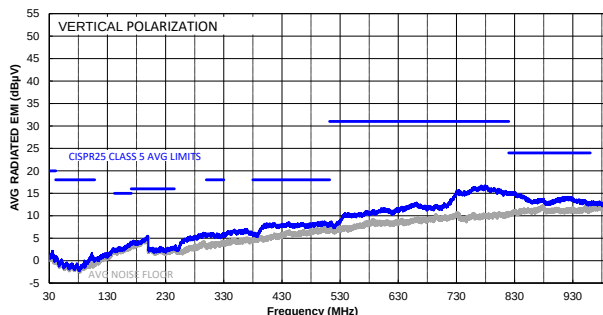
### CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



### CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



#### Note:

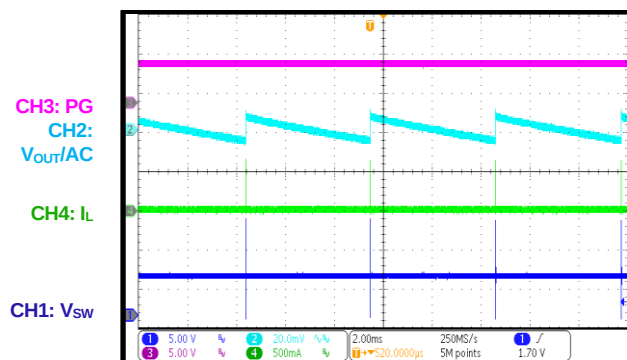
12) The EMC test results are based on the application circuit with EMI filters (see Figure 17 on page 39).

# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

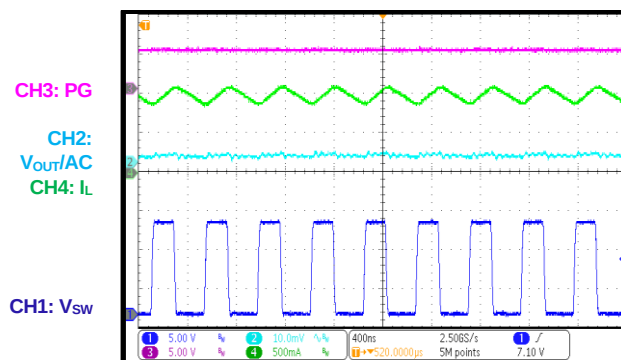
## Steady State

$I_{OUT} = 0A$



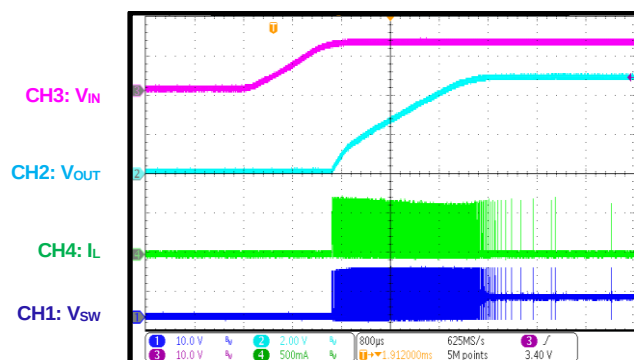
## Steady State

$I_{OUT} = 1A$



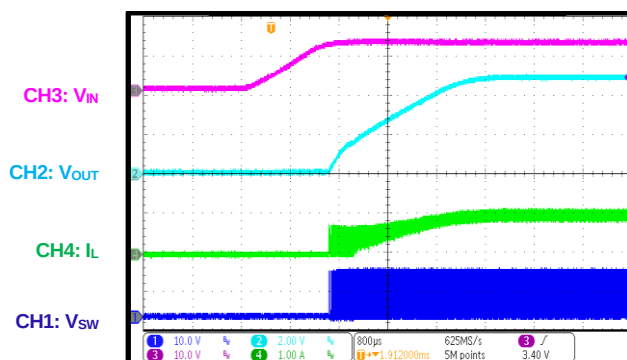
## Start-up through VIN

$I_{OUT} = 0A$



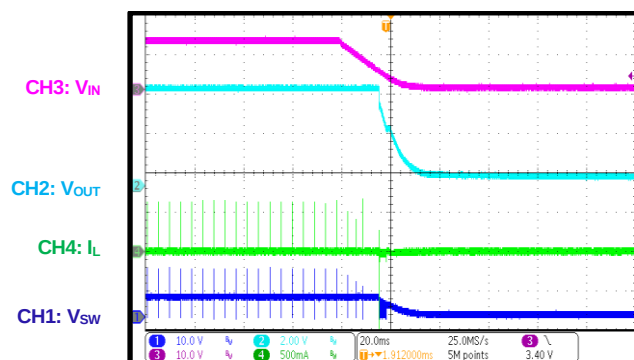
## Start-up through VIN

$I_{OUT} = 1A$



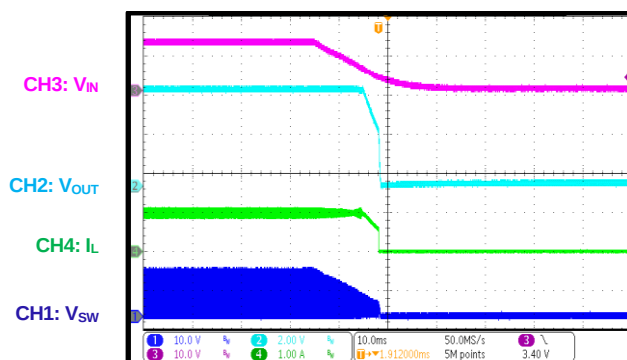
## Shutdown through VIN

$I_{OUT} = 0A$



## Shutdown through VIN

$I_{OUT} = 1A$

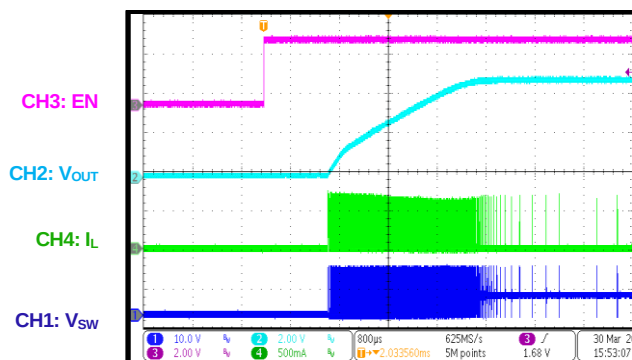


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

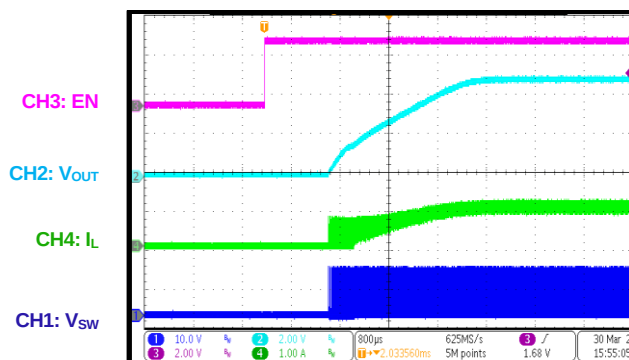
**Start-up through EN**

$I_{OUT} = 0A$



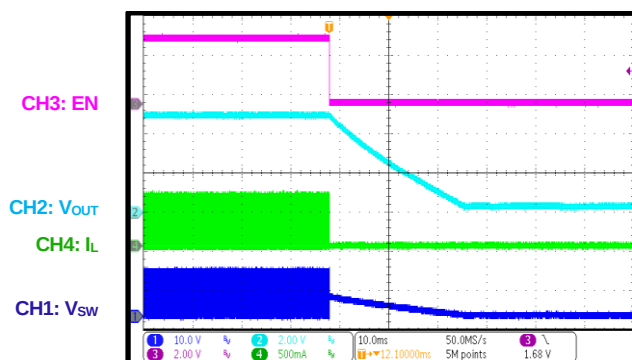
**Start-up through EN**

$I_{OUT} = 1A$



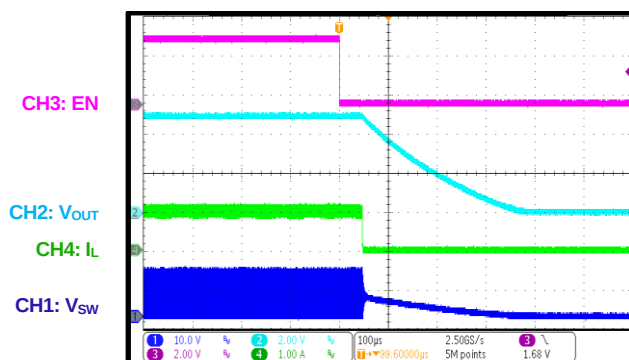
**Shutdown through EN**

$I_{OUT} = 0A$



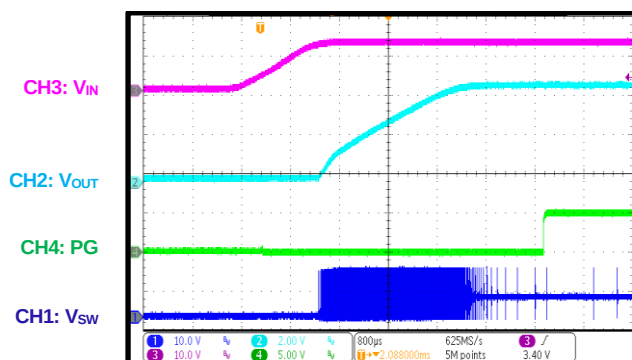
**Shutdown through EN**

$I_{OUT} = 1A$



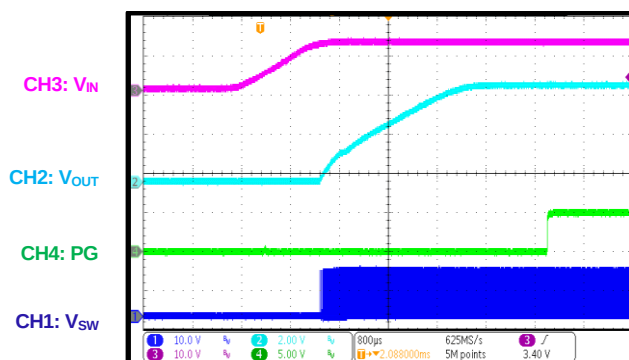
**PG in Start-up through VIN**

$I_{OUT} = 0A$



**PG in Start-up through VIN**

$I_{OUT} = 1A$

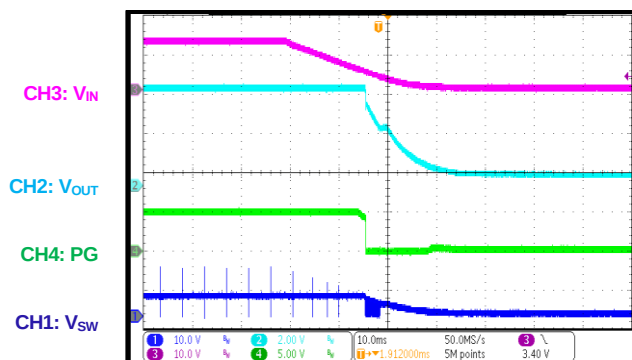


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

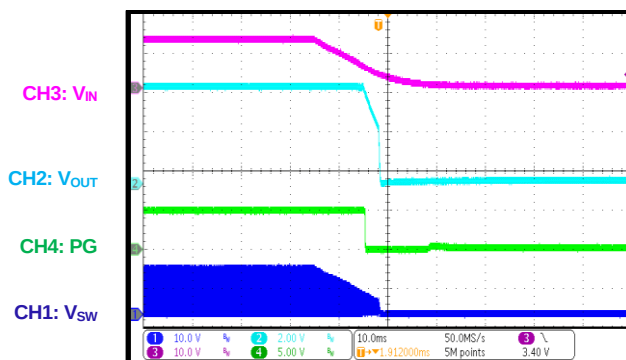
**PG in Shutdown through VIN**

$I_{OUT} = 0A$



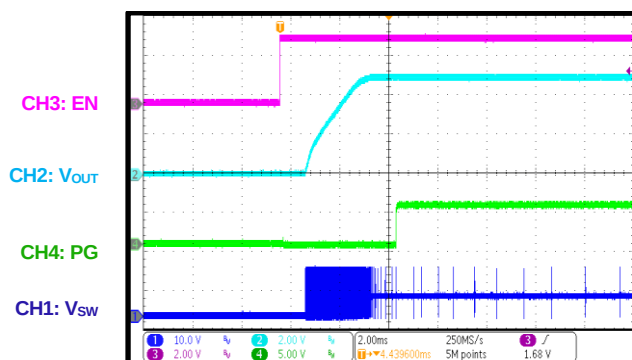
**PG in Shutdown through VIN**

$I_{OUT} = 1A$



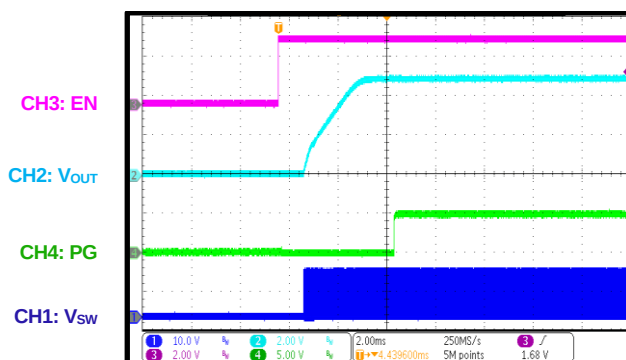
**PG in Start-up through EN**

$I_{OUT} = 0A$



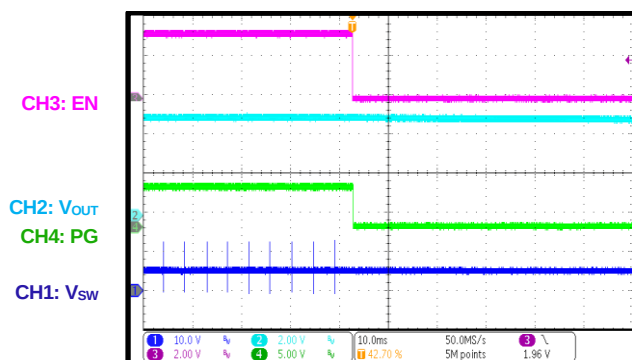
**PG in Start-up through EN**

$I_{OUT} = 1A$



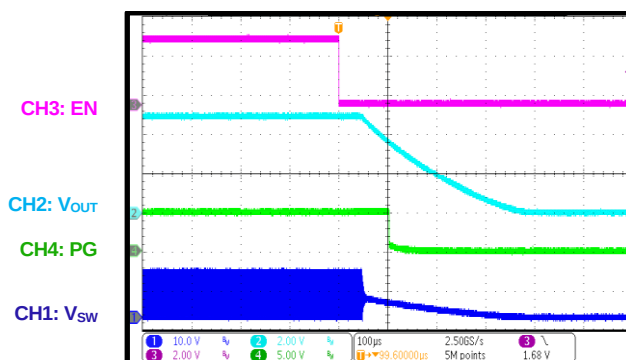
**PG in Shutdown through EN**

$I_{OUT} = 0A$



**PG in Shutdown through EN**

$I_{OUT} = 1A$

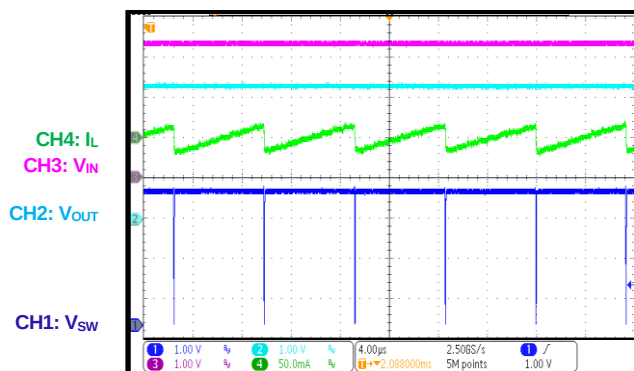


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

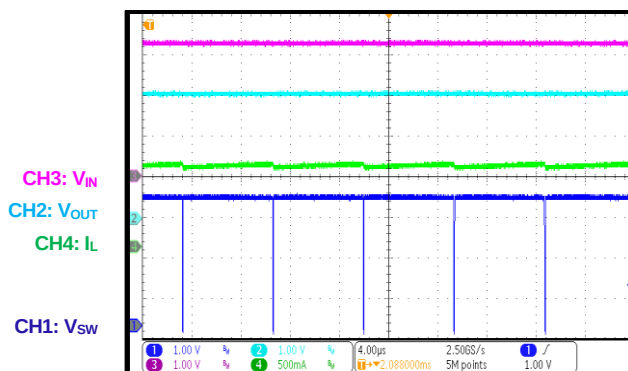
## Low-Dropout Mode

$I_{OUT} = 0A$ ,  $V_{IN} = 3.3V$



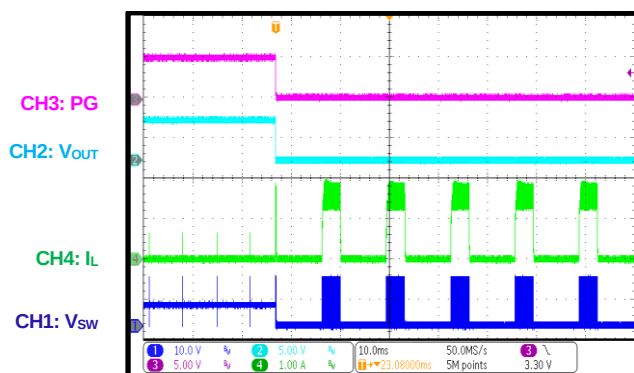
## Low-Dropout Mode

$I_{OUT} = 1A$ ,  $V_{IN} = 3.3V$



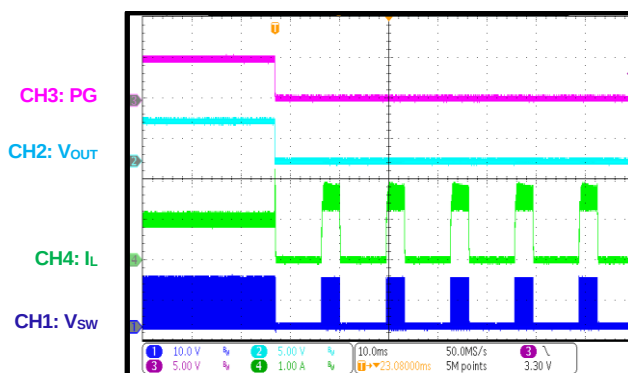
## SCP Entry

$I_{OUT} = 0A$



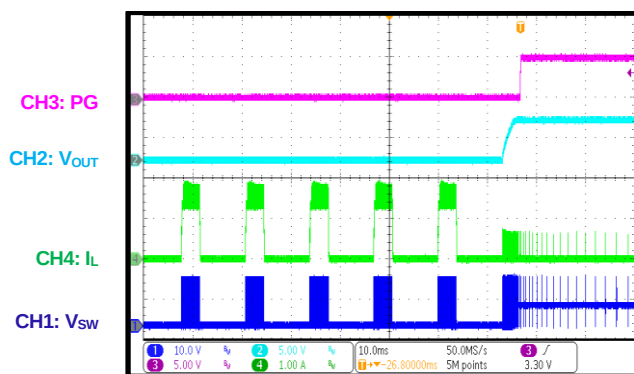
## SCP Entry

$I_{OUT} = 1A$



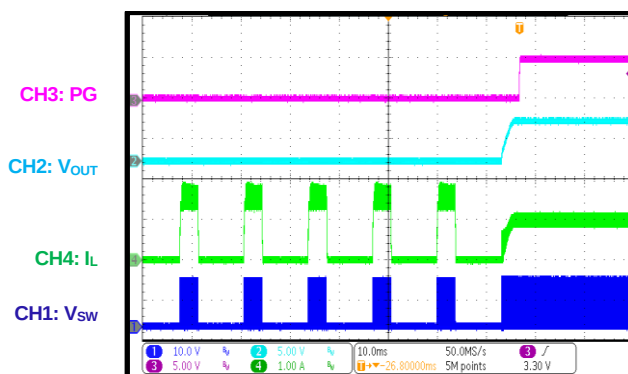
## SCP Recovery

$I_{OUT} = 0A$



## SCP Recovery

$I_{OUT} = 1A$

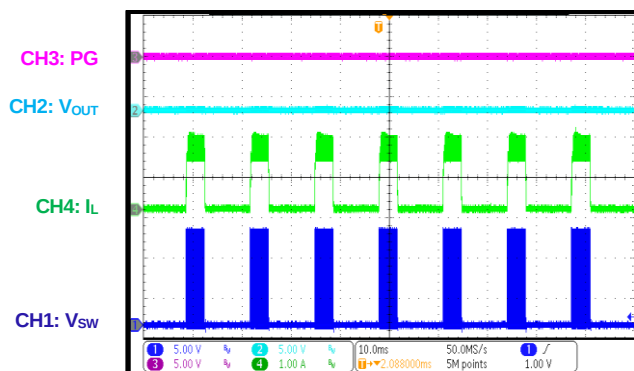


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

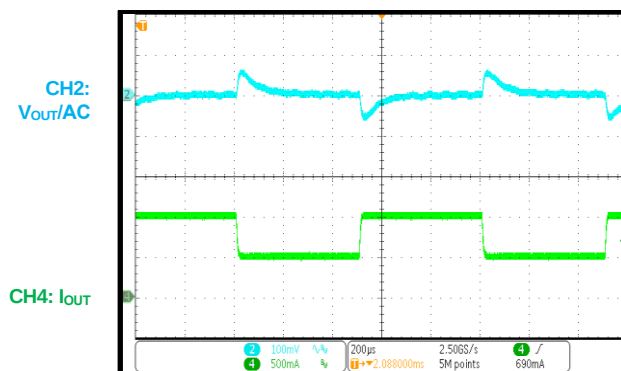
### SCP Steady State

$I_{OUT} = 0A$



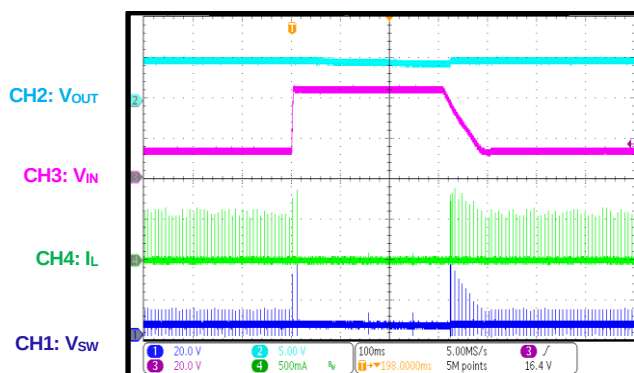
### Load Transient

$I_{OUT} = 0.5A$  to  $1A$ ,  $1.6A/\mu s$



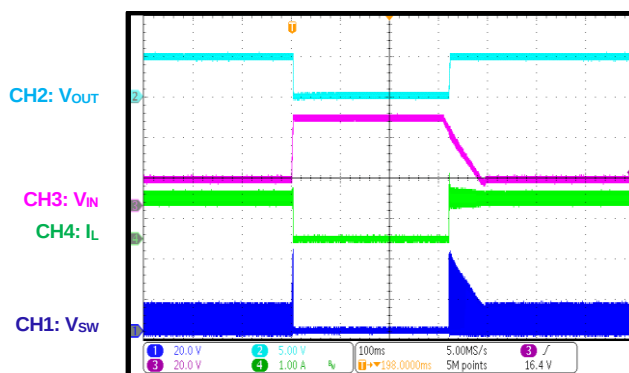
### Load Dump

$V_{IN} = 12V$  to  $42V$ ,  $I_{OUT} = 0A$



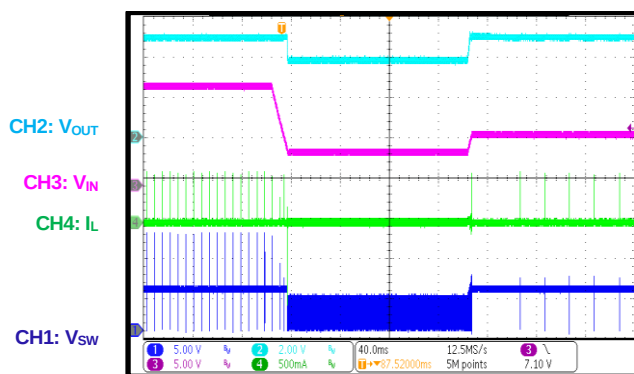
### Load Dump

$V_{IN} = 12V$  to  $42V$ ,  $I_{OUT} = 1A$



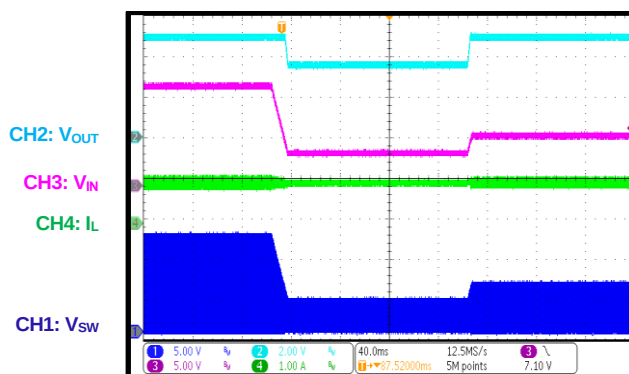
### Cold-Crank Conditions

$V_{IN} = 12V$  to  $3.3V$  to  $6V$ ,  $I_{OUT} = 0A$



### Cold-Crank Conditions

$V_{IN} = 12V$  to  $3.3V$  to  $6V$ ,  $I_{OUT} = 1A$

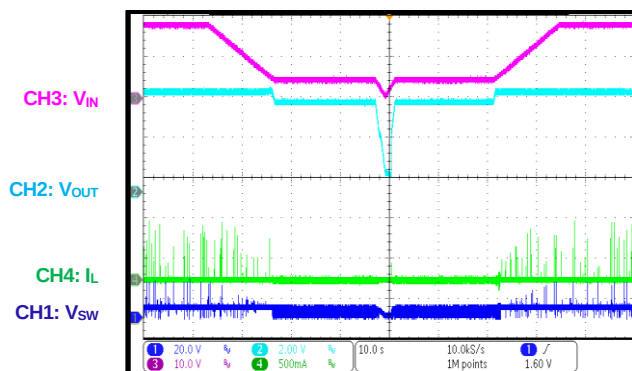


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  $L = 5.6\mu H$ ,  $C_{OUT} = 22\mu F \times 2$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

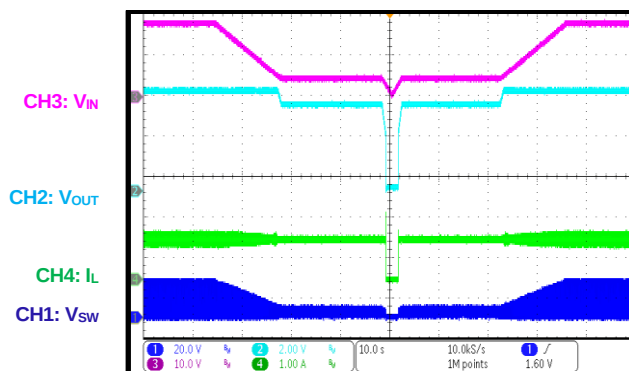
### VIN Ramp Down and Up

$V_{IN} = 18V$  to  $4.5V$  to  $0V$  to  $4.5V$  to  $18V$ ,  $I_{OUT}=0A$



### VIN Ramp Down and Up

$V_{IN} = 18V$  to  $4.5V$  to  $0V$  to  $4.5V$  to  $18V$ ,  $I_{OUT}=1A$



## FUNCTIONAL BLOCK DIAGRAMS

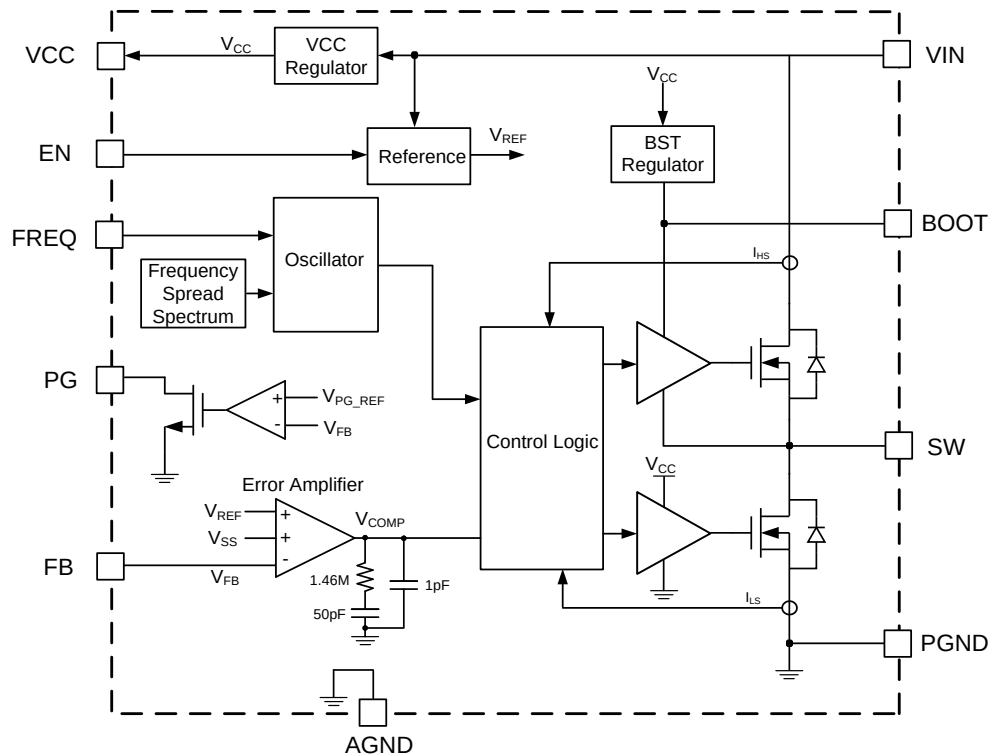


Figure 3: Functional Block Diagram (Adjustable Output)

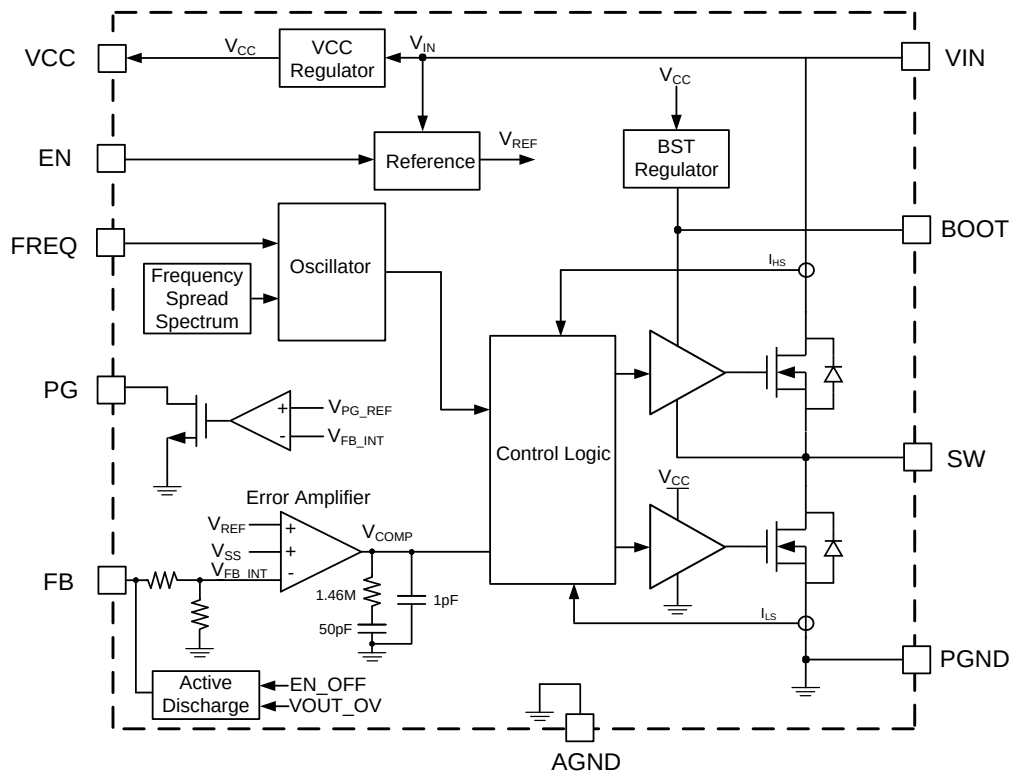


Figure 4: Functional Block Diagram (Fixed Output)

## OPERATION

The MPQ4321 is a synchronous, step-down switching converter with integrated internal high-side and low-side power MOSFETs. It provides 1A of highly efficient output current with peak current mode control.

The device features a wide input voltage range, configurable 350kHz to 2.5MHz switching frequency, internal soft start, and precision current limit. The MPQ4321's low operational quiescent current makes it well-suited for battery-powered applications.

### PWM Control

At moderate to high output currents, the MPQ4321 operates with fixed-frequency, peak current mode control to regulate the output voltage. A PWM cycle is initiated by the internal clock. At the rising edge of the clock, the high-side power MOSFET (HS-FET) turns on and remains on until the control signal reaches the value set by the internal COMP voltage ( $V_{COMP}$ ).

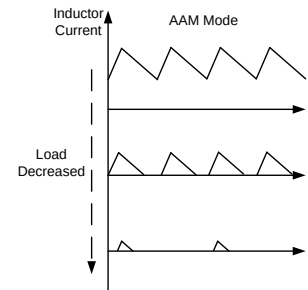
When the HS-FET is off, the low-side power MOSFET (LS-FET) turns on immediately, and stays on until the next cycle starts or the inductor current ( $I_L$ ) drops below the zero current detection (ZCD) threshold. The LS-FET remains off for at least the minimum off time before the next cycle starts.

If the current in the HS-FET cannot reach the value set by COMP within one PWM period, the HS-FET remains on and skips a turn-off operation. The HS-FET is forced off if it reaches the value set by COMP, or its 7 $\mu$ s maximum on time is reached. This operation mode extends the duty cycle, which achieves a low dropout when  $V_{IN}$  is almost equal to the output voltage ( $V_{OUT}$ ).

### Light Load Operation

The MPQ4321 works in advanced asynchronous mode (AAM) to optimize efficiency under light-load and no-load conditions.

When the inductor current approaches 0A under light loads, the MPQ4321 enters asynchronous operation. If the load is further decreased and  $V_{COMP}$  drops below the set value, the MPQ4321 enters AAM (see Figure 5).



**Figure 5: AAM Operation**

In AAM, the internal clock is reset every time  $V_{COMP}$  crosses over the set value, and the crossover time is used as a benchmark for the next clock. When the load increases and  $V_{COMP}$  exceeds the set value, the device operates in continuous conduction mode (CCM) or discontinuous conduction mode (DCM) with a constant switching frequency.

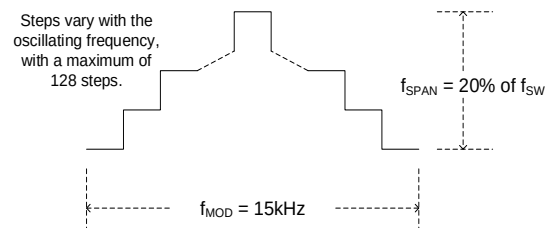
### Error Amplifier

The error amplifier compares the FB pin's voltage ( $V_{FB}$ ) with the internal reference (0.8V) and outputs a current proportional to the difference between the two values. This output current is then used to charge the compensation network to form  $V_{COMP}$ , which provides the error that controls the power MOSFET's duty cycle.

During normal operation, the minimum  $V_{COMP}$  is clamped to 0.9V, and the maximum  $V_{COMP}$  is clamped to 2.0V. COMP is internally pulled down to GND during shutdown.

### Spread Spectrum

The MPQ4321 uses a 15kHz modulation frequency with a maximum 128-step triangular profile to spread the internal oscillator frequency across a 20% ( $\pm 10\%$ ) window. The steps vary with the set oscillator frequency to ensure that the exact switching frequency steps cycle by cycle (see Figure 6).



**Figure 6: Spread Spectrum**

Side bands are created by modulating the switching frequency with the triangle modulation waveform. The emission power of the fundamental switching frequency and its harmonics are reduced, which also reduces the peak EMI noise.

### Soft Start

Soft start is implemented to prevent the converter's output voltage from overshooting during start-up. The soft-start time is fixed internally.

When the soft-start period starts, the soft-start voltage ( $V_{SS}$ ) rises from 0V to 1.2V with a specific slew rate. When  $V_{SS}$  is lower than the internal 0.8V reference voltage ( $V_{REF}$ ),  $V_{SS}$  overrides  $V_{REF}$ , and the error amplifier uses  $V_{SS}$  as the reference. When  $V_{SS}$  exceeds  $V_{REF}$ , the error amplifier uses  $V_{REF}$  as the reference.

### Pre-Biased Start-Up

If  $V_{FB}$  exceeds  $V_{SS}$  during start-up, this means that the output has a pre-biased voltage. Neither the HS-FET nor LS-FET turn on until  $V_{SS}$  exceeds  $V_{FB}$ .

### Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal runaway. If the silicon die temperature rises above its upper threshold (about 175°C), the device shuts down the power MOSFETs. If the temperature drops below its lower threshold (about 155°C), the thermal shutdown condition is removed, and the chip is enabled again.

### Start-Up and Shutdown

If both  $V_{IN}$  and EN exceeds their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

When the internal supply rail is up, the internal circuits start to work. If BOOT does not reach its refresh rising threshold (about 2.5V), the LS-FET turns on to charge BOOT. The HS-FET stays off during this time. When the soft-start block is enabled,  $V_{OUT}$  starts to ramp up slowly.  $V_{OUT}$  smoothly reaches its target within 5ms.

Three events can shut down the chip: EN going low,  $V_{IN}$  falling below its UVLO threshold, and thermal shutdown. During shutdown, the signaling path is blocked first to avoid any fault triggering. Then the COMP voltage is pulled down, and the floating driver works to disable the HS-FET.

## APPLICATION INFORMATION

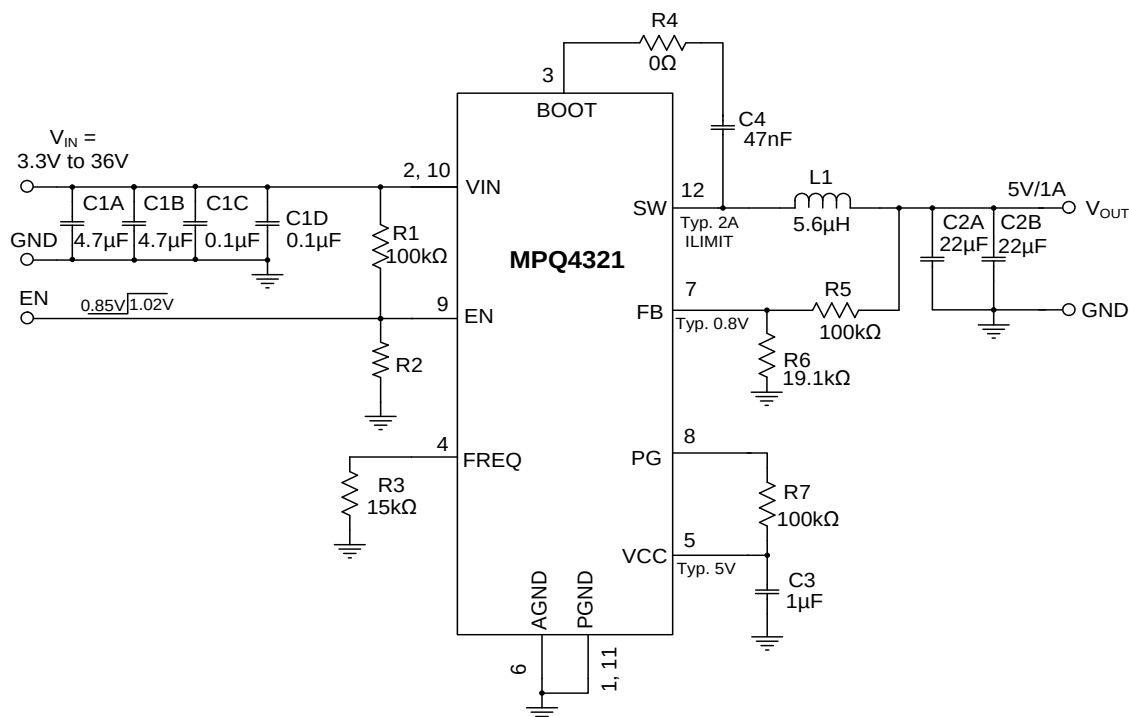


Figure 7: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{sw} = 2.2MHz$ )

Table 1: Design Guide Index

| Pin # | Pin Name | Component          | Design Guide Index                                        |
|-------|----------|--------------------|-----------------------------------------------------------|
| 1, 11 | PGND     | -                  | GND Connection (GND, Pins 1, 6, and 11)                   |
| 2, 10 | VIN      | C1A, C1B, C1C, C1D | Selecting the Input Capacitors (VIN, Pins 2 and 10)       |
| 3     | BOOT     | R4, C4             | Floating Driver and Bootstrap Charging (BOOT, Pin 3)      |
| 4     | FREQ     | R3                 | Setting the Switching Frequency (FREQ, Pin 4)             |
| 5     | VCC      | C3                 | Internal VCC (VCC, Pin 5)                                 |
| 6     | AGND     | -                  | GND Connection (GND, Pins 1, 6, and 11)                   |
| 7     | FB       | R5, R6             | Feedback (FB, Pin 7)                                      |
| 8     | PG       | R7                 | Power Good Indicator (PG, Pin 8)                          |
| 9     | EN       | R1, R2             | Enable and Under-Voltage Lockout (UVLO) (EN, Pin 9)       |
| 12    | SW       | L1, C2A, C2B       | Selecting the Inductor and Output Capacitors (SW, Pin 12) |

## Selecting the Input Capacitors (VIN, Pins 2 and 10)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7μF to 10μF capacitor. It is strongly recommended to use an additional lower-value capacitor (e.g. 0.1μF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since the input capacitor ( $C_{IN}$ ) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (1):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (1)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , calculated with Equation (2):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (2)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (3):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

## VIN Over-Voltage Protection (OVP)

The MPQ4321 stops switching when  $V_{IN}$  rises above its over-voltage rising threshold (typically 37.5V). The device resumes normal regulation and switching when  $V_{IN}$  drops below its over-voltage falling threshold (typically 36.5V).

## Floating Driver and Bootstrap Charging (BOOT, Pin 3)

The BOOT capacitor ( $C_4$ ) is recommended to be between 22nF to 100nF.

It is not recommended to place a resistor ( $R_{BOOT}$ ) in series with the BOOT capacitor, unless there is a strict EMI requirement.  $R_{BOOT}$  helps enhance EMI performance and reduce voltage stress at high input voltages, but also generates additional power consumption and reduces efficiency. When  $R_{BOOT}$  is necessary, it should be below 4Ω.

The voltage between BOOT and SW ( $V_{BOOT-SW}$ ) is regulated to about 5V by the dedicated internal bootstrap regulator. When  $V_{BOOT-SW}$  is below its regulated value, an N-channel MOSFET pass transistor connected from VCC to BOOT turns on to charge the bootstrap capacitor ( $C_{BOOT}$ ). The external circuit should provide enough voltage headroom to facilitate the charging. When the high-side MOSFET (HS-FET) is on, the BOOT voltage exceeds the VCC voltage, so the bootstrap capacitor cannot be charged.

Under conditions with higher duty cycles, the time available for bootstrap charging is shorter, so the bootstrap capacitor may not be charged sufficiently. In this case, the external circuit has insufficient voltage and time to charge the bootstrap capacitor. External circuitry can be used to ensure that the bootstrap voltage remains in the normal operation region.

If the bootstrap voltage reaches its under-voltage lockout (UVLO) threshold, the HS-FET turns off, and the LS-FET turns on with a minimum off time to refresh the bootstrap voltage with the set  $f_{SW}$ .

## Setting the Switching Frequency (FREQ, Pin 4)

A resistor ( $R_3$ ) can set the switching frequency (see Table 2 and the  $f_{SW}$  vs.  $R_{FREQ}$  curves on page 16).

The MPQ4321 oscillating frequency can be configured by an external resistor ( $R_{FREQ}$ ) connected from the FREQ pin to ground, placed as close as possible to the device.

Table 2 shows the relationship between the switching frequency ( $f_{SW}$ ) and  $R_{FREQ}$ .

**Table 2:  $f_{SW}$  vs.  $R_{FREQ}$**

| $R_{FREQ}$ (k $\Omega$ ) | $f_{SW}$ (kHz) | $R_{FREQ}$ (k $\Omega$ ) | $f_{SW}$ (kHz) |
|--------------------------|----------------|--------------------------|----------------|
| 100                      | 355            | 30.1                     | 1150           |
| 93.1                     | 385            | 26.1                     | 1300           |
| 86.6                     | 415            | 22.6                     | 1450           |
| 80.6                     | 450            | 20.5                     | 1600           |
| 75                       | 480            | 19.6                     | 1750           |
| 68.1                     | 520            | 17.8                     | 1900           |
| 59                       | 600            | 16.2                     | 2050           |
| 51.1                     | 700            | 15                       | 2200           |
| 40.2                     | 850            | 14.3                     | 2350           |
| 34.8                     | 1000           | 13.3                     | 2500           |

It is not possible to use a high  $f_{SW}$  with a high input voltage, since the minimum on time required for the HS-FET is limited. The MPQ4321 control loop automatically sets the maximum possible  $f_{SW}$  up to the set frequency, which also reduces excessive power loss.  $V_{OUT}$  is regulated by varying the duration of the HS-FET's switch-off time, which results in an automatic reduction of  $f_{SW}$ .

The device is guaranteed to comply with the HS-FET's minimum on time. An advantage of this method is that the device works at the target  $f_{SW}$  for as long as possible, and  $f_{SW}$  only changes when the device operates at high input voltages. For more details, see the  $f_{SW}$  vs.  $V_{IN}$  curve on page 16. In this scenario,  $R_{FREQ} = 15k\Omega$ , and  $V_{OUT} = 3.3V$ .

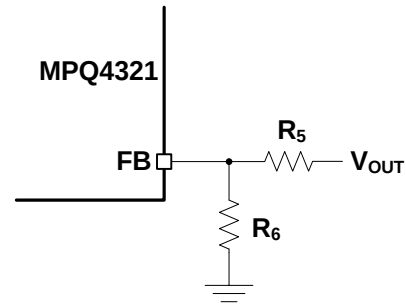
### Internal VCC (VCC, Pin 5)

The VCC capacitor (C3) is recommended to be 1 $\mu$ F.

Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses  $V_{IN}$  as its input and operates across the full  $V_{IN}$  range. When  $V_{IN}$  exceeds 5V, VCC is in full regulation. When  $V_{IN}$  drops below 5V, the VCC output degrades.

### Feedback (FB, Pin 7)

The feedback voltage is typically 0.8V if the device has an adjustable output. The external resistor divider connected to FB sets the output voltage (see Figure 8).

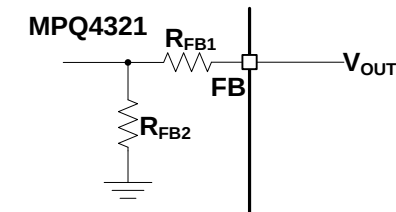


**Figure 8: Feedback Divider Network (Adjustable Output)**

Calculate  $R_6$  with Equation (4):

$$R_6 = \frac{R_5}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

For a fixed output, the FB resistor divider is integrated internally. This means that FB should be directly connected to the output to set the output voltage (see Figure 9). The following fixed outputs can be selected: 1V, 1.8V, 2.5V, 3.0V, 3.3V, 3.8V, and 5V.



**Figure 9: Feedback Divider Network (Fixed Output)**

Table 3 shows the relationship between the internal  $R_{FB}$  and  $V_{OUT}$ .

**Table 3:  $R_{FB}$  vs.  $V_{OUT}$**

| $V_{OUT}$ (V) | $R_{FB1}$ (k $\Omega$ ) | $R_{FB2}$ (k $\Omega$ ) |
|---------------|-------------------------|-------------------------|
| 1             | 64                      | 256                     |
| 1.8           | 320                     | 256                     |
| 2.5           | 544                     | 256                     |
| 3.0           | 704                     | 256                     |
| 3.3           | 800                     | 256                     |
| 3.8           | 960                     | 256                     |
| 5             | 1344                    | 256                     |

### Power Good Indicator (PG, Pin 8)

The PG resistor (R7) should have a resistance ( $R_{PG}$ ) that is about 100k $\Omega$ .

The MPQ4321 provides an open-drain power good (PG) output that indicates whether the device's output is within the specific window of its nominal value.

If using PG, connect it to a logic high level power source (e.g. 3.3V) via a pull-up resistor. PG goes high if the output voltage is within 94.5% to 105.5% of the nominal voltage; PG goes low if the output voltage is above 107% or below 93% of the nominal voltage. Float PG if it is not used.

### Enable and Under-Voltage Lockout (UVLO) (EN, Pin 9)

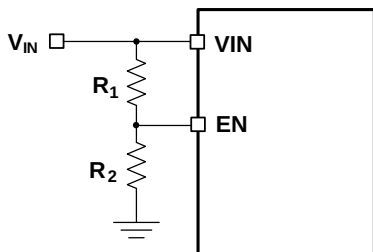
EN is a digital control pin that turns the regulator on and off.

#### Enabled by an External Logic High/Low Signal

When the EN voltage reaches 0.7V, BG does not turn on until  $V_{IN}$  exceeds 2.7V. BG then provides an accurate reference voltage for the EN threshold. Forcing EN above its rising threshold (about 1.02V) turns the device on. Turn the device off by driving EN below 0.85V. There is no internal pull-up or pull-down resistor connected to the EN pin, so do not float EN. An external pull-up or pull-down resistor is required if the control signal cannot give an accurate high or low logic.

#### Configurable $V_{IN}$ Under-Voltage Lockout (UVLO)

The MPQ4321 has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3.65V, while the falling threshold is about 2.9V. For applications that require a higher UVLO point, place an external resistor divider between  $V_{IN}$  and EN to raise the equivalent UVLO threshold (see Figure 10).



**Figure 10: Adjustable UVLO Using EN Divider**

The UVLO rising and falling thresholds can be calculated with Equation (5) and Equation (6), respectively:

$$INUV_{RISING} = (1 + \frac{R_1}{R_2}) \times V_{EN\_RISING} \quad (5)$$

$$INUV_{FALLING} = (1 + \frac{R_1}{R_2}) \times V_{EN\_FALLING} \quad (6)$$

Where  $V_{EN\_RISING}$  is 1.02V, and  $V_{EN\_FALLING}$  is 0.85V.

If EN is not used to control when the device turns on and off, connect EN to a high voltage source (e.g.  $V_{IN}$ ) to turn the device on by default.

### Selecting the Inductor and Output Capacitors (SW, Pin 12)

The inductor ( $L_1$ ) value can be estimated with Equation (7):

$$L_1 = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Where  $\Delta I_L$  is the peak-to-peak inductor ripple current.

A 1 $\mu$ H to 22 $\mu$ H inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current.

The peak inductor current ( $I_{LP}$ ) can be calculated with Equation (9):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Choose an inductor that does not saturate under the peak inductor current.

The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8f_{SW} \times C_{OUT}}) \quad (9)$$

Where L is the inductor value, and R<sub>ESR</sub> is the equivalent series resistance (ESR) of the output capacitor (C<sub>OUT</sub>). The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

When selecting an output capacitor, consider the allowable overshoot in V<sub>OUT</sub> if the load is suddenly removed. In this scenario, energy stored in the inductor is transferred to C<sub>OUT</sub>, causing its voltage to rise. To achieve an optimal overshoot relative to the regulated voltage, C<sub>OUT</sub> can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times \left(\left(\frac{V_{OUTMAX}}{V_{OUT}}\right)^2 - 1\right)} \quad (12)$$

Where V<sub>OUTMAX</sub>/V<sub>OUT</sub> is the allowable maximum overshoot. After calculating the capacitance that meets both the ripple and overshoot requirements, choose the larger capacitance value.

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4321 can be optimized for a wide range of capacitance and ESR values.

### Peak and Valley Current Limit

Both the HS-FET and LS-FET have cycle-by-cycle current-limit protection. When the inductor current (I<sub>L</sub>) reaches the high-side peak current limit (typically 2A) while the HS-FET is on, the HS-FET is forced off immediately to prevent the current from rising further.

When the LS-FET is on, the next clock's rising edge is held until I<sub>L</sub> drops below the low-side valley current limit (typically 1.5A). Then I<sub>L</sub> can drop to a sufficiently low value when the HS-FET turns on again. This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

### Short-Circuit Protection (SCP)

the output is shorted to ground, and the output voltage drops below 70% of its nominal output, the MPQ4321 shuts down and begins discharging V<sub>SS</sub>. The device restarts with a full soft start when V<sub>SS</sub> is fully discharged. This hiccup process is repeated until the fault is removed.

### Output Over-Voltage Protection (OVP) and Discharge

The MPQ4321 stops switching if the output voltage exceeds 130% of its nominal regulation value. Then an internal 75Ω discharge path from FB to GND is activated to discharge V<sub>OUT</sub>. This discharge path only can be activated if the output is fixed. The part resumes switching when V<sub>OUT</sub> drops back to 125% of its nominal value, and then the discharge path is disabled.

For a fixed output, the V<sub>OUT</sub> discharge path is also activated if an EN shutdown occurs while VCC exceeds its UVLO threshold. When VCC drops to its UVLO threshold, this path is deactivated.

### GND Connection (Pins 1, 6, and 11)

See the PCB Layout Guidelines section on the next page for more details.

### PCB Layout Guidelines <sup>(13)</sup>

Efficient PCB layout, especially input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 11 and follow the guidelines below:

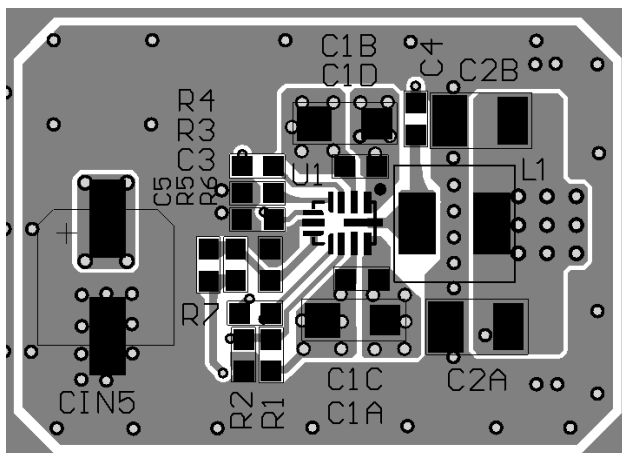
1. Place symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass

capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.

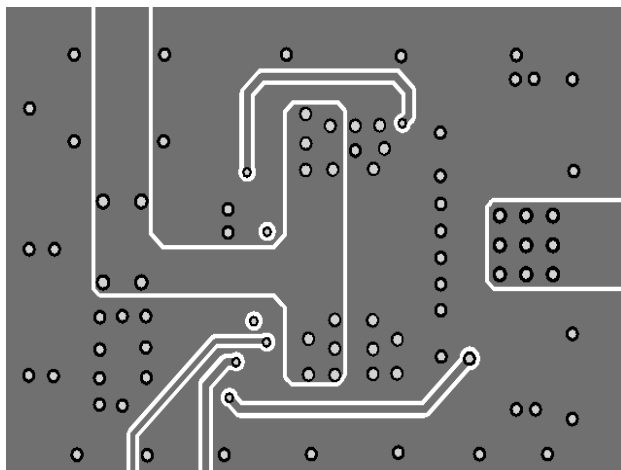
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and AGND as possible.
8. Route SW and BOOT away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip to ensure the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

**Note:**

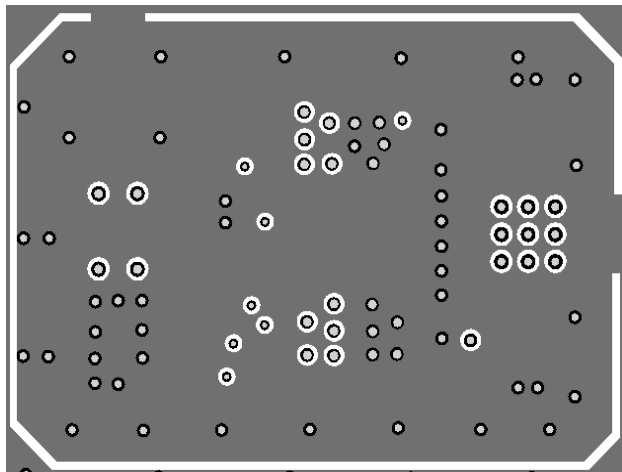
13) The recommended PCB layout is based on Figure 7 on page 30.



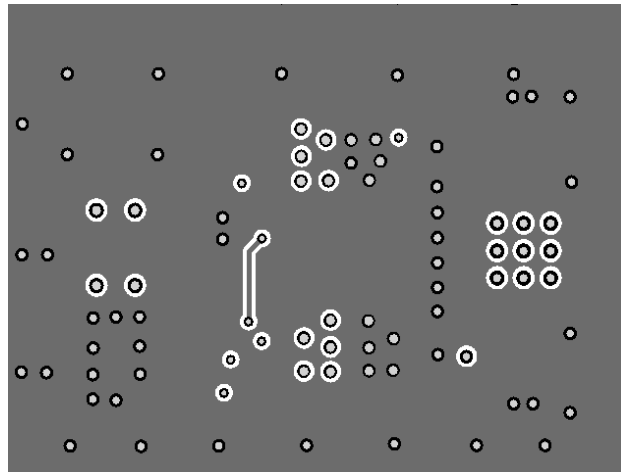
**Top Layer and Top Silk**



**Middle Layer 2**



**Middle Layer 1**



**Bottom Layer and Bottom Silk**

**Figure 11: Recommended PCB Layout**

## TYPICAL APPLICATION CIRCUITS

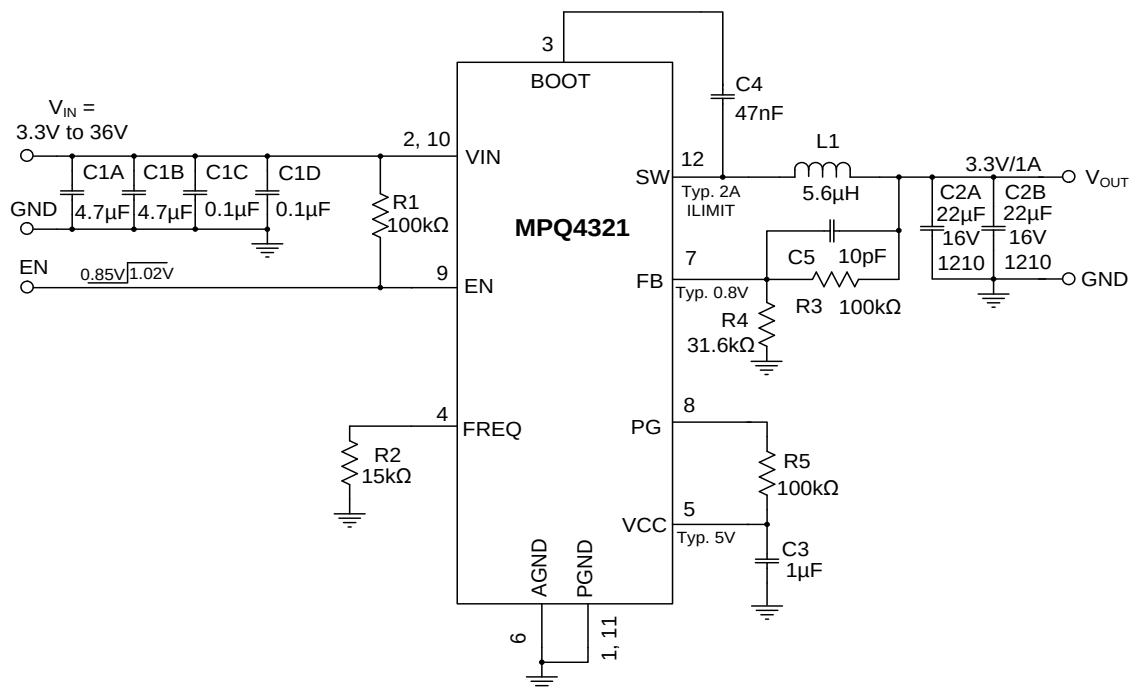


Figure 12: Typical Application Circuit ( $V_{OUT} = 3.3V$ ,  $f_{sw} = 2.2MHz$ )

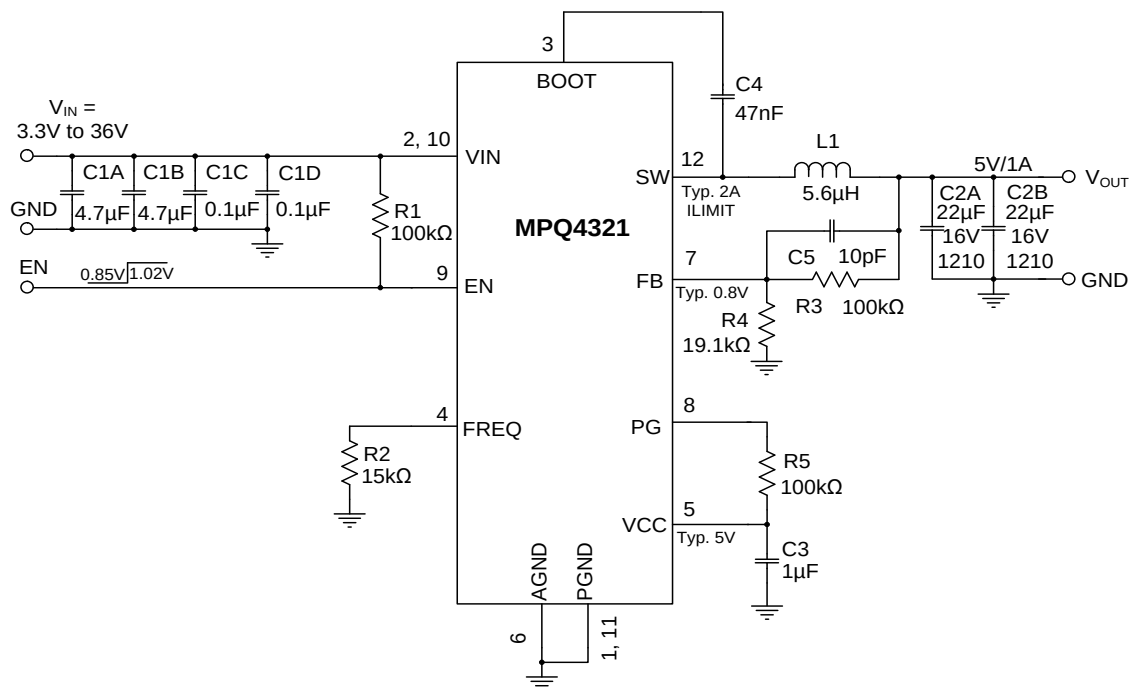
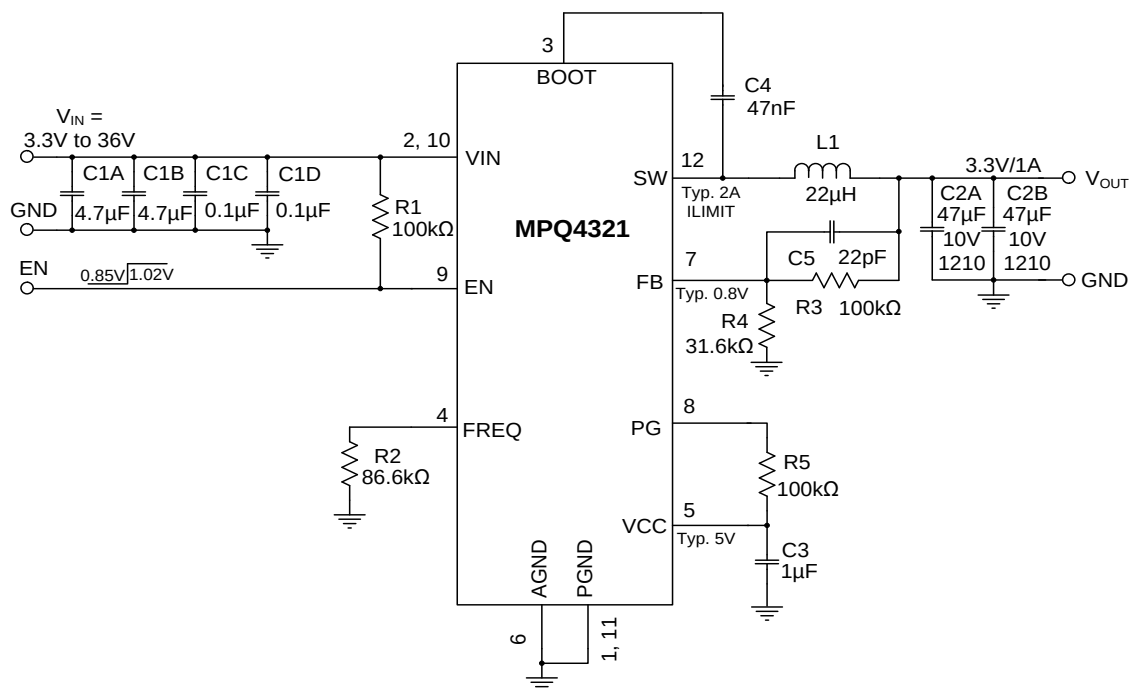
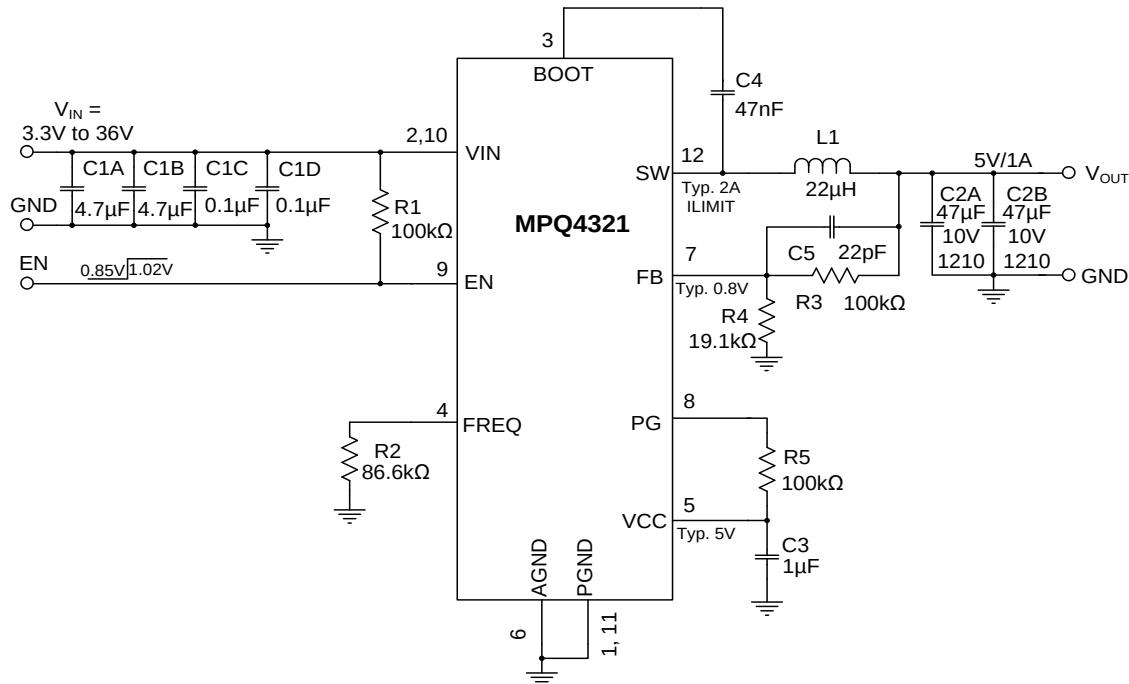


Figure 13: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{sw} = 2.2MHz$ )

## TYPICAL APPLICATION CIRCUITS *(continued)*



**Figure 14: Typical Application Circuit ( $V_{OUT} = 3.3V$ ,  $f_{SW} = 415kHz$ )**



**Figure 15: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{SW} = 415kHz$ )**

# TYPICAL APPLICATION CIRCUITS *(continued)*

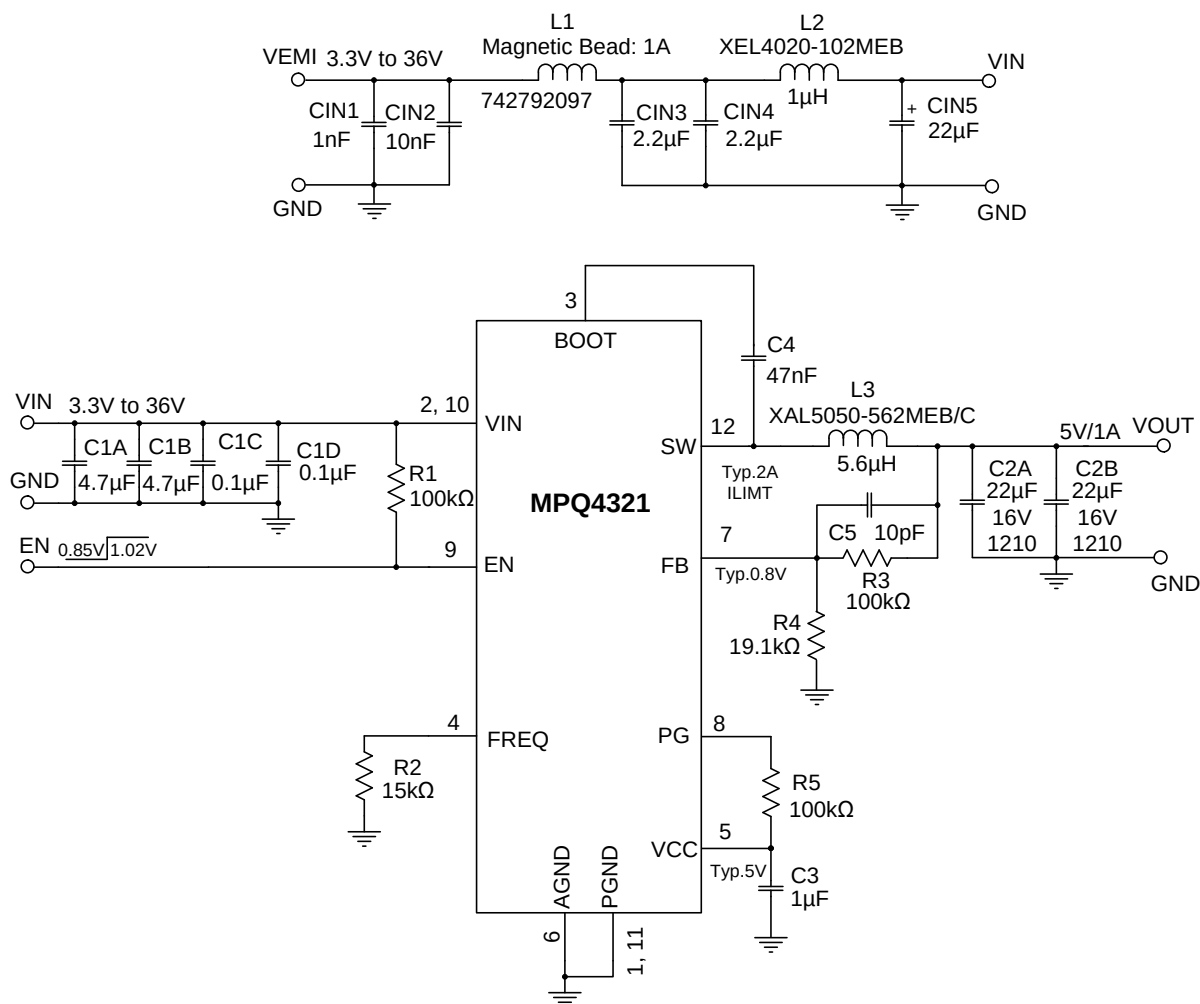


Figure 16: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$  with EMI Filters)

# TYPICAL APPLICATION CIRCUITS *(continued)*

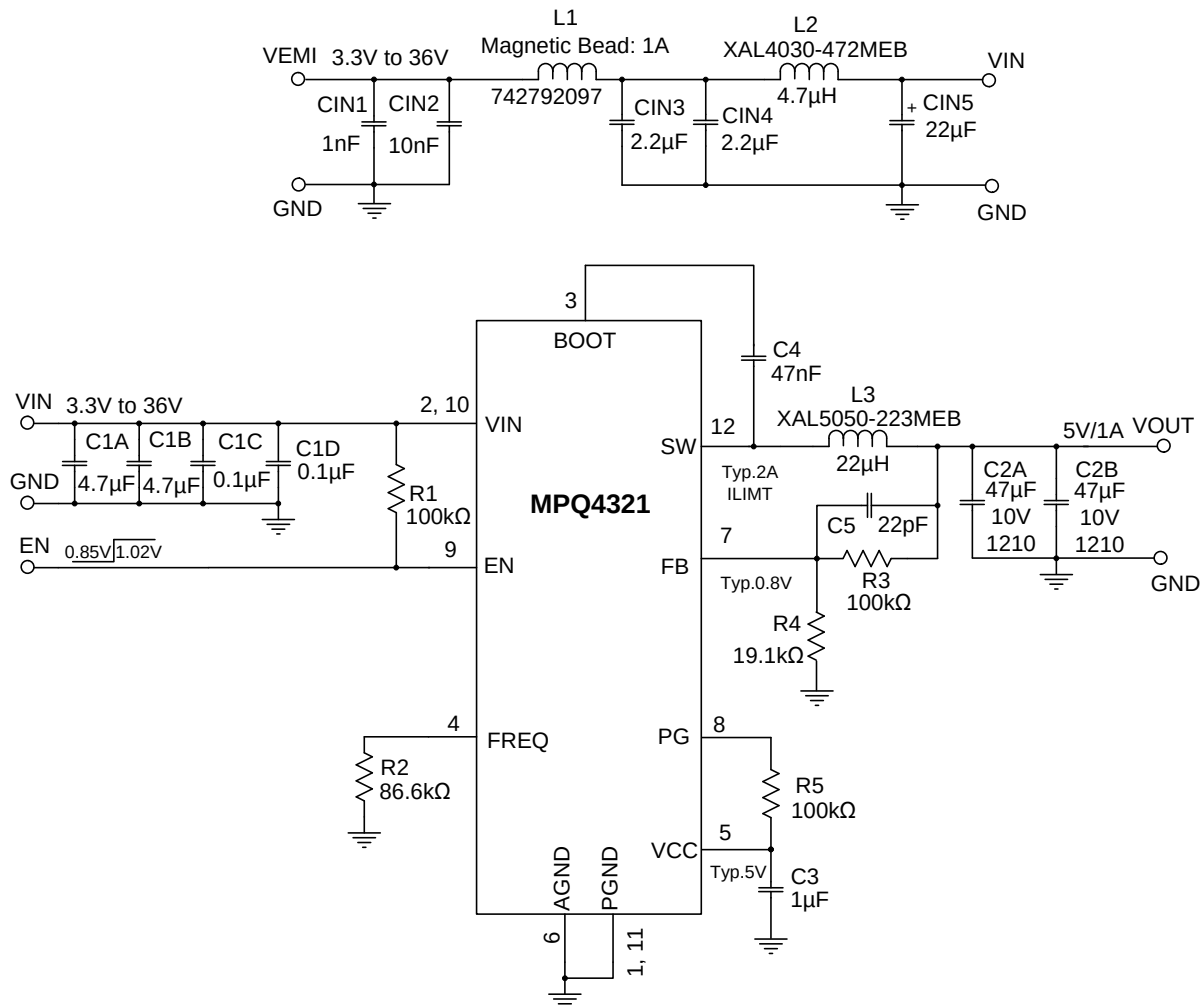
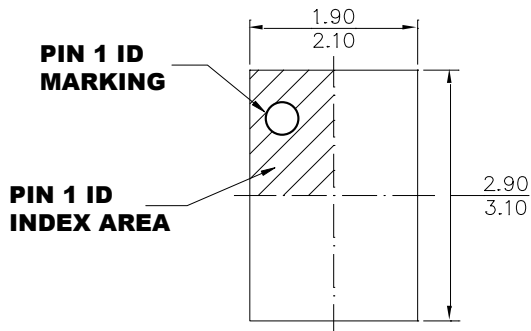


Figure 17: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{sw} = 415kHz$  with EMI Filters)

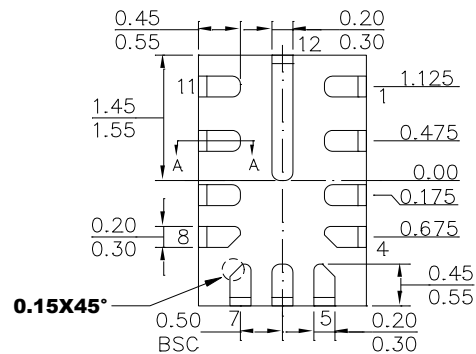
## PACKAGE INFORMATION

### QFN-12 (2mmx3mm)

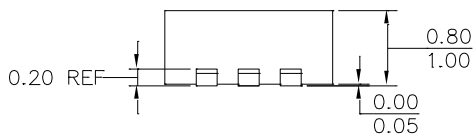
## Wettable Flank



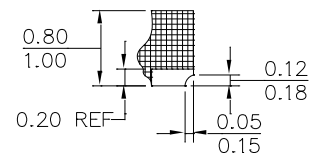
### TOP VIEW



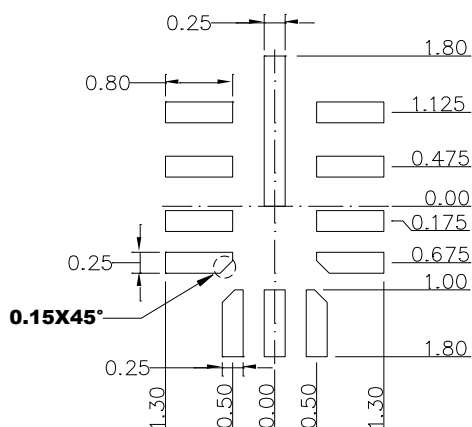
### BOTTOM VIEW



### SIDE VIEW



## SECTION A-A



## RECOMMENDED LAND PATTERN

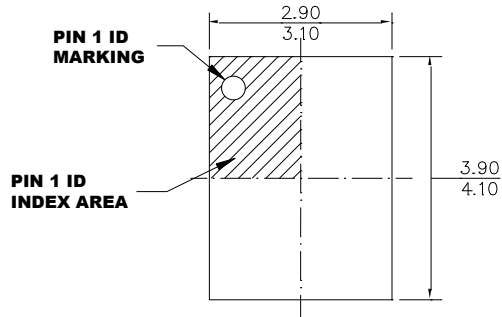
**NOTE:**

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

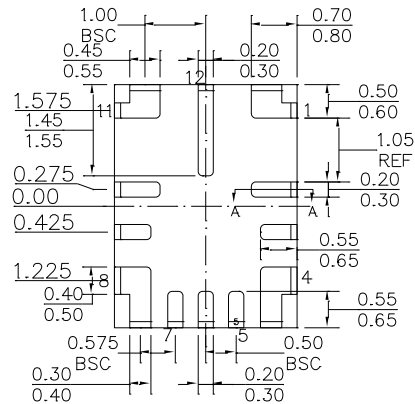
# PACKAGE INFORMATION

## QFN-12 (3mmx4mm)

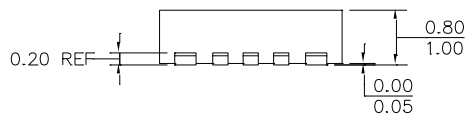
### Wettable Flank



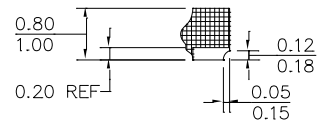
**TOP VIEW**



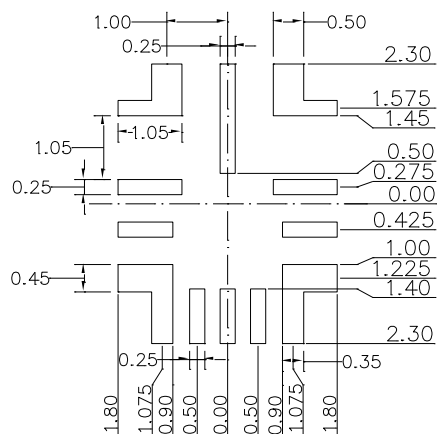
**BOTTOM VIEW**



**SIDE VIEW**



**SECTION A-A**

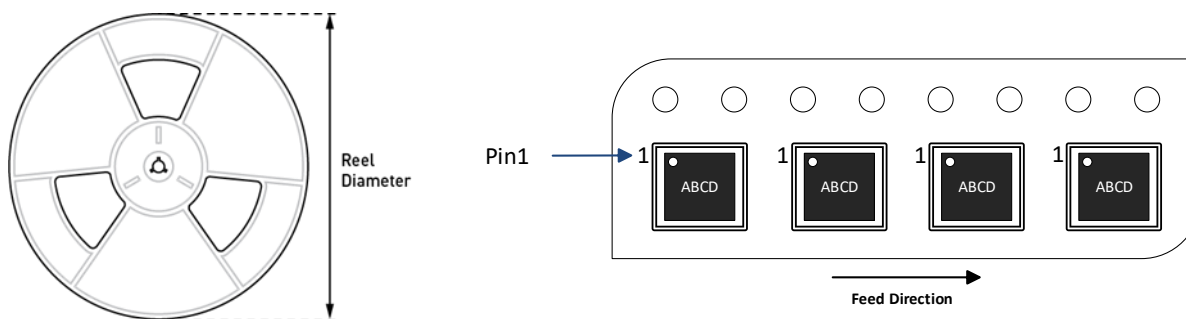


**RECOMMENDED LAND PATTERN**

### NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION



| Part Number         | Package Description | Quantity/ Reel | Quantity/ Tube <sup>(14)</sup> | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---------------------|---------------------|----------------|--------------------------------|----------------|---------------|--------------------|--------------------|
| MPQ4321GDE-AEC1-Z   | QFN-12 (2mmx3mm)    | 5000           | N/A                            | N/A            | 13in          | 12mm               | 8mm                |
| MPQ4321GDE-5-AEC1-Z | QFN-12 (2mmx3mm)    | 5000           | N/A                            | N/A            | 13in          | 12mm               | 8mm                |
| MPQ4321GLE-AEC1-Z   | QFN-12 (3mmx4mm)    | 5000           | N/A                            | N/A            | 13in          | 12mm               | 8mm                |

### Note:

14) N/A indicates “not available” in tubes. For the 500-piece tape & reel prototype quantities, contact the factory. (The order code for the 500-piece partial reel is “-P”, while the tape and reel dimensions remain the same as the full reel.)

## REVISION HISTORY

| Revision # | Revision Date | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Pages Updated       |
|------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|
| 1.0        | 4/30/2021     | Initial Release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | -                   |
| 1.1        | 5/17/2021     | Change the human body model (HBM) to $\pm 2\text{kV}$                                                                                                                                                                                                                                                                                                                                                                                                                                             | 5                   |
| 1.2        | 3/29/2023     | Updated formatting in headers                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | All                 |
|            |               | Deleted the PN “MPQ4321GDE-33-AEC1” in Ordering Information, Top Marking, and Carrier Information sections                                                                                                                                                                                                                                                                                                                                                                                        | 3, 42               |
|            |               | Updated new ESD format:<br><ul style="list-style-type: none"> <li>Updated “Operating junction temp (<math>T_J</math>)” to “<math>-40^\circ\text{C}</math> to <math>+150^\circ\text{C}</math>”</li> <li>Added description about <math>\theta_{JC}</math> in Notes 7, 8, and 9</li> </ul> Updated the minimum $V_{IN}$ for start-up from 3.8V to 3.9V, so that it matches the UVLO rising’s maximum value                                                                                           | 5                   |
|            |               | <ul style="list-style-type: none"> <li>Added Note 10 to “Minimum on time” and “Minimum off time”</li> <li>Updated remaining notes to align with new numbering</li> </ul>                                                                                                                                                                                                                                                                                                                          | 6, 8, 17–20, 35, 42 |
|            |               | <ul style="list-style-type: none"> <li>Added <math>I_{FB}</math> for the fixed output version in EC table</li> <li>Added “Output voltage accuracy of 5V fixed output version”</li> <li>Updated “PG rising/falling delay” to “PG rising/falling deglitch time”</li> <li>Added HS peak current limit min/max value as 1.5A/2.6A</li> <li>Added LS valley current limit min/max value as 1A/2A</li> <li>Added PG rising/falling threshold for fixed output and adjustable output versions</li> </ul> | 7                   |
|            |               | Updated C4 from 100nF to 47nF in Figure 7, as well as Figures 12–17                                                                                                                                                                                                                                                                                                                                                                                                                               | 30, 36–39           |
|            |               | Updated Floating Driver and Bootstrap Charging (BOOT, Pin 3) section:<br><ul style="list-style-type: none"> <li>Recommended <math>C_{BOOT}</math> is “22nF to 100nF”</li> <li>Recommended <math>R_{BOOT}</math> is “below <math>4\Omega</math>”</li> <li>“P-channel MOSFET” is “N-channel MOSFET”</li> </ul>                                                                                                                                                                                      | 31                  |
|            |               | Updated Figure 11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 35                  |
|            |               | Updated POD for QFN-12 (3mmx4mm)                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 41                  |
|            |               | Updated formatting for Note 12                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 42                  |

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