MPM3530

55V, 3A, Step-Down Power Module

DESCRIPTION

The MPM3530 is an easy-to-use, fully integrated, 55V input, 3A, step-down, DC/DC power module. The MPM3530 integrates a monolithic DC/DC converter, power inductor, input capacitors, and the necessary resistors and capacitors in a compact QFN package. The total power solution only requires a minimal number of external components.

The MPM3530 adopts a peak-current-mode control architecture with a fast transient response. This module provides over-current protection (OCP) with valley-current detection, which is used to prevent current runaway. The MPM3530 also has accurate and reliable over-voltage protection (OVP) and auto-recovery thermal protection. An optional external soft start is available, and enable and power good indicator functions are provided. To increase efficiency, the MPM3530 scales down the switching frequency automatically when the load is light.

FEATURES

- Wide 4.5V to 55V Operating Input Range
- Efficiency up to 92.3%
- Adjustable, Wide Output Voltage: 1V to 15V
- Programmable Switching Frequency with External SYNC Function
- External Soft Start (SS)
- Over-Current Protection (OCP)
- High Efficiency for Light-Load Operation
- Over-Voltage Protection (OVP) and Thermal Shutdown Protection
- Power Good (PG) Indication
- Meet EN55022 Class B Emission
- Operating Temperature Range: -40°C to 85°C
- Available in a QFN-47 (10mmx12mmx4mm) Package

APPLICATIONS

- Industrial Power Systems
- Diagnostic Machines/Test Equipment
- Distributed Power Systems
- Telecom and Networking Systems

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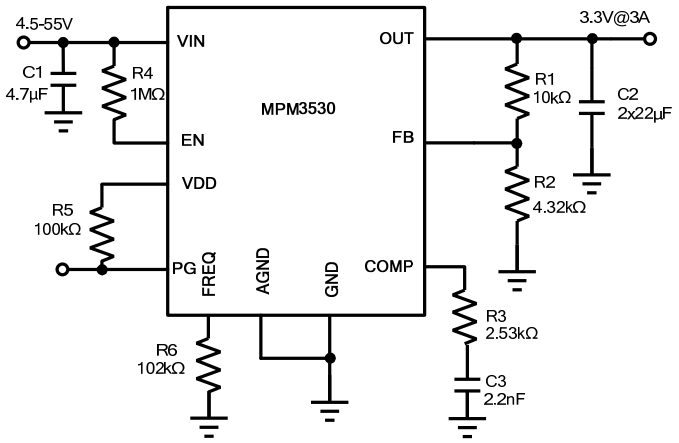
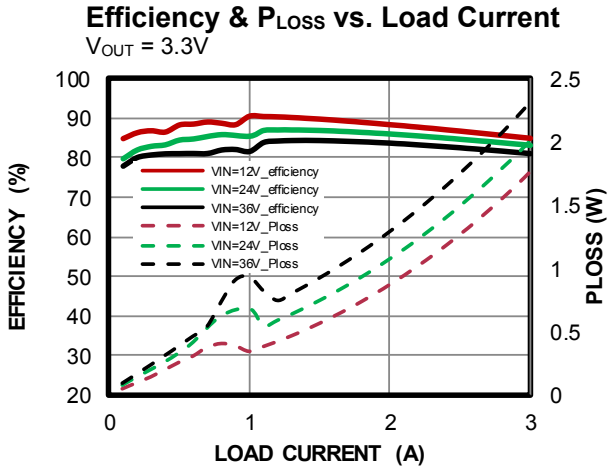
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3530GRF	QFN-47 (10mmx12mmx4mm)	*See Below*

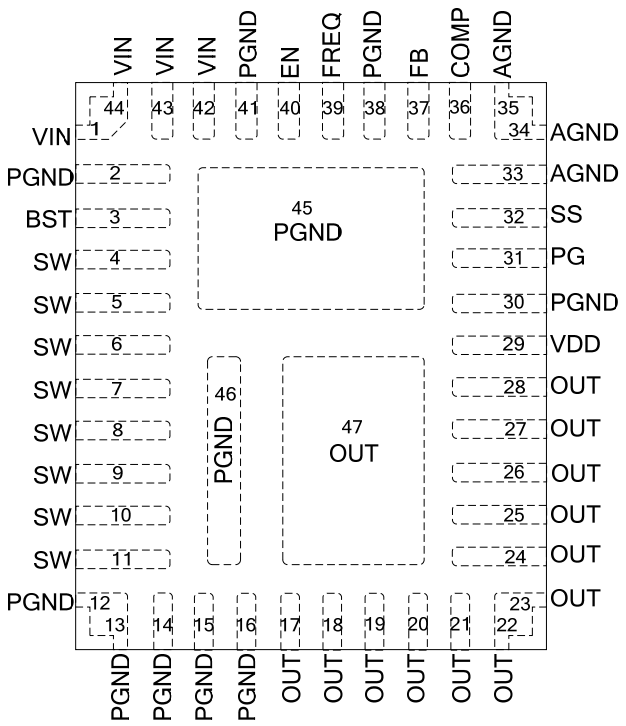
TOP MARKING

MPSYYWW
MP3530
LLLLLLLLL
M

MPS: MPS prefix
YY: Year code
WW: Week code
MP3530: First six digits of the part number
LLLLLLLLL: Lot number
M: Module

PACKAGE REFERENCE

TOP VIEW



QFN-47 (10mmx12mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 42 - 44	VIN	**Input supply.** VIN supplies power to all of the internal control circuitries and the VDD regulator. Place a decoupling capacitor to ground close to VIN to minimize switching spikes. Use wide traces to connect VIN.
2, 12 - 16, 30, 38, 41, 45, 46	PGND	**Module power ground pin.**
3	BST	**Bootstrap.** BST is the positive power supply for the internal floating high-side MOSFET driver. Keep BST floating.
4 - 11	SW	**Switch output.** Keep SW floating.
17 - 28, 47	OUT	**Module voltage output node.** Use wide traces to connect OUT.
29	VDD	**Power for internal MOSFET driver and BST charging circuit.**
31	PG	**Power good indication.** Connect a resistor from PG to a pull-up power source if it is being used.
32	SS	**Soft start.** Float SS for a default 1.2ms SS time. The SS time can be extended by connecting an external capacitor between SS and AGND.
33 - 35	AGND	**Ground for internal logic and signal circuit.**
36	COMP	**Compensation networks setting.** Connect an external resistor series with a capacitor between COMP and AGND. See the Application Information section on page 15 for compensation network configuration details.
37	FB	**Feedback.** FB is the input to the PWM comparator. Connect an external resistor divider between the output and AGND.
39	FREQ	**Frequency set pin.** Connect a resistor from FREQ to ground to set the switching frequency. If an external SYNC clock is applied to FREQ, the converter follows this SYNC clock frequency.
40	EN	**Enable input.** Pull EN below the specified threshold to shut down the chip. There is no internal pull-up or pull-down circuit, so EN cannot be floated.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 60V
V_{SW} ..... -0.5 to (V_{IN} + 0.5V)
V_{BST} ..... V_{SW} + 6V
V_{OUT} 16.5V
All other pins ..... -0.3V to 6V
EN sink current 150μA
All other pins ..... -0.3V to 4V
Continuous power dissipation (T_A = +25°C) (2) 5W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4.5V to 55V
Output voltage (V_{OUT}) ..... 1V to 15V
Operating junction temp. (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-47 (10mmx12mmx4mm)
EVM3530-RF-01A (4) ..... 17 .... 3.4 .... °C/W
JESD51-7 (5) ..... 17 .... 7.4 .... °C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EVM3530-RF-01A,4-layer PCB, 76mmx76mm.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{EN} = 3.3V, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range						
Input voltage range	V_{IN}		4.5		55	V
Output Voltage Range						
Output voltage range	V_{OUT}		1		15	V
Load regulation (6)	VOUT_DC _Load	V_{IN} = 24V, load current from 0 to 3A		1		%V_{OUT}
Line regulation (6)	VOUT_DC _Line	I_{OUT} = 3A, V_{IN} from 4.5V to 55V		1		%V_{OUT}
Quiescent Current						
Quiescent current	I_Q	V_{EN} = 3.3V, V_{FB} = 1.02V		450	670	μA
Current Limit						
Peak current limit	I_{LIMIT}	10% duty cycle	5.5	8.5	11.5	A
VDD Regulator						
VDD regulator output voltage	V_{DD}		3.4	3.6	3.8	V
Switching Frequency						
Switching frequency	f_{SW}	R_{FREQ} = 100kΩ	400	520	640	kHz
Over-Voltage and Under-Voltage Protection (OVP, UVP)						
OVP threshold	VOVP_TH	VFB(OVP)/VFB	108	115	122	%
VIN UVLO rising threshold	VINUV_R		3.7	3.9	4.1	V
VIN UVLO falling threshold	VINUV_F		3.3	3.5	3.7	V
Error Amplifier						
Feedback voltage	V_{FB}	4.5V ≤ VIN ≤ 55V	0.98	1	1.02	V
FB current	I_{FB}	V_{FB} = 1.07V		10	50	nA
COMP sink/source current	I_{COMP}		10	30	52	μA
PWM Comparator						
Minimum on time (7)	tON_MIN			90		ns
Minimum off time	tOFF_MIN			100		ns
Enable (EN)						
EN rising threshold	VEN_R		1.4	1.6	1.8	V
EN falling threshold	VEN_F		1.1	1.3	1.5	V
EN threshold hysteresis	VEN_HYS			300		mV
Soft Start (SS)						
Soft-start time (6)	tSS			1.2		ms
Power Good						
Power good threshold	VPG_TH	V_{OUT} rising, VFB(PG)/VFB	86	90	94	%
		V_{OUT} falling, VFB(PG)/VFB	81	85	89	
Power good hysteresis	VPG_HYS	ΔVFB(PG)/VFB		5		%
Power good delay	tPG_DL	V_{OUT} rising	8	22	37	μs
		V_{OUT} falling	8	21	33	μs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{EN} = 3.3V, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal						
Thermal shutdown (7)	T_{SD}			170		°C
Thermal hysteresis (7)	T_{SD_HYS}			10		°C

NOTES:
6) Not tested in production and guaranteed by over-temperature correlation.
7) Not tested in production and guaranteed by sample characterization.

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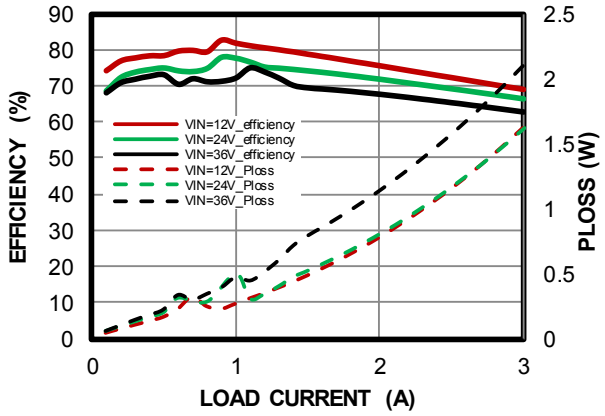
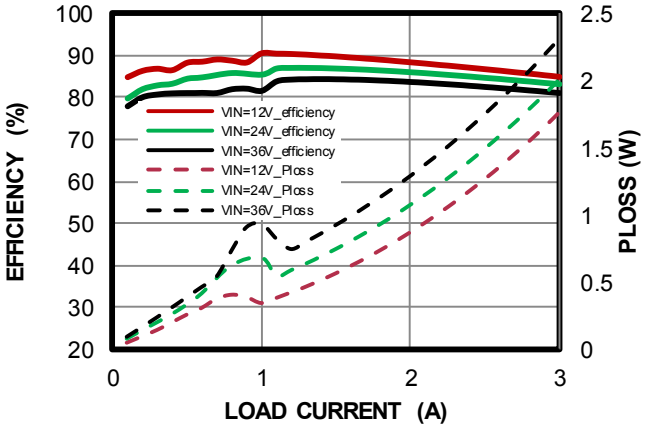
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

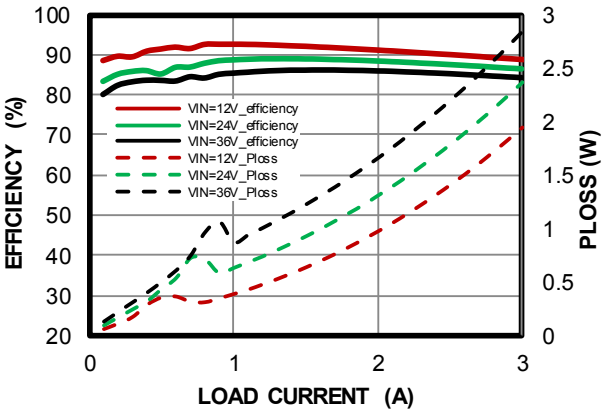
Efficiency & P_{LOSS} vs. Load Current
V_{OUT} = 1.2V



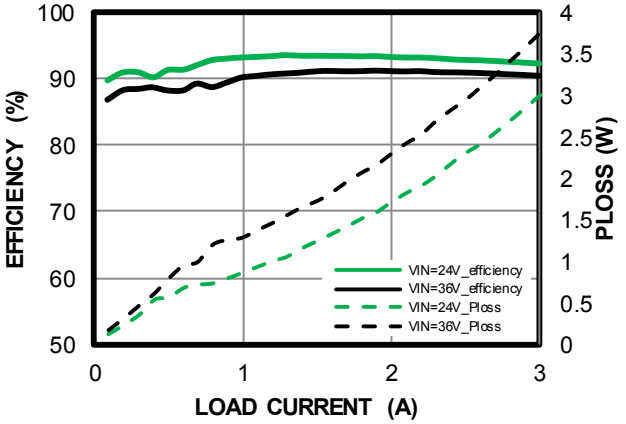
Efficiency & P_{LOSS} vs. Load Current
V_{OUT} = 3.3V



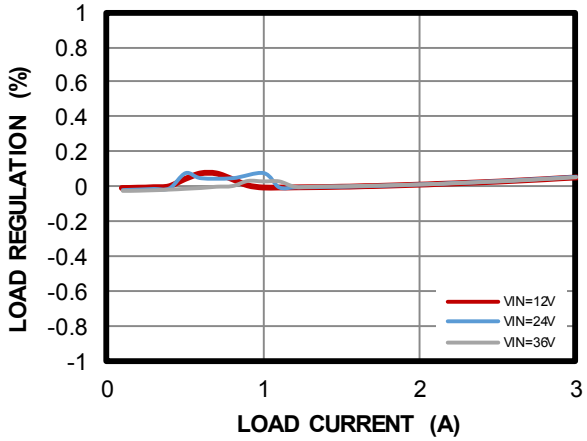
Efficiency & P_{LOSS} vs. Load Current
V_{OUT} = 5V



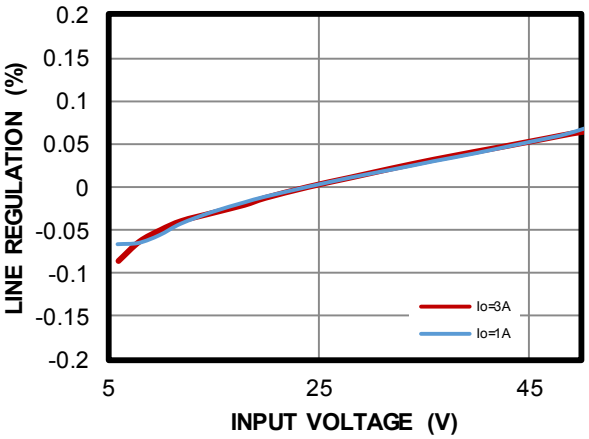
Efficiency & P_{LOSS} vs. Load Current
V_{OUT} = 12V



Load Regulation
V_{OUT} = 3.3V



Line Regulation
V_{OUT} = 3.3V



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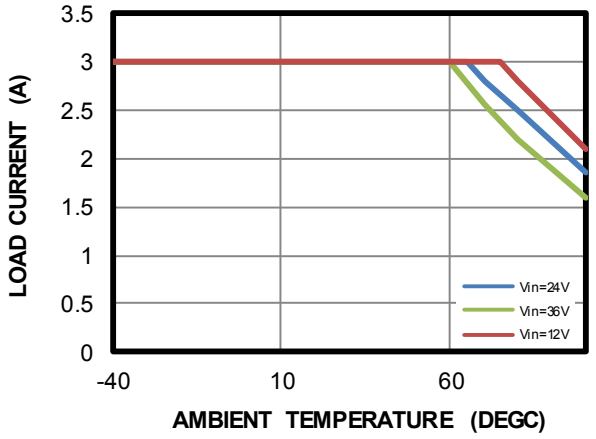
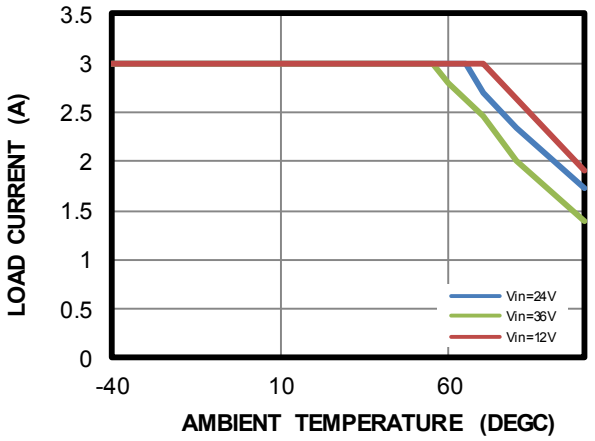
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

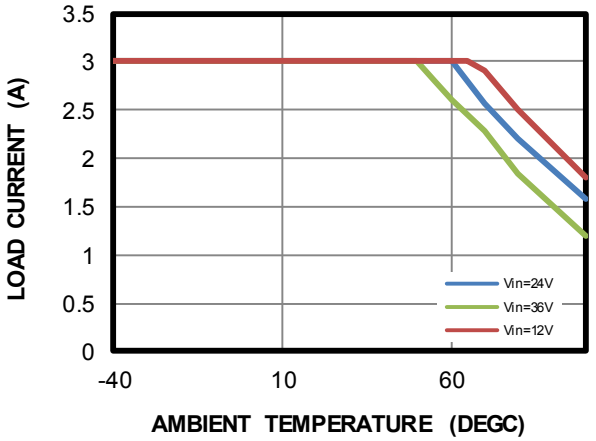
Thermal Derating
V_{OUT} = 1.2V



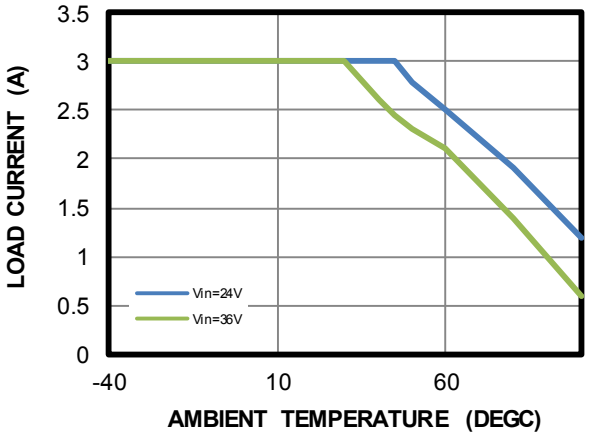
Thermal Derating
V_{OUT} = 3.3V



Thermal Derating
V_{OUT} = 5V



Thermal Derating
V_{OUT} = 12V



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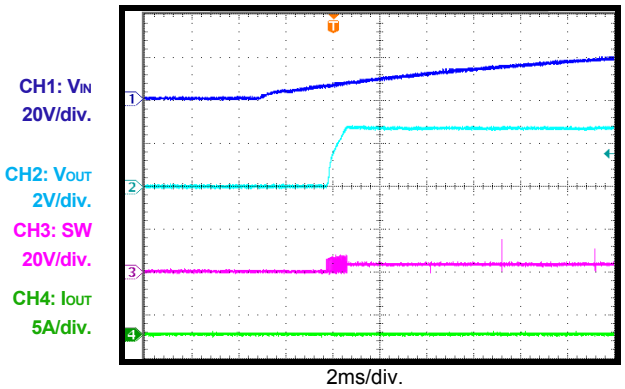
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

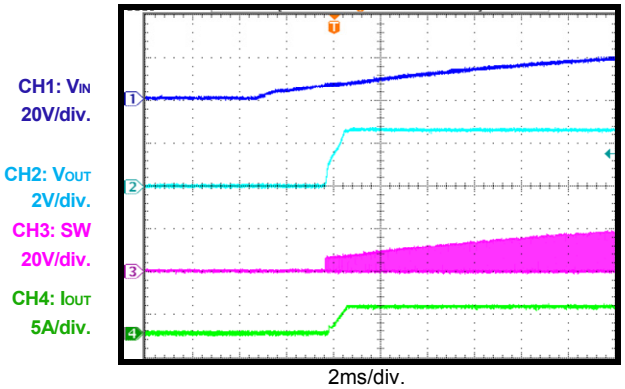
Start-Up through VIN

V_{OUT} = 3.3V, I_{OUT} = 0A



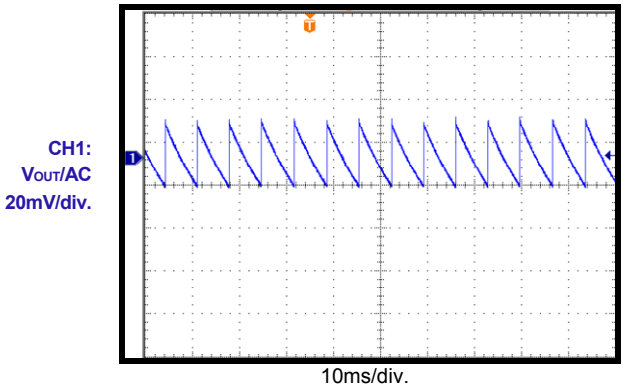
Start-Up through VIN

V_{OUT} = 3.3V, I_{OUT} = 3A



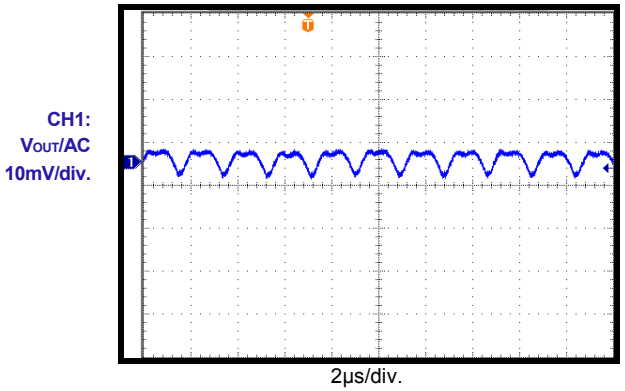
Output Ripple

V_{OUT} = 3.3V, I_{OUT} = 0A, 4x22µF caps



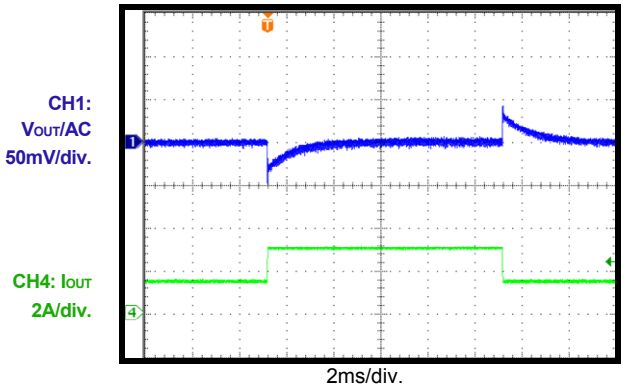
Output Ripple

V_{OUT} = 3.3V, I_{OUT} = 3A, 4x22µF caps



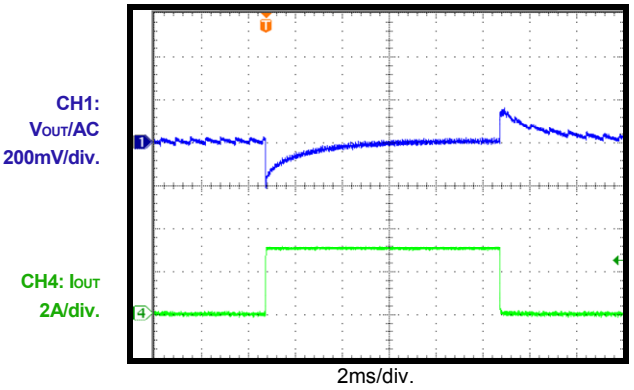
Load Transient Response

V_{OUT} = 3.3V, 1.5 - 3A, 4x22µF caps



Load Transient Response

V_{OUT} = 3.3V, I_{OUT} = 0 - 3A, 4x22µF caps



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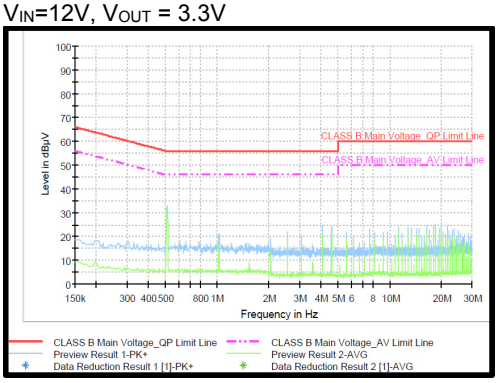
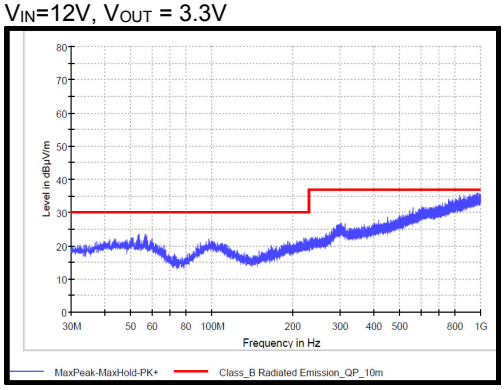
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

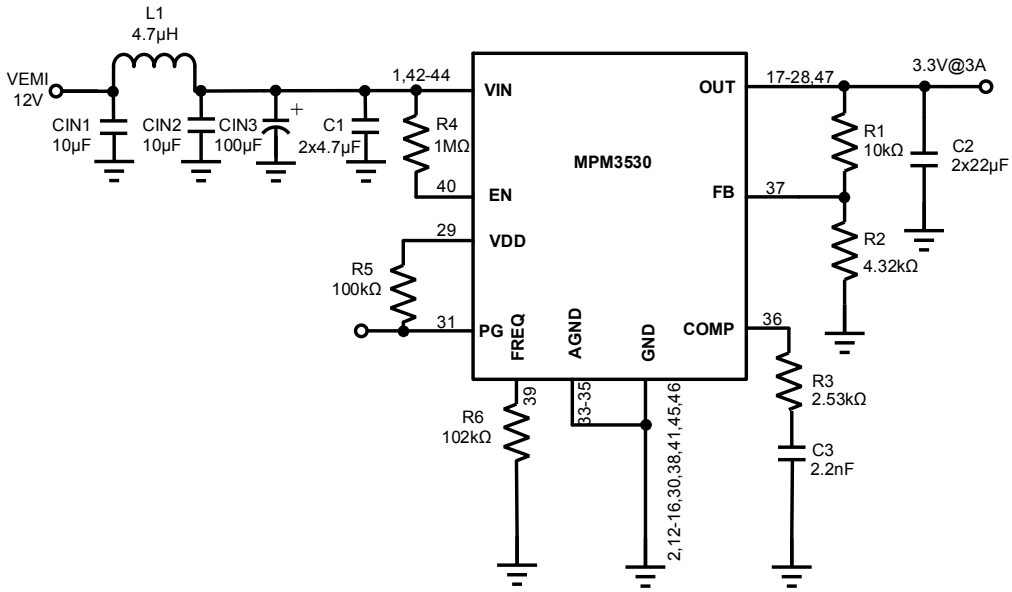
Conducted Emission, EN55022 Class B
V_{IN}=12V, V_{OUT} = 3.3V



Radiated Emission, EN55022 Class B
V_{IN}=12V, V_{OUT} = 3.3V



EMI TEST CIRCUIT



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BLOCK DIAGRAM

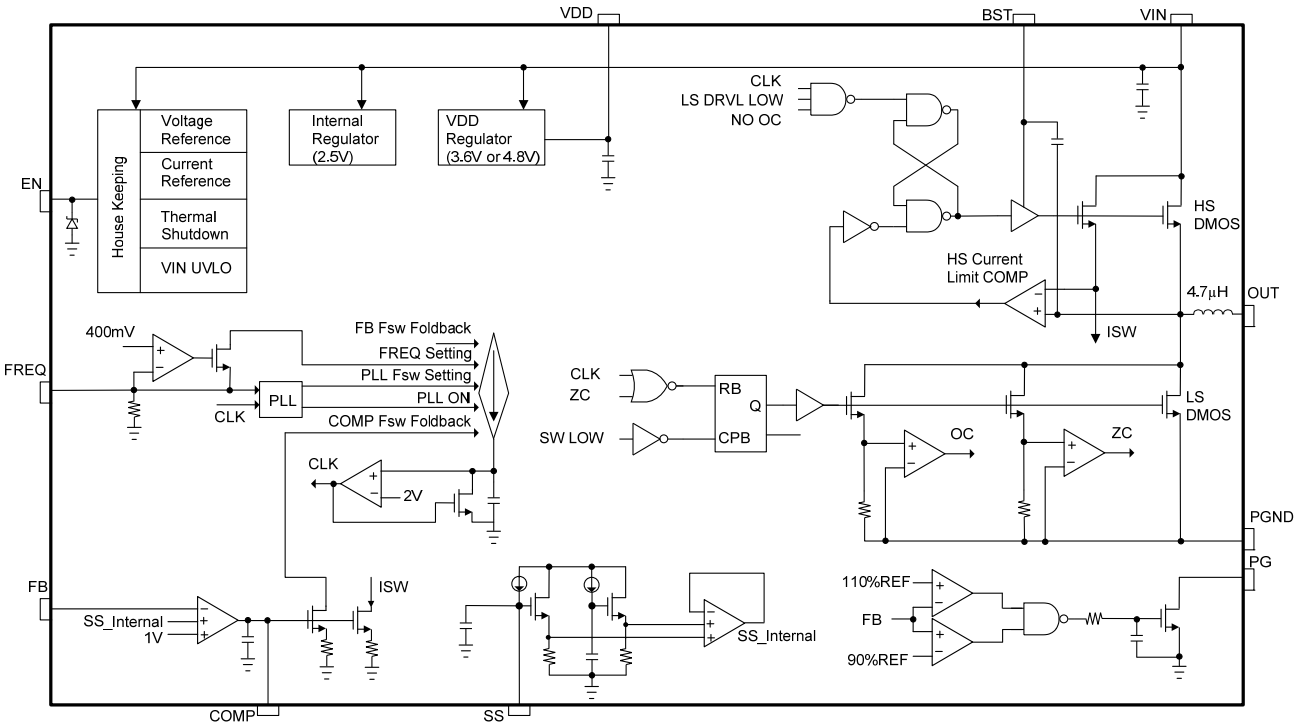

Figure 1: Functional Block Diagram

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OPERATION

The MPM3530 is a high-performance and complete power solution that features a wide input voltage range, high efficiency, external/internal soft start, programmable frequency, and comprehensive protection modes (OVP, OCP, OTP).

Pulse-Width Modulation (PWM) Control

The MPM3530 uses peak-current-mode control to regulate the output voltage. A pulse-width modulation (PWM) cycle is initiated by the internal clock at the beginning of every cycle. After the high-side MOSFET (HS-FET) turns on, the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the COMP voltage (V_{COMP}), which is the output of the internal error amplifier (EA). The output voltage of the error amplifier depends on the difference of the output feedback voltage and the internal high-precision reference, and it decides how much energy should be transferred to the load. The higher the load current, the higher V_{COMP} will be. After the high-side switch turns off, the low-side switch turns on, and the inductor current flows through the low-side switch. To avoid a shoot-through issue, a dead time is inserted to prevent the HS-FET and LS-FET from turning on at the same time. For each turn-on and turn-off in a switching cycle, the HS-FET turns on and off with a minimum on and off time limit.

Light-Load Operation

To achieve high efficiency, the MPM3530 uses two features during light load.

First, when the load current decreases, the inductor current drops at the same time. The LS-FET turns off to save driver loss when the inductor current drops to zero.

Second, when the load decreases, the switching frequency is scaled down to reduce the switching loss after V_{COMP} drops down below a certain threshold.

Error Amplifier (EA)

The error amplifier compares the FB voltage (V_{FB}) with the internal reference and outputs a current proportional to the difference between the two. This current is used to charge the external compensation networks to form V_{COMP}, which is used to control the HS-FET peak current and regulate the output voltage.

Oscillator and SYNC Function

The internal oscillator frequency is set by the frequency set resistor (R_{FREQ}) connected between FREQ and GND. The relationship between the oscillator frequency and R_{FREQ} is shown in Table 1 on page 14.

During light load, the switching frequency is scaled down according to V_{COMP}. The switching frequency starts decreasing when V_{COMP} is lower than about 0.8V. The switching is disabled when V_{COMP} drops below about 0.7V. Reduce switching loss and thermal dissipation, the switching frequency is decreased according to V_{FB}. When FB is lower than 25% x REF, the switching frequency starts decreasing from the normal value and finally drops to 5% of the normal value when FB is zero.

FREQ can be used to synchronize the internal oscillator rising edge to an external clock falling edge. Ensure that the high amplitude of the SYNC clock is higher than 1.5V and the low amplitude is lower than 1V to drive the internal logic. The recommended external SYNC frequency is in the range of 100kHz to 1MHz. There is no pulse-width requirement but note that there is always a parasitic capacitance of the pad. If the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in the application.

Enable Control (EN)

EN is a control pin that turns the module on and off. Drive EN above 1.6V to turn on the regulator. Drive EN below 1.3V to turn off the regulator.

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There is no internal pull-up or pull-down at EN, so when it is floating, the EN status is uncertain. EN is clamped internally using a 6.5V Zener diode between EN and GND. Connecting EN to a voltage source directly without any pull-up resistor requires limiting the voltage amplitude to ≤6V to prevent damage to the Zener diode. EN can be connected to a higher voltage (such as VIN) through a pull-up resistor if the system does not have another logic signal acting as the enable signal. If doing this, ensure that the pull-up resistor is high enough to keep the sink current flowing into EN below 150μA to avoid damaging the Zener diode. For example, when connecting EN to V_{IN} = 12V, $R_{PULL-UP}$ ≥ (12V - 6.5V) ÷ 150μA = 37kΩ.

Soft Start (SS)

A soft start (SS) is implemented in the MPM3530 to ensure a smooth output voltage during power-on and power-off. The soft-start function also helps reduce inrush current during start-up. The soft-start function is achieved by ramping SS up slowly and using SS to override the internal reference (REF) when SS - 900mV is lower than REF. When SS - 900mV is higher than REF, REF regains control. 900mV is the offset voltage of SS, which means SS is detected as 0 internally when it is lower than 900mV. To minimize the delay for SS to reach 0.9V, an internal pull-up circuit with about 30μA of average current pulls SS up to 600mV. Then use a 4μA constant current to charge SS until it reaches 2.5V. When SS is in the range of 0.9 - 1.9V, it overrides REF as the reference voltage of the error amplifier. During this period, the output voltage ramps up from 0 to the regulated value following the rise of SS.

An internal 4.7nF SS capacitor is used in the MPM3530. The default SS time can be estimated with Equation (1):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (1)$$

The default SS time is about 1.2ms. If a longer SS time is needed, an external SS capacitor can be added between SS and AGND. The external capacitor value can be determined with Equation (2):

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} - 4.7(nF) \quad (2)$$

Over-Voltage Protection (OVP)

The MPM3530 monitors the feedback output voltage to achieve over-voltage protection (OVP). If V_{FB} is higher than 103% x REF, the MPM3530 switches to sleep mode, the HS-FET turns off, and the LS-FET turns on to discharge the output energy. The MPM3530 resumes normal operation after V_{FB} drops below 103% x REF. If V_{FB} is higher than 110% x REF, the HS-FET and LS-FET are turned off immediately. Then both MOSFETs are latched, and the PG signal is asserted to indicate the fault status. Recycle EN or VIN to clear the protection.

Over-Current Protection (OCP)

The MPM3530 has cycle-by-cycle peak-current-limit protection and valley-current detection protection. The inductor current is monitored during the HS-FET on state. If the inductor current exceeds the current limit value set by V_{COMP}, the HS-FET turns off immediately. Then the LS-FET is turned on to discharge the energy, and the inductor current decreases. The HS-FET will not turn on again unless the inductor valley current is below a certain current threshold (valley current limit). This is useful for preventing an inductor current runaway. Both the peak current limit and the valley current limit values depend on V_{FB}. If the feedback output voltage is higher than 50% x REF, the current limit value is at the normal value. If the feedback output voltage is lower than 50% x RFF, the current limit decreases to half the normal value when the feedback output voltage is zero. This feature is very useful for reducing over-current protection (OCP) thermal dissipation, which may worsen when the output voltage is shorted. It is also useful for reducing high inrush current during start-up.

Under-Voltage Lockout (UVLO) Protection

The MPM3530 has an input under-voltage lockout protection (UVLO). Assuming that EN is

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active, the MPM3530 is powered on when the input voltage is higher than the UVLO rising threshold. The MPM3530 is powered off when the input voltage drops below the UVLO falling threshold.

Thermal Shutdown Protection

Thermal shutdown is employed in the MPM3530 by monitoring the temperature internally. If the junction temperature exceeds the threshold (typically 170°C), the regulator shuts off. The regulator turns on again when the temperature drops below 160°C. There is a hysteresis of ~10°C.

Power Good (PG)

The MPM3530 has one power good (PG) pin out to indicate normal operation after a soft-start time. PG is the open drain of an internal MOSFET and should be connected to VDD or an external voltage source through a resistor (i.e.: 100kΩ). After the input voltage is applied, the MOSFET is turned on, and PG is pulled to GND before SS is ready. After V_{FB} reaches 90% of V_{REF}, the MOSFET turns off, and PG is pulled high by an external voltage source. When V_{FB} drops to 85% of V_{REF}, the PG voltage is pulled to GND to indicate a failure output status.

Floating Driver and Bootstrap Charging

An internal bootstrap capacitor (typically 0.1μF) between BST and SW powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.3V with a hysteresis of 300mV. The driver's UVLO is soft-start related. When the bootstrap voltage reaches its UVLO threshold, the soft-start circuit resets. When the bootstrap UVLO is gone, the reset is off, and the soft-start process resumes.

The dedicated internal bootstrap regulator regulates and charges the bootstrap capacitor to 4.2V. When the voltage between the BST and SW nodes is less than its regulation, a PMOS pass transistor from VIN to BST turns on. The charging current path is from VIN to BST to SW.

As long as V_{IN} is higher than V_{SW} sufficiently, the bootstrap capacitor can be charged. When the HS-FET is on, $V_{IN} \approx V_{SW}$, so the bootstrap capacitor cannot be charged. When the LS-FET is on, the difference between V_{IN} and V_{SW} is at its largest, making it the best period to charge. When there is no current in the inductor, $V_{SW} = V_{OUT}$, so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor. At higher duty cycles, there is less time for the bootstrap charging, so the bootstrap capacitor may not be charged sufficiently. If the internal circuit does not have sufficient voltage and the bootstrap capacitor is not charged, extra external circuitry can be used to ensure that the bootstrap voltage is within the normal operating region.

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APPLICATION INFORMATION

Setting the Switching Frequency

The MPM3530 has an externally adjustable frequency. The switching frequency (f_{SW}) can be set using a resistor at FREQ (R_{FREQ}). Table 1 shows recommended R_{FREQ} values for various f_{SW} values.

Table 1: f_{SW} vs. R_{FREQ}

f_{SW} (kHz)	R_{FREQ} (kΩ)
1000	47.5
900	56
800	63.4
700	73.2
600	84.5
500	102
400	133
300	178
200	261
100	523

Setting the Output Voltage

A resistive voltage divider from the output voltage to FB sets the output voltage. The voltage divider divides the output voltage down to the feedback voltage by the ratio shown in Equation (3):

$$V_{FB} = V_{OUT} \times \frac{R2}{R1+R2} \quad (3)$$

Calculate the output voltage with Equation (4):

$$V_{OUT} = V_{FB} \times \frac{R1+R2}{R2} \quad (4)$$

For example, if R1 is 10kΩ, then R2 can be calculated with Equation (5):

$$R2 = \frac{10}{V_{OUT} - 1} k\Omega \quad (5)$$

For a 3.3V output voltage, R1 is 10kΩ, and R2 is 4.32kΩ.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use capacitors with a low equivalent series resistance (ESR) for the best performance. Ceramic capacitors are preferred, but tantalum or low ESR electrolytic capacitors may also be sufficient.

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor (C1) can be electrolytic, tantalum, or ceramic.

When using electrolytic or tantalum capacitors, place a small, high-quality, ceramic capacitor (0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be approximated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. Low ESR capacitors are recommended to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (9)$$

Where L is the inductor value, and R_{ESR} is the ESR value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and contributes the most to the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency.

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For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPM3530 can be optimized for a wide range of capacitances and ESR values.

Compensation Components

The MPM3530 employs current-mode control for easy compensation and fast transient response. COMP is the output of the internal error amplifier and controls system stability and transient response. A series resistor-capacitor combination sets a pole-zero combination to control the control system's characteristics. The DC gain of the voltage feedback loop can be calculated with Equation (12):

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}} \quad (12)$$

Where A_{VEA} is the error amplifier voltage gain (1000V/V), G_{CS} is the current-sense transconductance (12A/V), and R_{LOAD} is the load resistor value.

The system has two important poles: one due to the compensation capacitor (C3) and the output resistor of the error amplifier, and the other due to the output capacitor and the load resistor. These poles can be determined with Equation (13) and Equation (14):

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}} \quad (13)$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}} \quad (14)$$

Where G_{EA} is the error-amplifier transconductance (540μA/V).

The system has one important zero due to the compensation capacitor and the compensation resistor (R3).

This zero can be determined with Equation (15):

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3} \quad (15)$$

The system may have another significant zero if the output capacitor has a large capacitance or a high ESR value. This zero can be determined with Equation (16):

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}} \quad (16)$$

In this case, a third pole set by the compensation capacitor (C4) and the compensation resistor can compensate for the effect of the ESR zero. This pole can be determined with Equation (17):

$$f_{P3} = \frac{1}{2\pi \times C4 \times R3} \quad (17)$$

The goal of compensation design is to shape the converter transfer function for a desired loop gain. The system crossover frequency where the feedback loop has unity gain is important, since lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies lead to system instability. Generally, set the crossover frequency to ~0.1xf_{SW}.

Use the following steps to design the compensation:

1. Choose R3 to set the desired crossover frequency. R3 can be determined with Equation (18):

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} \quad (18)$$

   Where f_C is the desired crossover frequency.

2. Choose C3 to achieve the desired phase margin. For applications with typical inductor values, set the compensation zero (f_{Z1}) to <0.25xf_C to provide a sufficient phase margin.

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3. C3 can be calculated with Equation (19):

$$C3 > \frac{4}{2\pi \times R3 \times f_C} \quad (19)$$

Determine if C4 is required. C4 is required if the ESR zero of the output capacitor is located at <0.5xf_{SW}, or Equation (20) is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_{SW}}{2} \quad (20)$$

If this is the case, use C4 to set the pole (f_{P3}) at the location of the ESR zero. Determine C4 with Equation (21):

$$C4 = \frac{C2 \times R_{ESR}}{R3} \quad (21)$$

External Bootstrap Diode

For high duty-cycle operations where V_{OUT}/V_{IN} > 65%, there is less time available for the bootstrap charging, so the bootstrap capacitor may not be charged sufficiently. This affects efficiency and normal operation. An external bootstrap diode from the 3 - 5V rail to BST can help charge the bootstrap capacitor and enhance efficiency (see Figure 2). The output voltage is a good choice for this power supply if it is in the above range. The bootstrap diode can be a low-cost one, such as IN4148 or BAT54.

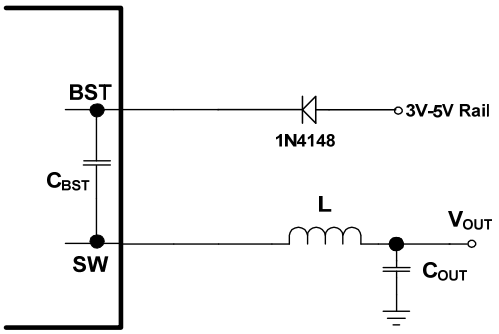

Figure 2: External Bootstrap Diode

At no load or light load, the converter may operate in pulse-skip mode to maintain the output-voltage regulation. Under this condition, V_{SW} = V_{OUT} for most of the time, so the diode from V_{OUT} to BST cannot charge the bootstrap capacitor. For a sufficient gate voltage during pulse-skip mode, V_{IN} - V_{OUT} should be no less than 3V. For example, if V_{OUT} = 3.3V, then V_{IN} must exceed 3.3V + 3V = 6.3V to maintain a sufficient bootstrap voltage at no load or light load. To meet this requirement, EN can program the input UVLO voltage to V_{OUT} + 3V.

PCB Layout Guidelines [10]

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 3 and follow the guidelines below.

1. Keep the connection of the input ground and GND as short and wide as possible.
2. Ensure that all feedback connections are short and direct.
3. Place the feedback resistors as close as to the chip as possible.
4. Route sensitive analog areas such as FB away from SW.
5. Place enough vias around the chip for better thermal performances.

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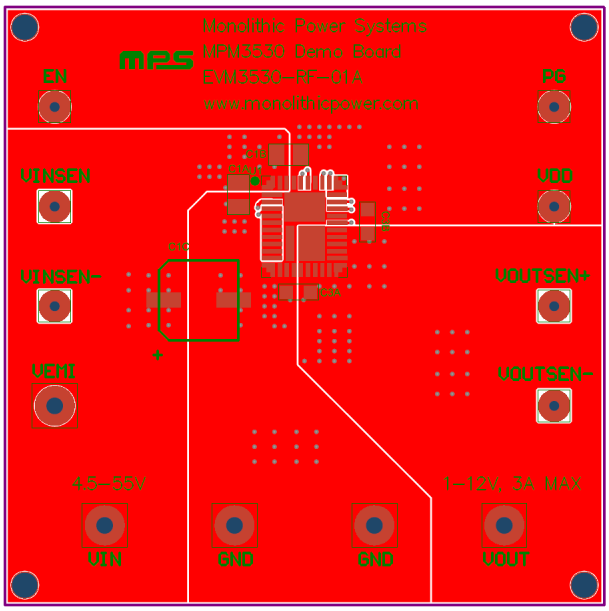
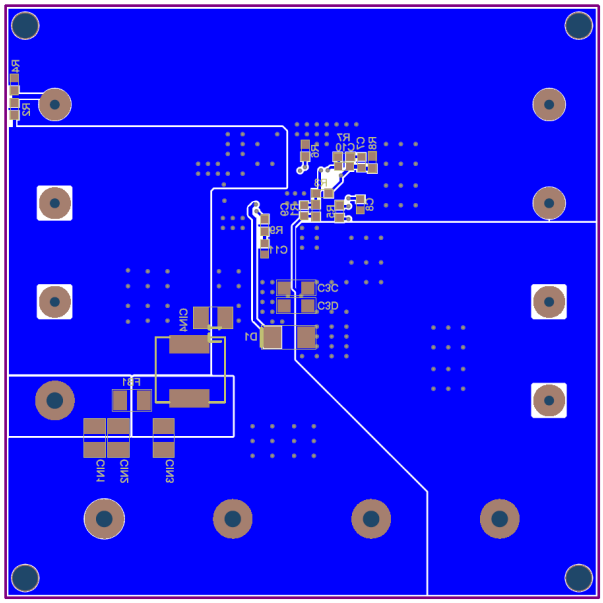


Top Layer



Bottom Layer

Figure 3: Recommended Layout

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TYPICAL APPLICATION CIRCUITS

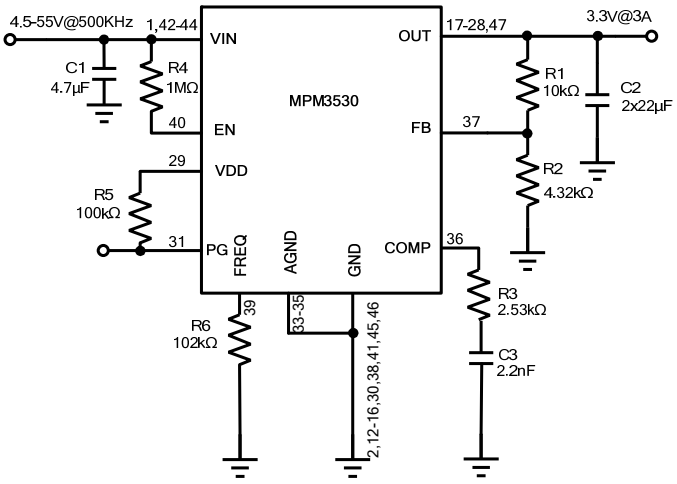

Figure 4: 3.3V Output Typical Application Circuit

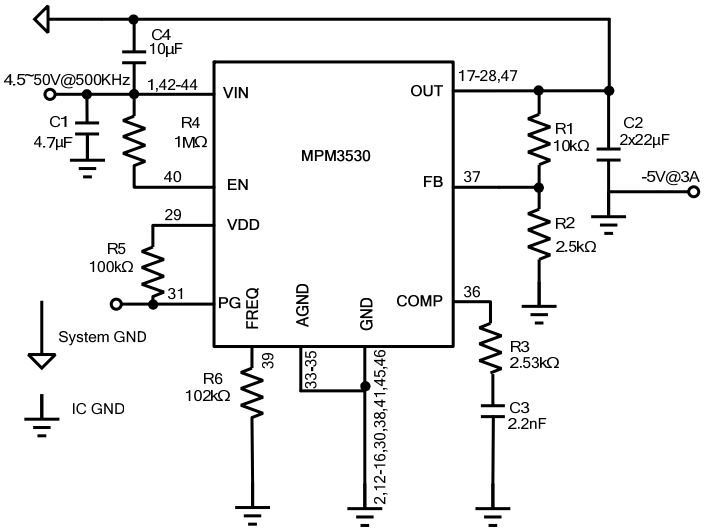

Figure 5: -5V Output Typical Application Circuit

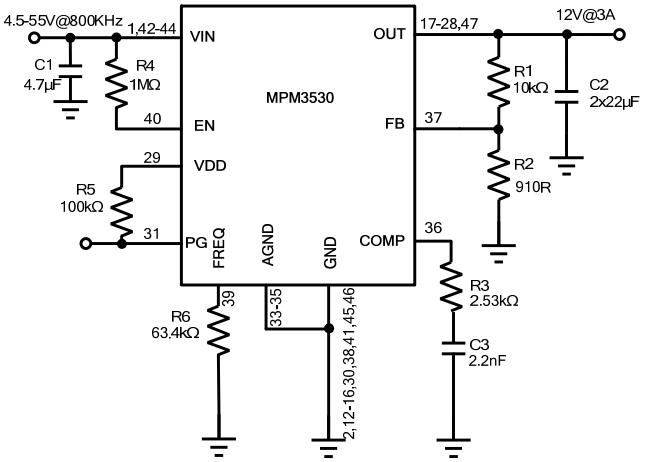

Figure 6: 12V Output Typical Application Circuit

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TYPICAL APPLICATION CIRCUITS *(continued)*

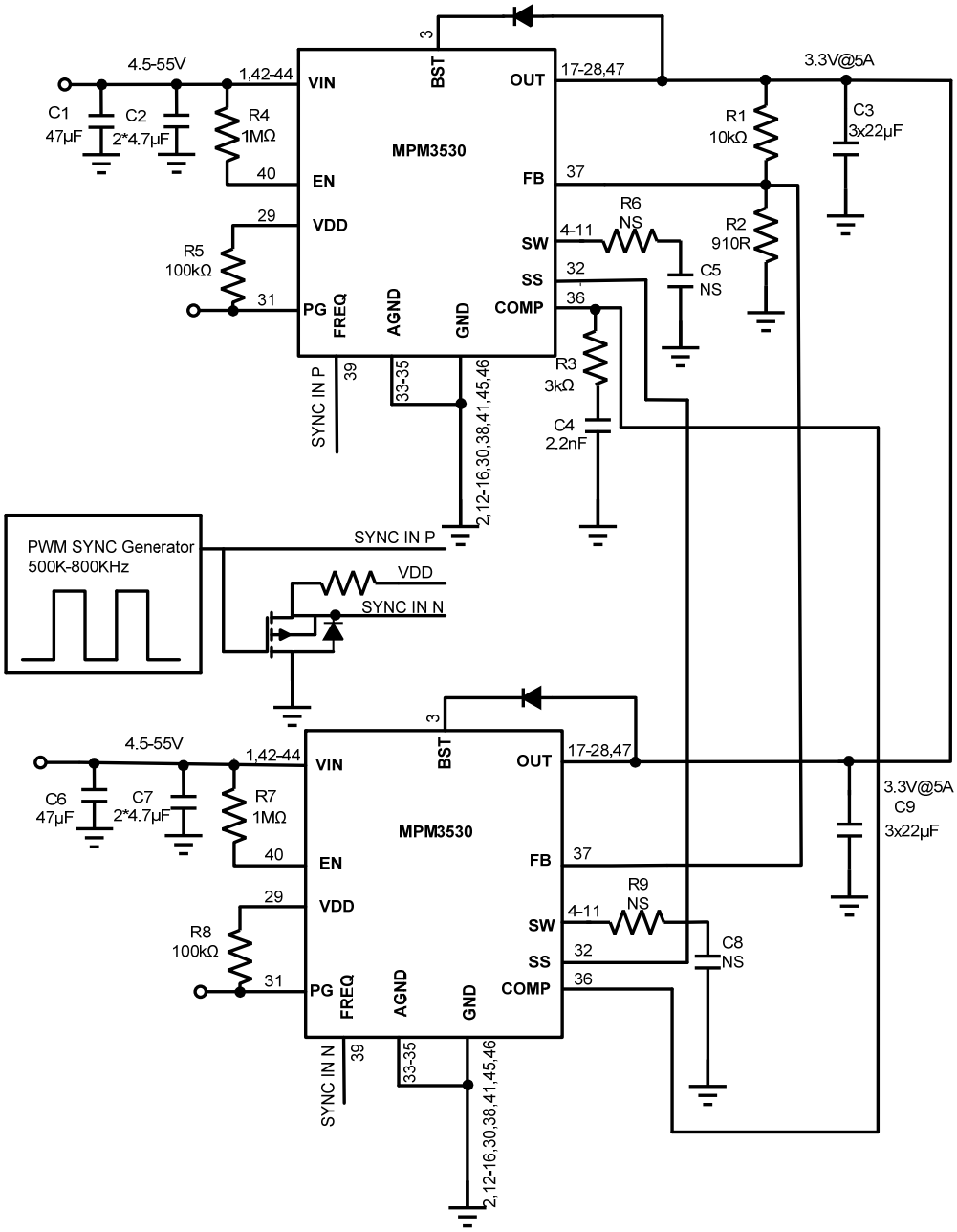

Figure 7: Two-Phase Parallel Connection Typical Application Circuit

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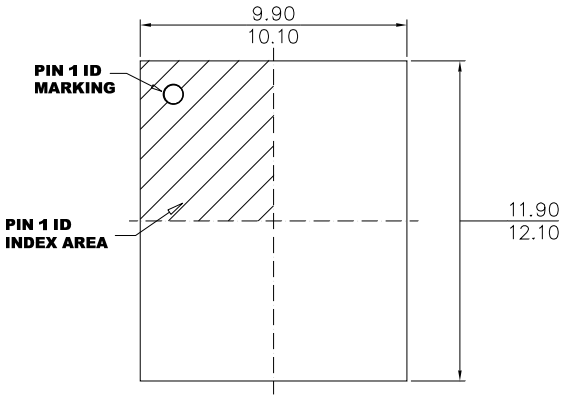
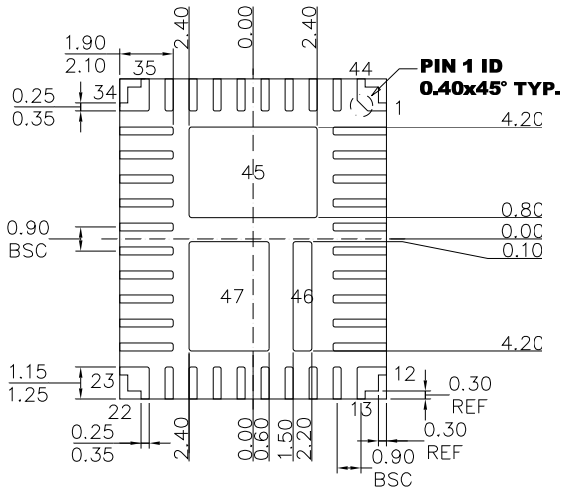
PACKAGE INFORMATION

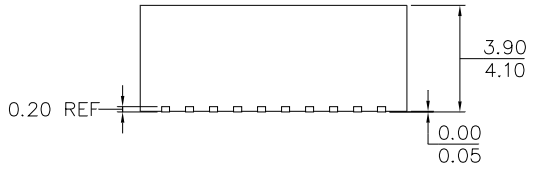
QFN-47 (10mmx12mmx4mm)



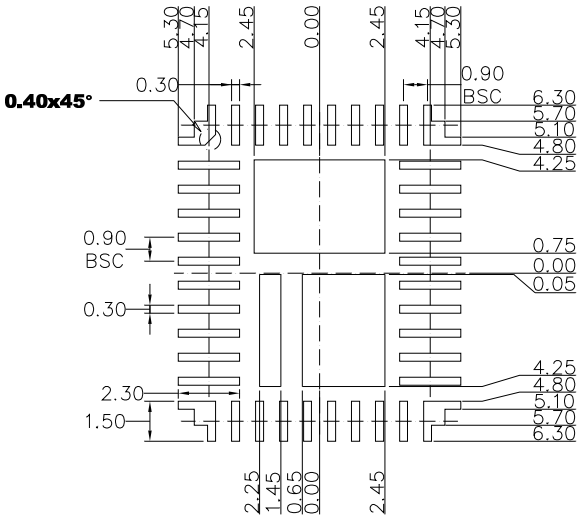
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	9/22/2018	Initial Release	-
1.2	11/9/2020	Updated EMI waveforms and EMI test circuit	9

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