MP3428A

19A, 600kHz, 20V Wide Input Range, Synchronous Boost Converter with Input Disconnect Function

The Future of Analog IC Technology®

DESCRIPTION

The MP3428A is a 600kHz, fixed frequency, high-efficiency, wide input range, current-mode boost converter with optional input disconnect and an input average current limit function. The input disconnect feature provides additional protection by isolating the input from the output during output short or shutdown. For battery-operated applications, this feature also helps in preventing battery depletion. With a programmable input average current limit, the MP3428A supports a wide range of applications, including POS, Thunderbolt, Bluetooth Audio, Power Banks, and Fuel Cells. The MP3428A features a 10mΩ, 24V power switch and a synchronous gate driver for high efficiency. An external compensation pin allows flexibility in setting loop dynamics and obtaining optimal transient performance at all conditions.

The MP3428A includes under-voltage lockout, switching current limiting, and thermal shutdown to prevent damage in the event of an output overload.

The MP3428A is available in a low-profile QFN-22 (3mm x 4mm) package.

FEATURES

- 3V to 20V Wide Input Range
- Integrated 10mΩ Low-Side Power FET
- SDR Driver for Synchronous Solution
- 19A Internal Switch Current Limit or External Programmable Input Current Limit
- Input Disconnect and Output SCP
- External Soft Start and Compensation for Higher Flexibility
- Programmable UVLO and Hysteresis
- < 1μA Shutdown Current
- Thermal Shutdown at 150°C
- Available in QFN-22 (3mm x 4mm) Package

APPLICATIONS

- Thunderbolt Interface
- Notebooks and Tablets
- Bluetooth Audio
- Power Banks
- Fuel Cells
- POS Systems
- Other Electronic Accessories

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

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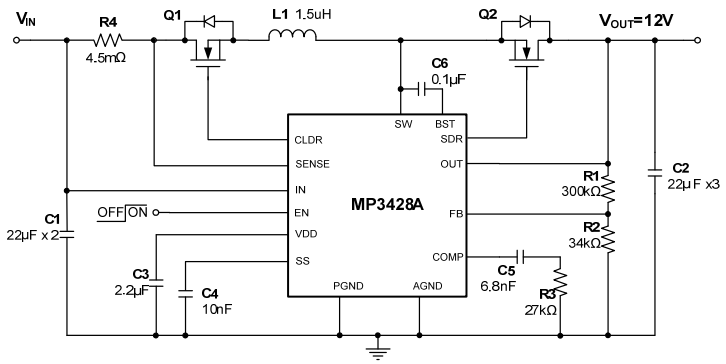
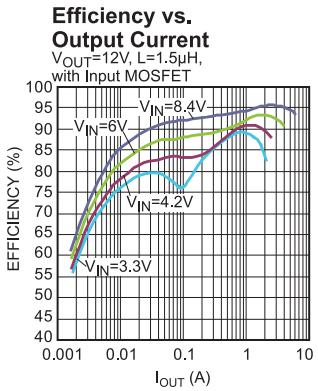
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3428AGL	QFN-22 (3mm x 4mm)	*See Below*

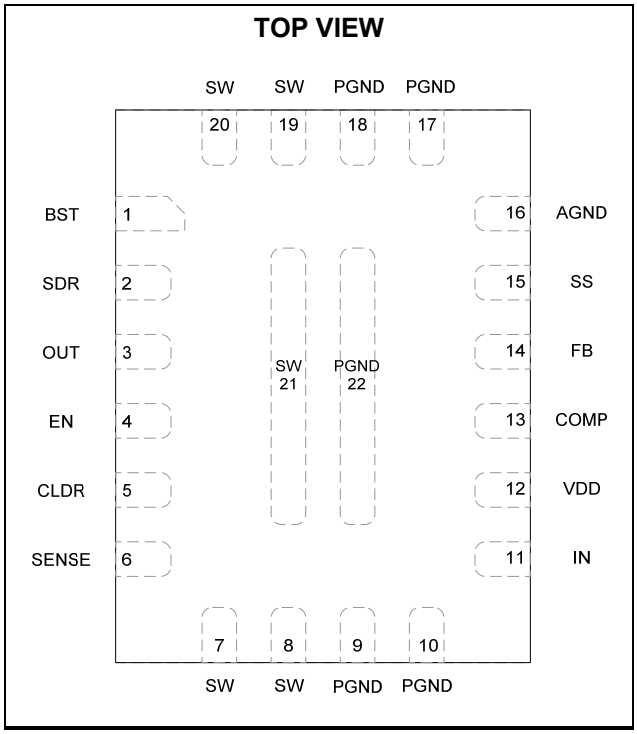
* For Tape & Reel, add suffix –Z (e.g. MP3428AGL–Z)

TOP MARKING

MPYW
3428
ALLL

MP: MPS prefix
Y: Year code
W: Week code
3428A: First five digits of the part number
LLL: Lot number

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

SW .....–0.3V to +24V (28V for <10ns)
IN, SENSE, OUT .....–0.3V to +24V
CLDR .....–0.3V to Vin +5.5V
BST, SDR .....–0.3V to Vsw +5.5V
All other pins .....–0.3V to +5.5V
EN bias current…… 0.5mA(2)
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (T_A= +25°C)(3)
..... 2.6W

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....3V to 20V
Output voltage (V_{OUT}).....V_{IN} to 22V
EN bias current……0mA to 0.3mA(2)
Operating junction temp.(T_J).... -40°C to +125°C

Thermal Resistance (5)	θ_{JA}	θ_{JC}	
QFN-22 (3mm x 4mm) ….	48	11	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) Refer to the "Enable and Programmable UVLO" section
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, T_J = -40°C 125°C, typical value is tested at 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating input voltage	V_{IN}		3		20	V
Input UVLO	IN_{UVLO-R}	V_{IN} rising	2.6	2.68	2.76	V
Input UVLO hysteresis	$IN_{UVLO-HYS}$			250		mV
Operating VDD voltage	V_{DD}	V_{IN} = 12V		5		V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on IN, T_J = 25°C			1	μA
Quiescent current	I_{Q-OUT}	V_{FB} = 1.35V, V_{IN} = 3.3V, V_{OUT} = 12V, no switching, measured on OUT		650	750	μA
	I_{Q-IN}	V_{FB} = 1.35V, V_{IN} = 3.3V, V_{OUT} = 12V, no switching, Measured on IN		110	150	
Switching frequency	F_S	T_J = 25°C	510	600	690	kHz
		T_J = -40°C to 125°C	450		690	
Minimum off time (6)	$T_{MIN-OFF}$	V_{FB} = 0V		280		ns
Minimum on time (6)	T_{MIN-ON}			120		ns
EN turn-on threshold	V_{EN-ON}	V_{EN} rising (switching)	1.27	1.33	1.39	V
EN high threshold	V_{EN-H}	V_{EN} rising (micro power)			1.0	V
EN low threshold	V_{EN-L}	V_{EN} falling (micro power)	0.4			V
EN turn-on hysteresis current	I_{EN-HYS}	1.0V < EN < 1.4V	3	4.5	6	μA
EN input bias current	I_{EN}	V_{EN} = 0V, 3.3V		0		μA
Soft-start charge current	I_{SS}		5	7	9	μA
FB reference voltage	V_{FB}	T_J = 25°C	1.212	1.225	1.238	V
		T_J = -40°C to 125°C	1.207	1.225	1.243	
FB input\bias current	I_{FB}	V_{FB} = 1V	–50			nA
SDR rise time(6)	$T_{SDR-Rise}$	C_{Load} = 2.7nF, test from 10% to 90%		20		ns
SDR fall time(6)	$T_{SDR-Fall}$	C_{Load} = 2.7nF, test from 90% to 10%		30		ns
Error amp voltage gain(7)	A_{V-EA}			300		V/V
Error amp transconductance	G_{EA}			160		μA/V
Error amp max. output current		V_{FB} = 1V or 1.5V		22		μA
Current to COMP gain	Gcs	V_{CLDR} = GND		27		A/V
Sense to COMP gain	Gxcs	CLDR float, $\Delta V_{SENSE}/\Delta V_{COMP}$		103		mV/V
Comp threshold for switching (6)	V_{PSM}			0.5		V
Comp high clamp				2		V
SW on-resistance	R_{ON}			10		mΩ

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, T_J = -40°C 125°C, typical value is tested at 25℃, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SW current limit	I_{LIMT}	V_{CLDR} = GND, duty cycle = 40%	19	25	29	A
External sense average current limit	V_{CL}	CLDR float	45	54	63	mV
Linear charge start-up SCP blanking time	T_{CL}	CLDR float		0.5		ms
Thermal shutdown(6)	T_{SD}			150		°C
Thermal shutdown hysteresis(6)	T_{SD-HYS}			25		°C

NOTES:
6) Guaranteed by characterization, not tested in production.
7) Guaranteed by design.

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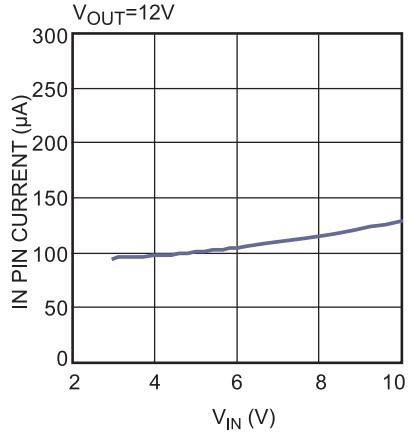
TYPICAL ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L = 1.5μH, T_A = 25°C, unless otherwise noted.

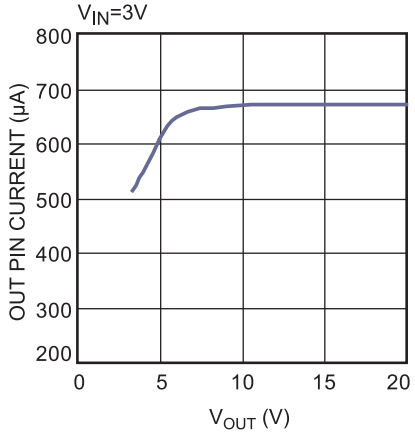
IN Quiescent Current vs. Input Voltage

V_{OUT}=12V



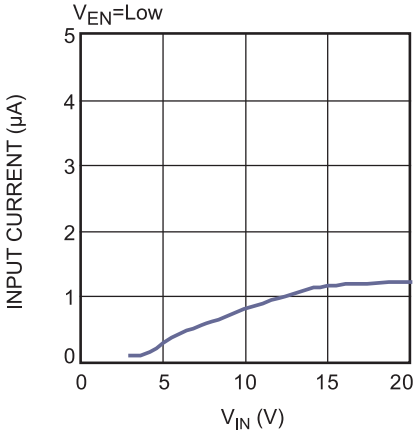
OUT Quiescent Current vs. Output Voltage

V_{IN}=3V

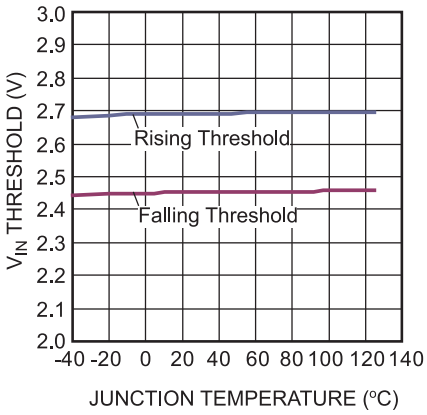


Shutdown Current vs. Input Voltage

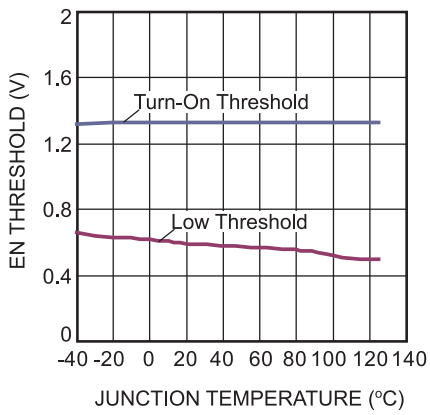
V_{EN}=Low



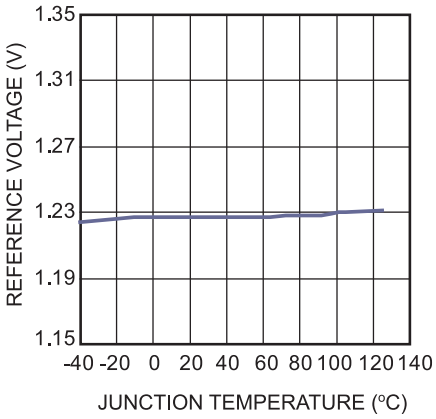
VIN UVLO Threshold vs. Temperature



EN Threshold vs. Temperature

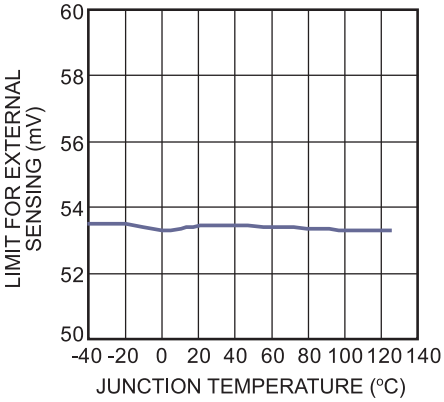


FB Reference Voltage vs. Temperature

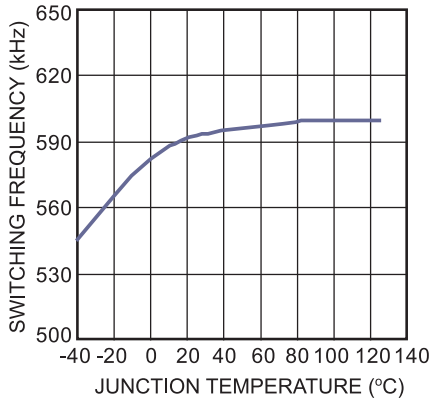


External Sense Average Current Limit vs. Temperature

V_{CLDR}=Float

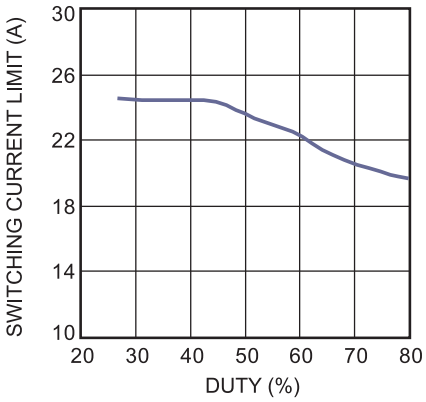


Switching Frequency vs. Temperature



Internal Current Limit vs. Duty

V_{CLDR}=GND



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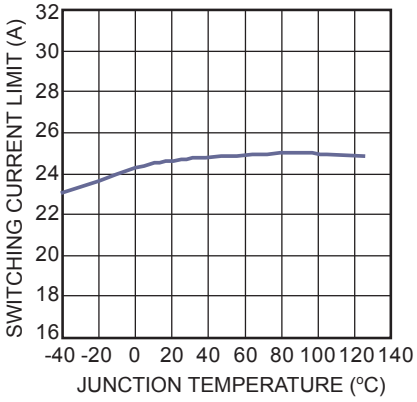
TYPICAL ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L = 1.5μH, T_A = 25°C, unless otherwise noted.

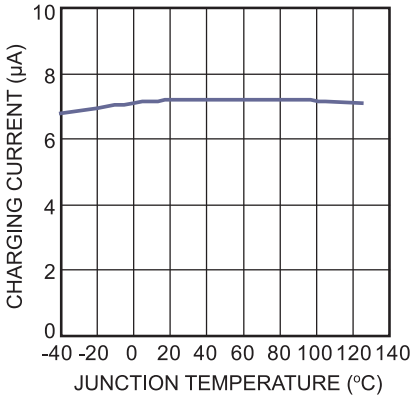
Internal Current Limit vs.Temperature

V_{CLDR}=GND, DUTY=40%



SS Charge Current vs. Temperature

V_{SS}=0V



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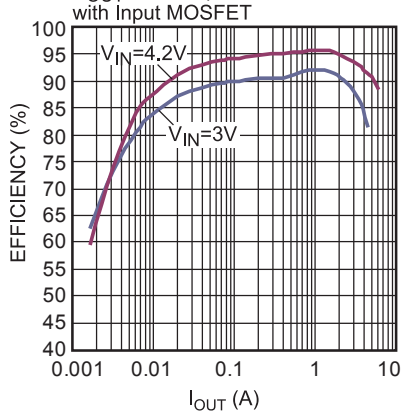
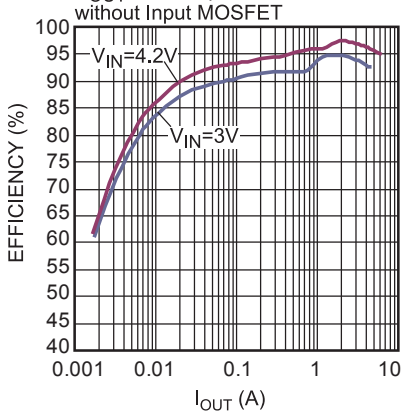
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5μH, I_{OUT} = 2A, C_{OUT} = 22μF*3, R_{SENSE} = 4.5mΩ, add input disconnect and output SCP MOSFET, tested on 4-layer board, T_A = 25°C, unless otherwise noted.

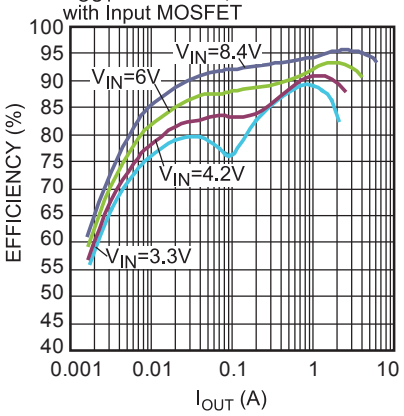
Efficiency vs. Output Current
V_{OUT}=5V, L=1μH, with Input MOSFET



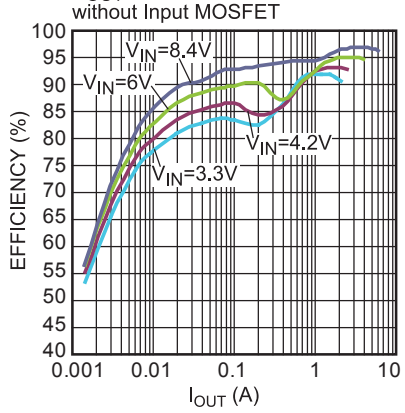
Efficiency vs. Output Current
V_{OUT}=5V, L=1μH, CLDR=GND, without Input MOSFET



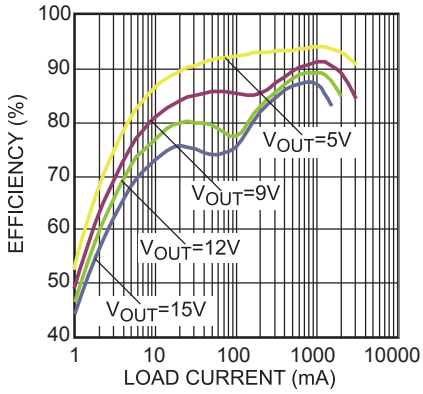
Efficiency vs. Output Current
V_{OUT}=12V, L=1.5μH, with Input MOSFET



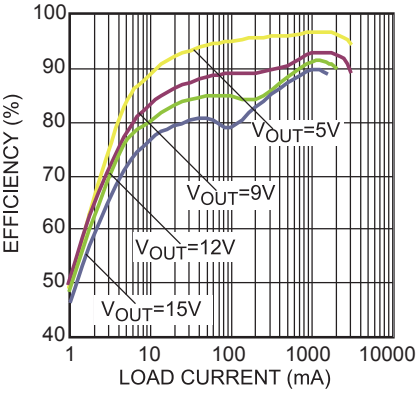
Efficiency vs. Output Current
V_{OUT}=12V, L=1.5μH, CLDR=GND, without Input MOSFET



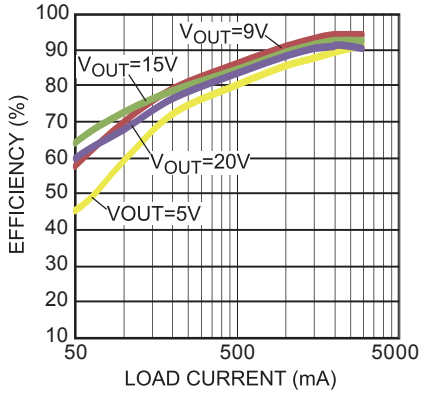
Efficiency For Figure 10
V_{IN}=3.3V



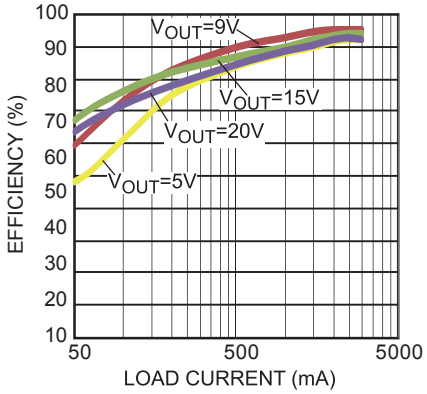
Efficiency For Figure 10
V_{IN}=4.2V



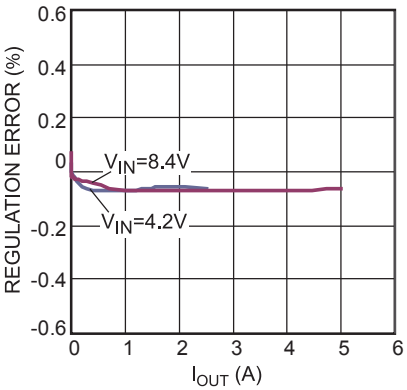
Efficiency For Figure 11
V_{IN}=6.6V



Efficiency For Figure 11
V_{IN}=8.4V



Load Regulation



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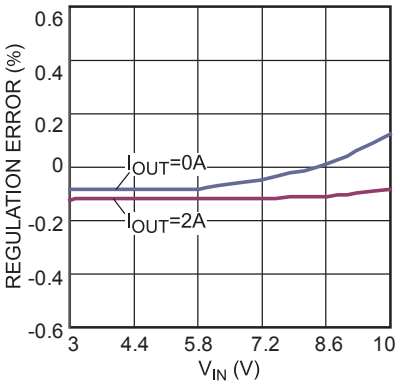
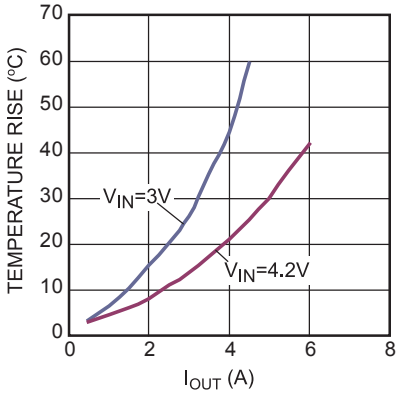
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5μH, I_{OUT} = 2A, C_{OUT} = 22μF*3, R_{SENSE} = 4.5mΩ, add input disconnect and output SCP MOSFET, tested on 4-layer board, T_A = 25°C, unless otherwise noted.

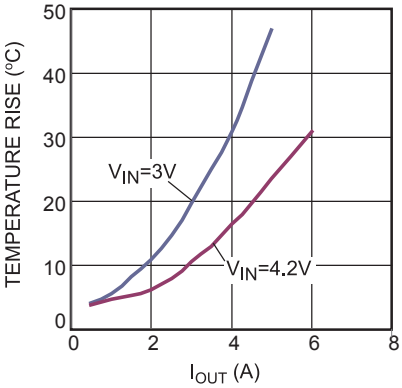
Line Regulation



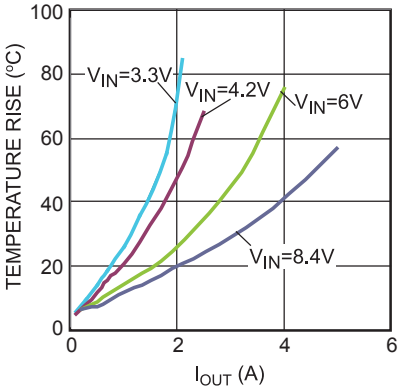
Case Temperature Rise
V_{OUT}=5V, L=1μH, with Input MOSFET



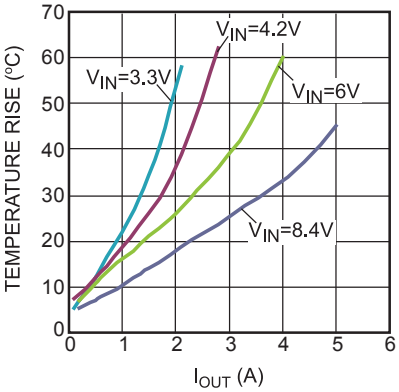
Case Temperature Rise
V_{OUT}=5V, L=1μH, CLDR=GND, without Input MOSFET



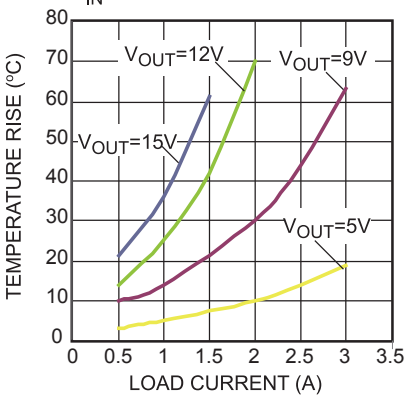
Case Temperature Rise
V_{OUT}=12V, with Input MOSFET



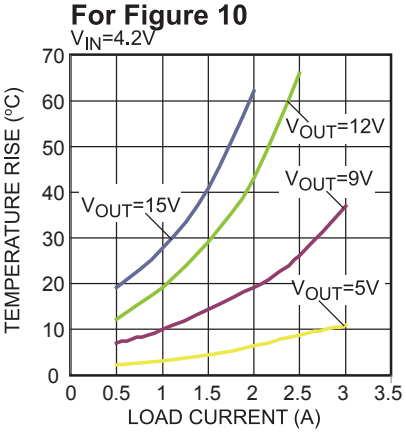
Case Temperature Rise
V_{OUT}=12V, CLDR=GND, without Input MOSFET



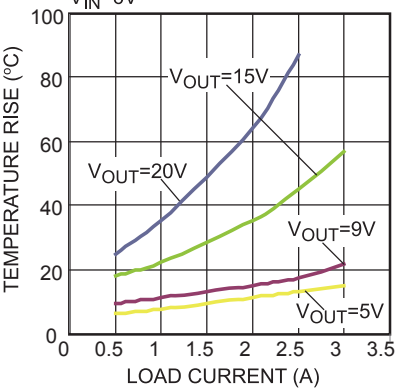
Case Temperature Rising For Figure 10
V_{IN}=3.3V



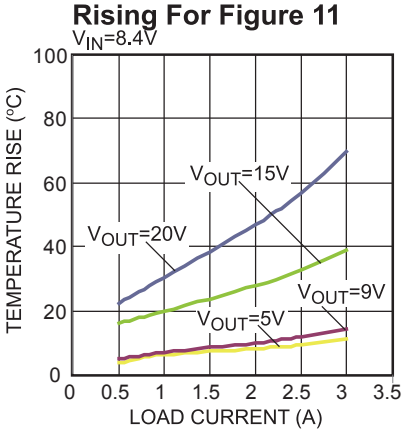
Case Temperature Rising For Figure 10
V_{IN}=4.2V



MP3428A Case Temperature Rising For Figure 11
V_{IN}=6V



MP3428A Case Temperature Rising For Figure 11
V_{IN}=8.4V



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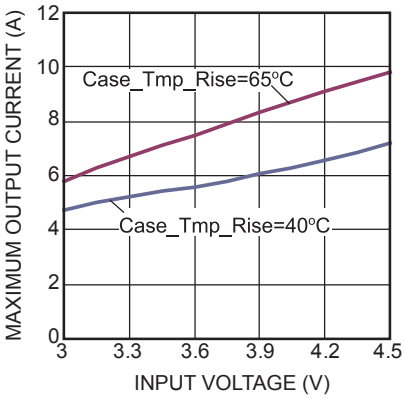
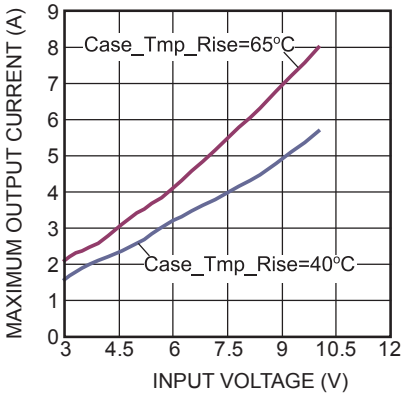
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5μH, I_{OUT} = 2A, C_{OUT} = 22μF*3, R_{SENSE} = 4.5mΩ, add input disconnect and output SCP MOSFET, T_A = 25°C, unless otherwise noted.

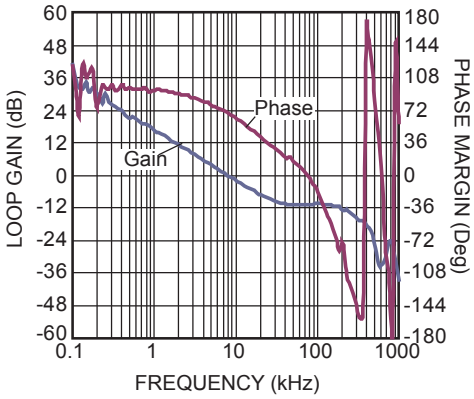
Load Capability
V_{OUT}=5V, CLDR=GND, without Input MOSFET



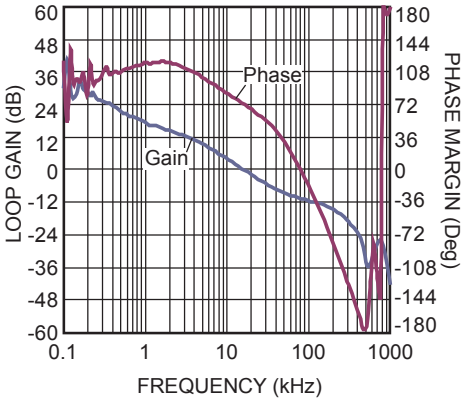
Load Capability
V_{OUT}=12V, CLDR=GND, without Input MOSFET



Bode Plot
V_{IN}=3.3V, I_{OUT}=2A



Bode Plot
V_{IN}=6V, I_{OUT}=4A



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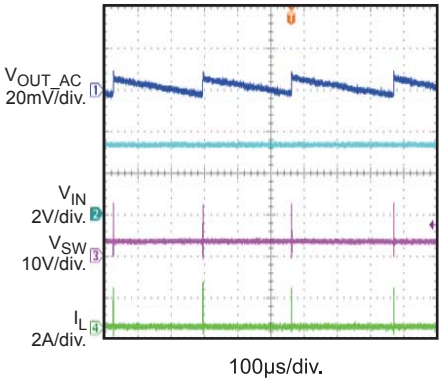
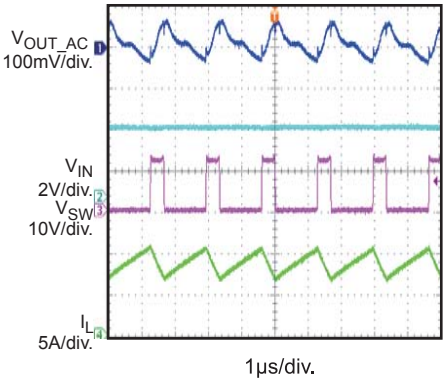
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5μH, I_{OUT} = 2A, C_{OUT} = 22μF*3, R_{SENSE} = 4.5mΩ, add input disconnect and output SCP MOSFET, T_A = 25°C, unless otherwise noted.

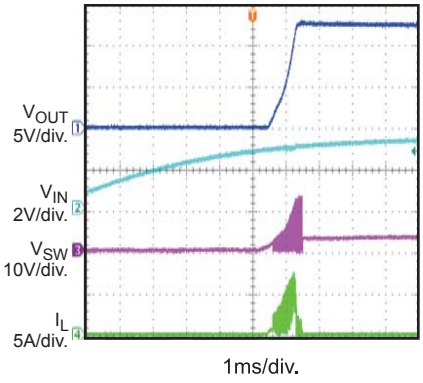
Steady State
I_{OUT}=0A



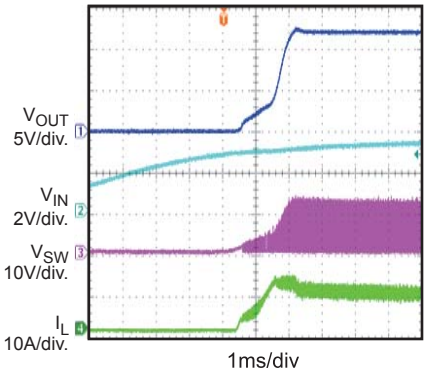
Steady State
I_{OUT}=2A



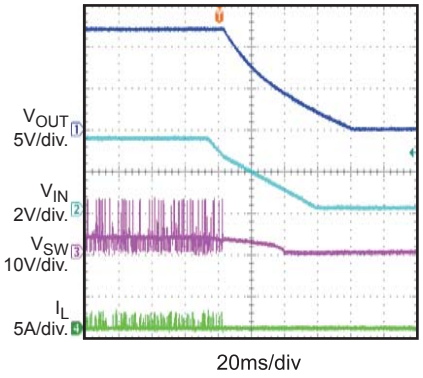
V_{IN} Start-Up
I_{OUT}=0A



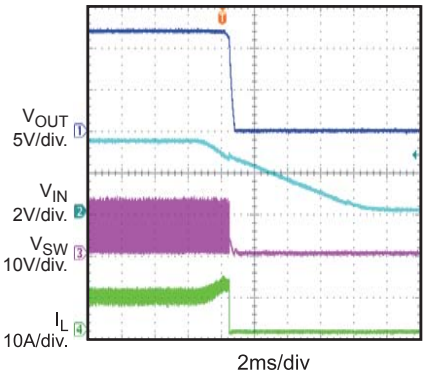
V_{IN} Start-Up
I_{OUT}=2A



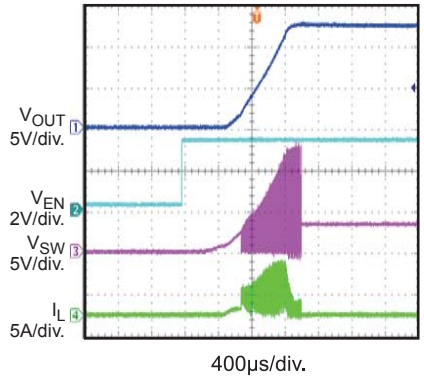
V_{IN} Shutdown
I_{OUT}=0.01A



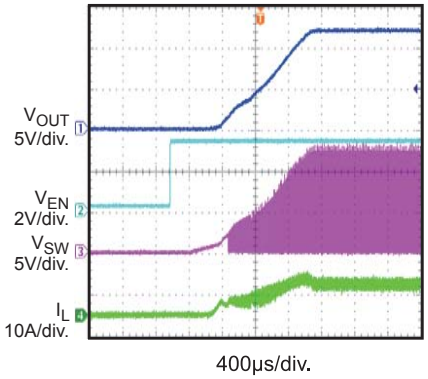
V_{IN} Shutdown
I_{OUT}=2A



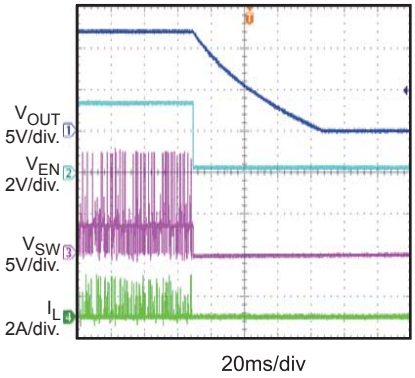
EN Start-Up
I_{OUT}=0A



EN Start-Up
I_{OUT}=2A



EN Shutdown
I_{OUT}=0.01A



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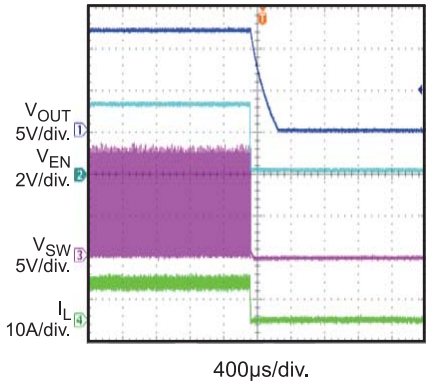
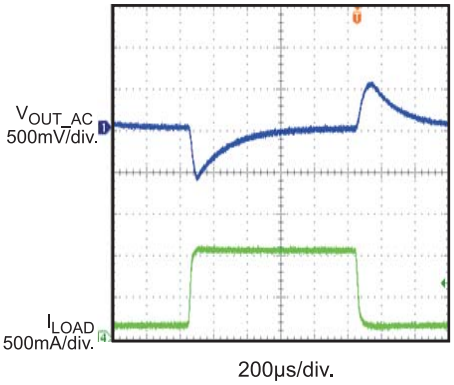
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5μH, I_{OUT} = 2A, C_{OUT} = 22μF*3, R_{SENSE} = 4.5mΩ, add input disconnect and output SCP MOSFET, T_A = 25°C, unless otherwise noted.

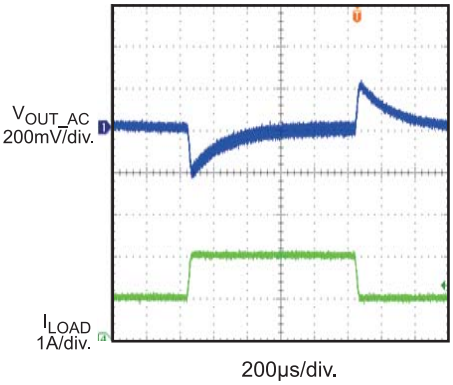
EN Shutdown
I_{OUT}=2A



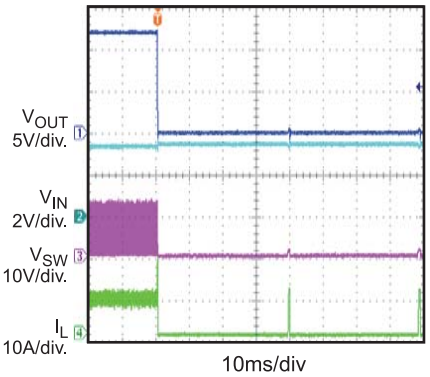
Response to Transient Load
V_{IN}=6V, I_{OUT}=0.1A to 1A@25mA/μs



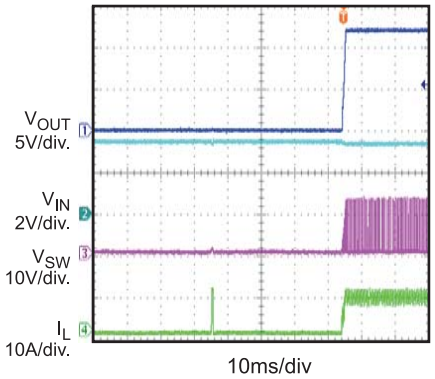
Response to Transient Load
V_{IN}=6V, I_{OUT}=1A to 2A@25mA/μs



Response to Output Short
I_{OUT}=2A



Recovery from Output Short
I_{OUT}=2A



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PIN FUNCTIONS

Package Pin #	Name	Description
1	BST	**Bootstrap.** BST powers the SDR driver.
2	SDR	**Synchronous gate driver for the output rectifier.**
3	OUT	**Samples the output voltage and charges the BST capacitor**. VDD is powered from OUT when V_{OUT} is higher than V_{IN}.
4	EN	**Regulator on/off control input**. EN high turns on the internally regulator circuit. EN low turns off the regulator circuit. An input higher than the EN turn-on threshold will enable the IC to start switching. When not used, connect EN to the input source (through a 100kΩ pull-up resistor if VIN > 5.5V) for automatic start-up. Also, EN can be used to program Vin UVLO. Do NOT leave EN floating.
5	CLDR	**Driver for the input disconnect MOSFET.** If it's connected to the gate of the input MOSFET or floating, an external current-sense resistor is needed. Connect CLDR to GND to use the internal current sense circuit. Do NOT pull CLDR down to GND through a resistor.
6	SENSE	**Voltage sense.** Voltage sensed between SENSE and IN determines the external current-sense signal. Connect SENSE to IN if the internal current sense solution is selected.
7,8,19,20,21	SW	**Power switch output.** SW is the drain of the internal power MOSFET. Connect the power inductor and output rectifier to SW.
9,10,17,18,22	PGND	**Power ground.**
11	IN	**Input supply.** IN must be bypassed locally.
12	VDD	**Internal bias supply.** Decouple with a 2.2μF ceramic capacitor as close to VDD as possible.
13	COMP	**Compensation.** Connect a capacitor and resistor in series to analog ground for loop stability.
14	FB	**Feedback input.** The reference voltage is 1.225V. Connect a resistor divider from V_{OUT} to FB.
15	SS	**Soft-start control.** Connect a soft-start capacitor to SS. The soft-start capacitor is charged with a constant current. Leave SS disconnected if the soft start is not used.
16	AGND	**Analog ground.**

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FUNCTIONAL BLOCK DIAGRAM

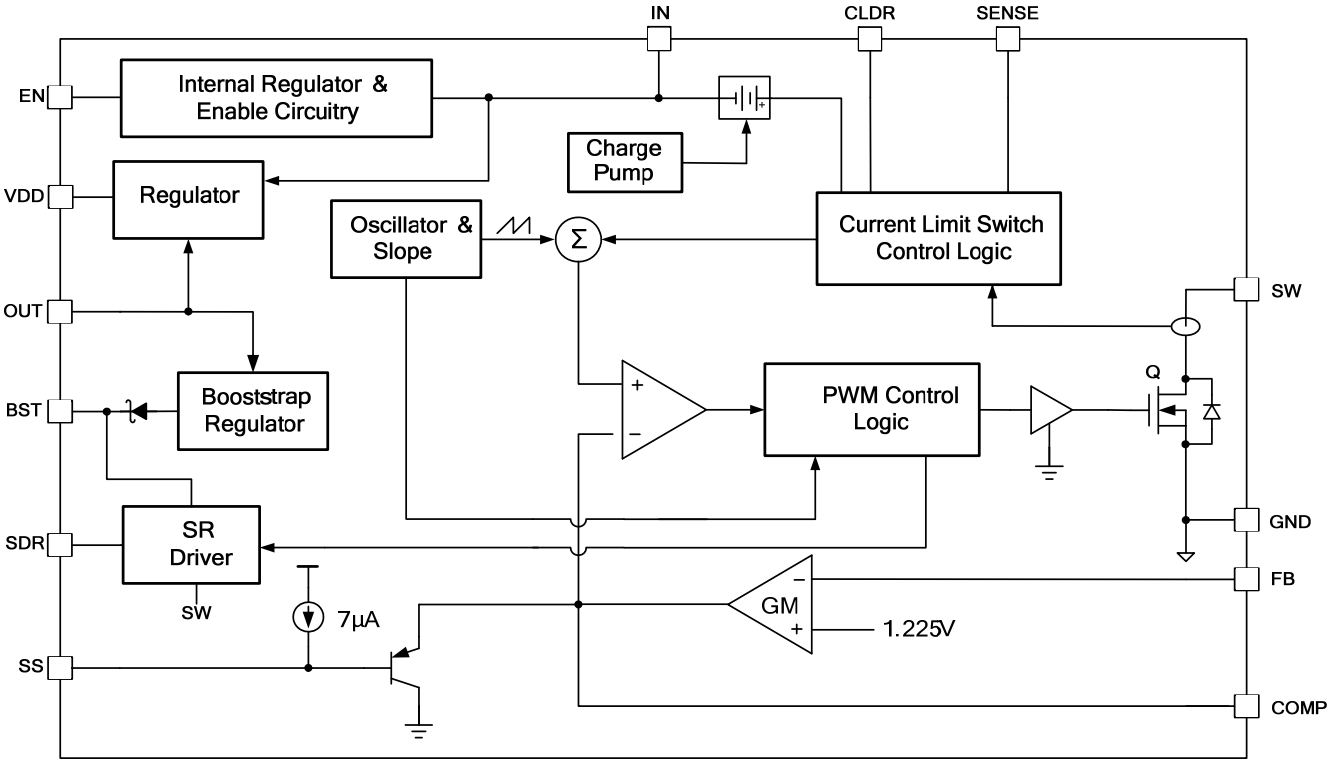

Figure 1: Functional Block Diagram

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OPERATION

Boost Function

The MP3428A uses a constant frequency, peak current mode, boost regulation architecture to regulate the output voltage.

At the beginning of each cycle, the N-channel MOSFET switch Q is turned on, forcing the inductor current to rise. The current flowing through switch Q is measured externally (or measured internally when CLDR is connected to GND) and converted to a voltage by the current amplifier. That voltage is compared with the error voltage on the internal COMP, which is a buffer voltage from the external COMP pin during normal operation. The voltage on the external COMP pin is an amplified version of the difference between the 1.225V reference voltage and the feedback voltage. When the sensed voltage is equal to the buffered COMP voltage, the PWM comparator turns off switch Q, forcing the inductor current into the output capacitor through the external rectifier. This causes the inductor current to decrease. The peak inductor current is controlled by the voltage on COMP, which in turn is controlled by the output voltage. Thus the output voltage is regulated by the inductor current to satisfy the load. Current mode regulation improves the transient response and control loop stability.

VDD Power

The MP3428A internal circuit is powered by VDD. A ceramic capacitor (no lower than 2.2μF) is required to decouple VDD. During start-up, VDD power is regulated from IN. Once the output voltage exceeds the input voltage, VDD is powered from V_{OUT} instead of V_{IN}. This allows the MP3428A to maintain low R_{ON} and high efficiency even with low input voltage.

Soft Start (SS)

The MP3428A uses one external capacitor on SS to control the switching frequency during start-up. The operation frequency is initially 1/4 of the normal frequency. As the SS capacitor is charged (the charging happens after the MP3428A runs in boost operation), the frequency increases continually. When the voltage on SS exceeds 0.65V, the frequency switches to a normal frequency. In addition, the voltage on COMP is clamped within V_{SS} + 0.7V. So during start-up, the COMP voltage reaches 0.7V quickly and then rises at the same rate of V_{SS}. These two mechanisms prevent high inrush current from the input power supply.

SDR and BST Function

The MP3428A generates a synchronous gate driver, which is complementary to the gate driver of the internal low-side MOSFET. The SDR driver is powered from BST (5V, typically). A low Q_G, N-channel MOSFET with a gate threshold voltage lower than 2.5V is preferred for synchronous rectification. In high-power application, using a synchronous rectifier switch improves the overall converting efficiency. If a synchronous rectifier switch is not used, float SDR.

The 5V BST voltage is powered from OUT. If the output voltage is low or the duty cycle is too low, the BST voltage may not be regulated to 5V, triggering a BST_UVLO. If this condition occurs, a Schottky diode from an external 5V source to BST is recommended. Otherwise the SDR driver signal may be lost.

Current Sensing Configuration

The MP3428A offers the option of using an internal circuit or an external resistor to sense the inductor current. When using an internal current-sense circuit, the CLDR must be connected directly to GND before powering on. Meanwhile, SENSE should be connected to IN. In this condition, the internally sensed current is compared to both the COMP voltage and the peak inductor current limit to generate the duty cycle.

When CLDR is connected to the gate of the input MOSFET or left floating before powering on, the inductor current is sensed by an external resistor between IN and SENSE. Under this configuration, the externally sensed current is compared with COMP for low-side switch on/off control. The over-load protection or disconnect function is achieved by

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monitoring the average input current through the external sensing resistor (see the "Protection and Input Disconnect Function" section below for additional details).

Protection and Input Disconnect Function

The MP3428A features excellent OCP and SCP.

During start-up, the MP3428A monitors the voltage on CLDR to determine internal or external current sensing. Connecting CLDR to the gate of an external MOSFET or leaving it floating selects an external sensing resistor; connecting CLDR directly to GND selects an internal sensing circuit.

If internal current sensing is selected, OCP is achieved by limiting the peak inductor current in every switching cycle (without hiccup in OCP) unless V_{OUT} is pulled below V_{IN}. After the SS voltage exceeds about 0.7V, the MP3428A may run in hiccup if it detects that the output voltage is lower than the input voltage. This prevents the MP3428A from damage even if there isn't an input disconnecting MOSFET during a heavy-load condition.

If external current sensing is selected, CLDR is charged by a typical 13μA current from the internal charge pump. Once the voltage on CLDR reaches the MOSFET's threshold, the input current is generated, charging up the output capacitors, and hence the output voltage follows the CLDR voltage with a MOSFET (V_{TH}) threshold difference. The MP3428A has a current feedback loop to control the CLDR and COMP voltage, so the input current will not exceed V_{CL}(mV)/R_{SENSE}(mΩ).

During start-up with external current sensing (if V_{CLDR} is lower than V_{IN} + 1.6V), the linear charge current limit works with the V_{CL}/R_{SENSE} limitation (V_{CLDR} is regulated to limit the current), and the MP3428A shuts down if the linear charge current limit is triggered for more than 0.5ms by pulling CLDR down to GND. The MP3428A will wait for 20ms~70ms (the hiccup time depends on V_{IN} and V_{OUT}) to restart if it is not reset by V_{IN} or EN. A normal load will not lead to hiccup protection during start-up.

If V_{CLDR} is higher than V_{IN} + 1.6V, boost switching is enabled. SS is charged, and the power MOSFET turns on/off periodically to regulate V_{OUT} following the SS signal. When the MP3428A starts switching, and V_{OUT} is lower than V_{IN}, both the linear charge current limit (regulated CLDR voltage) and the boost input average current limit (regulated COMP voltage) begin to work; both the control loops work with the limit of V_{CL}/R_{SENSE}.

After V_{OUT} is charged higher than V_{IN} in boost mode, only the boost input average current limit works (regulated COMP voltage). The MP3428A will not trigger hiccup OCP unless the SS voltage is higher than 0.7V, and V_{OUT} drops lower than V_{IN}. If hiccup protection is triggered in switching mode, the switching stops, and CLDR is pulled low. It will re-start after 20ms~70ms, depending on V_{IN} and V_{OUT}. The recovery process is the same as the start-up process.

Table 1 shows the detailed over-current-protection mode when using an external current-sense resistor.

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Table 1: MP3428A OCP Mode when Using an External Current-Sense Resistor

Condition	Work Mode	OCP Action
$V_{CLDR} < V_{IN} + 1.6V$	Linear charge mode, no boost switching	Linear charge current limit works: (1) V_{CLDR} is regulated down to keep the input current at V_{CL}/R_{SENSE}. (2) If the linear charge OCP lasts 0.5ms, the MP3428A triggers hiccup protection. Boost input average current limit does not work.
$V_{CLDR} \geq V_{IN} + 1.6V$ (8) $V_{OUT} \leq V_{IN}$ $V_{SS} \leq 0.7V$	Boost switching	Linear charge current limit works: (1) V_{CLDR} is regulated down to keep the input current at V_{CL}/R_{SENSE}. (2) If the linear charge OCP lasts 0.5ms, the MP3428A triggers hiccup protection. Boost input average current limit works: (1) COMP voltage is regulated to keep the input average current at V_{CL}/R_{SENSE}.
$V_{CLDR} \geq V_{IN} + 1.6V$ (8) $V_{OUT} \leq V_{IN}$ $V_{SS} > 0.7V$	Boost switching	Runs into hiccup protection without delay.
$V_{CLDR} \geq V_{IN} + 1.6V$ (8) $V_{OUT} > V_{IN}$	Boost switching	The linear charge current limit does not work. V_{CLDR} remains high. Boost input average current limit works. (1) COMP voltage is regulated to keep the input average current at V_{CL}/R_{SENSE}, no hiccup.

NOTE:

8) After start-up, the $V_{CLDR} \geq V_{IN} + 1.6V$ condition is registered if V_{CLDR} is higher than $V_{IN} + 1.6V$ one time. This means the MP3428A treats the condition as $V_{CLDR} \geq V_{IN} + 1.6V$ even if V_{CLDR} falls below $V_{IN} + 1.6V$ again in protection mode (unless it is turned off by the hiccup protection or by the power re-cycle).

If the inductor current ramps quickly and the inductor peak current exceeds 100(mV)/R_{SENSE}(mΩ), the MP3428A shuts down immediately, entering SCP hiccup. This fast protection allows the MP3428A to survive all SCP events.

When the MP3428A is shut down by EN or V_{IN}, CLDR is pulled down to GND, so the output and input are well isolated by the input MOSFET. This is the V_{IN}-to-V_{OUT} disconnecting function.

Light-Load Operation

To optimize efficiency at light load, the MP3428A employs a foldback frequency and a pulse-skipping mechanism. When the load becomes lighter, the COMP voltage decreases, causing the MP3428A to enter foldback operation (the lighter the load, the lower the frequency). However, if the load becomes exceedingly low, the MP3428A enters PSM. PSM operation is optimized so that only one switching pulse is launched in every burst cycle.

Enable (EN) and Programmable UVLO

EN enables and disables the MP3428A. When voltage higher than V_{EN_H} (1V) is applied, the MP3428A starts up some of the internal circuits (micro-power mode). If the EN voltage continues to increase higher than V_{EN_ON} (1.33V), the MP3428A enables all functions and begins to boost operation. Boost operation is disabled if the EN voltage is lower than V_{EN_ON} (1.33V). To shut down the MP3428A completely, a voltage less than V_{EN_L} (0.4V) is required on EN. After shutdown, the MP3428A sinks a current less than 1μA from the input power.

The maximum recommended voltage on EN is 5.5V. If the EN control signal comes from a voltage higher than 5.5V, a resistor should be added between EN and the control source. An internal Zener diode on EN clamps the EN voltage to prevent runaway. Ensure the Zener clamped current flowing into EN is less than 0.3mA.

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EN can be used to program Vin's UVLO (see the "Applications\UVLO Hysteresis" section for additional details.

Output Over-Voltage Protection

Except for controlling the COMP signal to regulate the output voltage, the MP3428A also provides over-voltage protection. If the FB voltage is higher than 108% of the reference voltage, boost switching stops. When the FB voltage drops below 104% of the reference voltage, the device resumes switching automatically.

Thermal Shutdown

The device has an internal temperature monitor. If the die temperature exceeds 150°C, the converter shuts down. Once the temperature drops below 125°C, the converter will turn on again.

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APPLICATION INFORMATION

Components referred to below apply to the "Typical Application" circuit.

Selecting the Current Limit Resistor

The MP3428A features an average current limit when the external sensing resistor is used. The resistor (R_{SENSE}) connected between IN and SENSE sets the current limit (I_{CL}). See Equation (1):

$$I_{CL} = V_{CL} / R_{SENSE} \quad (1)$$

Where, V_{CL} is 54mV, typically, I_{CL} is in amperes, and R_{SENSE} is in mΩ.

Considering the parasitic inductance on the sense resistor, a small package resistor (e.g., 0805 package) is recommended. (Add several parallel resistors if the power rating is lower than requested.) To reduce the affection of parasitic resistance and noise, a sense resistor with higher than 4mΩ resistance is recommended.

UVLO Hysteresis

The MP3428A features a programmable UVLO hysteresis. When powering up, EN sinks a 4.5μA current from the upper resistor, R_{TOP} (see Figure 2). VIN must increase in voltage to overcome the current sink. The VIN start-up threshold is determined by Equation (2):

$$V_{IN-ON} = V_{EN-ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 4.5\mu A \times R_{TOP} \quad (2)$$

Where, V_{EN-ON} is the EN voltage turn-on threshold (1.33V, typically).

Once the EN voltage reaches V_{EN-ON}, the 4.5μA sink current turns off to create a reverse hysteresis for the VIN falling threshold. See Equation (3):

$$V_{IN-UVLO-HYS} = 4.5\mu A \times R_{TOP} \quad (3)$$

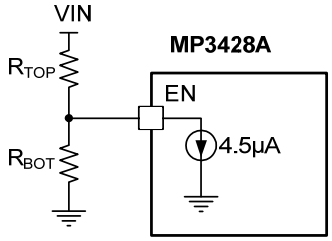

Figure 2: V_{IN} VULO Program

Selecting the Soft-Start Capacitor

The MP3428A includes a soft-start circuit that limits the voltage on COMP during start-up to prevent excessive input current. This prevents premature termination of the source voltage at start-up due to input current overshoot. When power is applied to the MP3428A and enable is asserted, a 7μA internal current source charges the external capacitor at SS. The SS voltage clamps the COMP voltage (as well as the inductor peak current) until the output is close to regulation or until COMP reaches 2V. For most applications, a 10nF SS capacitor is sufficient. If the output capacitance is large or the front power supply cannot withstand the huge inrush current, SS capacitors can be increased properly.

Setting the Output Voltage

The output voltage is fed back through two sense resistors in series. The feedback reference voltage is 1.225V, typically. The output voltage is determined with Equation (4):

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2}) \quad (4)$$

Where:
R1 is the top feedback resistor.
R2 is the bottom feedback resistor.
V_{REF} is the reference voltage (1.225V, typically).

Choose the feedback resistors in the 10kΩ range (or higher) for good efficiency.

Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low ESR capacitor is required to minimize noise. Ceramic capacitors are preferred, but tantalum or low ESR electrolytic capacitors will suffice.

At least two 22μF capacitors are recommended for high-power applications, considering loop stability. The capacitor can be electrolytic, tantalum, or ceramic. However, since the capacitor absorbs the input switching current, it requires an adequate ripple current rating. Use a capacitor with a RMS current rating greater than the inductor ripple current (see the "Selecting the Inductor" section to determine the inductor ripple current).

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To ensure stable operation, place the input capacitor as close to the IC as possible. Alternately, a smaller, high-quality 0.1μF ceramic capacitor may be placed closer to the IC while the larger capacitor placed farther away. If using this technique, a larger electrolytic or tantalum type capacitor is recommended. All ceramic capacitors should be placed close to the MP3428A input.

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to minimize the output voltage ripple. The characteristics of the output capacitor affect the stability of the regulation control system. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. If using ceramic capacitors, the impedance of the capacitor at the switching frequency is dominated by the capacitance, so the output voltage ripple is independent of the ESR. The output voltage ripple is estimated with Equation (5):

$$V_{RIPPLE} = \frac{(1-\frac{V_{IN}}{V_{OUT}}) \times I_{LOAD}}{C_{OUT} \times F_{SW}} \quad (5)$$

Where V_{RIPPLE} is the output ripple voltage, V_{IN} and V_{OUT} are the DC input and output voltages respectively, I_{LOAD} is the load current, Fsw is the 600kHz fixed switching frequency, and C_{OUT} is the capacitance of the output capacitor.

If using tantalum or low ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, so the output ripple is estimated using Equation (6):

$$V_{RIPPLE} = \frac{(1-\frac{V_{IN}}{V_{OUT}}) \times I_{LOAD}}{C_{OUT} \times F_{SW}} + \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}} \quad (6)$$

Where, R_{ESR} is the equivalent series resistance of the output capacitors.

Choose an output capacitor to satisfy the output ripple and load transient requirements of the design. Capacitance de-rating should be taken into consideration when designing high output voltage applications. Three 22μF ceramic capacitors are suitable for most applications.

Selecting the Inductor

The inductor is required to force the higher output voltage while being driven by the input voltage. A higher value inductor has less ripple current, resulting in lower peak inductor current. This reduces stress on the internal N-channel switch and enhances efficiency. However, the higher value inductor has a larger physical size, a higher series resistance, and a lower saturation current.

A good rule of thumb is to allow the peak-to-peak ripple current to be approximately 30%-40% of the maximum input current. Make sure that the peak inductor current is below 75% of the current limit at the operating duty cycle to prevent loss of regulation due to the current limit. Also, make sure that the inductor does not saturate under the worst-case load transient and start-up conditions. Calculate the required inductance value with Equation (7) and Equation (8):

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times F_{SW} \times \Delta I} \quad (7)$$

$$I_{IN(max)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta} \quad (8)$$

Where :

$I_{LOAD(MAX)}$ is the maximum load current.

ΔI is the peak-to-peak inductor ripple current.

ΔI = (30% - 40%) x $I_{IN\ (MAX)}$.

η is the efficiency.

Selecting the Output Rectifier

The MP3428A features a SDR gate driver. Instead of a Schottky diode, an N-channel MOSFET can be used to free-wheel the inductor current when the internal MOSFET is off. The SDR gate driver voltage has a high 5V voltage, so choose an N-channel MOSFET compatible with a 5V gate voltage rating. The minimum high level is about 3V. Therefore, the MOSFET's turn-on threshold is recommended lower than 2.5V.

In some low output applications, such as a 5V output, the voltage across the BST capacitor may be insufficient. In this case, a Schottky diode should be connected from the output port to BST, conducting the current into the BST capacitor when SW goes low (see Figure 3).

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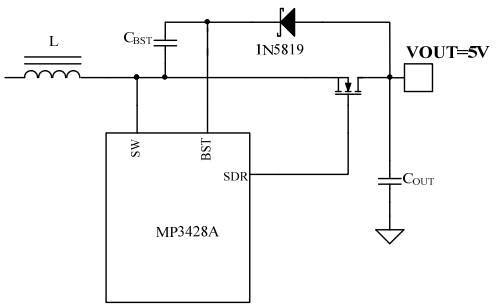

Figure 3: BST Charger for Low Output Application

The MOSFET voltage rating should be equal to or higher than the output voltage. The average current rating must be higher than the maximum load current, and the peak current rating must be higher than the peak inductor current. If a Schottky diode is used as the output rectifier, the same specifications should be considered.

Selecting the Input MOSFET

The MP3428A integrates one CLDR pin to drive an external N-channel MOSFET to disconnect the input power or limit the input current. The following key factors should be considered when selecting the input disconnecting MOSFET:

1. Drain-to-source voltage rating. This value should be higher than V_{IN} plus V_{TH} of the input MOSFET.
2. Drain-to-source current rating. The maximum current through the input disconnecting MOSFET is the maximum input current. This occurs when the input voltage is at a minimum and the load power is at a maximum.
3. SOA. The MOSFET should survive when conducting a current pulse that has a high level of V_{CL}(mV)/R_{SENSE}(mΩ) and lasts for Css(nF) x 0.7(V)/7(uA) + 0.5 (units: ms).
4. Gate-to-source voltage rating. The positive gate-to-source voltage rating should be higher than 5.5V while the negative voltage rating should be higher than the value of the output voltage. If the output voltage is too high and the MOSFET gate-to-source rating cannot meet the requirement, a diode from the source to the gate of the disconnecting MOSFET is recommended (see Figure 4).
5. Gate-to-source threshold voltage. The threshold should be lower than 1.5V. A 1V~1.2V overall temperature range is preferred.
6. On resistance ($R_{DS\ ON}$). It should be small for high conversion efficiency.
7. Low leakage current. It should be low for better isolation.

In addition, size and thermal temperature should be taken into consideration.

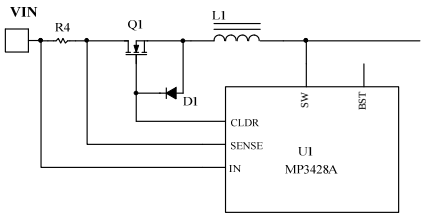

Figure 4: Gate Protection Diode for High Output Voltage Condition

Compensation

The output of the transconductance error amplifier (COMP) is used to compensate the regulation control system. The system uses two poles and one zero to stabilize the control loop.

The poles are F_{P1} (set by the output capacitor, C_{OUT}, and the load resistance), and F_{P2} (start from origin). The zero F_{Z1} is set by the compensation capacitor (C_{COMP}) and the compensation resistor (R_{COMP}). These are determined by Equation (9) and Equation (10):

$$F_{P1} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}} (Hz) \quad (9)$$

$$F_{Z1} = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} (Hz) \quad (10)$$

Where, R_{LOAD} is the load resistance.

The DC loop gain is calculated using Equation (11):

$$A_{VDC} = \frac{A_{VEA} \times V_{IN} \times R_{LOAD} \times V_{FB} \times G_{CS} \times R_{COMP}}{2 \times V_{OUT}^2} (V/V) \quad (11)$$

Where G_{CS} is the compensation voltage to the inductor current gain, A_{VEA} is the error amplifier voltage gain, and V_{FB} is the feedback regulation threshold.

Also, there is a right-half-plane zero (F_{RHPZ}) that exists in continuous conduction mode (the inductor current does not drop to zero in each cycle). The frequency of the right-half-plane zero is determined with Equation (12):

$$F_{RHPZ} = \frac{R_{LOAD}}{2 \times \pi \times L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 (Hz) \quad (12)$$

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The right-half-plane zero increases the gain and reduces the phase simultaneously, which results in a smaller phase and gain margin. The worst-case condition occurs when the input voltage is at its minimum and the output power is at its maximum.

Compensation recommendations are listed in the "Typical Application Circuits" section.

PCB Layout Guidelines

High frequency switching regulators require very careful layout for stable operation and low noise. All components must be placed as close to the IC as possible. For best results, refer to Figure 5 and follow the guidelines below. The corresponding schematic can be found on page 1.

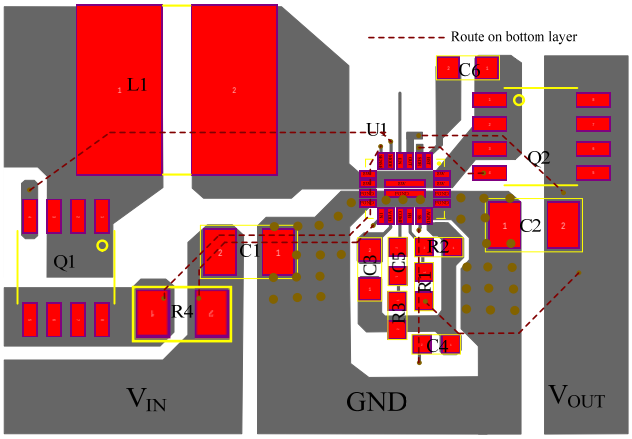

Figure 5: Recommended PCB Layout

Keep the output loop (SW, PGND, Q2, and C2) as small as possible.

1. Place the FB divider R1 and R2 as close as possible to FB.
2. Route the sensing traces (SENSE and IN) in parallel closely with a small closed area. A 0805 package is recommended for the sensing resistor (R4) to reduce parasitic inductance.
3. Connect FB and OUT feedback from the output capacitor (C2).
4. Connect the compensation components and SS capacitor to AGND with a short loop.
5. Connect the VDD capacitor to AGND with a short loop. Do NOT connect to the PGND net before connecting to the IC and AGND.
6. Keep the input loop (C1, R4, Q1, L1, SW, and PGND) as small as possible. Also, make the BST and SDR path as short as possible.
7. Place enough GND vias close to the MP3428A for good thermal dissipation.
8. Do NOT place vias on the SW net.
9. Use a 4-layer PCB for high-power applications.
10. Place wide copper and vias associated with the input MOSFET's drain pin for thermal dissipation.

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2: Design Example

V_{IN}	3.3V-10V
V_{OUT}	12V
I_{OUT}	0A to 2A(9)

The maximum output current is determined by the permitted temperature rising, current limit, and input voltage. The detailed application schematic is shown in Figure 6. The typical performance and circuit waveforms have been shown in the "Typical Performance Characteristics" section. For more device applications, please refer to the related evaluation board datasheets.

NOTE:

9) The maximum load capability may be limited by the permitted temperature rising.

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TYPICAL APPLICATION CIRCUITS

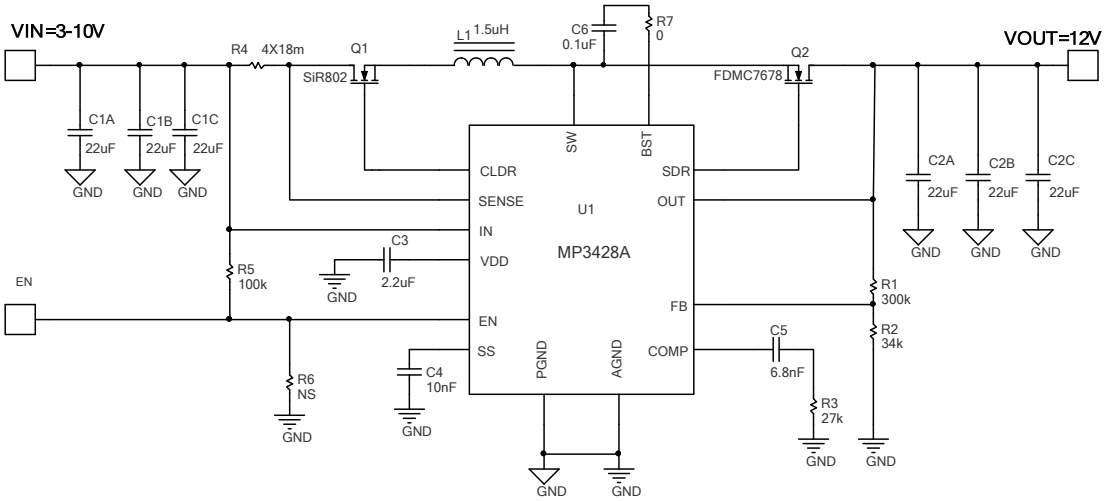

Figure 6: 12V Output Synchronous Solution with Input Disconnect Function

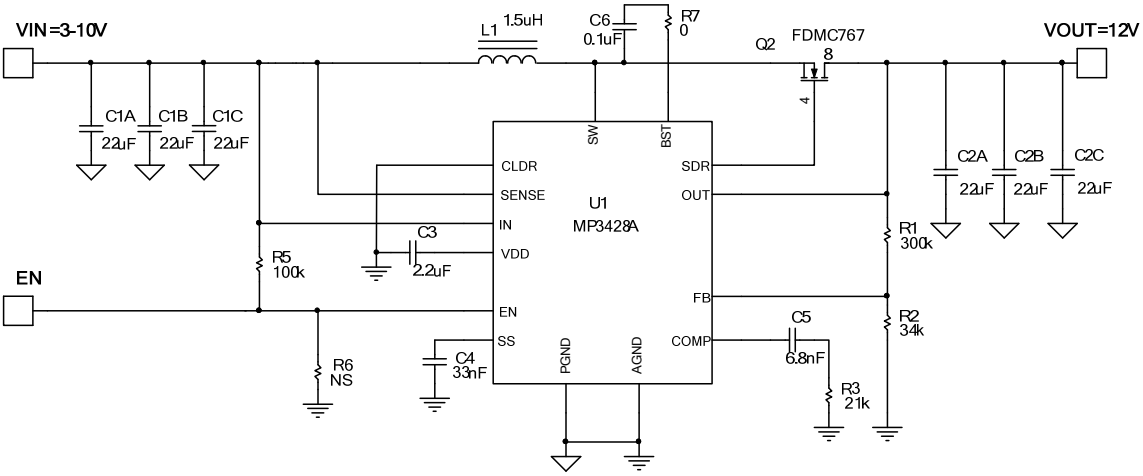

Figure 7: 12V Output Synchronous Solution Using an Internal Current-Sensing Circuit

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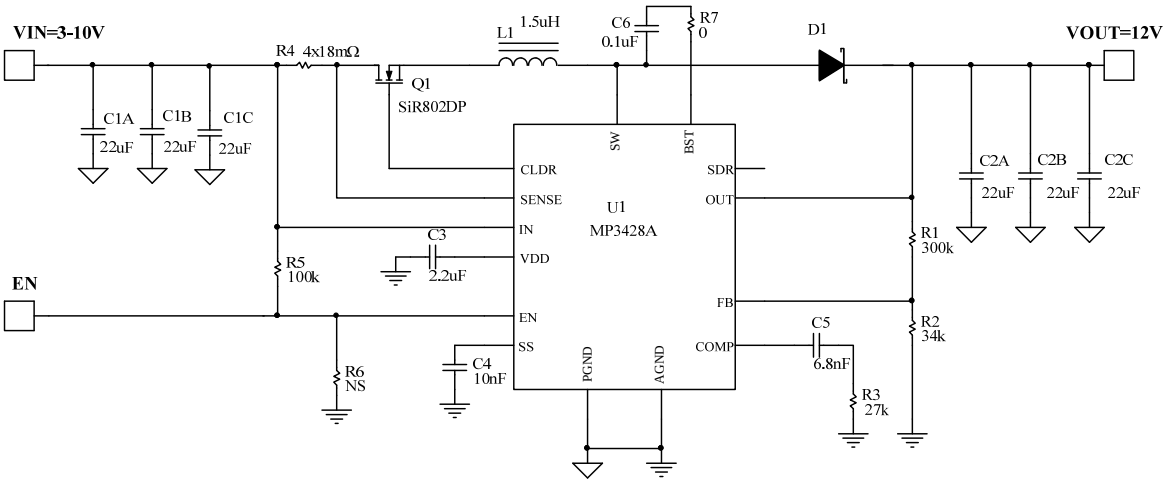

Figure 8: 12V Output Non-Synchronous Solution with Input Disconnect Function

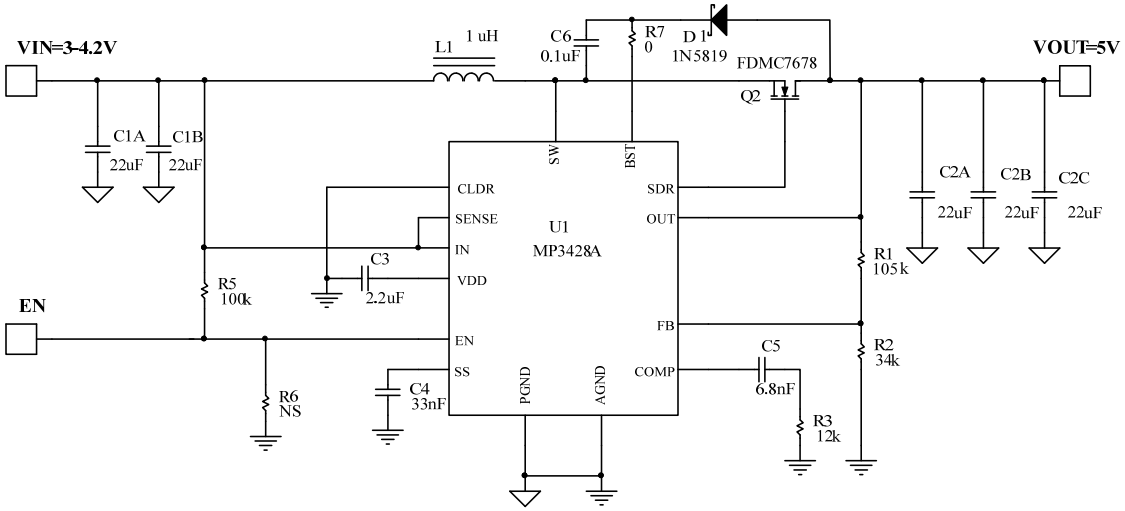

Figure 9: 5V Output Synchronous Solution Using Internal Current-Sensing Circuit

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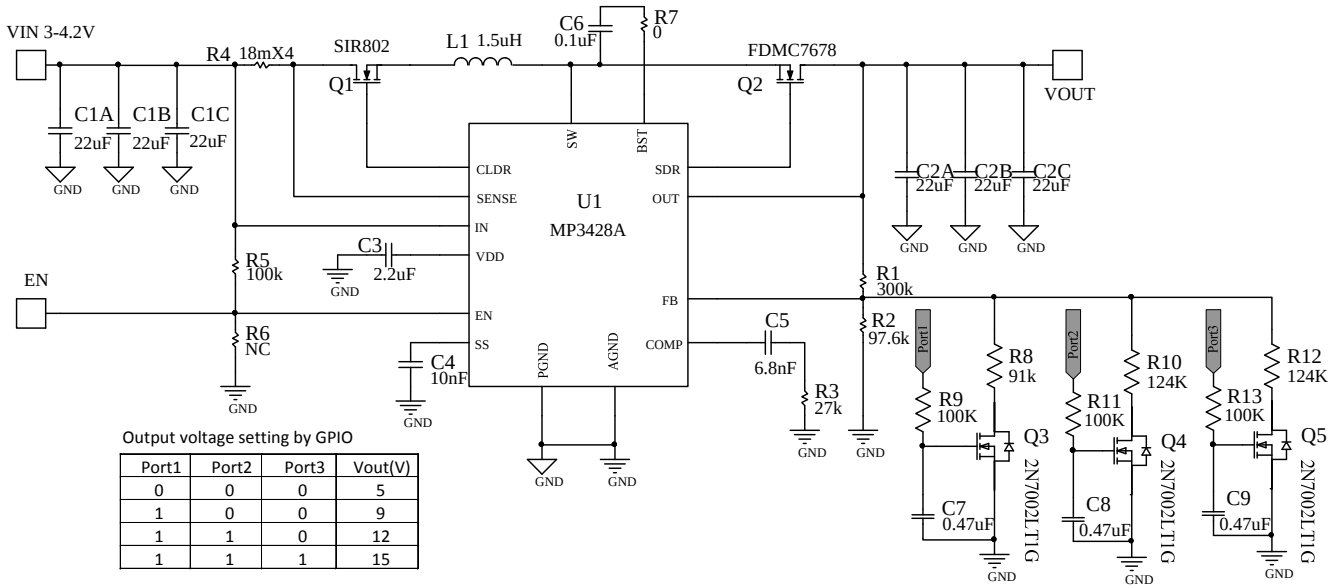
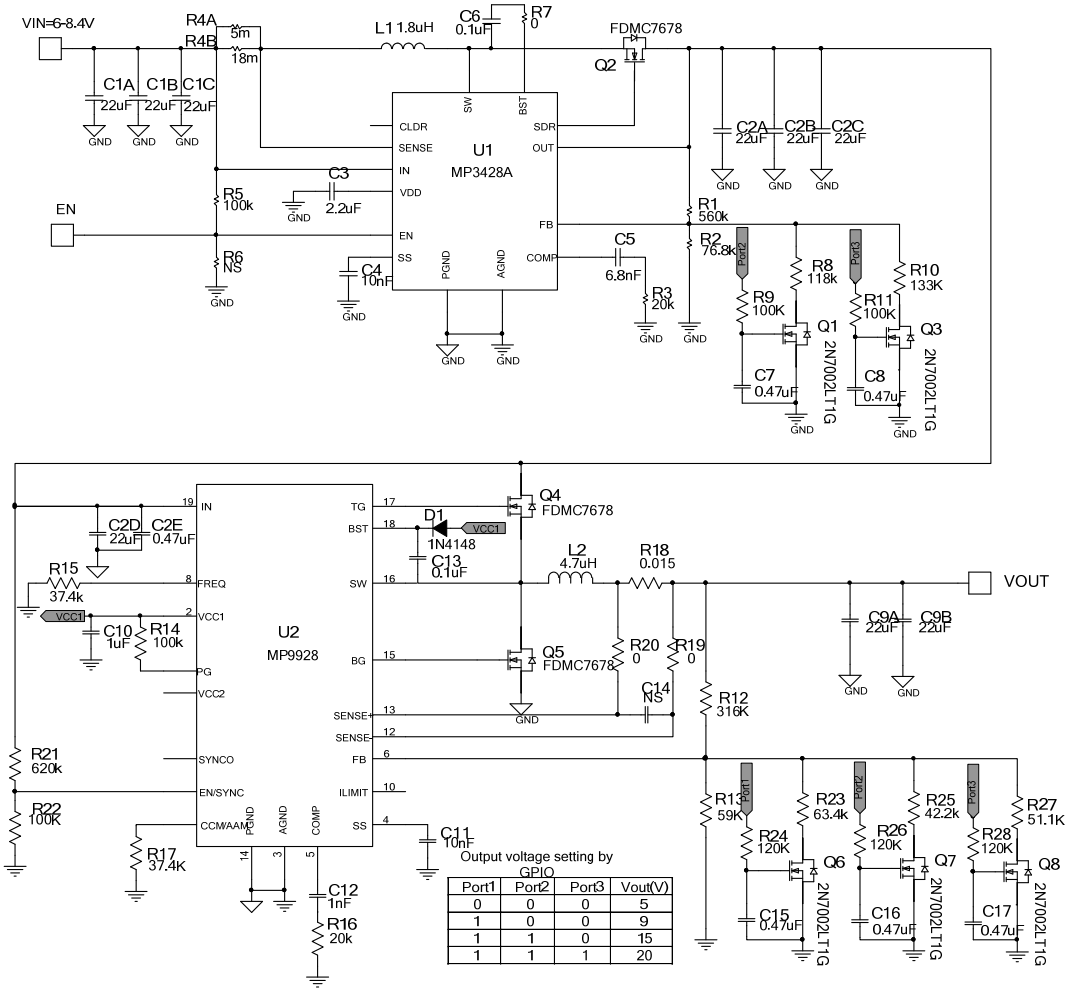


Output voltage setting by GPIO

Port1	Port2	Port3	Vout(V)
0	0	0	5
1	0	0	9
1	1	0	12
1	1	1	15

Figure 10: USB Type-C Power Supply Application from Signal Cell Battery



Output voltage setting by GPIO

Port1	Port2	Port3	Vout(V)
0	0	0	5
1	0	0	9
1	1	0	15
1	1	1	20

Figure 11: USB Type-C Power Supply Application from Dual Cell Batteries

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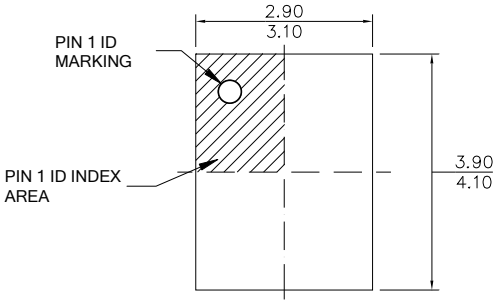
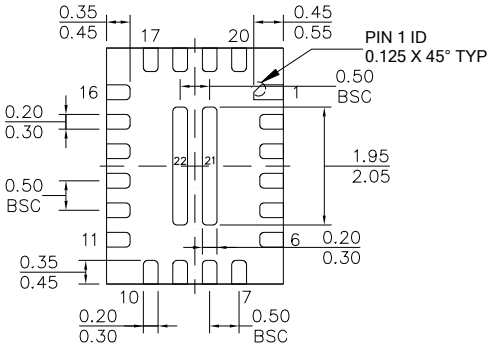
PACKAGE INFORMATION

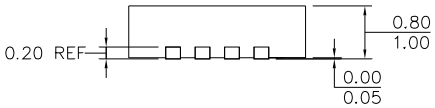
QFN-22 (3mm x 4mm)



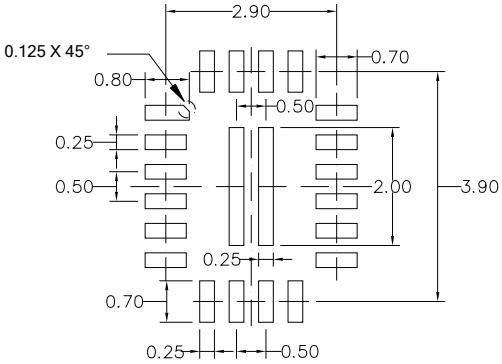
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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