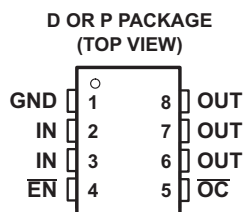


POWER-DISTRIBUTION SWITCHES

FEATURES

- 95-mΩ Maximum (5-V Input) High-Side MOSFET Switch
- Short-Circuit Protection and Thermal Protection
- Logic Overcurrent Output
- 4-V to 7-V Operating Range
- Enable Input Compatible With 3-V and 5-V Logic
- Controlled Rise and Fall Times Limit Current Surges and Minimize EMI
- Undervoltage Lockout Ensures That Switch is Off at Start-Up
- 10-μA Maximum Standby Current
- Available in Space-Saving 8-Pin SOIC and 8-Pin PDIP
- 0°C to 125°C Operating Junction Temperature Range
- 12-kV Output, 6-kV Input Electrostatic-Discharge Protection
- UL Listed (TPS2014) – File No. E169910



DESCRIPTION

The TPS2014 and TPS2015 power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The high-side switch is a 95-mΩ n-channel MOSFET. The switch is controlled by a logic enable that is compatible with 3-V and 5-V logic. Gate drive is provided by an internal charge pump designed to control the power switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 4 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS20xx limits the output current to a safe level by switching into a constant-current mode, and the overcurrent logic output is set to low. Continuous heavy overloads and short circuits will increase the power dissipation in the switch and cause the junction temperature to rise. A thermal protection circuit is implemented, which shuts the switch off to prevent damage when the junction temperature exceeds its thermal limit. An undervoltage lockout is provided to ensure the switch is in the off state at start-up.

The TPS2014 and TPS2015 differ only in short-circuit current limits. The TPS2014 is designed to limit at 1.2 A load and the TPS2015 limits at 2 A (see the available options table). The TPS20xx is available in 8-pin small-outline integrated circuit (SOIC) and 8-pin PDIP packages, and operates over a junction temperature range of 0°C to 125°C.

GENERAL SWITCH CATALOG						
33 mΩ, single	80 mΩ, single	80 mΩ, dual	80 mΩ, dual	80 mΩ, triple	80 mΩ, quad	80 mΩ, quad
TPS201xA 0.2 A - 2 A TPS202x 0.2 A - 2 A TPS203x 0.2 A - 2 A	TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A	TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



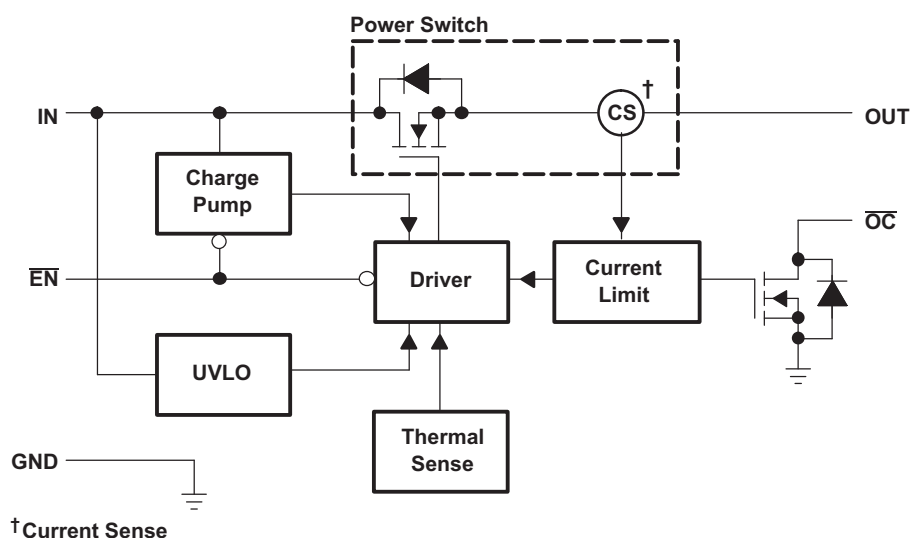
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C	PACKAGED DEVICES ⁽¹⁾		CHIP FORM (Y)
			SOIC (D) ⁽²⁾	PDIP (P)	
0°C TO 85°C	0.6 A	1.2 A	TPS2014D	TPS2014P	TPS2014Y
	1 A	2 A	TPS2015D	TPS2015P	TPS2015Y

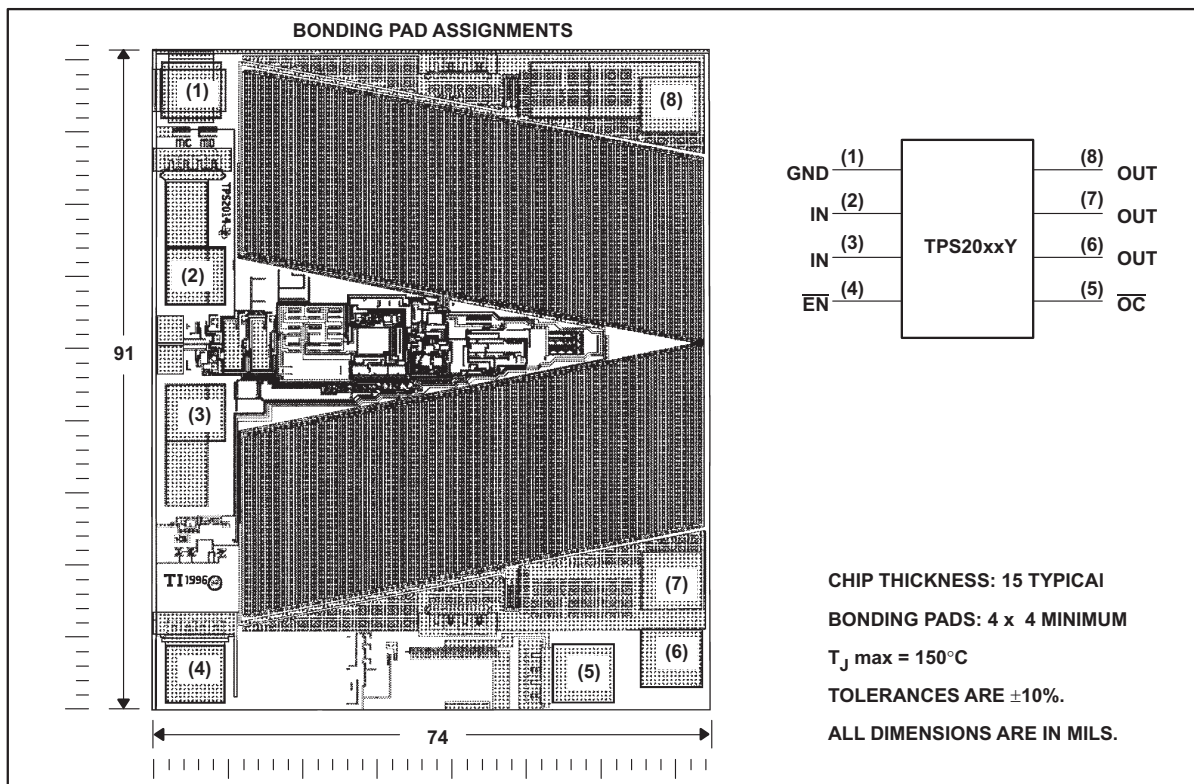
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2014DR).

FUNCTIONAL BLOCK DIAGRAM



TPSA20xxY CHIP INFORMATION

This chip, when properly assembled, displays characteristics similar to those of the TPS20xx. Ultrasonic bonding may be used on the doped aluminium bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.



TERMINAL FUNCTIONS

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{EN}$	4	I	Enable input. Logic low at $\overline{EN}$ turns the power switch on.
GND	1	I	Ground
$\overline{IN}$	2, 3	I	Input voltage
$\overline{OC}$	5	O	$\overline{OC}$ is asserted active low during a fault condition.
OUT	6-8	O	Power switch output

DETAILED DESCRIPTION

POWER SWITCH

The power switch is an N-channel MOSFET with a maximum on-state resistance of 95 m Ω ($V_{I(IN)} = 5V$), configured as a high-side switch.

Charge Pump

An internal 100-kHz charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 4 V and requires very little supply current.

Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range instead of the microsecond or nanosecond range for a standard FET.

Enable ($\overline{EN}$)

A logic high on $\overline{EN}$ turns off the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 A. A logic zero input restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

Overcurrent ($\overline{OC}$)

$\overline{OC}$ is an open-drain logic output that is asserted (active low) when an overload or short circuit is encountered. The output remains asserted until the overload or short-circuit condition is removed.

Current Sense

A sense FET monitors the current supplied to the load. The sense FET provides a much more efficient way to measure current than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its linear region, which switches the output into a constant current mode and simply holds the current constant while varying the voltage on the load.

Thermal Sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 180C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

Undervoltage Lockout

An internal voltage sense monitors the input voltage. When the input voltage is below 3.2 V nominal, a control signal turns off the power switch.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		UNIT
$V_I^{(2)}$	Input voltage range	-0.3 V to 7 V
$V_O^{(2)}$	Output voltage range	-0.3 V to $V_{I(IN)} + 0.3$ V
V_I at $\overline{EN}$	Input voltage range	-0.3 V to 7 V
I_O	Continuous output current	Internally limited
	Continuous total power dissipation	See Dissipation Rating Table
T_J	Operating virtual junction temperature range	0°C to 125°C
T_{stg}	Storage temperature range,	-65°C to 150°C
	Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
P	1175 mW	9.4 mW/°C	752 mW	235 mW
D	725 mW	5.8 mW/°C	464 mW	145 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V _I	Input voltage		4	5.5	V
V _I at $\overline{EN}$	Input voltage		0	5.5	V
I _O	Continuous output current	TPS2014	0	0.6	A
		TPS2015	0	1	
T _J	Operating virtual junction temperature		0	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN)} = 5.5$ V, I_O = rated current, $\overline{EN} = 0$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
POWER SWITCH					
r_{on} On-state resistance	$V_I = 5.5$ V, $T_J = 25^\circ\text{C}$		75	95	mΩ
	$V_I = 5$ V, $T_J = 25^\circ\text{C}$		80	95	
	$V_I = 4.5$ V, $T_J = 25^\circ\text{C}$		90	110	
	$V_I = 4$ V, $T_J = 25^\circ\text{C}$		96	110	
I_{lkg} Leakage current, output	$\overline{EN} = V_I$, $T_J = 25^\circ\text{C}$		0.001	1	A
	$\overline{EN} = V_I$, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			10	
	$V_I = 5.5$ V, $T_J = 25^\circ\text{C}$, $C_L = 1$ F		4		ms
	$V_I = 4$ V, $T_J = 25^\circ\text{C}$, $C_L = 1$ F		3.8		
t_f Fall time, output	$V_I = 5.5$ V, $T_J = 25^\circ\text{C}$, $C_L = 1$ F		3.9		ms
	$V_I = 4$ V, $T_J = 25^\circ\text{C}$, $C_L = 1$ F		3.5		

- (1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating junction temperature range, $V_{I(IN)} = 5.5\text{ V}$, $I_O = \text{rated current}$, $\overline{EN} = 0\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP	MAX	UNIT
ENABLE INPUT ($\overline{\text{EN}}$)							
V _{IH}	High-level input voltage	4 V ≤ V _I ≤ 5.5 V		2			V
V _{IL}	Low-level input voltage	4 V ≤ V _I ≤ 5.5 V		0.8			V
I _I	Input current	$\overline{\text{EN}}$ = 0 V or $\overline{\text{EN}}$ = V _I		0.5	0.5		A
t _{PLH}	Propagation (delay) time, low to high output	C _L = 1 F		20			mA
t _{PHL}	Propagation (delay) time, high to low output	C _L = 1 F		40			
CURRENT LIMIT							
I _{OS}	Short-circuit output current	T _J = 25C, V _I = 5.5 V	TPS2014	0.66	1.2	1.8	A
			TPS2015	1.1	2	3	
SUPPLY CURRENT							
I _{DDL}	Supply current, low-level output	$\overline{\text{EN}}$ = V _I	T _J = 25C	0.015		10	A
			0°C ≤ T _J ≤ 125°C			10	
I _{DDH}	Supply current, high-level output	$\overline{\text{EN}}$ = 0 V	T _J = 25C	73		100	A
			0°C ≤ T _J ≤ 125°C			100	
UNDERVOLTAGE LOCKOUT							
V _{IL}	Low-level input voltage			2	3.2	4	V
$\overline{\text{OC}}$							
I _{OS}	Short-circuit output current	0°C ≤ T _J ≤ 125°C		5			mA
V _{OL}	Low-level output voltage	0°C ≤ T _J ≤ 125°C		0.3			

ELECTRICAL CHARACTERISTICS (CONTINUED)

over recommended operating junction temperature range, $V_{I(IN)} = 5.5\text{ V}$, $I_O = \text{rated current}$, $\overline{EN} = 0\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		TPS2014Y, TPS2015Y			UNIT
				MIN	TYP	MAX	
POWER SWITCH							
r _{on}	On-state resistance	V _I = 5.5 V, T _J = 25C		75			mΩ
		V _I = 5 V, T _J = 25C		80			
		V _I = 4.5V, T _J = 25C		90			
		V _I = 4 V, T _J = 25C		96			
I _{lkg}	Leakage current, output	EN = V _I , T _J = 25C		0.001			A
		EN = V _I , 0°C ≤ T _J ≤ 125°C		10			
t _r	Rise time, output	V _I = 5.5 V, T _J = 25C, C _L = 1 F		4			ms
		V _I = 4 V, T _J = 25C, C _L = 1 F		3.8			
t _f	Fall time, output	V _I = 5.5 V, T _J = 25C, C _L = 1 F		3.9			ms
		V _I = 4 V, T _J = 25C, C _L = 1 F		3.5			
ENABLE INPUT (EN)							
V _{IH}	High-level input voltage	4 V ≤ V _I ≤ 5.5 V		2			V
V _{IL}	Low-level input voltage	4 V ≤ V _I ≤ 5.5 V		0.8			V
I _I	Input current	EN= 0 V or EN = V _I		0.5			A
t _{PLH}	Propagation (delay) time, low to high output	C _L = 1 F		20			ms
t _{PHL}	Propagation (delay) time, high to low output	C _L = 1 F		40			
CURRENT LIMIT							
I _{OS}	Short-circuit output current	T _J = 25C,	V _I = 5.5 V	TPS2014	1.2		A
				TPS2015	2		
SUPPLY CURRENT							
I _{DDL}	Supply current, low-level output	EN = V _I	T _J = 25C	0.015		A	
			0°C ≤ T _J ≤ 125°C	10			
I _{DDH}	Supply current, high-level output	EN = 0 V	T _J = 25C	73		A	
			0°C ≤ T _J ≤ 125°C	100			
UNDERVOLTAGE LOCKOUT							
V _{IL}	Low-level input voltage			3.2		V	
OC							
I _{OS}	Short-circuit output current	0°C ≤ T _J ≤ 125°C		5		mA	
V _{OL}	Low-level output voltage	0°C ≤ T _J ≤ 125°C		0.3			

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

PARAMETER MEASUREMENT INFORMATION

Table 1. Table of Timing Diagrams

	FIGURE
Propagation Delay and Rise Time With 1- μ F Load, $V_{I(IN)} = 5$ V	1
Propagation Delay and Fall Time With 1- μ F Load, $V_{I(IN)} = 5$ V	2
TPS2014 Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)} = 5$ V	3
TPS2015 Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)} = 5$ V	4
TPS2014 Threshold Current, $V_{I(IN)} = 5$ V	5
TPS2015 Threshold Current, $V_{I(IN)} = 5$ V	6
TPS2014 (Enabled) into Short Circuit, $V_{I(IN)} = 5$ V	7
TPS2015 (Enabled) into Short Circuit, $V_{I(IN)} = 5$ V	8

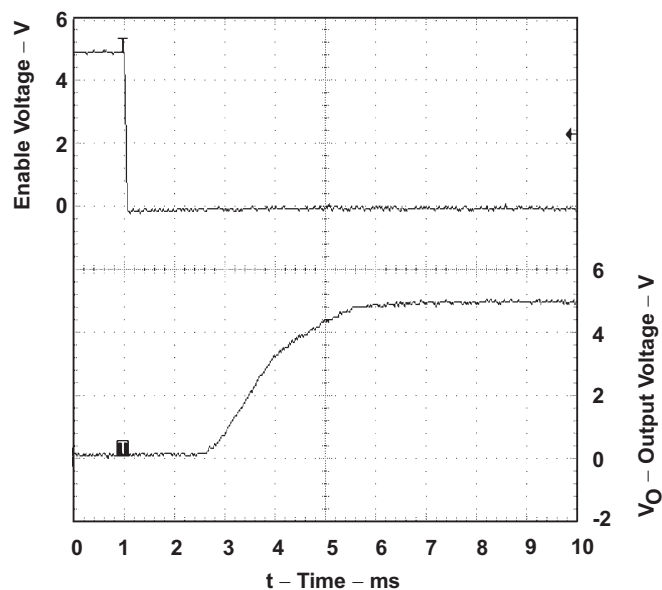


Figure 1. Propagation Delay and Rise Time With 1- μ F Load, $V_{I(IN)} = 5$ V

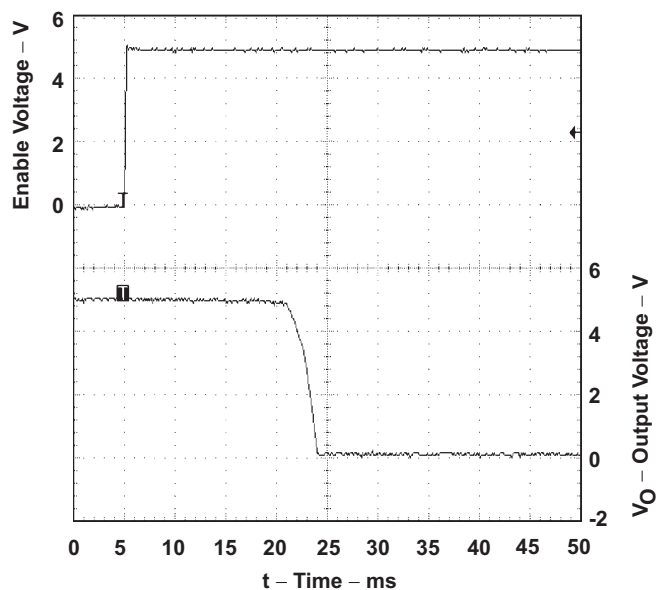


Figure 2. Propagation Delay and Fall Time With 1- μ F Load, $V_{I(IN)} = 5$ V

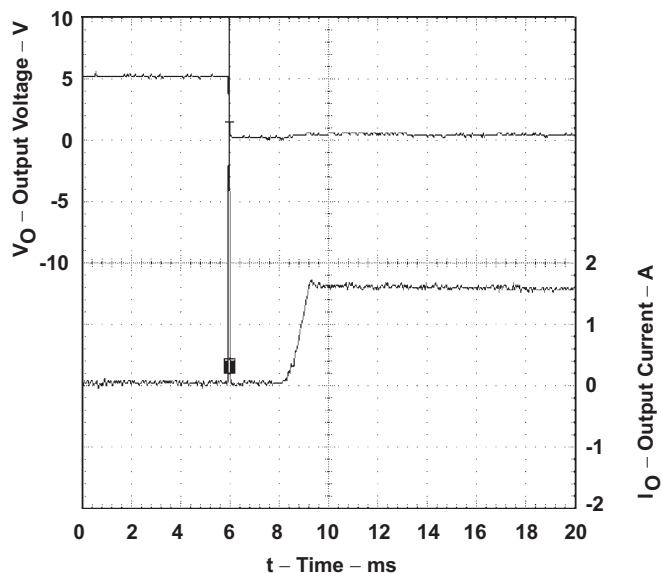


Figure 3. TPS2014 Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)} = 5$ V

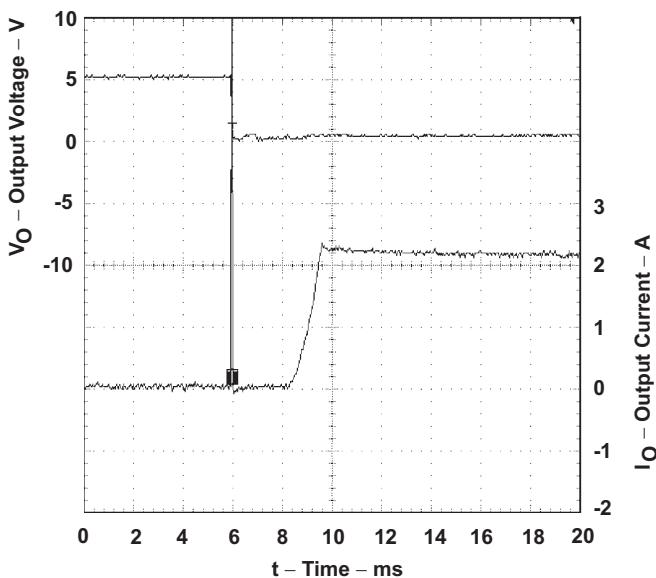


Figure 4. TPS2015 Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)} = 5$ V

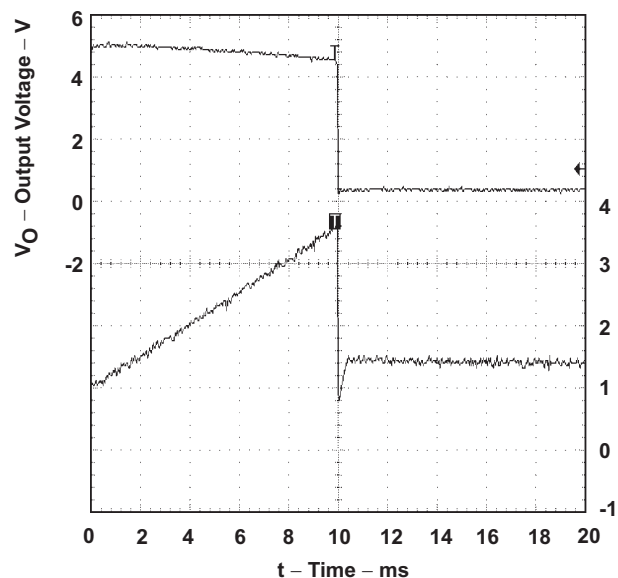


Figure 5. TPS2014 Threshold Current, $V_{I(IN)} = 5\text{ V}$

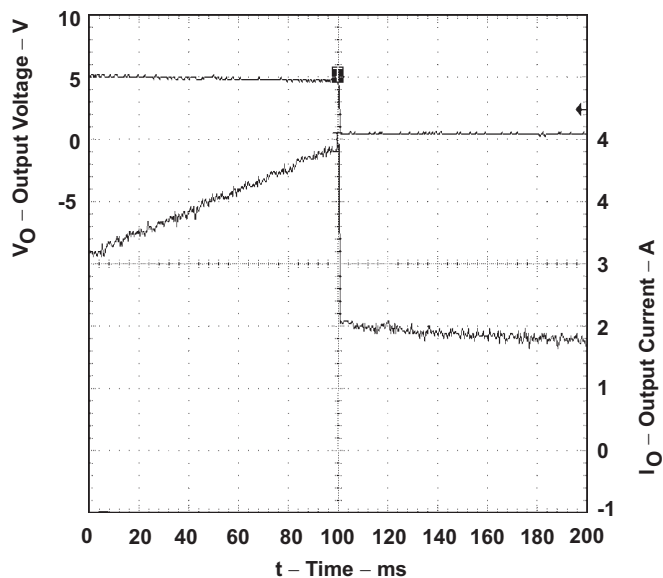


Figure 6. TPS2015 Threshold Current, $V_{I(IN)} = 5\text{ V}$

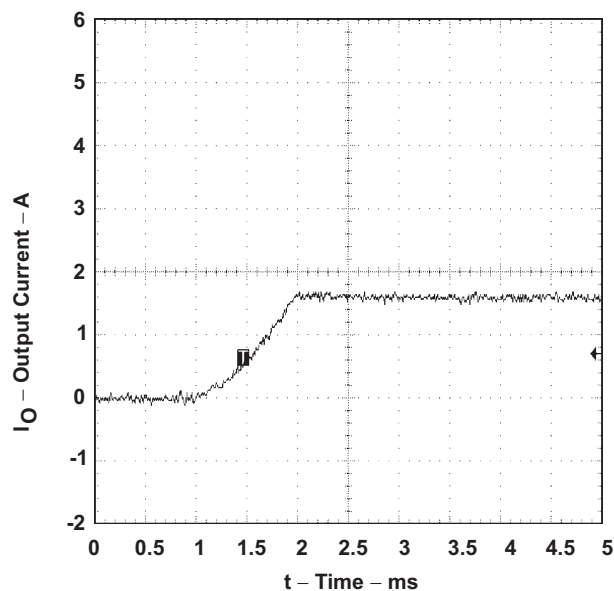


Figure 7. TPS2014 (Enabled) Into Short Circuit, $V_{I(IN)} = 5\text{ V}$

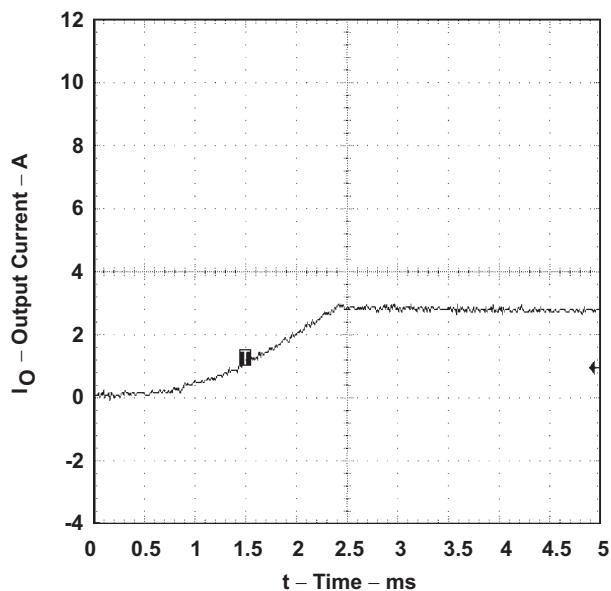


Figure 8. TPS2015 (Enabled) Into Short Circuit, $V_{I(IN)} = 5\text{ V}$

TYPICAL CHARACTERISTICS

Table of Graphs START HERE

		FIGURE
Turn-On Delay Time	vs Input Voltage	9
Turn-Off Delay Time	vs Input Voltage	10
Rise Time	vs Output Current	11
Fall Time	vs Output Current	12
Supply Current, Output Enabled	vs Junction Temperature	13
Supply Current, Output Enabled	vs Junction Temperature	14
Supply Current, Output Enabled	vs Input Voltage	15
Supply Current, Output Enabled	vs Input Voltage	16
On-State Resistance	vs Junction Temperature	17
On-State Resistance	vs Input Voltage	18
Input Voltage to Output Voltage	vs Input Voltage	19
Short-Circuit Output Current	vs Input Voltage	20
Threshold Trip Current	vs Input Voltage	21
Short-Circuit Output Current	vs Junction Temperature	22
UVLO Trip Voltage	vs Junction Temperature	23

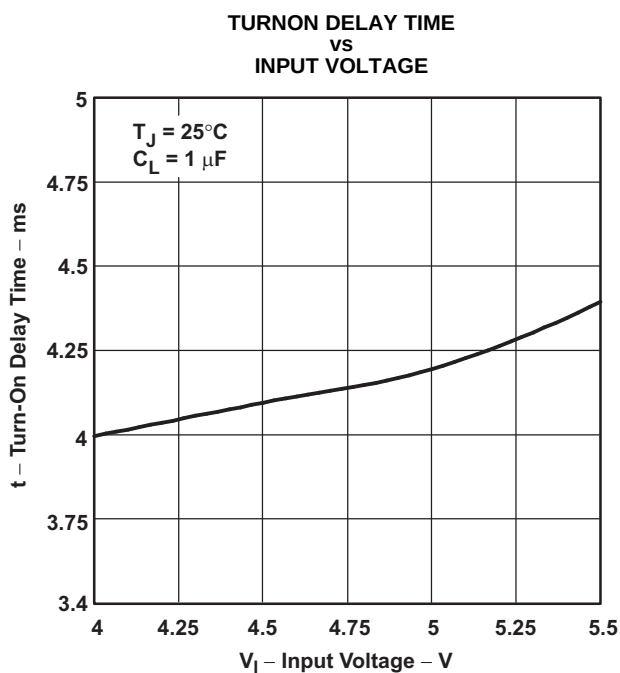


Figure 9.

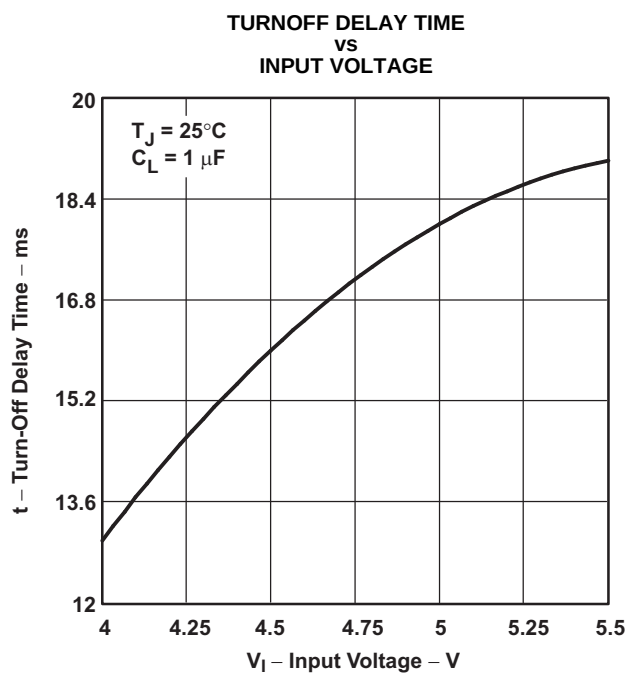


Figure 10.

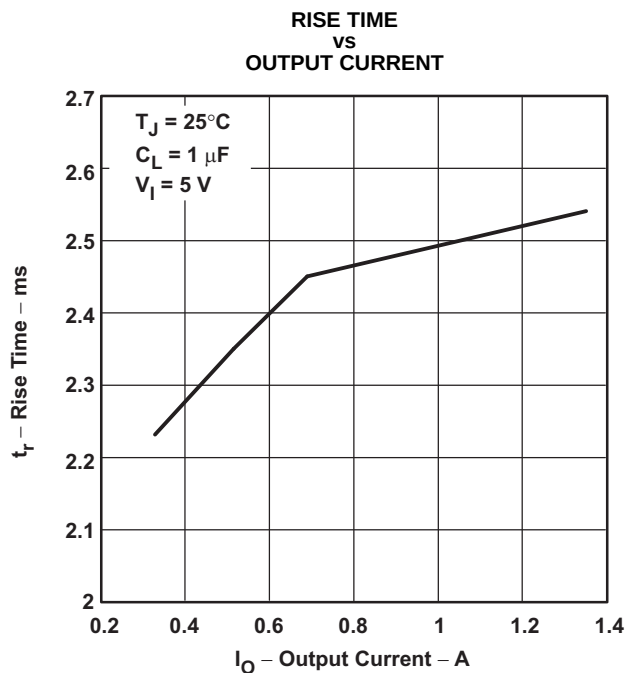


Figure 11.

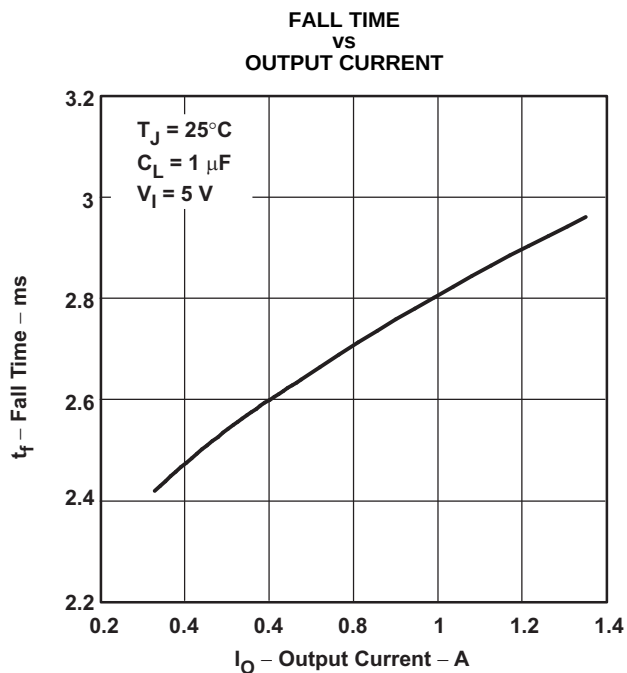


Figure 12.

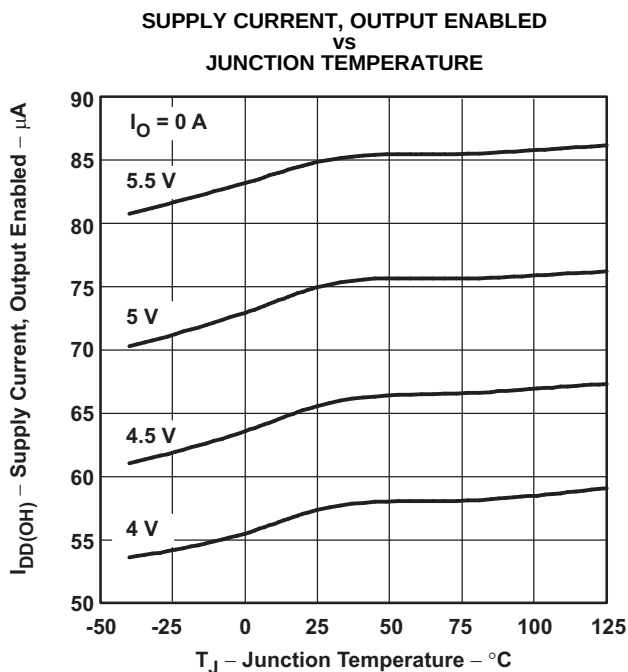


Figure 13.

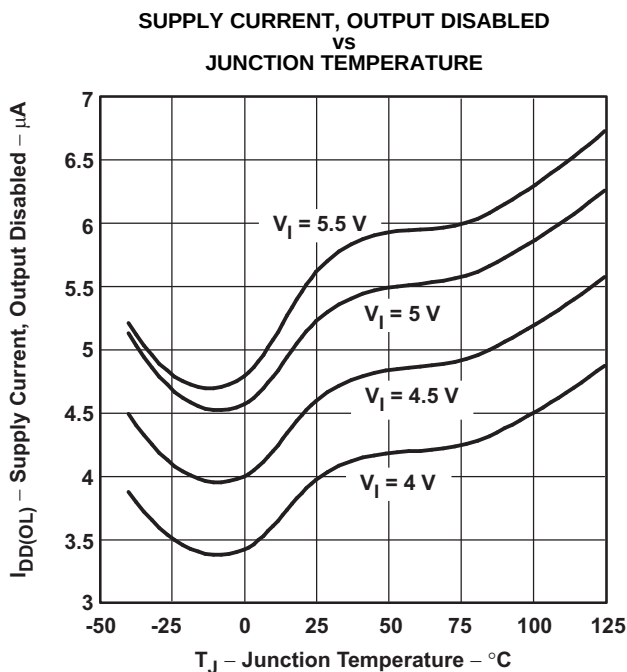


Figure 14.

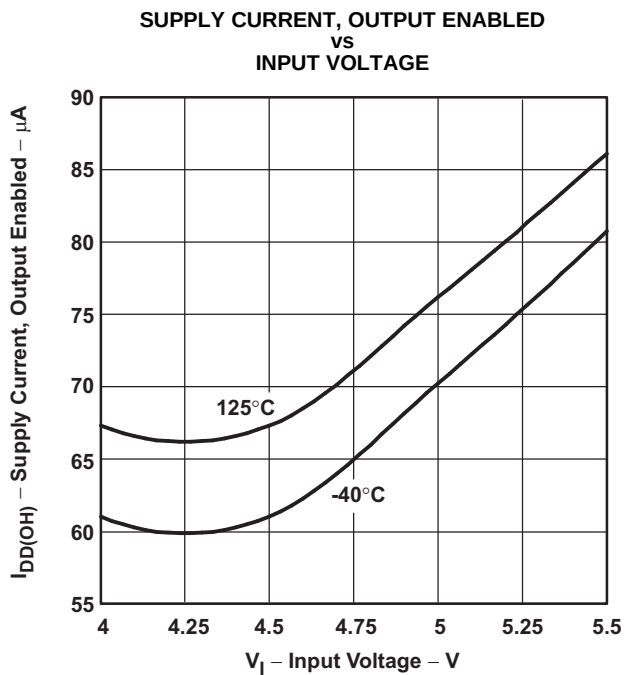


Figure 15.

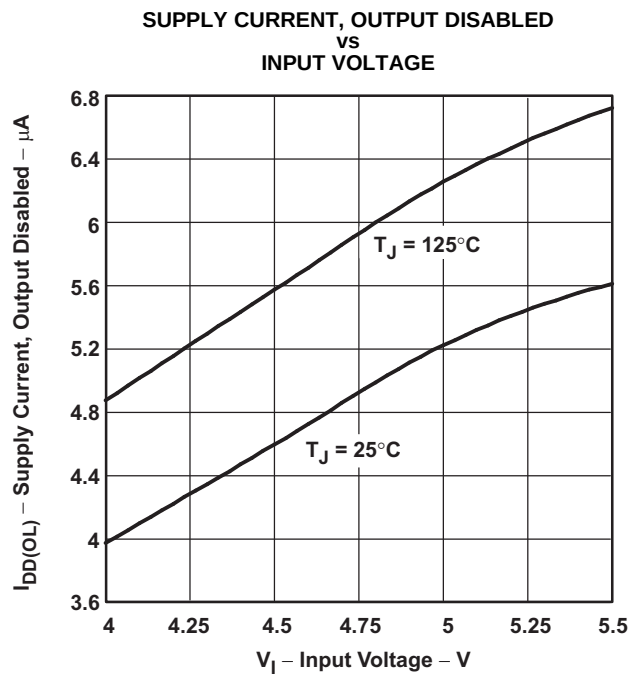


Figure 16.

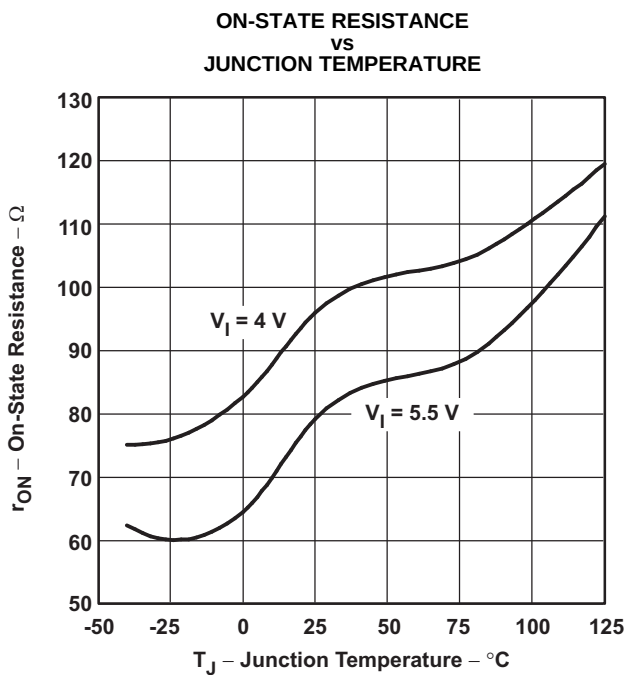


Figure 17.

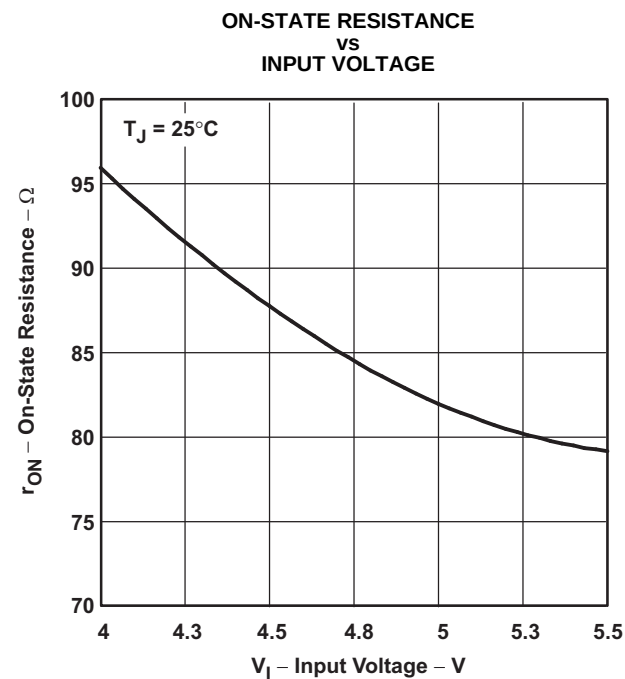


Figure 18.

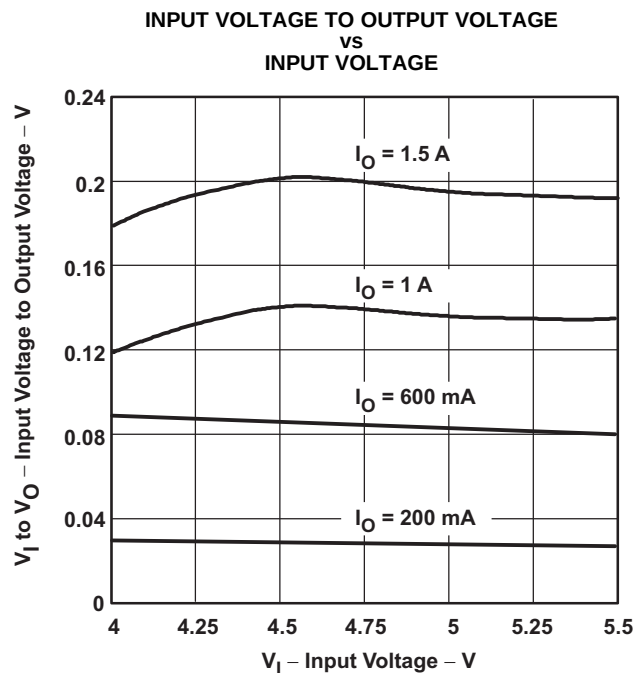


Figure 19.

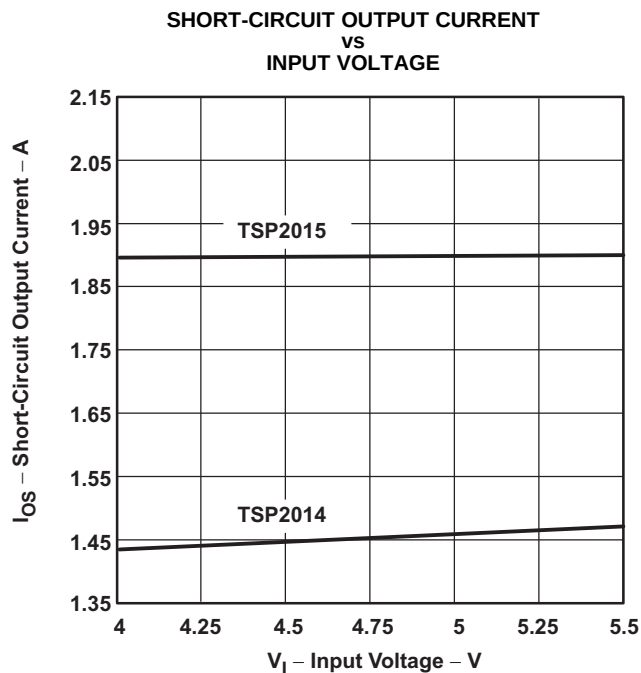


Figure 20.

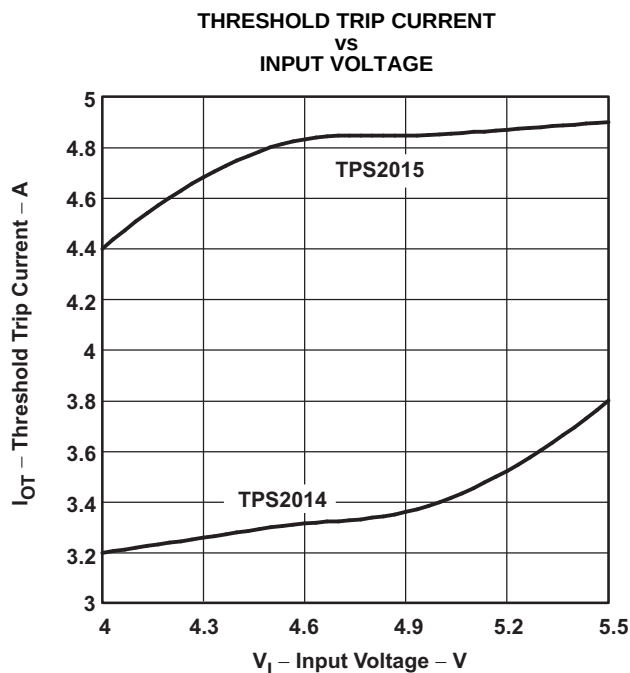


Figure 21.

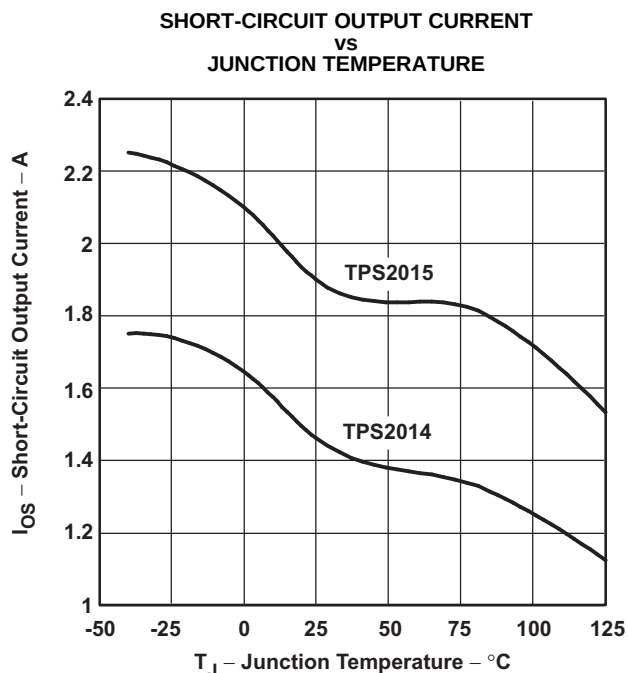


Figure 22.

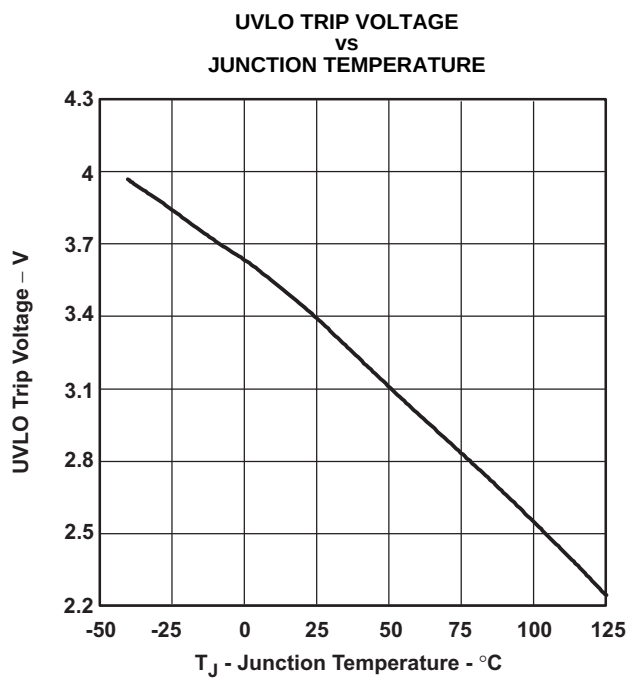


Figure 23.

APPLICATION INFORMATION

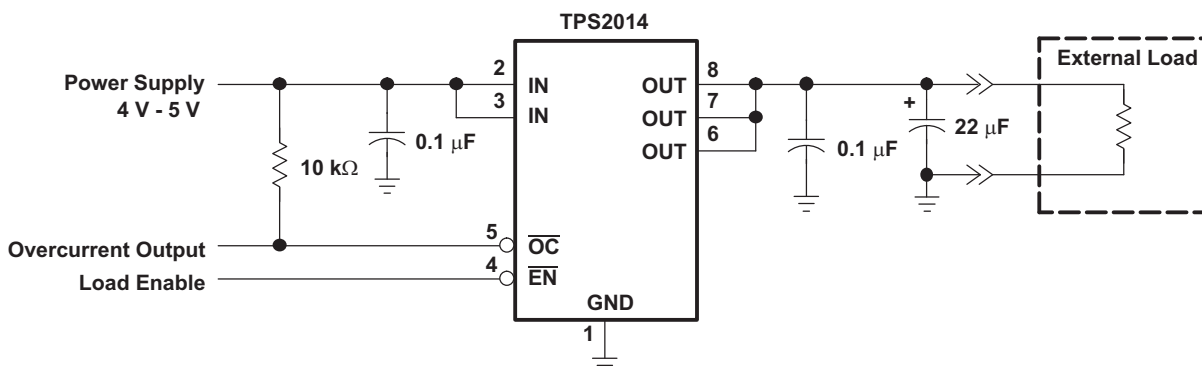


Figure 24. Typical Application

POWER SUPPLY CONSIDERATIONS

The TPS20xx has multiple inputs and outputs that must be connected in parallel to minimize voltage drop and prevent unnecessary power dissipation.

A 0.1-F ceramic bypass capacitor between IN and GND, close to the device, is recommended. A high-value electrolytic capacitor is also desirable when the output load is heavy or has large paralleled capacitors. Bypassing the output with a 0.1-F ceramic capacitor improves the immunity of the device to electrostatic discharge (ESD).

OVERCURRENT

A sense FET is employed to check for overcurrent conditions. Unlike sense resistors and polyfuses, sense FETs do not increase series resistance to the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Shutdown only occurs when the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 7 and Figure 8). The TPS20xx senses the short and immediately switches into a constant-current output.

Under the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents flow for a short time before the current-limit circuit can react (see Figure 3 and Figure 4). After the current-limit circuit has tripped, the device limits normally.

Under the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached (see Figure 5 and Figure 6). The TPS20xx is capable of delivering current up to the current-limit threshold without damage. When the threshold has been reached, the device switches into its constant-current mode.

POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance of the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistance of these packages is high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find r_{on} at the input voltage and at the operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read r_{on} from Figure 17. Next calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature °C

$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, P = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

THERMAL PROTECTION

Thermal protection is provided to prevent damage to the IC when heavy-overload or a short-circuit fault is present for an extended period of time. The fault forces the TPS20xx into constant current mode, which causes the voltage across the high-side switch to increase. Under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to dangerously high levels. The protection circuit senses the junction temperature of the switch and shuts it off. The switch remains off until the junction temperature has dropped approximately 20°C. The switch continues to cycle in this manner until the load fault or the input power is removed.

UNDERVOLTAGE LOCKOUT

An undervoltage lockout is provided to ensure that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 3.2 V, the power switch quickly turns off. This facilitates the design of hot-insertion systems that may not have the ability to turn off the power switch before input power is removed. Upon reapplication of the input voltage (if enabled), the power switch turns on with a controlled rise time to reduce inrush current, EMI, and voltage overshoots.

For proper operation of the UVLO, the TPS20xx requires the voltage decay from 3 V to 2 V to take at least 200 s. Capacitance is added to the input or output of the TPS20xx to increase this decay rate. Capacitance is generally added to the output to lower inrush current due to input capacitance.

UNIVERSAL SERIAL BUS (USB) APPLICATIONS

The USB specification provides for five different classes of devices based on their power sourcing and sinking requirements. These classes of devices are: bus-powered hub, self-powered hub, lower power bus-powered function, high power bus-powered function, and self-powered functions. The TPS20xx can provide power distribution solutions for many of these devices.

BUS-POWERED AND SELF-POWER HUBS

Hubs provide data and power for downstream functions through output ports. Self-power hubs have internal power supplies that furnish power to downstream functions. Each port is required to supply 500 mA continuous to a downstream function. Each port must have overcurrent protection to meet the regulatory safety limit that no single port can deliver more than 5 A. The self-power hub must also have a method to detect and report an overcurrent condition to the USB host. The TPS20xx provides the required current-limiting function and has an overcurrent logic output to inform the hub controller of the fault condition. The on-state resistance of the TPS20xx is low enough to meet all USB voltage regulation requirements. The switch also provides the capability to remove power from a faulted port.

Bus-powered hubs distribute power and data from an input port to downstream ports. Each output port is required to supply 100 mA continuous. A bus-powered hub is not required to provide overcurrent protection because it is provided by the upstream port. In order to power up in a low power state, the self-powered hub must be able to switch power to its output ports. The TPS20xx can also provide this function.

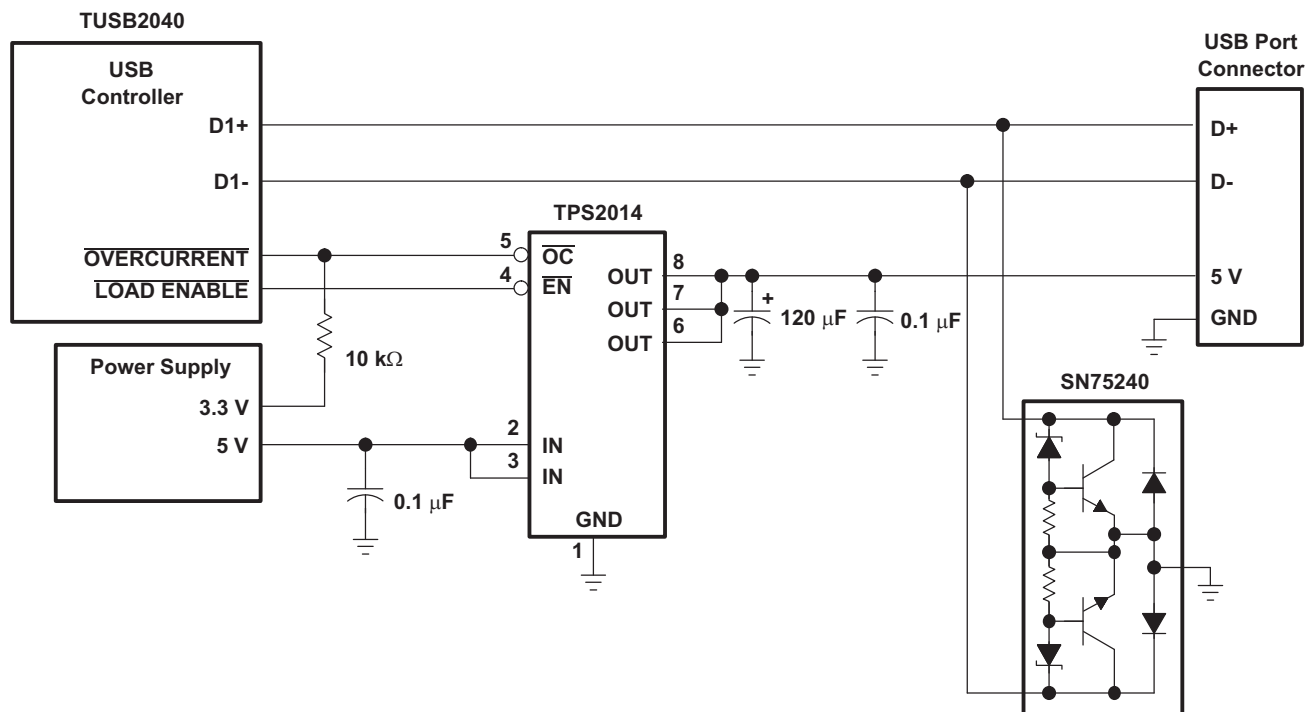


Figure 25. Typical USB Self-Powered Hub Application

LOW POWER BUS-POWERED FUNCTIONS AND HIGH POWER BUS-POWERED FUNCTIONS

Low-power and high-power bus-powered functions are powered by their input ports. If the load of the function is more than the parallel combination of 44Ω and 10 μF, it must implement inrush current limiting. The TPS20xx provides this function with its controlled rise time during turn on.

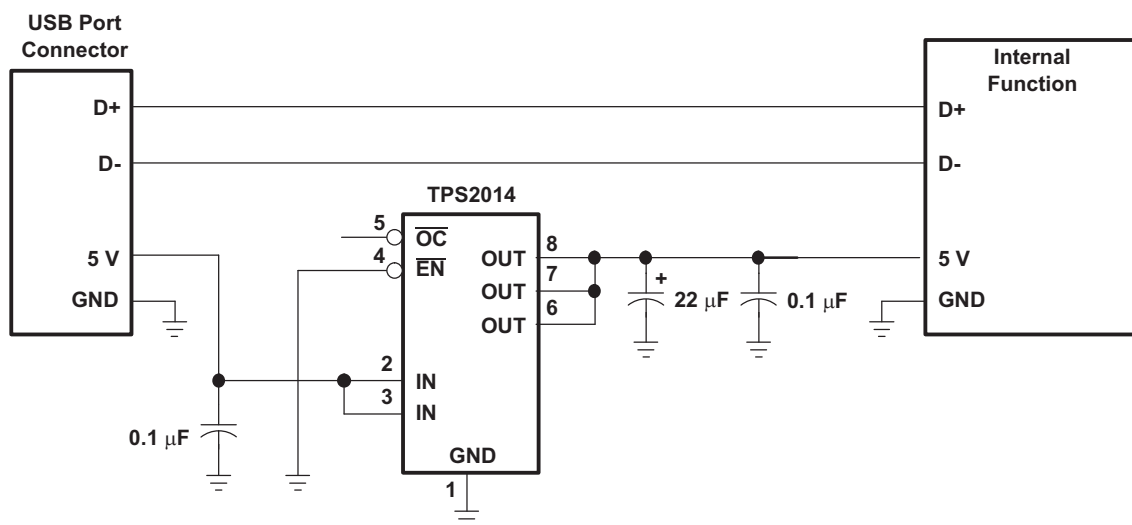


Figure 26. Typical USB Bus-Powered Function Application

ESD PROTECTION

All TPS20xx terminals incorporate ESD-protection circuitry designed to withstand a 6-kV human-body-model discharge as defined in MIL-STD-883C. Additionally, the output is protected from discharges up to 12 kV.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2014D.A	NRND	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	See TPS2014D	2014
TPS2014DR.A	NRND	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See TPS2014DR	2014
TPS2014P.A	NRND	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	See TPS2014P	TPS2014P
TPS2015D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	2015
TPS2015D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	2015
TPS2015DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	2015
TPS2015DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	2015

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

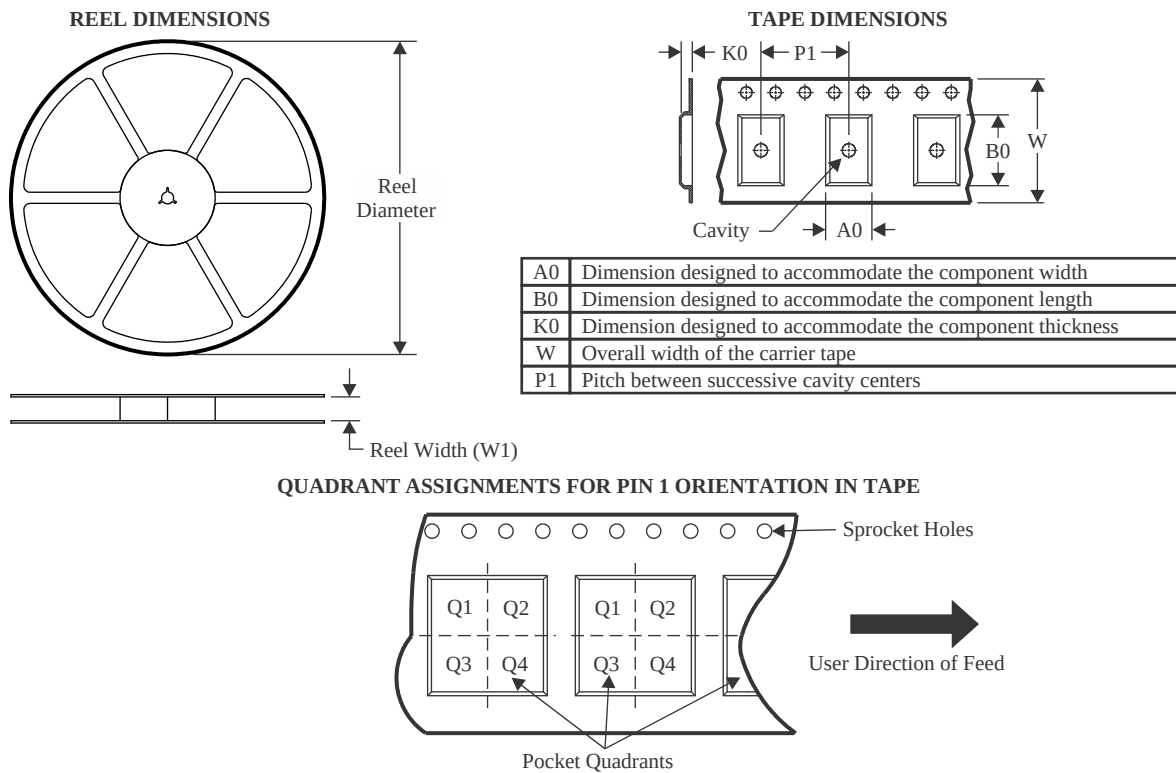
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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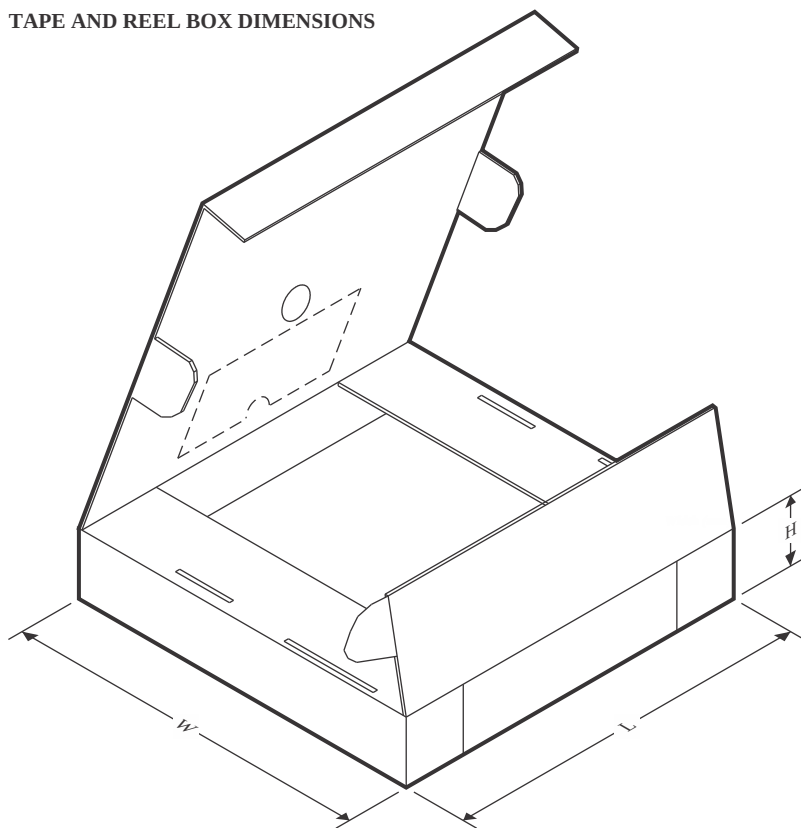
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2015DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

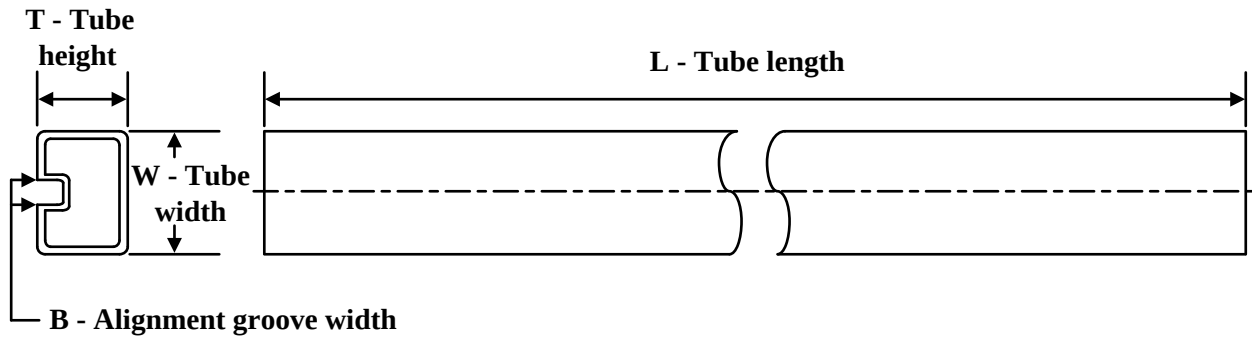
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2015DR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS2014D.A	D	SOIC	8	75	507	8	3940	4.32
TPS2014P.A	P	PDIP	8	50	506	13.97	11230	4.32
TPS2015D	D	SOIC	8	75	507	8	3940	4.32
TPS2015D.A	D	SOIC	8	75	507	8	3940	4.32



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



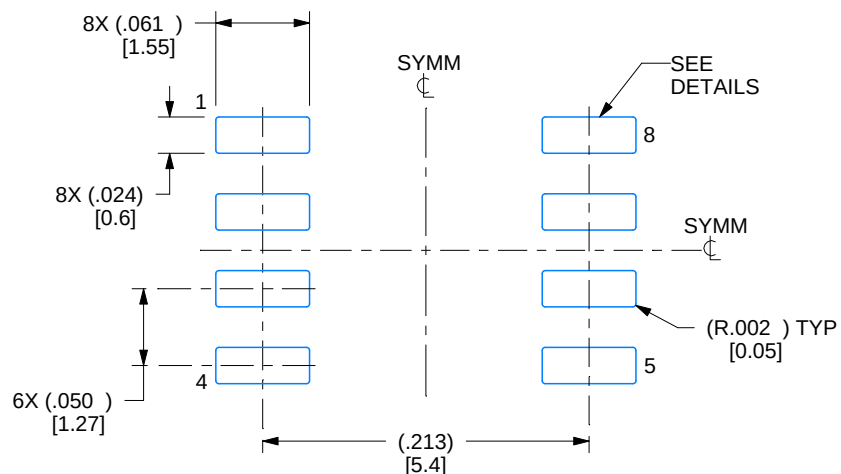
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

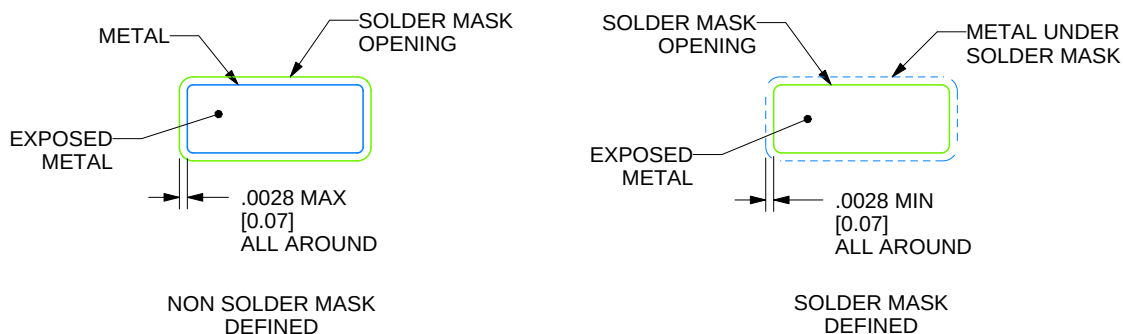
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

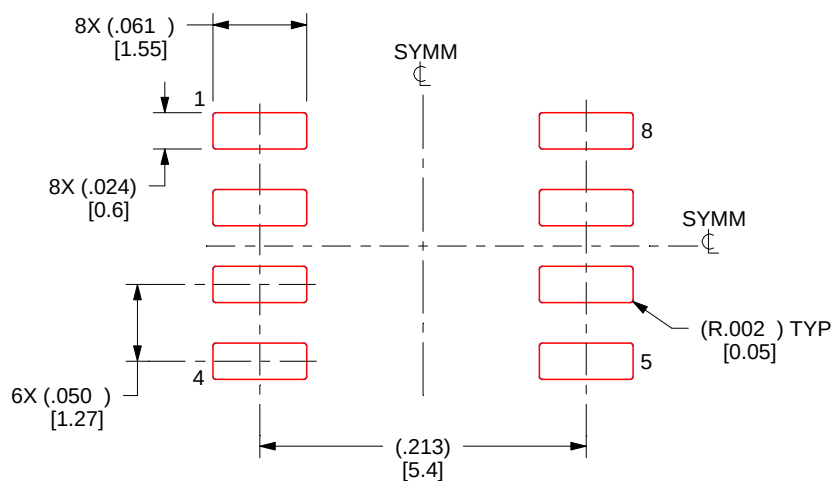
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

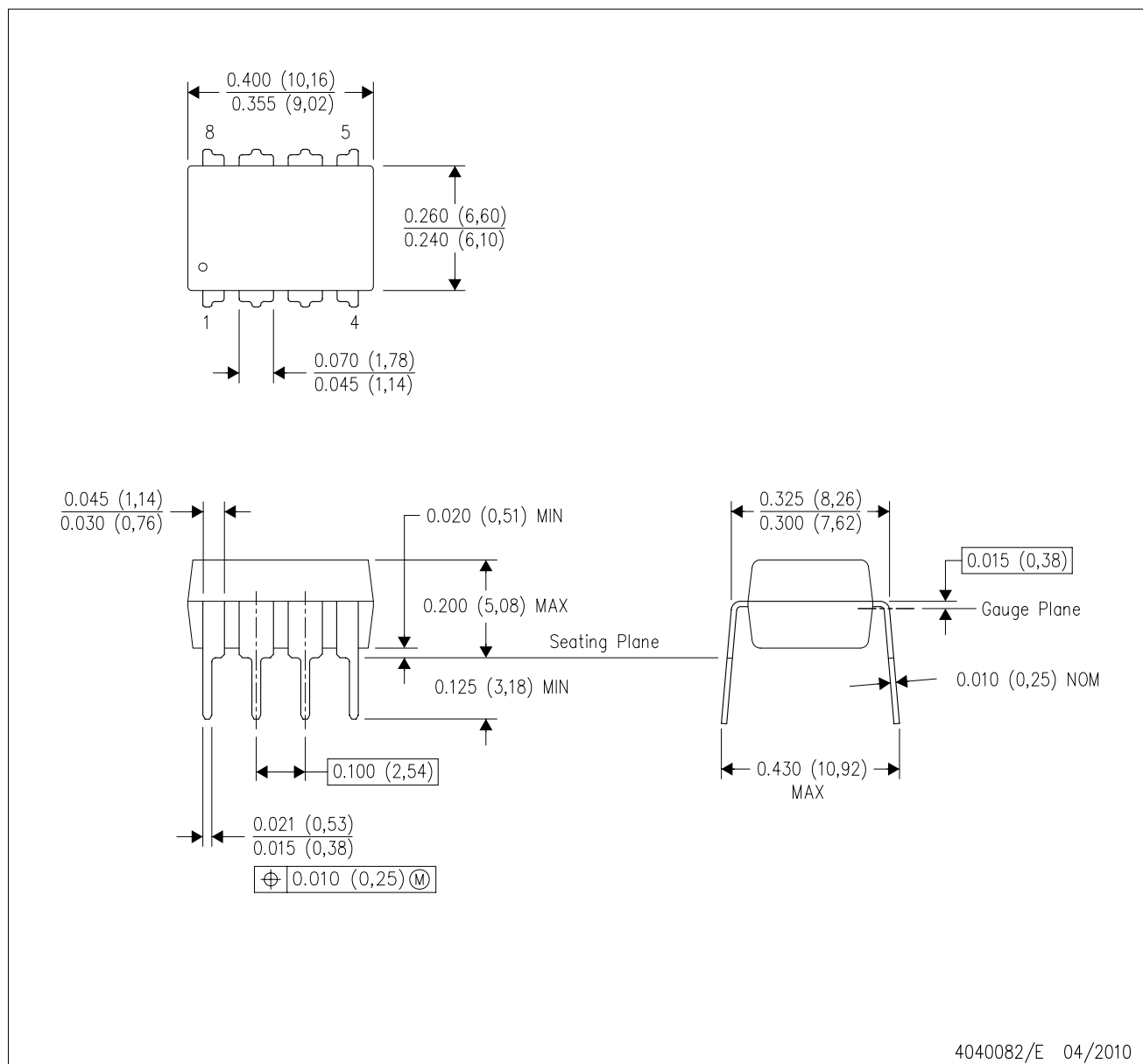
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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