

1N59xxBRNG Series

3 W DO-41 Surmetic 30 Zener Voltage Regulators

This is a 1N59xxBRNG series with limits and excellent operating characteristics that reflect the superior capabilities of silicon-oxide passivated junctions. All this in an axial-lead, transfer-molded plastic package that offers protection in all common environmental conditions.

Features

- Zener Voltage Range – 3.3 V to 200 V
- ESD Rating of Class 3 (>16 KV) per Human Body Model
- Surge Rating of 98 W @ 1 ms
- Maximum Limits Guaranteed on up to Six Electrical Parameters
- Package No Larger than the Conventional 1 W Package
- This is a Pb-Free Device

Mechanical Characteristics

CASE: Void free, transfer-molded, thermosetting plastic

FINISH: All external surfaces are corrosion resistant and leads are readily solderable

MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 260°C, 1/16" from the case for 10 seconds

POLARITY: Cathode indicated by polarity band

MOUNTING POSITION: Any

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Max. Steady State Power Dissipation @ $T_L = 75^\circ\text{C}$, Lead Length = 3/8" Derate above 75°C	P_D	3.0 24	W mW/°C
Steady State Power Dissipation @ $T_A = 50^\circ\text{C}$ Derate above 50°C	P_D	1.0 6.67	W mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to +200	°C

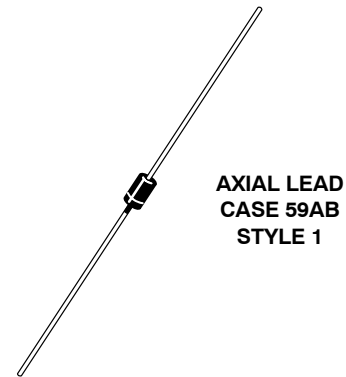
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

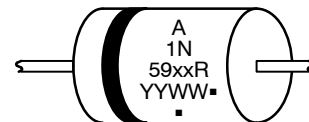


ON Semiconductor®

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MARKING DIAGRAM



A = Assembly Location
1N59xxR = Device Number
YY = Year
WW = Work Week
■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
1N59xxBRNG	Axial Lead (Pb-Free)	3000 Units / Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

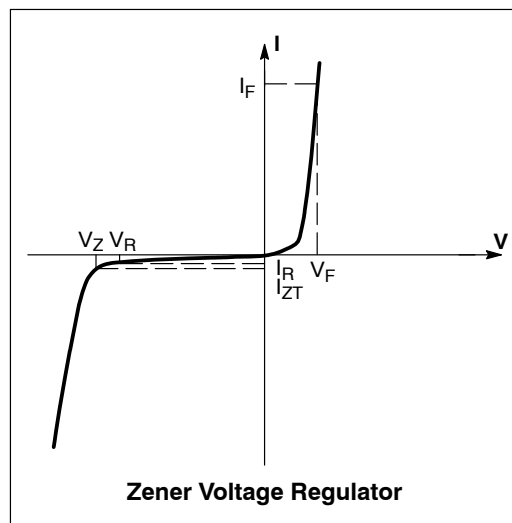
1N59xxBRNG Series

ELECTRICAL CHARACTERISTICS

($T_L = 30^\circ\text{C}$ unless otherwise noted,

$V_F = 1.5\text{ V Max @ } I_F = 200\text{ mAdc}$ for all types)

Symbol	Parameter
V_Z	Reverse Zener Voltage @ I_{ZT}
I_{ZT}	Reverse Current
Z_{ZT}	Maximum Zener Impedance @ I_{ZT}
I_{ZK}	Reverse Current
Z_{ZK}	Maximum Zener Impedance @ I_{ZK}
I_R	Reverse Leakage Current @ V_R
V_R	Breakdown Voltage
I_F	Forward Current
V_F	Forward Voltage @ I_F
I_{ZM}	Maximum DC Zener Current



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ELECTRICAL CHARACTERISTICS ($T_L = 30^\circ\text{C}$ unless otherwise noted, $V_F = 1.5\text{ V Max}$ @ $I_F = 200\text{ mAdc}$ for all types)

Device [†] (Note 1)	Device Marking	Zener Voltage (Note 2)				Zener Impedance (Note 3)			Leakage Current		I _{ZM}
		V _Z (Volts)			@ I _{ZT}	Z _{ZT} @ I _{ZT}	Z _{ZK} @ I _{ZK}	I _R @ V _R			
		Min	Nom	Max	mA	Ω	Ω	mA	μA Max	Volts	
1N5929BRNG	1N5929R	14.25	15	15.75	25.0	9	600	0.25	1	11.4	100
1N5932BRNG	1N5932R	19.00	20	21.00	18.7	14	650	0.25	1	15.2	75
1N5934BRNG	1N5934R	22.80	24	25.20	15.6	19	700	0.25	1	18.2	62

[†]The "G" suffix indicates Pb-Free package available.

1. TOLERANCE AND TYPE NUMBER DESIGNATION

Tolerance designation – device tolerance of $\pm 5\%$ are indicated by a "B" suffix.

2. ZENER VOLTAGE (V_Z) MEASUREMENT

ON Semiconductor guarantees the zener voltage when measured at 90 seconds while maintaining the lead temperature (T_L) at $30^\circ\text{C} \pm 1^\circ\text{C}$, $3/8"$ from the diode body.

3. ZENER IMPEDANCE (Z_Z) DERIVATION

The zener impedance is derived from 60 seconds AC voltage, which results when an AC current having an rms value equal to 10% of the DC zener current (I_{ZT} or I_{ZK}) is superimposed on I_{ZT} or I_{ZK} .

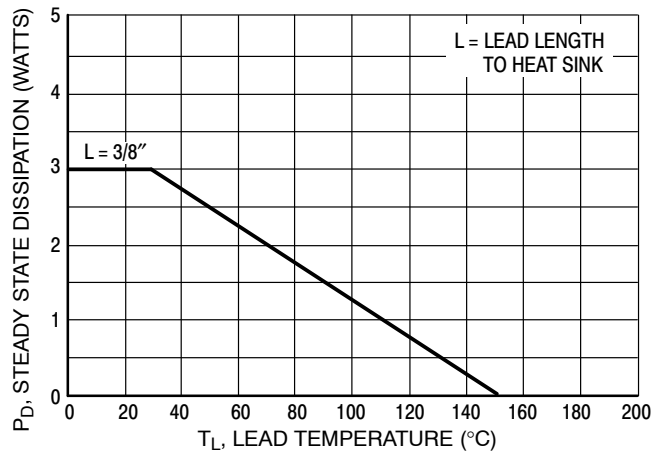


Figure 1. Power Temperature Derating Curve

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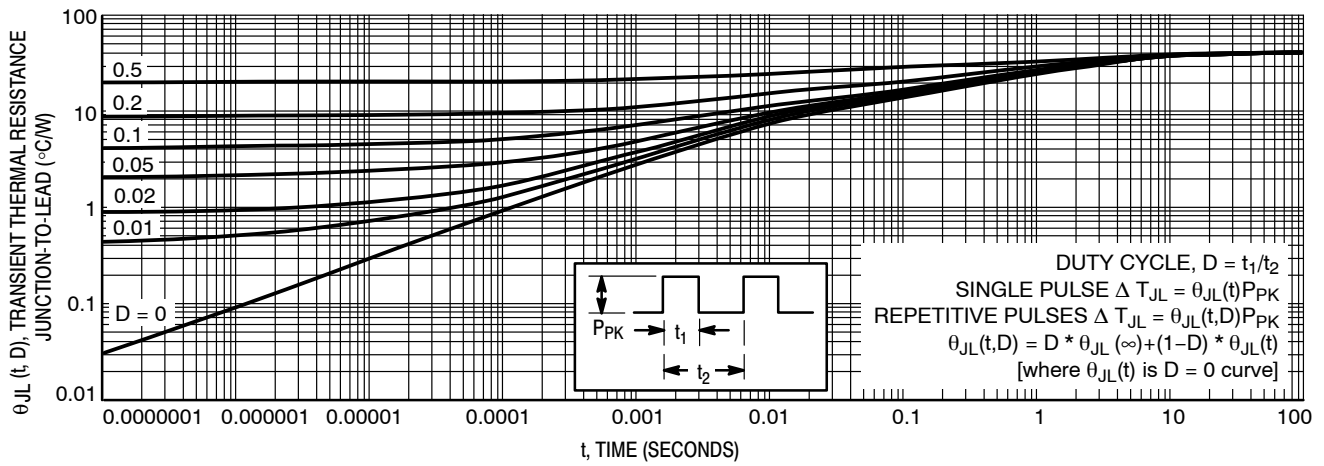


Figure 2. Typical Thermal Response L, Lead Length = 3/8 Inch

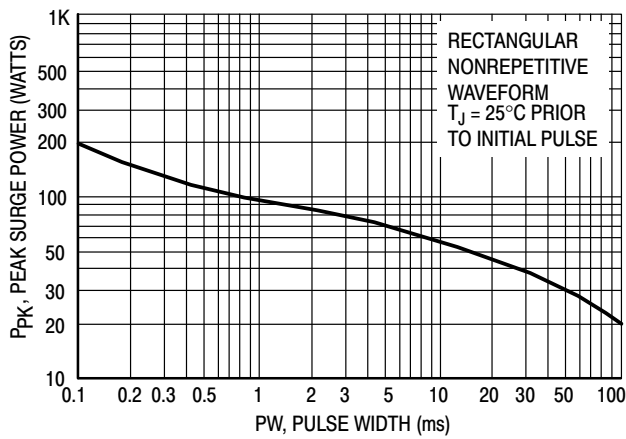


Figure 3. Maximum Surge Power

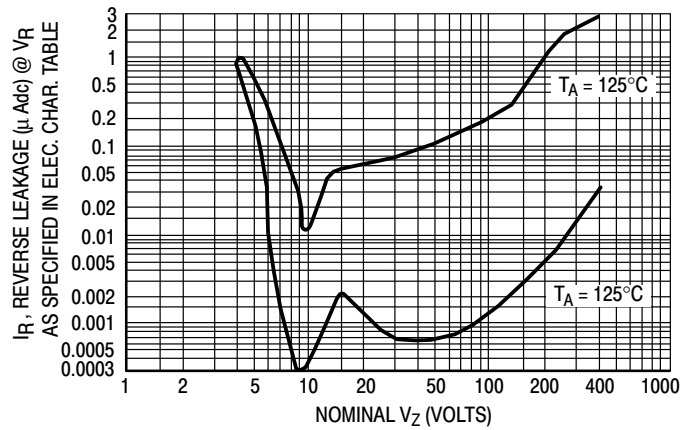


Figure 4. Typical Reverse Leakage

APPLICATION NOTE

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions in order to calculate its value. The following procedure is recommended:

Lead Temperature, T_L , should be determined from:

$$T_L = \theta_{LA} P_D + T_A$$

θ_{LA} is the lead-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$) and P_D is the power dissipation. The value for θ_{LA} will vary and depends on the device mounting method. θ_{LA} is generally $30\text{--}40^{\circ}\text{C}/\text{W}$ for the various clips and tie points in common use and for printed circuit board wiring.

The temperature of the lead can also be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L , the junction temperature may be determined by:

$$T_J = T_L + \Delta T_{JL}$$

ΔT_{JL} is the increase in junction temperature above the lead temperature and may be found from Figure 2 for a train of power pulses ($L = 3/8$ inch) or from Figure 10 for dc power.

$$\Delta T_{JL} = \theta_{JL} P_D$$

For worst-case design, using expected limits of I_Z , limits of P_D and the extremes of T_J (ΔT_J) may be estimated. Changes in voltage, V_Z , can then be found from:

$$\Delta V = \theta_{VZ} \Delta T_J$$

θ_{VZ} , the zener voltage temperature coefficient, is found from Figures 5 and 6.

Under high power-pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, keep current excursions as low as possible.

Data of Figure 2 should not be used to compute surge capability. Surge limitations are given in Figure 3. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 3 be exceeded.

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TEMPERATURE COEFFICIENT RANGES

(90% of the Units are in the Ranges Indicated)

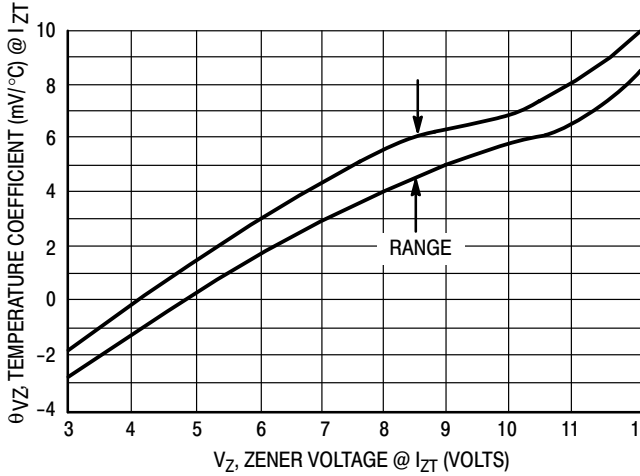


Figure 5. Units To 12 Volts

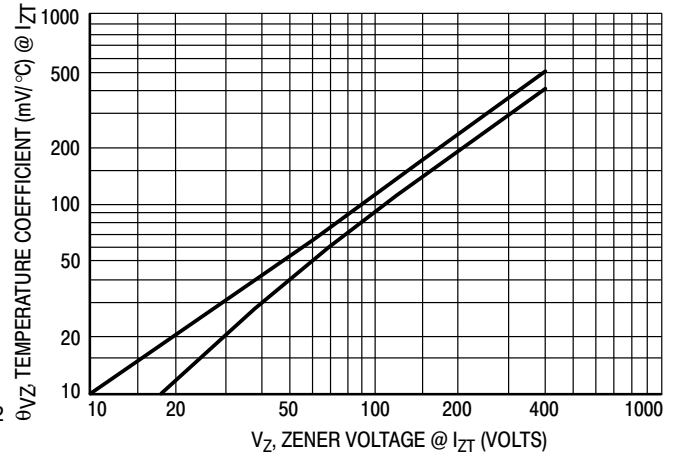


Figure 6. Units 10 To 400 Volts

ZENER VOLTAGE versus ZENER CURRENT

(Figures 7, 8 and 9)

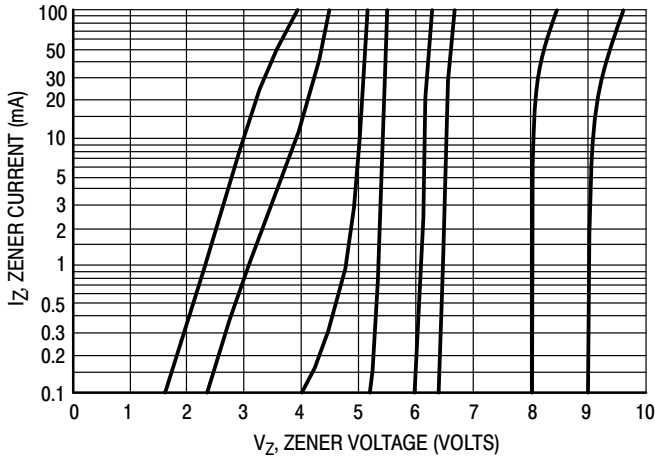


Figure 7. $V_Z = 3.3$ thru 10 Volts

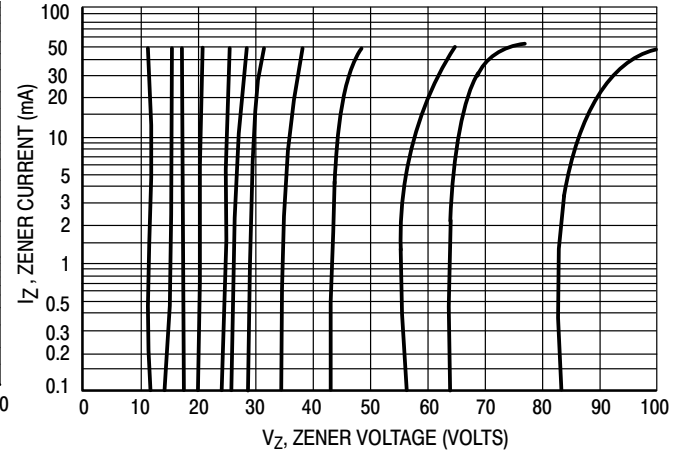


Figure 8. $V_Z = 12$ thru 82 Volts

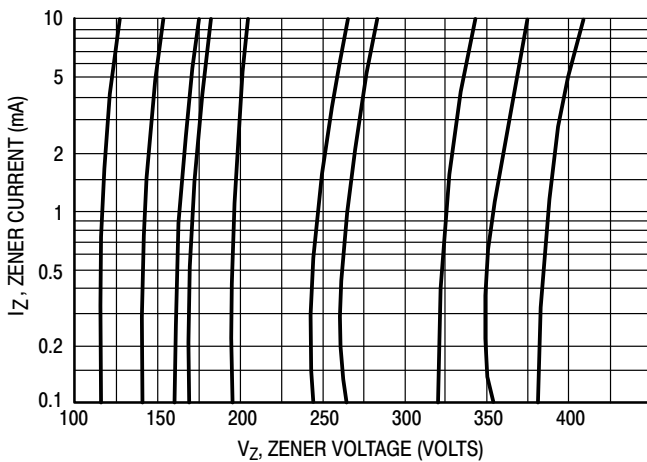


Figure 9. $V_Z = 100$ thru 400 Volts

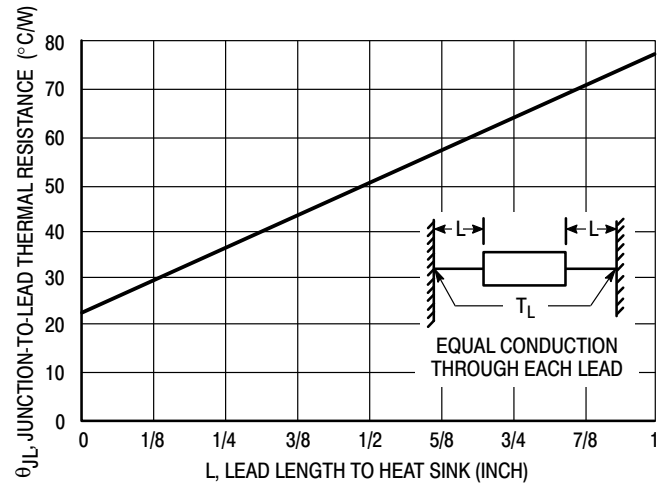


Figure 10. Typical Thermal Resistance

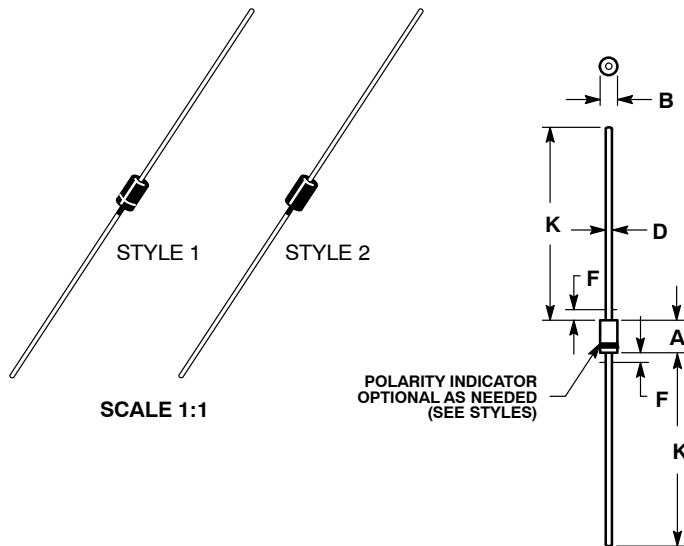
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



AXIAL LEAD CASE 59AB ISSUE O

DATE 07 DEC 2011



STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

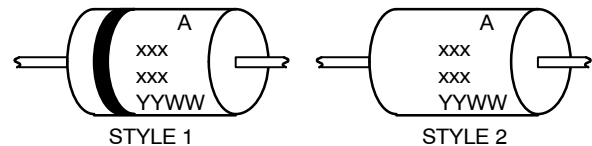
STYLE 2:
NO POLARITY

NOTES:

1. CONTROLLING DIMENSION: INCHES.
2. PACKAGE CONTOUR IS OPTIONAL WITHIN DIMENSIONS A AND B. HEAT SLUGS, IF ANY, SHALL BE WITHIN DIMENSION B BUT NOT SUBJECT TO ITS MINIMUM VALUE.
3. DIMENSION A DEFINES THE ENTIRE BODY INCLUDING HEAT SLUGS.
4. DIMENSION B IS MEASURED AT THE MAXIMUM DIAMETER OF THE BODY.
5. POLARITY SHALL BE DENOTED BY A CATHODE BAND.
6. LEAD DIAMETER, D, IS NOT CONTROLLED IN ZONE F.
7. ALL RULES AND NOTES ASSOCIATED WITH JEDEC DO-41 OUTLINE SHALL APPLY

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.161	0.205	4.10	5.20
B	0.079	0.106	2.00	2.70
D	0.028	0.034	0.71	0.86
F	---	0.050	---	1.27
K	0.540	---	13.70	---

GENERIC MARKING DIAGRAM*



xxxxxxx = Specific Device Code
A = Assembly Location
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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