



High-Speed Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.5MHz
- HIGH SLEW RATE: 35V/ μ s
- LOW OFFSET: $\pm 250\mu$ V max
- LOW BIAS CURRENT: ± 1 pA max
- FAST SETTLING TIME: 1 μ s to 0.01%
- UNITY-GAIN STABLE

DESCRIPTION

The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic *Difet* (dielectrically isolated FET) construction provides an unusual combination of high-speed and accuracy.

Its wide-bandwidth design minimizes dynamic errors. High slew rate and fast settling time allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion minimize AC errors. All specifications are rated with a 1k Ω resistor in parallel with 500pF load. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

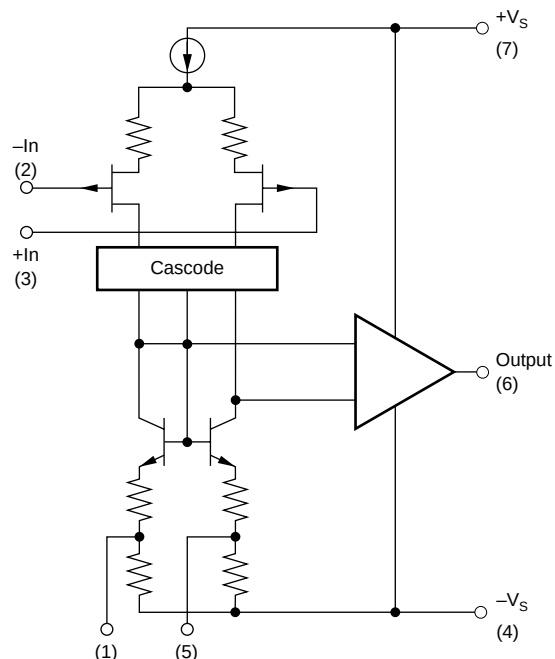
Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. *Difet* construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.

Difet[®] Burr-Brown Corp.

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DATA CONVERSION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage	$\pm 18V_{DC}$
Internal Power Dissipation ($T_J \leq +175^\circ C$)	1000mW
Differential Input Voltage	Total V_S
Input Voltage Range	$\pm V_S$
Storage Temperature Range	
P and U Packages	$-40^\circ C$ to $+125^\circ C$
Operating Temperature Range	
P and U Packages	$-25^\circ C$ to $+85^\circ C$
Lead Temperature	
U Package, SO (3s)	$+260^\circ C$
Output Short-Circuit to Ground ($+25^\circ C$)	Continuous
Junction Temperature	$+175^\circ C$

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

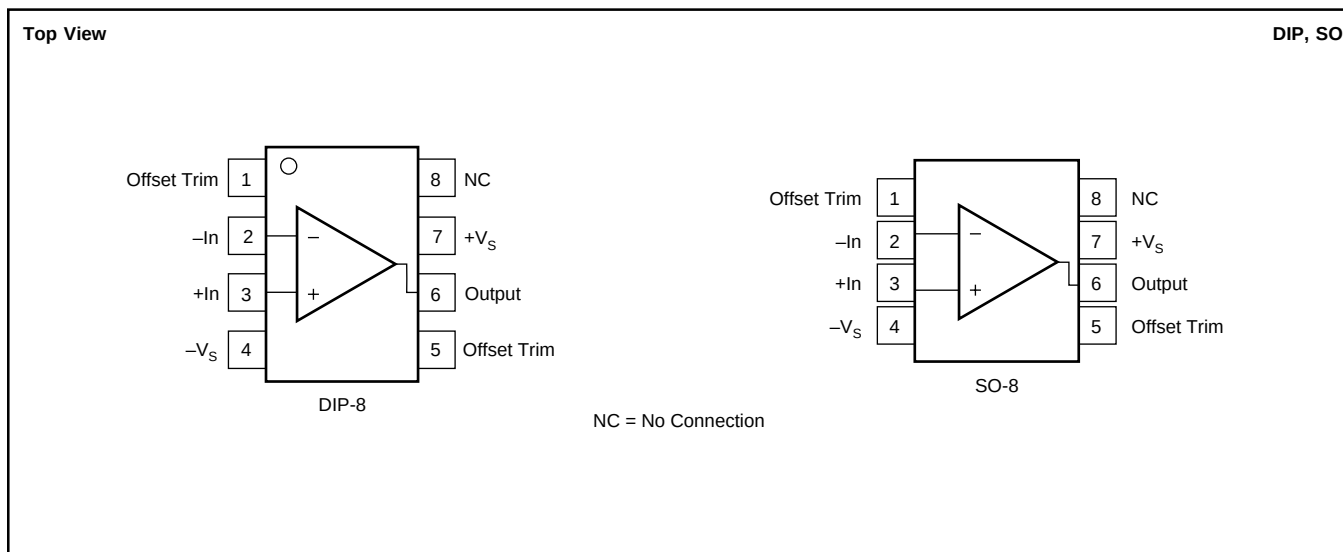
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	OFFSET VOLTAGE MAX (μV) AT $25^\circ C$	PACKAGE-LEAD	PACKAGE DESIGNATOR ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA602AP	± 2000	DIP-8	P	$-25^\circ C$ to $+85^\circ C$	602AP	602AP	Tubes, 50
OPA602BP	± 1000	"	"	"	602BP	602BP	Tubes, 50
OPA602AU	± 3000	SO-8	D	$-25^\circ C$ to $+85^\circ C$	602AU	602AU	Tubes, 100

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATIONS



ELECTRICAL CHARACTERISTICS

At $V_S = \pm 15V_{DC}$ and $T_A = +25^\circ C$, unless otherwise noted.

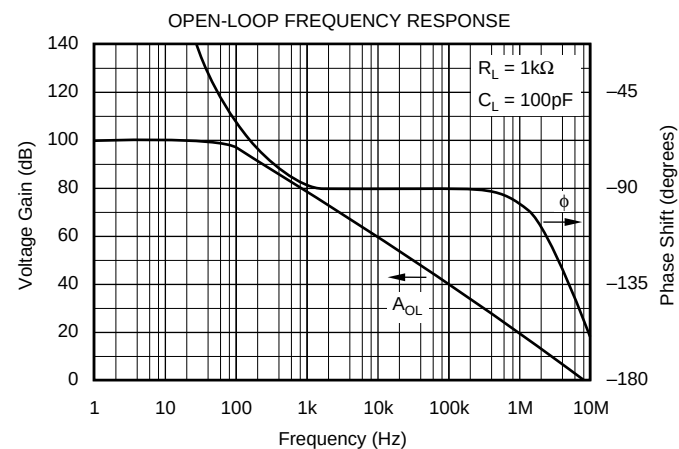
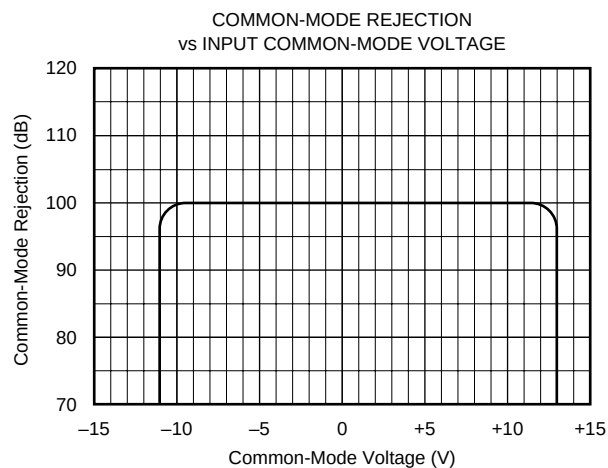
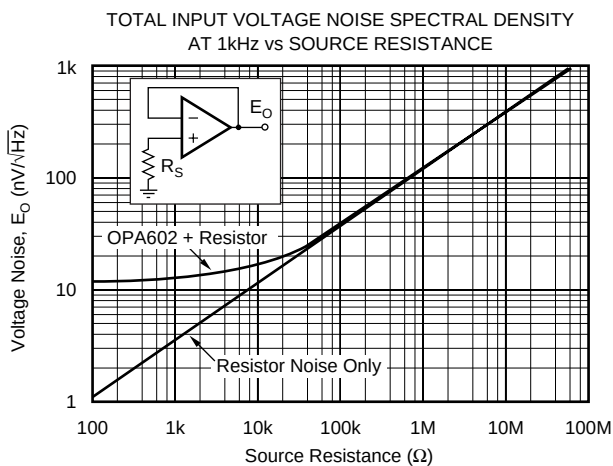
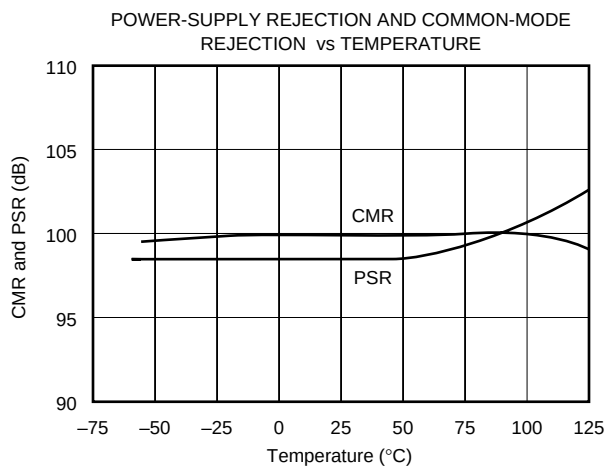
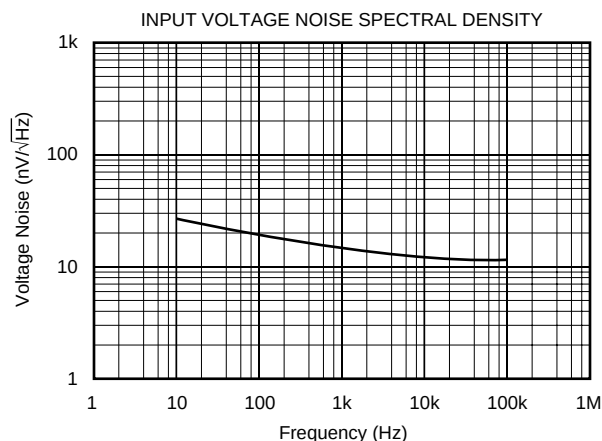
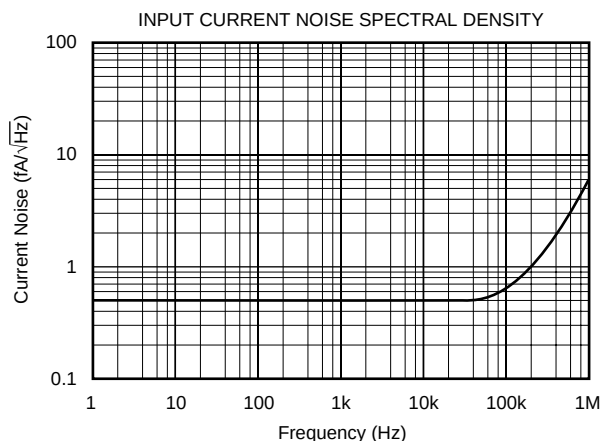
PARAMETER	CONDITIONS	OPA602BP			OPA602AP, AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE Voltage: $f_O = 10\text{Hz}$ $f_O = 100\text{Hz}$ $f_O = 1\text{kHz}$ $f_O = 10\text{kHz}$ $f_B = 10\text{Hz to } 10\text{kHz}$ $f_B = 0.1\text{Hz to } 10\text{Hz}$ Current: $f_B = 0.1\text{Hz to } 10\text{Hz}$ $f_O = 0.1\text{Hz to } 20\text{kHz}$			23 19 13 12 1.4 0.95			*		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ μVrms $\mu\text{Vp-p}$
OFFSET VOLTAGE Input Offset Voltage: P Package U Package Over Specified Temperature P, U Packages Average Drift ⁽¹⁾ Supply Rejection	$T_A = T_{MIN} \text{ to } T_{MAX}$ $\pm V_S = 12\text{V to } 18\text{V}$		0.5 ± 0.75 ± 3 100	1 ± 1.5 ± 5		1 1 ± 1.5 *	2 3 ± 15	mV mV mV $\mu\text{V}/^\circ\text{C}$ dB
BIAS CURRENT Input Bias Current Over Specified Temperature	$V_{CM} = 0V_{DC}$		± 1 ± 20	± 2 ± 200		± 2 ± 20	± 10 ± 500	pA pA
OFFSET CURRENT Input Offset Current Over Specified Temperature	$V_{CM} = 0V_{DC}$		0.5 20	2 200		1 20	10 500	pA pA
INPUT IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$ $10^{14} \parallel 3$			*		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10V_{DC}$	± 10.2 88	+13, -11 100		*	*		V dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 1\text{k}\Omega$	88	100		75	*		dB
FREQUENCY RESPONSE Gain Bandwidth Full-Power Response Slew Rate Settling Time: 0.1% 0.01%	Gain = 100 $20\text{Vp-p}, R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{V}, R_L = 1\text{k}\Omega$ Gain = -1, $R_L = 1\text{k}\Omega$ $C_L = 500\text{pF}, 10\text{V Step}$	4 24	6.5 570 35		3.5 20	*		MHz kHz V/ μs μs μs
RATED OUTPUT Voltage Output Current Output Output Resistance Load Capacitance Stability Short-Circuit Current	$R_L = 1\text{k}\Omega$ $V_O = \pm 10V_{DC}$ 1MHz, Open Loop Gain = +1	± 11.5 ± 15 ± 30	+12.9, -13.8 ± 20 80 1500 ± 50		± 11 * ± 25	* * * *		V mA Ω pF mA
POWER SUPPLY Rated Voltage Voltage Range, Derated Performance Current, Quiescent Over Specified Temperature	$I_O = 0\text{mADC}$	± 5	± 15 3 3.5	± 18 4 4.5	*	*	*	V_{DC} V_{DC} mA mA
TEMPERATURE RANGE Specification Operating: P, U Packages Storage: P, U Packages θ_{JA}	Ambient Temperature	-25 -25 -40 200		+85 +85 +125	* * * *		* * * $^\circ\text{C/W}$	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$

* Same specifications as OPA602BP.

NOTE: (1) OPA602AP, AU ensured by design with a 99% confidence level.

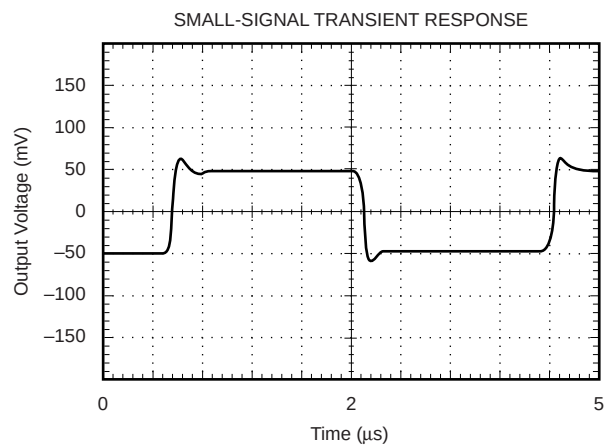
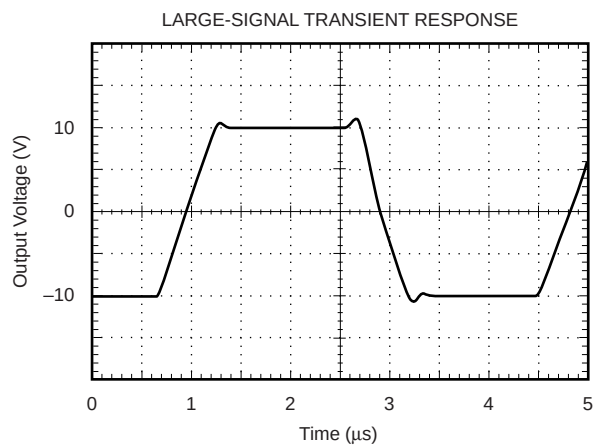
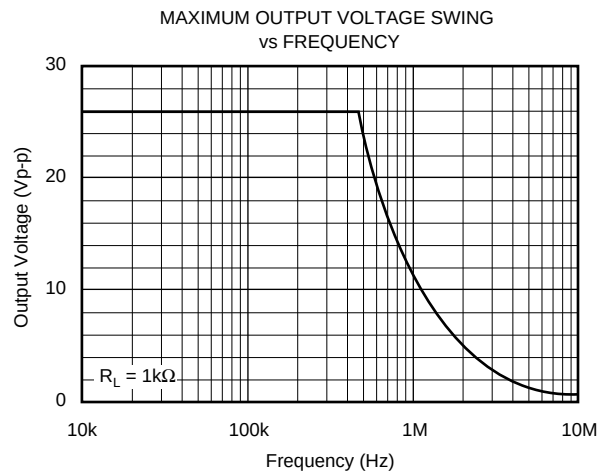
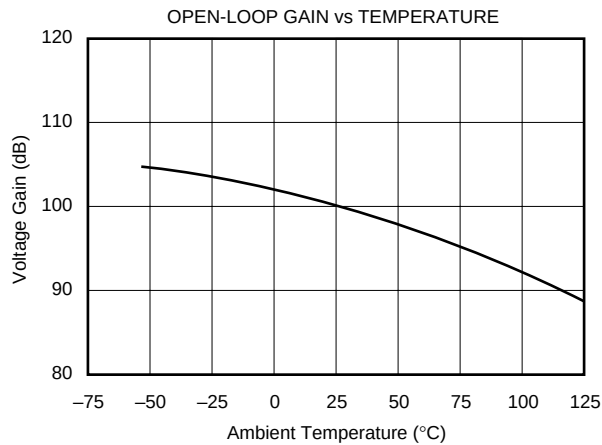
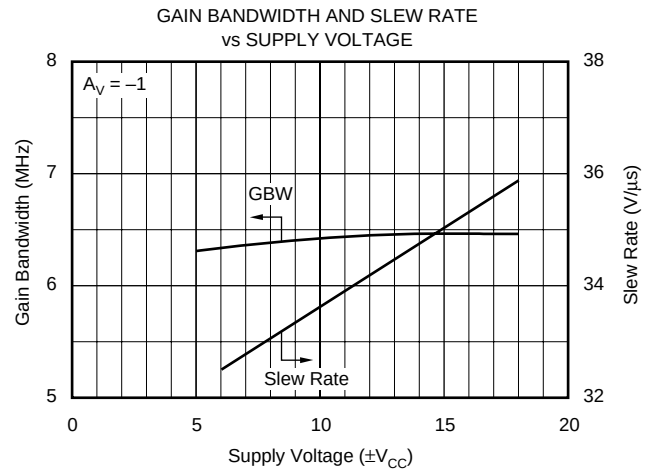
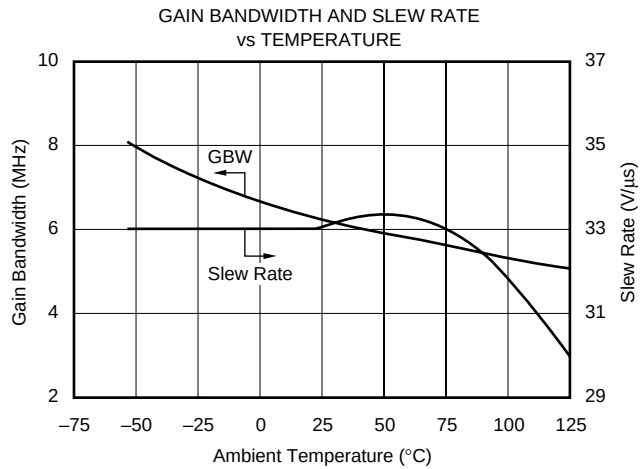
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}_{\text{DC}}$, unless otherwise noted.



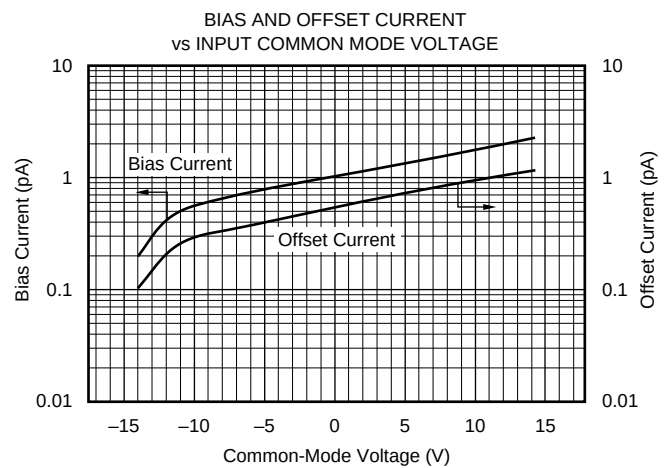
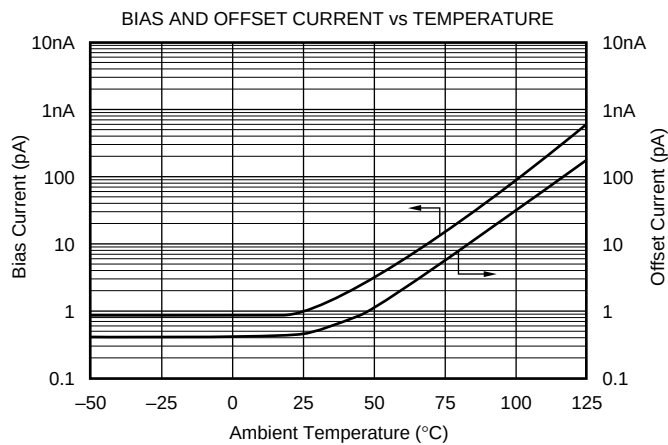
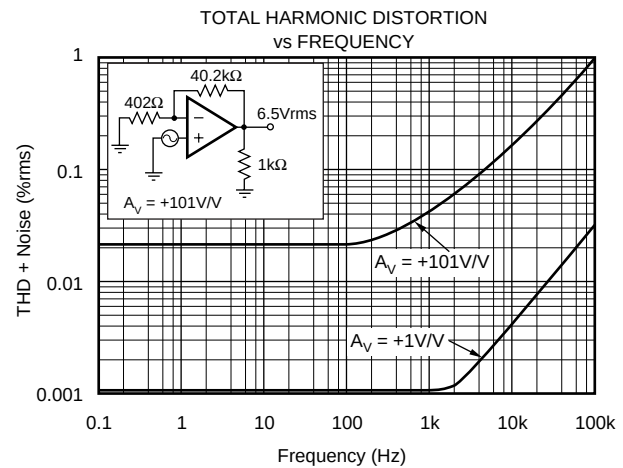
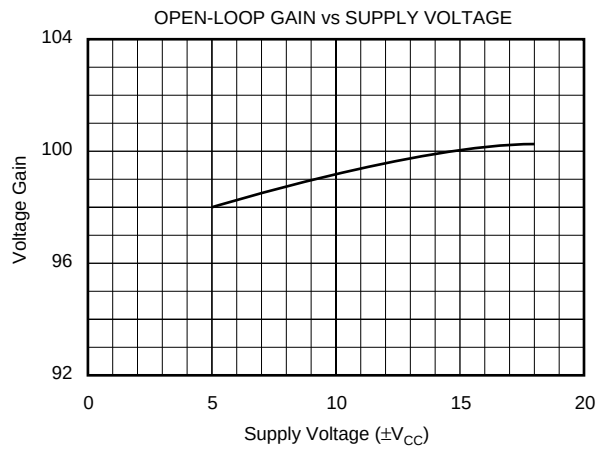
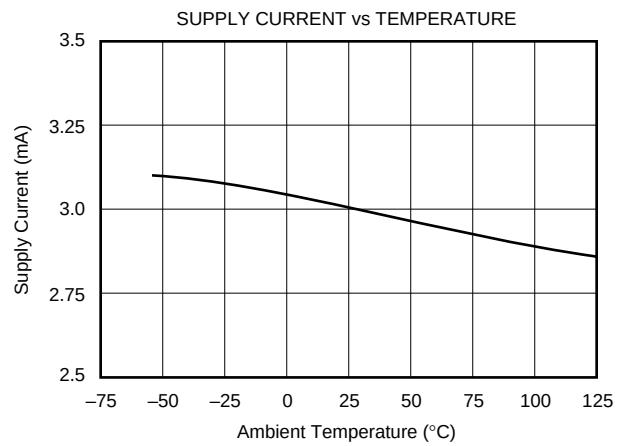
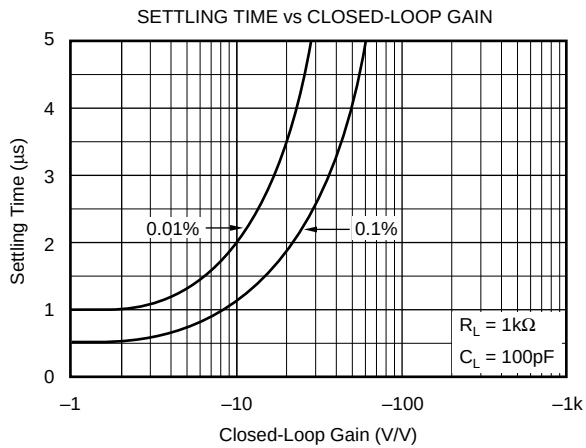
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}_{\text{DC}}$, unless otherwise noted.



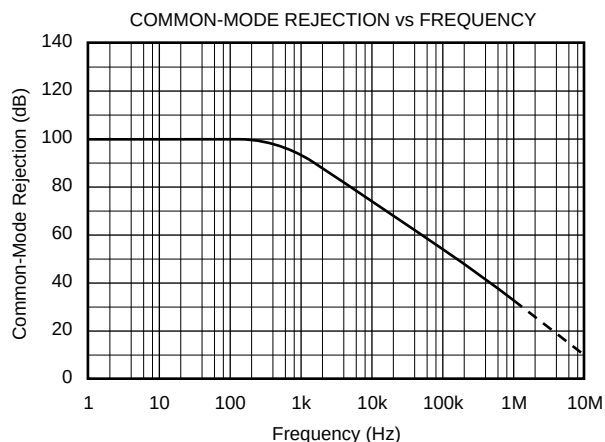
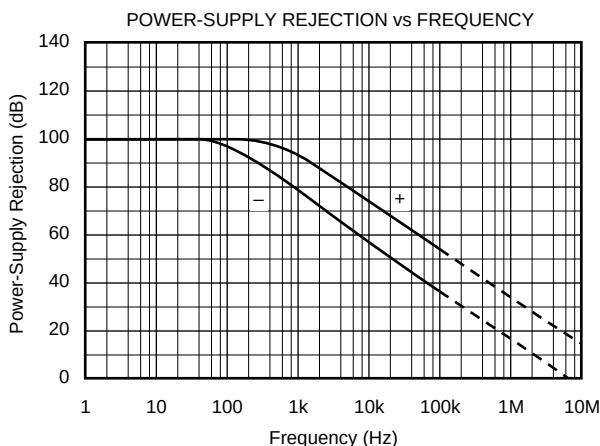
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}_{\text{DC}}$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}_{\text{DC}}$, unless otherwise noted.



APPLICATIONS INFORMATION

Unity-gain stability with good phase margin and excellent output drive characteristics bring freedom from the subtle problems associated with other high-speed amplifiers. However, as with any high-speed, wide bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the inverting input pin.

Power supplies should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases $0.1\mu\text{F}$ ceramic capacitors are adequate. Applications with heavier loads and fast transient waveforms may benefit from use of additional $1.0\mu\text{F}$ tantalum bypass capacitors.

INPUT BIAS CURRENT GUARDING

Leakage currents across printed circuit boards can easily exceed the input bias current of the OPA602. A circuit board “guard” pattern, as shown in Figure 1, is an effective solution to difficult leakage problems. This guard pattern must be repeated on all layers of a multilayer board. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage currents will flow harmlessly to the low-impedance node.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be cleaned with appropriate solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at $+85^\circ\text{C}$.

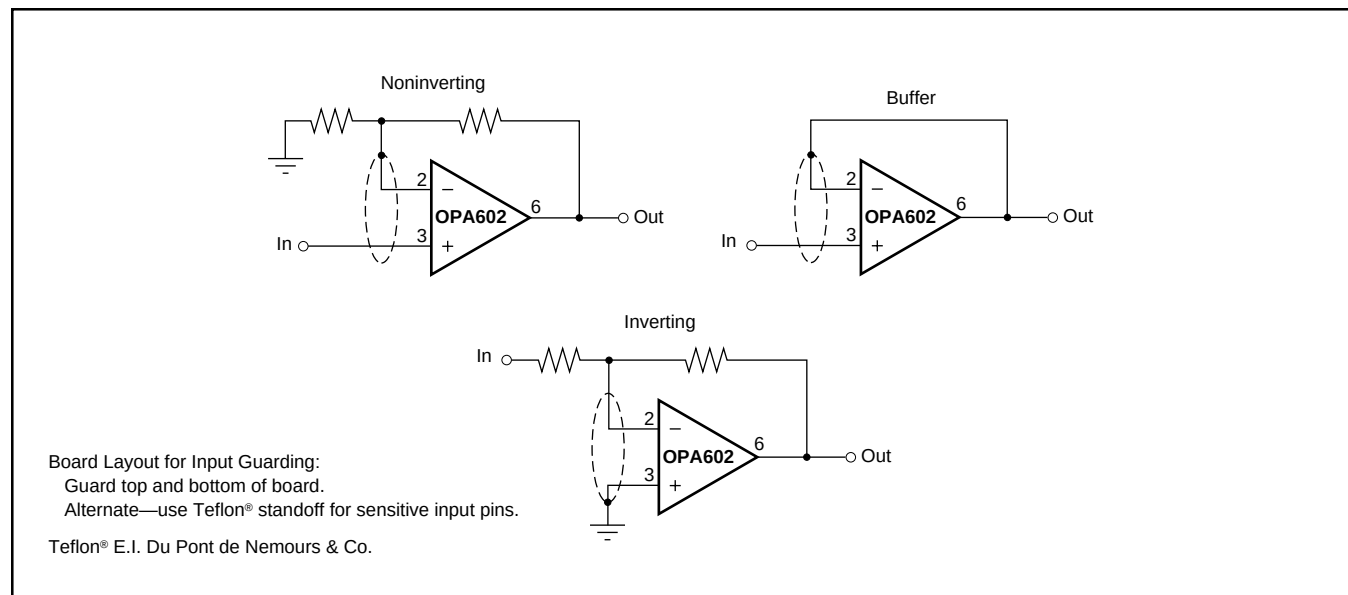
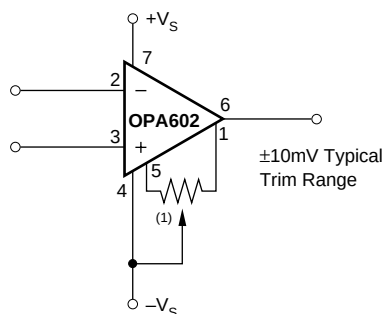


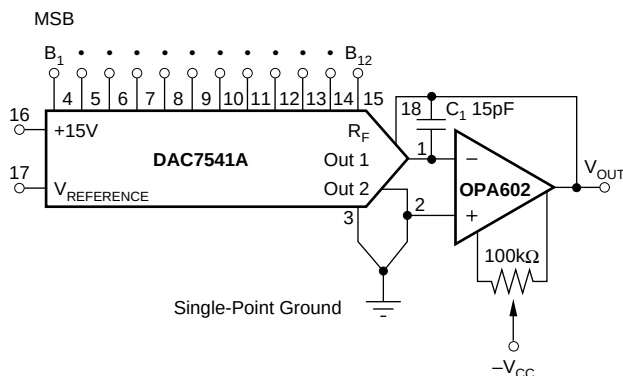
FIGURE 1. Connection of Input Guard.

APPLICATION CIRCUITS



NOTE: (1) 10kΩ to 1MΩ trim potentiometer (100kΩ recommended).

FIGURE 2. Offset Voltage Trim.



$$V_{OUT} = -V_{REF} \left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \dots + \frac{B_{12}}{4096} \right)$$

$$-10V \leq V_{REF} \leq +10V$$

$$0 \leq V_{OUT} \leq -\frac{4095}{4096} V_{REF}$$

Where: $B_N = 1$ if the B_N digital input is high.
 $B_N = 0$ if the B_N digital input is low.

FIGURE 3. Voltage Output Digital-to-Analog Converter.

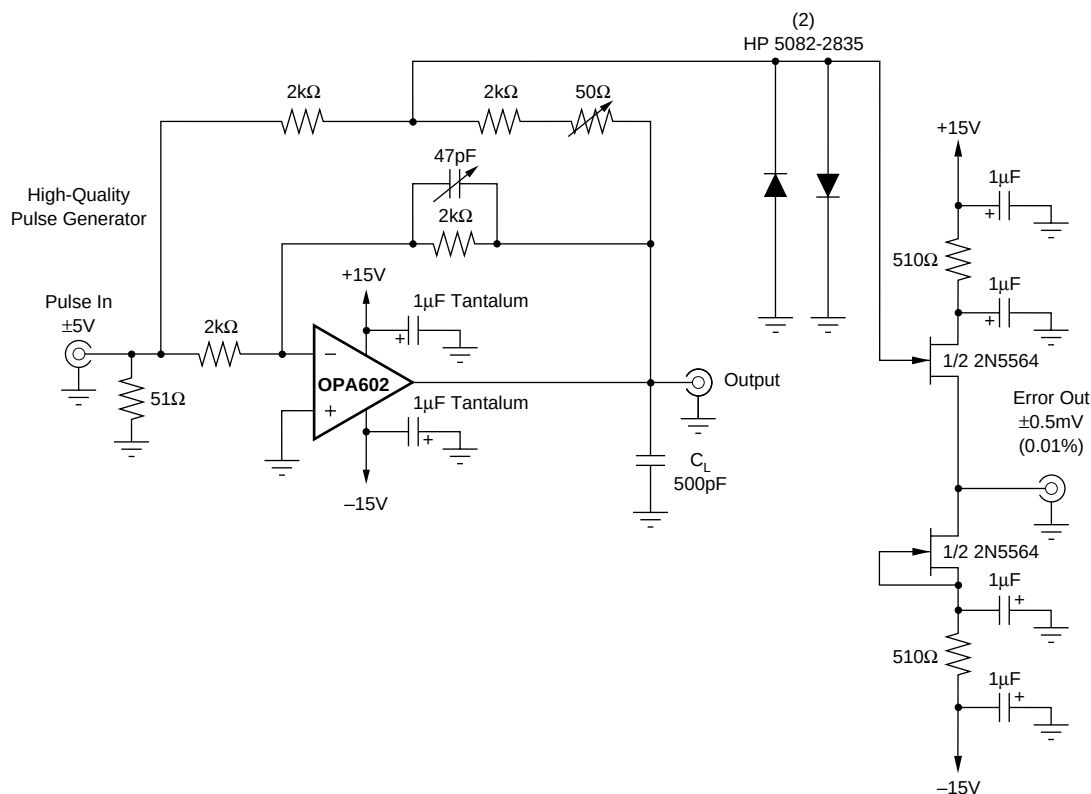
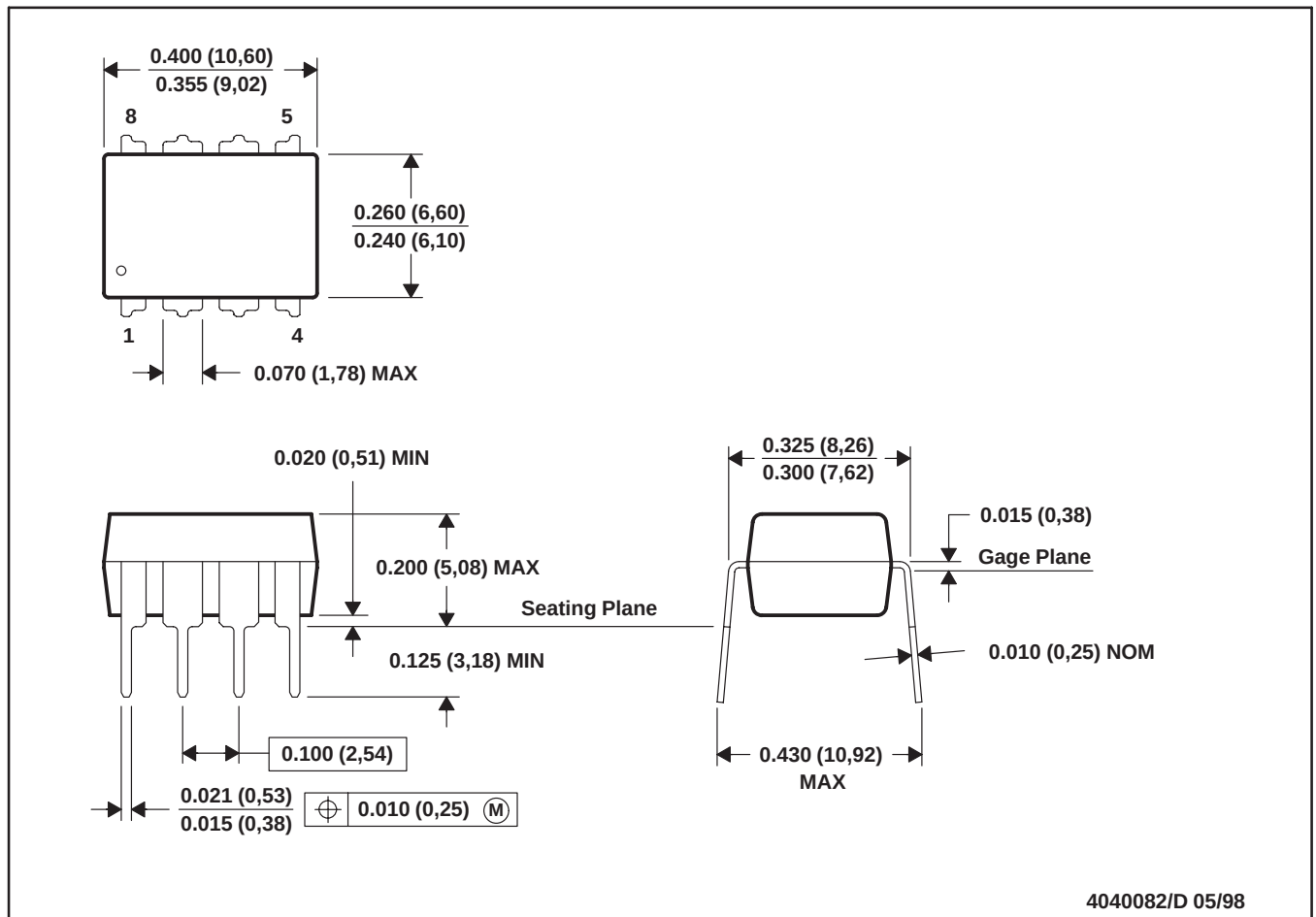


FIGURE 4. Settling Time and Slew Rate Test Circuit.

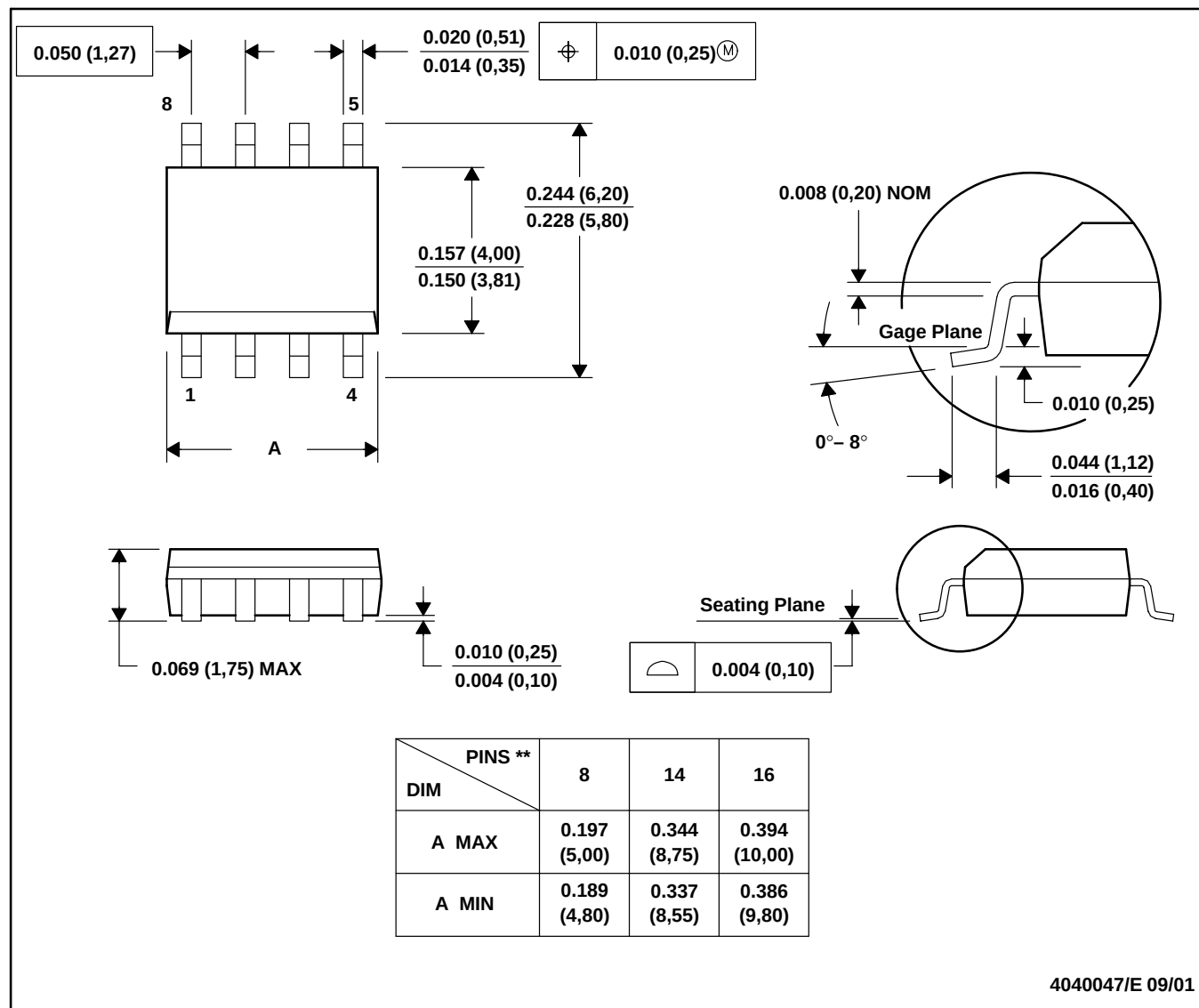


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA602AU	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 602AU
OPA602AU.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 602AU
OPA602AU/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 602AU
OPA602AU/2K5.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 602AU
OPA602AU/2K5E4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 602AU
OPA602AUE4	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 602AU
OPA602BP	Obsolete	Production	PDIP (P) 8	-	-	Call TI	Call TI	-	OPA602BP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

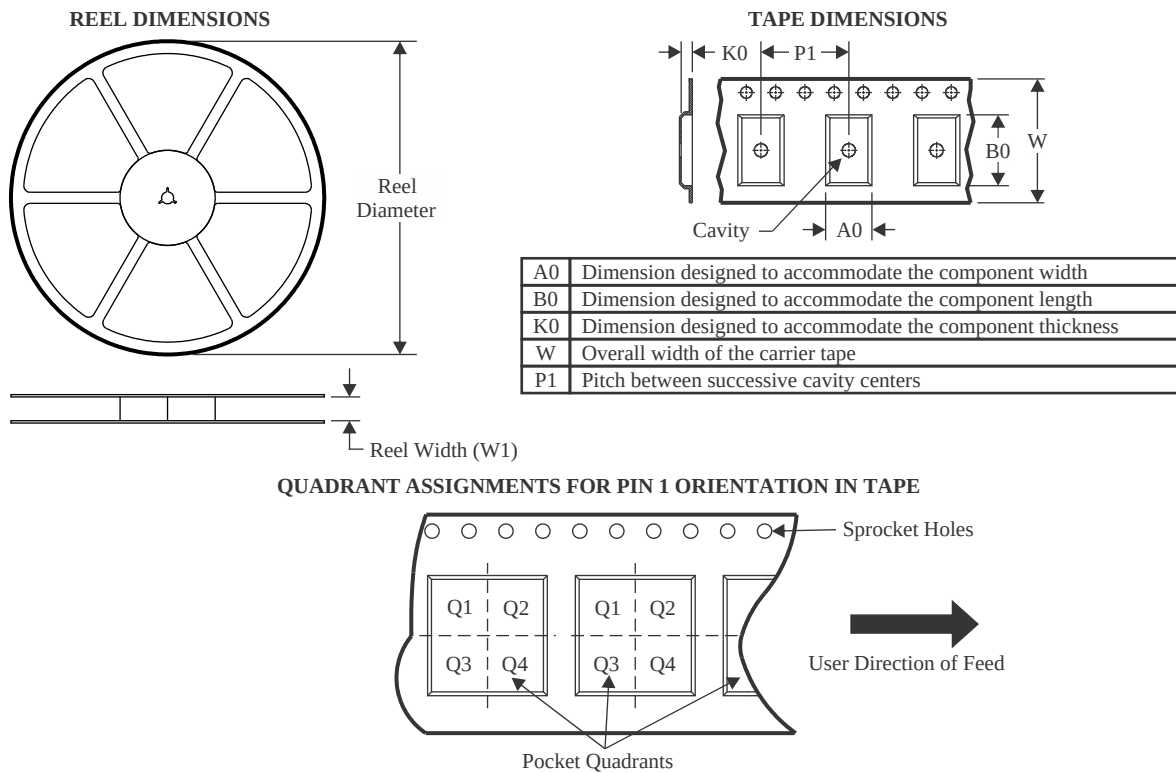
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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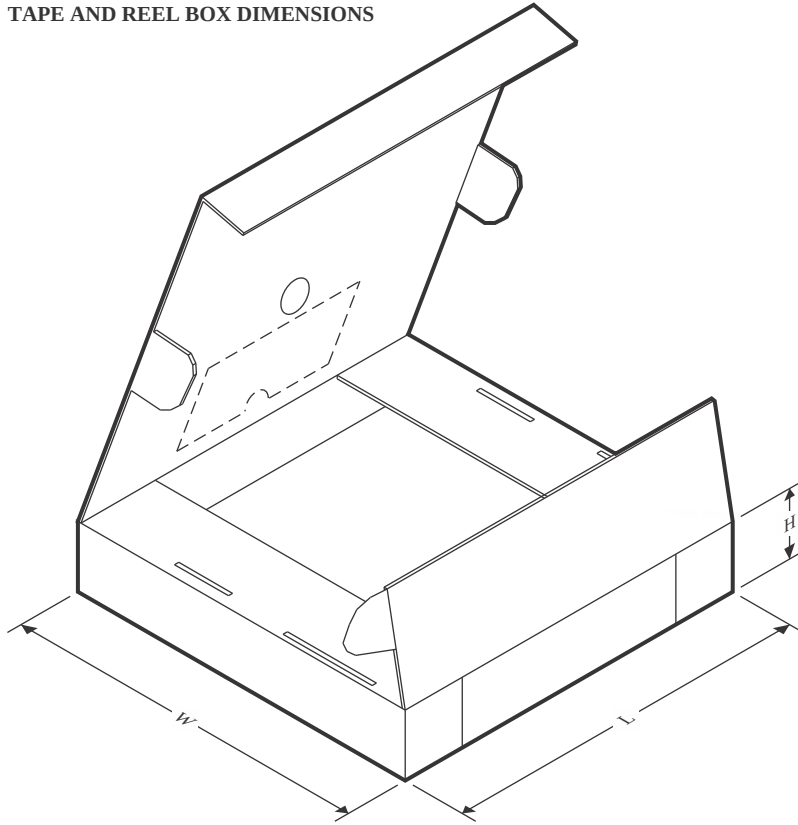
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA602AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

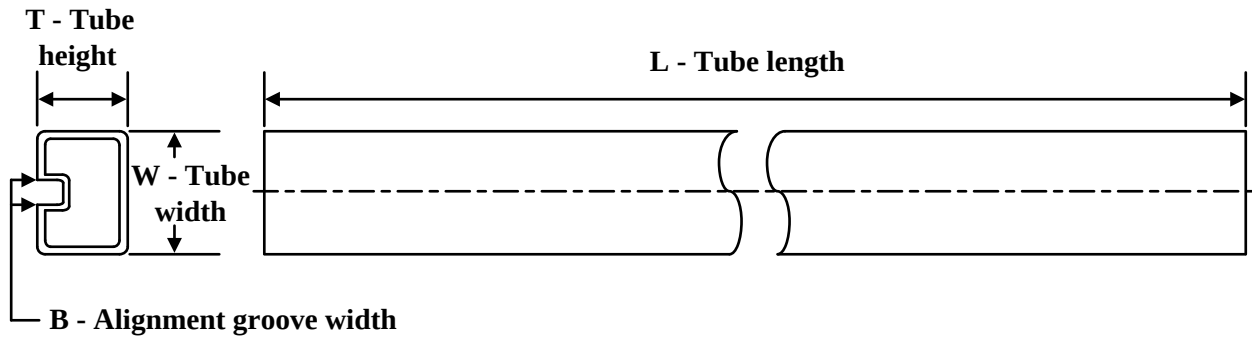
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA602AU/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA602AU	D	SOIC	8	75	506.6	8	3940	4.32
OPA602AU.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA602AUE4	D	SOIC	8	75	506.6	8	3940	4.32

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