TPS65987DDK USB Type-C® and USB PD Controller with Integrated Power Switches For USB4 and Thunderbolt 4 Devices

1 Features

- This device is certified by the USB-IF for PD3.0
  - PD3.0 silicon is required for certification of new USB PD designs
    - TID#: 5431
  - Article on PD2.0 vs. PD3.0
- TPS65987DDK is a USB4 and Thunderbolt 4 (TBT4) Device PD3.0 controller
  - This PD controller is only intended for use in USB4 device designs
  - Refer to Intel Reference Design document number 631605
  - If designing something other than a USB4 device, please refer to selection guide and getting started information at www.ti.com/usb-c and E2E guide
- Integrated fully managed power paths:
  - Integrated two 5-20 V, 5-A, 25-mΩ bidirectional switches
  - UL2367 cert #: 20190107-E169910
  - IEC62368-1 cert #: US-34617-UL
- Integrated robust power path protection
  - Integrated reverse current protection, undervoltage protection, overvoltage protection, and slew rate control for both 20-V/5-A power paths when configured to Sink
  - Integrated undervoltage protection, overvoltage protection, and current limiting for inrush current protection for both 20-V/5-A power paths when configured to Source
- USB Type-C® Power Delivery (PD) controller
  - 13 configurable GPIOs
  - USB PD 3.0 certified
  - USB Type-C specification certified
  - Cable attach and orientation detection
  - Integrated VCONN switch
  - Physical layer and policy engine
  - 3.3-V LDO output for dead battery support
  - Power supply from 3.3 V or VBUS source
  - 1 I2C primary or secondary port
  - 1 I2C primary only port
  - 1 I2C secondary only port

2 Applications

- Docking systems
- Monitors
- USB4 hubs

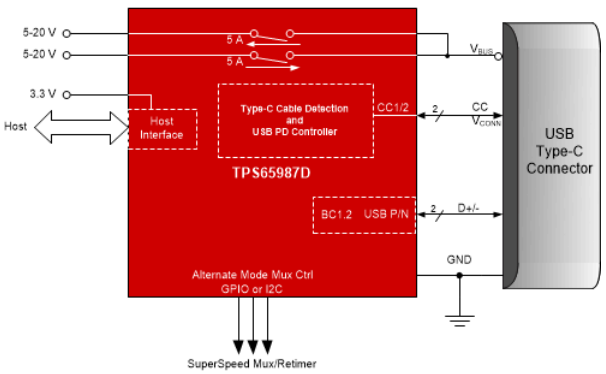
3 Description

The TPS65987DDK is a highly integrated stand-alone USB Type-C and Power Delivery (PD) controller optimized for USB4 & TBT4 Device. The TPS65987DDK integrates fully managed power paths with robust protection for a complete USB-C PD solution. The TPS65987DDK is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection for a single USB Type-C connector. Upon cable detection, the TPS65987DDK communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65987DDK enables the appropriate power path and configures alternate mode settings for external multiplexers. This device is featured on Intel's Reference Design for USB4 & TBT4 Device end equipments ensuring the PD controller has proper system level interaction in these types of designs. This greatly reduces system design complexity and results in reduced time to market.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS65987DDK	QFN (56)	7.00 mm x 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

Changes from Revision * (September 2020) to Revision A (August 2021)	Page
• Updated the *Features* list	1
• Updated the document title	1
• Globally changed instances of legacy terminology to controller and peripheral where SPI is mentioned	1
• Updated the *Description* section	1

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5 Pin Configuration and Functions

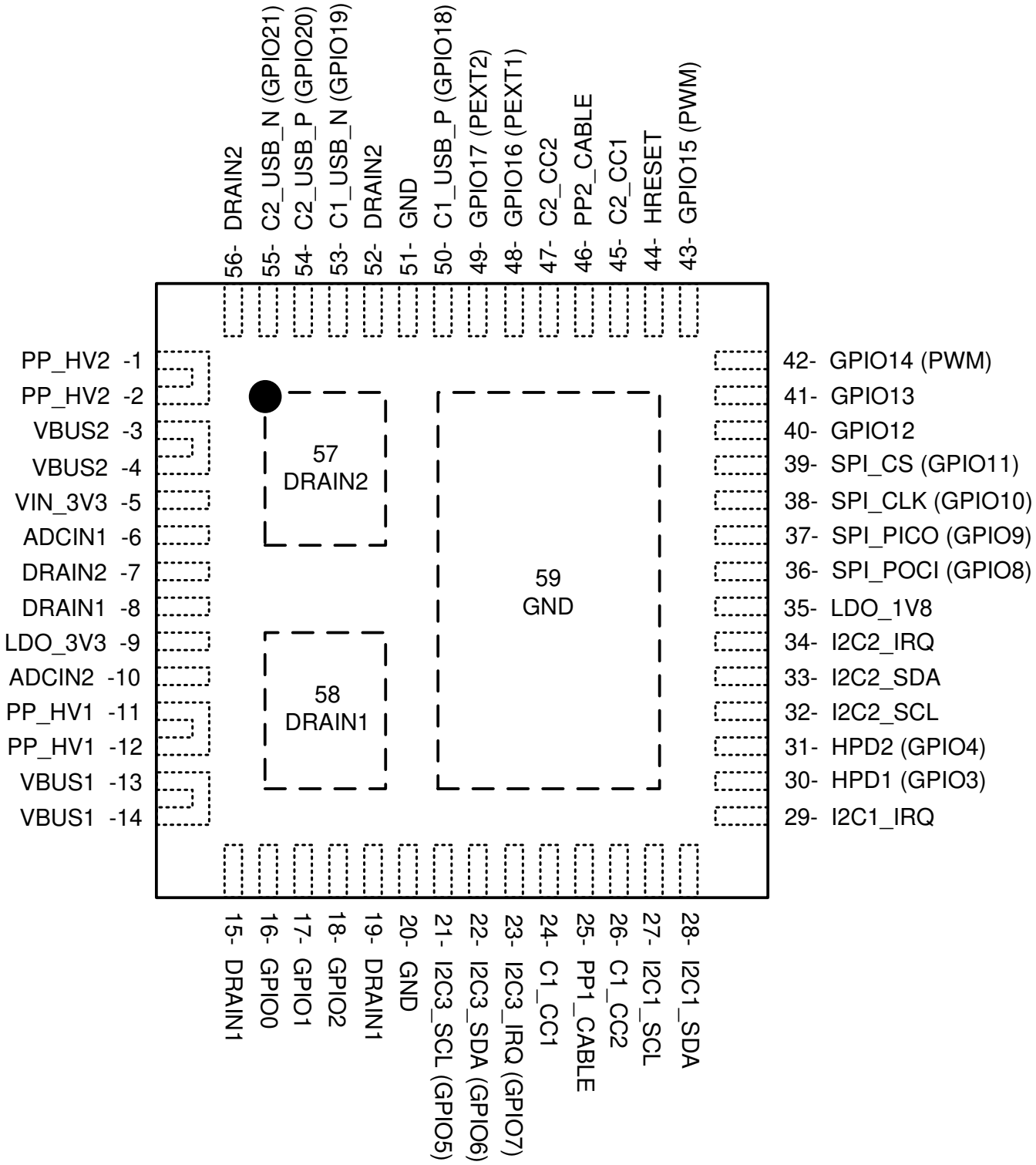

Figure 5-1. RSH Package 56-Pin QFN Top View

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Table 5-1. Pin Functions

PIN		TYPE[2]	RESET STATE[1]	DESCRIPTION
NAME	NO.			
ADCIN1	6	I	Input	Boot configuration Input. Connect to resistor divider between LDO_3V3 and GND.
ADCIN2	10	I	Input	I2C address configuration Input. Connect to resistor divider between LDO_3V3 and GND.
C_CC1	24	I/O	High-Z	Output to Type-C CC or VCONN pin . Filter noise with capacitor to GND.
C_CC2	26	I/O	High-Z	Output to Type-C CC or VCONN pin . Filter noise with capacitor to GND.
C_USB_N (GPIO19)	53	I/O	Input (High-Z)	USB D– connection for BC1.2 support.
C_USB_P (GPIO18)	50	I/O	Input (High-Z)	USB D+ connection for BC1.2 support.
DRAIN1	8, 15, 19, 58	—	—	Drain of internal power path 1. Connect thermal pad 58 to as big of pad as possible on PCB for best thermal performance. Short the other pins to this thermal pad.
DRAIN2	7, 52, 56, 57	—	—	Drain of internal power path 2. Connect thermal pad 57 to as big of pad as possible on PCB for best thermal performance. Short the other pins to this thermal pad.
GND	20, 45 , 46, 47, 51	—	—	Unused pin. Tie to GND.
GPIO0	16	I/O	Input (High-Z)	General Purpose Digital I/O 0. Float pin when unused. GPIO0 is asserted low during the TPS65987DDK boot process. Once device configuration and patches are loaded GPIO0 is released.
GPIO1	17	I/O	Input (High-Z)	General Purpose Digital I/O 1. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO2	18	I/O	Input (High-Z)	General Purpose Digital I/O 2. Float pin when unused.
GPIO3 (HPD)	30	I/O	Input (High-Z)	General Purpose Digital I/O 3. Configured as Hot Plug Detect (HPD) TX and RX when DisplayPort alternate mode is enabled. Float pin when unused.
GPIO4	31	I/O	Input (High-Z)	General Purpose Digital I/O 4. Float pin when unused.
I2C3_SCL (GPIO5)	21	I/O	Input (High-Z)	I2C port 3 serial clock. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used. Float pin when unused.
I2C3_SDA (GPIO6)	22	I/O	Input (High-Z)	I2C port 3 serial data. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used. Float pin when unused.
$\overline{\text{I2C3_IRQ}}$ (GPIO7)	23	I/O	Input (High-Z)	I2C port 3 interrupt detection (port 3 operates as an I2C Master Only). Active low detection. Connect to the I2C slave's interrupt line to detect when the slave issues an interrupt. Float pin when unused.
GPIO12	40	I/O	Input (High-Z)	General Purpose Digital I/O 12. Float pin when unused.
GPIO13	41	I/O	Input (High-Z)	General Purpose Digital I/O 13. Float pin when unused.
GPIO14 (PWM)	42	I/O	Input (High-Z)	General Purpose Digital I/O 14. May also function as a PWM output. Float pin when unused.
GPIO15 (PWM)	43	I/O	Input (High-Z)	General Purpose Digital I/O 15. May also function as a PWM output. Float pin when unused.

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Table 5-1. Pin Functions (continued)

PIN		TYPE[2]	RESET STATE[1]	DESCRIPTION
NAME	NO.			
GPIO16 (PP_EXT1)	48	I/O	Input (High-Z)	General Purpose Digital I/O 16. May also function as single wire enable signal for external power path 1. Pull-down with external resistor when used for external path control. Float pin when unused.
GPIO17 (PP_EXT2)	49	I/O	Input (High-Z)	General Purpose Digital I/O 17. May also function as single wire enable signal for external power path 2. Pull-down with external resistor when used for external path control. Float pin when unused.
GPIO20	54	I/O	Input (High-Z)	General Purpose Digital I/O 20. Float pin when unused.
GPIO21	55	I/O	Input (High-Z)	General Purpose Digital I/O 21. Float pin when unused.
HRESET	44	I/O	Input	Active high hardware reset input. Will reinitialize all device settings. Ground pin when HRESET functionality will not be used.
$\overline{\text{I2C1_IRQ}}$	29	O	High-Z	I2C port 1 interrupt. Active low. Implement externally as an open drain with a pull-up resistance. Float pin when unused.
I2C1_SCL	27	I/O	High-Z	I2C port 1 serial clock. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used or unused.
I2C1_SDA	28	I/O	High-Z	I2C port 1 serial data. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used or unused.
$\overline{\text{I2C2_IRQ}}$	34	O	High-Z	I2C port 2 interrupt. Active low. Implement externally as an open drain with a pull-up resistance. Float pin when unused.
I2C2_SCL	32	I/O	High-Z	I2C port 2 serial clock. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used or unused.
I2C2_SDA	33	I/O	High-Z	I2C port 2 serial data. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used or unused.
LDO_1V8	35	PWR	—	Output of the 1.8-V LDO for internal circuitry. Bypass with capacitor to GND
LDO_3V3	9	PWR	—	Output of the VBUS to 3.3-V LDO or connected to VIN_3V3 by a switch. Main internal supply rail. Used to power external flash memory. Bypass with capacitor to GND.
PP_CABLE	25	PWR	—	5-V supply input for port 1 C_CC pins. Bypass with capacitor to GND.
PP_HV1	11, 12	PWR	—	System side of first VBUS power switch. Bypass with capacitor to ground. Tie to ground when unused.
PP_HV2	1, 2	PWR	—	System side of second VBUS power switch. Bypass with capacitor to ground. Tie to ground when unused.
SPI_CLK	38	I/O	Input	SPI serial clock. Ground pin when unused.
SPI_POCI	36	I/O	Input	SPI serial controller input from peripheral. Ground pin when unused.
SPI_PICO	37	I/O	Input	SPI serial controller output to peripheral. Ground pin when unused.
$\overline{\text{SPI_CS}}$	39	I/O	Input	SPI chip select. Ground pin when unused.
VBUS1	13, 14	PWR	—	Port side of first VBUS power switch. Bypass with capacitor to ground. Tie to VBUS2.

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Table 5-1. Pin Functions (continued)

PIN		TYPE[2]	RESET STATE[1]	DESCRIPTION
NAME	NO.			
VBUS2	3, 4	PWR	—	Port side of second VBUS power switch. Bypass with capacitor to ground. Tie to VBUS1.
VIN_3V3	5	PWR	—	Supply for core circuitry and I/O. Bypass with capacitor to GND.
Thermal Pad (PPAD)	59	GND	—	Ground reference for the device as well as thermal pad used to conduct heat. from the device. This connection serves two purposes. The first purpose is to provide an electrical ground connection for the device. The second purpose is to provide a low thermal-impedance path from the device die to the PCB. This pad must be connected to a ground plane.

(1) Reset State indicates the state of a given pin immediately following power application, prior to any configuration from firmware.
(2) I = input, O = output, I/O = bidirectional, GND = ground, PWR = power, NC = no connect.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage(2)	PP_CABLE	–0.3	6	V
	VIN_3V3	–0.3	3.6	
Output voltage(2)	LDO_1V8	–0.3	2	V
	LDO_3V3	–0.3	3.6	
	I2Cx _IRQ, SPI_PICO, SPI_CLK, SPI_CS, SWD_CLK	–0.3	LDO_3V3 + 0.3 (3)	
I/O voltage (2)	PP_HVx, VBUSx(4)	–0.3	24	V
	I2Cx_SDA, I2Cx_SCL, SPI_POCI, GPIOn, HRESET, ADCINx	–0.3	LDO_3V3 + 0.3 (3)	
	C_USB_P, C_USB_N	–0.5	6	
	C_CC1, C_CC2	–0.5	6	
Operating junction temperature, T_J		–10	125	°C
Operating junction temperature PPHV switch, T_J		–10	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to underside power pad. The underside power pad should be directly connected to the ground plane of the board.
(3) Not to exceed 3.6 V.
(4) For VBUSx a TVS with a break down voltage falling between the Recommended max and the Abs max value is recommended such as TVS2200.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input voltage, V_I (1)	VIN_3V3	3.135		3.45	V
	PP_CABLE	2.95		5.5	
	PP_HV	4.5		22	
I/O voltage, V_{IO} (1)	VBUS	4		22	V
	C_USB_P, C_USB_N	0		LDO_3V3	
	C_CC1, C_CC2	0		5.5	
	GPIOn, I2Cx_SDA, I2Cx_SCL, SPI, ADCIN1, ADCIN2	0		LDO_3V3	
Operating ambient temperature, T_A		–10		75	°C
Operating junction temperature, T_J		–10		125	

(1) All voltage values are with respect to underside power pad. Underside power pad must be directly connected to ground plane of the board.

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6.4 Thermal Information

THERMAL METRIC[1]		TPS65987DDK RSH (QFN) 56 PINS	UNIT
$R_{\theta JA}$ [2]	Junction-to-ambient thermal resistance	57.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.4	°C/W
$R_{\theta JB}$ [2]	Junction-to-board thermal resistance	30	°C/W
ψ_{JT} [2]	Junction-to-top characterization parameter	34.1	°C/W
ψ_{JB} [2]	Junction-to-board characterization parameter	29.9	°C/W
$R_{\theta JC(bot_Controller)}$	Junction-to-case (bottom GND pad) thermal resistance	0.7	°C/W
$R_{\theta JC(bot_FET)}$	Junction-to-case (bottom DRAIN 1/2 pad) thermal resistance	5.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Thermal metrics are not JDEC standard values and are based on the TPS65988 evaluation board.

6.5 Power Supply Requirements and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL						
V_{IN_3V3}	Input 3.3-V supply		3.135	3.3	3.45	V
PP_CABLE	Input to power Vconn output on C_CC pins		2.95	5	5.5	V
PP_HV	Source power from PP_HV to VBUS		4.5	5	22	V
VBUS	Sink power from VBUS to PP_HV		4	5	22	V
C_{VIN_3V3}	Recommended capacitance on the VIN_3V3 pin		5	10		µF
C_{PP_CABLE}	Recommended capacitance on PPx_CABLE pins		2.5	4.7		µF
$C_{PP_HV_SRC}$	Recommended capacitance on PP_HVx pin when configured as a source		2.5	4.7		µF
$C_{PP_HV_SNK}$	Recommended capacitance on PP_HVx pin when configured as a sink		1	47	120	µF
C_{VBUS}	Recommended capacitance on VBUSx pins		0.5	1	12	µF
INTERNAL						
V_{LDO_3V3}	Output voltage of LDO from VBUS to LDO_3V3	VIN_3V3 = 0 V, VBUS1 ≥ 4 V, 0 ≤ I_{LOAD} ≤ 50 mA	3.15	3.3	3.45	V
$V_{DO_LDO_3V3}$	Drop out voltage of LDO_3V3 from VBUS	I_{LOAD} = 50 mA	250	500	850	mV
$I_{LDO_3V3_EX}$	Allowed External Load current on LDO_3V3 pin				25	mA
V_{LDO_1V8}	Output voltage of LDO_1V8	0 ≤ I_{LOAD} ≤ 20 mA	1.75	1.8	1.85	V
V_{FWD_DROP}	Forward voltage drop across VIN_3V3 to LDO_3V3 switch	I_{LOAD} = 50 mA			200	mV
C_{LDO_3V3}	Recommended capacitance on LDO_3V3 pin		5	10	25	µF
C_{LDO_1V8}	Recommended capacitance on LDO_1V8 pin		2.2	4.7	6	µF
SUPERVISORY						
UV_LDO3V3	Undervoltage threshold for LDO_3V3. Locks out 1.8-V LDOs.	LDO_3V3 rising	2.2	2.325	2.45	V

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6.5 Power Supply Requirements and Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVH_LDO3V3	Undervoltage hysteresis for LDO_3V3	LDO_3V3 falling	20	80	150	mV
UV_PCBL	Undervoltage threshold for PP_CABLE	PP_CABLE rising	2.5	2.625	2.75	V
UVH_PCBL	Undervoltage hysteresis for PP_PCABLE	PP_CABLE falling	20	50	80	mV
OV_VBUS	Overvoltage threshold for VBUS. This value is a 6-bit programmable threshold	VBUS rising	5		24	V
OVLSB_VBUS	Overvoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS rising		328		mV
OVH_VBUS	Overvoltage hysteresis for VBUS	VBUS falling, % of OV_VBUS	1.4	1.65	1.9	%
UV_VBUS	Undervoltage threshold for VBUS. This value is a 6-bit programmable threshold.	VBUS falling	2.5		18.21	V
UVLSB_VBUS	Undervoltage threshold step for VBUS. This value is the LSB of the programmable threshold.	VBUS falling		249		mV
UVH_VBUS	Undervoltage hysteresis for VBUS	VBUS rising, % of UV_VBUS	0.9	1.3	1.7	%

6.6 Power Consumption Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VIN_3V3} (1)	Sleep (Sink)	VIN_3V3 = 3.3 V, VBUS = 0 V, No cable connected, T_j = 25°C, configured as sink, BC1.2 disabled		45		µA
	Sleep (Source/DRP)	VIN_3V3 = 3.3 V, VBUS = 0 V, No cable connected, T_j = 25°C, configured as source or DRP, BC1.2 disabled		55		µA
I_{VIN_3V3} (1)	Idle (Attached)	VIN_3V3 = 3.3 V, Cable connected, No active PD communication, T_j = 25°C		5		mA
I_{VIN_3V3} (1)	Active	VIN_3V3 = 3.3 V, T_j = 25°C		8		mA

(1) Does not include current draw due to GPIO loading

6.7 Power Switch Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PPCC}	PP_CABLE to C_CCn power switch resistance	4.7 ≤ PP_CABLE ≤ 5.5		222	325	mΩ
		2.95 ≤ PP_CABLE < 4.7		269	414	mΩ
R_{PPHV}	PP_HVx to VBUSx power switch resistance	Tj = 25°C		25	33	mΩ
I_{PPHV}	Continuous current capabillity of power path from PP_HVx to VBUSx				5	A
I_{PPCC}	Continuous current capabillity of power path from PP_CABLE to C_CCn	T_J = 125°C			320	mA
		T_J = 85°C			600	mA
I_{HVACT}	Active quiescent current from PP_HV pin, EN_HV = 1	Source Configuration, Comparator RCP function enabled, I_{LOAD} = 100 mA			1	mA
I_{HVSD}	Shutdown quiescent current from PP_HV pin, EN_HV = 0	V_{PPHV} = 20 V			100	µA

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6.7 Power Switch Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCC}	Over Current Clamp Firmware Selectable Settings		1.140	1.267	1.393	A
			1.380	1.533	1.687	A
			1.620	1.800	1.980	A
			1.860	2.067	2.273	A
			2.100	2.333	2.567	A
			2.34	2.600	2.860	A
			2.580	2.867	3.153	A
			2.820	3.133	3.447	A
			3.060	3.400	3.74	A
			3.300	3.667	4.033	A
			3.540	3.933	4.327	A
			3.780	4.200	4.620	A
			4.020	4.467	4.913	A
			4.260	4.733	5.207	A
			4.500	5.00	5.500	A
			4.740	5.267	5.793	A
			4.980	5.533	6.087	A
			5.220	5.800	6.380	A
			5.460	6.067	6.673	A
			5.697	6.330	6.963	A
I_{OCP}	PP_HV Quick Response Current Limit			10		A
$I_{LIMPPCC}$	PP_CABLE current limit		0.6	0.75	0.9	A
$I_{HV_ACC\ 1}$	PP_HV current sense accuracy	I = 100 mA, Reverse current blocking disabled	3.9	6	8.1	A/V
$I_{HV_ACC\ 1}$	PP_HV current sense accuracy	I = 200 mA	4.8	6	7.2	A/V
$I_{HV_ACC\ 1}$	PP_HV current sense accuracy	I = 500 mA	5.28	6	6.72	A/V
$I_{HV_ACC\ 1}$	PP_HV current sense accuracy	I ≥ 1 A	5.4	6	6.6	A/V
t_{ON_HV}	PP_HV path turn on time from enable to VBUS = 95% of PP_HV voltage	Configured as a source or as a sink with soft start disabled. PP_HV = 20 V, CVBUS = 10 µF, I_{LOAD} = 100 mA			8	ms
t_{ON_FRS}	PP_HV path turn on time from enable to VBUS = 95% of PP_HV voltage during an FRS enable	Configured as a source. PP_HV = 5 V, CVBUS = 10 µF, I_{LOAD} = 100 mA			150	µs
t_{ON_CC}	PP_CABLE path turn on time from enable to C_CCn = 95% of the PP_CABLE voltage	PP_CABLE = 5 V, C_CCn = 500 nF, I_{LOAD} = 100 mA			2	ms
SS	Configurable soft start slew rate for sink configuration	I_{LOAD} = 100 mA, setting 0	0.270	0.409	0.45	V/ms
		I_{LOAD} = 100 mA, setting 1	0.6	0.787	1	V/ms
		I_{LOAD} = 100 mA, setting 2	1.2	1.567	1.7	V/ms
		I_{LOAD} = 100 mA, setting 3	2.3	3.388	3.6	V/ms
V_{REVPHV}	Reverse current blocking voltage threshold for PP_HV switch	Diode Mode		6	10	mV
		Comparator Mode		3	6	mV
V_{SAFE0V}	Voltage that is a safe 0 V per USB-PD specification		0		0.8	V
t_{SAFE0V}	Voltage transition time to VSAFE0V				650	ms

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6.7 Power Switch Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SRPOS	Maximum slew rate for positive voltage transitions				0.03	V/µs
SRNEG	Maximum slew rate for negative voltage transitions		–0.03			V/µs
t_{STABLE}	EN to stable time for both positive and negative voltage transitions				275	ms
$V_{SRCVALID}$	Supply output tolerance beyond V_{SRCNEW} during time t_{STABLE}		–0.5		0.5	V
V_{SRCNEW}	Supply output tolerance		–5		5	%
$t_{VCONNDIS}$	Time from cable detach to VVCONNDIS				250	ms
$V_{VCONNDIS}$	Voltage at which V_{CONN} is considered discharged				150	mV

6.8 Cable Detection Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{H_CC_USB}$	Source Current through each C_CC pin when in a disconnected state and Configured as a Source advertising Default USB current to a peripheral device		73.6	80	86.4	µA
$I_{H_CC_1P5}$	Source Current through each C_CC pin when in a disconnected state when Configured as a Source advertising 1.5-A to a UFP		165.6	180	194.4	µA
$I_{H_CC_3P0}$	Source Current through each C_CC pin when in a disconnected state and Configured as a Source advertising 3.0-A to a UFP.	VIN_3V3 ≥ 3.135 V, V_{CC} < 2.6 V	303.6	330	356.4	µA
$V_{D_CCH_USB}$	Voltage Threshold for detecting a Source attach when configured as a Sink and the Source is advertising Default USB current source capability		0.15	0.2	0.25	V
$V_{D_CCH_1P5}$	Voltage Threshold for detecting a Source advertising 1.5-A source capability when configured as a Sink		0.61	0.66	0.7	V
$V_{D_CCH_3P0}$	Voltage Threshold for detecting a Source advertising 3-A source capability when configured as a Sink		1.16	1.23	1.31	V
$V_{H_CCD_USB}$	Voltage Threshold for detecting a Sink attach when configured as a Source and advertising Default USB current source capability.	IH_CC = IH_CC_USB	1.5	1.55	1.65	V
$V_{H_CCD_1P5}$	Voltage Threshold for detecting a Sink attach when configured as a Source and advertising 1.5-A source capability	IH_CC = IH_CC_1P5	1.5	1.55	1.65	V
$V_{H_CCD_3P0}$	Voltage Threshold for detecting a Sink attach when configured as a Source and advertising 3.0-A source capability.	IH_CC = IH_CC_3P0 VIN_3V3 ≥ 3.135 V	2.45	2.55	2.615	V
$V_{H_CCA_USB}$	Voltage Threshold for detecting an active cable attach when configured as a Source and advertising Default USB current capability.		0.15	0.2	0.25	V
$V_{H_CCA_1P5}$	Voltage Threshold for detecting active cables attach when configured as a Source and advertising 1.5-A capability.		0.35	0.4	0.45	V

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6.8 Cable Detection Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{H_CCA_3P0}$	Voltage Threshold for detecting active cables attach when configured as a Source and advertising 3-A capability.		0.75	0.8	0.85	V
R_{D_CC}	Pulldown resistance through each C_CC pin when in a disconnect state and configured as a Sink. LDO_3V3 powered.	V = 1 V, 1.5 V	4.59	5.1	5.61	kΩ
$R_{D_CC_OPEN}$	Pulldown resistance through each C_CC pin when in a disabled state. LDO_3V3 powered.	V = 0 V to LDO_3V3	500			kΩ
R_{D_DB}	Pulldown resistance through each C_CC pin when LDO_3V3 unpowered	V = 1.5 V, 2.0 V	4.08	5.1	6.12	kΩ
R_{FRSWAP}	Fast Role Swap signal pull down				5	Ω
V_{TH_FRS}	Fast role swap request detection voltage threshold		490	520	550	mV

6.9 USB-PD Baseband Signal Requirements and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON						
PD_BITRATE	PD data bit rate		270	300	330	Kbps
UI (2)	Unit interval (1/PD_BITRATE)		3.03	3.33	3.7	µs
CCBLPLUG (1)	Capacitance for a cable plug (each plug on a cable may have up to this value)				25	pF
ZCABLE	Cable characteristic impedance		32		65	Ω
CRECEIVER (3)	Receiver capacitance. Capacitance looking into C_CCn pin when in receiver mode.			100		pF
TRANSMITTER						
ZDRIVER	TX output impedance. Source output impedance at the Nyquist frequency of USB2.0 low speed (750kHz) while the source is driving the C_CCn line.		33		75	Ω
t_{RISE}	Rise time. 10 % to 90 % amplitude points, minimum is under an unloaded condition. Maximum set by TX mask.		300			ns
t_{FALL}	Fall time. 90 % to 10 % amplitude points, minimum is under an unloaded condition. Maximum set by TX mask.		300			ns
V_{TX}	Transmit high voltage		1.05	1.125	1.2	V
RECEIVER						
V_{RXTR}	Rx receive rising input threshold	Port configured as Source	840	875	910	mV
V_{RXTR}	Rx receive rising input threshold	Port configured as Sink	504	525	546	mV
V_{RXTF}	Rx receive falling input threshold	Port configured as Sink	240	250	260	mV
V_{RXTF}	Rx receive falling input threshold	Port configured as Source	576	600	624	mV
NCOUNT	Number of transitions for signal detection (number to count to detect non-idle bus).		3			

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6.9 USB-PD Baseband Signal Requirements and Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TTRANWIN	Time window for detecting non-idle bus.		12		20	µs
ZBMCRX	Receiver input impedance	Does not include pull-up or pulldown resistance from cable detect. Transmitter is Hi-Z.	5			MΩ
TRXFILTER (4)	Rx bandwidth limiting filter. Time constant of a single pole filter to limit broadband noise ingression		100			ns

(1) The capacitance of the bulk cable is not included in the CCBLPLUG definition. It is modeled as a transmission line.
(2) UI denotes the time to transmit an unencoded data bit not the shortest high or low times on the wire after encoding with BMC. A single data bit cell has duration of 1 UI, but a data bit cell with value 1 will contain a centrally place 01 or 10 transition in addition to the transition at the start of the cell.
(3) CRECEIVER includes only the internal capacitance on a C_CCn pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications. TI recommends adding capacitance to bring the total pin capacitance to 300 pF for improved TX behavior.
(4) Broadband noise ingression is because of coupling in the cable interconnect.

6.10 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_MAIN}	Thermal Shutdown Temperature of the main thermal shutdown	Temperature rising	145	160	175	°C
T_{SDH_MAIN}	Thermal Shutdown hysteresis of the main thermal shutdown	Temperature falling		20		°C
T_{SD_PWR}	Thermal Shutdown Temperature of the power path block	Temperature rising	145	160	175	°C
T_{SDH_PWR}	Thermal Shutdown hysteresis of the power path block	Temperature falling		20		°C

6.11 Oscillator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC_24M}	24-MHz oscillator		22.8	24	25.2	MHz
f_{OSC_100K}	100-kHz oscillator		95	100	105	kHz

6.12 I/O Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
SPI_VIH	High-level input voltage	LDO_1V8 = 1.8 V	1.3			V
SPI_VIL	Low input voltage	LDO_1V8 = 1.8 V			0.63	V
SPI_HYS	Input hysteresis voltage	LDO_1V8 = 1.8 V	0.09			V
SPI_ILKG	Leakage current	Output is Hi-Z, VIN = 0 to LDO_3V3	-1		1	µA
SPI_VOH	SPI output high voltage	IO = –2 mA, LDO_3V3 = 3.3 V	2.88			V
SPI_VOL	SPI output low voltage	IO = 2 mA			0.4	V
SWDIO						
SWDCLK						
GPIO						
GPIO_VIH	High-level input voltage	LDO_1V8 = 1.8 V	1.3			V

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6.12 I/O Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO_VIL	Low input voltage	LDO_1V8 = 1.8 V			0.63	V
GPIO_HYS	Input hysteresis voltage	LDO_1V8 = 1.8 V	0.09			V
GPIO_ILKG	I/O leakage current	INPUT = 0 V to VDD	–1		1	µA
GPIO_RPU	Pullup resistance	Pullup enabled	50	100	150	kΩ
GPIO_RPD	Pulldown resistance	Pulldown enabled	50	100	150	kΩ
GPIO_DG	Digital input path deglitch			20		ns
GPIO_VOH	GPIO output high voltage	IO = –2 mA, LDO_3V3 = 3.3 V	2.88			V
GPIO_VOL	GPIO output low voltage	IO = 2 mA, LDO_3V3 = 3.3 V			0.4	V
I2C_IRQx						
OD_VOL	Low-level output voltage	I_{OL} = 2 mA			0.4	V
OD_LKG	Leakage current	Output is Hi-Z, VIN = 0 to LDO_3V3	–1		1	µA

6.13 I²C Requirements and Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA AND SCL COMMON CHARACTERISTICS						
I_{LEAK}	Input leakage current	Voltage on Pin = LDO_3V3	–3		3	µA
V_{OL}	SDA output low voltage	I_{OL} = 3 mA, LDO_3V3 = 3.3 V			0.4	V
I_{OL}	SDA max output low current	V_{OL} = 0.4 V	3			mA
		V_{OL} = 0.6 V	6			mA
V_{IL}	Input low signal	LDO_3V3 = 3.3 V			0.99	V
		LDO_1V8 = 1.8 V			0.54	V
V_{IH}	Input high signal	LDO_3V3 = 3.3 V	2.31			V
		LDO_1V8 = 1.8 V	1.3			V
V_{HYS}	Input hysteresis	LDO_3V3 = 3.3 V	0.17			V
		LDO_1V8 = 1.8 V	0.09			V
t_{SP}	I²C pulse width suppressed				50	ns
C_I	Pin capacitance				10	pF
SDA AND SCL STANDARD MODE CHARACTERISTICS						
f_{SCL}	I²C clock frequency		0		100	kHz
t_{HIGH}	I²C clock high time		4			µs
t_{LOW}	I²C clock low time		4.7			µs
$t_{SU;DAT}$	I²C serial data setup time		250			ns
$t_{HD;DAT}$	I²C serial data hold time		0			ns
$t_{VD;DAT}$	I²C valid data time	SCL low to SDA output valid			3.45	µs
$t_{VD;ACK}$	I²C valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			3.45	µs
t_{OCF}	I²C output fall time	10-pF to 400-pF bus			250	ns
t_{BUF}	I²C bus free time between stop and start		4.7			µs
$t_{SU;STA}$	I²C start or repeated Start condition setup time		4.7			µs
$t_{HD;STA}$	I²C Start or repeated Start condition hold time		4			µs

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6.13 I²C Requirements and Characteristics (continued)

over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SU;STO}$	I²C Stop condition setup time		4			µs
SDA AND SCL FAST MODE CHARACTERISTICS						
f_{SCL}	I²C clock frequency	Configured as Slave	0		400	kHz
f_{SCL_MASTER}	I²C clock frequency	Configured as Master	0	320	400	kHz
t_{HIGH}	I²C clock high time		0.6			µs
t_{LOW}	I²C clock low time		1.3			µs
$t_{SU;DAT}$	I²C serial data setup time		100			ns
$t_{HD;DAT}$	I²C serial data hold time		0			ns
$t_{VD;DAT}$	I²C Valid data time	SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	I²C Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			0.9	µs
t_{OCF}	I²C output fall time	10-pF to 40-pF bus, V_{DD} = 3.3 V	12		250	ns
		10-pF to 400-pF bus, V_{DD} = 1.8 V	6.5		250	ns
t_{BUF}	I²C bus free time between stop and start		1.3			µs
$t_{SU;STA}$	I²C start or repeated Start condition setup time		0.6			µs
$t_{HD;STA}$	I²C Start or repeated Start condition hold time		0.6			µs
$t_{SU;STO}$	I²C Stop condition setup time		0.6			µs

6.14 SPI Controller Timing Requirements

			MIN	NOM	MAX	UNIT
f_{SPI}	Frequency of SPI_CLK		11.4	12	12.6	MHz
t_{PER}	Period of SPI_CLK (1/F_SPI)		79.36	83.33	87.72	ns
t_{WHI}	SPI_CLK high width		30			ns
t_{WLO}	SPI_CLK low width		30			ns
t_{DACT}	SPI_SZZ falling to SPI_CLK rising delay time		30		50	ns
t_{DINACT}	SPI_CLK falling to SPI_SSZ rising delay time		158		180	ns
t_{DPICO}	SPI_CLK falling to SPI_PICO Valid delay time		–10		10	ns
t_{SUPOCI}	SPI_POCI valid to SPI_CLK falling setup time		33			ns
t_{HDMSIO}	SPI_CLK falling to SPI_POCI invalid hold time		0			ns
t_{RIN}	SPI_POCI input rise time				5	ns
t_{RSPI}	SPI_SSZ/CLK/PICO rise time	10% to 90%, C_L = 5 to 50 pF, LDO_3V3 = 3.3 V	1		25	ns
t_{FSPI}	SPI_SSZ/CLK/PICO fall time	90% to 10%, C_L = 5 to 50 pF, LDO_3V3 = 3.3 V	1		25	ns

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6.15 HPD Timing Requirements

			MIN	NOM	MAX	UNIT
DP SOURCE SIDE (HPD TX)						
t_{IRQ_MIN}	HPD IRQ minimum assert time		675	750	825	µs
$t_{2\ MS_MIN}$	HPD assert 2-ms min time		3	3.33	3.67	ms
DP SINK SIDE (HPD RX)						
t_{HPD_HDB}	HPD high debounce time	HPD_HDB_SEL = 0	300	375	450	µs
		HPD_HDB_SEL = 1	100	111	122	ms
t_{HPD_LDB}	HPD low debounce time		300	375	450	µs
t_{HPD_IRQ}	HPD IRQ limit time		1.35	1.5	1.65	ms

6.16 Typical Characteristics

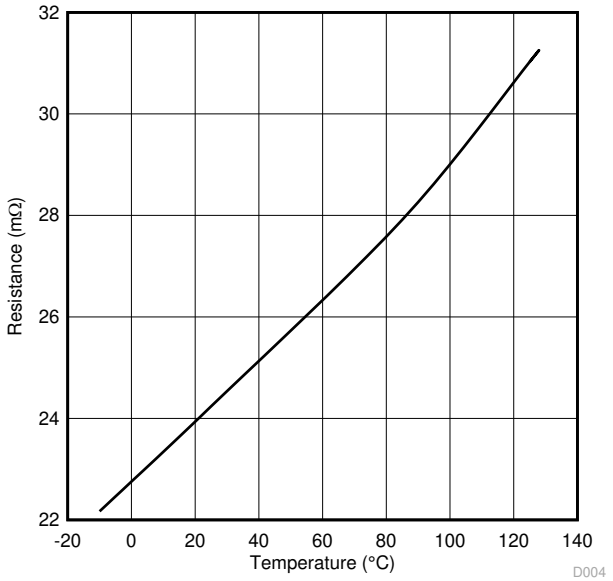

Figure 6-1. PPHVx Rdson vs Junction Temperature

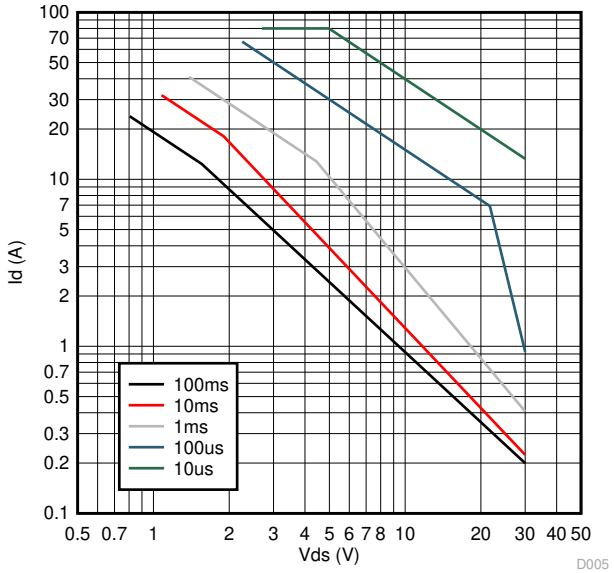

Figure 6-2. PPHVx SOA Curve

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7 Parameter Measurement Information

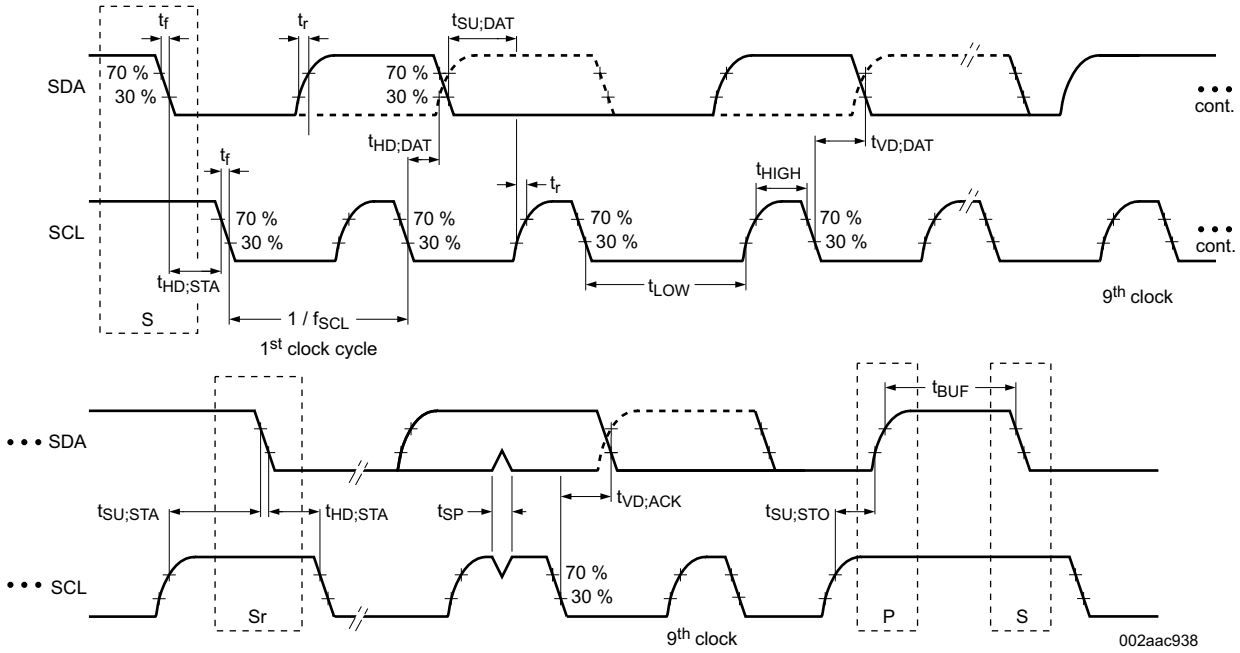

Figure 7-1. I²C Slave Interface Timing

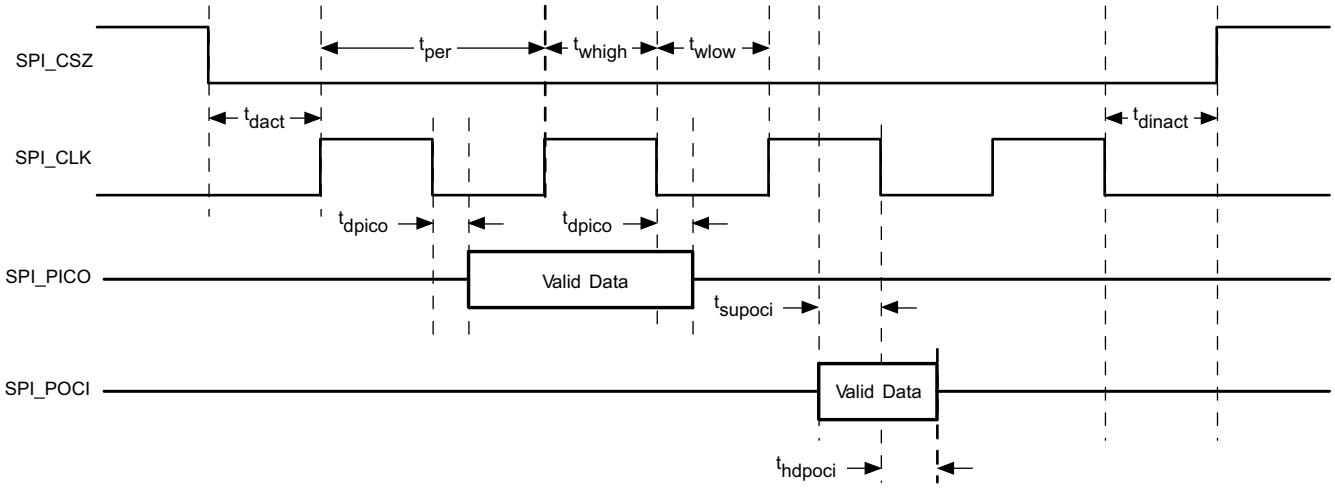

Figure 7-2. SPI Controller Timing

8 Detailed Description

8.1 Overview

The TPS65987DDK is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for a USB Type-C and PD plug or receptacles. The TPS65987DDK communicates with the cable and another USB Type-C and PD device at the opposite end of the cable, enables integrated port power switch, controls an external high current port power switch and negotiates alternate modes . The TPS65987DDK may also control an attached super-speed multiplexer via GPIO or I^2C to simultaneously support USB3.0/3.1 data rates and DisplayPort video.

The TPS65987DDK is divided into five main sections:

- USB-PD controller
- cable plug and orientation detection circuitry
- port power switches
- power management circuitry
- digital core

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the C_CC1 pin or the C_CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of its features and more detailed circuitry, see the *USB-PD Physical Layer* section.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and also automatically detects the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of its features and more detailed circuitry, see *Port Power Switches*.

The port power switches provide power to the system port through the VBUS pin and also through the C_CC1 or C_CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of its features and more detailed circuitry, see the *Port Power Switches* section.

The power management circuitry receives and provides power to the TPS65987DDK internal circuitry and to the LDO_3V3 output. For a high-level block diagram of the power management circuitry, a description of its features and more detailed circuitry, see the *Power Management* section.

The digital core provides the engine for receiving, processing and sending all USB-PD packets as well as handling control of all other TPS65987DDK functionality. A portion of the digital core contains ROM memory which contains all the necessary firmware required to execute Type-C and PD applications. In addition, a section of the ROM called boot code, is capable of initializing the TPS65987DDK, loading of device configuration information and loading any code patches into volatile memory in the digital core. For a high-level block diagram of the digital core, a description of its features and more detailed circuitry, see the *Digital Core* section.

The TPS65987DDK is an I^2C slave to be controlled by a host processor (see the *I^2C Interfaces* section), and an SPI controller to write to and read from an optional external flash memory (see the *SPI Controller Interface* section).

The TPS65987DDK also integrates a thermal shutdown mechanism (see the*Thermal Shutdown* section) and runs off of accurate clocks provided by the integrated oscillators (see the *Oscillators* section).

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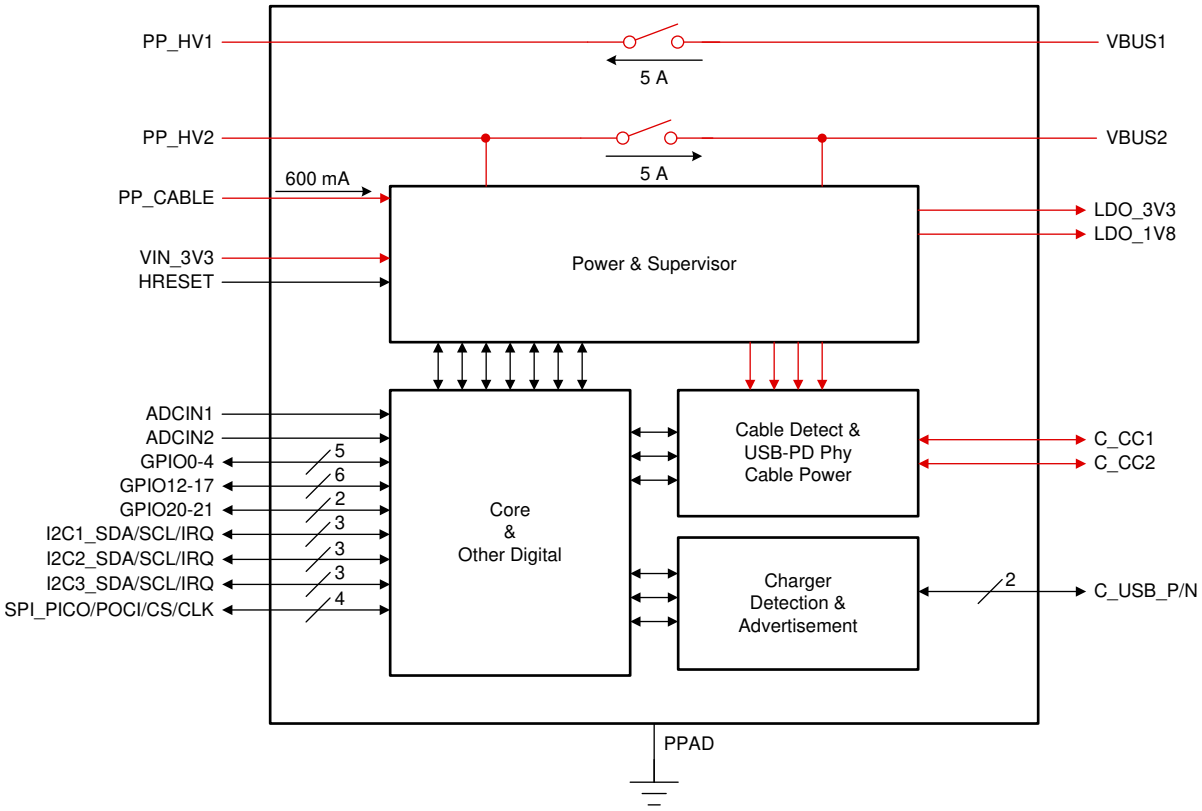
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 USB-PD Physical Layer

Figure 8-1 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block.

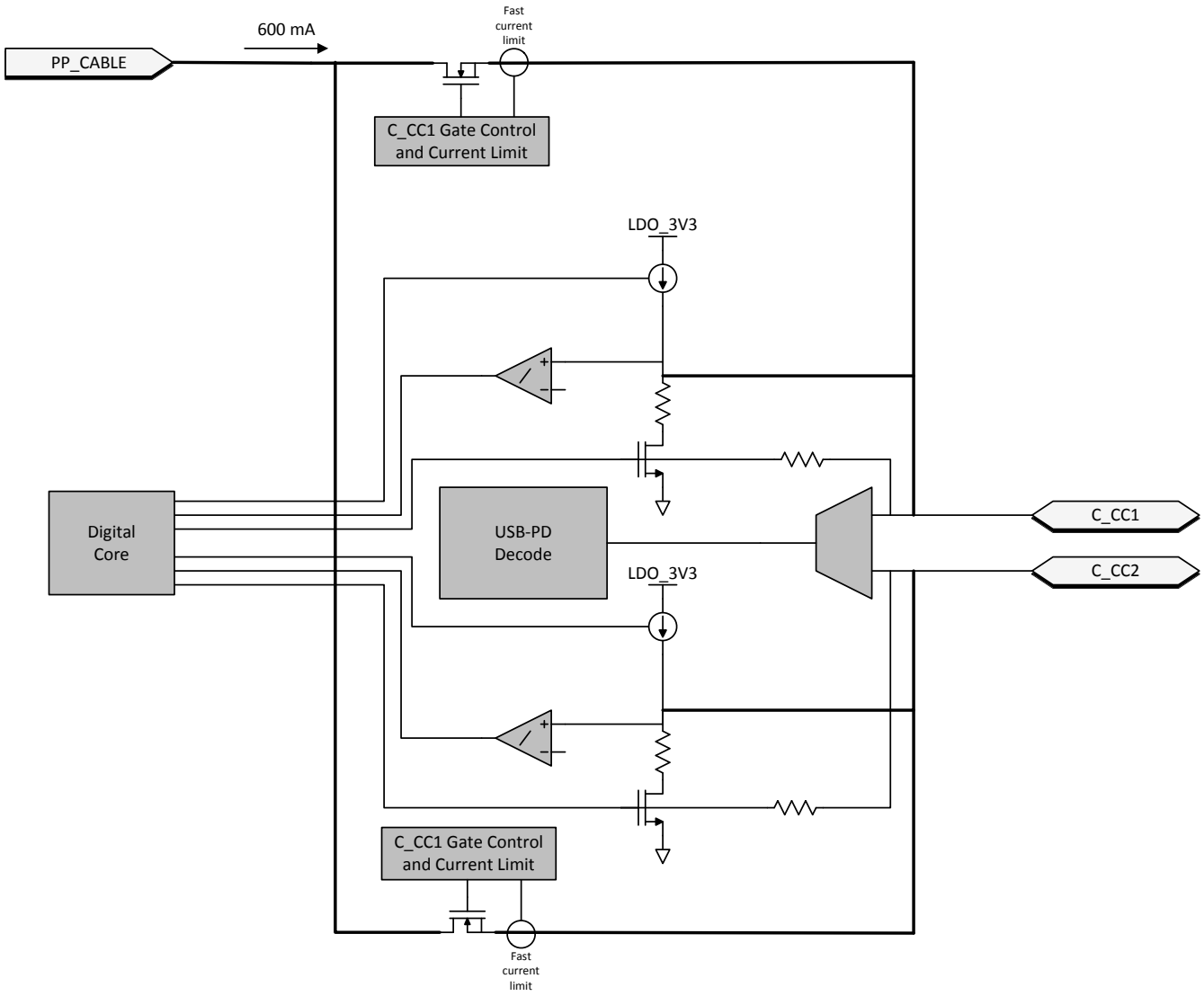


Figure 8-1. USB-PD Physical Layer, Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (C_CC1 or C_CC2) that is DC biased due to the DFP (or UFP) cable attach mechanism shown in *Port Power Switches*.

8.3.1.1 USB-PD Encoding and Signaling

Figure 8-2 illustrates the high-level block diagram of the baseband USB-PD transmitter. Figure 8-3 illustrates the high-level block diagram of the baseband USB-PD receiver.

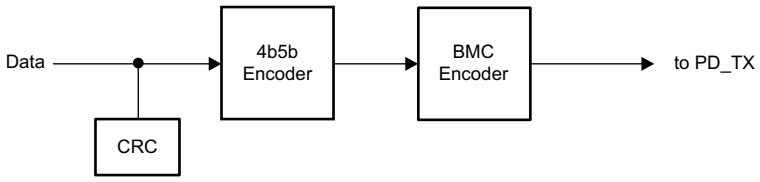


Figure 8-2. USB-PD Baseband Transmitter Block Diagram

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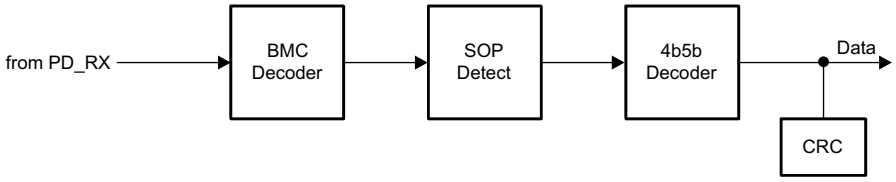

Figure 8-3. USB-PD Baseband Receiver Block Diagram

The USB-PD baseband signal is driven on the C_CCn pins with a tri-state driver. The tri-state driver is slew rate limited to reduce the high frequency components imparted on the cable and to avoid interference with frequencies used for communication.

8.3.1.2 USB-PD Bi-Phase Marked Coding

The USBP-PD physical layer implemented in the TPS65987DDK is compliant to the *USB-PD Specifications*. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). Figure 8-4 illustrates Biphase Mark Coding.

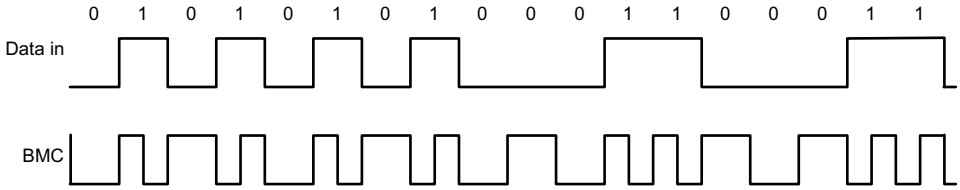

Figure 8-4. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the C_CC1 or C_CC2 pins with a tri-state driver. The tri-state driver is slew rate to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to ensure the receiver clocks the final bit of EOP.

8.3.1.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Since a BMC coded “1” contains a signal edge at the beginning and middle of the UI, and the BMC coded “0” contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude due to the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate that has minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the *USB-PD Specifications* for more details.

8.3.1.4 USB-PD BMC Transmitter

The TPS65987DDK transmits and receives USB-PD data over one of the C_CCn pins for a given CC pin pair (one pair per USB Type-C port). The C_CCn pins are also used to determine the cable orientation (see *Port Power Switches*) and maintain the cable/device attach detection. Thus, a DC bias exists on the C_CCn pins. The transmitter driver overdrives the C_CCn DC bias while transmitting, but returns to a Hi-Z state allowing the DC voltage to return to the C_CCn pin when not transmitting. Figure 8-5 shows the USB-PD BMC TX and RX driver block diagram.

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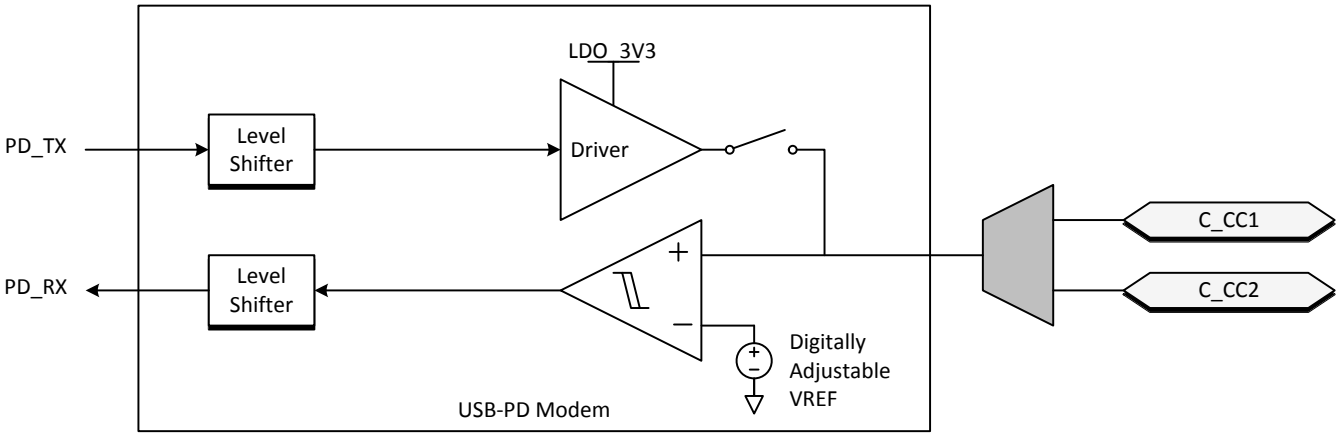

Figure 8-5. USB-PD BMC TX/Rx Block Diagram

Figure 8-6 shows the transmission of the BMC data on top of the DC bias. Note, The DC bias can be anywhere between the minimum threshold for detecting a UFP attach (VD_CCH_USB) and the maximum threshold for detecting a UFP attach to a DFP (VD_CCH_3P0). This means that the DC bias can be below VOH of the transmitter driver or above VOH.

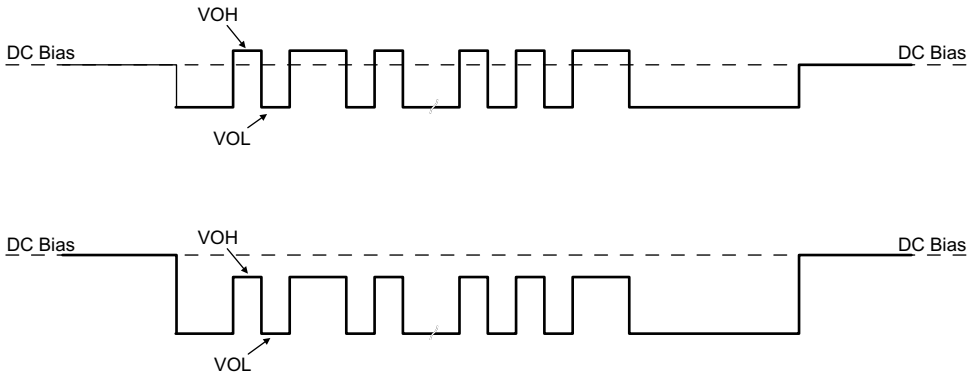

Figure 8-6. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the C_CCn lines. The signal peak, VTXP, is set to meet the TX masks defined in the *USB-PD Specifications*.

When driving the line, the transmitter driver has an output impedance of ZDRIVER. ZDRIVER is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. ZDRIVER impacts the noise ingression in the cable.

Figure 8-7 shows the simplified circuit determining ZDRIVER. It is specified such that noise at the receiver is bounded.

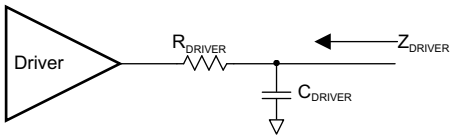

Figure 8-7. ZDRIVER Circuit

8.3.1.5 USB-PD BMC Receiver

The receiver block of the TPS65987DDK receives a signal that falls within the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

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Figure 8-8 shows an example of a multi-drop USB-PD connection. This connection has the typical UFP (device) to DFP (host) connection, but also includes cable USB-PD TX/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (ZBMCRX). The USB-PD Specification also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

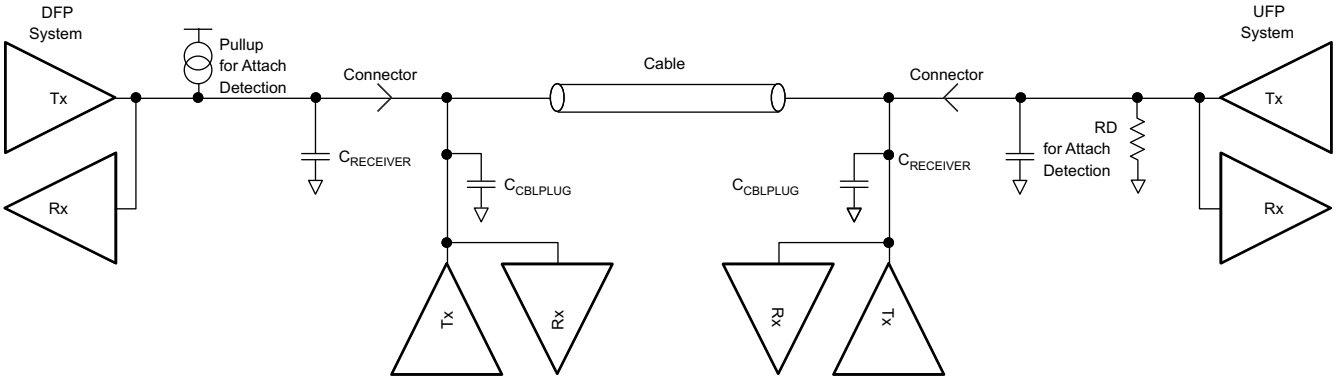

Figure 8-8. Example USB-PD Multi-Drop Configuration

8.3.2 Power Management

The TPS65987DDK power management block receives power and generates voltages to provide power to the TPS65987DDK internal circuitry. These generated power rails are LDO_3V3 and LDO_1V8. LDO_3V3 may also be used as a low power output for external flash memory. The power supply path is shown in Figure 8-9.

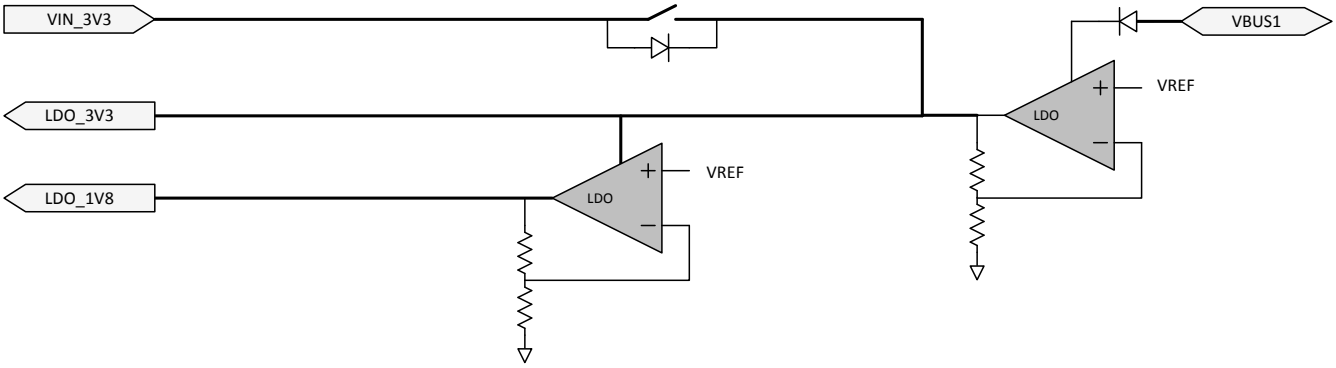

Figure 8-9. Power Supplies

The TPS65987DDK is powered from either VIN_3V3, VBUS1, or VBUS2. The normal power supply input is VIN3V3. In this mode, current flows from VIN_3V3 to LDO3V3 to power the core 3.3-V circuitry and I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V8 to power the 1.8-V core digital circuitry. When VIn_3V3 power is unavailable and power is available on VBUS1 or VBUS2 , the TPS65987DDK is powered from VBUS. In this mode, the voltage on VBUS1 or VBUS 2 is stepped down through an LDO to LDO_3V3.

8.3.2.1 Power-On and Supervisory Functions

A power-on reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present.

8.3.2.2 VBUS LDO

The TPS65987DDK contains an internal high-voltage LDO which is capable of converting up to 22 V from VBUS to 3.3 V for powering internal device circuitry. The VBUS LDO is only used during dead battery operation while the VIN_3V3 supply is not present. The VBUS LDO may be powered from either VBUS1 or VBUS2. The path connecting each VBUS to the internal LDO blocks reverse current, preventing power on one VBUS from leaking to the other. When power is present on both VBUS inputs, the internal LDO draws current from both VBUS pins.

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8.3.2.3 Supply Switch Over

VIN_3V3 takes precedence over VBUS, meaning that when both supply voltages are present the TPS65987DDK powers from VIN_3V3. See Figure 8-9 for a diagram showing the power supply path block. There are two cases in which a power supply switch-over occurs. The first is when VBUS is present first and then VIN_3V3 becomes available. In this case, the supply automatically switches over to VIN_3V3 and brown-out prevention is verified by design. The other way a supply switch-over occurs is when both supplies are present and VIN_3V3 is removed and falls below 2.85 V. In this case, a hard reset of the TPS65987DDK is initiated by device firmware, prompting a re-boot.

8.3.3 Port Power Switches

The figure below shows the TPS65987DDK internal power paths. The TPS65987DDK features two internal high-voltage power paths. Each path contains two back to back common drain N-Fets, current monitor, overvoltage monitor, undervoltage monitor, and temperature sensing circuitry. Each path may conduct up to 5 A safely. Additional external paths may be controlled through the TPS65987DDK GPIOs.

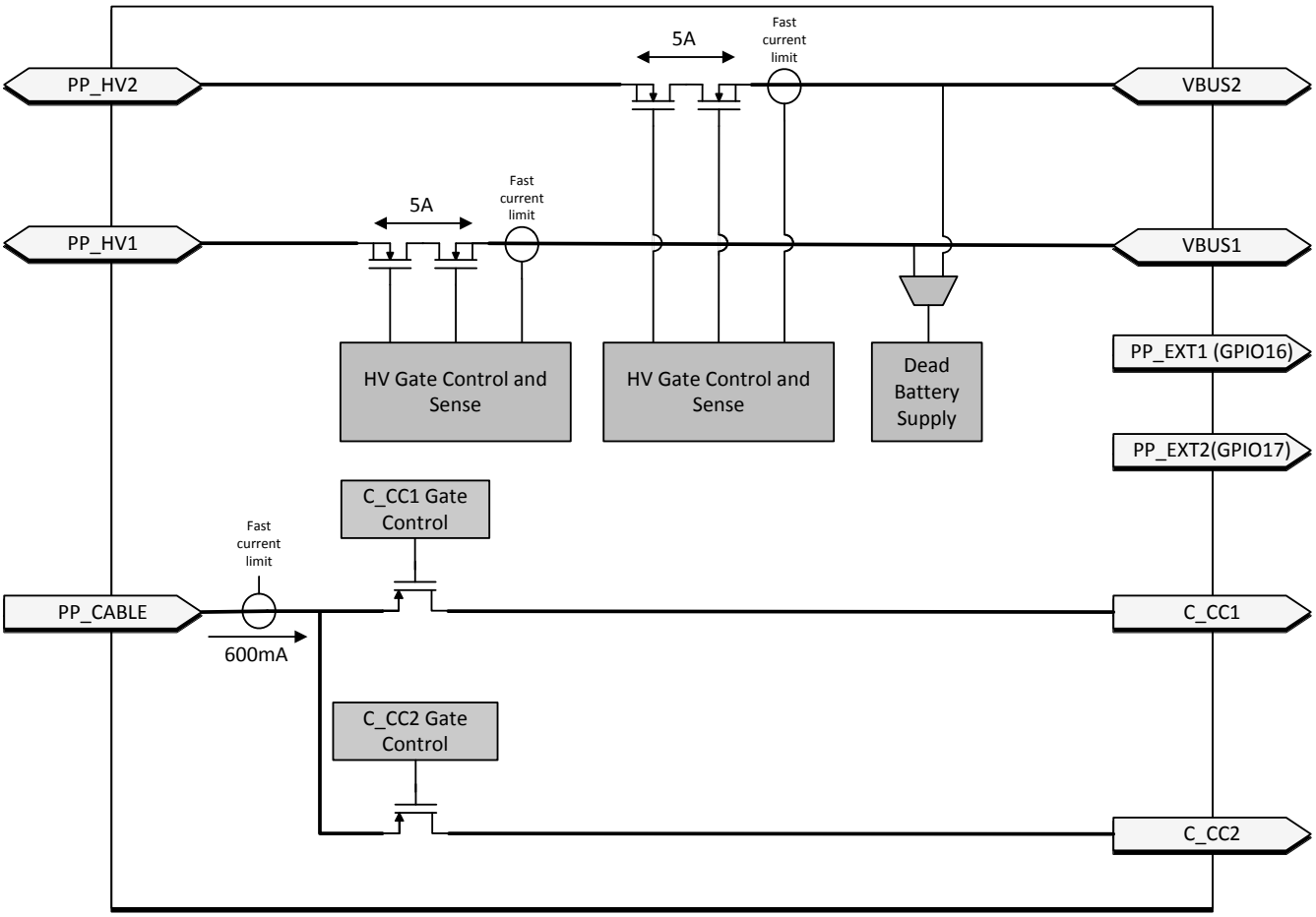

Figure 8-10. Port Power Switches

8.3.3.1 PP_HV Power Switch

The TPS65987DDK has two integrated bi-directional high-voltage switches that are rated for up to 5 A of current. Each switch may be used as either a sink or source path for supporting USB-PD power up to 20 V at 5 A of current.

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Note

The power paths can sustain up to 5 A of continuous current as long as the internal junction temperature of each path remains below 150°C. Care should be taken to follow the layout recommendations described in Thermal Dissipation for FET Drain Pads.

Note

It is recommended to use PPHV1 as a sink path and PPHV2 as a source path.

8.3.3.1.1 PP_HV Overcurrent Clamp

The internal source PP_HV path has an integrated overcurrent clamp circuit. The current through the internal PP_HV paths are current limited to I_{OCC}. The I_{OCC} value is selected by application firmware and only enabled while acting as a source. When the current through the switch exceeds I_{OCC}, the current clamping circuit activates and the path behaves as a constant current source. If the duration of the overcurrent event exceeds the deglitch time, the switch is latched off.

8.3.3.1.2 PP_HV Overcurrent Protection

The TPS65987DDK continuously monitors the forward voltage drop across the internal power switches. When a forward drop corresponding to a forward current of I_{OCP} is detected the internal power switch is latched off to protect the internal switches as well as upstream power supplies.

8.3.3.1.3 PP_HV OVP and UVP

Both the overvoltage and undervoltage protection levels are configured by application firmware. When the voltage on a port's VBUS pin exceeds the set overvoltage threshold or falls below the set undervoltage threshold the associated PP_HV path is automatically disabled.

8.3.3.1.4 PP_HV Reverse Current Protection

The TPS65987DDK reverse current protection has two modes of operation: Comparator Mode and Ideal Diode Mode. Both modes disable the power switch in cases of reverse current. The comparator protection mode is enabled when the switch is operating as a source, while the ideal diode protection is enabled while operating as a sink.

In the Comparator mode of reverse current protection, the power switch is allowed to behave resistively until the current reaches the amount calculated in Equation 1 and then blocks reverse current from VBUS to PP_HV. Figure 8-11 shows the diode behavior of the switch with comparator mode enabled.

$$IREVHV = VREVHV/RPPHV \quad (1)$$

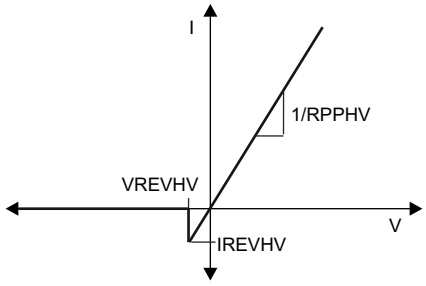

Figure 8-11. Comparator Mode (Source) Internal HV Switch I-V Curve

In the Ideal Diode mode of reverse current protection, the switch behaves as an ideal diode and blocks reverse current from PP_HV to VBUS. Figure 8-12 shows the diode behavior of the switch with ideal diode mode enabled.

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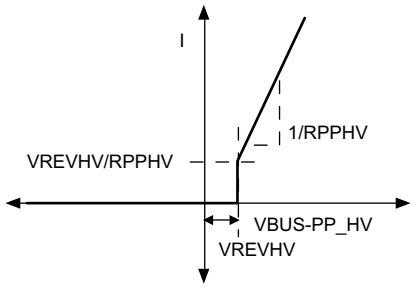

Figure 8-12. Ideal Diode Mode (Sink) Internal HV Switch I-V Curve

8.3.3.2 Schottky for Current Surge Protection

To prevent the possibility of large ground currents into the TPS65987DDK during sudden disconnects due to inductive effects in a cable, it is recommended that a Schottky diode be placed from VBUS to ground as shown in Figure 8-13.

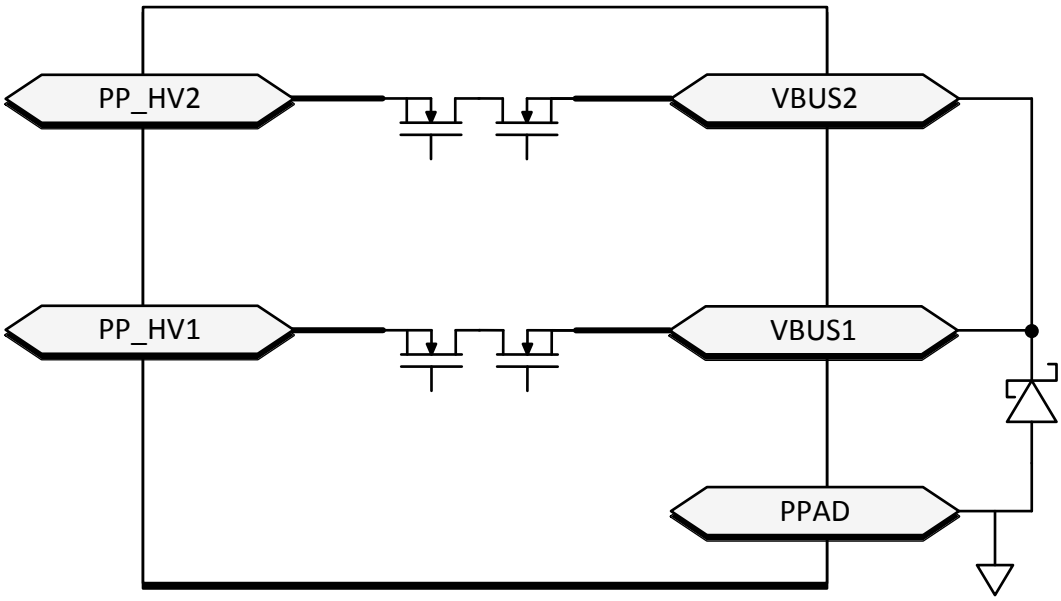

Figure 8-13. Schottky for Current Surge Protection

8.3.3.3 PP_EXT Power Path Control

GPIO16 and GPIO17 of the TPS65987DDK are intended for control of additional external power paths. These GPIO are active high when configured for external path control and disables in response to an OVP or UVP event. Overcurrent protection and thermal shutdown are not available for external power paths controlled by GPIO16 and GPIO17.

Note

GPIO16 and GPIO17 must be pulled to ground through an external pull-down resistor when used as external path control signals.

8.3.3.4 PP_CABLE Power Switch

The TPS65987DDK has an integrated 5-V unidirectional power mux that is rated for up to 600 mA of current. The mux may supply power to either of the port CC pins for use as VCONN power.

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8.3.3.4.1 PP_CABLE Overcurrent Protection

When enabled and providing VCONN power the TPS65987DDK PP_CABLE power switches have a 600-mA current limit. When the current through the PP_CABLE switch exceeds 600 mA, the current limiting circuit activates and the switch behaves as a constant current source. The switches do not have reverse current blocking when the switch is enabled and current is flowing to either C_CC1 or C_CC2.

8.3.3.4.2 PP_CABLE Input Good Monitor

The TPS65987DDK monitors the voltage at the PP_CABLE pins prior to enabling the power switch. If the voltage at PP_CABLE exceeds the input good threshold the switch is allowed to close, otherwise the switch remains open. Once the switch has been enabled, PP_CABLE is allowed to fall below the input good threshold.

8.3.3.5 VBUS Transition to VSAFE5V

The TPS65987DDK has an integrated active pull-down on VBUS for transitioning from high voltage to VSAFE5V. When the high voltage switch is disabled and VBUS > VSAFE5V, an amplifier turns on a current source and pulls down on VBUS. The amplifier implements active slew rate control by adjusting the pull-down current to prevent the slew rate from exceeding specification. When VBUS falls to VSAFE5V, the pull-down is turned off.

8.3.3.6 VBUS Transition to VSAFE0V

When VBUS transitions to near 0 V (VSAFE0V), the pull-down circuit in VBUS Transition to VSAFE5V is turned on until VBUS reaches VSAFE0V. This transition occurs within time TSAFE0V.

8.3.4 Cable Plug and Orientation Detection

Figure 8-14 shows the plug and orientation detection block at each C_CCn pin (C_CC1, C_CC2). Each pin has identical detection circuitry.

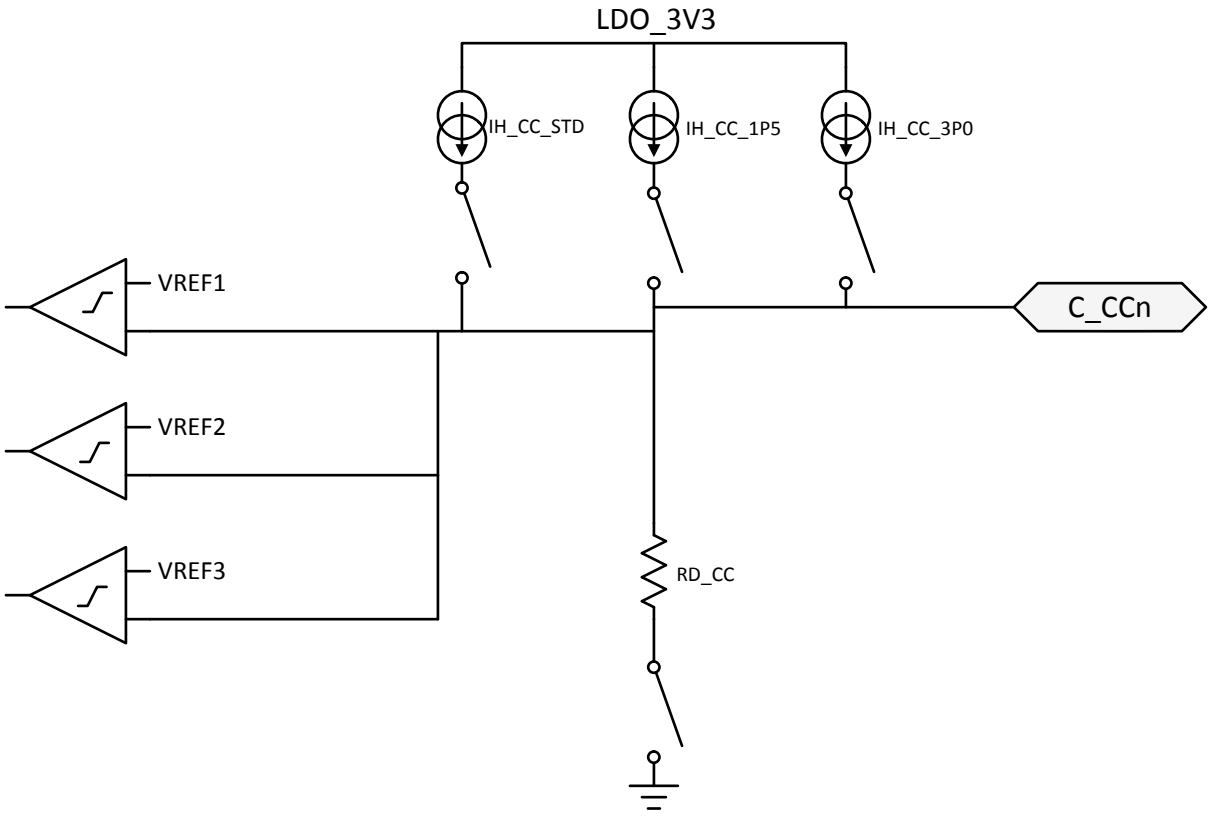

Figure 8-14. Plug and Orientation Detection Block

8.3.4.1 Configured as a DFP

When one of the TPS65987DDK ports is configured as a DFP, the device detects when a cable or a UFP is attached using the C_CC1 and C_CC2 pins. When in a disconnected state, the TPS65987DDK monitors the voltages on these pins to determine what, if anything, is connected. See USB Type-C Specification for more information.

Table 8-1 shows the Cable Detect States for a DFP.

Table 8-1. Cable Detect States for a DFP

C_CC1	C_CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both C_CC pins for attach. Power is not applied to VBUS or VCONN until a UFP connect is detected.
Rd	Open	UFP attached	Monitor C_CC1 for detach. Power is applied to VBUS but not to VCONN (C_CC2).
Open	Rd	UFP attached	Monitor C_CC2 for detach. Power is applied to VBUS but not to VCONN (C_CC1).
Ra	Open	Powered Cable-No UFP attached	Monitor C_CC2 for a UFP attach and C_CC1 for cable detach. Power is not applied to VBUS or VCONN (C_CC1) until a UFP attach is detected.
Open	Ra	Powered Cable-No UFP attached	Monitor C_CC1 for a UFP attach and C_CC2 for cable detach. Power is not applied to VBUS or VCONN (C_CC1) until a UFP attach is detected.
Ra	Rd	Powered Cable-UFP Attached	Provide power on VBUS and VCONN (C_CC1) then monitor C_CC2 for a UFP detach. C_CC1 is not monitored for a detach.
Rd	Ra	Powered Cable-UFP attached	Provide power on VBUS and VCONN (C_CC2) then monitor C_CC1 for a UFP detach. C_CC2 is not monitored for a detach.
Rd	Rd	Debug Accessory Mode attached	Sense either C_CC pin for detach.
Ra	Ra	Audio Adapter Accessory Mode attached	Sense either C_CC pin for detach.

When a TPS65987DDK port is configured as a DFP, a current IH_CC is driven out each C_CCn pin and each pin is monitored for different states. When a UFP is attached to the pin a pull-down resistance of Rd to GND exists. The current IH_CC is then forced across the resistance Rd generating a voltage at the C_CCn pin.

When configured as a DFP advertising Default USB current sourcing capability, the TPS65987DDK applies IH_CC_USB to each C_CCn pin. When a UFP with a pull-down resistance Rd is attached, the voltage on the C_CCn pin pulls below VH_CCD_USB. The TPS65987DDK can be configured to advertise default (500 mA or 900 mA), 1.5-A and 3-A sourcing capabilities when acting as a DFP.

When the C_CCn pin is connected to an active cable VCONN input, the pull-down resistance is different (Ra). In this case the voltage on the C_CCn pin will pull below VH_CCA_USB/1P5/3P0 and the system recognizes the active cable.

The VH_CCD_USB/1P5/3P0 thresholds are monitored to detect a disconnection from each of these cases respectively. When a connection has been recognized and the voltage on the C_CCn pin rises above the VH_CCD_USB/1P5/3P0 threshold, the system registers a disconnection.

8.3.4.2 Configured as a UFP

When a TPS65987DDK port is configured as a UFP, the TPS65987DDK presents a pull-down resistance RD_CC on each C_CCn pin and waits for a DFP to attach and pull-up the voltage on the pin. The DFP pulls-up the C_CCn pin by applying either a resistance or a current. The UFP detects an attachment by the presence of VBUS. The UFP determines the advertised current from the DFP by the pull-up applied to the C_CCn pin.

8.3.4.3 Configured as a DRP

When a TPS65987DDK port is configured as a DRP, the TPS65987DDK alternates the port's C_CCn pins between the pull-down resistance, Rd, and pull-up current source, Rp.

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8.3.4.4 Fast Role Swap Signaling

The TPS65987DDK cable plug block contains additional circuitry that may be used to support the Fast Role Swap (FRS) behavior defined in the USB Power Delivery Specification. The circuitry provided for this functionality is detailed in Figure 8-15.

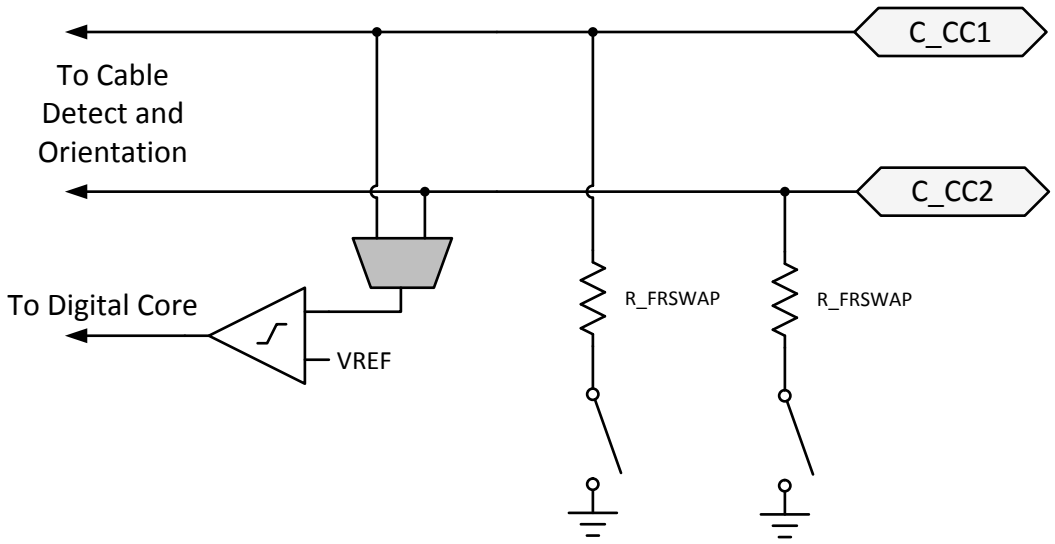

Figure 8-15. Fast Role Swap Detection and Signaling

When a TPS65987DDK port is operating as a sink with FRS enabled, the TPS65987DDK monitors the CC pin voltage. If the CC voltage falls below VTH_FRS a fast role swap situation is detected and signaled to the digital core. When this signal is detected the TPS65987DDK ceases operating as a sink and begin operating as a source.

When a TPS65987DDK port is operating as a source with FRS enabled, the TPS65987DDK digital core can signal to the connected port partner that a fast role swap is required by enabling the R_FRSWAP pull down on the connected CC pin. When this signal is sent the TPS65987DDK ceases operating as the source and begin operating as a sink.

8.3.5 Dead Battery Operation

8.3.5.1 Dead Battery Advertisement

The TPS65987DDK supports booting from no-battery or dead-battery conditions by receiving power from VBUS. Type-C USB ports require a sink to present Rd on the CC pin before a USB Type-C source provides a voltage on VBUS. The TPS65987DDK hardware is configured to present this Rd during a dead-battery or no-battery condition. Additional circuitry provides a mechanism to turn off this Rd once the device no longer requires power from VBUS. Figure 8-16 shows the configuration of the C_CCn pins, and elaborates on the basic cable plug and orientation detection block shown in Figure 8-14. A resistance R_RPD is connected to the gate of the pull-down FET on each C_CCn pin. During normal operation when configured as a sink, RD is RD_CC; however, while dead-battery or no-battery conditions exist, the resistance is un-trimmed and is RD_DB. When RD_DB is presented during dead-battery or no-battery, application code switches to RD_CC.

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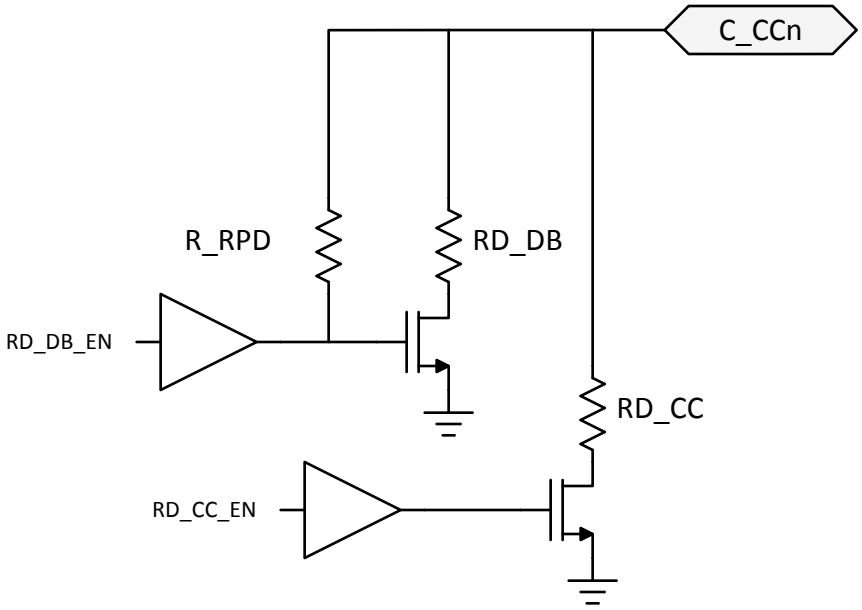

Figure 8-16. Dead Battery Pull-Down Resistor

In this case, the gate driver for the pull-down FET is Hi-Z at its output. When an external connection pulls up on C_CCn (the case when connected to a DFP advertising with a pull-up resistance Rp or pull-up current), the connection through R_RPD pulls up on the FET gate turning on the pull-down through RD_DB. In this condition, the C_CCn pin acts as a clamp VTH_DB in series with the resistance RD_DB.

8.3.5.2 BUSPOWER (ADCIN1)

The BUSPOWER input to the internal ADC controls the behavior of the TPS65987DDK in response to VBUS being supplied during a dead battery condition. The pin must be externally tied to the LDO_3V3 output via a resistive divider. At power-up the ADC converts the BUSPOWER voltage and the digital core uses this value to determine start-up behavior. It is recommended to tie ADCin1 to LDO_3V3 through a resistor divider as shown in Figure 8-17. For more information about how to use the ADCIN1 pin to configure the TPS65987DDK, see the Boot section.

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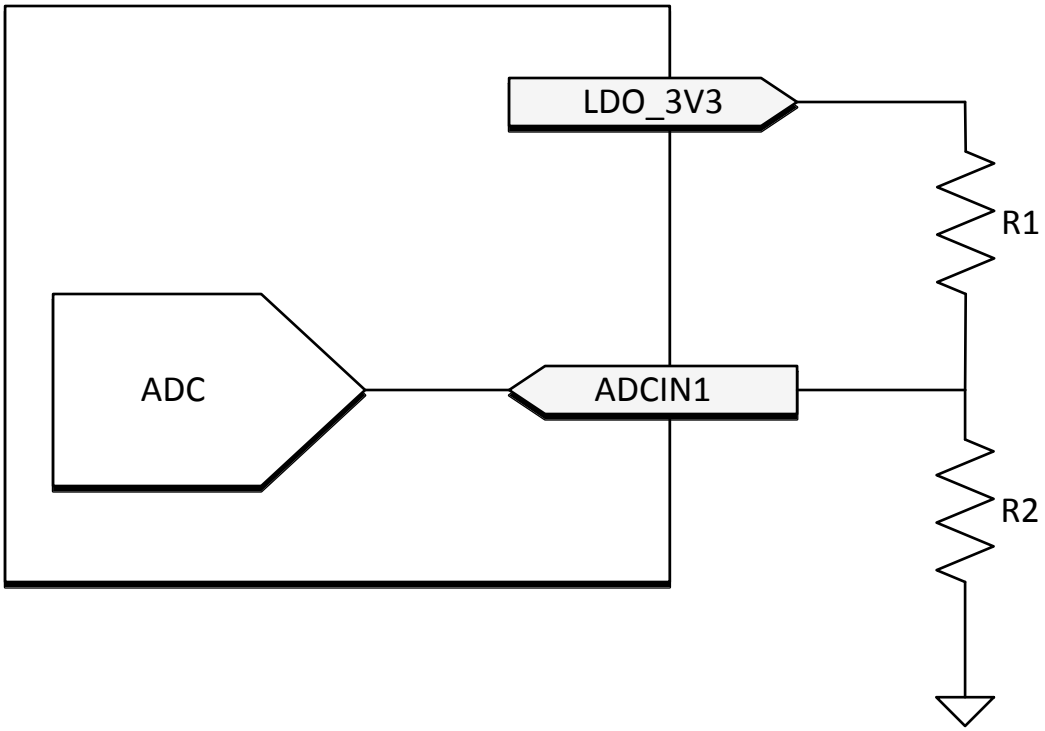

Figure 8-17. ADCIN1 Resistor Divider

Note

Devices implementing the BP_WaitFor3V3_External configuration must use GPIO16 for external sink path control.

8.3.6 ADC

The TPS65987DDK integrated ADC is accessible to internal firmware only. The ADC reads are not available for external use.

8.3.7 DisplayPort HPD

To enable HPD signaling through PD messaging, a single pin is used as the HPD input and output for each port. When events occur on these pins during a DisplayPort connection though the Type-C connector (configured by firmware), hardware timers trigger and interrupt the digital core to indicate needed PD messaging. When one of the TPS65987DDK's ports is operating as a DP source, its corresponding HPD pin operates as an output (HPD TX), and when a port is operating as a DP sink, its corresponding HPD pin operates as an input (HPD RX). When DisplayPort is not enabled via firmware the HPD pin operates as a generic GPIO (GPIO3).

8.3.8 Digital Interfaces

8.3.8.1 General GPIO

Figure 8-18 shows the GPIO I/O buffer for all GPIOn pins. GPIOn pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a de-glitched digital input . The push-pull output is a simple CMOS output with independent pull-down control allowing open-drain connections. The weak push-pull is also a CMOS output, but with GPIO_RPU resistance in series with the drain. The supply voltage to the output buffer is LDO_3V3 and LDO_1V8 to the input buffer. When interfacing with non 3.3-V I/O devices the output buffer may be configured as an open drain output and an external pull-up resistor attached to the GPIO pin. The pull-up and pull-down output

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drivers are independently controlled from the input and are enabled or disabled via application code in the digital core.

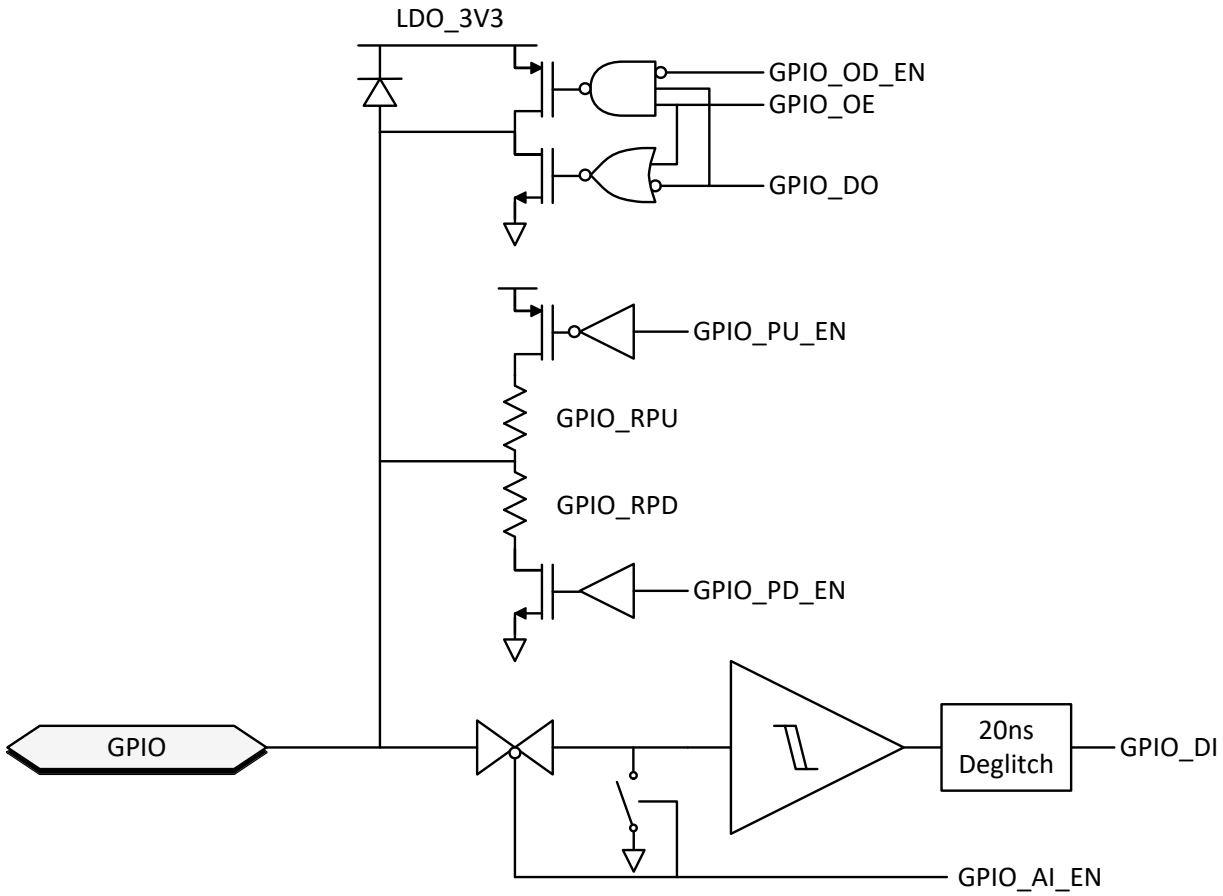

Figure 8-18. General GPIO Buffer

8.3.8.2 I²C

The TPS65987DDK features three I²C interfaces. The I²C1 interface is configurable to operate as a master or slave. The I²C2 interface may only operate as a slave. The I²C3 interface may only operate as a master. The I²C I/O driver is shown in Figure 8-19. This I/O consists of an open-drain output and in input comparator with de-glitching. The I²C input thresholds are set by LDO_1V8 and by default.

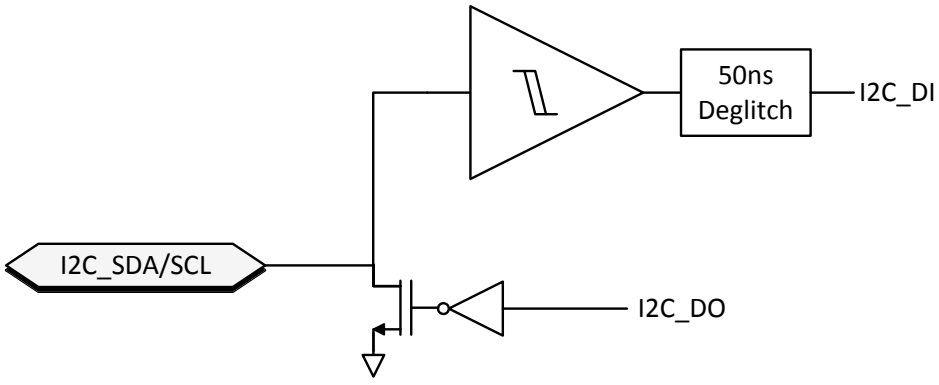

Figure 8-19. I²C Buffer

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8.3.8.3 SPI

The TPS65987DDK has a single SPI controller interface for use with external memory devices. Figure 8-20 shows the I/O buffers for the SPI interface.

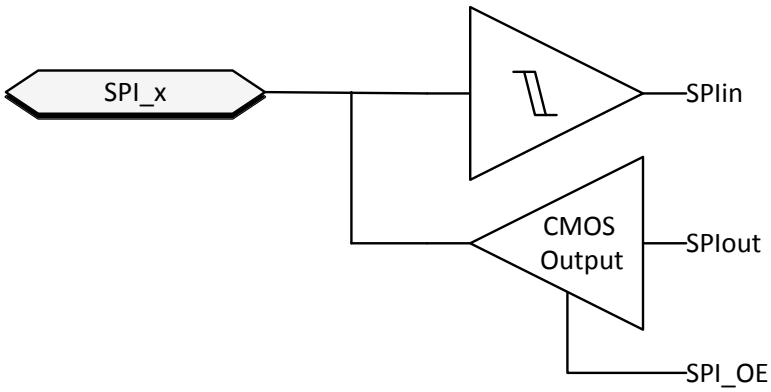

Figure 8-20. SPI buffer

8.3.9 Digital Core

The figure below shows a simplified block diagram of the digital core.

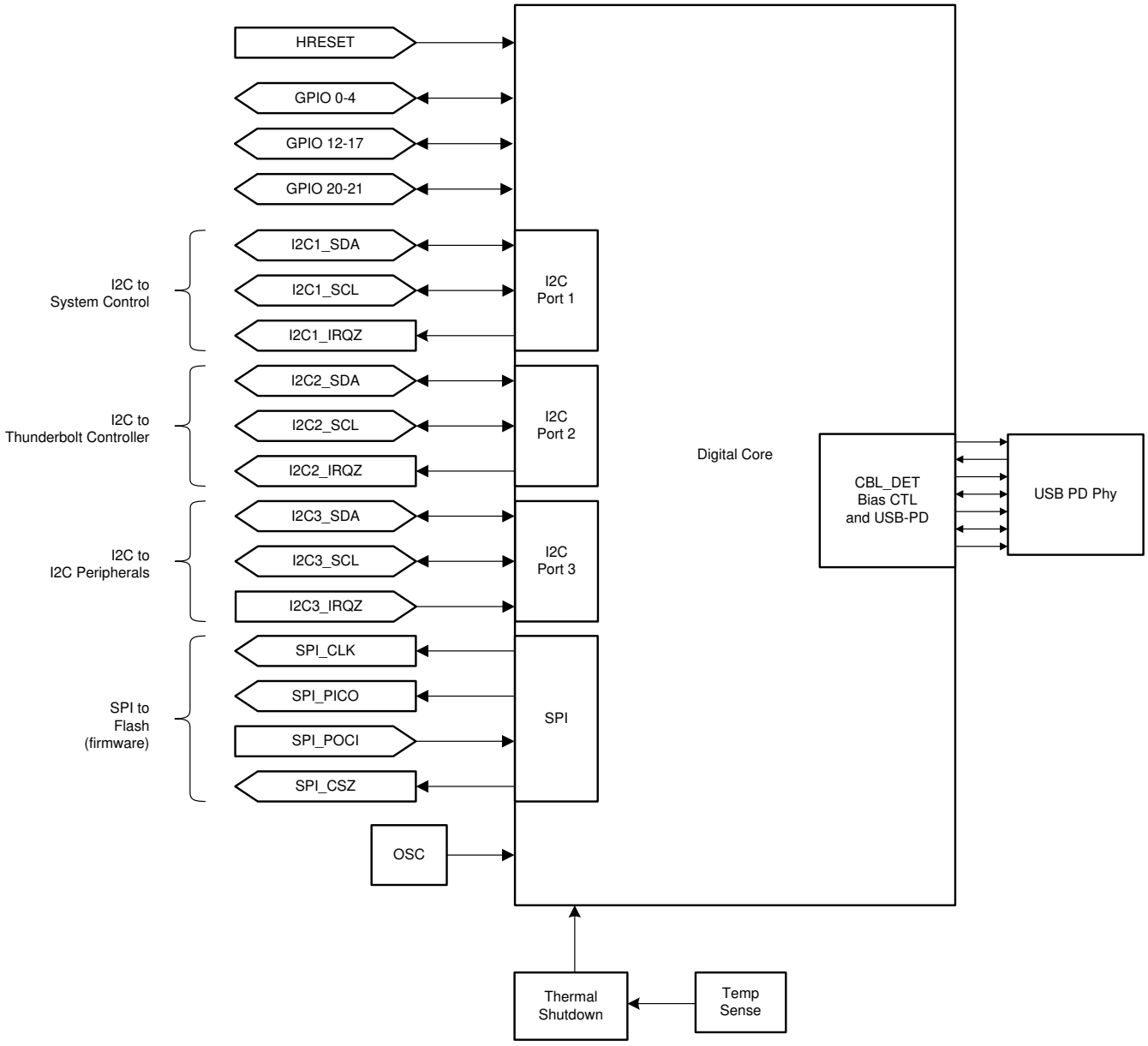

Figure 8-21. Digital Core Block Diagram

8.3.10 I²C Interfaces

8.3.10.1 I²C Interface Description

The TPS65987DDK support Standard and Fast mode I²C interface. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

A master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input and output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as

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changes in the data line at this time are interpreted as control commands (Start or Stop). The master sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

Figure 8-22 shows the start and stop conditions of the transfer. Figure 8-23 shows the SDA and SCL signals for transferring a bit. Figure 8-24 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

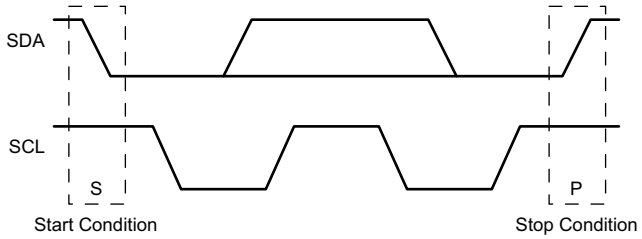

Figure 8-22. I²C Definition of Start and Stop Conditions

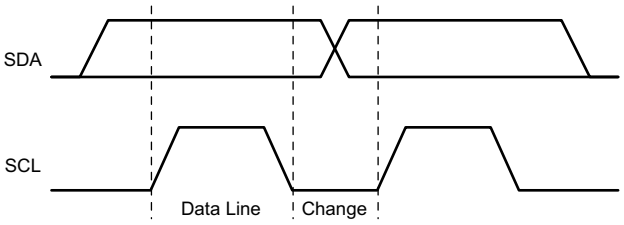

Figure 8-23. I²C Bit Transfer

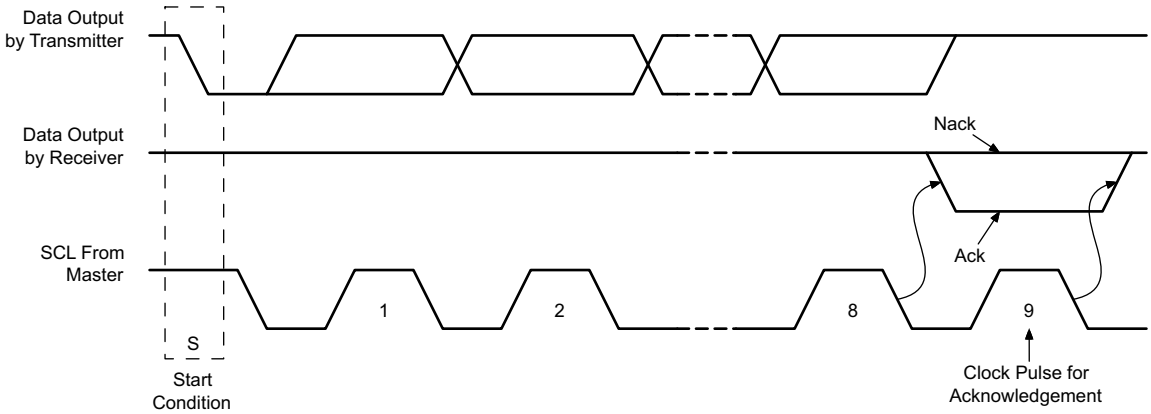

Figure 8-24. I²C Acknowledgment

8.3.10.2 I²C Clock Stretching

The TPS65987DDK features clock stretching for the I²C protocol. The TPS65987DDK slave I²C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more

data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line remains low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4 µs for standard 100-kbps I²C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

8.3.10.3 I²C Address Setting

The boot flow sets the hardware configurable unique I²C address of the TPS65987DDK before the port is enabled to respond to I²C transactions. For the I2C1 interface, the unique I²C address is determined by the analog level set by the analog ADCIN2 pin as shown in Table 8-2 .

Table 8-2. I²C Default Unique Address I2C1

DEFAULT I²C UNIQUE ADDRESS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Set by ADCIN2 divider, see I²C Pin Address Setting (ADCIN2)							R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							

For the I2C2 interface, the unique I²C address is a fixed value as shown in Table 8-3 .

Table 8-3. I²C Default Unique Address I2C2

DEFAULT I²C UNIQUE ADDRESS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Set by ADCIN2 divider, see I²C Pin Address Setting (ADCIN2)							R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

Note

The TPS65987DDK I2C address values are set and controlled by device firmware. Certain firmware configurations may override the presented address settings.

8.3.10.4 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C master and a single TPS65987DDK. The I²C Slave sub-address is used to receive or respond to Host Interface protocol commands. Figure 8-25 and Figure 8-26 show the write and read protocol for the I²C slave interface, and a key is included in Figure 8-27 to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

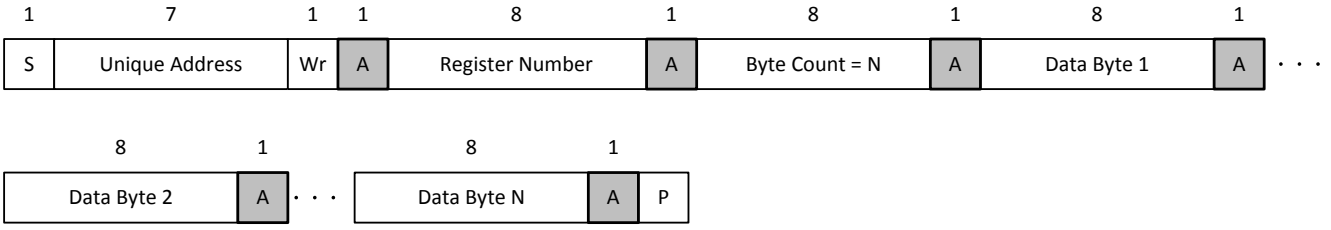

Figure 8-25. I²C Unique Address Write Register Protocol

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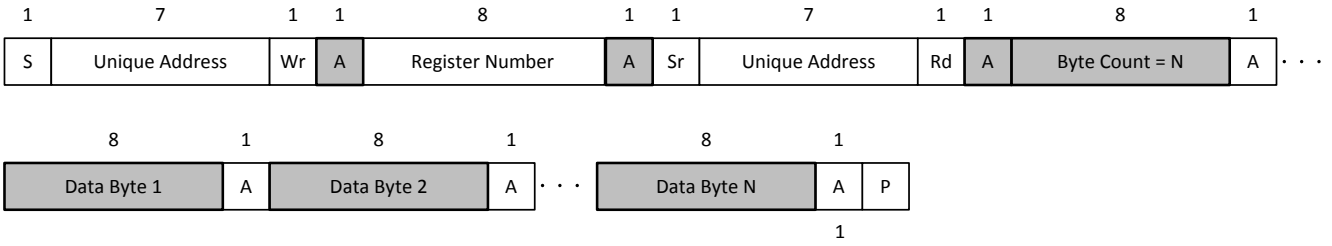

Figure 8-26. I²C Unique Address Read Register Protocol

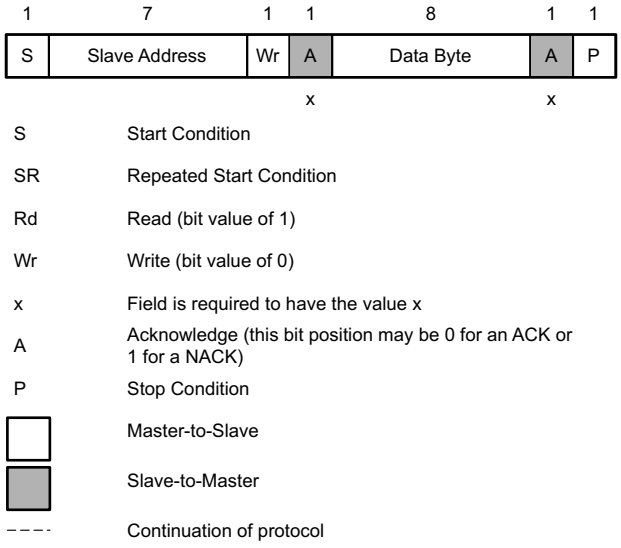

Figure 8-27. I²C Read/Write Protocol Key

8.3.10.5 I²C Pin Address Setting (ADCIN2)

To enable the setting of multiple I²C addresses using a single TPS65987DDK pin, a resistor divider is placed externally on the ADCIN2 pin. The internal ADC then decodes the address from this divider value. Figure 8-28 shows the decoding.

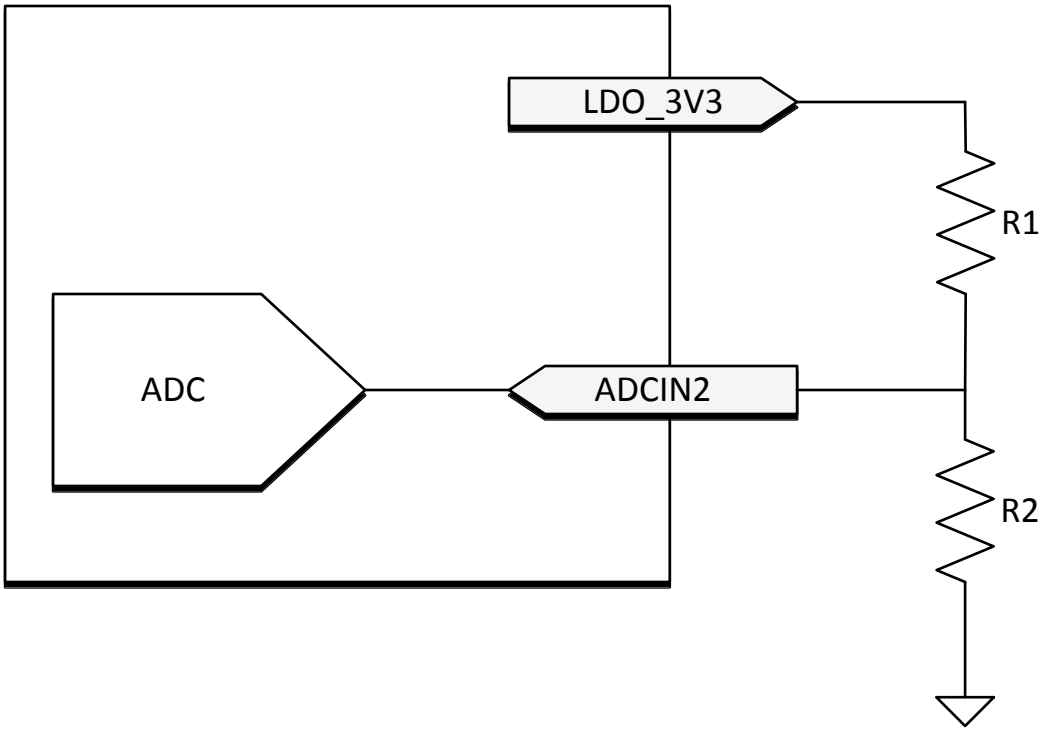

Figure 8-28. I²C Address Divider

Table 8-4 lists the external divider needed to set bits [3:1] of the I²C Unique Address.

Table 8-4. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C1 UNIQUE ADDRESS (7bit)	I²C2 UNIQUE ADDRESS (7bit)
DIV_min	DIV_max	I²C1 SLAVE ADDRESS	I²C2 SLAVE ADDRESS
Short to GND	0.18	0x20	0x38
0.20	0.38	0x21	0x3F
0.40	0.58	0x22	0x4F
0.6	Short to LDO_3V3	0x23	0x48

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

8.3.11 SPI Controller Interface

The TPS65987DDK loads any ROM patch and-or configuration from flash memory during the boot sequence. The TPS65987DDK is designed to power the flash from LDO_3V3 in order to support dead-battery or no-battery conditions, and therefore pull-up resistors used for the flash memory must be tied to LDO_3V3. The flash memory IC must support 12 MHz SPI clock frequency. The size of the flash must be at least 64 kB. The SPI controller of the TPS65987DDK supports SPI Mode 0. For Mode 0, data delay is defined s0 that data is output on the same cycle as chip select ($\overline{\text{SPI_CS}}$ pin) becomes active. The chip select polarity is active-low. The clock phase is defined such that data (on the SPI_POCI and SPI_PICO pins) is shifted out on the falling edge of the clock (SPI_CLK pin) and data is sampled on the rising edge of the clock. The clock polarity for chip select is defined such that when data is not being transferred the SPI_CLK pin is held (or idling) low. The minimum erasable sector size of the flash must be 4 KB. The W25X05CL or similar is recommended.

8.3.12 Thermal Shutdown

The TPS65987DDK features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all

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functions except for supervisory circuitry when die temperature goes above a rising temperature of TSD_MAIN. The temperature shutdown has a hysteresis of TSDH_MAIN and when the temperature falls back below this value, the device resumes normal operation.

The power path thermal shutdown monitors the temperature of each internal power path and disables the power path in response to an overtemperature event. Once the temperature falls below TSDH_PWR the path can be configured to resume operation or remain disabled until re-enabled by firmware.

8.3.13 Oscillators

The TPS65987DDK has two independent oscillators for generating internal clock domains. A 24-MHz oscillator generates clocks for the core during normal operation. A 100-kHz oscillator generates clocks for various timers and clocking the core during low power states.

8.4 Device Functional Modes

8.4.1 Boot

At initial power on the device goes through a boot routine. This routine is responsible for initializing device register values and loading device patch and configuration bundles. The device's functional behavior after boot can be configured through the use of pin straps on the SPI_POCI and ADCIN1 pins as shown in Table 8-5.

Table 8-5. Boot Mode Pin Strapping

SPI_POCI	ADCIN1 DIV = R2/(R1+R2)(1)		DEAD BATTERY MODE	DEVICE CONFIGURATION
	DIV MIN	DIV MAX		
1	0.00	0.18	BP_NoResponse	Safe Configuration
1	0.20	0.28	BP_WaitFor3V3_Internal	Safe Configuration
1	0.30	0.38	BP_ECWait_Internal	Infinite Wait
1	0.40	0.48	BP_WaitFor3V3_External	Safe Configuration
1	0.50	0.58	BP_ECWait_External	Infinite Wait
1	0.60	1.00	BP_NoWait	Safe Configuration
0	0.10	0.18	BP_NoResponse	Infinite Wait
0	0.20	0.28	BP_NoResponse	Infinite Wait
0	0.30	0.38	BP_ECWait_Internal	Infinite Wait
0	0.40	0.48	BP_NoWait	Configuration 3
0	0.50	0.58	BP_ECWait_External	Infinite Wait
0	0.60	0.68	BP_NoResponse	Infinite Wait
0	0.70	0.78	BP_NoWait	Reserved
0	0.80	0.88	BP_NoResponse	Infinite Wait
0	0.90	1.00	BP_NoWait	Configuration 5

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

The pin strapping configures two different parameters, Dead battery mode and device configuration. The dead battery mode selects device behavior when powered from VBUS. The dead battery mode behaviors are detailed in Table 8-6.

Table 8-6. Dead Battery Configurations

CONFIGURATION	DESCRIPTION
BP_NoResponse	No power switch is enabled and the device does not start-up until VIN_3V3 is present.
BP_WaitFor3V3_Internal	The internal power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.

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Table 8-6. Dead Battery Configurations (continued)

CONFIGURATION	DESCRIPTION
BP_WaitFor3V3_External	The external power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.
BP_ECWait_Internal	The internal power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device infinitely tries to load configuration.
BP_ECWait_External	The external power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device infinitely tries to load configuration.
BP_NoWait	The device continues to start-up and attempts to load configurations while receiving power from VBUS. Once configuration is loaded the appropriate power switch is closed based on the loaded configuration.

Note

Devices implementing the BP_WaitFor3V3_External or BP_ECWait_External configuration must use GPIO16 for external sink path control, while devices implementing the BP_WaitFor3V3_Internal or BP_ECWait_Internal must use PPHV1 as the sink path.

When powering up from VIN_3V3 or VBUS the device will attempt to load configuration information from the SPI or I2C digital interfaces. The device configuration settings select the device behavior should configuration information not be available during the device boot process. Table 8-7 shows the device behavior for each device configuration setting.

Table 8-7. Device Default Configurations

CONFIGURATION	DESCRIPTION
Safe	Ports disabled, if powered from VBUS operates a legacy sink
Infinite Wait	Device infinitely waits in boot state for configuration information
Configuration 1	Reserved
Configuration 2	Reserved
Configuration 3	UFP only (Internal Switch) 5-20 V at 0.9 - 3.0-A Sink capability TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled
Configuration 4	Reserved
Configuration 5	UFP only (External Switch)) 5-20 V at 0.9-3.0-A Sink capability 5 V at 3.0-A Source capability TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled

8.4.2 Power States

The TPS65987DDK may operate in one of three different power states: Active, Idle, or Sleep. The functionality available in each state is summarized in Table 8-8.

Table 8-8. Power States

	ACTIVE	IDLE	SLEEP
Type-C State			
Type-C State	Connected or Unconnected	Connected or Unconnected	Unconnected
Type-C Port 2 State	Connected or Unconnected	Connected or Unconnected	Unconnected
LDO_3V3(1)	Valid	Valid	Valid
LDO_1V8	Valid	Valid	Valid
Oscillator Status			
Digital Core Clock Frequency	12 MHz	4 MHz - 6 MHz	100 kHz

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Table 8-8. Power States (continued)

	ACTIVE	IDLE	SLEEP
100-kHz Oscillator Status	Enabled	Enabled	Enabled
24-MHz Oscillator Status	Enabled	Enabled	Disabled
Available Features			
Type-C Detection	Yes	Yes	Yes
PD Communication	Yes	No	No
I2C Communication	Yes	Yes	No
SPI Communication	Yes	No	No
Wake Events			
Wake on Attach/Detach	N/A	Yes	Yes
Wake on PD Communication	N/A	Yes(2)	No
Wake on I2C Communication	N/A	Yes	Yes

(1) LDO_3V3 may be generated from either VIN_3V3 or VBUS. If LDO_3V3 is generated from VBUS, TPS65987DDK port only operate as sinks.
(2) Wake up from Idle to Active upon a PD message is supported however the first PD message received is lost.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS65987DDK firmware implements a host interface over I^2C to allow for the configuration and control of all device options. Initial device configuration is configured through a configuration bundle loaded onto the device during boot. The bundle may be loaded through I^2C or SPI. The TPS65987DDK configuration bundle and host interface allow the device to be customized for each specific application. The configuration bundle can be generated through the Application Customization Tool.

9.2 Typical Applications

9.2.1 USB4 Device Application with Host Charging

The figure below shows a USB4 Device application, where there are a total of four Type-C PD Ports. One port is the main connection to a USB4 Host that is a UFP in terms of data and a source of power. The other three ports are DFPs in terms of data and source power. Generally the main UFP source Type-C PD port provides the highest power (up to 100 W) to charge a USB4 Host. The key four devices in the system are the PD Controller (2), Dock Management Controller, USB4 Hub Controller, and UFP Variable Power Supply.

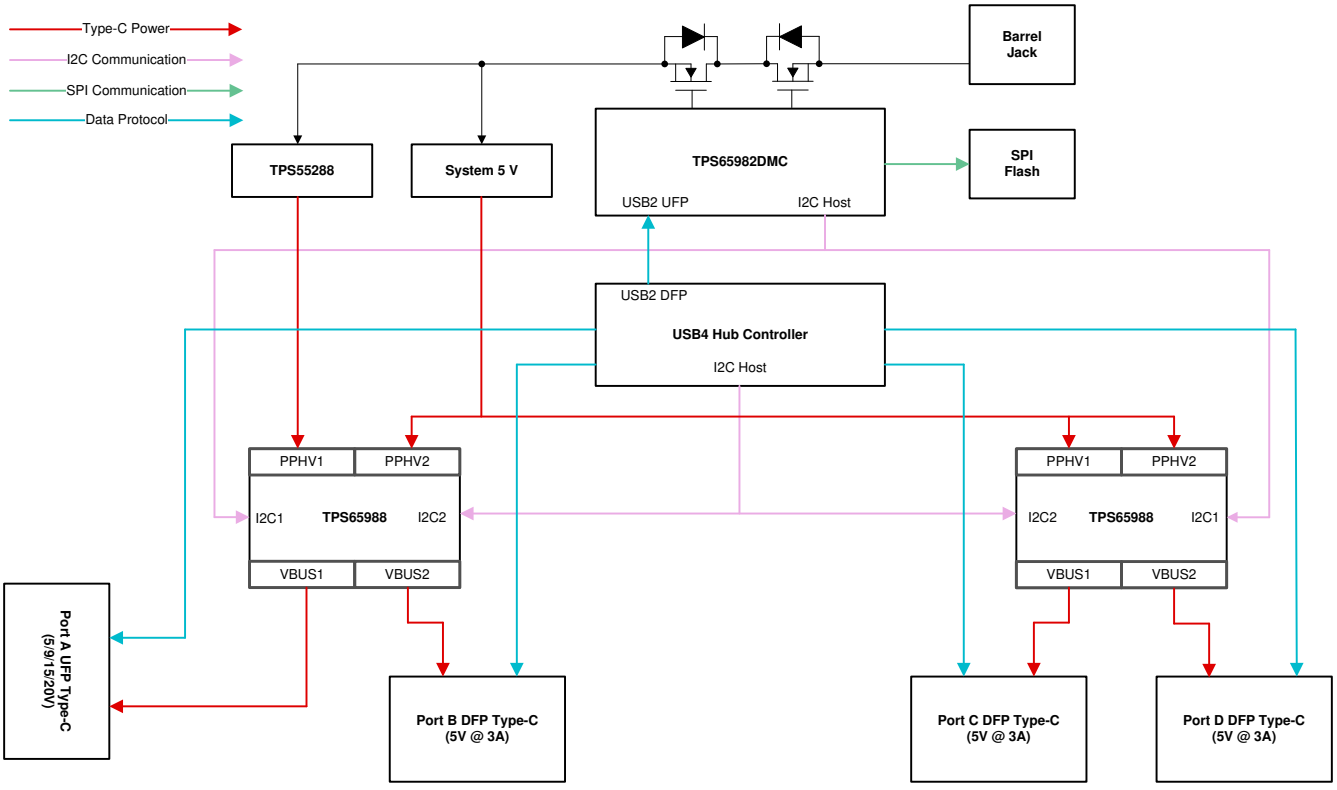

Figure 9-1. USB4 Device Block Diagram

In this application, two dual port TPS65987DDK PD controllers are used to determine the connection and provide power on the Type-C ports. The primary TPS65987DDK manages Port A (UFP Source) and Port B (DFP Source). The secondary TPS65987DDK manages the other two, Port C (DFP Source) and Port D (DFP Source). For systems that do not need all four ports a combination of TPS65987DDK and TPS65987DDK may be used to

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scale for specific design requirements. The PD controllers have two I2C clients that are controlled by the Dock Management Controller and the USB4 Hub Controller. The PD controllers have an optional I2C Host that may be used to control a variable power supply.

The Dock Management Controller (DMC), TPS65982DMC, main functions are the Connection Manager, Power Manager, Input Power Control, Secure Firmware Update & booting of the PD controllers. The Connection Manager determines the capabilities of the UFP connection and sets the DFP capabilities accordingly. The Power Manager keeps the power allocated to each of the Type-C ports within a specific power budget and also monitors the entire system power to keep from over loading the Barrel Jack adapter supply. The DMC also controls the input power to the system and soft starts the power path to prevent large inrush currents when the Barrel Jack supply is connected. The Secure Firmware Update is accomplished over USB2, the DMC is connected to one of the USB2 DFP ports on the USB4 Hub Controller or USB2 Hub in the system. The DMC provides the Secure Firmware Update for itself and the PD controllers. The DMC will boot the PD controllers over the I2C connection. The I2C connection between the DMC and PD controllers also serves as communication channel for the Connection and Power Manager.

The USB4 Hub Controller manages the data paths for all of the Type-C ports and determines the required data protocol by reading the PD controller status over I2C connection. The UFP port is the main connection to the USB4 Hub Controller from a USB4 host. The other DFP ports act as expansion ports to connect other USB Type-C & PD devices.

The UFP Variable Power Supply provides 5 V/9 V/15 V/20 V up to 100 W to charge the connected USB4 host. The TPS55288 is used in this application since it is capable of tightly regulating the output voltage and current. The TPS55288 is best connected to the I2C Host on the Primary PD controller, to set the output voltage and current regulation. The other DFP ports generally support 5 V @ 3 A to connect to Type-C & PD devices.

9.2.1.1 Design Requirements

9.2.1.1.1 Power Supply Design Requirements

Table 9-1 shows the Power Design parameters for the USB4 Device application.

Table 9-1. Power Supply Design Requirements

POWER DESGIN PARAMETERS	VALUE	CURRENT PATH
UFP Source Port A	5 V/9 V/15 V/20 V @ 5 A	Host Charging VBUS
DFP Source Port B/C/D	5 V @ 9 A (3 A per port)	DFP VBUS
PP_CABLE Port A/B/C/D	5 V @ 2 A (500 mA per port)	VCONN Source
DMC External Input Path	20 V @ 10 A (Imax sensed)	USB4 Device Input Power
VIN_3V3 PD Controller & DMC	3.3 V @ 150 mA (50 mA per device)	PD Controller & DMC Power

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 USB Power Delivery Source Capabilities

Table 9-2 summarizes the source PDOs for all of the ports for the USB4 Device.

Table 9-2. Source Capabilities

PORT	PDO TYPES	VOLTAGE	CURRENT
Port A	Fixed	5 V/9 V/15 V/20 V	3 A/3 A/3 A/5 A
Port B	Fixed	5 V	3 A
Port C	Fixed	5 V	3 A
Port D	Fixed	5 V	3 A

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9.2.1.2.2 USB Power Delivery Sink Capabilities

The UFP Source port is the only DRP port that may connect as a DFP or UFP which means that it should have at least one sink capability when connected as a UFP. The DFP ports can only connect as a DFP, where they do not have any sink capabilities.

Table 9-3. Sink Capabilities

PORT	PDO TYPES	VOLTAGE	CURRENT
Port A	Fixed	5 V	0 A

9.2.1.2.3 Supported Data Modes

USB4 Hub Controllers may vary on the data supported on the UFP and DFP ports. In this specific example the USB4 Hub Controllers support USB3, DisplayPort, Thunderbolt, and USB4 on the UFP Port. The DFP Ports will also support these modes when connected to other Type-C & PD devices.

Table 9-4. Data Modes

MODE OF OPERATION	DATA	DATA ROLE
USB Data	USB3.1 Gen2	UFP: Device, DFP: Host
DisplayPort	DP Video	UFP: UFP_D, DFP: DFP_D
Thunderbolt	PCIe/DP Video	UFP: Host/Device, DFP: Host
USB4	Tunneled USB3/PCIe/DP	UFP: Device, DFP Host

9.2.1.2.4 USB4 Hub Controller & PD Controller I2C Communication

The I2C connection from the PD controllers and the USB4 Hub Controller communicates the connection present at the Type-C Ports. Each port on the USB4 controller may have its I2C interrupt pin to notify the USB4 Hub Controller which port has a new connection. The PD controllers have an option to use the shared interrupt for both ports or to have a separate interrupt for each port that is mapped to a GPIO in its configuration. In the shared interrupt case, the USB4 Hub Controller will query both port addresses and will determine which port has a data connection. For the dedicated interrupt the USB4 hub controller will only query the specific port address and determine the connection present.

Figure 9-2 shows the dedicated GPIO interrupt connection.

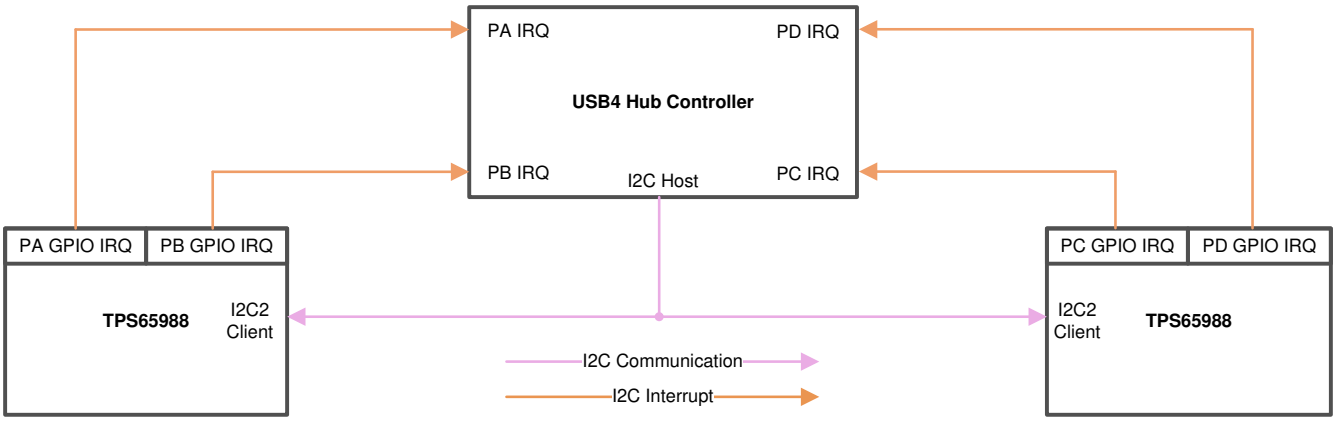

Figure 9-2. Dedicated Interrupts for USB4 Hub

Figure 9-3 shows the shared interrupt connection on I2C2_IRQ.

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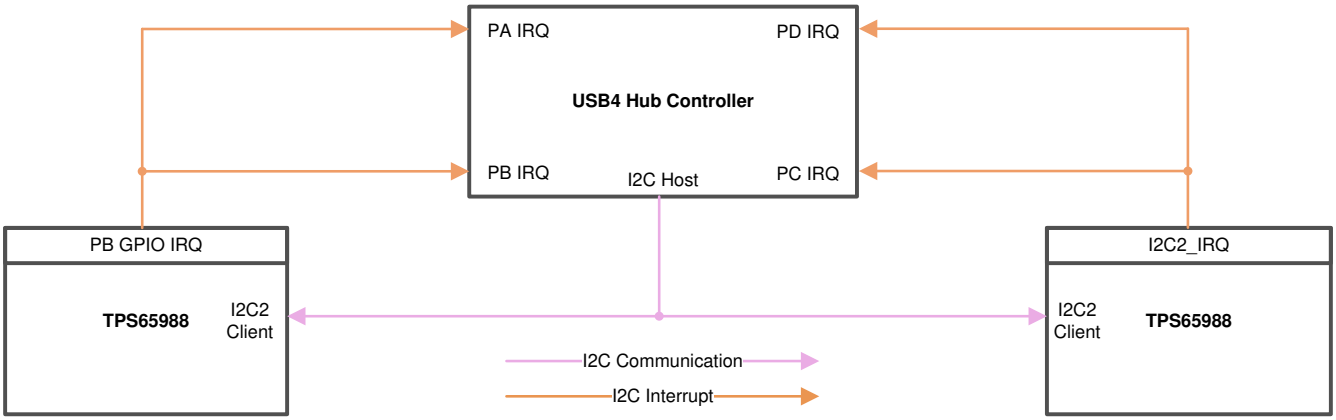

Figure 9-3. Shared Interrupts for USB4 Hub

Table 9-5 shows an example of the port I2C addresses for each of the PD controller ports.

Table 9-5. Recommended I2C Addresses - Hub Controller

PORT	I2C ADDRESS
Port A	0x38
Port B	0x3F
Port C	0x48
Port D	0x4F

9.2.1.2.5 Dock Management Controller & PD Controller I2C Communication

The I2C connection from the PD controllers and the Dock Management Controller communicates to boot up the PD controllers and enable the Connection & Power Manager functions. The DMC has two GPIO dedicated for Port A/B and Port C/D interrupts. The shared interrupt connection to the Dock Management Controller will query both port addresses and will determine which port has been updated.

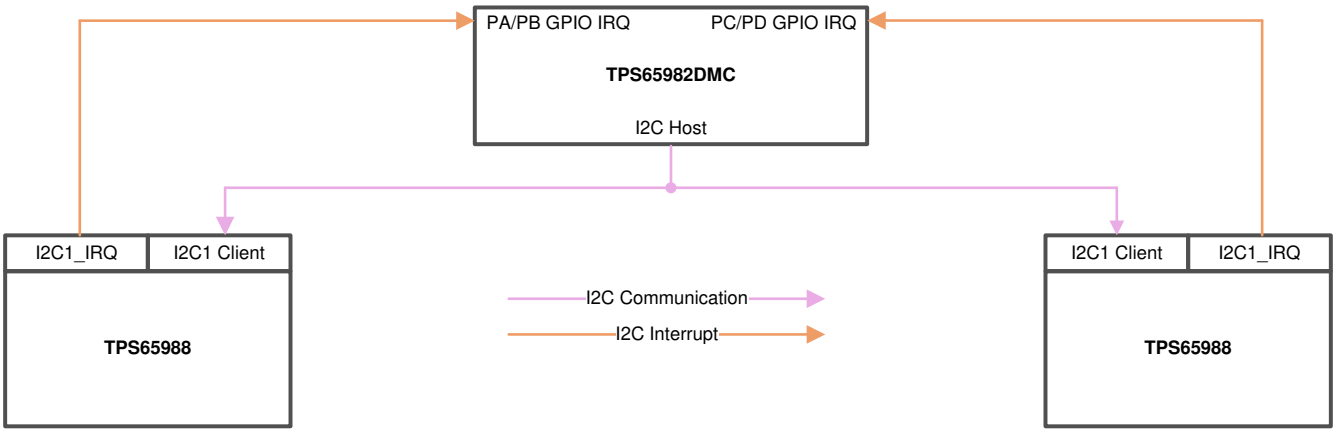

Figure 9-4. Interupt Configuration for DMC

Table 9-6 shows and example of the port I2C address for each of the PD controller ports.

Table 9-6. Recommended I2C Addresses - DMC

PORT	I2C ADDRESS
Port A	0x20
Port B	0x24
Port C	0x21

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Table 9-6. Recommended I2C Addresses - DMC (continued)

PORT	I2C ADDRESS
Port D	0x25

9.2.1.2.6 SPI Flash Options

The TPS65982DMC is connected to the SPI Flash which contains the firmware for the DMC and the PD controllers connected. Table 9-7 shows the supported SPI flash options.

Table 9-7. SPI Flash Options

MANUFACTURER	PART NUMBER	SIZE
Winbond	W25Q80JVNIQ	8 Mb
Spansion	S25FL208K	8 Mb
AMIC	A25L080	8 Mb
Macronix	MX25L8006EM1I	8 Mb
Micron	M25PE80-VMN6TP	8 Mb
Micron	M25PX80-VMN6TP	8 Mb

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10 Power Supply Recommendations

10.1 3.3-V Power

10.1.1 VIN_3V3 Input Switch

The VIN_3V3 input is the main supply to the TPS65987DDK device. The VIN_3V3 switch (see Figure 8-9) is a unidirectional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when 3.3 V is available. See Table 10-1 for the recommended external capacitance on the VIN_3V3 pin.

10.1.2 VBUS 3.3-V LDO

The 3.3-V LDO from VBUS steps down voltage from VBUS to LDO_3V3 which allows the TPS65987DDK device to be powered from VBUS when VIN_3V3 is unavailable. This LDO steps down any recommended voltage on the VBUS pin. When VBUS is 20 V, as is allowable by USB PD, the internal circuitry of the TPS65987DDK device operates without triggering thermal shutdown; however, a significant external load on the LDO_3V3 pin can increase the temperature enough to trigger a thermal shutdown. The VBUS 3.3-V LDO blocks reverse current from LDO_3V3 back to VBUS allowing VBUS to be unpowered when LDO_3V3 is driven from another source. See Table 10-1 for the recommended external capacitance on the VBUS and LDO_3V3 pins.

10.2 1.8-V Power

The internal circuitry is powered from 1.8 V. The 1.8-V LDO steps the voltage down from LDO_3V3 to 1.8 V. The 1.8-V LDO provides power to all internal low-voltage digital circuits which includes the digital core, memory and other digital circuits. The 1.8-V LDO also provides power to all internal low-voltage analog circuits. See Table 10-1 for the recommended external capacitance on the LDO_1V8 pin.

10.3 Recommended Supply Load Capacitance

Table 10-1 lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

Table 10-1. Recommended Supply Load Capacitance

PARAMETER	DESCRIPTION	VOLTAGE RATING	CAPACITANCE		
			MIN (ABSOLUTE)	TYP (PLACED)	MAX (ABSOLUTE)
CVIN_3V3	Capacitance on VIN_3V3	6.3 V	5 µF	10 µF	
CLDO_3V3	Capacitance on LDO_3V3	6.3 V	5 µF	10 µF	25 µF
CLDO_1V8	Capacitance on LDO_1V8	4 V	2.2 µF	4.7 µF	12 µF
CVBUS1	Capacitance on VBUS1	25 V	0.5 µF	1 µF	12 µF
CVBUS2	Capacitance on VBUS2	25 V	0.5 µF	1 µF	12 µF
CPP_HV_SRC	Capacitance on PP_HV when configured as a 5-V source	10 V	2.5 µF	4.7 µF	
CPP_HV_SNK	Capacitance on PP_HV when configured as a 20-V sink	25 V	1 µF	47 µF	120 µF
CPP_CABLE	Capacitance on PP_CABLE. When shorted to PP_HV congifured as a 5-V source, the CPP_HV_SRC capacitance may be shared.	10 V	2.5 µF	4.7 µF	

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11 Layout

11.1 Layout Guidelines

Proper routing and placement will maintain signal integrity for high speed signals and improve the heat dissipation from the TPS65987DDK power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. It is a best practice to consult with board manufacturing to verify manufacturing capabilities.

11.1.1 Top TPS65987DDK Placement and Bottom Component Placement and Layout

When the TPS65987DDK is placed on top and its components on bottom the solution size will be at its smallest.

11.2 Layout Example

Follow the differential impedances for Super and High Speed signals defined by their specifications (DisplayPort - AUXN/P and USB2.0). All I/O will be fanned out to provide an example for routing out all pins, not all designs will use all of the I/O on the TPS65987DDK.

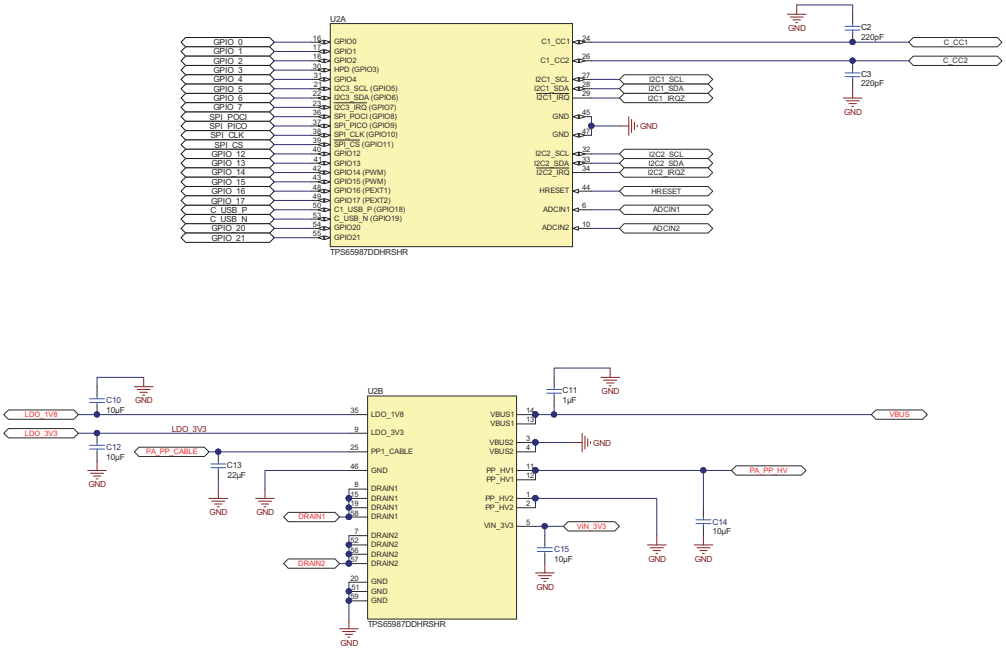

Figure 11-1. Example Schematic

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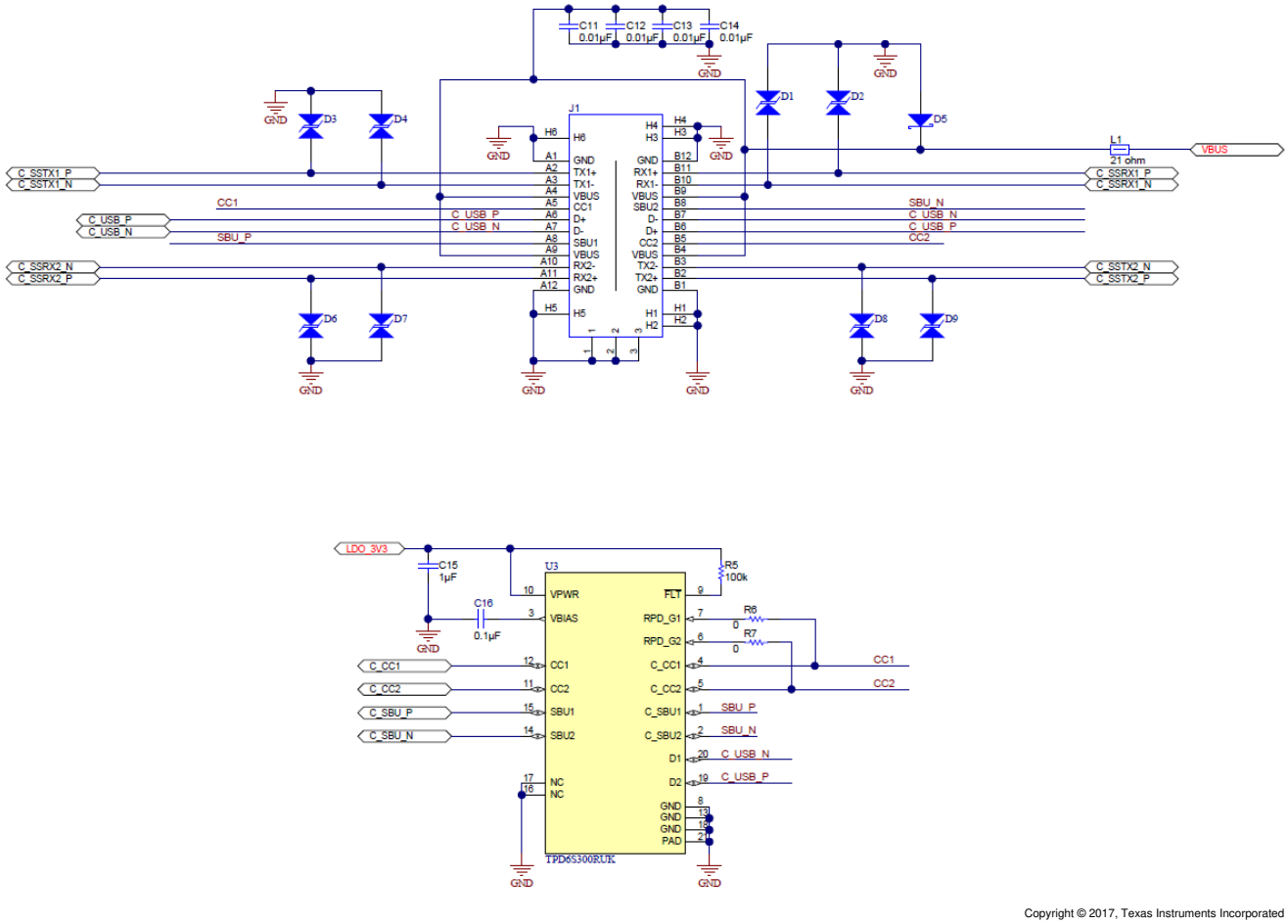

Figure 11-2. Example Schematic2

11.3 Component Placement

Top and bottom placement is used for this example to minimize solution size. The TPS65987DDK is placed on the top side of the board and the majority of its components are placed on the bottom side. When placing the components on the bottom side, it is recommended that they are placed directly under the TPS65987DDK. When placing the VBUS and PPHV capacitors it is easiest to place them with the GND terminal of the capacitors to face outward from the TPS65987DDK or to the side since the drain connection pads on the bottom layer should not be connected to anything and left floating. All other components that are for pins on the GND pad side of the TPS65987DDK should be placed where the GND terminal is underneath the GND pad.

The CC capacitors must be placed on the same side as the TPS65987DDK close to the respective CC1 and CC2 pins. Do NOT via to another layer in between the CC pins to the CC capacitor, placing a via after the CC capacitor is recommended.

The ADCIN1/2 voltage divider resistors can be placed where convenient. In this layout example they are placed on the opposite layer of the TPS65987DDK close to the LDO_3V3 pin to simplify routing.

The figures below show the placement in 2-D and 3-D.

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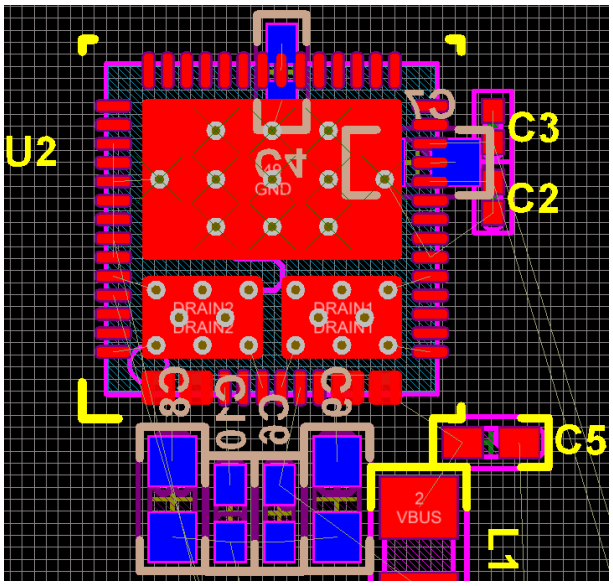

Figure 11-3. Top View Layout

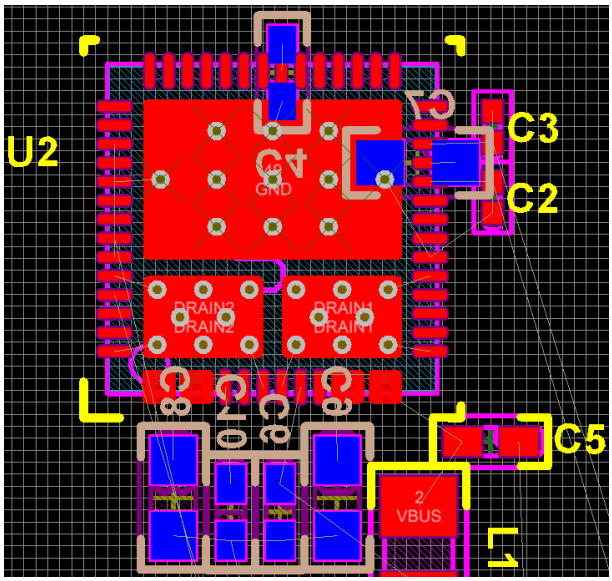

Figure 11-4. Bottom View Layout

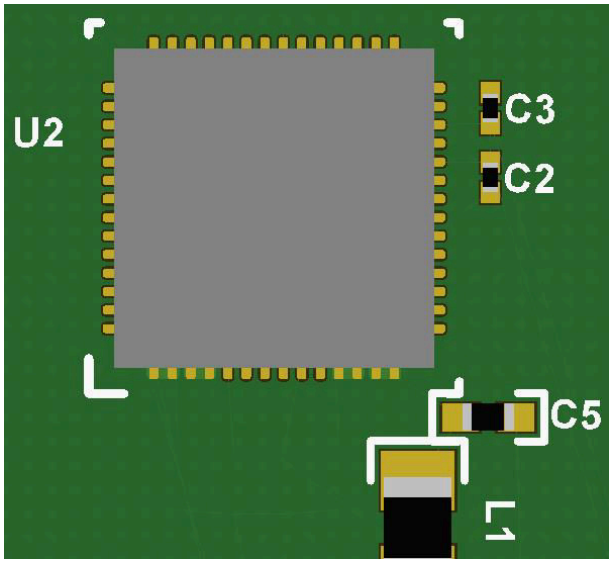

Figure 11-5. Top View 3-D

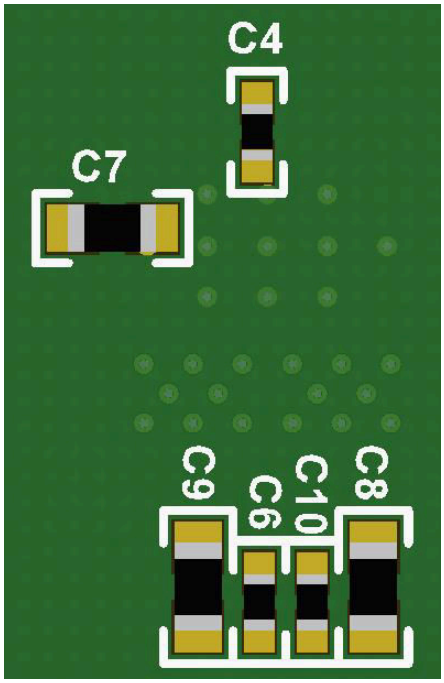

Figure 11-6. Bottom View 3-D

11.4 Routing PP_HV1/2, VBUS, PP_CABLE, VIN_3V3, LDO_3V3, LDO_1V8

On the top side, create pours for PP_HV1/2 and VBUS1/2 to extend area to place 8-mil hole and 16-mil diameter vias to connect to the bottom layer. See the figure below for the recommended via sizing.

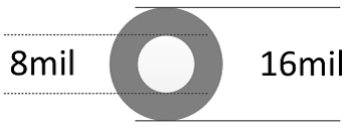

Figure 11-7. Recommended Minimum Via Sizing

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A minimum of four vias should be used to connect between the top and bottom layer power paths. For the bottom layer, place pours that will connect the PP_HV1/2 and VBUS capacitors to their respective vias. For 5-A systems, special consideration must be taken for ensuring enough copper is used to handle the higher current. For 0.5-oz copper, top or bottom pours, with 0.5-oz plating will require about 120-mil pour width for 5-A support. When routing the 5 A through a 0.5-oz internal layer, more than 200 mil will be required to carry the current.

The figures below show the pours used in this example.

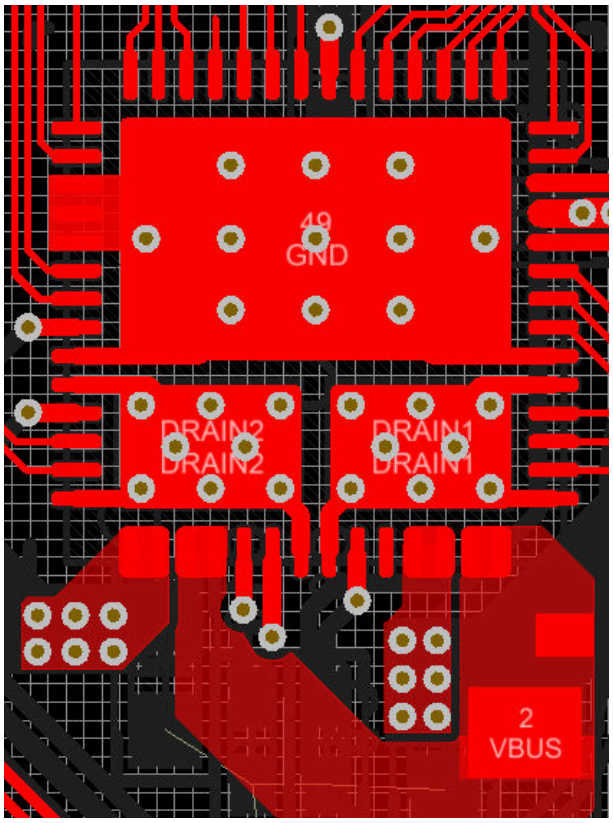

Figure 11-8. Top Polygon Pours

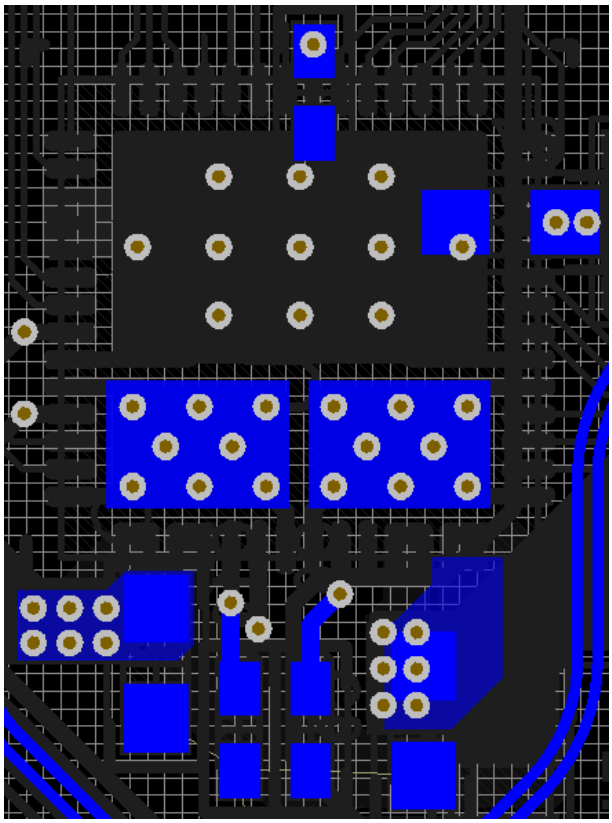

Figure 11-9. Bottom Polygon Pours

For PP_CABLE, it is recommended to connect the capacitor to the pin with two vias. They should be placed side by side and as close to the pin as possible to allow for routing the CC lines.

Connect the bottom side VIN_3V3 and LDO_3V3 capacitors with traces through a via. The vias should have a straight connection to the respective pins. LDO_1V8 is connected through a via on the outside of the pin and connected with a trace on the bottom side capacitor.

11.5 Routing CC and GPIO

Routing the CC lines with a 8-mil trace will ensure the needed current for supporting powered Type-C cables through VCONN. For more information on VCONN refer to the Type-C specification. For capacitor GND pin use a 16-mil trace if possible.

Most of the GPIO signals can be fanned out on the top layer with a 4-mil trace. The PP_EXT1/2 GPIO control go through a via to be routed on another layer.

Figure 11-10 below shows the CC and GPIO routing.

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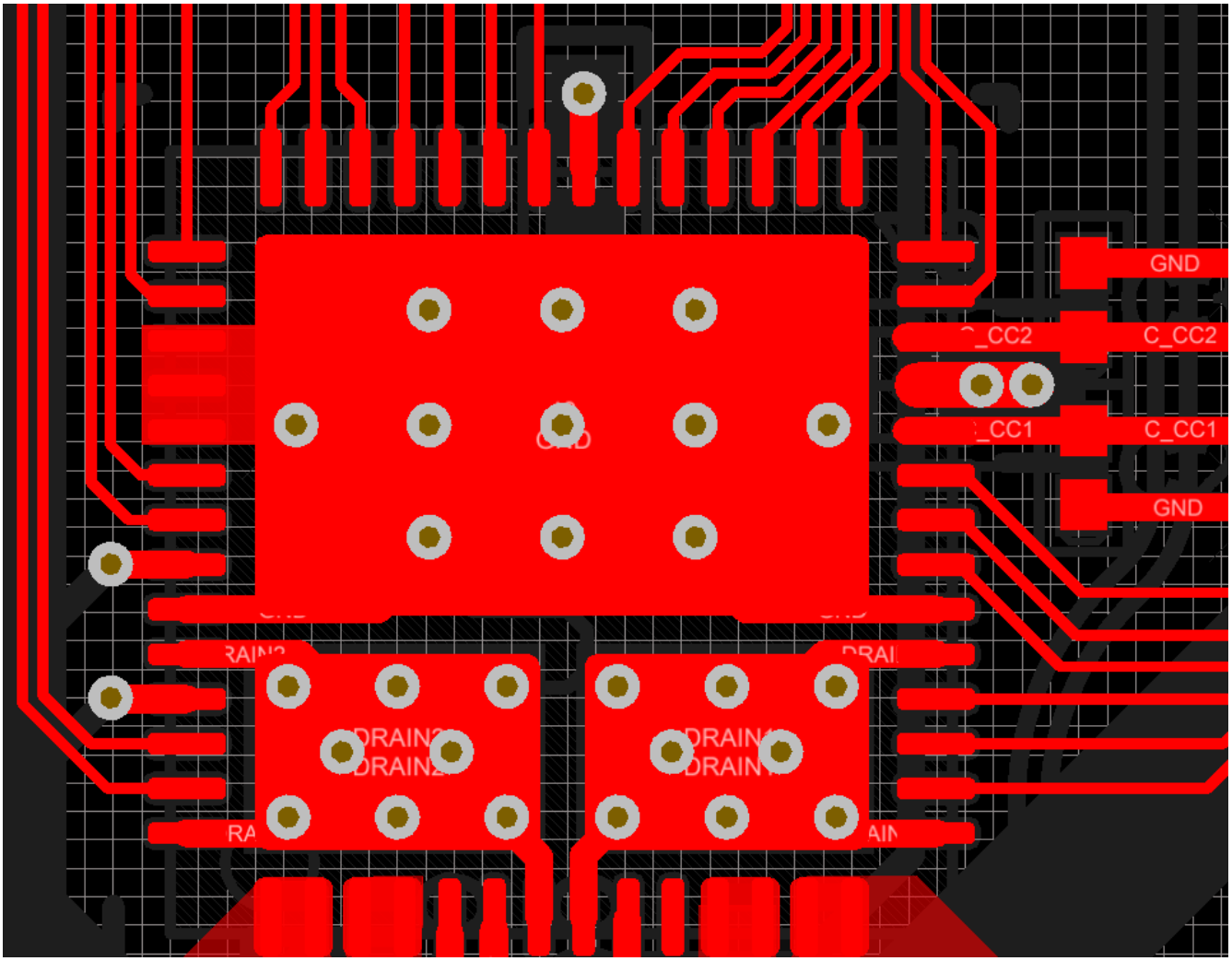

Figure 11-10. CC Routing and GPIO Fan-Out

Table 11-1. Routing Widths

ROUTE	WIDTH (mil minimum)
CC1, CC2, PP_CABLE1, PP_CABLE2	8
VIN_3V3, LDO_3V3, LDO_1V8	6
Component GND	10
GPIO	4

11.6 Thermal Dissipation for FET Drain Pads

The TPS65987DDK contains two internal FETs. To assist with thermal dissipation of these FETs, the drains of the FETs are connected to two metal pads underneath the IC. When completing a board layout for the TPS65987DDK, it is important to provide copper pours on the top and bottom layer of the PCB for the thermal pads of each FET.

When looking at the footprint for the TPS65987DDK, pins 57 and 58 are two smaller pads underneath the device. These are the drain pads for the two internal FETs. The dimensions are 1.75 mil x 2.6 mil and 1.75 mil x 2.55 mil for pins 57 and 58 respectively. Each of these FET pads should contain a minimum of six thermal vias through the PCB. This layout example contains 8 thermal vias through the PCB. On the bottom side of the PCB, the 1.75 mil x 2.6 mil and 1.75 mil x 2.55 mil thermal pads are mirrored to assist with thermal dissipation.

The figures below show the copper fills for the FET Drain pads.

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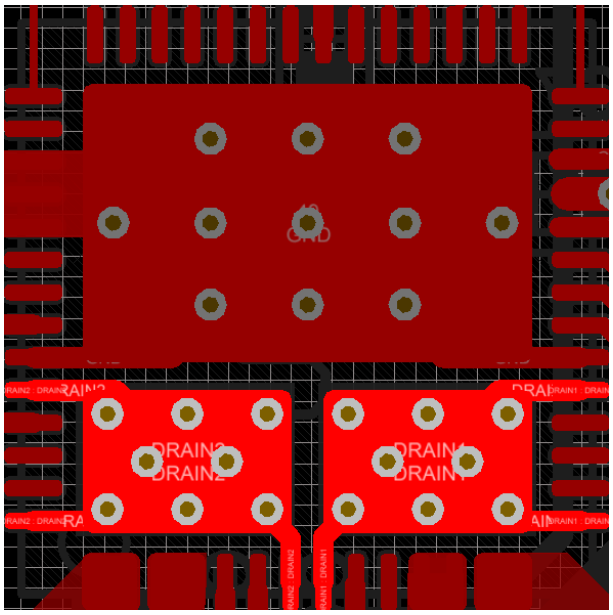

Figure 11-11. Top Layer FET Pads

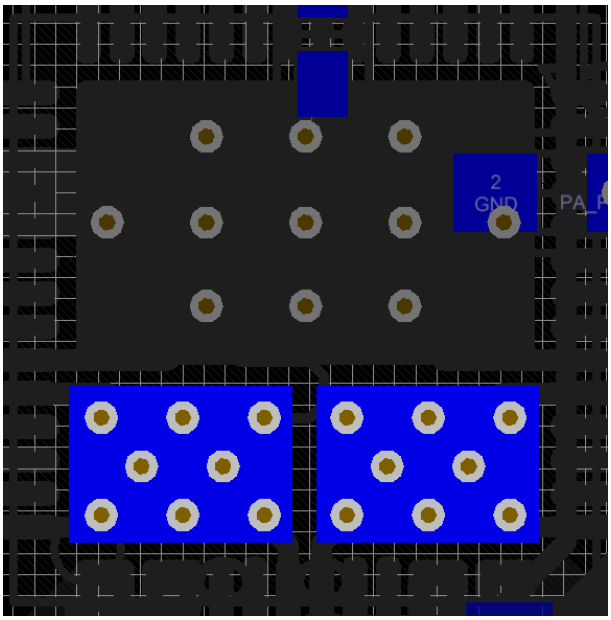

Figure 11-12. Bottom Layer FET Pads

As seen in the figures above, it is recommended to connect the Drain pins to their respective Drain pads underneath the IC. This will help with thermal dissipation by moving some of the heat away from the device. To further assist with thermal dissipation, it is possible to add copper fins on the top layer for both of the FET Drain Pads. When calculating the relative thermal dissipation, the first 3 mm of copper away from the device contribute largely to the thermal performance. Once the copper expands beyond 3 mm from the IC, there are diminishing returns in thermal performance.

Figure 11-13 highlights an example with copper fins to improve thermal dissipation.

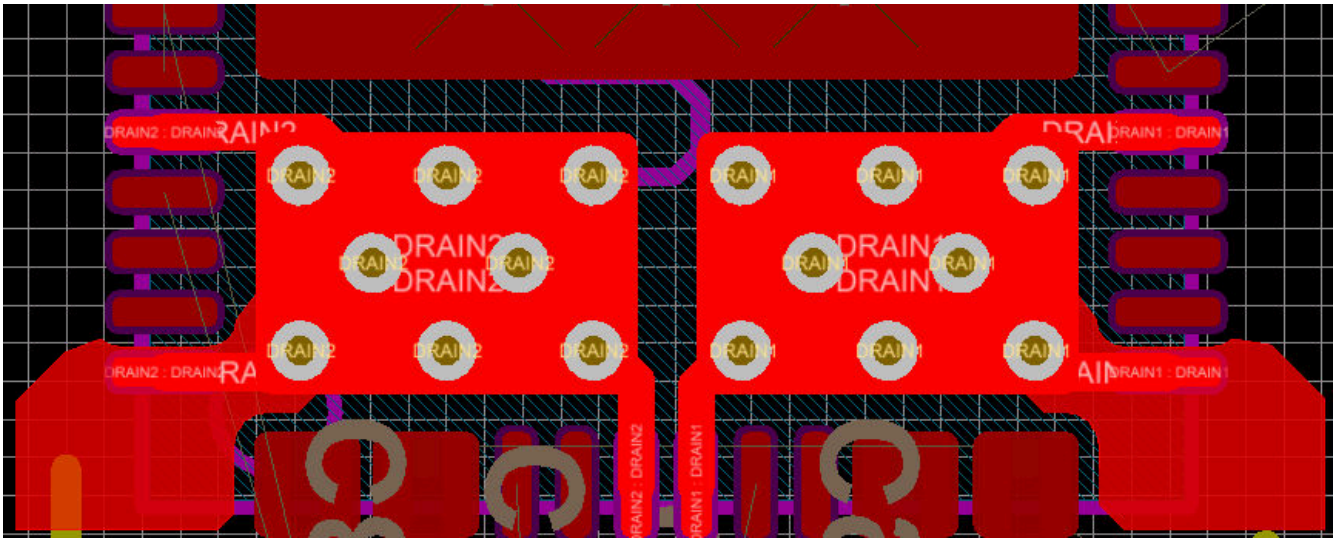

Figure 11-13. Copper Fins on Drain Pad

The thermal vias under each of the FET Drain Pads should be filled. Filling the vias will greatly improve the thermal dissipation on the FETs as there is significantly more copper that is connecting the top layer pad to the bottom layer copper. Alternatively, the vias can be epoxy filled but they will have higher thermal resistance. Each 8-/16-mil to 10-/20-mil via could have a thermal resistance ranging from 175°C/W to 200°C/W with board manufacturing variation. When doing thermal calculations it is recommended to use the worst case 200°C/W

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which will give a set of six vias a thermal resistance of approximately 33°C/W from the top to bottom pad. The vias in the FET pads should only be connected to copper pads on the top and bottom layers of the PCB. These should not be connected to GND. Refer to the image below to see which layers should be connected for the GND vias and FET Pad vias.

Figure 11-7 shows a common stack-up for systems that require Super Speed and high power routing.

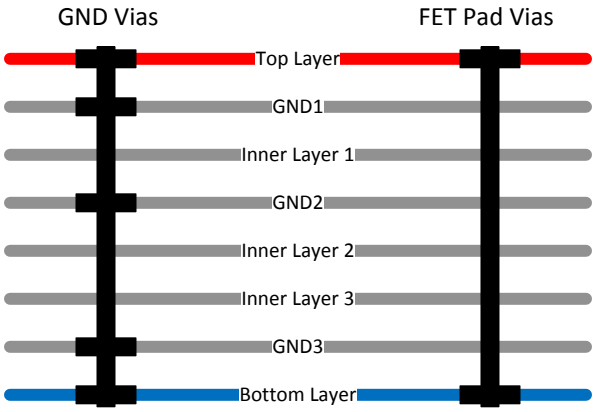

Figure 11-14. PCB Stack-Up

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Firmware Warranty Disclaimer

IN ORDER FOR THE TPS6598X DEVICE TO FUNCTION IN ACCORDANCE WITH THIS SPECIFICATIONS, YOU WILL NEED TO DOWNLOAD THE LATEST VERSION OF THE FIRMWARE FOR THE DEVICE. IF YOU DO NOT DOWNLOAD AND INCORPORATE THE LATEST VERSION OF THE FIRMWARE INTO THE DEVICE, THEN THE DEVICE IS PROVIDED “AS IS” AND TI MAKES NO WARRANTY OR REPRESENTATION WHATSOEVER IN RESPECT OF SUCH DEVICE, AND DISCLAIMS ANY AND ALL WARRANTIES AND REPRESENTATIONS WITH RESPECT TO SUCH DEVICE. FURTHER, IF YOU DO NOT DOWNLOAD AND INCORPORATE THE LATEST VERSION OF THE FIRMWARE INTO THE DEVICE, TI WILL NOT BE LIABLE FOR AND SPECIFICALLY DISCLAIMS ANY DAMAGES, INCLUDING DIRECT DAMAGES, HOWEVER CAUSED, WHETHER ARISING UNDER CONTRACT, TORT, NEGLIGENCE, OR OTHER THEORY OF LIABILITY RELATING TO THE DEVICE, EVEN IF TI IS ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

12.2 Documentation Support

12.2.1 Related Documentation

- *TUSB1064 USB TYPE-C™ DP Alt Mode 10 Gbps Sink-Side Linear Redriver Crosspoint Switch* data sheet

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65987DDKRSHR	NRND	Production	VQFN (RSH) | 56	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-10 to 75	T65987D DK
TPS65987DDKRSHR.A	NRND	Production	VQFN (RSH) | 56	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-10 to 75	T65987D DK
TPS65987DDKRSHR.B	NRND	Production	VQFN (RSH) | 56	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-10 to 75	T65987D DK

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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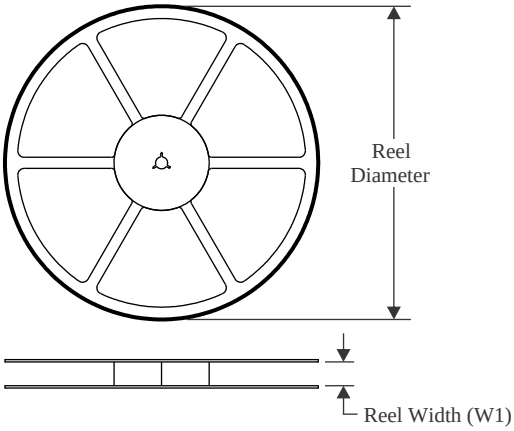
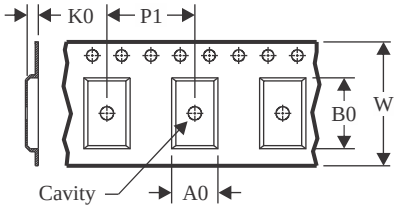
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

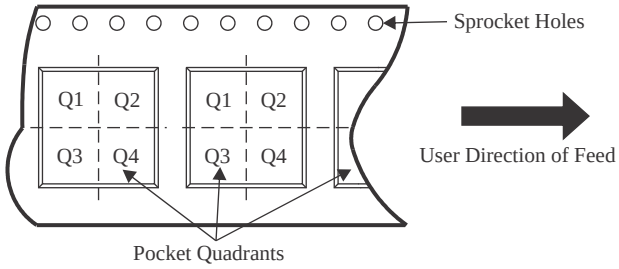


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

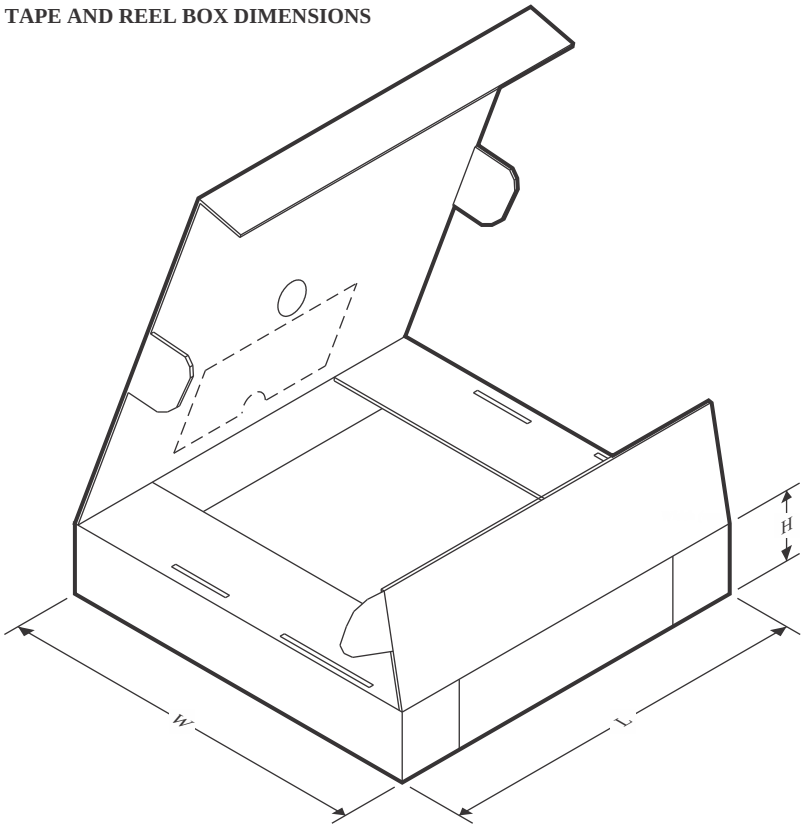
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65987DDKRSHR	VQFN	RSH	56	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

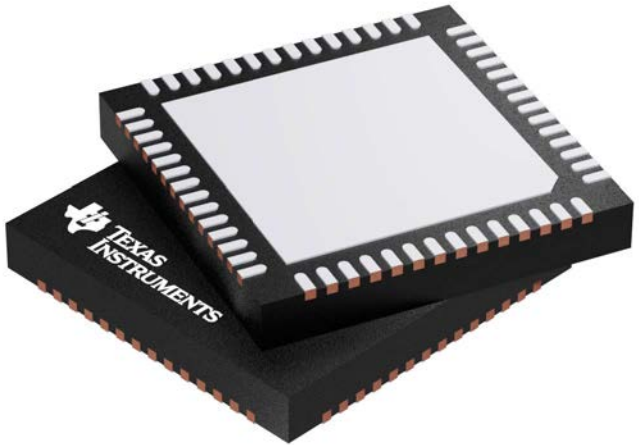
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65987DDKRSHR	VQFN	RSH	56	2500	367.0	367.0	38.0

GENERIC PACKAGE VIEW

RSH 56

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

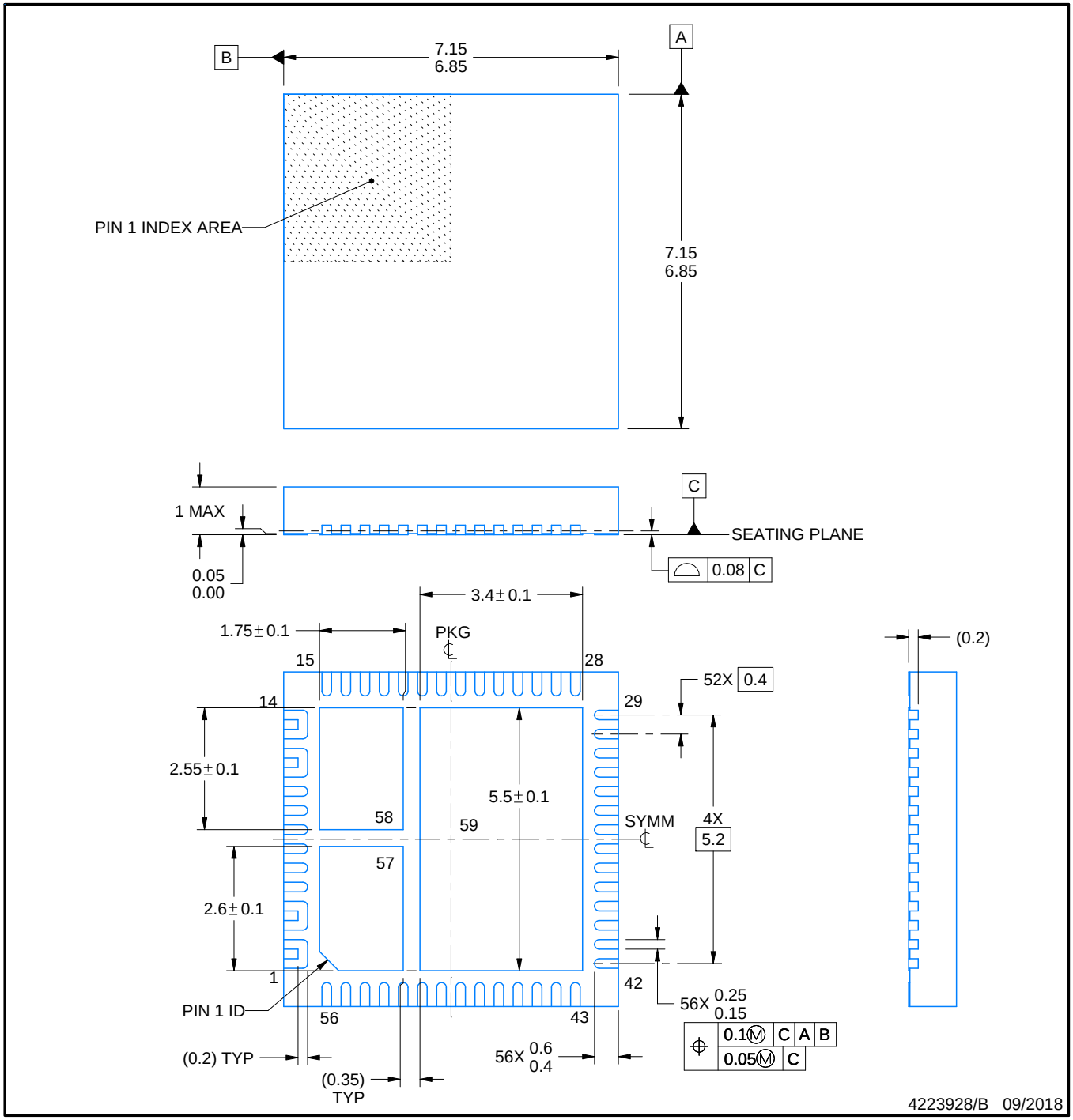
4207513/D

PACKAGE OUTLINE

RSH0056E

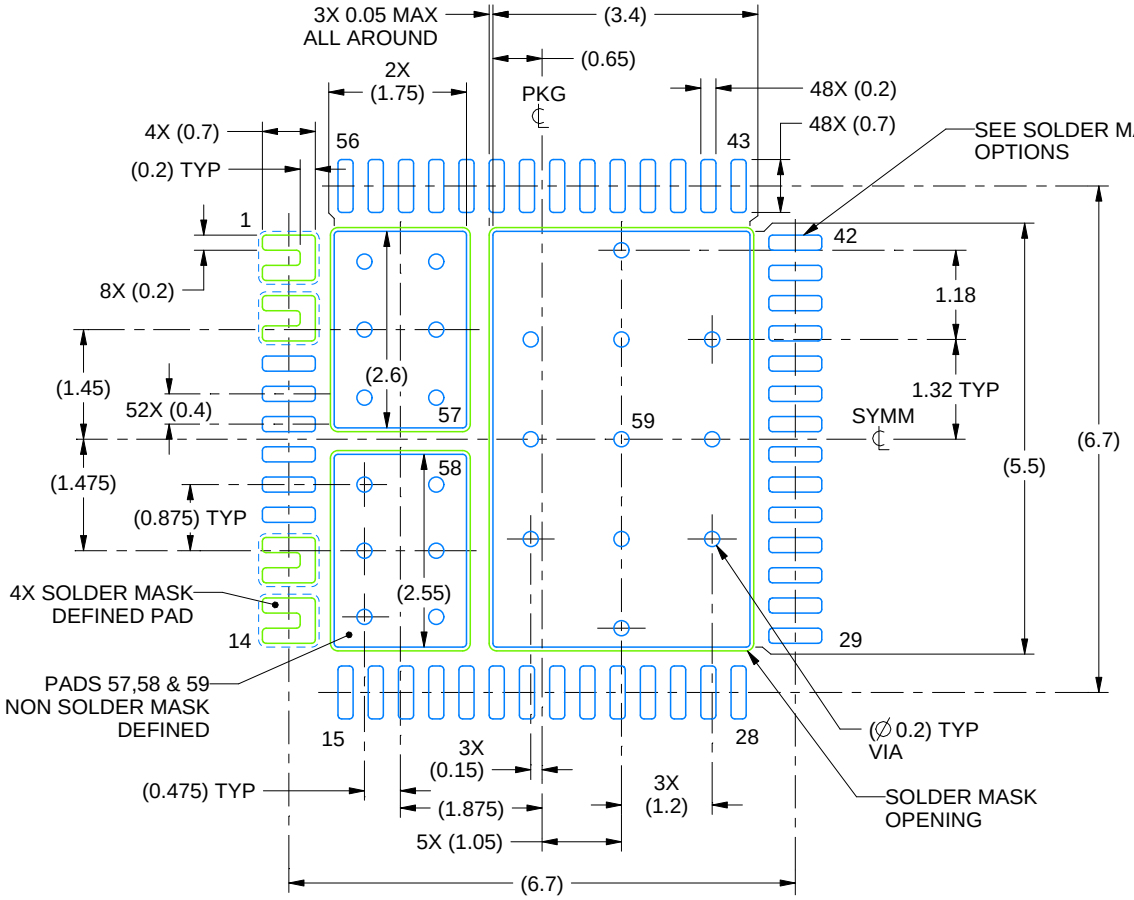
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

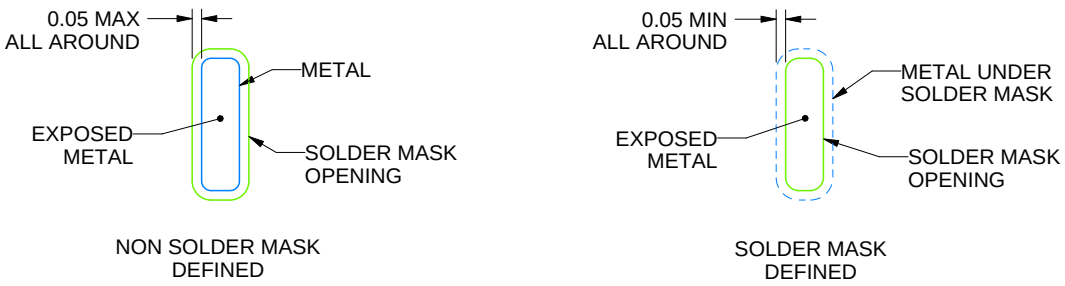


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

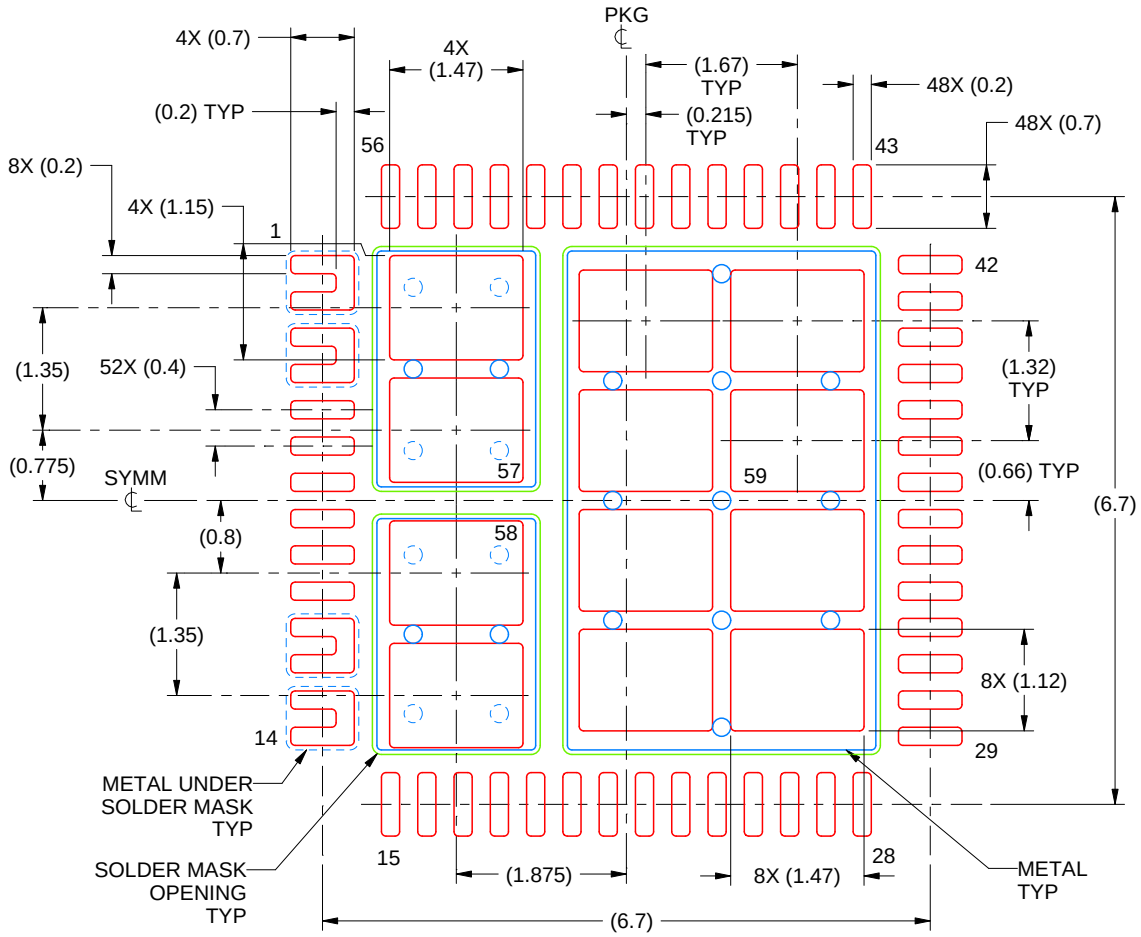


SOLDER MASK OPTIONS
NOT TO SCALE

4223928/A 09/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL

EXPOSED PAD PRINTED SOLDER COVERAGE BY AREA
PAD 57 & 58: 75%
PAD 59: 70%
SCALE: 12X

4223928/B 09/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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