

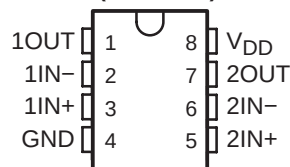
LinCMOS™ DUAL DIFFERENTIAL COMPARATOR

TLC352

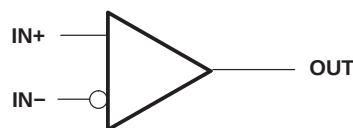
SLCS016A – SEPTEMBER 1985 – REVISED SEPTEMBER 2002

- Single- or Dual-Supply Operation
- Wide Range of Supply Voltages
1.5 V to 18 V
- Very Low Supply Current Drain
150 μ A Typ at 5 V
65 μ A Typ at 1.4 V
- Built-In ESD Protection
- High Input Impedance . . . $10^{12} \Omega$ Typ
- Extremely Low Input Bias Current 5 pA Typ
- Ultrastable Low Input Offset Voltage
- Input Offset Voltage Change at Worst-Case
Input Conditions Typically 0.23 μ V/ Month,
Including the First 30 Days
- Common-Mode Input Voltage Range
Includes Ground
- Outputs Compatible With TTL, MOS, and
CMOS
- Pin-Compatible With LM393

TLC352C, TLC352I . . . D OR P PACKAGE
(TOP VIEW)



symbol (each comparator)



description

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 1.4 V to 18 V. Each device features extremely high input impedance (typically greater than $10^{12} \Omega$), which allows direct interface to high-impedance sources. The output are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC352 to operate from 1.4-V supply makes this device ideal for low-voltage battery applications.

The TLC352 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC352C is characterized for operation from 0°C to 70°C. The TLC352I is characterized for operation over the industrial temperature range of – 40°C to 85°C.

AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGE	
		SMALL-OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC352CD	TLC352CP
– 40°C to 85°C	5 mV	TLC352ID	TLC352IP

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC352 CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



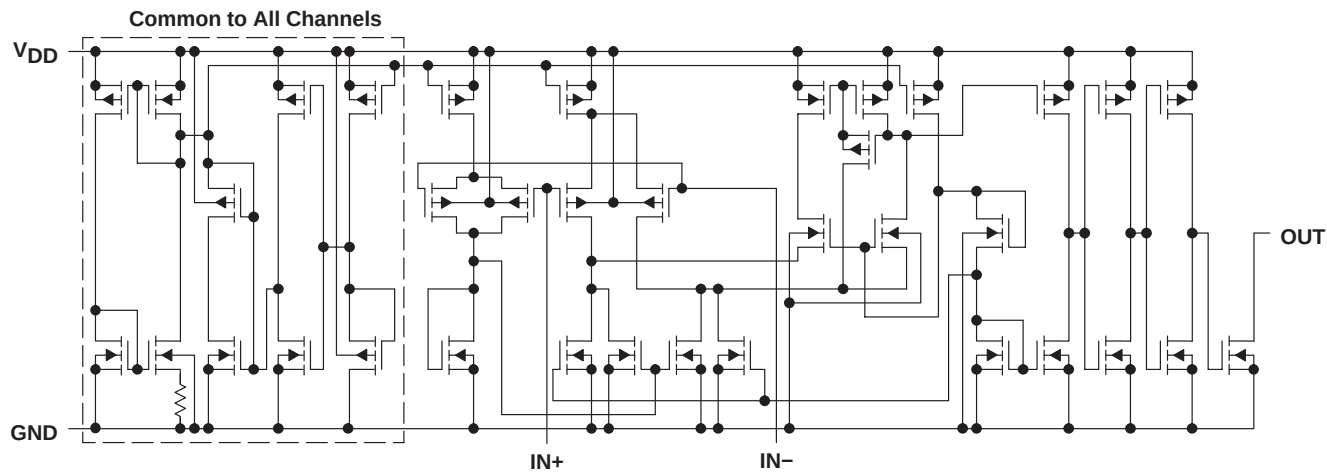
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TLC352
LinCMOS™ DUAL DIFFERENTIAL COMPARATOR

SLCS016A – SEPTEMBER 1985 – REVISED SEPTEMBER 2002

equivalent schematic (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Table with 2 columns: Parameter and Rating. Rows include Supply voltage (VDD), Differential input voltage (VID), Input voltage (VI), Input voltage range, Output voltage (VO), Input current (II), Output current (IO), Duration of output short circuit, Continuous total dissipation, Operating free-air temperature range (TA) for TLC352C and TLC352I, Storage temperature range, and Lead temperature.

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

- NOTES: 1. All voltage values except differential voltages are with respect to the network ground.
- 2. Differential voltages are at IN+ with respect to IN-.
- 3. Short circuits from outputs to VDD can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

Table with 6 columns: PACKAGE, TA ≤ 25°C POWER RATING, DERATING FACTOR, DERATE ABOVE TA, TA = 70°C POWER RATING, TA = 85°C POWER RATING. Rows for D and P packages.

recommended operating conditions

	TLC352C		TLC352I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	1.4	16	1.4	16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5\text{ V}$				
	0	3.5	0	3.5	V
Operating free-air temperature, T_A	$V_{DD} = 10\text{ V}$				
	0	8.5	0	8.5	V
	0	70	-40	85	°C

electrical characteristics at specified free-air temperature, $V_{DD} = 1.4\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC352C			TLC352I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = V_{ICR} \text{ min, See Note 4}$	25°C	2	5	5	2	2	5	mV
		Full range			6.5			7	
I_{IO} Input offset current		25°C	1			1			pA
		MAX			0.3			1	nA
I_{IB} Input bias current		25°C	5			5			pA
		MAX			0.6			2	nA
V_{ICR} Common-mode input voltage range		Full range	0 to 0.2			0 to 0.2			V
V_{OL} Low-level output voltage		25°C	100	200	200	100	200	200	mV
		Full range			200			200	
I_{OL} Low-level output current	$V_{ID} = -0.5\text{ V, } V_{OL} = 0.3\text{ V}$	25°C	1	1.6		1	1.6		mA
I_{DD} Supply current (two comparators)	$V_{ID} = 0.5\text{ V, No load}$	25°C	65	150	150	65	150	150	μA
		Full range			200			200	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC352C, -40°C to 85°C for TLC352I. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kΩ resistor between the output and V_{DD} . They can be verified by applying the limit value to the input and checking for the appropriate output state.

TLC352

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC352C			TLC352I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = V_{ICR}$ min, See Note 5	25°C		1	5		1	5	mV
		Full range			6.5			7	
I_{IO} Input offset current		25°C		1			1		pA
		MAX			0.3			1	nA
I_{IB} Input bias current		25°C		5			5		pA
		MAX			0.6			2	nA
V_{ICR} Common-mode input voltage range		25°C	0 to $V_{DD} - 1$			0 to $V_{DD} - 1$			V
		Full range	0 to $V_{DD} - 1.5$			0 to $V_{DD} - 1.5$			
I_{OH} High-level output current	$V_{ID} = 1\text{ V}$	25°C		0.1			0.1		nA
	$V_{OH} = 5\text{ V}$								
	$V_{OH} = 15\text{ V}$	Full range			1			1	μA
V_{OL} Low-level output voltage	$V_{ID} = 1\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C		150	400		150	400	mV
		Full range			700			700	
I_{OL} Low-level output current	$V_{ID} = -1\text{ V}$, $V_{OL} = 1.5\text{ V}$	25°C	6	16		6	16		mA
I_{DD} Supply current (two comparators)	$V_{ID} = 1\text{ V}$, No load	25°C		0.15	0.3		0.15	0.3	mA
		Full range			0.4			0.4	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC352C, -40°C to 85°C for TLC352I. IMPORTANT: See Parameter Measurement Information.

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-k Ω resistor between the output and V_{DD} . They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLC352C, TLC352I			UNIT
		MIN	TYP	MAX	
Response time	R_L connected to 5 V through 5.1 k Ω , $C_L = 15\text{ pF}^\ddagger$, See Note 6				ns
	100-mV input step with 5-mV overdrive TTL-level input step		650	200	

‡ C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes state.

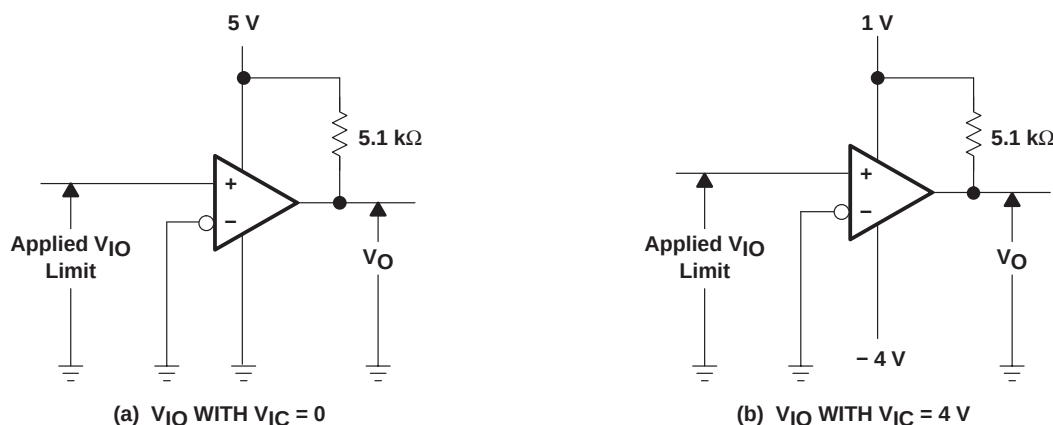


Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

PARAMETER INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

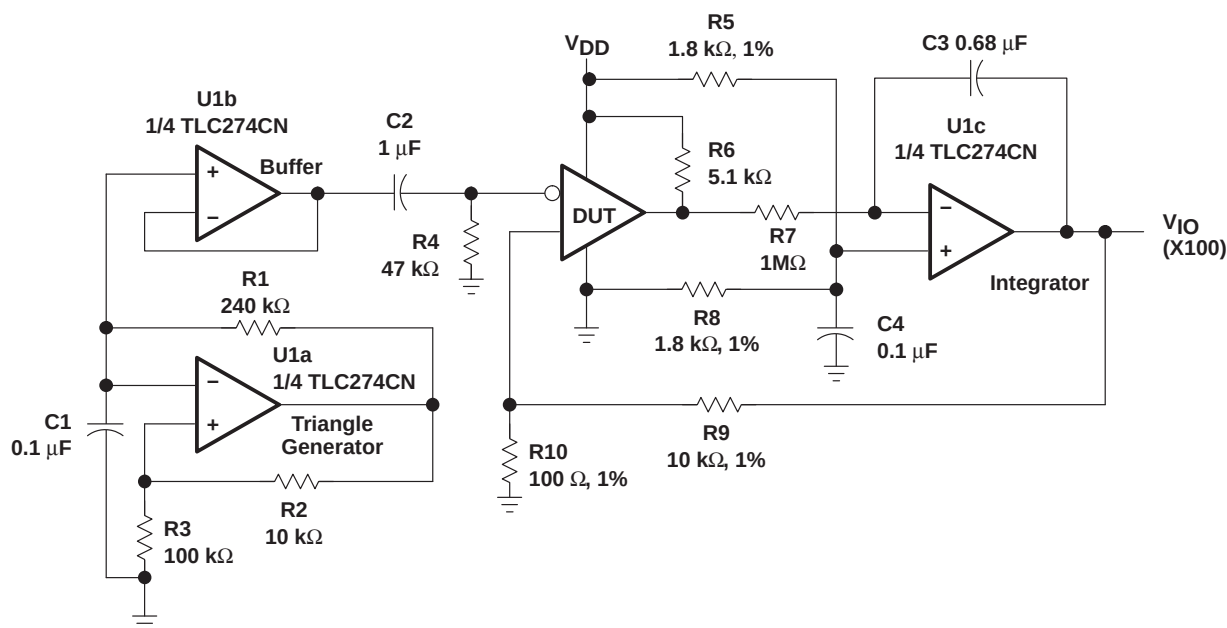
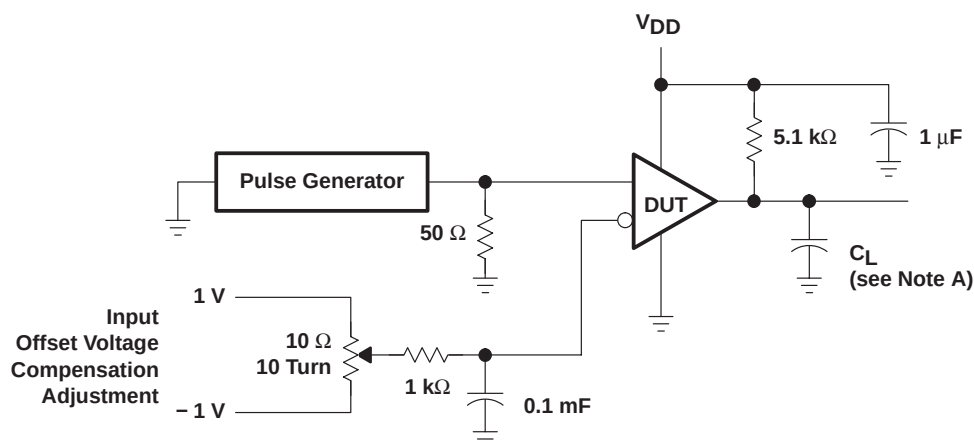


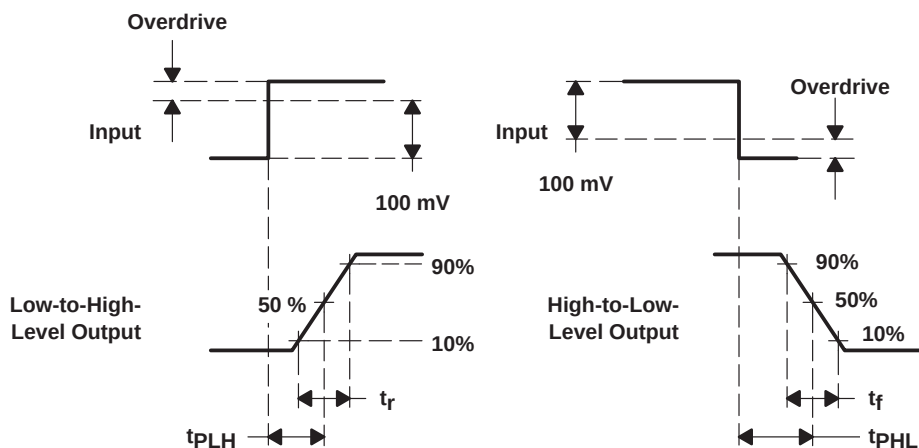
Figure 2. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 3. Response, Rise, and Fall Times Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC352CD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	352C
TLC352CDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	352C
TLC352CDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	352C
TLC352CP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC352CP
TLC352CP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC352CP
TLC352ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	352I
TLC352IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	352I
TLC352IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	352I
TLC352IDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLC352IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC352IP
TLC352IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC352IP
TLC352IPW	Obsolete	Production	TSSOP (PW) 8	-	-	Call TI	Call TI	-40 to 85	P352I
TLC352IPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	P352I
TLC352IPWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	P352I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

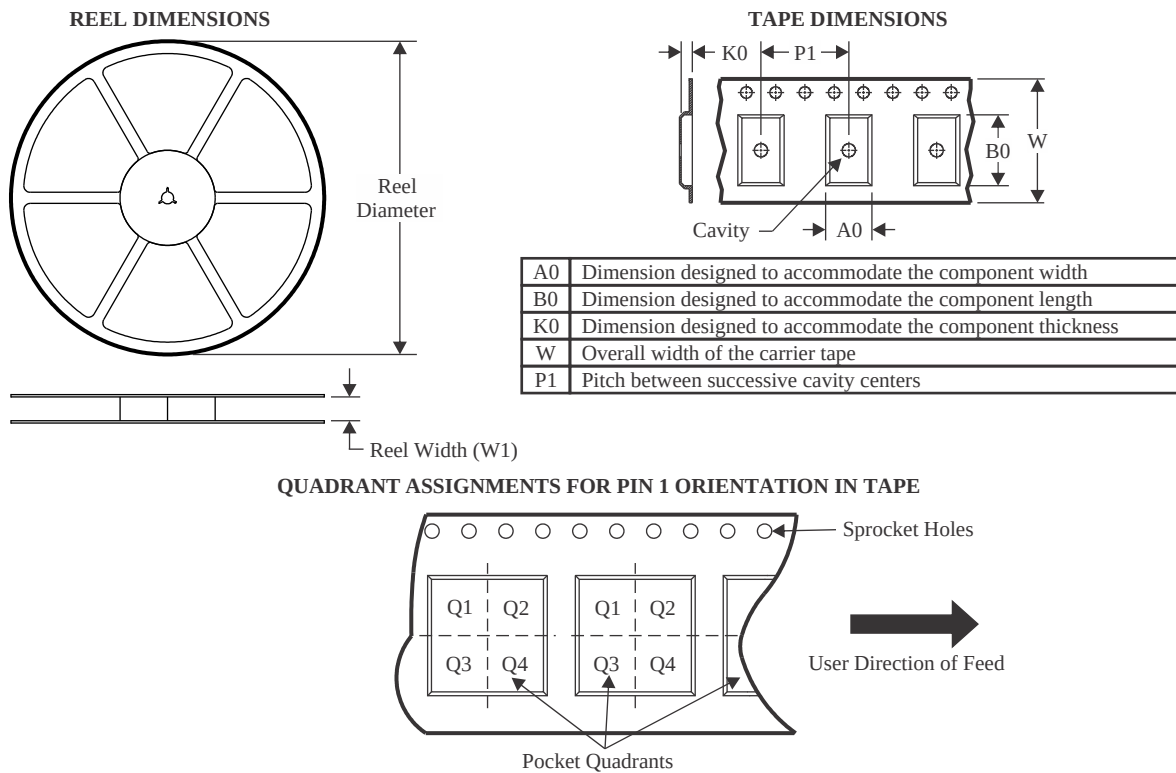
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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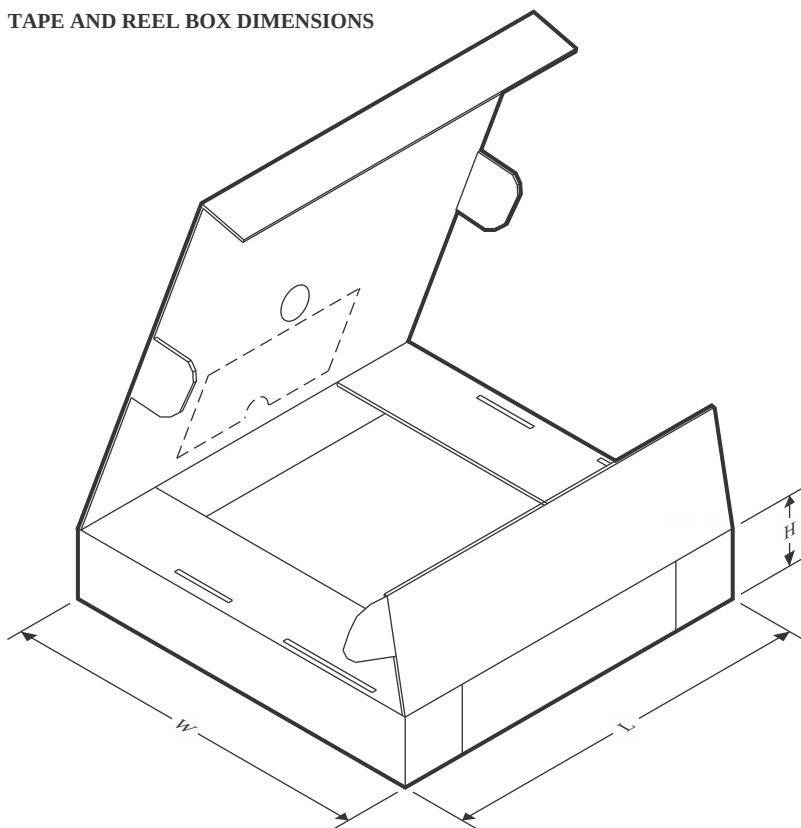
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC352CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC352IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC352IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC352IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

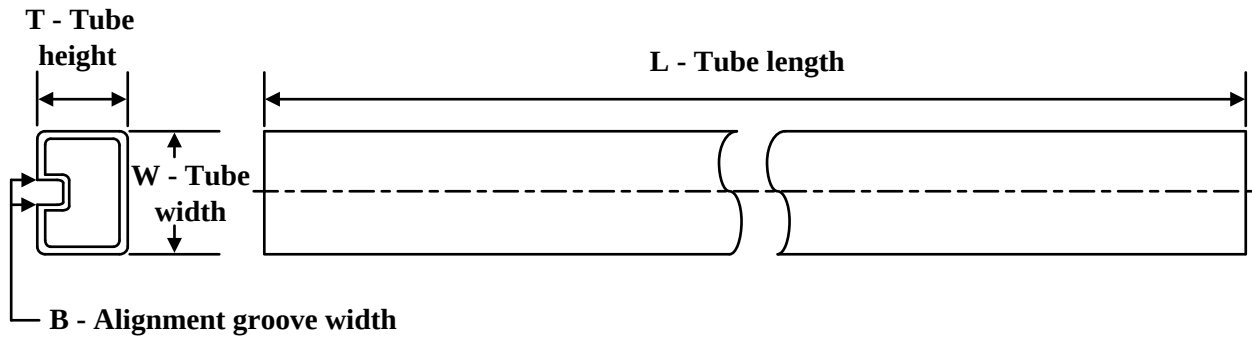
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

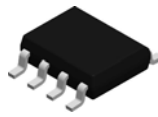
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC352CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC352IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC352IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC352IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC352CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC352CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC352IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC352IP.A	P	PDIP	8	50	506	13.97	11230	4.32

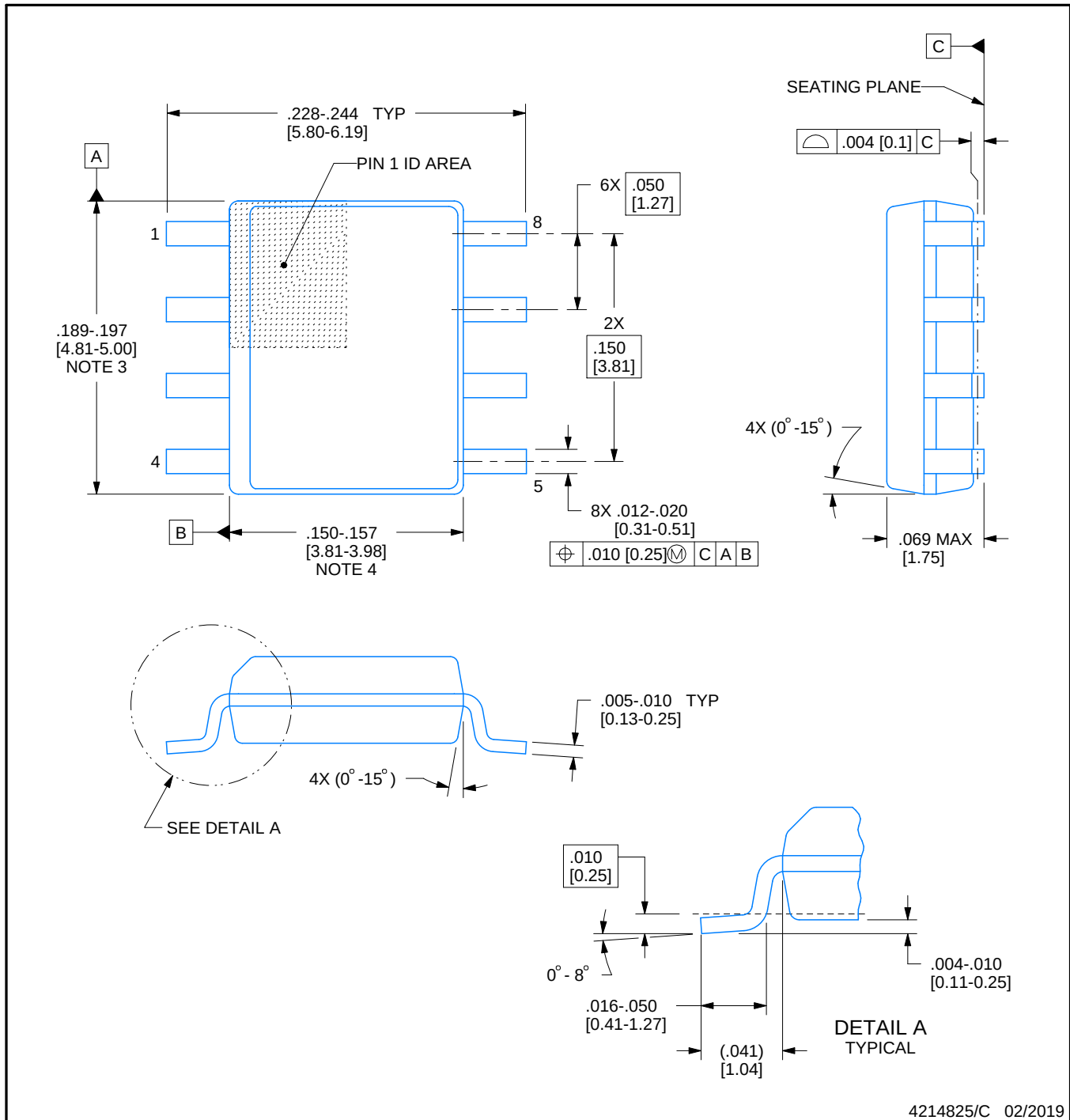


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

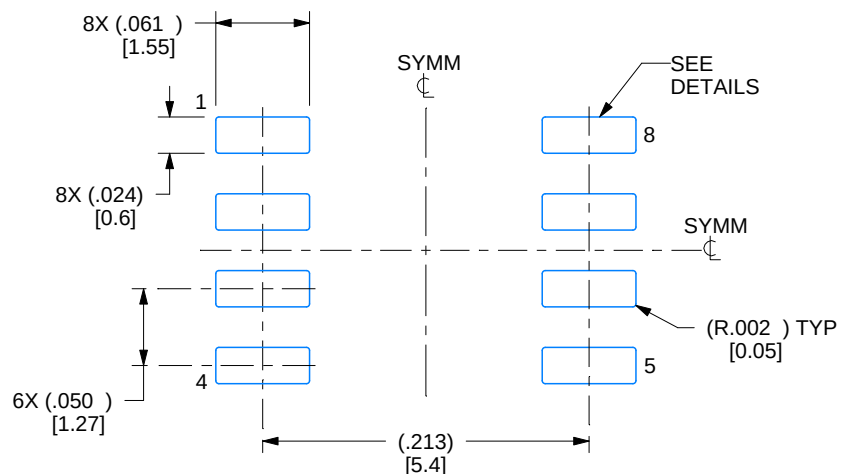
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

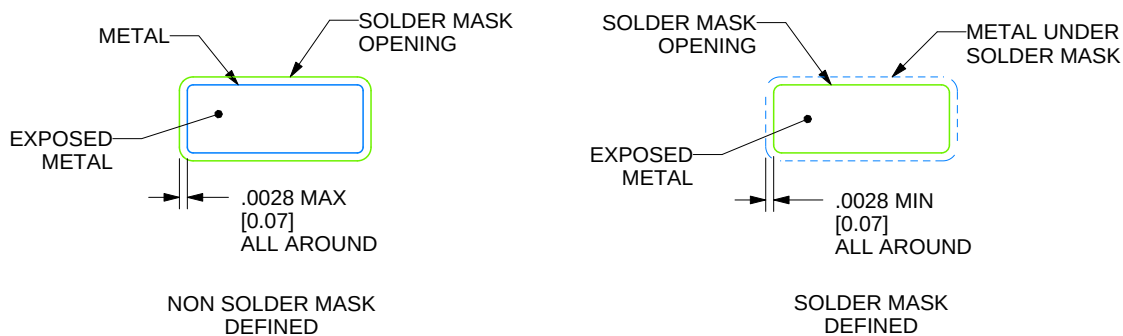
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

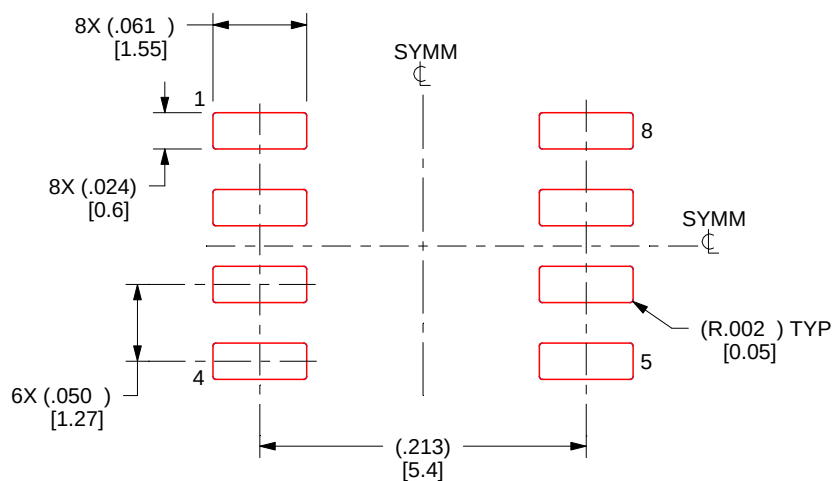
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

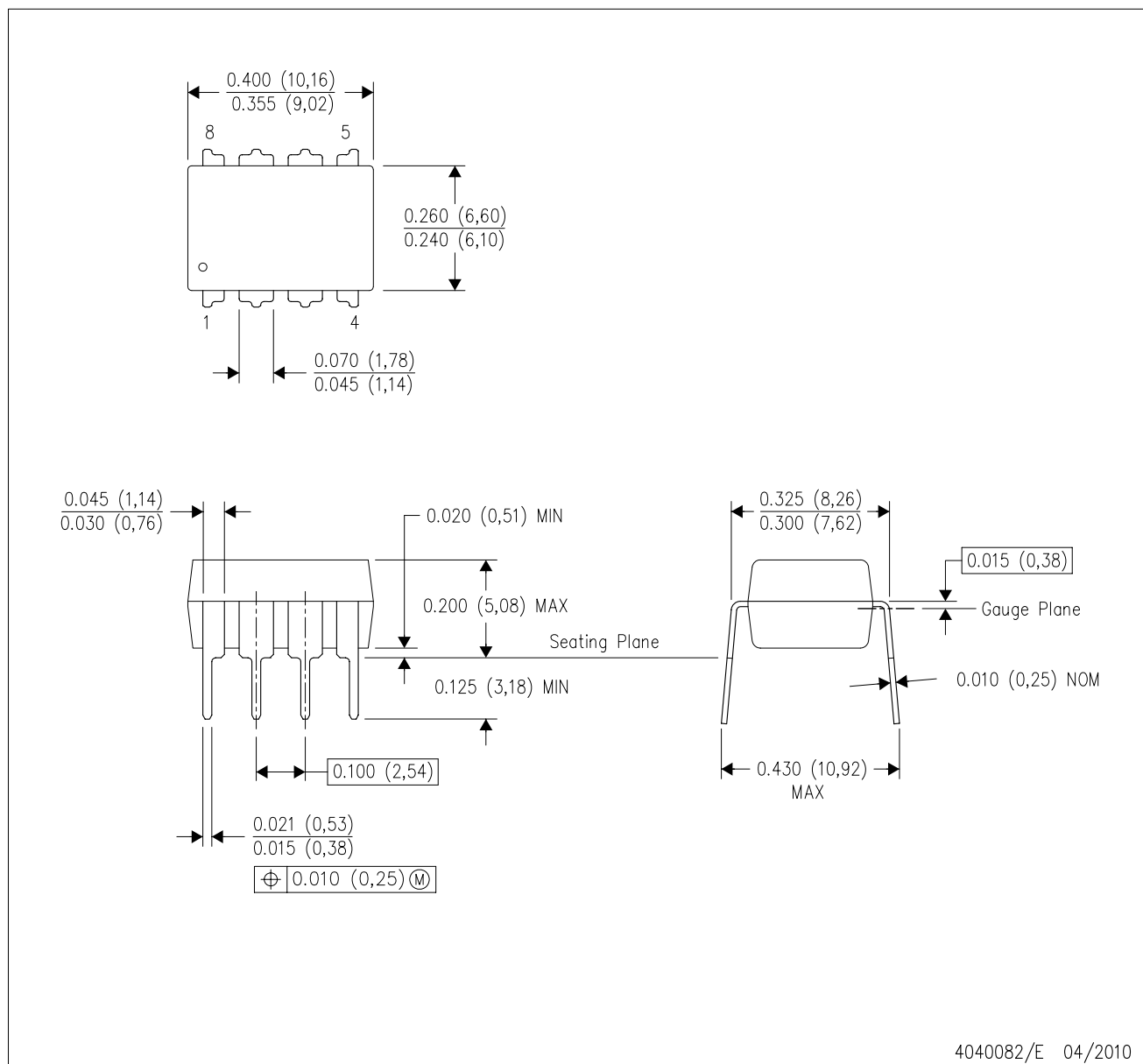
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



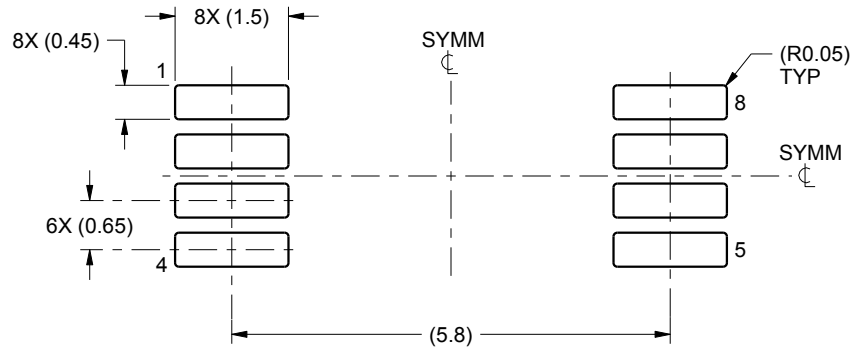
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

EXAMPLE BOARD LAYOUT

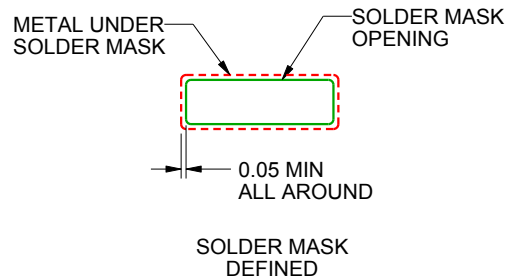
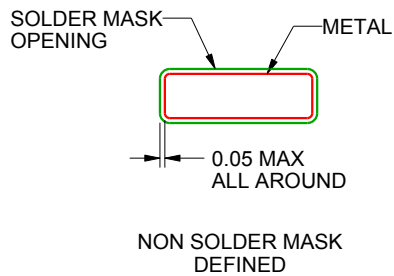
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

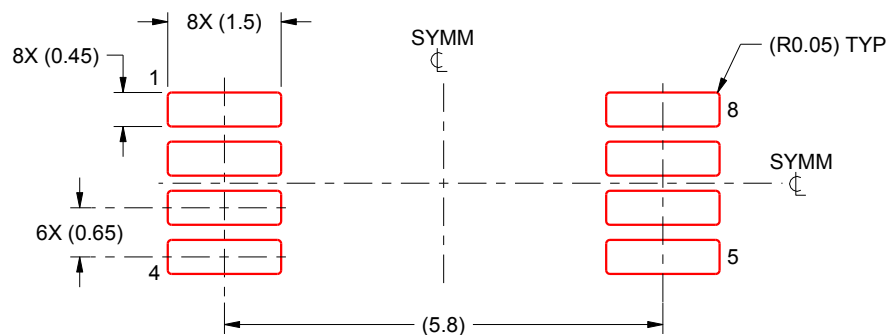
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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