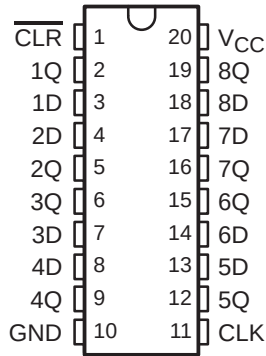


# SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

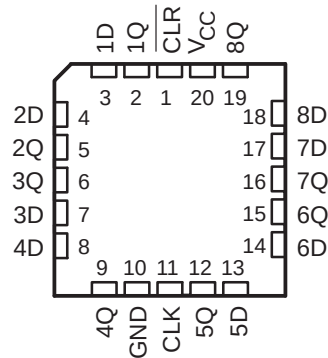
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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Unregulated Battery Operation Down To 2.7 V
- Buffered Clock and Direct-Clear Inputs
- Individual Data Input to Each Flip-Flop
- $I_{off}$  Supports Partial-Power-Down-Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54LVTH273 . . . J PACKAGE  
SN74LVTH273 . . . DB, DW, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LVTH273 . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH273 devices are positive-edge-triggered flip-flops with a direct-clear input. Information at the data (D) inputs meeting the setup-time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

## ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE†   |               | ORDERABLE<br>PART NUMBER | TOP-SIDE<br>MARKING |
|----------------|------------|---------------|--------------------------|---------------------|
| –40°C to 85°C  | SOIC – DW  | Tube          | SN74LVTH273DW            | LVTH273             |
|                |            | Tape and reel | SN74LVTH273DWR           |                     |
|                | SOP – NS   | Tape and reel | SN74LVTH273NSR           | LVTH273             |
|                | SSOP – DB  | Tape and reel | SN74LVTH273DBR           | LXH273              |
|                | TSSOP – PW | Tube          | SN74LVTH273PW            | LXH273              |
|                |            | Tape and reel | SN74LVTH273PWR           |                     |
| –55°C to 125°C | CDIP – J   | Tube          | SNJ54LVTH273J            | SNJ54LVTH273J       |
|                | LCCC – FK  | Tube          | SNJ54LVTH273FK           | SNJ54LVTH273FK      |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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SN54LVTH273, SN74LVTH273  
3.3-V ABT OCTAL D-TYPE FLIP-FLOPS  
WITH CLEAR

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description/ordering information (continued)

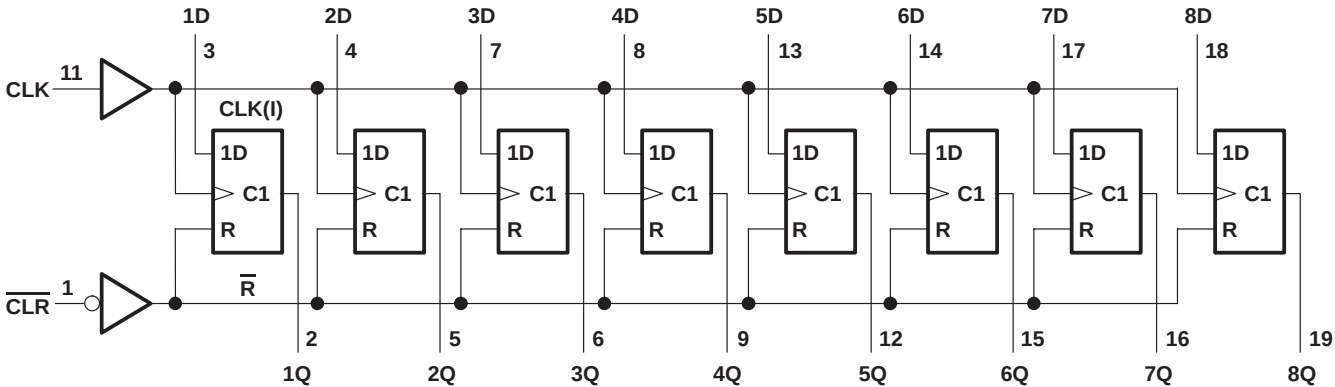
Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE  
(each flip-flop)

| INPUTS                  |            |   | OUTPUT<br>Q |
|-------------------------|------------|---|-------------|
| $\overline{\text{CLR}}$ | CLK        | D |             |
| L                       | X          | X | L           |
| H                       | $\uparrow$ | H | H           |
| H                       | $\uparrow$ | L | L           |
| H                       | H or L     | X | $Q_0$       |

logic diagram (positive logic)



# SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                                |                            |
|--------------------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$                                                 | –0.5 V to 4.6 V            |
| Input voltage range, $V_I$ (see Note 1)                                        | –0.5 V to 7 V              |
| Voltage range applied to any output in the power-off state, $V_O$ (see Note 1) | –0.5 V to 7 V              |
| Voltage range applied to any output in the high state, $V_O$ (see Note 1)      | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, $I_O$ : SN54LVTH273                  | 96 mA                      |
| SN74LVTH273                                                                    | 128 mA                     |
| Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH273     | 48 mA                      |
| SN74LVTH273                                                                    | 64 mA                      |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                                    | –50 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                                   | –50 mA                     |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package              | 70°C/W                     |
| DW package                                                                     | 58°C/W                     |
| NS package                                                                     | 60°C/W                     |
| PW package                                                                     | 83°C/W                     |
| Storage temperature range, $T_{stg}$                                           | –65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

|                                                        | SN54LVTH273 |     | SN74LVTH273 |     | UNIT |
|--------------------------------------------------------|-------------|-----|-------------|-----|------|
|                                                        | MIN         | MAX | MIN         | MAX |      |
| $V_{CC}$ Supply voltage                                | 2.7         | 3.6 | 2.7         | 3.6 | V    |
| $V_{IH}$ High-level input voltage                      | 2           |     | 2           |     | V    |
| $V_{IL}$ Low-level input voltage                       |             | 0.8 |             | 0.8 | V    |
| $V_I$ Input voltage                                    |             | 5.5 |             | 5.5 | V    |
| $I_{OH}$ High-level output current                     |             | –24 |             | –32 | mA   |
| $I_{OL}$ Low-level output current                      |             | 48  |             | 64  | mA   |
| $\Delta t/\Delta v$ Input transition rise or fall rate |             | 10  |             | 10  | ns/V |
| $T_A$ Operating free-air temperature                   | –55         | 125 | –40         | 85  | °C   |

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LVTH273, SN74LVTH273

## 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS

### WITH CLEAR

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER            |                | TEST CONDITIONS                                                                                              |                                  | SN54LVTH273          |      | SN74LVTH273          |      | UNIT |      |
|----------------------|----------------|--------------------------------------------------------------------------------------------------------------|----------------------------------|----------------------|------|----------------------|------|------|------|
|                      |                |                                                                                                              |                                  | MIN                  | TYP† | MAX                  | MIN  |      | TYP† |
| V <sub>IK</sub>      |                | V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = -18 mA                                                             |                                  | -1.2                 |      | -1.2                 |      | V    |      |
| V <sub>OH</sub>      |                | V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = -100 μA                                                  |                                  | V <sub>CC</sub> -0.2 |      | V <sub>CC</sub> -0.2 |      | V    |      |
|                      |                | V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = -8 mA                                                             |                                  | 2.4                  |      | 2.4                  |      |      |      |
|                      |                | V <sub>CC</sub> = 3 V                                                                                        | I <sub>OH</sub> = -24 mA         | 2                    |      |                      |      |      |      |
|                      |                |                                                                                                              | I <sub>OH</sub> = -32 mA         |                      |      | 2                    |      |      |      |
| V <sub>OL</sub>      |                | V <sub>CC</sub> = 2.7 V                                                                                      | I <sub>OL</sub> = 100 μA         | 0.2                  |      | 0.2                  |      | V    |      |
|                      |                |                                                                                                              | I <sub>OL</sub> = 24 mA          | 0.5                  |      | 0.5                  |      |      |      |
|                      |                | V <sub>CC</sub> = 3 V                                                                                        | I <sub>OL</sub> = 16 mA          | 0.4                  |      | 0.4                  |      |      |      |
|                      |                |                                                                                                              | I <sub>OL</sub> = 32 mA          | 0.5                  |      | 0.5                  |      |      |      |
|                      |                |                                                                                                              | I <sub>OL</sub> = 48 mA          | 0.55                 |      |                      |      |      |      |
|                      |                |                                                                                                              | I <sub>OL</sub> = 64 mA          |                      |      | 0.55                 |      |      |      |
|                      |                |                                                                                                              |                                  |                      |      |                      |      |      |      |
| I <sub>I</sub>       |                | V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V                                                         |                                  | 10                   |      | 10                   |      | μA   |      |
|                      | Control inputs | V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND                                             |                                  | ±1                   |      | ±1                   |      |      |      |
|                      | Data inputs    | V <sub>CC</sub> = 3.6 V                                                                                      | V <sub>I</sub> = V <sub>CC</sub> |                      | 1    |                      | 1    |      |      |
|                      |                |                                                                                                              | V <sub>I</sub> = 0               |                      | -5   |                      | -5   |      |      |
| I <sub>off</sub>     |                | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V                                           |                                  |                      |      | ±100                 |      | μA   |      |
| I <sub>I(hold)</sub> | Data inputs    | V <sub>CC</sub> = 3 V                                                                                        | V <sub>I</sub> = 0.8 V           |                      | 75   |                      | 75   |      | μA   |
|                      |                |                                                                                                              | V <sub>I</sub> = 2 V             |                      | -75  |                      | -75  |      |      |
|                      |                | V <sub>CC</sub> = 3.6 V‡, V <sub>I</sub> = 0 to 3.6 V                                                        |                                  |                      |      | 500<br>-750          |      |      |      |
| I <sub>CC</sub>      |                | V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND                         | Outputs high                     |                      | 0.19 |                      | 0.19 |      | mA   |
|                      |                |                                                                                                              | Outputs low                      |                      | 5    |                      | 5    |      |      |
| ΔI <sub>CC</sub> §   |                | V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND |                                  | 0.2                  |      | 0.2                  |      | mA   |      |
| C <sub>I</sub>       |                | V <sub>I</sub> = 3 V or 0                                                                                    |                                  | 4                    |      | 4                    |      | pF   |      |

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}\text{ or GND}$ .

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

|                    |                                        |                              | SN54LVTH273                                   |     |                         |     | SN74LVTH273                                   |     |                         |     | UNIT |
|--------------------|----------------------------------------|------------------------------|-----------------------------------------------|-----|-------------------------|-----|-----------------------------------------------|-----|-------------------------|-----|------|
|                    |                                        |                              | $V_{CC} = 3.3\text{ V}$<br>$\pm 0.3\text{ V}$ |     | $V_{CC} = 2.7\text{ V}$ |     | $V_{CC} = 3.3\text{ V}$<br>$\pm 0.3\text{ V}$ |     | $V_{CC} = 2.7\text{ V}$ |     |      |
|                    |                                        |                              | MIN                                           | MAX | MIN                     | MAX | MIN                                           | MAX | MIN                     | MAX |      |
| $f_{\text{clock}}$ | Clock frequency                        |                              | 150                                           |     |                         |     | 150                                           |     |                         |     | MHz  |
| $t_w$              | Pulse duration                         |                              | 3.3                                           |     | 3.3                     |     | 3.3                                           |     | 3.3                     |     | ns   |
| $t_{\text{su}}$    | Setup time                             | Data high or low before CLK↑ | 2.3                                           |     | 2.7                     |     | 2.3                                           |     | 2.7                     |     | ns   |
|                    |                                        | CLR high before CLK↑         | 2.3                                           |     | 2.7                     |     | 2.3                                           |     | 2.7                     |     |      |
| $t_h$              | Hold time, data high or low after CLK↑ |                              | 0                                             |     | 0                       |     | 0                                             |     | 0                       |     | ns   |

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# SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT)         | TO<br>(OUTPUT) | SN54LVTH273                        |     |                         |     | SN74LVTH273                        |                  |     |                         | UNIT |
|------------------|-------------------------|----------------|------------------------------------|-----|-------------------------|-----|------------------------------------|------------------|-----|-------------------------|------|
|                  |                         |                | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |                  |     | V <sub>CC</sub> = 2.7 V |      |
|                  |                         |                | MIN                                | MAX | MIN                     | MAX | MIN                                | TYP <sup>†</sup> | MAX | MIN                     |      |
| f <sub>max</sub> |                         |                | 150                                |     |                         |     | 150                                |                  |     |                         | MHz  |
| t <sub>PLH</sub> | CLK                     | Any Q          | 1.6                                | 5   |                         | 5.6 | 1.7                                | 3.2              | 4.9 | 5.5                     | ns   |
| t <sub>PHL</sub> |                         |                | 1.8                                | 4.9 |                         | 5.2 | 1.9                                | 3.2              | 4.8 | 5.1                     |      |
| t <sub>PHL</sub> | $\overline{\text{CLR}}$ | Any Q          | 1.5                                | 4.4 |                         | 4.8 | 1.6                                | 2.7              | 4.3 | 4.7                     | ns   |

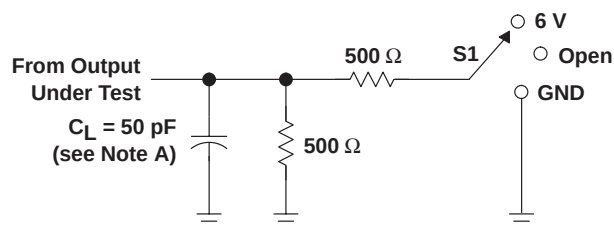
<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

# SN54LVTH273, SN74LVTH273

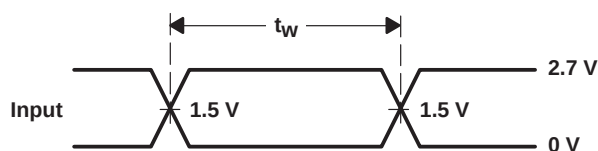
## 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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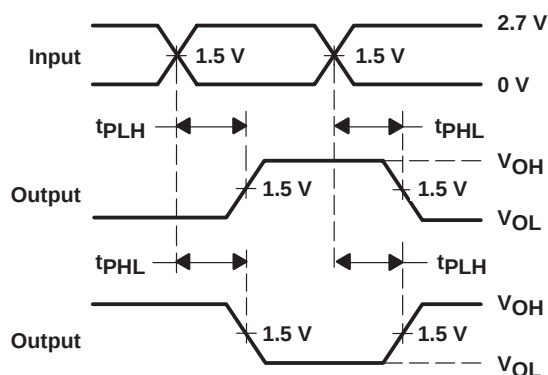
### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

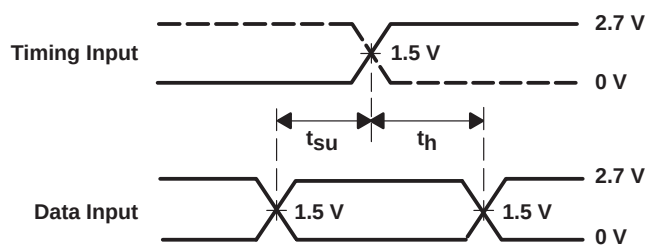


VOLTAGE WAVEFORMS  
PULSE DURATION

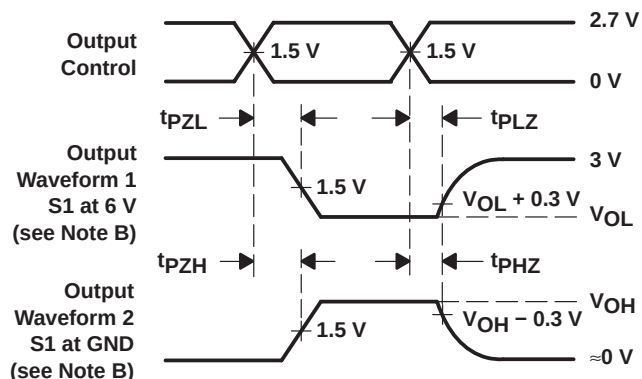


VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS

| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V  |
| $t_{PHZ}/t_{PZH}$ | GND  |



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74LVTH273DBR</a>   | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LXH273              |
| SN74LVTH273DBR.B                 | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LXH273              |
| SN74LVTH273DBRG4.B               | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LXH273              |
| <a href="#">SN74LVTH273DW</a>    | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH273             |
| SN74LVTH273DW.B                  | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH273             |
| <a href="#">SN74LVTH273DWR</a>   | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH273             |
| SN74LVTH273DWR.B                 | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH273             |
| SN74LVTH273DWRE4                 | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH273             |
| <a href="#">SN74LVTH273NSR</a>   | Active        | Production           | SOP (NS)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH273             |
| SN74LVTH273NSR.B                 | Active        | Production           | SOP (NS)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH273             |
| <a href="#">SN74LVTH273PW</a>    | Active        | Production           | TSSOP (PW)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LXH273              |
| SN74LVTH273PW.B                  | Active        | Production           | TSSOP (PW)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LXH273              |
| <a href="#">SN74LVTH273PWR</a>   | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | LXH273              |
| SN74LVTH273PWR.B                 | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LXH273              |
| <a href="#">SN74LVTH273PWRG4</a> | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LXH273              |
| SN74LVTH273PWRG4.B               | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LXH273              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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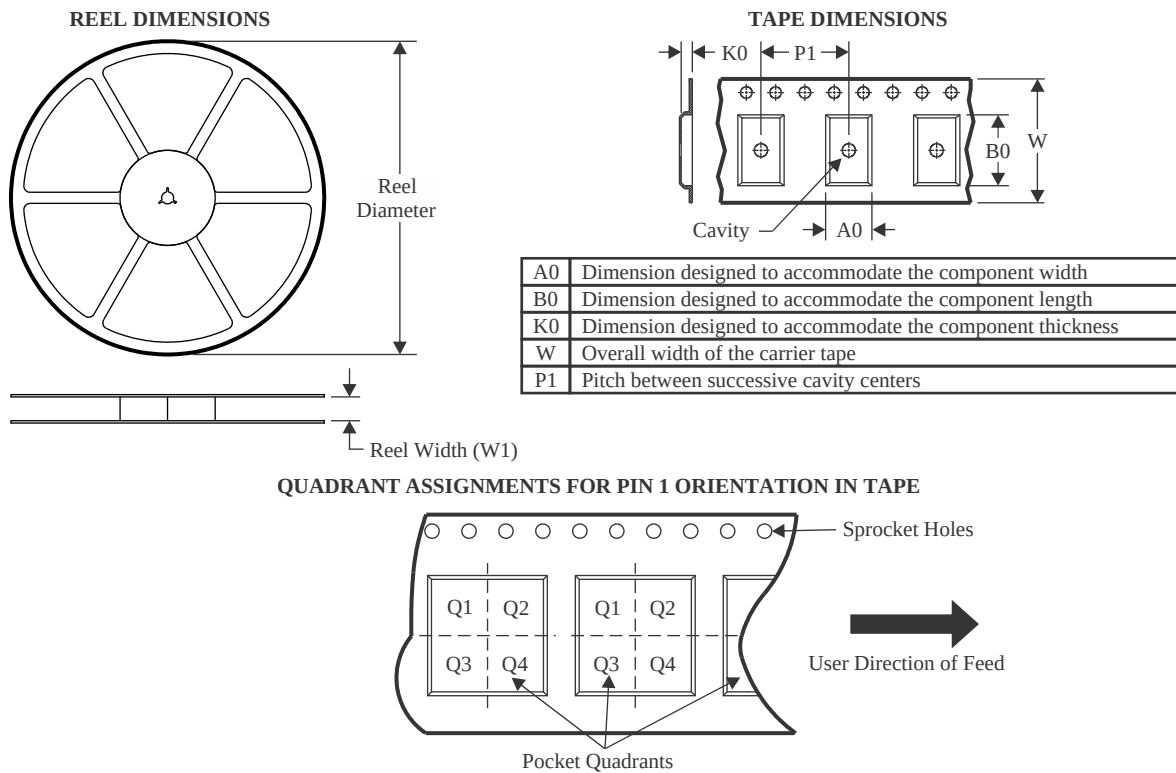
**OTHER QUALIFIED VERSIONS OF SN74LVTH273 :**

- Enhanced Product : [SN74LVTH273-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

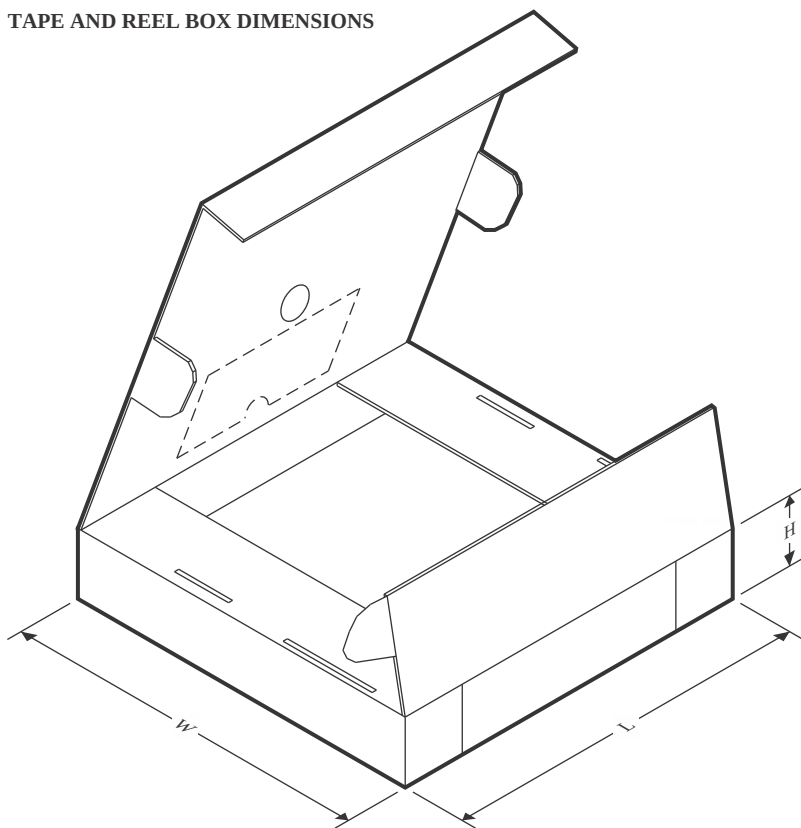
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVTH273DBR   | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVTH273DWR   | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LVTH273NSR   | SOP          | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74LVTH273PWR   | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74LVTH273PWRG4 | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |

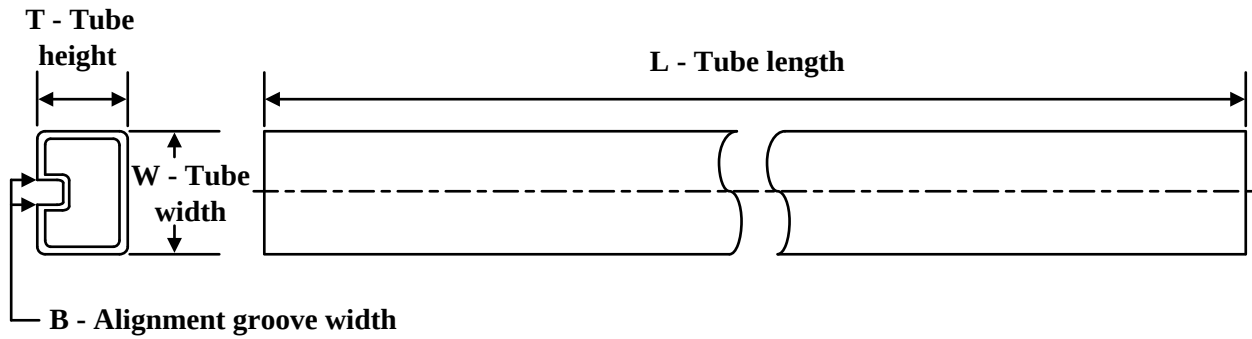
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVTH273DBR   | SSOP         | DB              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LVTH273DWR   | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVTH273NSR   | SOP          | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVTH273PWR   | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LVTH273PWRG4 | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

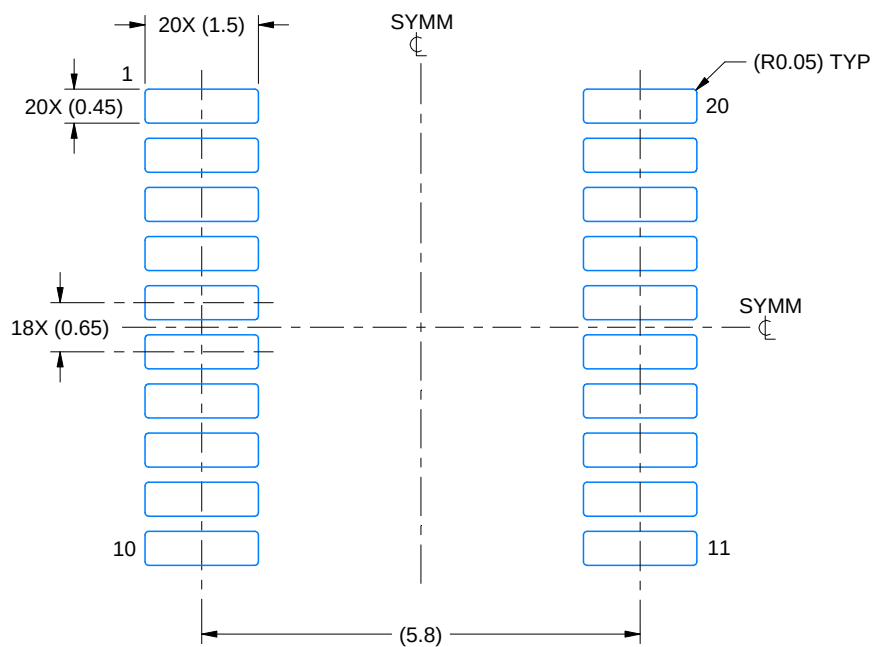
| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVTH273DW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74LVTH273DW.B | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74LVTH273PW   | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVTH273PW.B | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |



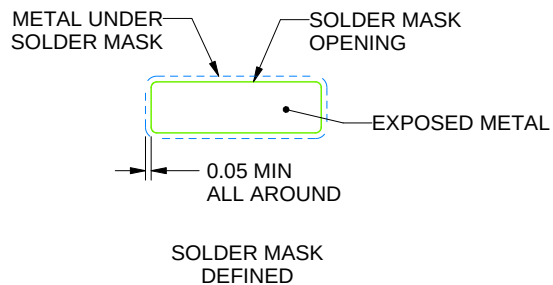
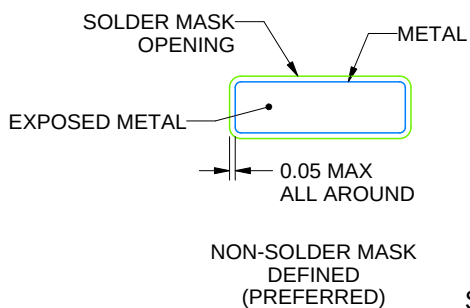
**PW0020A**

**TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

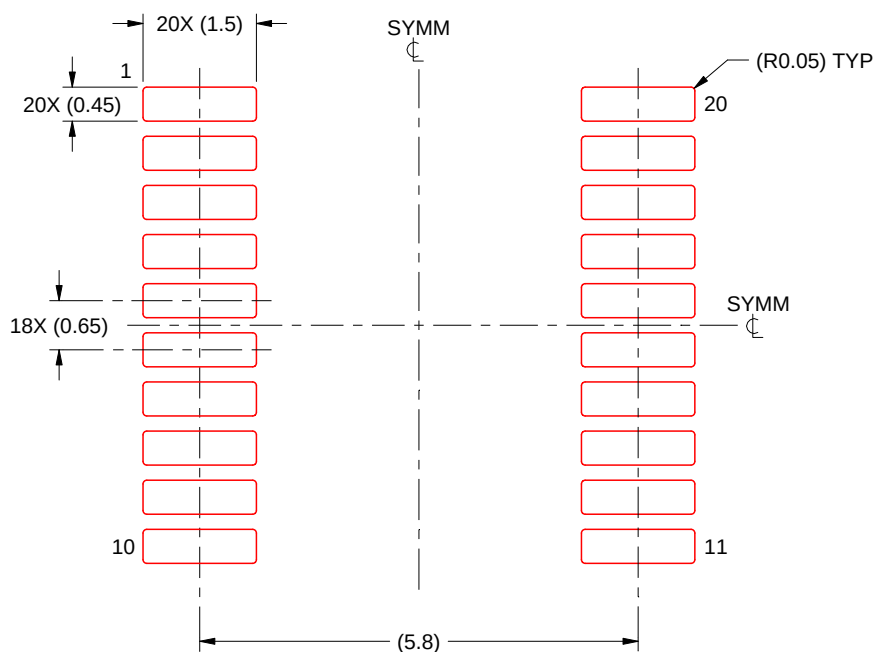
6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

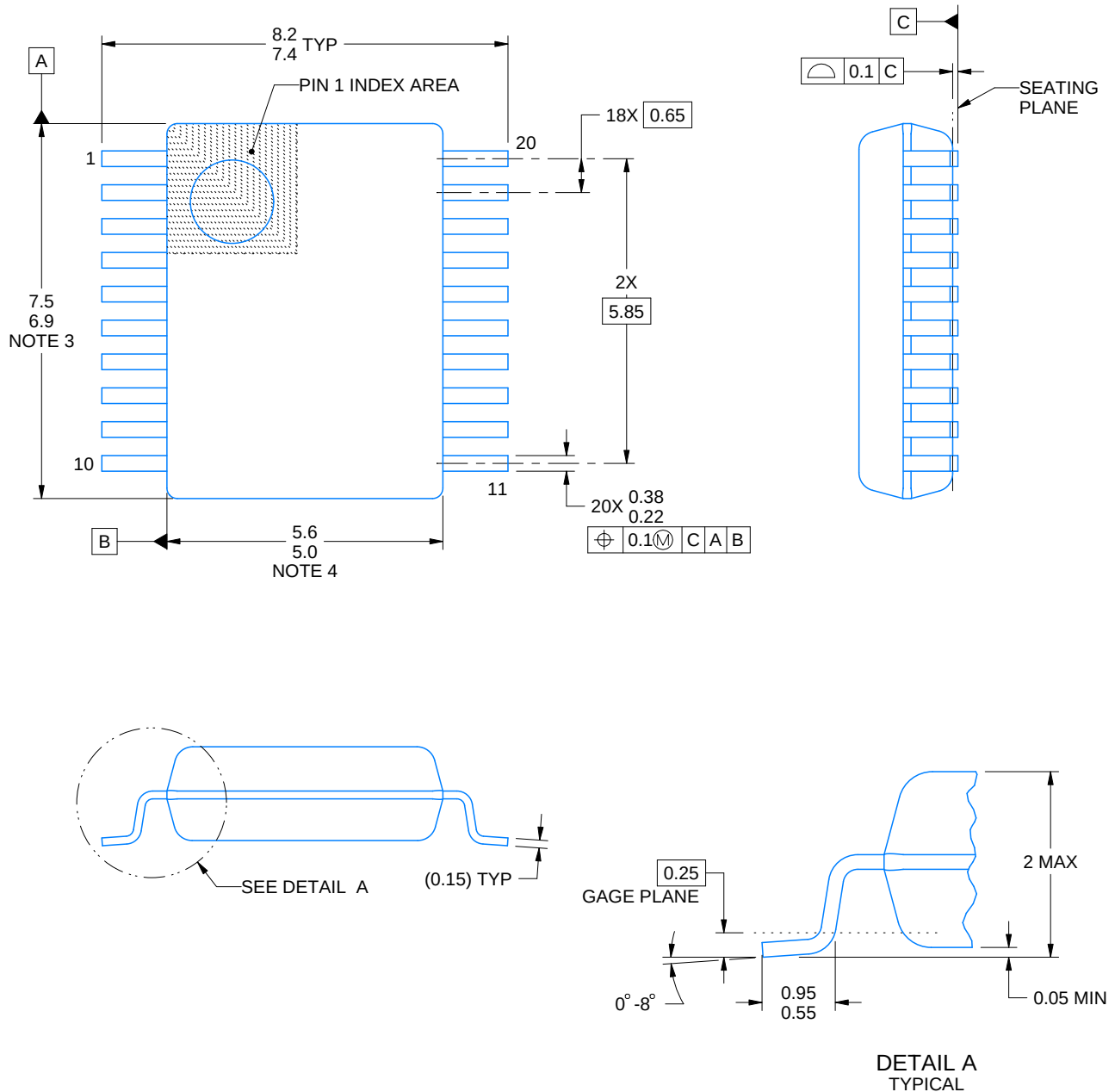
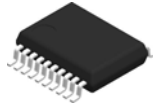


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

## NOTES:

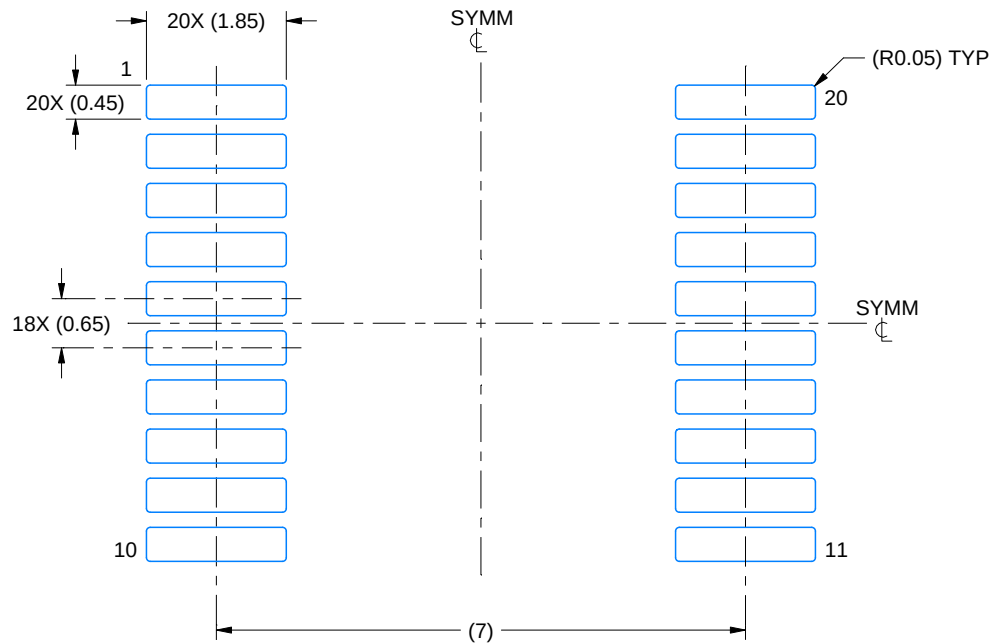
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

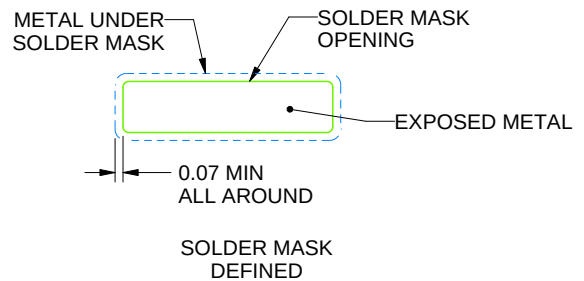
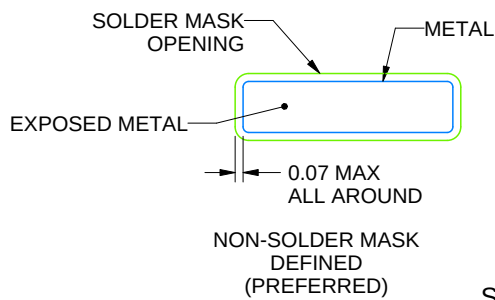
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

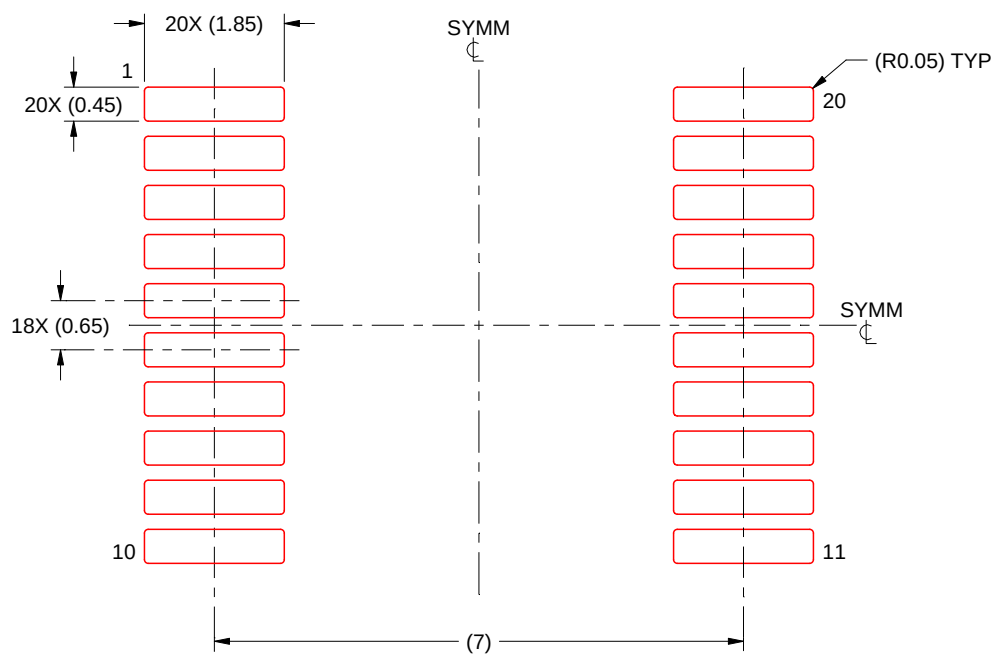
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

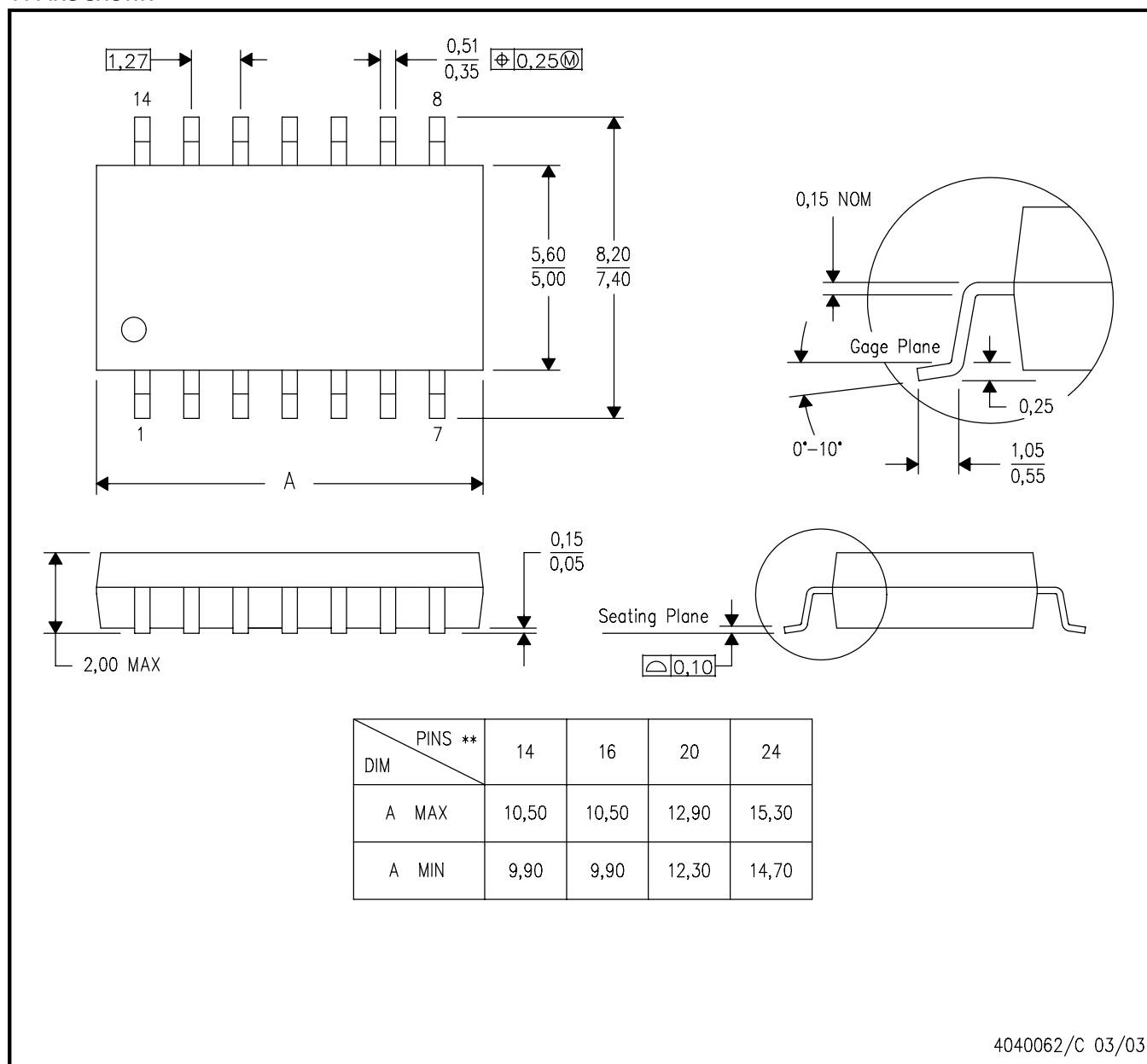
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

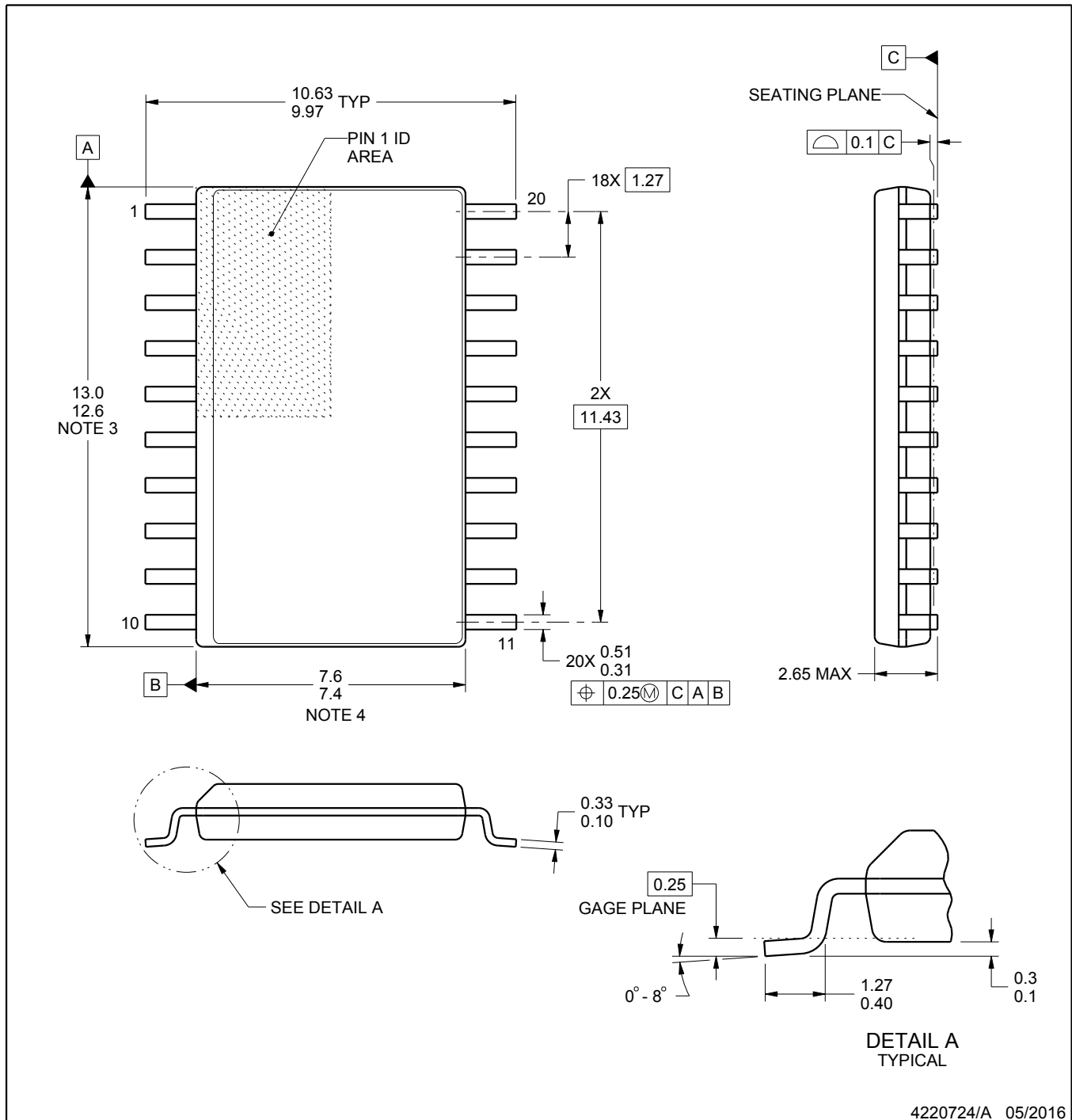
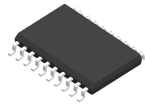
NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



4220724/A 05/2016

## NOTES:

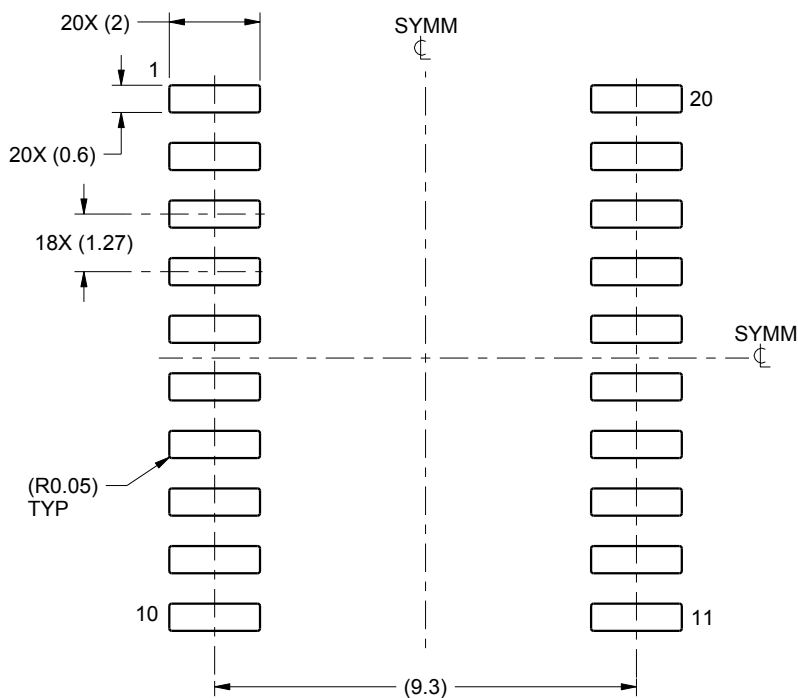
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

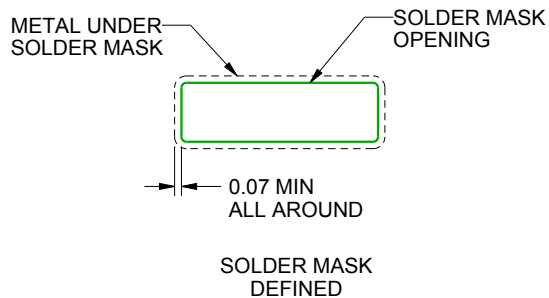
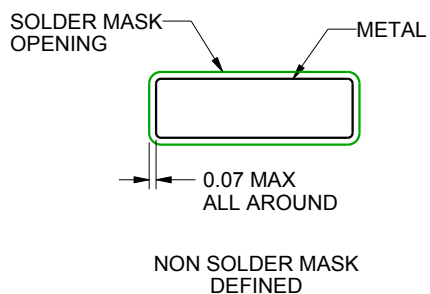
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

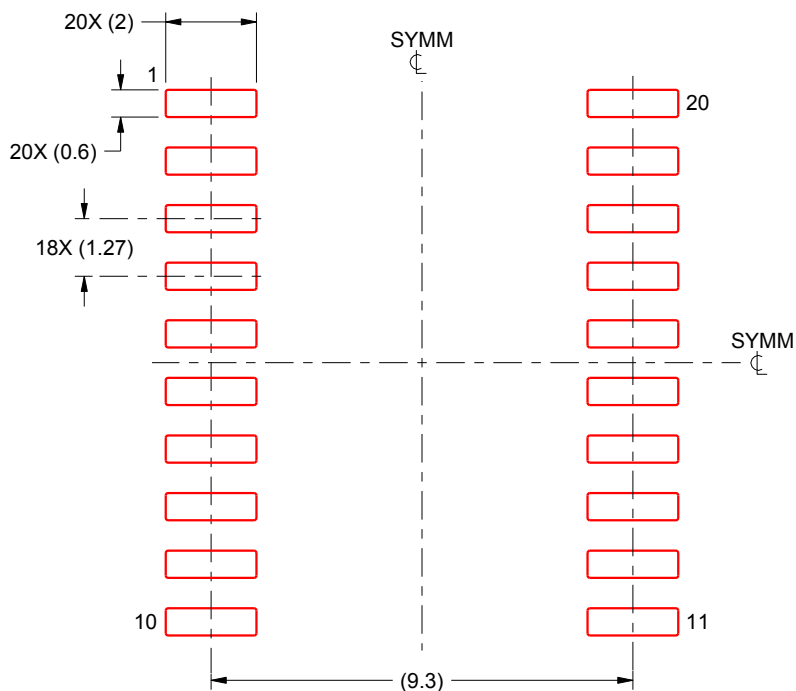
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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