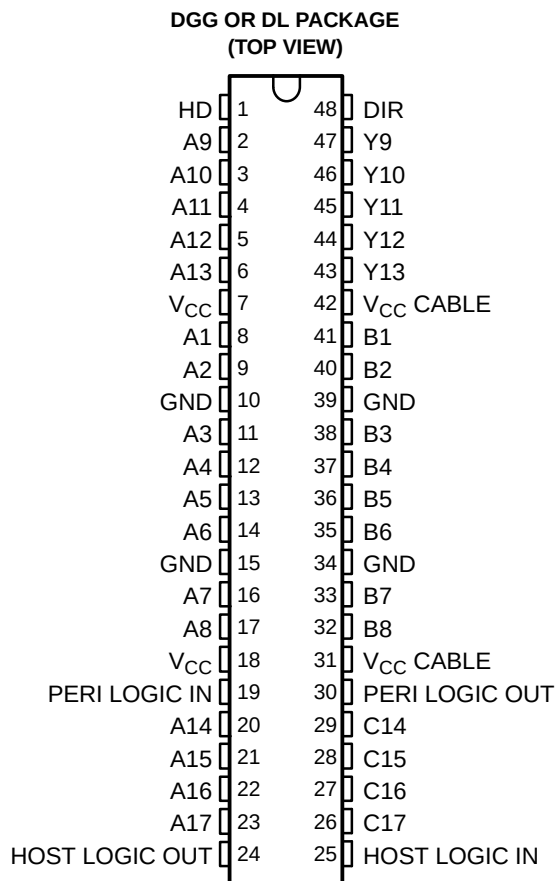


FEATURES

- **Auto-Power-Up Feature Prevents Printer Errors When Printer Is Turned On, But No Valid Signal Is at A9–A13 Pins**
- **1.4-k Ω Pullup Resistors Integrated on All Open-Drain Outputs Eliminate the Need for Discrete Resistors**
- **Designed for IEEE Std 1284-I (Level-1 Type) and IEEE Std 1284-II (Level-2 Type) Electrical Specifications**
- **Flow-Through Architecture Optimizes PCB Layout**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection**
 - **± 4 kV – Human-Body Model**
 - **± 8 kV – IEC 61000-4-2, Contact Discharge (Connector Pins)**
 - **± 15 kV – IEC 61000-4-2, Air-Gap Discharge (Connector Pins)**
 - **± 15 kV – Human-Body Model (Connector Pins)**



DESCRIPTION/ORDERING INFORMATION

The SN74LVCE161284 is designed for 3-V to 3.6-V V_{CC} operation. This device provides asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

This device has eight bidirectional bits; data can flow in the A-to-B direction when the direction-control input (DIR) is high and in the B-to-A direction when DIR is low. This device also has five drivers that drive the cable side and four receivers. The SN74LVCE161284 has one receiver dedicated to the HOST LOGIC line and a driver to drive the PERI LOGIC line.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SSOP – DL	Tube	SN74LVCE161284DL	LVCE161284
		Tape and reel	SN74LVCE161284DLR	
	TSSOP – DGG	Tape and reel	SN74LVCE161284DGGR	LVCE161284

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The output drive mode is determined by the high-drive (HD) control pin. When HD is high, the outputs are in a totem-pole configuration, and in an open-drain configuration when HD is low. This meets the drive requirements as specified in the IEEE Std 1284-I (level-1 type) and IEEE Std 1284-II (level-2 type) parallel peripheral-interface specifications. Except for HOST LOGIC IN and peripheral logic out (PERI LOGIC OUT), all cable-side pins have a 1.4-k Ω integrated pullup resistor. The pullup resistor is switched off if the associated output driver is in the low state or if the output voltage is above V_{CC} CABLE. If V_{CC} CABLE is off, PERI LOGIC OUT is set to low.

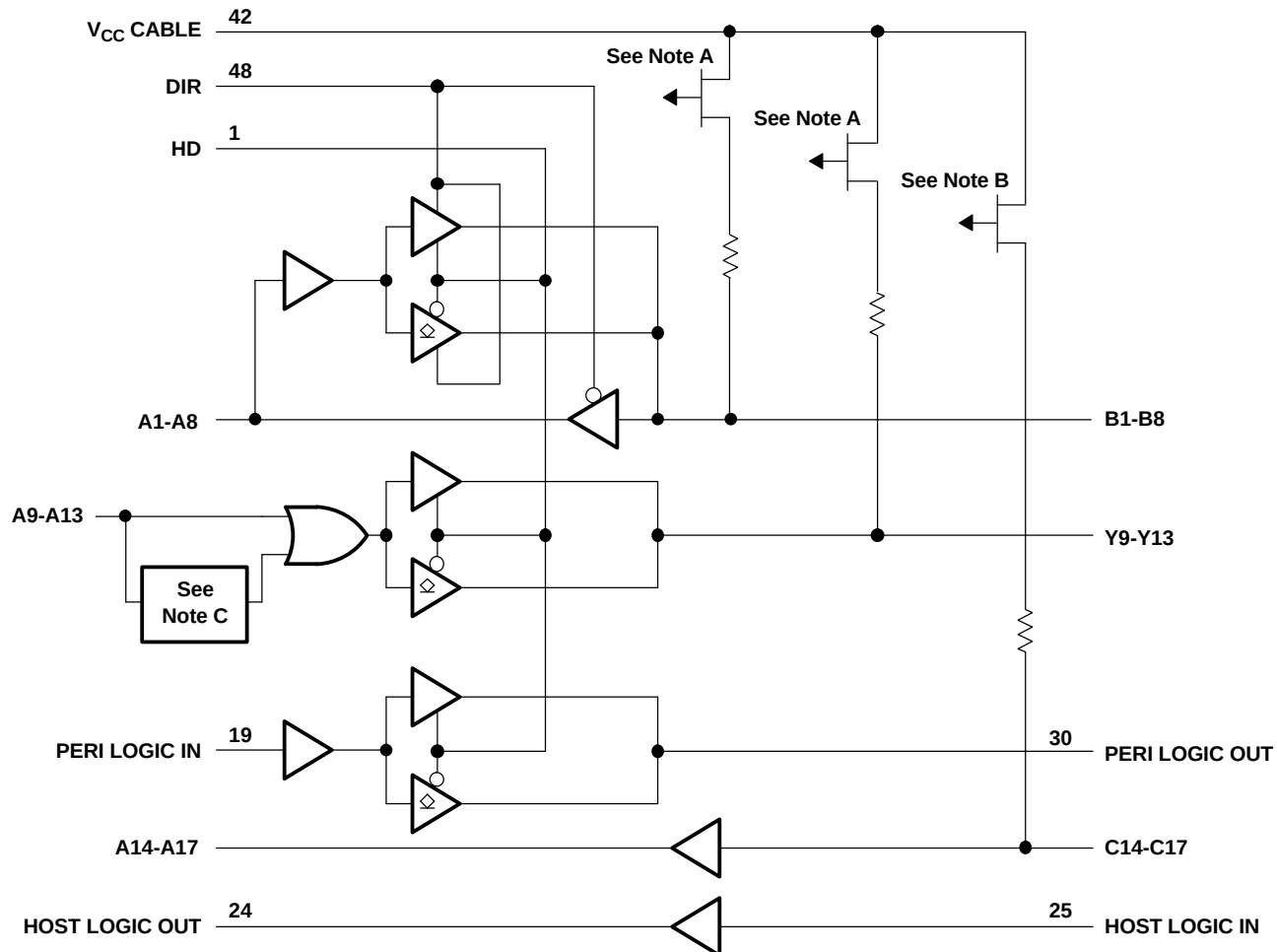
The device has two supply voltages. V_{CC} is designed for 3-V to 3.6-V operation. V_{CC} CABLE supplies the inputs and output buffers of the cable side only and is designed for 3-V to 3.6-V and for 4.7-V to 5.5-V operation. Even when V_{CC} CABLE is 3 V to 3.6 V, the cable-side I/O pins are 5-V tolerant.

The Y outputs (Y9–Y13) stay in the high state after power on until an associated input (A9–A13) goes high. When an associated input goes high, all Y outputs are activated, and noninverting signals of the associated inputs are driven through Y outputs. This special feature prevents printer-system errors caused by deasserting the BUSY signal in the cable at power on.

FUNCTION TABLE

INPUTS		OUTPUT	MODE
DIR	HD		
L	L	Open drain	A9–A13 to Y9–Y13 and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	B1–B8 to A1–A8 and C14–C17 to A14–A17
L	H	Totem pole	B1–B8 to A1–A8, A9–A13 to Y9–Y13, PERI LOGIC IN to PERI LOGIC OUT, and C14–C17 to A14–A17
H	L	Open drain	A1–A8 to B1–B8, A9–A13 to Y9–Y13, and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	C14–C17 to A14–A17
H	H	Totem pole	A1–A8 to B1–B8, A9–A13 to Y9–Y13, C14–C17 to A14–A17, and PERI LOGIC IN to PERI LOGIC OUT

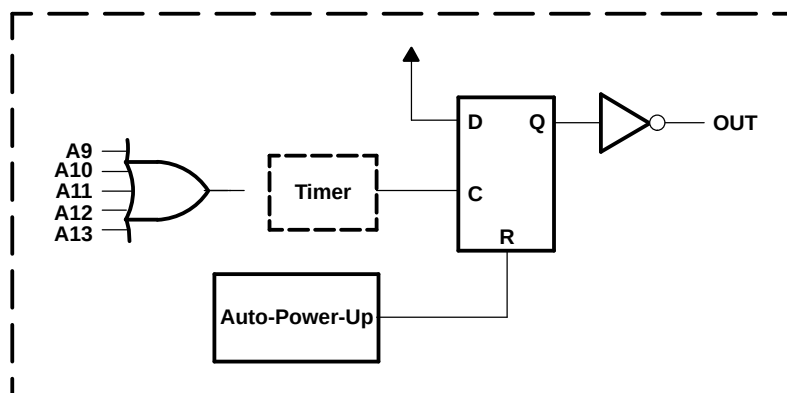
LOGIC DIAGRAM



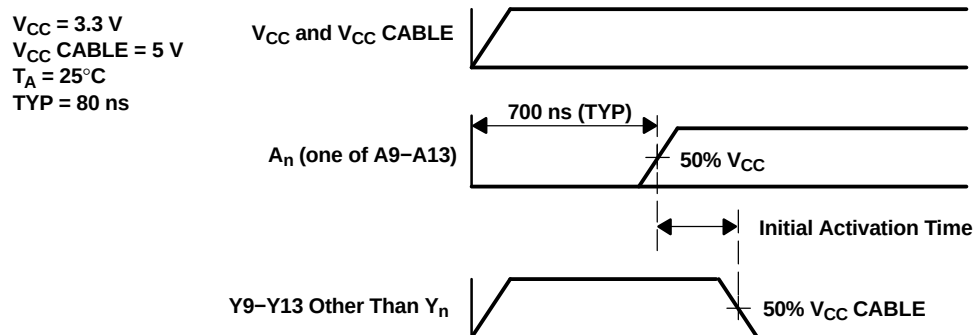
- NOTES: A. The PMOS transistors prevent backdriving current from the signal pins to V_{CC} CABLE when V_{CC} CABLE is open or at GND. The PMOS transistor is turned off when the associated driver is in the low state.
B. The PMOS transistor prevents backdriving current from the signal pins to V_{CC} CABLE when V_{CC} CABLE is open or at GND.
C. Active input detection circuit forces Y9-Y13 to the high state after power-on, until one of the A9-A13 goes high (see Figure 1).

SN74LVCE161284
19-BIT IEEE STD 1284 TRANSLATION TRANSCEIVER
WITH ERROR-FREE POWER UP

SCES541–JANUARY 2004–REVISED MARCH 2005



Active Input Detection Circuit



NOTE A: One of A9–A13 is switched as shown above, and the other four inputs are forced to low state.

Figure 1. Error-Free Circuit Timing

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC CABLE}	Supply voltage range		–0.5	7	V
V _{CC}	Supply voltage range		–0.5	4.6	V
V _I , V _O	Input and output voltage range	Cable side ⁽²⁾⁽³⁾	–2	7	V
		Peripheral side ⁽²⁾	–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		–20	mA
I _{OK}	Output clamp current	V _O < 0		–50	mA
I _O	Continuous output current	Except PERI LOGIC OUT		±50	mA
		PERI LOGIC OUT		±100	mA
	Continuous current through each V _{CC} or GND			±200	mA
I _{SK}	Output high sink current	V _O = 5.5 V and V _{CC CABLE} = 3 V		65	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DGG package		70	°C/W
		DL package		63	°C/W
T _{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The ac input-voltage pulse duration is limited to 40 ns if the amplitude is greater than –0.5 V.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC CABLE}	Supply voltage for the cable side, V _{CC CABLE} ≥ V _{CC}		3	5.5	V
V _{CC}	Supply voltage		3	3.6	V
V _{IH}	High-level input voltage	A, B, DIR, and HD	2		V
		C14–C17	2.3		
		HOST LOGIC IN	2.6		
		PERI LOGIC IN	2		
V _{IL}	Low-level input voltage	A, B, DIR, and HD		0.8	V
		C14–C17		0.8	
		HOST LOGIC IN		1.6	
		PERI LOGIC IN		0.8	
V _I	Input voltage	Peripheral side	0	V _{CC}	V
		Cable side	0	5.5	
V _O	Open-drain output voltage	HD low	0	5.5	V
I _{OH}	High-level output current	HD high, B and Y outputs		–14	mA
		A outputs and HOST LOGIC OUT		–4	
		PERI LOGIC OUT		–0.5	
I _{OL}	Low-level output current	B and Y outputs		14	mA
		A outputs and HOST LOGIC OUT		4	
		PERI LOGIC OUT		84	
T _A	Operating free-air temperature		0	70	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVCE161284

19-BIT IEEE STD 1284 TRANSLATION TRANSCEIVER

WITH ERROR-FREE POWER UP

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	V _{CC} CABLE	MIN	TYP ⁽¹⁾	MAX	UNIT
ΔV _I Hysteresis (V _{T+} – V _{T–})	All inputs except the C inputs and HOST LOGIC IN		3.3 V	5 V	0.4			V
	HOST LOGIC IN				0.2			
	C inputs				0.8			
V _{OH}	HD high, B and Y outputs	I _{OH} = –14 mA	3 V	3 V	2.23			V
			3.3 V	4.7 V	2.4			
	HD high, A outputs, and HOST LOGIC OUT	I _{OH} = –4 mA	3 V	3 V	2.4			
		I _{OH} = –50 μA			2.8			
	PERI LOGIC OUT	I _{OH} = –0.5 mA	3.15 V	3.15 V	3.1			
			3.3 V	4.7 V	4.5			
V _{OL}	B and Y outputs	I _{OL} = 14 mA	3 V	3 V	0.77			V
	A outputs and HOST LOGIC OUT	I _{OL} = 50 μA			0.2			
		I _{OL} = 4 mA			0.4			
		PERI LOGIC OUT			I _{OL} = 84 mA	0.9		
I _I	C inputs	V _I = V _{CC}	3.6 V	3.6 V	50			μA
		V _I = GND (pullup resistors)			–3.5			mA
	All inputs except B or C inputs	V _I = V _{CC} or GND		5.5 V	±1			μA
I _{OZ}	A1–A8	V _O = V _{CC} or GND	3.6 V	5.5 V	±20			μA
	B outputs	V _O = V _{CC} CABLE		3.6 V	50			mA
		V _O = GND (pullup resistors)			–3.5			
		Open-drain Y outputs			V _O = GND (pullup resistors)	–3.5		
I _{OZPU}	B and Y outputs	V _O = 5.5 V	0 to 1.5 V ⁽²⁾	0 to 1.5 V ⁽²⁾	350			μA
		V _O = GND			–5			mA
I _{OZPD}	B and Y outputs	V _O = 5.5 V	0 to 1.5 V ⁽²⁾	0 to 1.5 V ⁽²⁾	350			μA
		V _O = GND			–5			mA
I _{off}	Power-down input leakage, except A1–A8 or B1–B8 inputs	V _I or V _O = 0 to 3.6 V	0	0	100			μA
	Power-down output leakage, B1–B8 and Y9–Y13 outputs	V _I or V _O = 0 to 5.5 V			100			
I _{CC}		V _I = GND (12 × pullup)	3.6 V	3.6 V	45			mA
				5.5 V	70			
		V _I = V _{CC} , I _O = 0		3.6 V	0.8			
Z _O	B1–B8, Y9–Y13	I _{OH} = –35 mA	3.3 V	3.3 V	36			Ω
R pullup	B1–B8, Y9–Y13, C14–C17	V _O = 0 V (in high-impedance state)	3.3 V	3.3 V	1.15	1.65		kΩ
C _i	A9–A13, DIR, HD, PERI LOGIC IN	V _I = V _{CC} or GND	3.3 V	5 V	6.5			pF
	HOST LOGIC IN				4			
C _{io}	A1–A8	V _O = V _{CC} or GND	3.3 V	5 V	8			pF
	B1–B8				13			

(1) Typical values are measured at T_A = 25°C.

(2) Connect the V_{CC} pin to the V_{CC} CABLE pin.

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2 and Figure 3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Totem pole	A1–A8	B1–B8	2		30	ns
t _{PHL}				2		30	
t _{PLH}	Totem pole	A9–A13	Y9–Y13	2		30	ns
t _{PHL}				2		30	
t _{PLH}	Totem pole	B1–B8	A1–A8	2		12	ns
t _{PHL}				2		12	
t _{PLH}	Totem pole	C14–C17	A14–A17	2		14	ns
t _{PHL}				2		14	
t _{PLH}	Totem pole	PERI LOGIC IN	PERI LOGIC OUT	2		16	ns
t _{PHL}				2		16	
t _{PLH}	Totem pole	HOST LOGIC IN	HOST LOGIC OUT	1		18	ns
t _{PHL}				1		18	
t _{slew}	Totem pole	B1–B8 and Y9–Y13 outputs		0.05		0.4	V/ns
t _{PZH}		HD	B1–B8, Y9–Y13, and PERI LOGIC OUT	2		30	ns
t _{PHZ}				2		25	
t _{en} –t _{dis}		DIR	A1–A8	2		25	ns
t _{PHZ}		DIR	B1–B8	2		25	ns
t _{PLZ}				2		25	
t _r , t _f	Open drain	A1–A13	B1–B8 or Y9–Y13	1		120	ns
t _{sk(o)} ⁽²⁾		A1–A8 or B1–B8	B1–B8 or A1–A8		3	10	ns

(1) Typical values are measured at $V_{CC} = 3.3\text{ V}$, $V_{CC\text{ CABLE}} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

(2) Skew is measured at $1/2 (V_{OH} + V_{OL})$ for signals switching in the same direction.

Table 1. ESD Protection

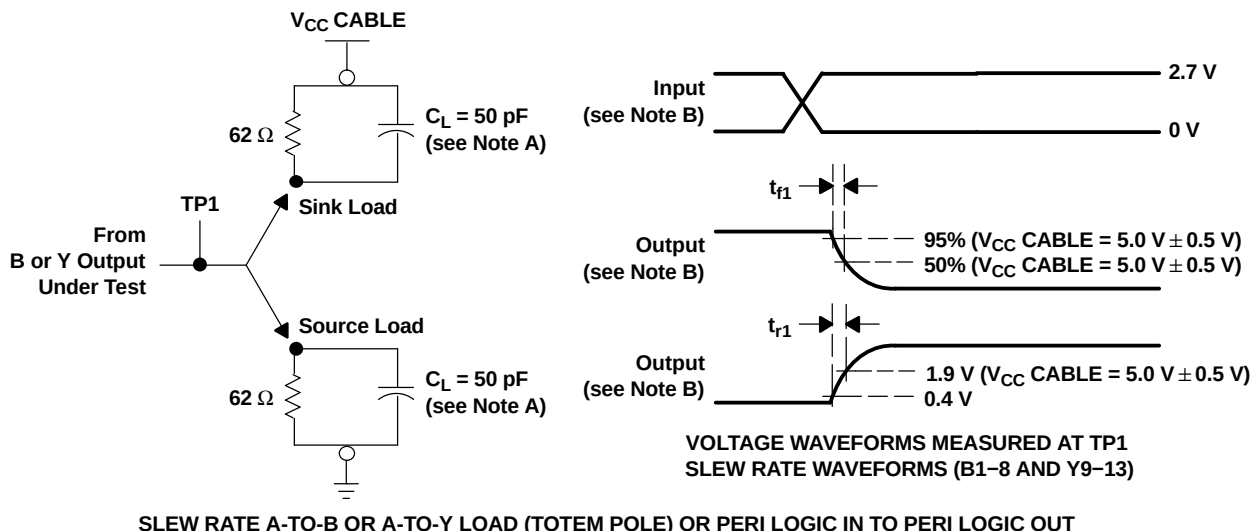
PIN	TEST CONDITIONS	TYP	UNIT
B1–B8, Y9–Y13, PERI LOGIC OUT, C14–C17, HOST LOGIC IN	HBM	± 15	kV
	Contact discharge, IEC 61000-4-2	± 8	
	Air-gap discharge, IEC 61000-4-2	± 15	
DIR, HD, A1–A8, A9–A13, PERI LOGIC IN, A14–A17, HOST LOGIC OUT	HBM	± 4	kV

Operating Characteristics

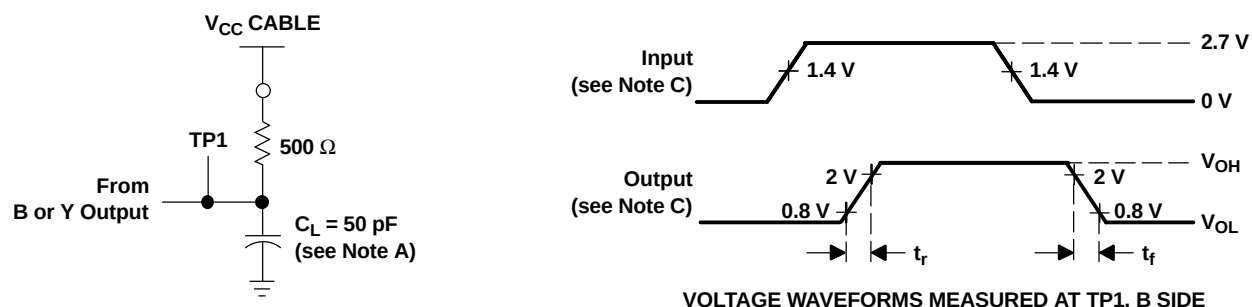
V_{CC} and $V_{CC\text{ CABLE}} = 3.3\text{ V}$, $C_L = 0$, $f = 10\text{ MHz}$, $T_A = 25^\circ\text{C}$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TYP	UNIT
C_{pd}	Power dissipation capacitance	A	B	15	pF
		A	Y	6	
		PERI LOGIC IN	PERI LOGIC OUT	10	
		B	A	33	
		C	A	29	
		HOST LOGIC IN	HOST LOGIC OUT	29	

PARAMETER MEASUREMENT INFORMATION



SLEW RATE A-TO-B OR A-TO-Y LOAD (TOTEM POLE) OR PERI LOGIC IN TO PERI LOGIC OUT



A-TO-B LOAD OR A-TO-Y LOAD (OPEN DRAIN) OR PERI LOGIC IN TO PERI LOGIC OUT

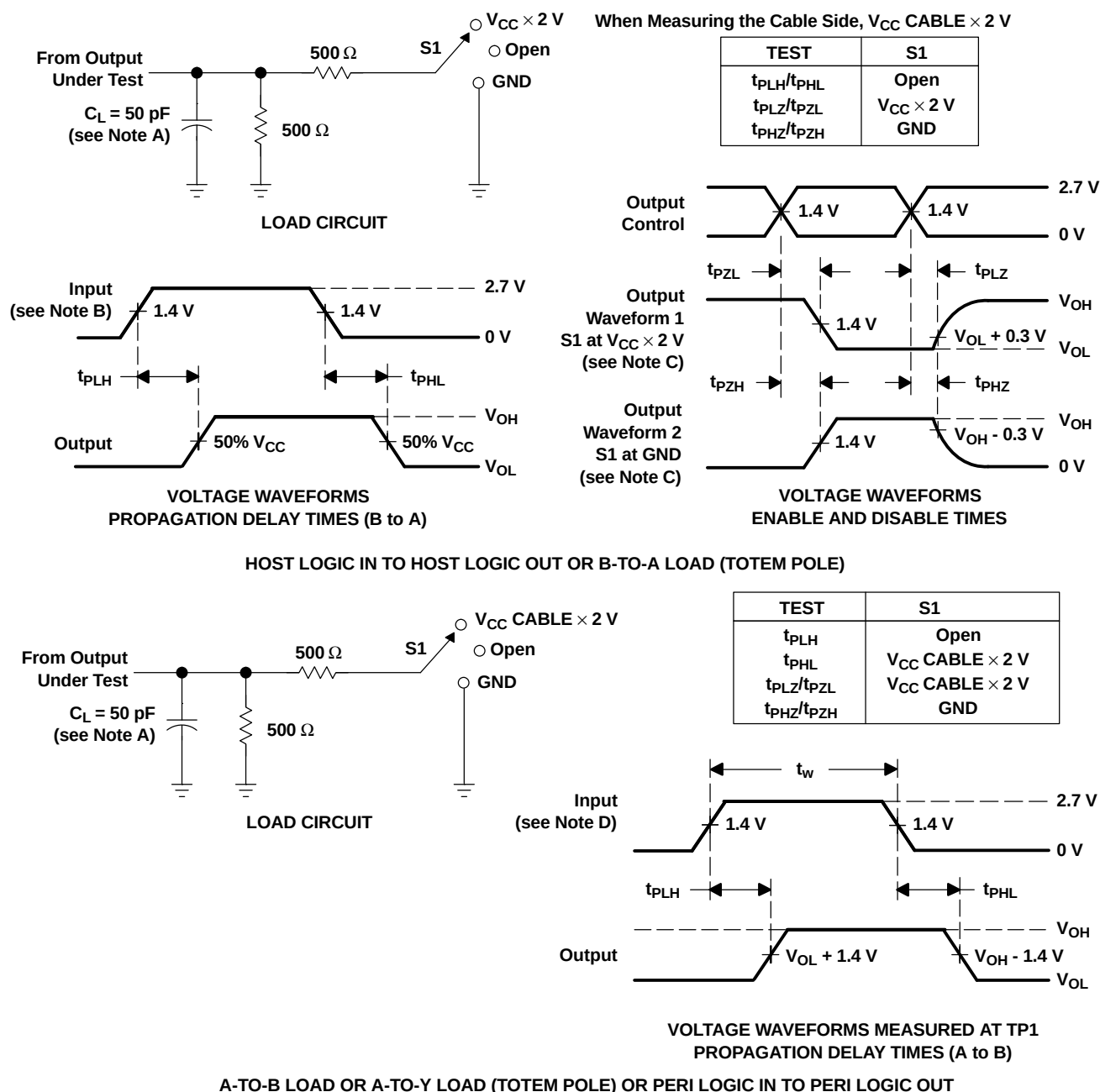
- NOTES: A. C_L includes probe and jig capacitance.
B. When V_{CC} CABLE is 3.3 V ± 0.3 V, slew rate is measured between 0.4 V and 0.9 V for the rising edge and between 2.4 V and 1.9 V for the falling edge. When V_{CC} CABLE is 5 V ± 0.5 V, slew rate is measured between 0.4 V and 1.9 V for the rising edge and between 95% V_{CC} CABLE and 50% V_{CC} CABLE for the falling edge.

$$t_{\text{slew fall}} = V_{\text{CC}} \left(\frac{95\% - 50\%}{t_{f1}} \right) \quad t_{\text{slew rise}} = \left(\frac{1.9 \text{ V} - 0.4 \text{ V}}{t_{r1}} \right)$$

- C. Input rise (t_r) and fall (t_f) times are 3 ns. Rise and fall times (open drain) are <120 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Input rise and fall times are 3 ns.
 - C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - D. Input rise and fall times are 3 ns. Pulse duration is $150 \text{ ns} < t_w < 10 \mu\text{s}$.
 - E. The outputs are measured one at a time, with one transition per measurement.
 - F. t_{PLZ} and t_{PZH} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVCE161284DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LVCE161284
SN74LVCE161284DGGR.A	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LVCE161284
SN74LVCE161284DLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LVCE161284
SN74LVCE161284DLR.A	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LVCE161284

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

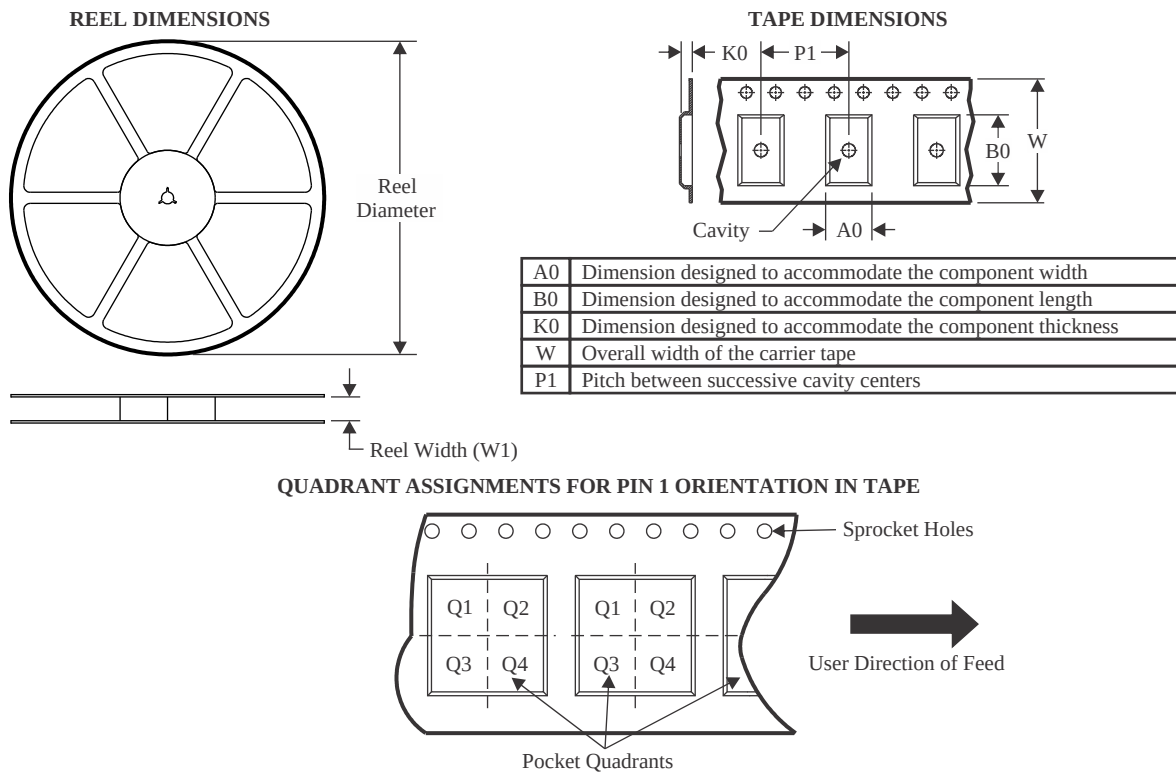
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

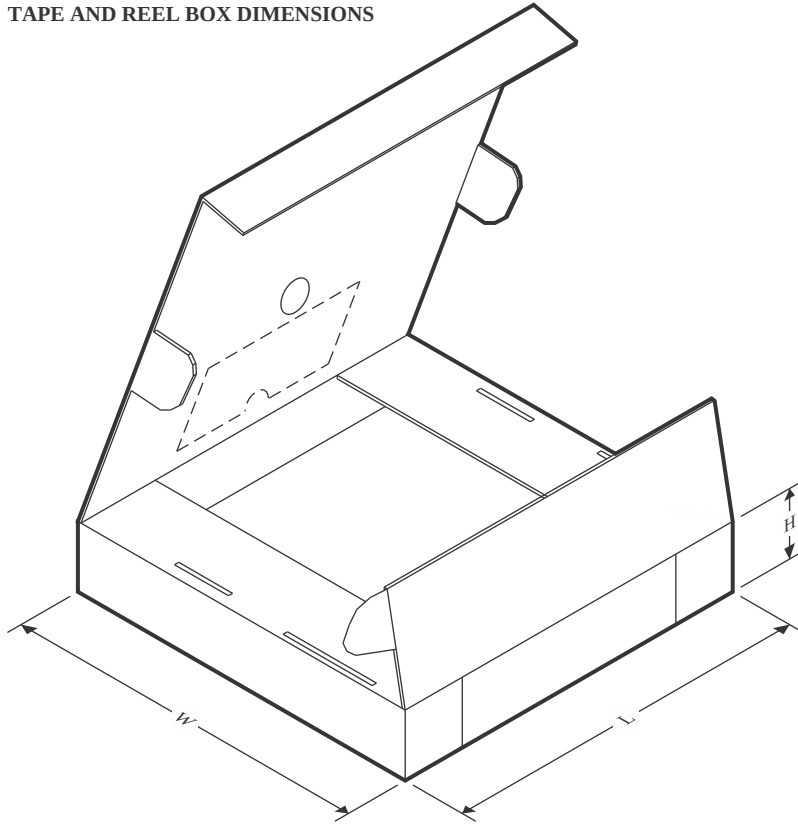
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCE161284DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVCE161284DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

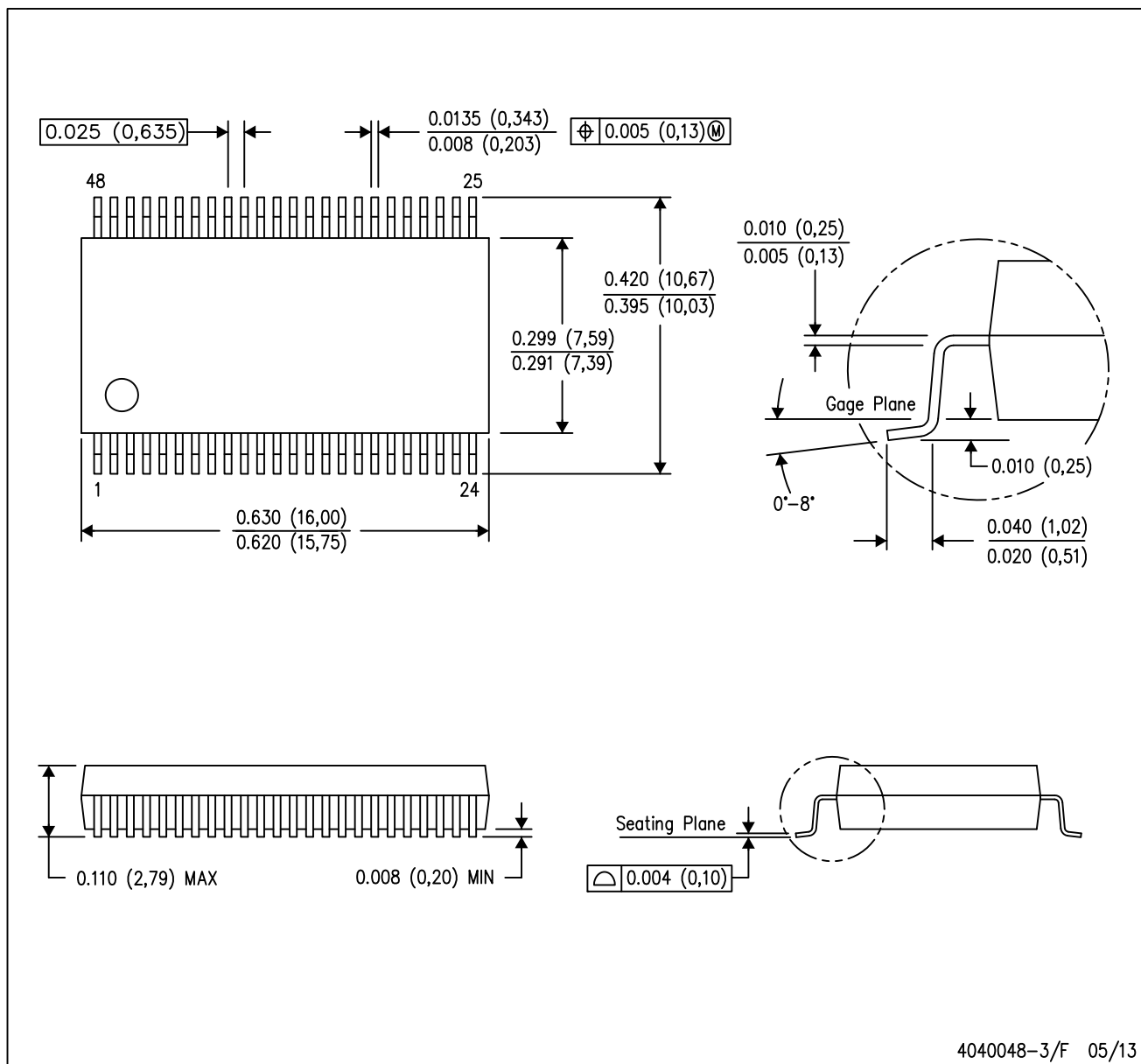


*All dimensions are nominal

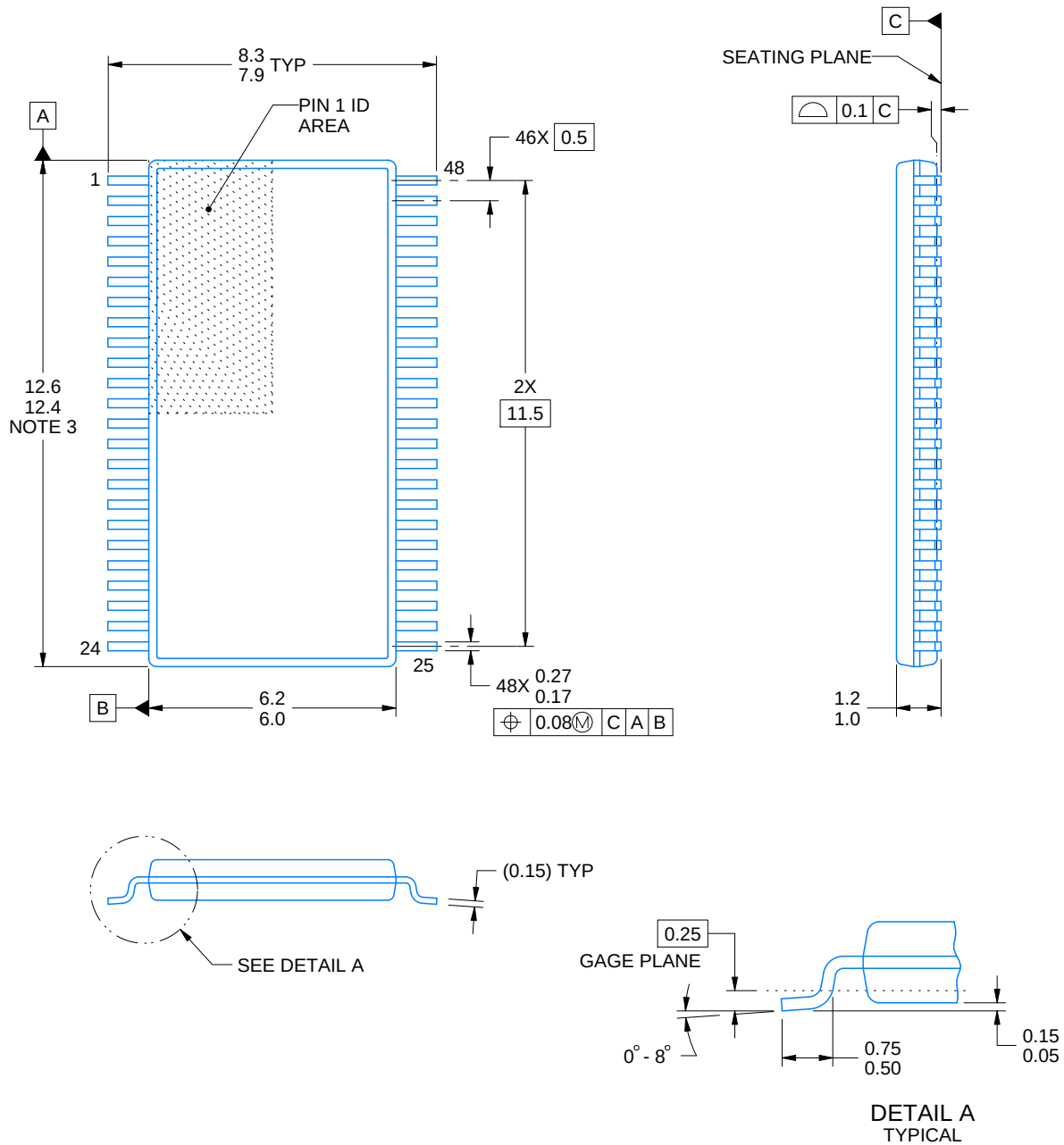
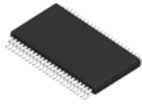
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCE161284DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVCE161284DLR	SSOP	DL	48	1000	367.0	367.0	55.0

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118



4214859/B 11/2020

NOTES:

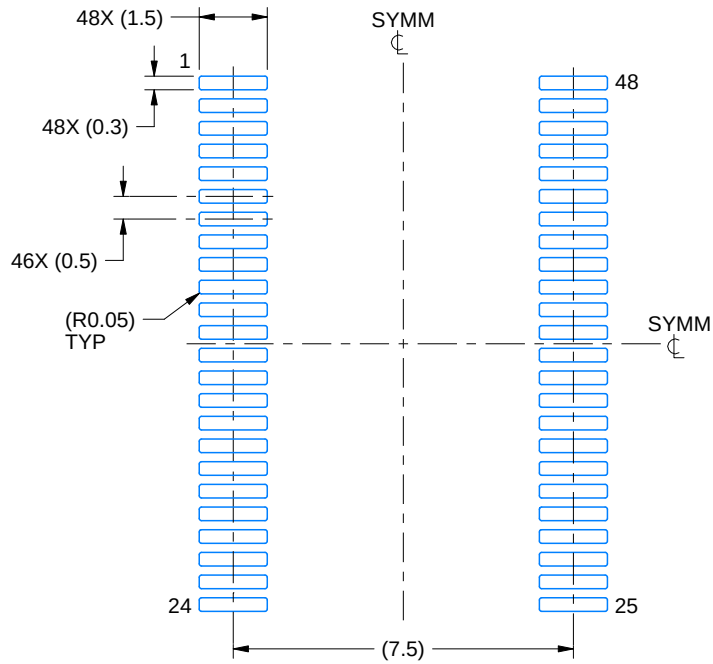
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

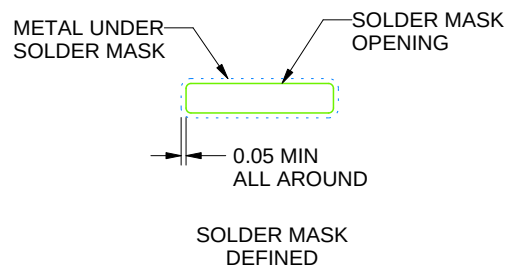
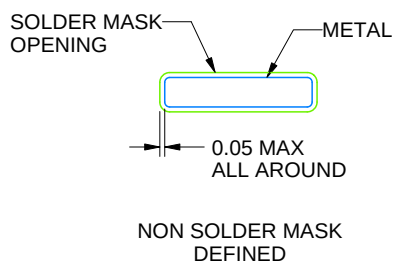
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

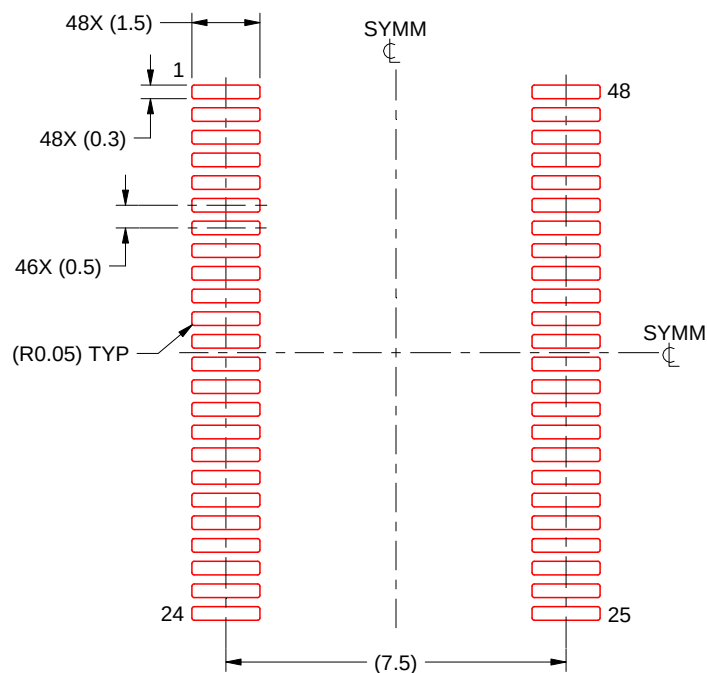
- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

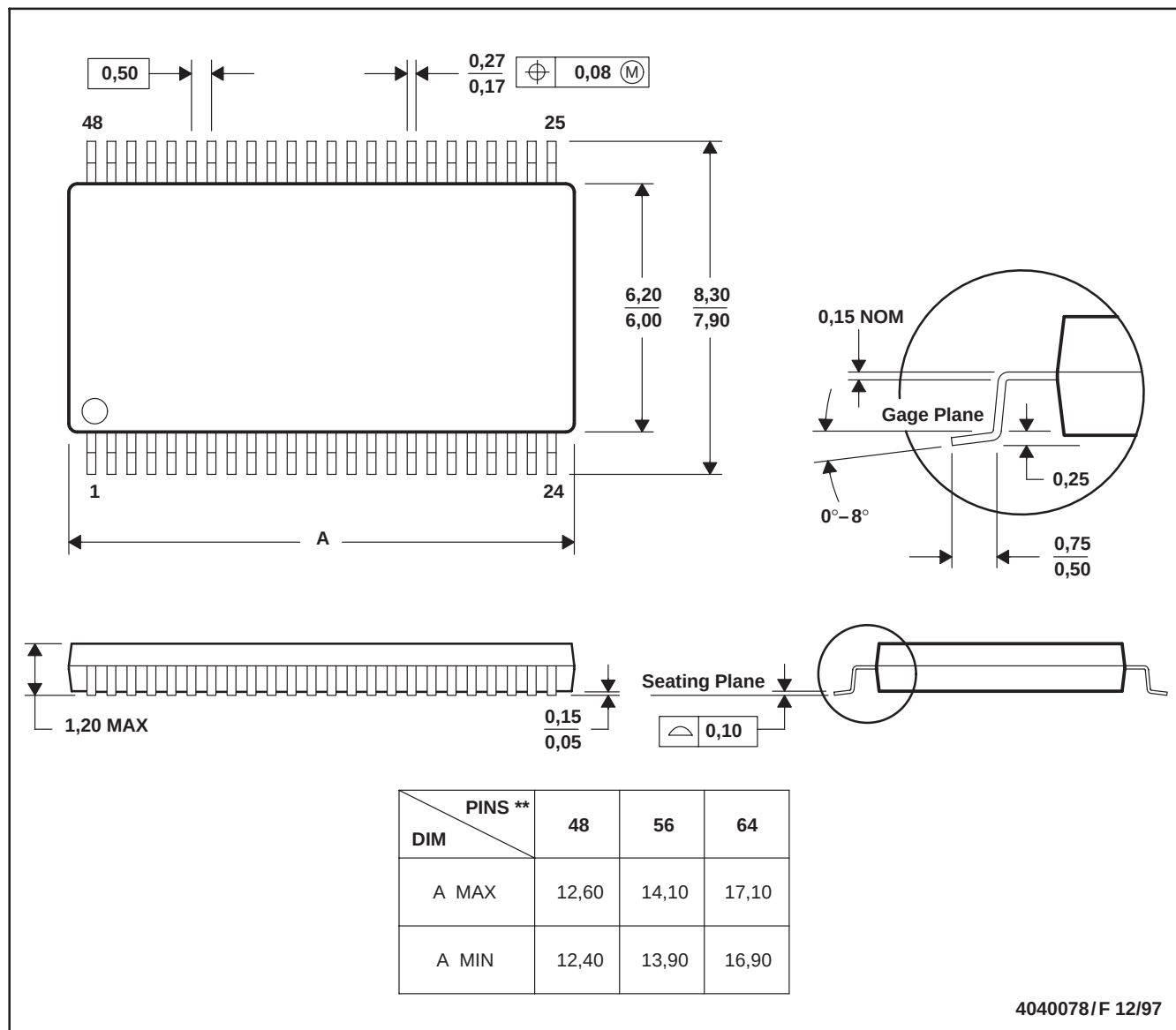
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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