

SN75LBC968 9-CHANNEL BUS TRANSCEIVER WITH ACTIVE TERMINATION

SLLS179E – APRIL 1994 – REVISED AUGUST 2005

- Nine Single-Ended SCSI Transceiver Channels With Active Termination
- Programmable Drivers Provide Active Negation (Totem Pole) or Wired-OR (Open Drain) Outputs
- 24-mA Current-Mode Active Termination With Common Nine-Channel Bus Enable
- Low Output Capacitance Presented to SCSI Bus, 13.5 pF Typ
- 3.3 V Compatible Logic Inputs Provide Bridge from 3 V Controllers to 5 V SCSI Bus
- Designed to Operate at 10-Million Data Transfers Per Second (Fast-SCSI)
- Controlled Driver Rise and Fall Times 5 ns Min
- High-Receiver Input-Voltage Hysteresis 500 mV Typ
- Receiver Input-Noise Pulse Filter 5 ns Typ
- Each Driver and Receiver Meets ANSI X3.131-1994 (SCSI-2) and the Proposed SCSI-3 Standards
- Power-Up/Power-Down Glitch Protection
- High Impedance Driver With V_{CC} at 0 V

description

The SN75LBC968 is a nine-channel transceiver with active termination that drives and receives the signals from the single-ended, parallel data buses such as the Small Computer-Systems

Interface (SCSI) bus. The features of the line drivers, receivers, and active-termination circuits provide the optimum signal-to-noise ratios for reliable data transmission. Integration of the termination and transceivers in the LinBiCMOS™ process provides the necessary analog-circuit performance, has low quiescent power, and reduces the capacitance presented to the bus over separate termination and I/O circuits.

The transceivers of the SN75LBC968 can be enabled to function as totem-pole or open-drain outputs. The open-drain mode drives the wired-OR lines of SCSI (BSY, SEL, and RST) by inputting the data to the direction control input DE/RE instead of the A input. When driving the data through the A input, the outputs become totem poles and provide active signal negation for a higher voltage level on low-to-high signal transitions on heavily loaded buses. In either mode, the turnon and turnoff output transition times are limited to minimize crosstalk through capacitive coupling to adjacent lines and RF emissions from the cable. The receivers are also designed for optimum analog performance by precisely controlling the input-voltage thresholds, providing wide input-voltage hysteresis and including an input-noise filter. These features significantly increase the likelihood of detecting only the desired data signal and rejecting noise.

DL PACKAGE
(TOP VIEW)

GND	1	56	8B
TE	2	55	GND
GND	3	54	CE
1A	4	53	NC
1DE/RE	5	52	NC
2A	6	51	NC
2DE/RE	7	50	7B
3A	8	49	NC
3DE/RE	9	48	6B
4A	10	47	NC
4DE/RE	11	46	5B
V_{CC1}	12	45	V_{CC}
GND	13	44	GND
GND	14	43	GND
GND	15	42	GND
GND	16	41	GND
GND	17	40	GND
V_{CC}	18	39	V_{CC}
5A	19	38	NC
5DE/RE	20	37	4B
6A	21	36	NC
6DE/RE	22	35	3B
7A	23	34	NC
7DE/RE	24	33	2B
8A	25	32	NC
8DE/RE	26	31	1B
9A	27	30	NC
9DE/RE	28	29	9B

NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**
WWW.TI.COM

Copyright © 2002 – 2005, Texas Instruments Incorporated

SN75LBC968

9-CHANNEL BUS TRANSCEIVER WITH ACTIVE TERMINATION

SLLS179E – APRIL 1994 – REVISED AUGUST 2005

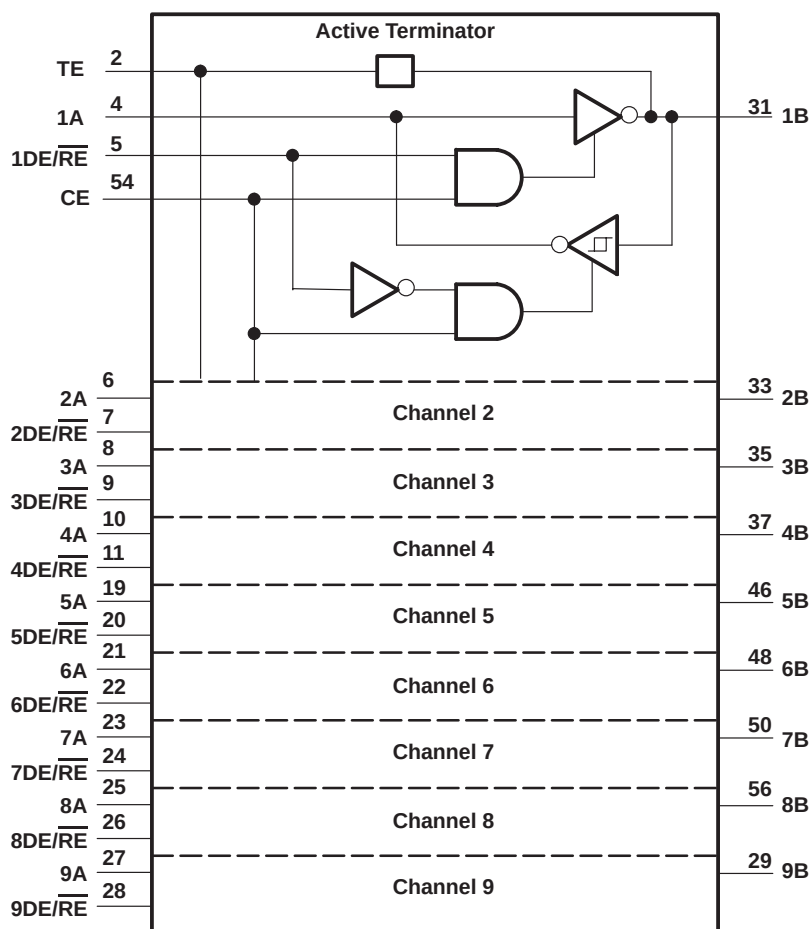
description (continued)

The communication between the SN75LBC968 and the controller can be accomplished at 3.3-V logic levels provided that the V_{CC1} input connects to the same supply rail as the controller. This provides a bridge from the lower-voltage circuit and the 5-V SCSI bus. The SN75LBC968 also removes the need for special I/O buffers (and associated power dissipation) on the controller itself. The SN75LBC968 must be used with a SCSI controller with support for Differential SCSI.

The integrated, current-mode, active termination supplies a constant 24 mA of current (TERMPWR) to the bus when the bus voltage falls below 2.5 V. This makes the next low-to-high (negation) signal transition independent of the low-level (asserted) bus voltage, unlike voltage-mode terminators. The termination current is provided through the TE input and from TERMPWR and can be disabled by letting the TE input float or by connecting it to ground. The termination circuitry is independent from the line drivers and receivers and V_{CC} or V_{CC1} . Operational termination is present as long as TERMPWR is applied.

The switching speeds of the SN75LBC968 are sufficient to transfer data over the data bus at ten million transfers per second (Fast-SCSI). The specification, $t_{sk(lim)}$, is for system skew budgeting and maintenance of bus set-up and hold times. The device is available in the space-efficient shrink-small-outline package (SSOP) with 25-mil lead pitch. The SN75LBC968 meets or exceeds the requirements of ANSI X3.131-1994 (SCSI-2) and the proposed SPI (SCSI-3) standards, and is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)



FUNCTION TABLE

	INPUTS					OUTPUTS	
	CE	DE/RE_n	A	B	TE	A	B
Terminator	L	X	X	X	GND	Z	Z
	L	X	X	X	Open	Z	Z
	L	X	X	X	V _{TE}	Z	-24 mA
Driver	H	H	L	NA	GND	Z	H
	H	H	L	NA	Open	Z	Z
	H	H	L	NA	V _{TE}	Z	-24 mA
	H	H	H	NA	GND	Z	L
	H	H	H	NA	Open	Z	L
	H	H	H	NA	V _{TE}	Z	L
Receiver	H	L	NA	L	GND	H	Z
	H	L	NA	L	Open	H	Z
	H	L	NA	L	V _{TE}	H	-24 mA
	H	L	NA	H	GND	L	Z
	H	L	NA	H	Open	L	Z
	H	L	NA	H	V _{TE}	L	-24 mA

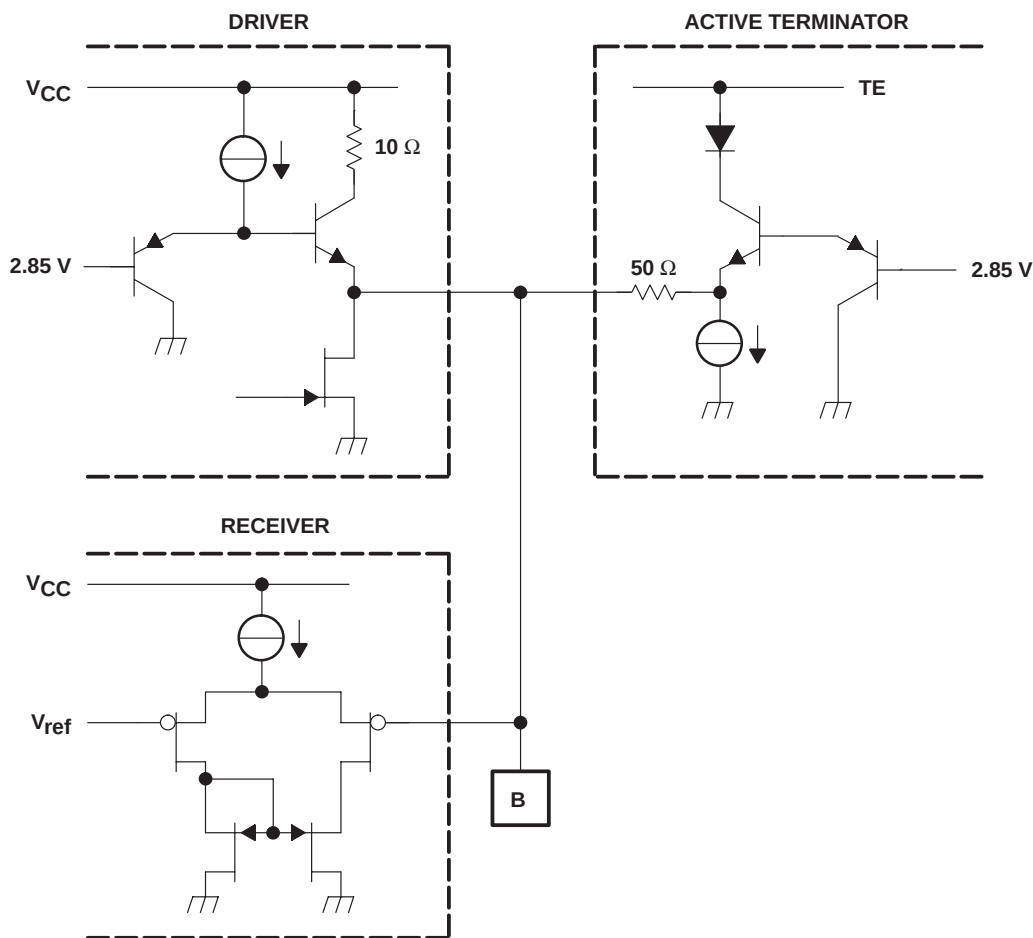
NOTE: Input A defaults to a high-level and input B a low-level if left open circuited.
 -24 mA = current-mode termination
 GND = Ground
 H = High L = Low
 NA = Not applicable
 Open = Open circuit
 V_{TE} = Termination power
 X = Don't care
 Z = High-impedance

SN75LBC968

9-CHANNEL BUS TRANSCEIVER WITH ACTIVE TERMINATION

SLLS179E – APRIL 1994 – REVISED AUGUST 2005

schematics



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} , V_{CC1} , V_{TE} (see Note 1)	–0.5 V to 7 V
Input voltage range, V_I (A-side)	$V_{CC1} + 0.3\text{ V}$
Bus voltage range (B-side)	–0.5 V to 7 V
Data I/O and control (A-side) voltage range	–0.5 V to 7 V
Continuous power dissipation (see Note 2)	Internally Limited
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

2. The maximum operating-junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR [†] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DL	2500 mW	20 mW/°C	1600 mW

[†] Derating factors are the inverse of the junction-to-ambient thermal resistance when board-mounted with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Supply voltage, V_{CC1} (see Note 3)		3		5.25	V
Termination voltage, V_{TE}		4.25		5.25	V
High-level input voltage, V_{IH}	DE/ $\overline{\text{RE}}$, CE, A, B	2			V
Low-level input voltage, V_{IL}	DE/ $\overline{\text{RE}}$, CE, A, B			0.8	V
High-level output current, I_{OH}	A			-8	mA
Low-level output current, I_{OL}	B			48	mA
	A			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 3: All electrical characteristics are measured with $V_{CC1} = V_{CC}$ unless otherwise noted.

driver electrical characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH} High-level output voltage	$I_{OH} = -20\text{ mA}$	2		V
V_{OL} Low-level output voltage	$I_{OL} = 48\text{ mA}$		0.5	V
I_{IH} High-level input current	$V_{IH} = 2\text{ V}$, $V_{CC} = V_{CC1} = 5.25\text{ V}$	-100		μA
I_{IL} Low-level input current, A	$V_{IL} = 0.5\text{ V}$, $V_{CC} = V_{CC1} = 5.25\text{ V}$	-100		μA
I_{OZ} High-impedance-state output current	$V_O = 5.25\text{ V}$, $V_{CC} = V_{CC1} = 5.25\text{ V}$	-100		μA
	$V_O = 0\text{ V}$, $V_{CC} = V_{CC1} = 5.25\text{ V}$	-100		

termination electrical characteristics over recommended operating conditions (unless otherwise noted) (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(OC)}$ Open-circuit output voltage	$I_O = 0\text{ mA}$, $V_{CC} = V_{CC1} = 0\text{ V}$	2.5	2.85	3.24	V
I_O Output current	$V_O = 0\text{ V}$, $V_{CC} = V_{CC1} = 0\text{ V}$			-24	mA
	$V_O = 0.5\text{ V}$, $V_{CC} = V_{CC1} = 0\text{ V}$	-20		-24	mA
	$V_O = 3\text{ V}$, $V_{CC} = V_{CC1} = 0\text{ V}$			100	μA
	$V_O = 4\text{ V}$, $V_{CC} = V_{CC1} = 0\text{ V}$	2		12	mA

SN75LBC968

9-CHANNEL BUS TRANSCEIVER WITH ACTIVE TERMINATION

SLLS179E – APRIL 1994 – REVISED AUGUST 2005

receiver electrical characteristics over recommended operating conditions (unless otherwise noted) (see Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = –8 mA	2	2.5		V
V _{OL}	Low-level output voltage	I _{OL} = 8 mA			0.8	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = V _{CC1}	1.2	1.6	2	V
V _{IT–}	Negative-going input threshold voltage		0.8	1.1	1.4	V
V _{hys}	Input hysteresis voltage (V _{IT+} – V _{IT–})		0.2	0.5		V
I _{IH}	High-level input current	V _{IH} = 2 V			100	μA
I _{IL}	Low-level input current	V _{IL} = 0.5 V			100	μA
I _{OZ}	High-impedance-state output current	V _O = 0 V			–100	μA
		V _O = 5.25 V			–100	

device electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
I _{CC}	Supply current to V _{CC} and V _{CC1}	All drivers, receivers, and terminator disabled		1.3	3	mA
		All receivers enabled, termination and drivers disabled, No load		14	21	
		All drivers enabled, termination and receivers disabled, No load		33	45	
				15	21	
I _{CC}	Supply current to TE	Termination and receivers enabled, No load		33	45	
C _O	Bus port capacitance (see Note 4)			13.5	16.5	pF
I _{IH}	High-level input current	DE/ $\overline{\text{RE}}$, CE			100	μA
I _{IL}	Low-level input current	DE/ $\overline{\text{RE}}$, CE			100	μA

[†] All typical values are at V_{CC} = V_{CC1} = 5 V, T_A = 25°C.

NOTE 4: Tested in accordance with Annex G X3T9.2/855D, revision 14

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
t _{PHL}	Propagation delay time, high- to low-level output (see Figure 4)	C _L = 15 pF	10		35	ns
t _{PLH}	Propagation delay time, low- to high-level output (see Figure 4)		15		45	ns
t _{sk(lim)}	Skew limit [‡] , the maximum delay time – minimum delay time	V _{CC} = V _{CC1} = 5 V, T _A = 25°C, C _L = 15 pF			14	ns
		V _{CC} = V _{CC1} = 5 V, T _A = 70°C, C _L = 15 pF			14	ns
t _{sk(p)}	Pulse skew, t _{PHL} – t _{PLH}	V _{CC} = V _{CC1} = 5 V, T _A = 25°C		8		ns
t _t	Output transition time, 10% to 90% or 90% to 10% of the steady-state output	15 pF < C _L < 100 pF	5		20	ns
t _{PLZ}	Propagation delay time, low-level to high-impedance output (see Figure 5)	From CE, C _L = 15 pF	5		150	ns
		From DE/ $\overline{\text{RE}}$, C _L = 15 pF			45	
t _{PZL}	Propagation delay time, high-impedance to low-level output (see Figure 5)	From CE, C _L = 15 pF	5		150	ns
		From DE/ $\overline{\text{RE}}$, C _L = 15 pF			45	

[†] All typical values are at V_{CC} = V_{CC1} = 5 V, T_A = 25°C.

[‡] The value for this parameter was derived from the difference between the slowest and the fastest driver delay times measured on devices from four sample wafer lots.

receiver switching characteristics over recommended of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
t _{PHL}	Propagation delay time, high- to low-level output	See Figure 6	5		20	ns
t _{PLH}	Propagation delay time, low- to high-level output		5		25	ns
t _{sk(lim)}	Skew limit [‡] , the maximum delay time – minimum delay time	V _{CC} = V _{CC1} = 5 V, T _A = 25°C, See Figure 6			8.5	ns
		V _{CC} = V _{CC1} = 5 V, T _A = 70°C, See Figure 6			8.5	ns
t _{sk(p)}	Pulse skew, t _{PHL} – t _{PLH}	V _{CC} = V _{CC1} = 5 V, T _A = 25°C, See Figure 6		6		ns
t _{PLZ}	Propagation delay time, low-level to high-impedance output	From CE, See Figure 7	5		150	ns
		From DE/ $\overline{\text{RE}}$, See Figure 7			45	
t _{PZL}	Propagation delay time, high-impedance to low-level output	From CE, See Figure 7	5		150	ns
		From DE/ $\overline{\text{RE}}$, See Figure 7			80	
t _{PHZ}	Propagation delay time, high-level to high-impedance output	From CE, See Figure 8	5		150	ns
		From DE/ $\overline{\text{RE}}$, See Figure 8			45	
t _{PZH}	Propagation delay time, high-impedance to high-level output	From CE, See Figure 8	5		150	ns
		From DE/ $\overline{\text{RE}}$, See Figure 8			80	

[†] All typical values are at V_{CC} = V_{CC1} = 5 V, T_A = 25°C.

[‡] The value for this parameter was derived from the difference between the slowest and the fastest driver delay times measured on devices from four sample wafer lots.

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{θJA}	Junction-to-free-air thermal resistance	Board-mounted, no air flow		50		°C/W
R _{θJC}	Junction-to-case thermal resistance			12		°C/W
T _{JS}	Junction-shutdown temperature			180		°C

PARAMETER MEASUREMENT INFORMATION

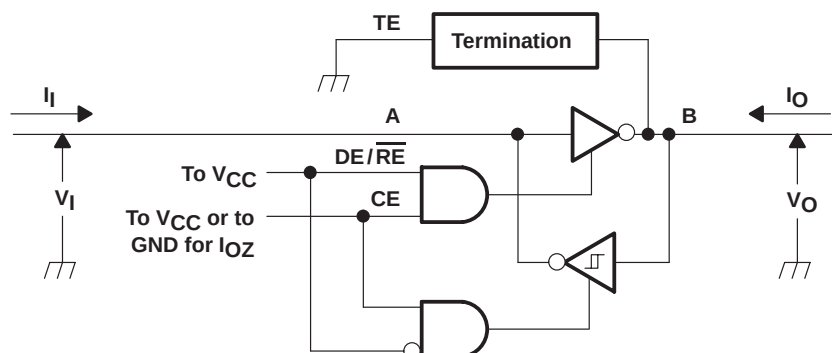


Figure 1. Driver Test Circuit Currents and Voltages.

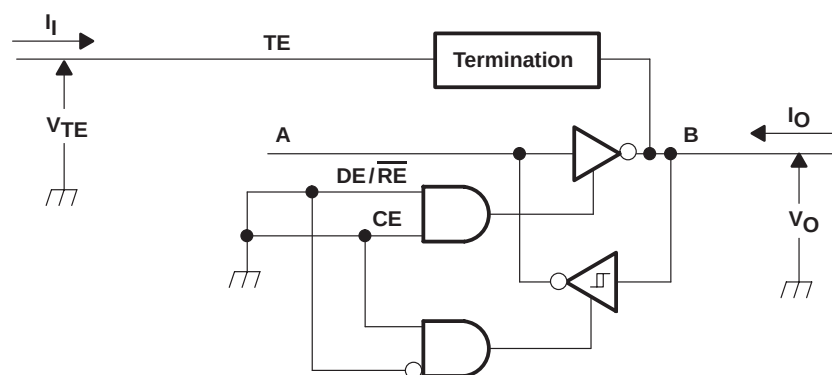


Figure 2. Active Termination Voltages, Currents, and Test Circuit.

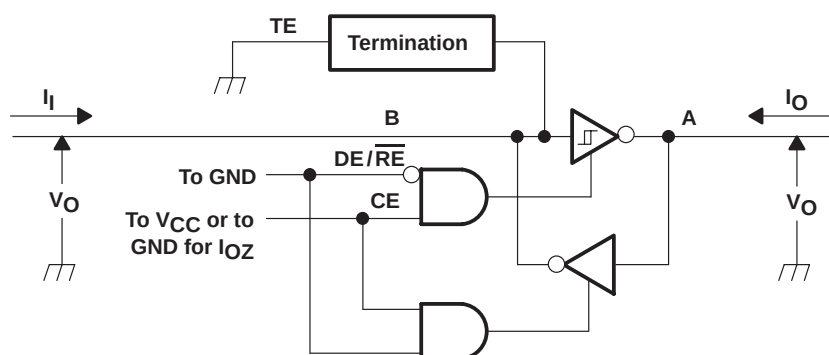
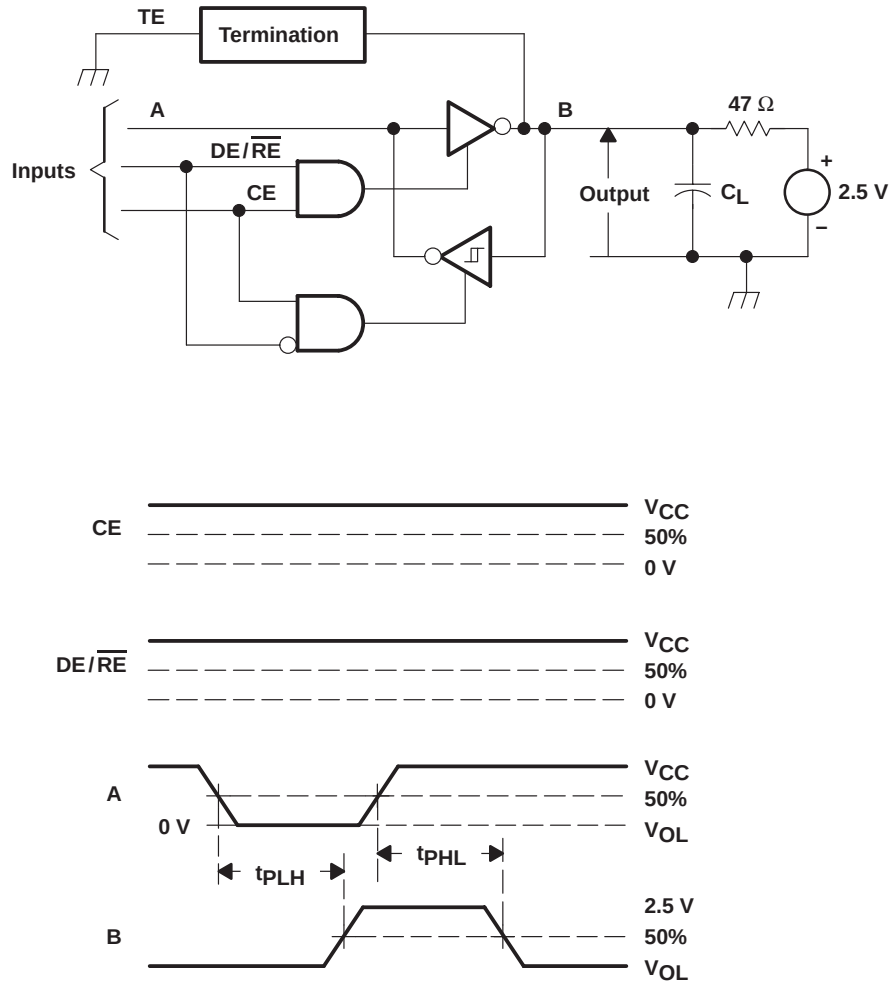


Figure 3. Receiver Voltages, Currents, and Test Circuit

- NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, $PRR \leq 1$ MHz, duty cycle = 50%, $Z_O = 50 \Omega$.
 B. All resistances are in ohms and $\pm 5\%$, unless otherwise indicated.
 C. All capacitances are in picofarads and $\pm 10\%$, unless otherwise indicated.
 D. All indicated voltages are ± 10 mV.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, $PRR \leq 1$ MHz, duty cycle = 50%, $Z_O = 50 \Omega$.
 B. All resistances are in ohms and $\pm 5\%$, unless otherwise indicated.
 C. All capacitances are in picofarads and $\pm 10\%$, unless otherwise indicated.
 D. All indicated voltages are ± 10 mV.

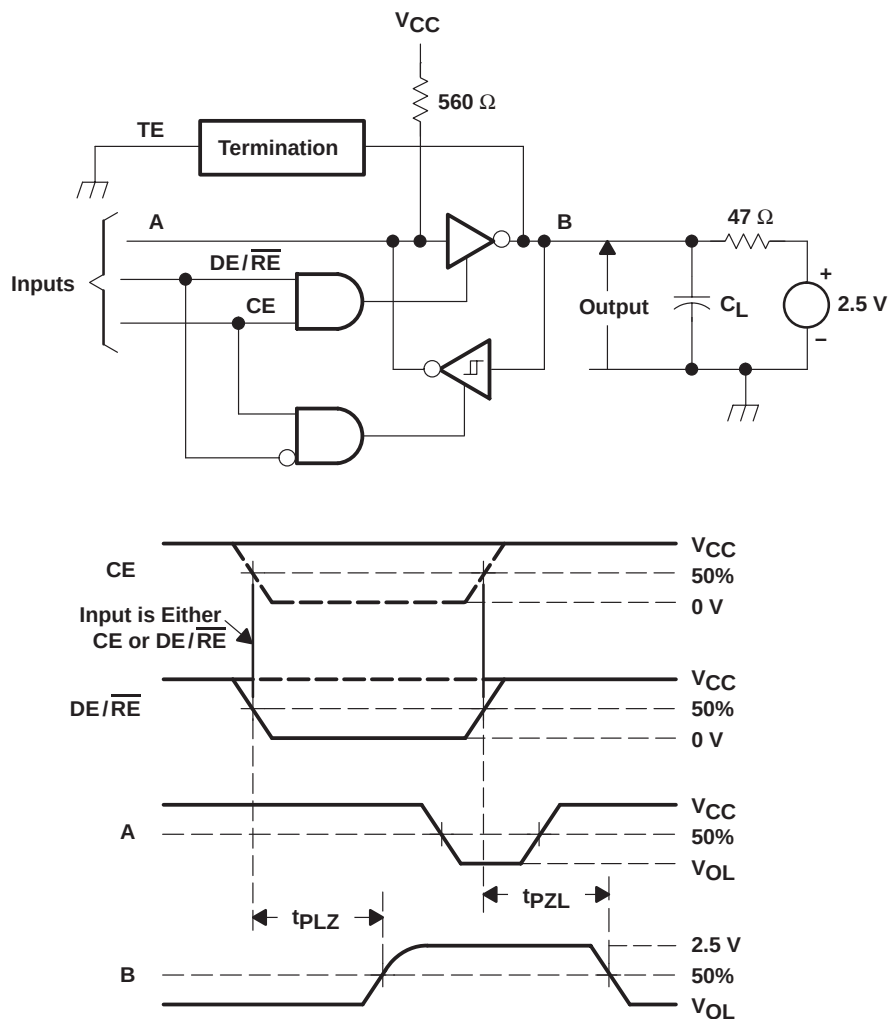
Figure 4. Driver Delay Time Test Circuit and Waveforms

SN75LBC968

9-CHANNEL BUS TRANSCEIVER WITH ACTIVE TERMINATION

SLLS179E – APRIL 1994 – REVISED AUGUST 2005

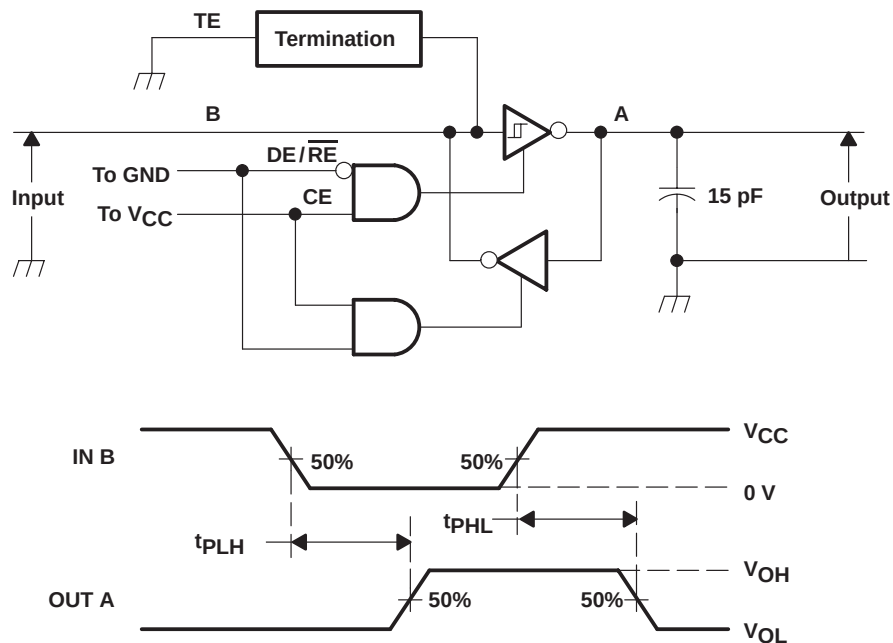
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, $PRR \leq 1$ MHz, duty cycle = 50%, $Z_O = 50$ ohms.
- B. All resistances are in ohms and $\pm 5\%$, unless otherwise indicated.
- C. All capacitances are in picofarads and $\pm 10\%$, unless otherwise indicated.
- D. All indicated voltages are ± 10 mV.

Figure 5. Driver Delay Time Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$, $PRR \leq 1\text{ MHz}$, duty cycle = 50%, $Z_O = 50\ \Omega$.
 - B. All resistances are in ohms and $\pm 5\%$, unless otherwise indicated.
 - C. All capacitances are in picofarads and $\pm 10\%$, unless otherwise indicated.
 - D. All indicated voltages are $\pm 10\text{ mV}$.

Figure 6. Receiver Propagation Delay Time Test Circuit and Waveforms

SLLS179E – APRIL 1994 – REVISED AUGUST 2005

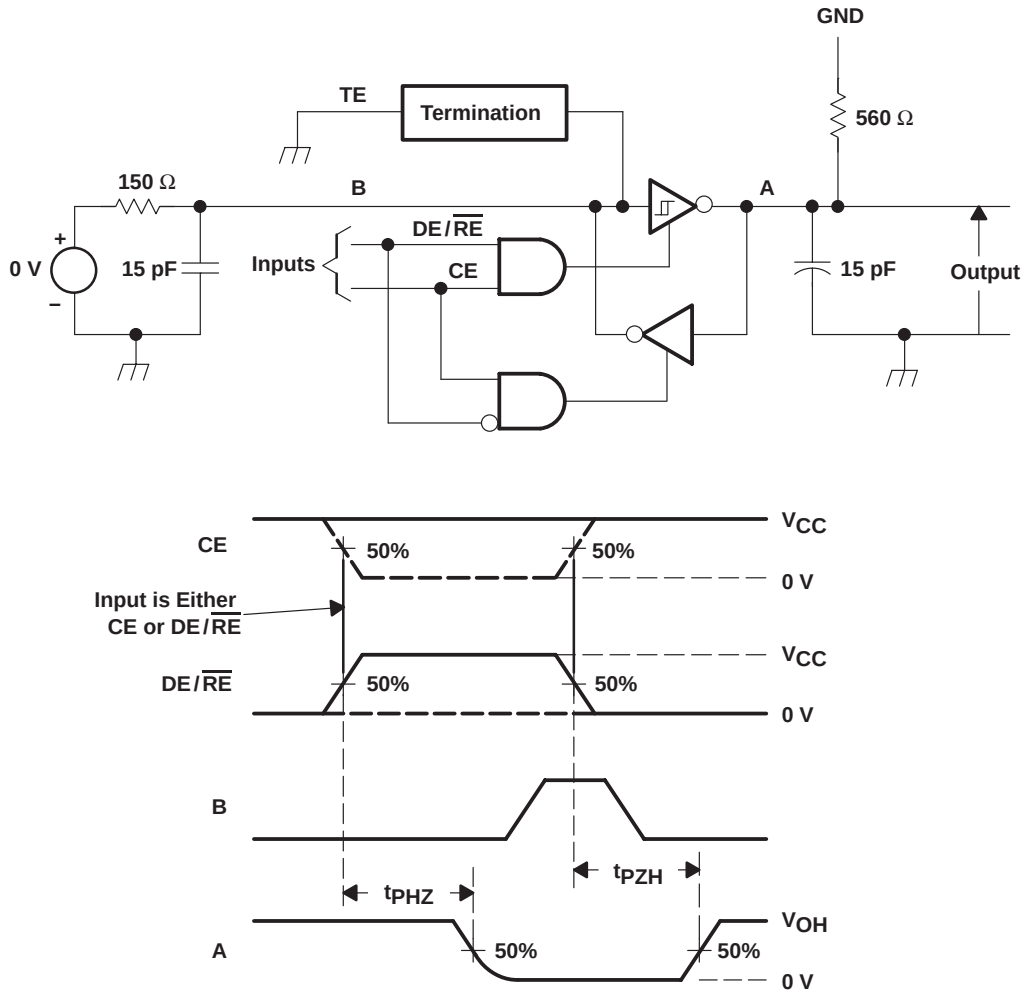
The figure consists of two parts: a circuit diagram and a timing diagram.

Circuit Diagram: A 2.5 V DC source is connected in series with a 47 Ω resistor and a 15 pF capacitor to the input of a 74VHC04 inverter. The input is also connected to a bus with inputs B, DE/RE, and CE. A termination block is connected to the input bus. The output of the inverter is connected to a 560 Ω resistor and a 15 pF capacitor, and is labeled "Output".

Timing Diagram: The diagram shows the timing relationships between the inputs and the output. The inputs are CE, DE/RE, and B. The output is A. The diagram shows the propagation delays t_{PLZ} and t_{PZL} , and the output levels V_{OH} and V_{OL} . The inputs CE and DE/RE are square waves with 50% duty cycle. The input B is a square wave. The output A shows the propagation delays t_{PLZ} and t_{PZL} , and is labeled with V_{OH} and V_{OL} levels.

Figure 7. Receiver Enable and Disable Times to and From Low-Level Output Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $\text{PRR} \leq 1 \text{ MHz}$, duty cycle = 50%, $Z_O = 50 \Omega$.
 B. All resistances are in ohms and $\pm 5\%$, unless otherwise indicated.
 C. All capacitances are in picofarads and $\pm 10\%$, unless otherwise indicated.
 D. All indicated voltages are $\pm 10 \text{ mV}$.

Figure 8. Receiver Enable and Disable Times to and From High-Level Output Test Circuit and Waveforms

SN75LBC968

9-CHANNEL BUS TRANSCEIVER

WITH ACTIVE TERMINATION

SLLS179E – APRIL 1994 – REVISED AUGUST 2005

TYPICAL CHARACTERISTICS

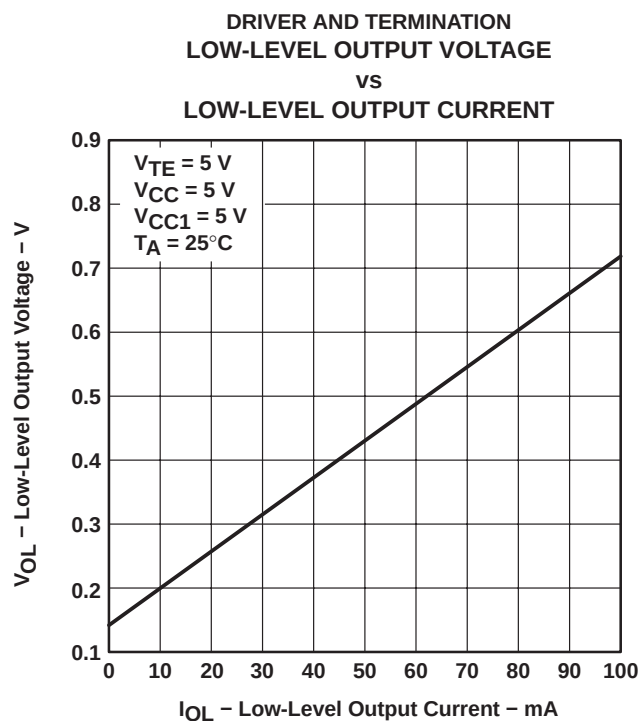


Figure 9

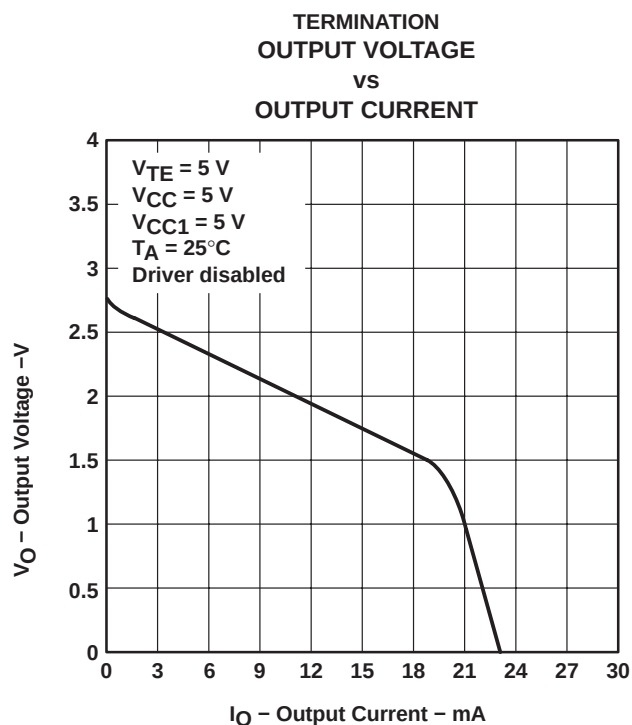


Figure 10

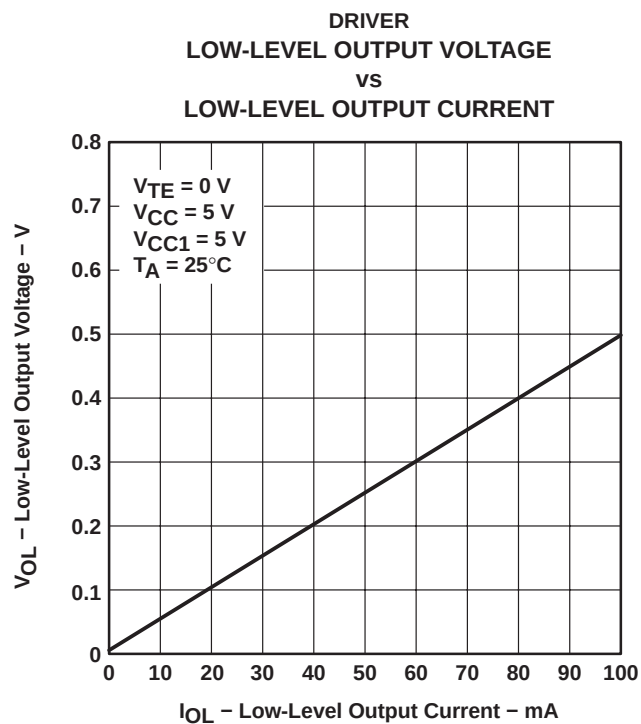


Figure 11

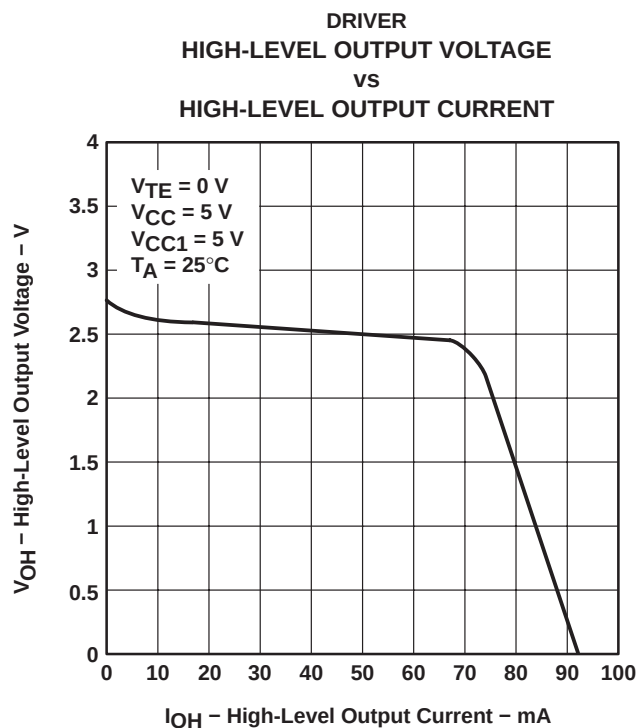


Figure 12

TYPICAL CHARACTERISTICS

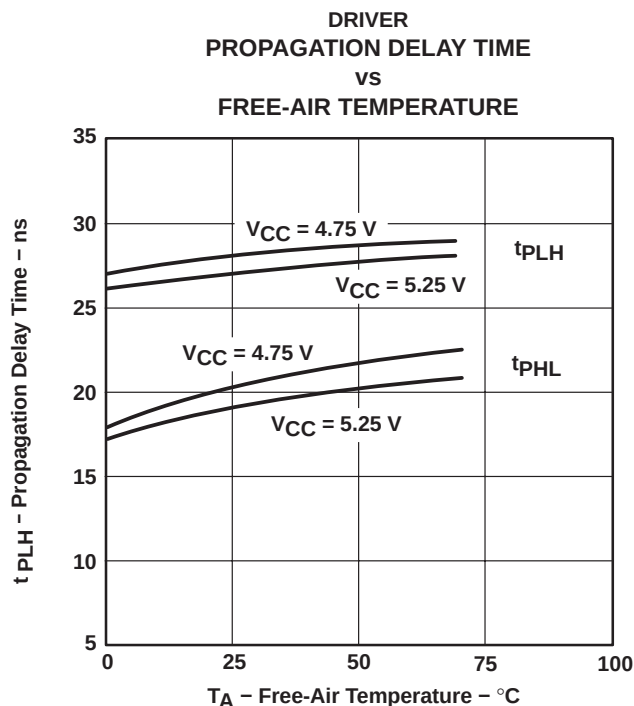


Figure 13

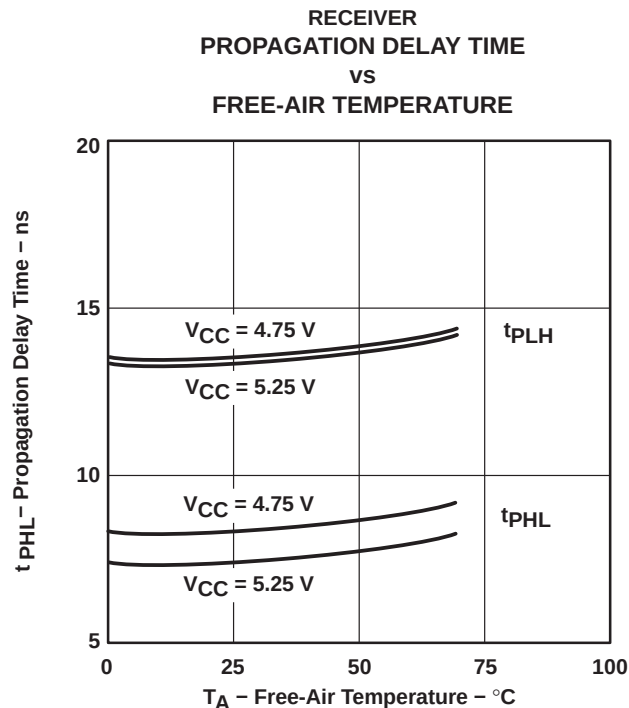


Figure 14

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LBC968DL	Last Time Buy	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LBC968
SN75LBC968DL.A	NRND	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LBC968

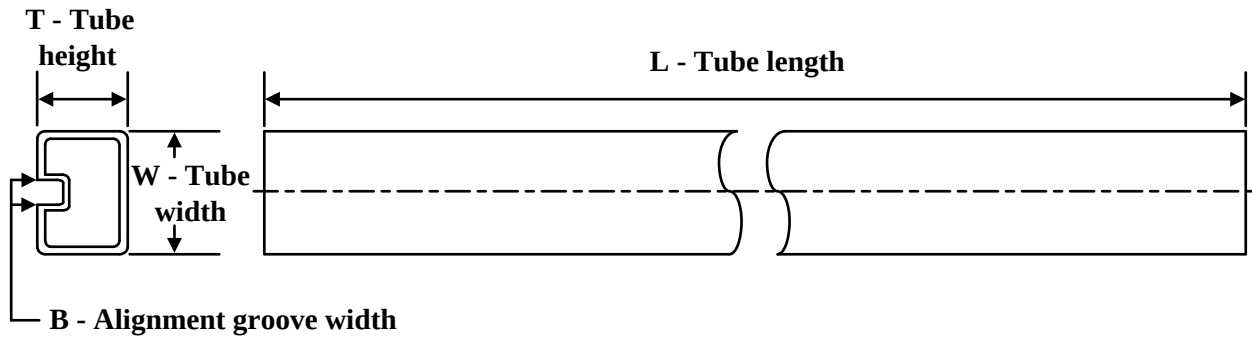
- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE

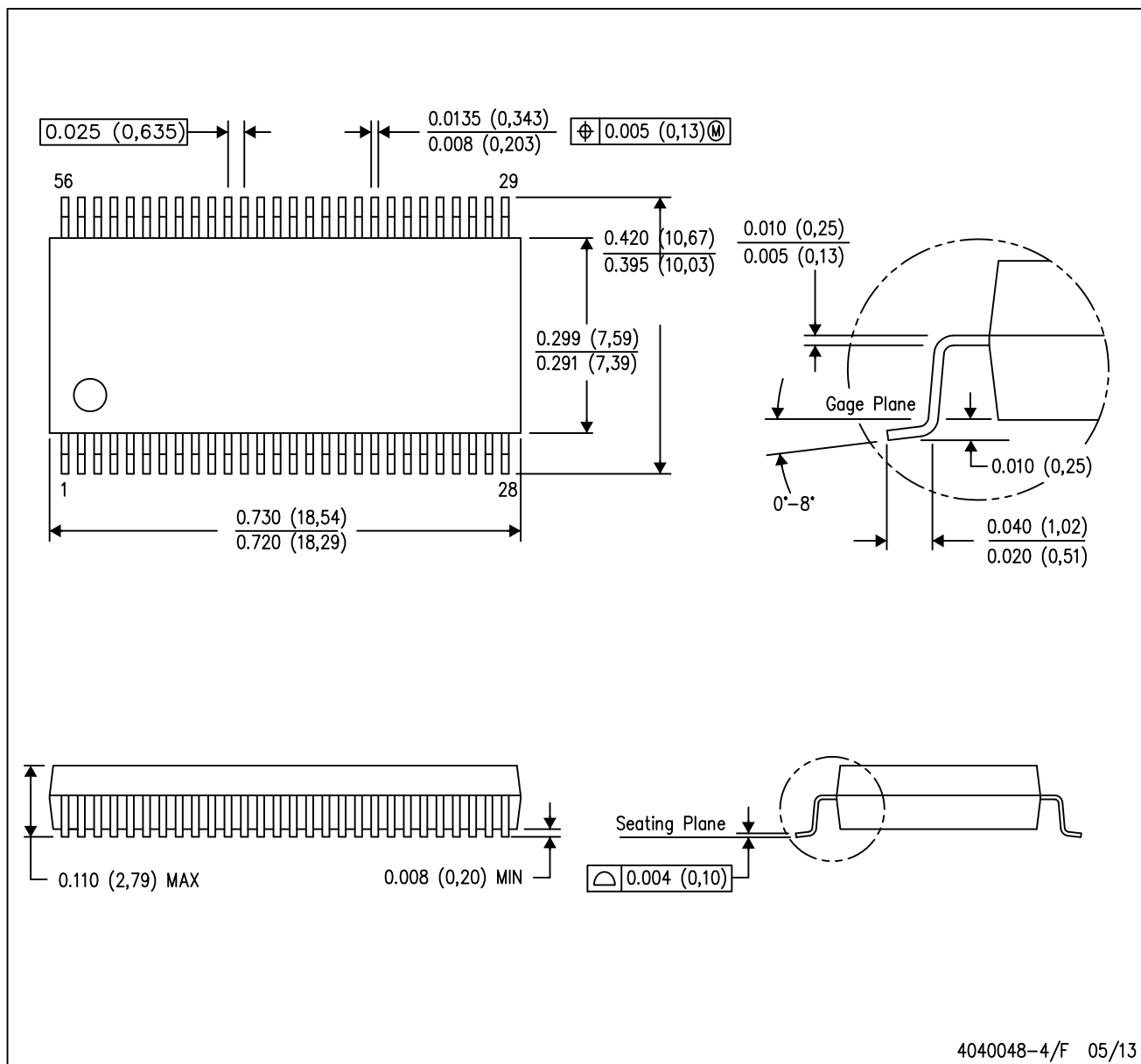


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75LBC968DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN75LBC968DL.A	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated