LMC604x CMOS, Dual, Micropower Operational Amplifiers

1 Features

- Typical values unless otherwise noted
- Low supply current: 10µA/amp
- Supply range: 4.5V to 15V, single supply
- Ultra-low input current: 2fA
- Rail-to-rail output swing
- Input common-mode includes ground

2 Applications

- Battery monitoring and power conditioning
- Photodiode and infrared-detector preamplifier
- Silicon-based transducer systems
- Portable analytic instruments
- pH-probe buffer amplifier
- Fire- and smoke-detection systems
- Charge amplifier for piezoelectric transducers

3 Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6041, LMC6042, and LMC6044 (LMC604x). Providing input currents of only 2fA (typical), the LMC604x operate from a single supply, with an output swing extending to each supply rail and an input voltage range that includes ground.

The LMC604x are designed for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, the high output drive, and an output swing to ground without requiring external pulldown resistors make these op amps an excellent choice for single-supply, battery-powered systems.

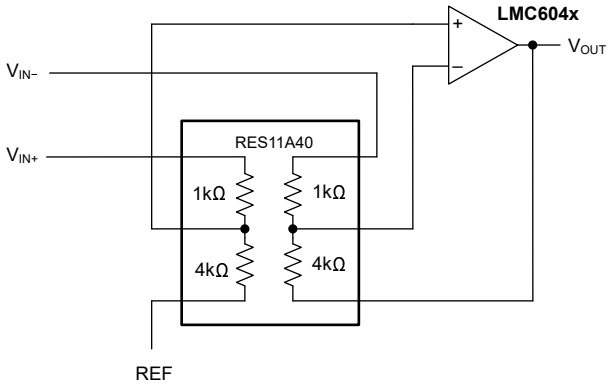
Other applications for the LMC604x include barcode-reader amplifiers, magnetic- and electric-field detectors, and portable electrometers.

This device is built with TI's advanced double-poly silicon-gate CMOS process.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
LMC6041	Single	D (SOIC, 8)
		P (PDIP, 8)
LMC6042	Dual	D (SOIC, 8)
		P (PDIP, 8)
LMC6044	Quad	D (SOIC, 14)
		N (PDIP, 14)

(1) For more information, see Section 9.



Difference Amplifier Application With RES11A

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4 Pin Configuration and Functions

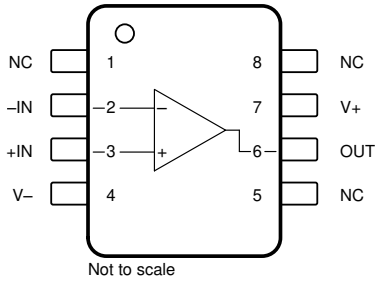

Figure 4-1. LMC6041: D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP (Top View)

Table 4-1. Pin Functions: LMC6041

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN	2	Input	Inverting input
+IN	3	Input	Noninverting input
NC	1, 5, 8	_	No connection. Leave unconnected or float this pin.
OUT	6	Output	Output
V–	4	Power	Negative (lowest) power supply
V+	7	Power	Positive (highest) power supply

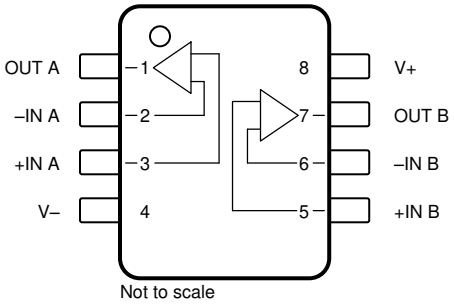

Figure 4-2. LMC6042: D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP (Top View)

Table 4-2. Pin Functions: LMC6042

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
–IN B	6	Input	Inverting input channel B
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
V–	4	Power	Negative supply
V+	8	Power	Positive supply

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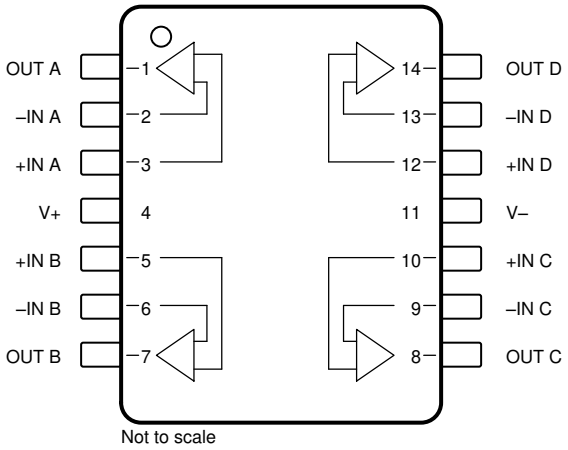

Figure 4-3. LMC6044: D Package, 14-Pin SOIC, and N Package, 14-Pin PDIP (Top View)

Table 4-3. Pin Functions: LMC6044

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
–IN B	6	Input	Inverting input channel B
–IN C	9	Input	Inverting input channel C
–IN D	13	Input	Inverting input channel D
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
+IN C	10	Input	Noninverting input channel C
+IN D	12	Input	Noninverting input channel D
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
OUT C	8	Output	Output channel C
OUT D	14	Output	Output channel D
V–	11	Power	Negative supply
V+	4	Power	Positive supply

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
	Differential input voltage			±Supply voltage	
V_S	Supply voltage, V_S = (V+) – (V–)			16	V
I_{SC}	Output short circuit(5)	To V+		See(3)	
		To V–		See(4)	
	Voltage at input/output pin		(V–) – 0.3	(V+) + 0.3	V
	Current at input pin			±5	mA
	Current at output pin			±18	
	Current at power supply pin			35	
P_D	Power dissipation			See(5)	
	Lead temperature (soldering, 10s)			260	°C
T_J	Junction temperature(5)			110	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Do not connect output to V+ when V+ is greater than 13V or reliability can be adversely affected.
(4) Applies to both single-supply operation. Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30mA over the long term can adversely affect reliability.
(5) The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A) / \theta_{JA}$.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply	4.5		15.5	V
		Dual supply	±2.25		±7.75	
P_D	Power dissipation				See(1)	
	Specified temperature		–40		+85	°C

(1) To operate the device at elevated temperatures, derate the device based on thermal resistance θ_{JA} with $P_D = (T_J - T_A) / \theta_{JA}$.

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5.4 Thermal Information: LMC6041

THERMAL METRIC[1]		LMC6041		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.0	101.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	57.9	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.3	38.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.0	18.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.5	37.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information: LMC6042

THERMAL METRIC[1]		LMC6042		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.0	101.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	52.0	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.9	38.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	18.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.1	37.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Thermal Information: LMC6044

THERMAL METRIC[1]		LMC6044		UNIT
		D (SOIC)	N (PDIP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.0	85.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	34.6	28.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.3	32.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.7	15.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.7	32.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.7 Electrical Characteristics

at $T_J = T_A = 25°C$, V+ = 5V, V– = 0V, $V_{CM} = 1.5V$, $V_{OUT} = V_S / 2$, and $R_L = 1M\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	LMC604xAI			±1	±3	mV
			T_A = –40°C to +85°C			±3.3	
		LMC604xI			±1	±6	
			T_A = –40°C to +85°C			±6.3	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			1.3		µV/°C
PSRR	Power-supply rejection ratio	Positive 5V ≤ V+ ≤ 15V, V_{OUT} = 2.5V	LMC604xAI	68	75		dB
			LMC604xAI, T_A = –40°C to +85°C	66			
			LMC604xI	62	75		
			LMC604xI, T_A = –40°C to +85°C	60			
		Negative 0V ≤ V– ≤ –10V, V_{OUT} = 2.5V	LMC604xAI	84	94		
			LMC604xAI, T_A = –40°C to +85°C	83			
			LMC604xI	74	94		
			LMC604xI, T_A = –40°C to +85°C	73			
INPUT BIAS CURRENT							
I_B	Input bias current				±2		fA
		T_A = –40°C to +85°C				±4	pA
I_{OS}	Input offset current				±1		fA
		T_A = –40°C to +85°C				±2	pA
NOISE							
e_n	Input voltage noise density	f = 1kHz			83		nV/√Hz
i_n	Input current noise density	f = 1kHz			12.5		fA/√Hz
THD	Total harmonic distortion	f = 1kHz, gain = – 5V/V, R_L = 100kΩ, $V_{OUT} = 12V_{pp}$, V+ = 15V			1		%
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	To positive rail V+ = 5V and 15V, CMRR ≥ 50dB		(V+) – 2.3	(V+) – 1.9		V
			LMC604xAI, T_A = –40°C to +85°C	(V+) – 2.5			
			LMC604xI, T_A = –40°C to +85°C	(V+) – 2.4			
		To negative rail V+ = 5V and 15V, CMRR ≥ 50dB			– 0.4	– 0.1	
			T_A = –40°C to +85°C			0	
CMRR	Common-mode rejection ratio	V+ = 15V, 0V ≤ V_{CM} ≤ 12V	LMC604xAI	68	75		dB
			LMC604xAI, T_A = –40°C to +85°C	66			
			LMC604xI	62	75		
			LMC604xI, T_A = –40°C to +85°C	60			
INPUT IMPEDANCE							
R_{IN}	Input resistance				>10		TΩ

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5.7 Electrical Characteristics (continued)

at $T_J = T_A = 25°C$, V+ = 5V, V– = 0V, $V_{CM} = 1.5V$, $V_{OUT} = V_S / 2$, and $R_L = 1M\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	Sourcing, V+ = 15V, 7.5V ≤ V_O ≤ 11.5V, R_L = 100kΩ to V+ / 2	LMC604xAI	300	1000		V/mV
			LMC604xAI, T_A = –40°C to +85°C	200			
			LMC604xI	300	1000		
			LMC604xI, T_A = –40°C to +85°C	200			
		Sinking, V+ = 15V, 2.5V ≤ V_O ≤ 7.5V, R_L = 100kΩ to V+ / 2	LMC604xAI	180	500		
			LMC604xAI, T_A = –40°C to +85°C	120			
			LMC604xI	90	500		
			LMC604xI, T_A = –40°C to +85°C	70			
		Sourcing, V+ = 15V, 7.5V ≤ V_O ≤ 11.5V, R_L = 25kΩ to V+ / 2	LMC604xAI	200	1000		
			LMC604xAI, T_A = –40°C to +85°C	160			
			LMC604xI	100	1000		
			LMC604xI, T_A = –40°C to +85°C	80			
		Sinking, V+ = 15V, 2.5V ≤ V_O ≤ 7.5V, R_L = 25kΩ to V+ / 2	LMC604xAI	100	250		
			LMC604xAI, T_A = –40°C to +85°C	60			
			LMC604xI	50	250		
			LMC604xI, T_A = –40°C to +85°C	40			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product	LMC6041			75		kHz
		LMC6042 and LMC6044			100		
SR	Slew rate[1]	V+ = 15V, 10V step, gain = 1	LMC604xAI	0.015	0.02		V/µs
			LMC604xAI, T_A = –40°C to +85°C	0.010			
			LMC604xI	0.010	0.02		
			LMC604xI, T_A = –40°C to +85°C	0.007			
	Crosstalk	Dual and quad channel, V+ = 15V, R_L = 100kΩ, f = 100Hz, $V_{OUT} = 12V_{pp}$			115		dB

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5.7 Electrical Characteristics (continued)

at $T_J = T_A = 25°C$, V+ = 5V, V– = 0V, $V_{CM} = 1.5V$, $V_{OUT} = V_S / 2$, and $R_L = 1M\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing	Positive rail V+ = 5V, R_L = 100kΩ to V+ / 2	LMC604xAI	4.970	4.987		V
			LMC604xAI, T_A = –40°C to +85°C	4.950			
			LMC604xI	4.940	4.987		
			LMC604xI, T_A = –40°C to +85°C	4.910			
		Negative rail V+ = 5V, R_L = 100kΩ to V+ / 2	LMC604xAI		0.004	0.030	
			LMC604xAI, T_A = –40°C to +85°C			0.050	
			LMC604xI		0.004	0.060	
			LMC604xI, T_A = –40°C to +85°C			0.090	
		Positive rail V+ = 5V, R_L = 25kΩ to V+ / 2	LMC604xAI	4.920	4.980		
			LMC604xAI, T_A = –40°C to +85°C	4.870			
			LMC604xI	4.870	4.980		
			LMC604xI, T_A = –40°C to +85°C	4.820			
		Negative rail V+ = 5V, R_L = 25kΩ to V+ / 2	LMC604xAI		0.010	0.080	
			LMC604xAI, T_A = –40°C to +85°C			0.130	
			LMC604xI		0.010	0.130	
			LMC604xI, T_A = –40°C to +85°C			0.180	
		Positive rail V+ = 15V, R_L = 100kΩ to V+ / 2	LMC604xAI	14.920	14.970		
			LMC604xAI, T_A = –40°C to +85°C	14.880			
			LMC604xI	14.880	14.970		
			LMC604xI, T_A = –40°C to +85°C	14.820			
		Negative rail V+ = 15V, R_L = 100kΩ to V+ / 2	LMC604xAI		0.007	0.030	
			LMC604xAI, T_A = –40°C to +85°C			0.050	
			LMC604xI		0.007	0.060	
			LMC604xI, T_A = –40°C to +85°C			0.090	
		Positive rail V+ = 15V, R_L = 25kΩ to V+ / 2	LMC604xAI	14.900	14.950		
			LMC604xAI, T_A = –40°C to +85°C	14.850			
			LMC604xI	14.850	14.950		
			LMC604xI, T_A = –40°C to +85°C	14.800			
		Negative rail V+ = 15V, R_L = 25kΩ to V+ / 2	LMC604xAI		0.022	0.100	
			LMC604xAI, T_A = –40°C to +85°C			0.150	
			LMC604xI		0.022	0.150	
			LMC604xI, T_A = –40°C to +85°C			0.200	

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5.7 Electrical Characteristics (continued)

at $T_J = T_A = 25°C$, V+ = 5V, V– = 0V, $V_{CM} = 1.5V$, $V_{OUT} = V_S / 2$, and $R_L = 1M\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SC}	Short-circuit current	Sourcing V+ = 5V, V_{OUT} = 0V	LMC604xAI	16	22		mA
			LMC604xAI, T_A = –40°C to +85°C	10			
			LMC604xI	13	22		
			LMC604xI, T_A = –40°C to +85°C	8			
		Sinking V+ = 5V, V_{OUT} = 0V	LMC604xAI	16	21		
			LMC604xAI, T_A = –40°C to +85°C	8			
			LMC604xI	13	21		
			LMC604xI, T_A = –40°C to +85°C	8			
		Sourcing V+ = 15V, V_{OUT} = 0V	LMC604xAI	15	40		
			LMC604xAI, T_A = –40°C to +85°C	10			
			LMC604xI	15	40		
			LMC604xI, T_A = –40°C to +85°C	10			
		Sinking V+ = 15V, V_{OUT} = 0V	LMC604xAI	24	39		
			LMC604xAI, T_A = –40°C to +85°C	8			
			LMC604xI	21	39		
			LMC604xI, T_A = –40°C to +85°C	8			

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5.7 Electrical Characteristics (continued)

at $T_J = T_A = 25°C$, V+ = 5V, V– = 0V, $V_{CM} = 1.5V$, $V_{OUT} = V_S / 2$, and $R_L = 1M\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_Q	Quiescent current, total	V+ = 5V	LMC6041AI		14	20	μA
			LMC6041AI, T_A = –40°C to +85°C			24	
			LMC6041I		14	26	
			LMC6041I, T_A = –40°C to +85°C			30	
			LMC6042AI		20	34	
			LMC6042AI, T_A = –40°C to +85°C			39	
			LMC6042I		20	45	
			LMC6042I, T_A = –40°C to +85°C			50	
			LMC6044AI		40	65	
			LMC6044AI, T_A = –40°C to +85°C			72	
			LMC6044I		40	75	
			LMC6044I, T_A = –40°C to +85°C			82	
		V+ = 15V	LMC6041AI		18	26	
			LMC6041AI, T_A = –40°C to +85°C			31	
			LMC6041I		18	34	
			LMC6041I, T_A = –40°C to +85°C			39	
			LMC6042AI		26	44	
			LMC6042AI, T_A = –40°C to +85°C			51	
			LMC6042I		26	56	
			LMC6042I, T_A = –40°C to +85°C			65	
			LMC6044AI		52	85	
			LMC6044AI, T_A = –40°C to +85°C			94	
			LMC6044I		52	98	
			LMC6044I, T_A = –40°C to +85°C			107	

(1) Number specified is the slower of the positive and negative slew rates.

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5.8 Typical Characteristics

at V_S = ±7.5V and T_A = 25°C (unless otherwise specified)

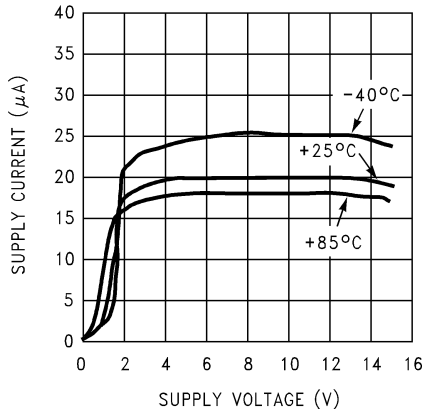

Figure 5-1. Supply Current vs Supply Voltage

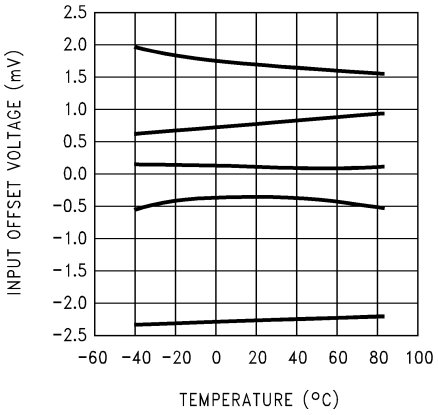

Figure 5-2. Offset Voltage vs Temperature of Five Representative Units

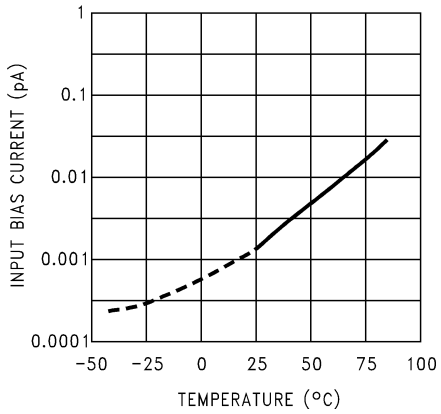

Figure 5-3. Input Bias Current vs Temperature

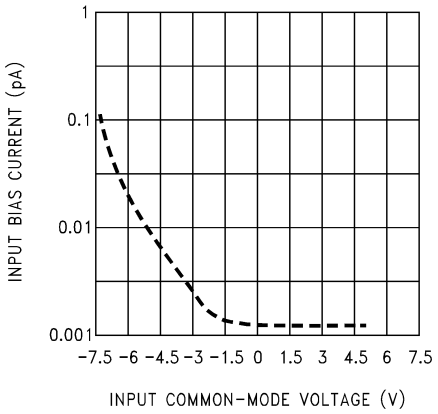

Figure 5-4. Input Bias Current vs Input Common-Mode Voltage

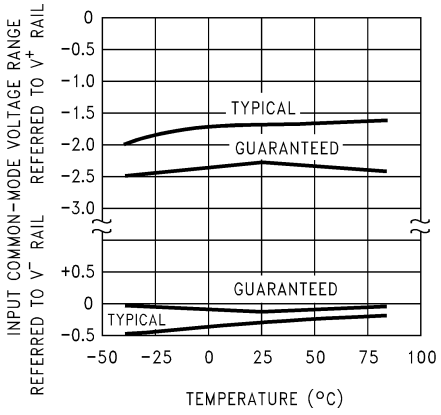

Figure 5-5. Input Bias Current Voltage Range vs Temperature

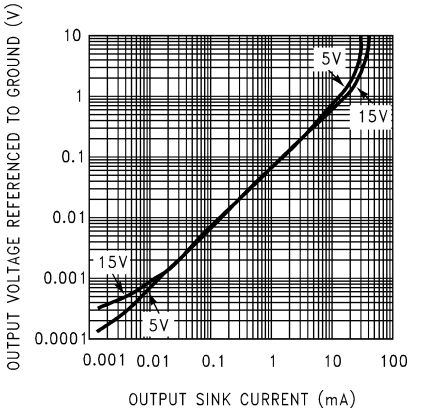

Figure 5-6. Output Characteristics Current Sinking

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5.8 Typical Characteristics (continued)

at V_S = ±7.5V and T_A = 25°C (unless otherwise specified)

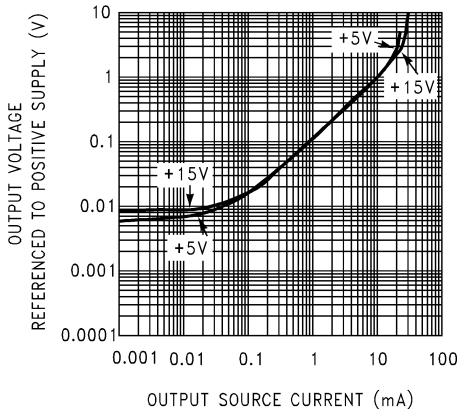

Figure 5-7. Output Characteristics Current Sourcing

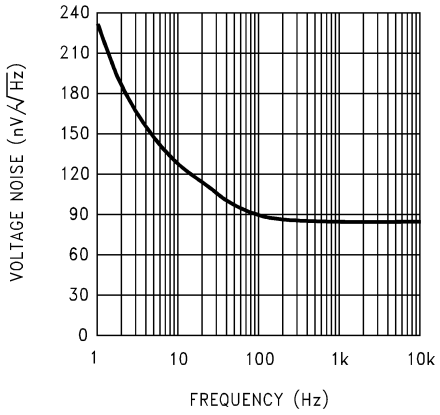

Figure 5-8. Input Voltage Noise vs Frequency

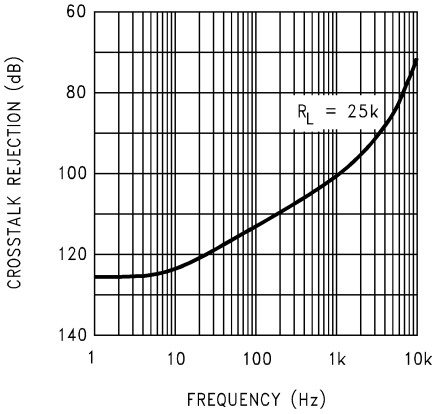

Figure 5-9. Crosstalk Rejection vs Frequency

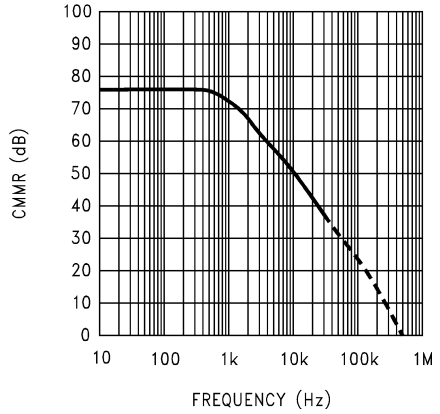

Figure 5-10. CMRR vs Frequency

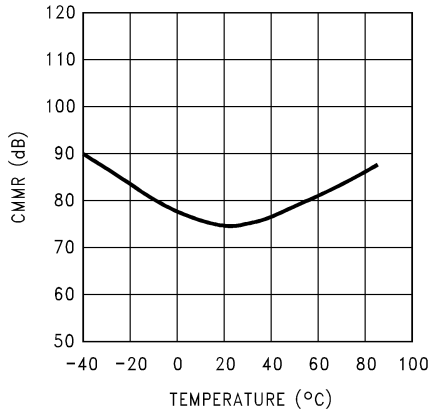

Figure 5-11. CMRR vs Temperature

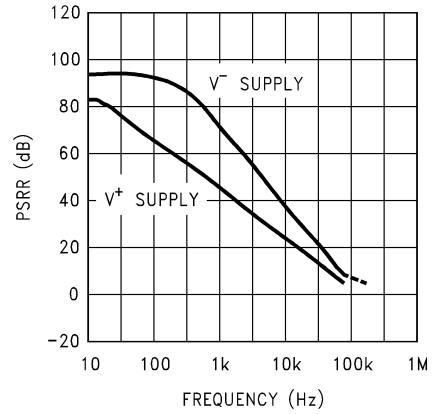

Figure 5-12. Power Supply Rejection Ratio vs Frequency

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5.8 Typical Characteristics (continued)

at V_S = ±7.5V and T_A = 25°C (unless otherwise specified)

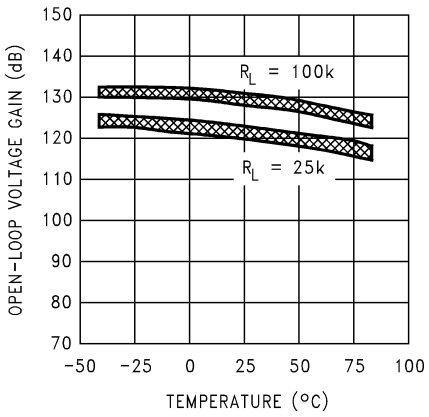

Figure 5-13. Open-Loop Voltage Gain vs Temperature

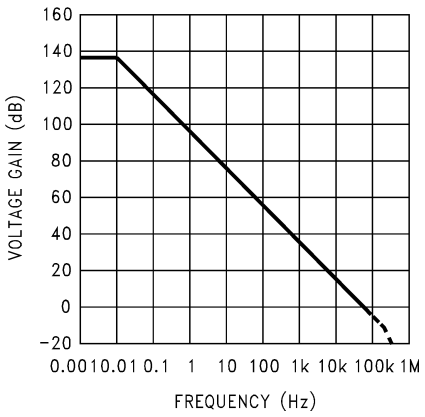

Figure 5-14. Open-Loop Frequency Response

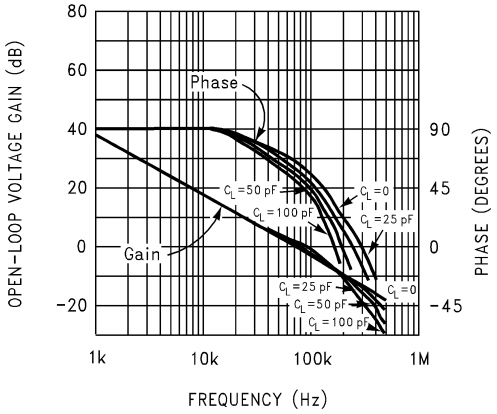

Figure 5-15. Gain and Phase Responses vs Load Capacitance

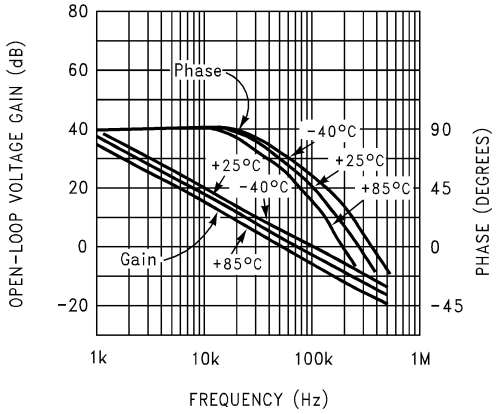

Figure 5-16. Gain and Phase Responses vs Temperature

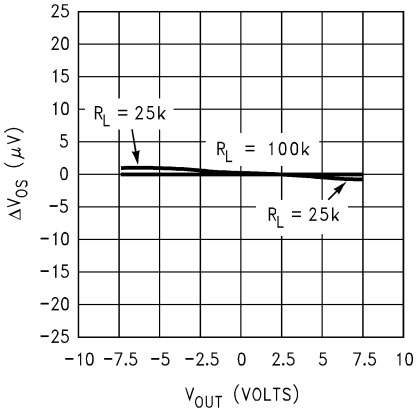

Figure 5-17. Gain Error (V_{OS} vs V_{OUT})

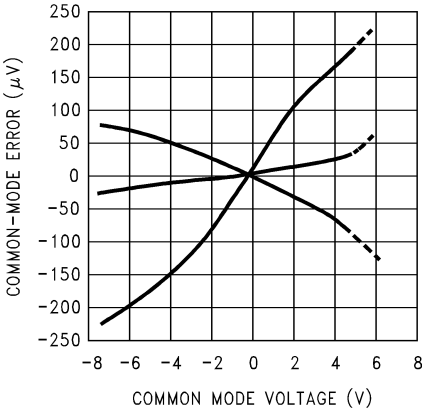

Figure 5-18. Common-Mode Error vs Common-Mode Voltage of Three Representative Units

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5.8 Typical Characteristics (continued)

at V_S = ±7.5V and T_A = 25°C (unless otherwise specified)

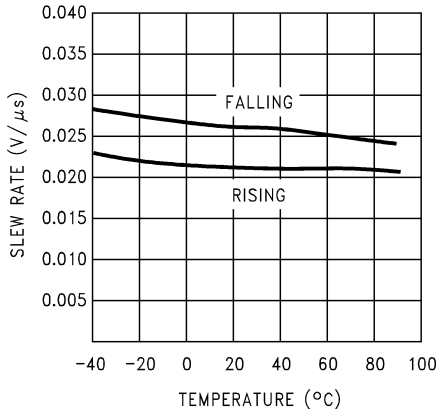

Figure 5-19. Noninverting Slew Rate vs Temperature

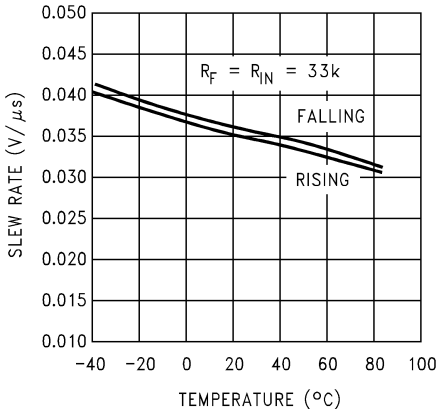

Figure 5-20. Inverting Slew Rate vs Temperature

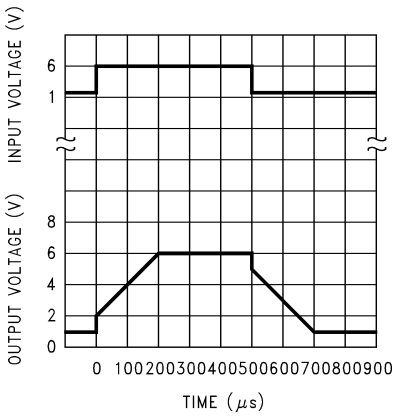

Figure 5-21. Noninverting Large Signal Pulse Response (A_V = +1)

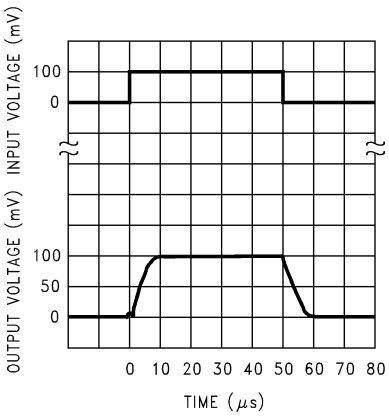

Figure 5-22. Noninverting Small-Signal Pulse Response

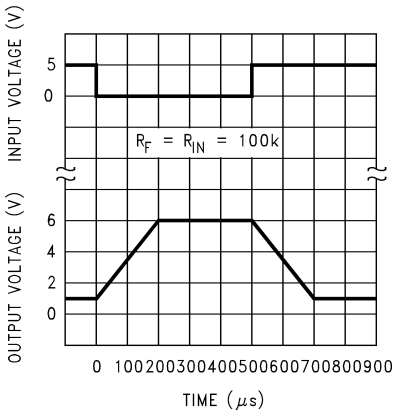

Figure 5-23. Inverting Large-Signal Pulse Response

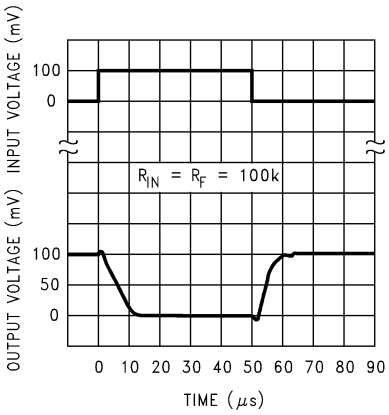

Figure 5-24. Inverting Small-Signal Pulse Response

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5.8 Typical Characteristics (continued)

at V_S = ±7.5V and T_A = 25°C (unless otherwise specified)

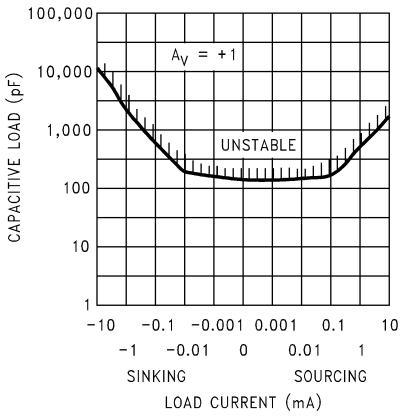

Figure 5-25. Stability vs Capacitive Load

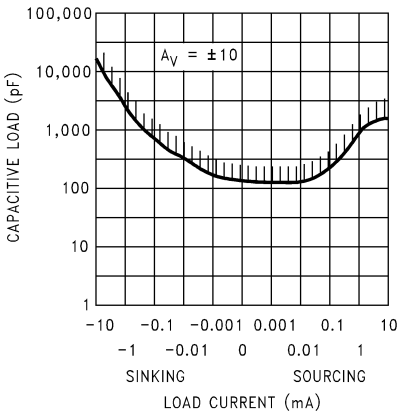

Figure 5-26. Stability vs Capacitive Load

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6 Application and Implementation

6.1 Application Information

6.1.1 Amplifier Topology

The LMC604x incorporate a novel op-amp design topology that enables a rail-to-rail output swing even when driving a large load. Special compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op amps. These features make the LMC604x both easier to design in, and provide higher speed than products typically found in this ultra-low power class.

6.1.2 Compensating For Input Capacitance

Large values of feedback resistance are quite common for amplifiers with ultra-low input current, such as the LMC604x.

Although the LMC604x are highly stable over a wide range of operating conditions, certain precautions must be taken to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When a high input impedance is demanded, guard the inputs of the LMC604x. Guarding input lines can not only reduce leakage, but lower stray input capacitance as well (see Section 6.3.1.1).

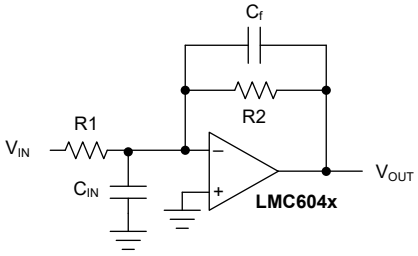

Figure 6-1. Canceling the Effect of Input Capacitance

Compensate for the effect of input capacitance by adding a capacitor. Place a capacitor, C_F, around the feedback resistor (as in Figure 6-1) so that:

$$\frac{1}{2\pi R1 C_{IN}} \geq \frac{1}{2\pi R2 C_F} \quad (1)$$

where

$$R1 C_{IN} \leq R2 C_F \quad (2)$$

The exact value of C_{IN} is often difficult to know, but C_F can be experimentally adjusted so that the desired pulse response is achieved. See the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

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6.1.3 Capacitive-Load Tolerance

Direct capacitive loading reduces the phase margin of many op amps. A pole in the feedback loop is created by the combination of the op-amp output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads. Figure 6-2 shows an example.

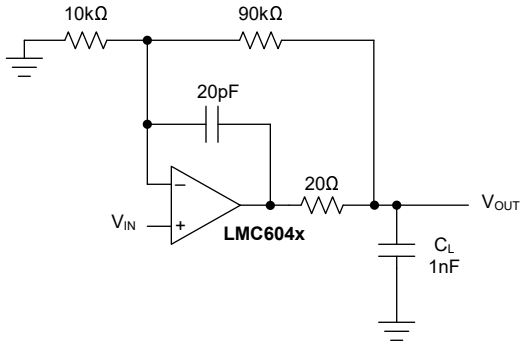

Figure 6-2. LMC604x Noninverting Gain-of-10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 6-2, R1 and C1 serve to counteract the loss of phase margin by feeding the high-frequency component of the output signal back into the inverting input of the amplifier, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pullup resistor to V^+ (Figure 6-3). Typically, a pullup resistor conducting 10µA or more significantly improves capacitive load responses. The value of the pullup resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. The open-loop gain of the amplifier can also be affected by the pullup resistor (see Section 5.7).

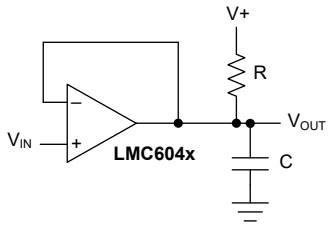

Figure 6-3. Compensating for Large Capacitive Loads With a Pullup Resistor

6.2 Typical Applications

6.2.1 Instrumentation Amplifiers

The extremely high input impedance and low power consumption of the LMC604x make these op amps an excellent choice for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are portable pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based pressure transducers.

The circuit in Figure 6-4 is recommended for applications where the common-mode input range is relatively low and the differential gain is in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 20µA. To maintain ultra-high input impedance, use ground rings and consider printed circuit board (PCB) layout an important part of the overall system design (see Printed Circuit Board Layout for High Impedance Work). Figure 6-4 shows that the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D.

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Rejection of the common-mode component of the input is accomplished by making the ratio of R1/R2 equal to R3/R4. So that:

$$\frac{R3}{R4} = \frac{R2}{R1} \tag{3}$$

The gain equation of the instrumentation amplifier is given by:

$$V_{OUT} = \frac{R4}{R3}\left(1 + \frac{R3}{R4} + \frac{R2 + R3}{R_0}\right) \tag{4}$$

A suggested design guideline is to minimize the difference of the value between R1 through R4. Minimizing often results in improved resistor temperature coefficient, amplifier gain, and CMRR over temperature. If RN = R1 = R2 = R3 = R4 then the gain equation is simplified as:

$$V_{OUT} = 2V_D\left(1 + \frac{R_N}{R_0}\right) \tag{5}$$

As a result of the *zero-in, zero-out* performance of the LMC604x, and output swing rail-to-rail, the dynamic range is only limited to the input common-mode range of 0V to V_S − 2.3V, the worst case at room temperature. This feature of the LMC604x makes these op amps an excellent choice for low-power instrumentation systems.

Figure 6-5 shows a complete instrumentation amplifier designed for a gain of 100. Provisions are made for the low-sensitivity trimming of CMRR and gain.

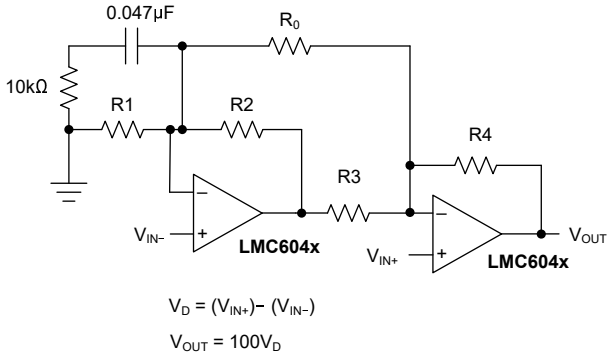

Figure 6-4. Two-Op-Amp Instrumentation Amplifier

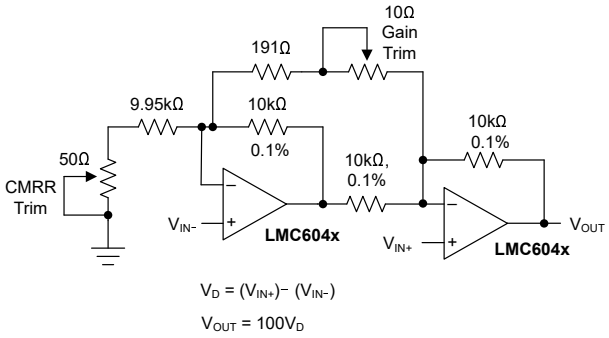

Figure 6-5. Low-Power, Two-Op-Amp Instrumentation Amplifier

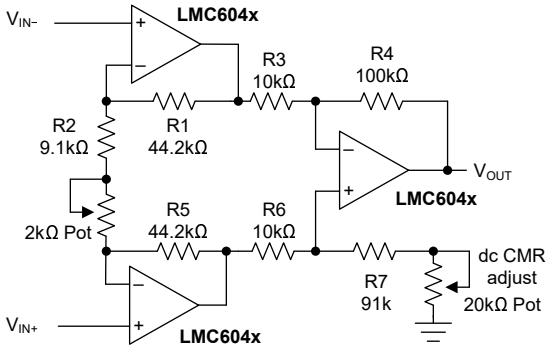

Figure 6-6. Instrumentation Amplifier

6.2.2 Low-Leakage Sample and Hold

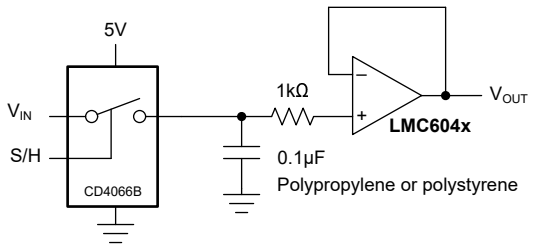

Figure 6-7. Low-Leakage Sample and Hold

6.2.3 Square-Wave Generator

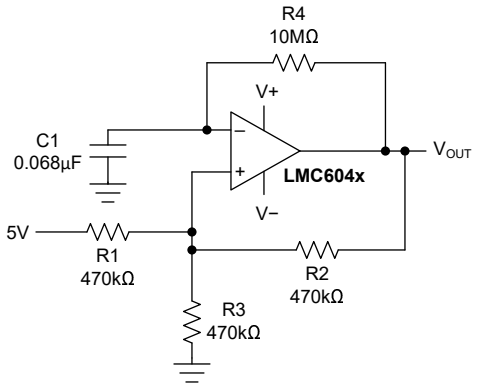

Figure 6-8. 1Hz Square-Wave Oscillator

6.2.4 AC Coupled Power Amplifier

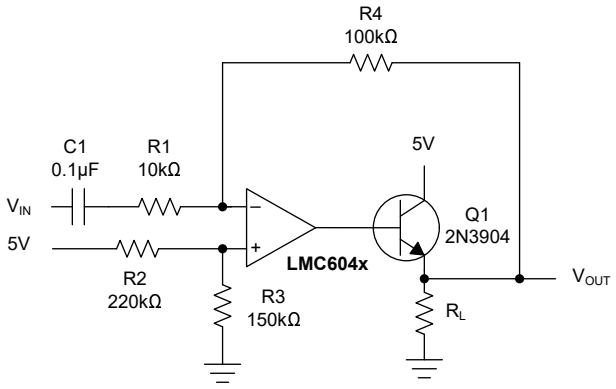

Figure 6-9. AC Coupled Power Amplifier

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6.3 Layout

6.3.1 Layout Guidelines

6.3.1.1 Printed-Circuit-Board Layout for High-Impedance Work

As a general rule, any circuit that must operate with less than 1000pA of leakage current requires special layout of the printed circuit board (PCB). To take advantage of the ultra-low input current of the LMC604x, typically 150fA, an excellent layout is essential. Fortunately, the techniques used to obtain low leakages are quite simple. First, do not ignore the surface leakage of the PCB, even though the leakage current can sometimes appear acceptably low, because under conditions of high humidity, dust, or contamination, the surface leakage can be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC604x inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and anything else connected to the inputs of the op amp (see also Figure 6-14). To have a significant effect, place guard rings on both the top and bottom of the PCB. Then, connect the foil to a voltage that is at the same voltage as the amplifier inputs, because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of 10^{12}, which is normally considered a very large resistance, can leak 5pA if the trace is a 5V bus adjacent to the pad of the input. This leakage can cause a 250 times degradation from the actual performance of the LMC604x. However, if a guard ring is held within 5mV of the inputs, then even a resistance of $10^{11}\Omega$ causes only 0.05pA of leakage current. See Figure 6-10 to Figure 6-12 for typical connections of guard rings for standard op-amp configurations

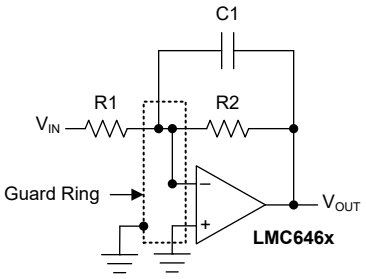

Figure 6-10. Typical Connections of Guard Rings: Inverting Amplifier

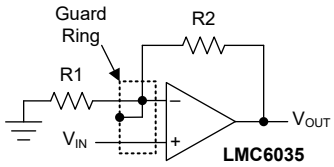

Figure 6-11. Typical Connections of Guard Rings: Noninverting Amplifier

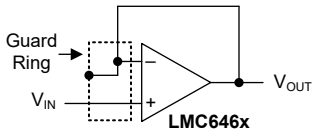

Figure 6-12. Typical Connections of Guard Rings: Follower

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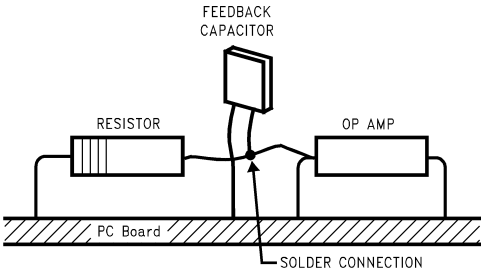
If laying out a PCB for the sake of just a few circuits is not practical, the following technique is even better than a guard ring. Do not insert the input pin of the amplifier into the PCB at all. Instead, bend the pin up in the air, and use only air as an insulator because air is an excellent insulator. In this case, you forgo some of the advantages of PCB construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. Figure 6-13 shows an example of air wiring.



Note: The input pins are lifted out of the PCB and soldered directly to components. All other pins connected to the PCB.

Figure 6-13. Air Wiring

6.3.2 Layout Examples

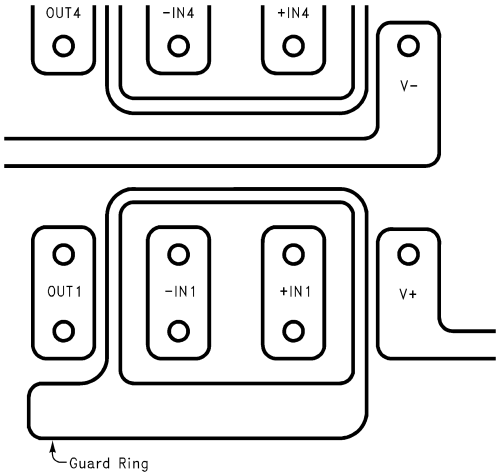


Figure 6-14. Example of Guard Ring in PCB Layout

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7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

Trademarks

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All trademarks are the property of their respective owners.

7.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2013) to Revision F (March 2025)	Page
• Added LMC6041 and LMC6044 to this data sheet; previously in SNOS610E and SNOS612D, respectively	1
• Added *Pin Configuration and Functions*	3
• Added ESD Ratings	5
• Added *Thermal Information*	6
• Updated parameter names and symbols	7
• Deleted footnotes 1 and 2 from DC *Electrical Characteristics*	7
• Changed input current noise from 0.2fA/$\sqrt{Hz}$ to 12.5fA/$\sqrt{Hz}$	7
• Changed total harmonic distortion from 0.01% to 1%	7
• Moved footnote 3 from DC *Electrical Characteristics* to open-loop voltage gain test conditions	7
• Changed open-loop gain MIN for R_L = 100kΩ (sourcing) from 400V/mV to 300V/mV for LMC604xAI	7
• Changed open-loop gain MIN for R_L = 100kΩ (sourcing, T_A = –40°C to +85°C) from 300V/mV to 200V/mV for LMC604xAI	7
• Deleted footnotes 1 and 2 from AC *Electrical Characteristics*	7
• Moved footnote 3 test conditions from AC *Electrical Characteristics* to slew rate test conditions	7
• Delete phase margin	7
• Moved footnote 4 from AC *Electrical Characteristics* to crosstalk test conditions	7
• Updated *Amplifier Topology*	17

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Changes from Revision D (March 2013) to Revision E (March 2013)	Page
• Changed layout of National Data Sheet to TI format	20

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9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC6041AIM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LMC60 41AIM
LMC6041AIMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41AIM
LMC6041AIMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41AIM
LMC6041AIMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41AIM
LMC6041IM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LMC60 41IM
LMC6041IMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41IM
LMC6041IMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41IM
LMC6041IMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41IM
LMC6041IN/NOPB	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	-40 to 85	LMC60 41IN
LMC6042AIJ	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	Call TI	Level-1-NA-UNLIM	-	LMC6042AIJ
LMC6042AIJ.A	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	Call TI	Level-1-NA-UNLIM	See LMC6042AIJ	LMC6042AIJ
LMC6042AIM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LMC60 42AIM
LMC6042AIMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 42AIM
LMC6042AIMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 42AIM
LMC6042AIMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 42AIM
LMC6042AIN/NOPB	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	-40 to 85	LMC60 42AIN
LMC6042IM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LMC60 42IM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC6042IMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 42IM
LMC6042IMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 42IM
LMC6042IMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 42IM
LMC6044AIM/NOPB	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	LMC6044 AIM
LMC6044AIMX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6044 AIM
LMC6044AIMX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6044 AIM
LMC6044AIMX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6044 AIM
LMC6044IMX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6044IM
LMC6044IMX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6044IM
LMC6044IMX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6044IM
LMC6044IN/NOPB	Obsolete	Production	PDIP (N) | 14	-	-	Call TI	Call TI	-40 to 85	LMC6044IN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

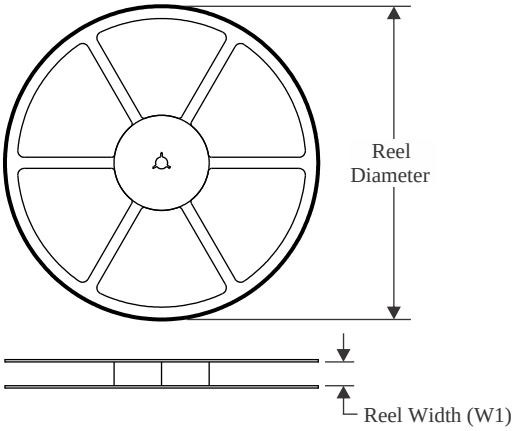
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

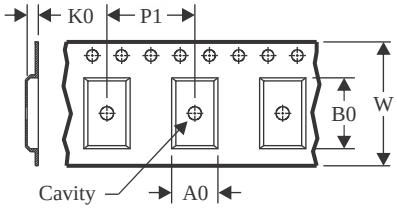
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

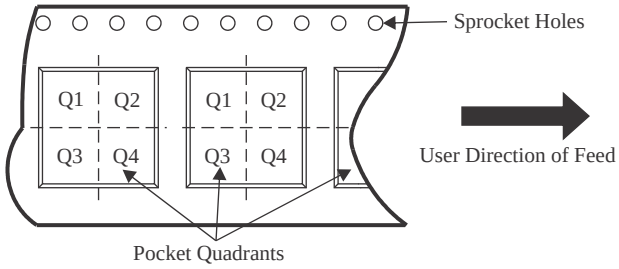


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

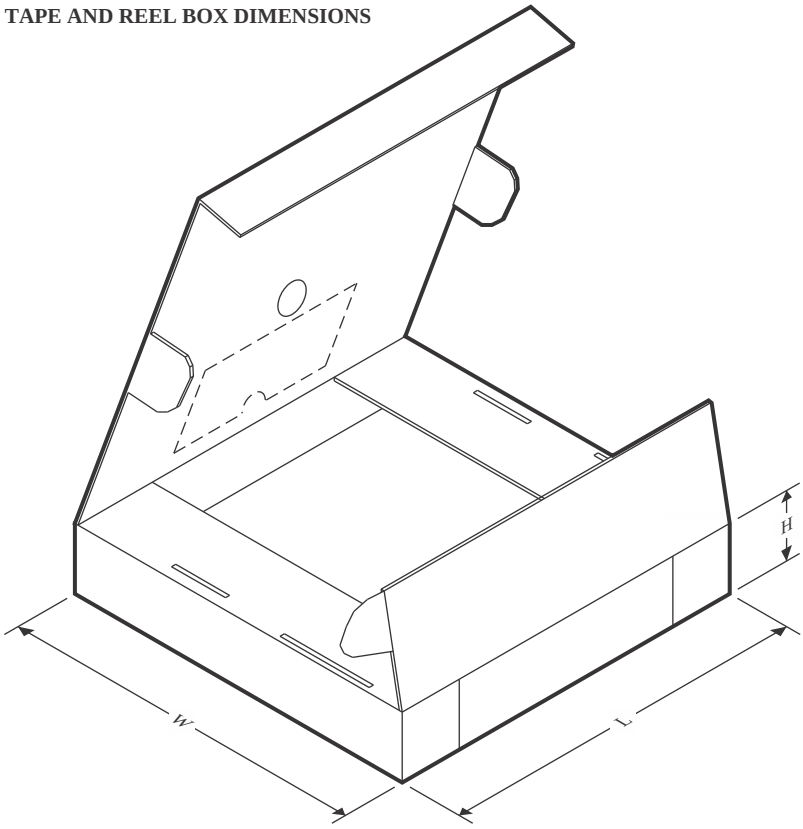
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6041AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6041IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6042AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6042IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6044AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6044IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

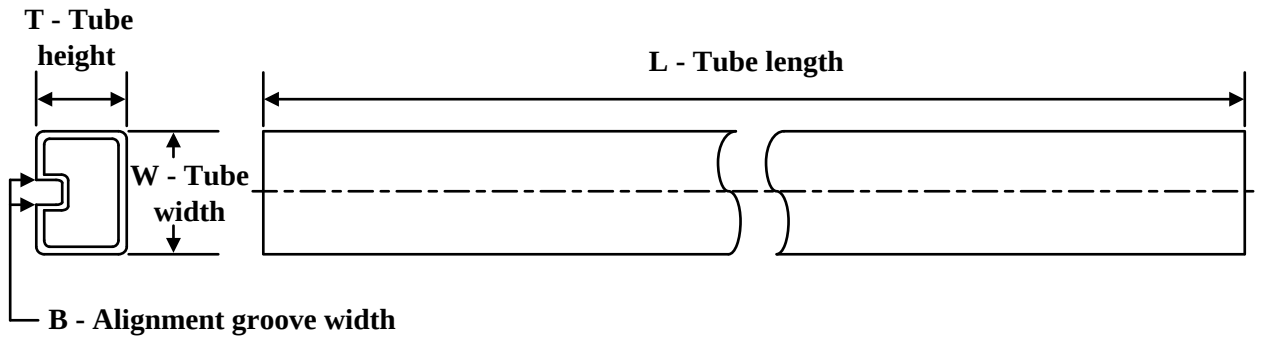
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6041AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6041IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6042AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6042IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6044AIMX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LMC6044IMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

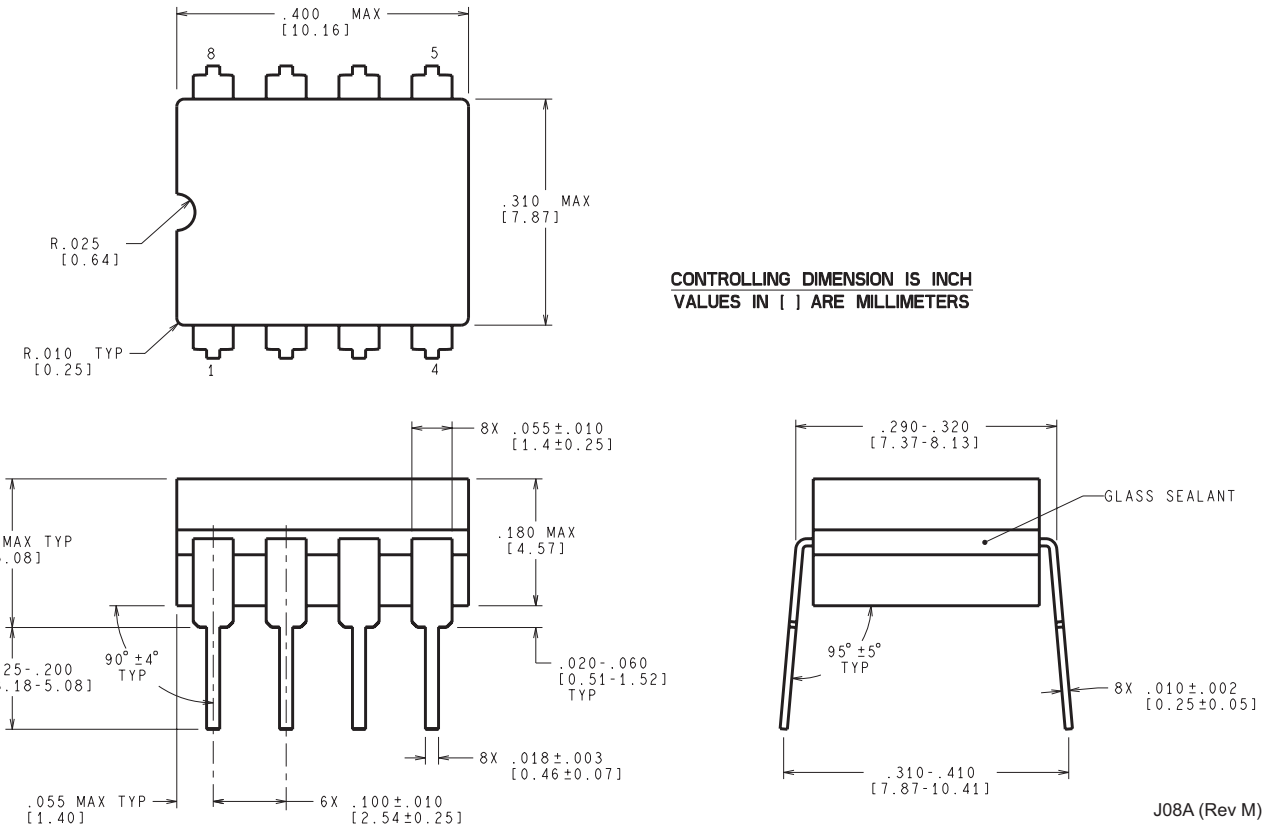
TUBE



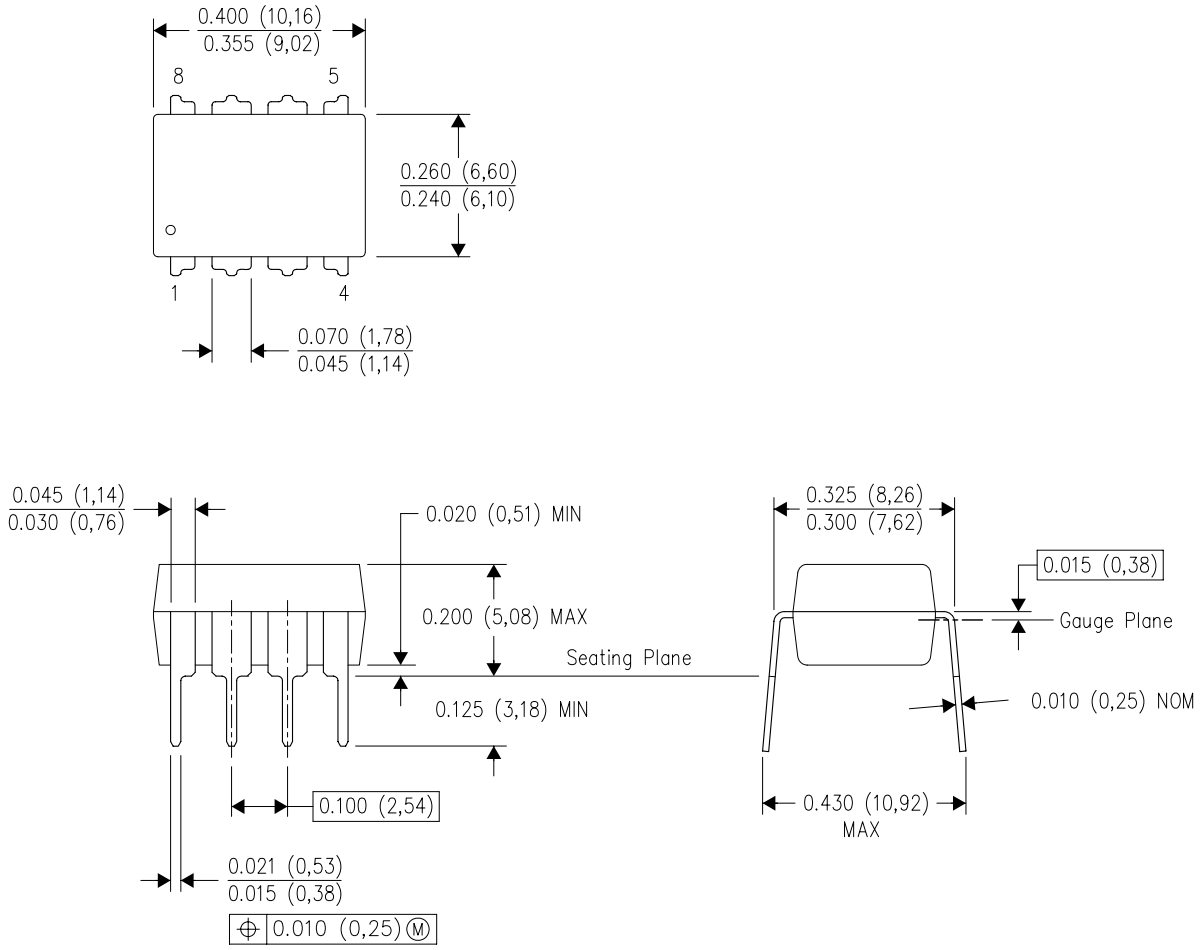
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMC6042AIJ	NAB	CDIP	8	40	502	14	11938	4.32
LMC6042AIJ.A	NAB	CDIP	8	40	502	14	11938	4.32

NAB0008A


.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

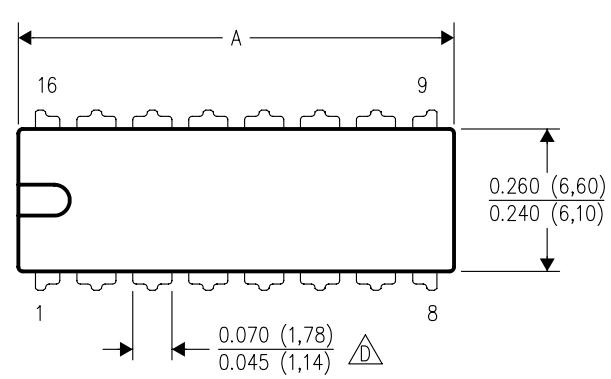


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

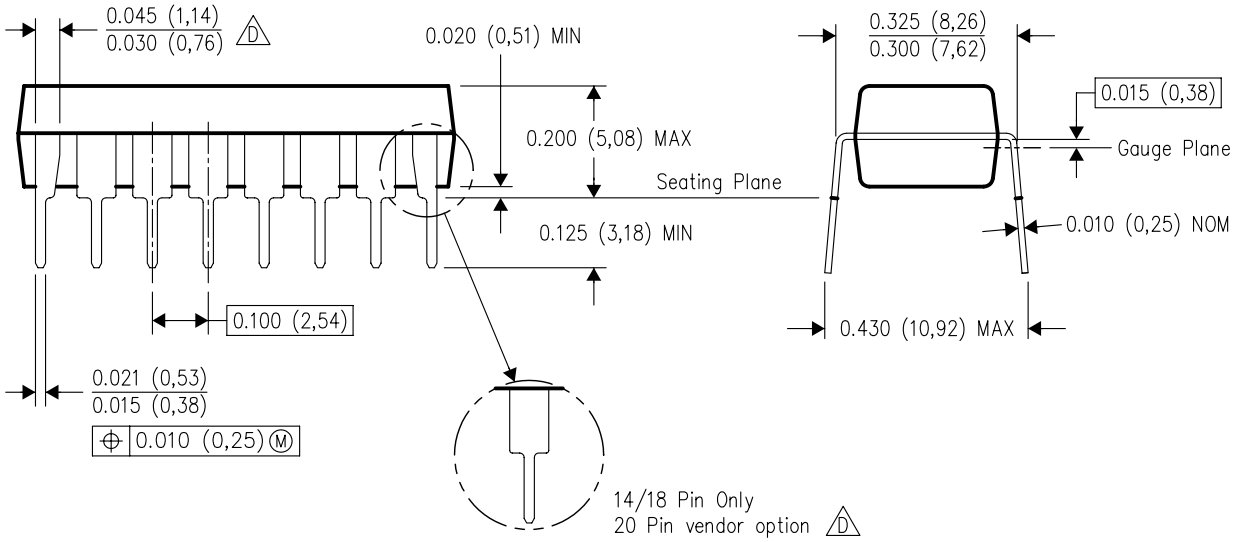
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

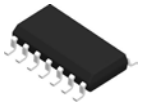


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

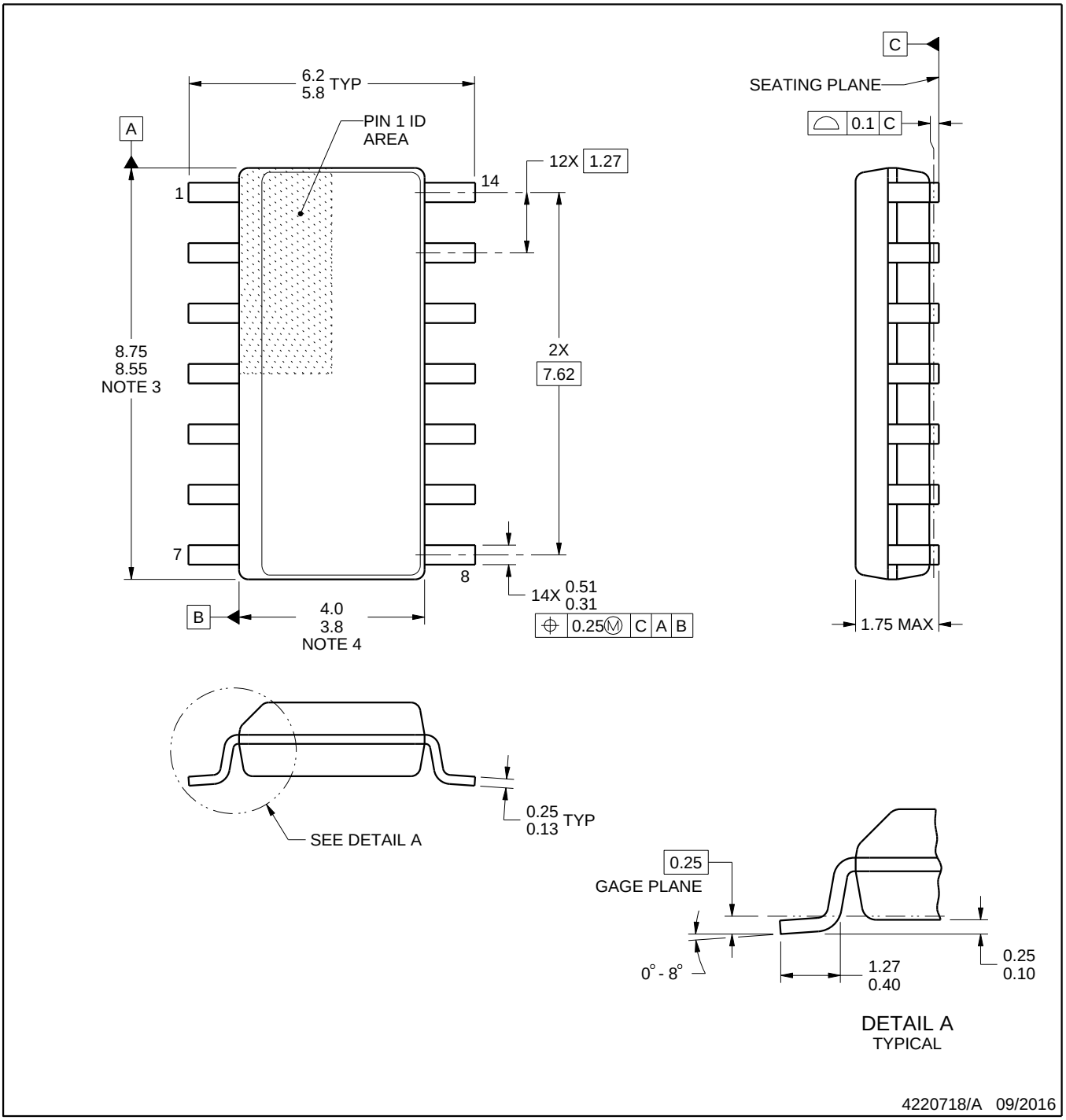


PACKAGE OUTLINE

D0014A

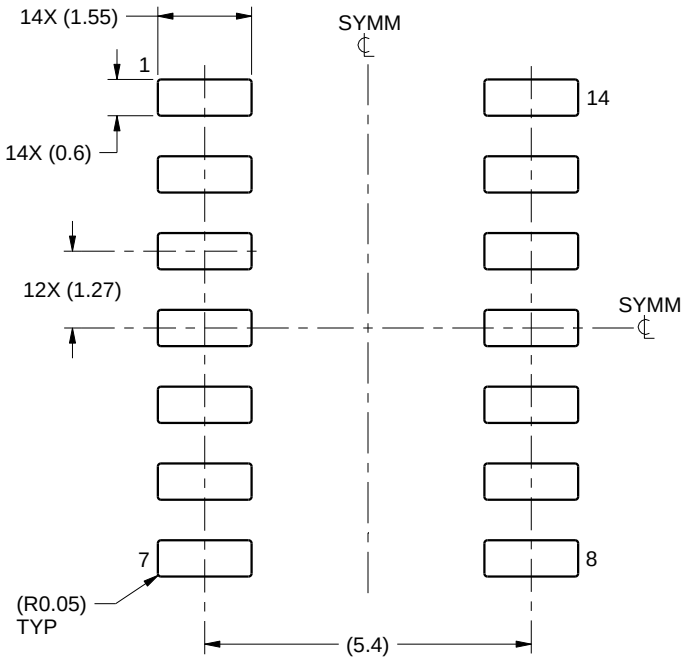
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

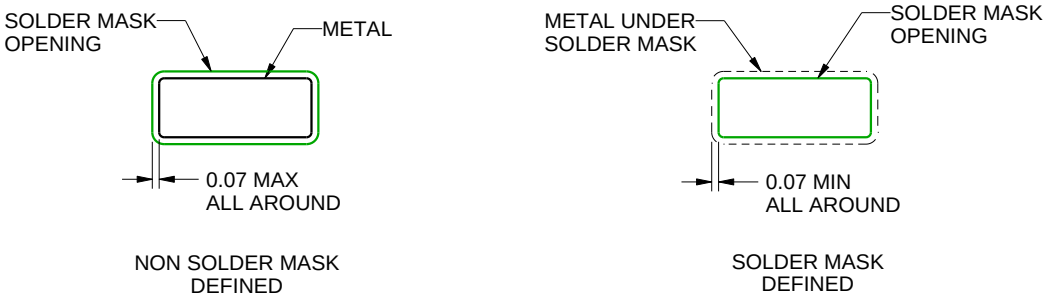


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

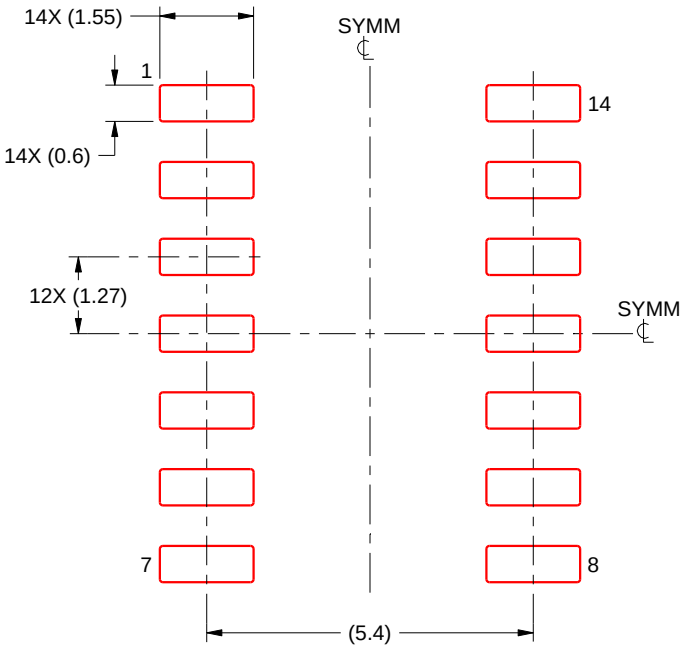
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

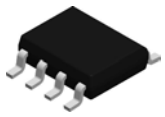


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

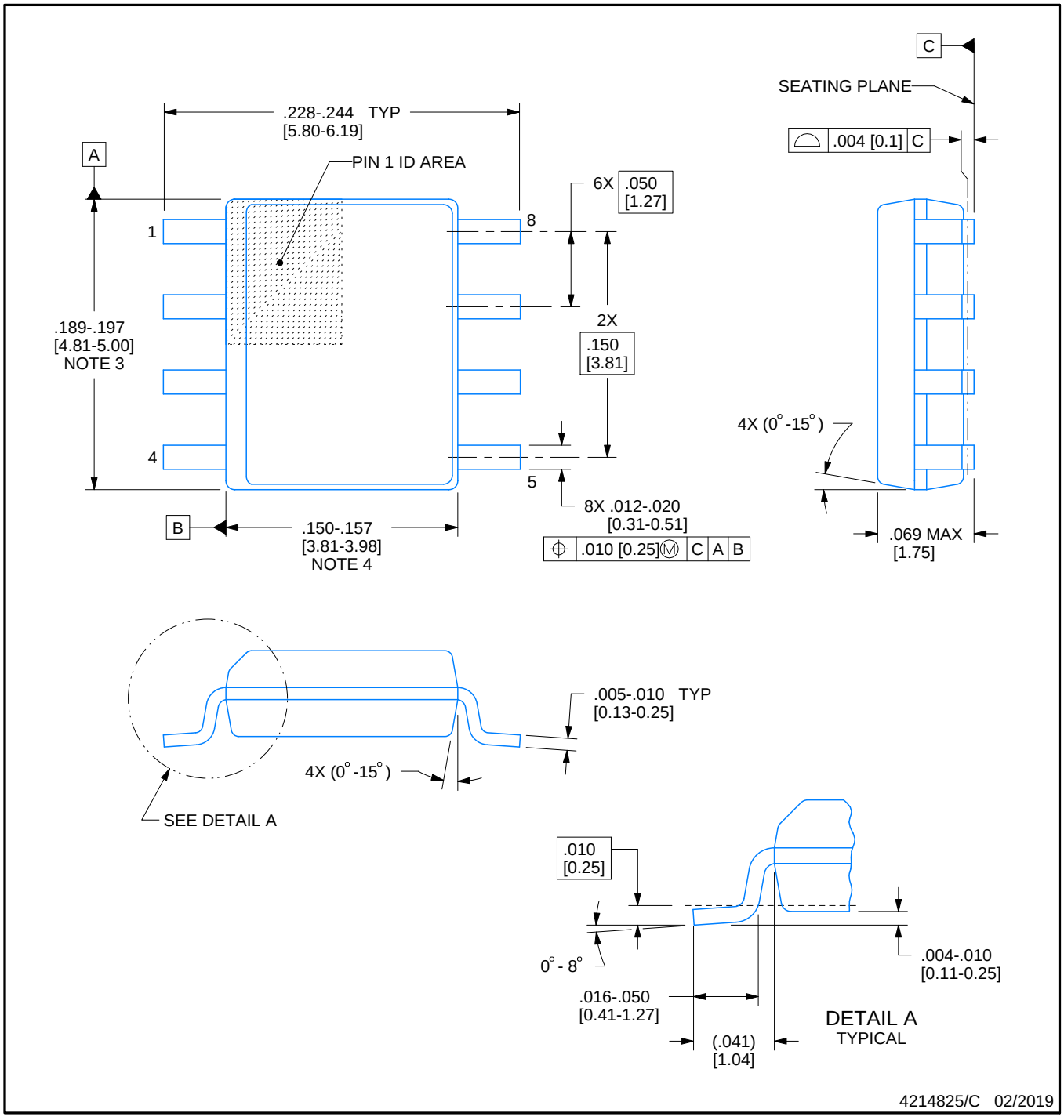


PACKAGE OUTLINE

D0008A

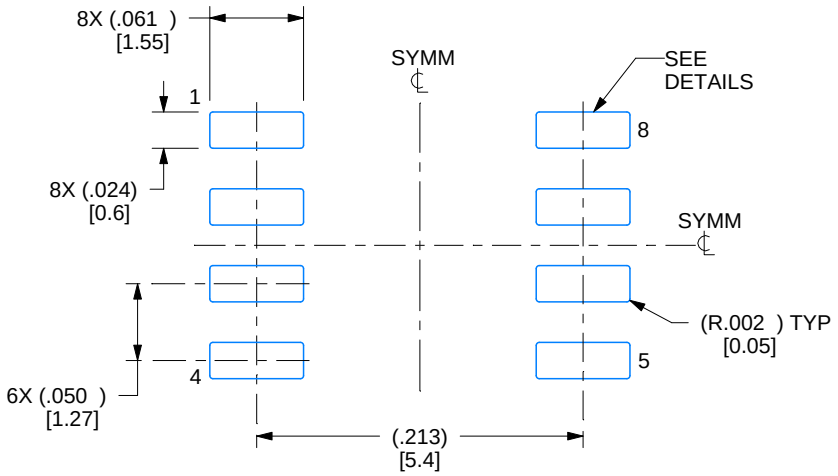
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

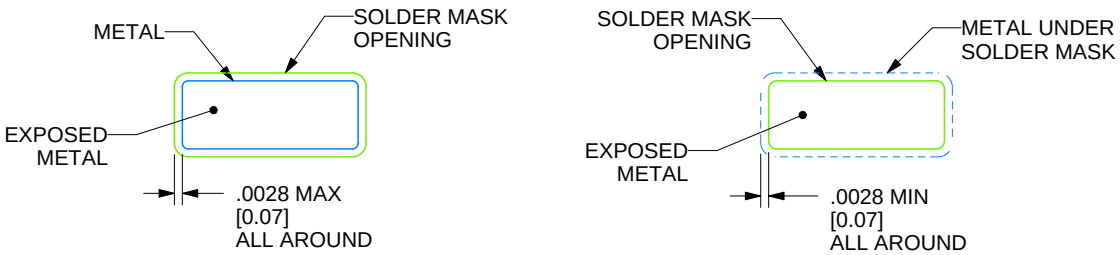


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

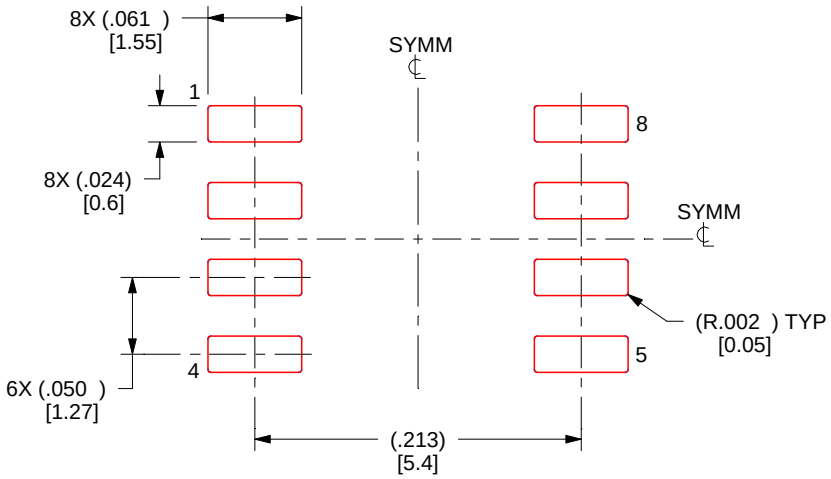
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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