

## Charge Pump DC-to-DC Voltage Converter

### Features

- Wide Operating Voltage Range: 1.5V to 15V
- Boost Pin for Higher Switching Frequency (Pin 1)
- High-Power Efficiency is 96%
- Easy to Use – Requires Only 2 External Non-Critical Passive Components
- Improved Direct Replacement for Industry Standard ICL7660 and Other Second Source Devices

### Applications

- Simple Conversion of +5V to  $\pm 5V$  Supplies
- Voltage Multiplication  $V_{OUT} = \pm nV_{IN}$
- Negative Supplies for Data Acquisition Systems and Instrumentation
- RS232 Power Supplies
- Supply Splitter,  $V_{OUT} = \pm V_S/2$

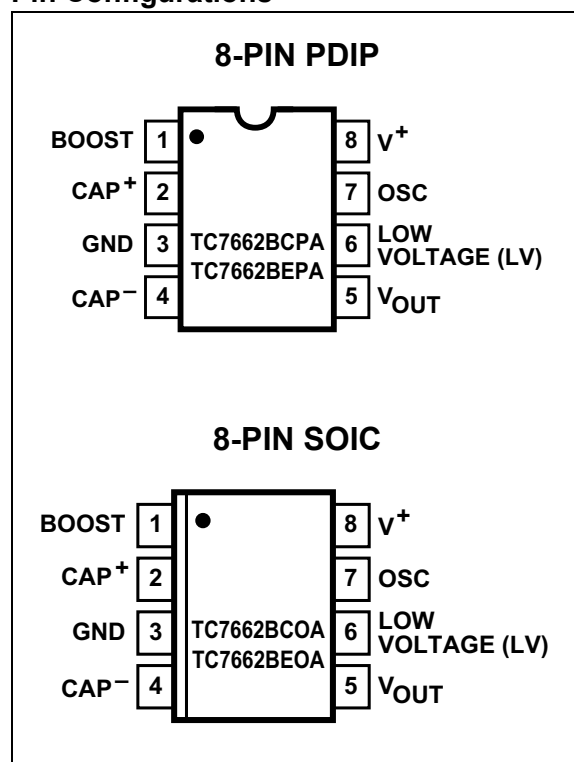
### General Description

The TC7662B is a pin-compatible upgrade to the Industry standard TC7660 charge pump voltage converter. It converts a +1.5V to +15V input to a corresponding -1.5 to -15V output using only two low-cost capacitors, eliminating inductors and their associated cost, size and EMI.

The on-board oscillator operates at a nominal frequency of 10 kHz. Frequency is increased to 35 kHz when pin 1 is connected to  $V^+$ , allowing the use of smaller external capacitors. Operation below 10 kHz (for lower supply current applications) is also possible by connecting an external capacitor from OSC to ground (with pin 1 open).

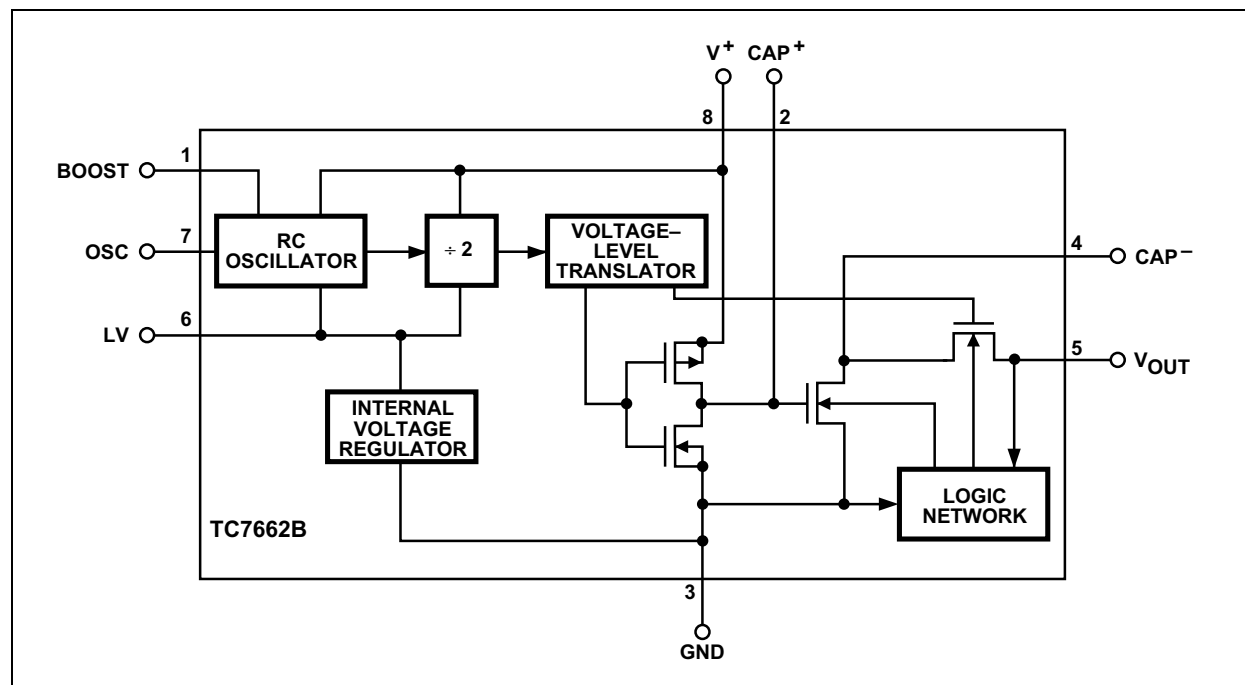
The TC7662B is available in both 8-pin PDIP and 8-pin small outline (SO) packages in commercial and extended temperature ranges.

### Pin Configurations



# TC7662B

## FUNCTIONAL BLOCK DIAGRAM



## 1.0 ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS†

|                                                         |                                      |
|---------------------------------------------------------|--------------------------------------|
| Supply Voltage .....                                    | +16.5V                               |
| LV, Boost and OSC Inputs Voltage (Note 1)               |                                      |
| $V^+ < 5.5V$ .....                                      | –0.3V to ( $V^+ + 0.3V$ )            |
| $> 5.5V$ .....                                          | ( $V^+ - 5.5V$ ) to ( $V^+ + 0.3V$ ) |
| Current Into LV (Note 1), $V^+ > 3.5V$ .....            | 20 $\mu A$                           |
| Output Short Duration, ( $V_{SUPPLY} \leq 5.5V$ ) ..... | Continuous                           |
| Power Dissipation ( $T_A \leq 70^\circ C$ ) (Note 2)    |                                      |
| PDIP .....                                              | 730 mW                               |
| SOIC .....                                              | 470 mW                               |
| Operating Temperature Range                             |                                      |
| C Suffix .....                                          | 0°C to +70°C                         |
| E Suffix .....                                          | –40°C to +85°C                       |
| Storage Temperature Range .....                         | –65°C to +150°C                      |
| Lead Temperature (soldering, 10 sec) .....              | +300°C                               |

† **Notice:** Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

$V_+ = 5V$ ,  $T_A = +25^\circ C$ , OSC = Free running, Test Circuit shown in Figure 4-1, unless otherwise specified.

| Parameter                                          | Sym     | Min | Typ | Max | Units   | Test Conditions                                                              |
|----------------------------------------------------|---------|-----|-----|-----|---------|------------------------------------------------------------------------------|
| Supply Current (Note 3)<br>(Boost pin OPEN OR GND) | I+      | —   | 80  | 80  | $\mu A$ | $R_L = \infty$ , +25°C                                                       |
|                                                    |         | —   | —   | 180 | $\mu A$ | 0°C $\leq T_A \leq$ +70°C                                                    |
|                                                    |         | —   | —   | 180 | $\mu A$ | –40°C $\leq T_A \leq$ +85°C                                                  |
|                                                    |         | —   | —   | 200 | $\mu A$ | –55°C $\leq T_A \leq$ +125°C                                                 |
| Supply Current<br>(Boost pin = V+)                 | I+      | —   | —   | 300 | $\mu A$ | 0°C $\leq T_A \leq$ +70°C                                                    |
|                                                    |         | —   | —   | 350 | $\mu A$ | –40°C $\leq T_A \leq$ +85°C                                                  |
|                                                    |         | —   | —   | 400 | $\mu A$ | –55°C $\leq T_A \leq$ +125°C                                                 |
| Supply Voltage Range, High<br>(Note 4)             | $V_H^+$ | 3.0 | —   | 15  | V       | $R_L = 10\text{ k}\Omega$ , LV Open,<br>$T_{MIN} \leq T_A \leq T_{MAX}$      |
| Supply Voltage Range, Low                          | $V_L^+$ | 1.5 | —   | 3.5 | V       | $R_L = 10\text{ k}\Omega$ ,<br>LV to GND,<br>$T_{MIN} \leq T_A \leq T_{MAX}$ |

- Note**
- 1: Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to “power up” of the TC7662B.
  - 2: Derate linearly above 50°C by 5.5 mW/°C.
  - 3: In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, in the order of 5 pF.
  - 4: The TC7662B can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.
  - 5: The pump switching frequency is 1/2 of the oscillator frequency.

# TC7662B

$V_+ = 5V$ ,  $T_A = +25^\circ C$ , OSC = Free running, Test Circuit shown in [Figure 4-1](#), unless otherwise specified.

| Parameter                                      | Sym          | Min | Typ  | Max | Units      | Test Conditions                                                                                   |
|------------------------------------------------|--------------|-----|------|-----|------------|---------------------------------------------------------------------------------------------------|
| Output Source Resistance                       | $R_{OUT}$    | —   | 65   | 100 | $\Omega$   | $I_{OUT} = 20 \text{ mA}$ ,<br>$0^\circ C \leq T_A \leq +70^\circ C$                              |
|                                                |              | —   | —    | 120 | $\Omega$   | $I_{OUT} = 20 \text{ mA}$ ,<br>$-40^\circ C \leq T_A \leq +85^\circ C$                            |
|                                                |              | —   | —    | 150 | $\Omega$   | $I_{OUT} = 20 \text{ mA}$ ,<br>$-55^\circ C \leq T_A \leq +125^\circ C$                           |
|                                                |              | —   | —    | 250 | $\Omega$   | $I_{OUT} = 3 \text{ mA}$ ,<br>$V^+ = 2V$ , LV to GND,<br>$0^\circ C \leq T_A \leq +70^\circ C$    |
|                                                |              | —   | —    | 300 | $\Omega$   | $I_{OUT} = 3 \text{ mA}$ ,<br>$V^+ = 2V$ , LV to GND,<br>$-40^\circ C \leq T_A \leq +85^\circ C$  |
|                                                |              | —   | —    | 400 | $\Omega$   | $I_{OUT} = 3 \text{ mA}$ ,<br>$V^+ = 2V$ , LV to GND,<br>$-55^\circ C \leq T_A \leq +125^\circ C$ |
| Oscillator Frequency                           | $f_{OSC}$    | 5   | 10   | —   | kHz        | $C_{OSC} = 0$ ,<br>Pin 1 Open or GND                                                              |
|                                                |              | —   | 35   | —   | kHz        | Pin 1 = $V^+$                                                                                     |
| Switching Frequency ( <a href="#">Note 5</a> ) | $f_{SW}$     | 2.5 | 5    | —   | kHz        | $C_{OSC} = 0$ ,<br>Pin 1 Open or GND                                                              |
|                                                |              | —   | 17.5 | —   | kHz        | Pin 1 = $V^+$                                                                                     |
| Power Efficiency                               | $P_{Eff}$    | 96  | 96   | —   | %          | $R_L = 5 \text{ k}\Omega$                                                                         |
|                                                |              | 95  | 97   | —   | %          | $T_{MIN} \leq T_A \leq T_{MAX}$                                                                   |
| Voltage Conversion Efficiency                  | $V_{OUT}Eff$ | 99  | 99.9 | —   | %          | $R_L = \infty$                                                                                    |
| Oscillator Impedance                           | $Z_{OSC}$    | —   | 1    | —   | M $\Omega$ | $V^+ = 2V$                                                                                        |
|                                                |              | —   | 100  | —   | k $\Omega$ | $V^+ = 2V$                                                                                        |

- Note**
- 1: Connecting any terminal to voltages greater than  $V^+$  or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TC7662B.
  - 2: Derate linearly above  $50^\circ C$  by  $5.5 \text{ mW}/^\circ C$ .
  - 3: In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, in the order of  $5 \text{ pF}$ .
  - 4: The TC7662B can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.
  - 5: The pump switching frequency is  $1/2$  of the oscillator frequency.

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and, therefore, outside the warranted range.

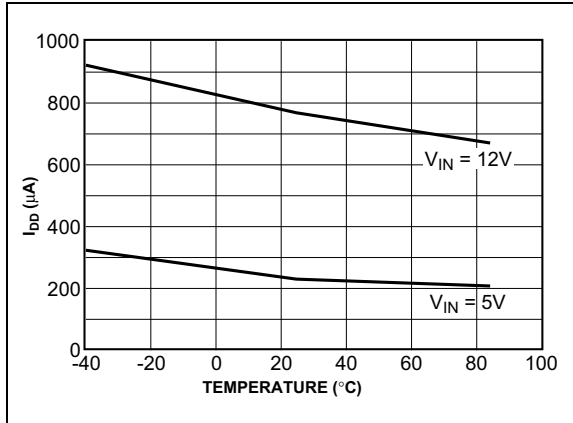


**FIGURE 2-1:** Supply Current vs. Temperature (with Boost Pin =  $V_{IN}$ ).

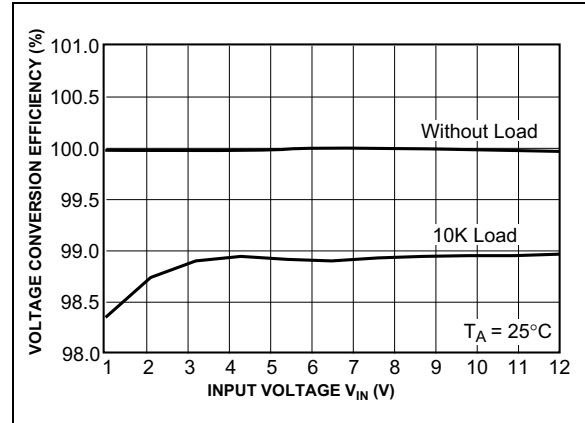


**FIGURE 2-4:** Voltage Conversion.

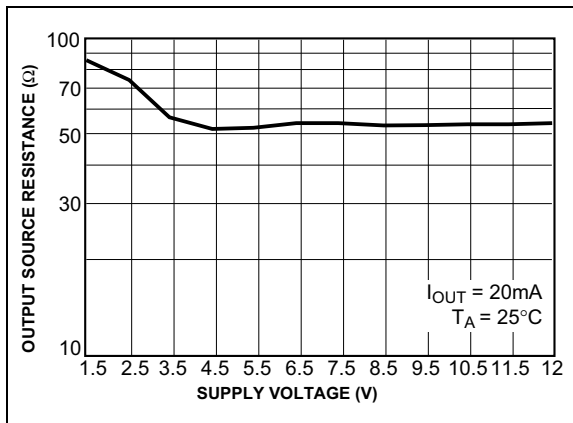


**FIGURE 2-2:** Output Source Resistance vs. Supply Voltage.

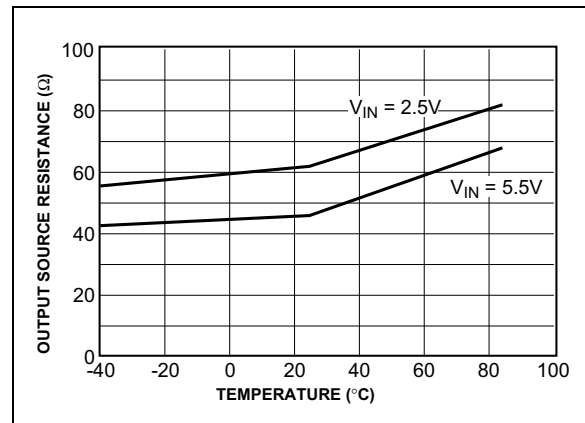


**FIGURE 2-5:** Output Source Resistance vs. Temperature.

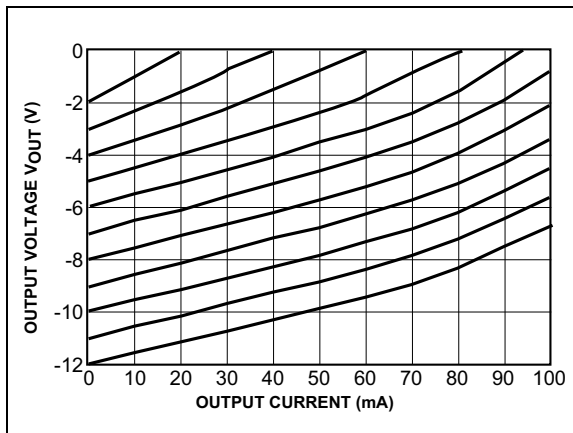


**FIGURE 2-3:** Output Voltage vs. Output Current.

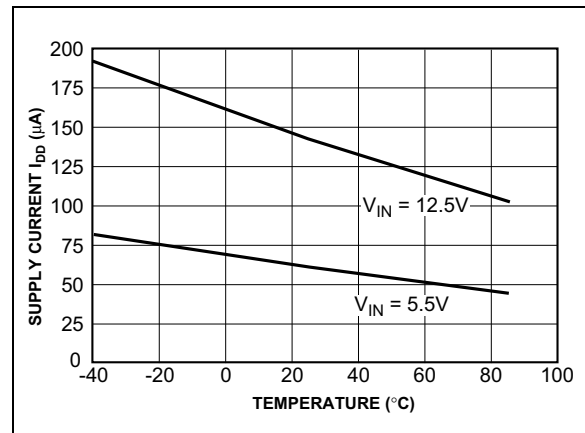


**FIGURE 2-6:** Supply Current vs. Temperature.

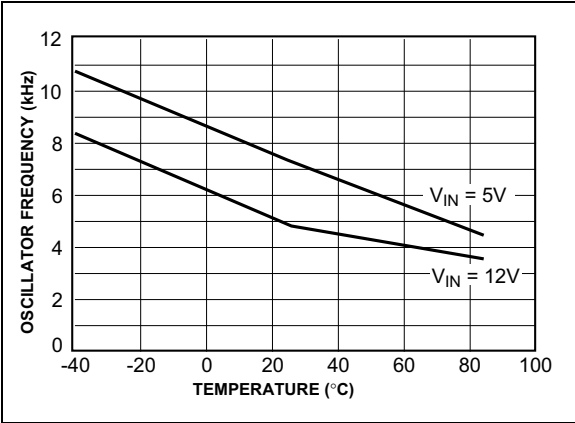


**FIGURE 2-7:** Unloaded Oscillator Frequency vs. Temperature.

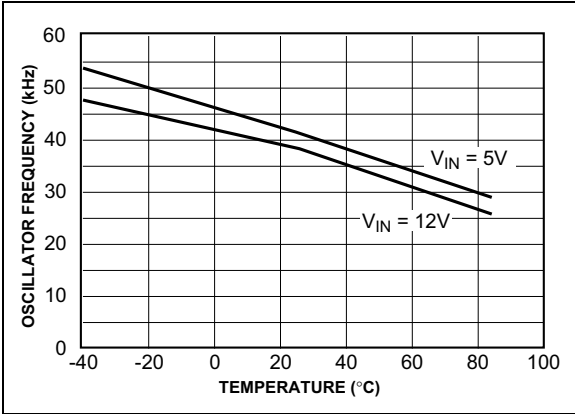


**FIGURE 2-8:** Unloaded Oscillator Frequency vs. Temperature with Boost Pin =  $V_{IN}$

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

| 8-Pin<br>PDIP/SOIC | Name                | Function                                                                            |
|--------------------|---------------------|-------------------------------------------------------------------------------------|
| 1                  | BOOST               | Boost pin; for the higher switching frequency, connect Pin 1 to the $V^+$ pin.      |
| 2                  | CAP <sup>+</sup>    | Charge pump capacitor positive terminal                                             |
| 3                  | GND                 | Ground terminal                                                                     |
| 4                  | CAP <sup>-</sup>    | Charge pump capacitor negative terminal                                             |
| 5                  | V <sub>OUT</sub>    | Output voltage                                                                      |
| 6                  | LOW<br>VOLTAGE (LV) | Low voltage pin. Connect to GND for $V^+ < 3.5V$ .                                  |
| 7                  | OSC                 | Oscillator control input; bypass with an external capacitor to slow the oscillator. |
| 8                  | V <sup>+</sup>      | Power supply positive voltage input                                                 |

## 4.0 DETAILED DESCRIPTION

The TC7662B contains all the necessary circuitry to complete a negative voltage converter, with the exception of two external capacitors which may be inexpensive 1  $\mu\text{F}$  polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 4-2, which shows an idealized negative voltage converter. Capacitor  $C_1$  is charged to a voltage  $V^+$  for the 1/2 cycle when switches  $S_1$  and  $S_3$  are closed. (Note: Switches  $S_2$  and  $S_4$  are open during this 1/2 cycle.) During the second 1/2 cycle of operation, switches  $S_2$  and  $S_4$  are closed, with  $S_1$  and  $S_3$  open, thereby shifting capacitor  $C_1$  negatively by  $V^+$  volts. Charge is then transferred from  $C_1$  to  $C_2$  such that the voltage on  $C_2$  is exactly  $V^+$ , assuming ideal switches and no load on  $C_2$ . The TC7662B approaches this ideal situation more closely than existing non-mechanical circuits.

In the TC7662B, the four switches of Figure 4-2 are MOS power switches;  $S_1$  is a P-channel device and  $S_2$ ,  $S_3$  and  $S_4$  are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of  $S_3$  and  $S_4$  must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit start-up, and under output short circuit conditions ( $V_{\text{OUT}} = V^+$ ), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high-power losses and probable device latch-up.

The problem is eliminated in the TC7662B by a logic network which senses the output voltage ( $V_{\text{OUT}}$ ) together with the level translators and switches the substrates of  $S_3$  and  $S_4$  to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the TC7662B is an integral part of the anti-latchup circuitry; however, its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low-voltage operation, the LV pin should be connected to GND, and the regulator will be disabled. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure a latch-up proof operation and prevent device damage.

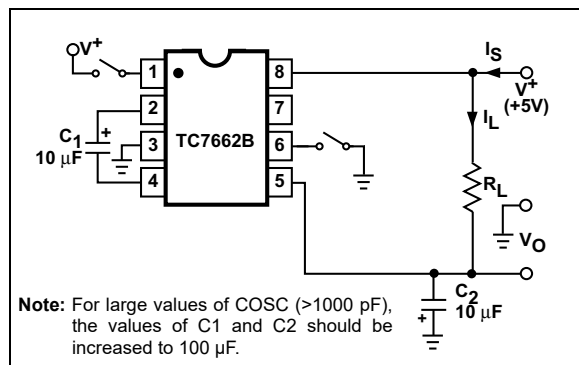


FIGURE 4-1: TC7662B Test Circuit.

## 4.1 Theoretical Power Efficiency Considerations

In theory, a voltage converter can approach 100% efficiency if certain conditions are met:

1. The drive circuitry consumes minimal power.
2. The output switches have extremely low ON resistance and virtually no offset.
3. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC7662B approaches these conditions for negative voltage conversion if large values of  $C_1$  and  $C_2$  are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is calculated using the formula:

$$E = \frac{1}{2} C_1 \times (V_1^2 - V_2^2)$$

$V_1$  and  $V_2$  are the voltages on  $C_1$  during the pump and transfer cycles. If the impedances of  $C_1$  and  $C_2$  are relatively high at the pump frequency (Figure 2-2) compared to the value of  $R_L$ , there will be a substantial difference in voltages  $V_1$  and  $V_2$ . Therefore, it is desirable not only to make  $C_2$  as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for  $C_1$  in order to achieve maximum efficiency of operation.

### Dos and Don'ts

1. Do not exceed maximum supply voltages.
2. Do not connect the LV terminal to GND for supply voltages greater than 3.5V.
3. Do not short circuit the output to  $V^+$  supply for voltages above 5.5V for extended periods; transient conditions including start-up are okay.

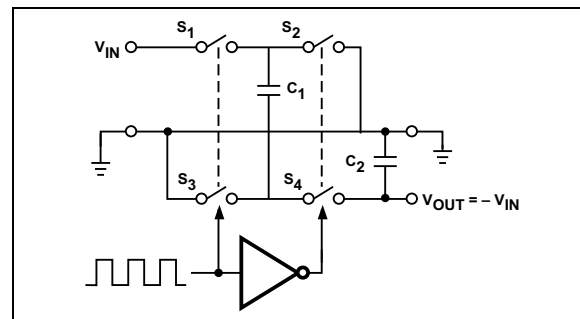


FIGURE 4-2: Idealized Negative Voltage Capacitor.

4. When using polarized capacitors in the Inverting mode, the + terminal of  $C_1$  must be connected to pin 2 of the TC7662B and the negative terminal of  $C_2$  must be connected to GND.
5. If the voltage supply driving the TC7662B has a large source impedance (25-30 $\Omega$ ), a 2.2  $\mu\text{F}$  capacitor from pin 8 to ground may be required to limit the rate of rise of the input voltage to less than 2V/ $\mu\text{sec}$ .

## 5.0 TYPICAL APPLICATIONS

### 5.1 Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the TC7662B for generation of negative supply voltages. Figure 5-1 shows typical connections to provide a negative supply where a positive supply of +1.5V to +15V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 3.5V.

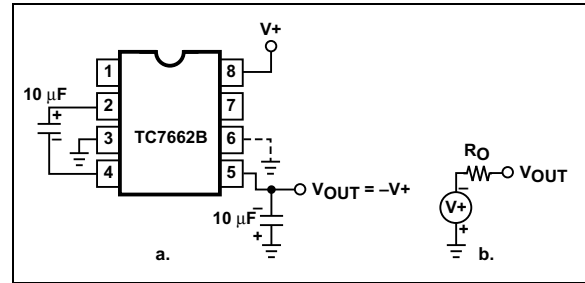


**FIGURE 5-1:** Simple Negative Converter and its Output Equivalent.

The output characteristics of the circuit in Figure 5-1 can be approximated by an ideal voltage source in series with a resistance as shown in Figure 5-1, section b. The voltage source has a value of  $-(V+)$ . The output impedance ( $R_O$ ) is a function of the ON resistance of the internal MOS switches (shown in Figure 4-2), the switching frequency, the value of  $C_1$  and  $C_2$  and the ESR (equivalent series resistance) of  $C_1$  and  $C_2$ . A good first order approximation for  $R_O$  is in Equation 5-1.

#### EQUATION 5-1:

$$R_O \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{f_{PUMP} \times C_1} + ESR_{C2}$$

Where  $f_{PUMP} = f_{OSC}/2$  and  $R_{SWx} =$  MOSFET, switch resistance. By combining the four  $R_{SWx}$  terms as  $R_{SW}$ , we get  $R_O$  in Equation 5-2.

#### EQUATION 5-2:

$$R_O \cong 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C_1} + 4 \times ESR_{C1} + ESR_{C2} \Omega$$

$R_{SW}$ , the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs, Figure 2-2 and Figure 2-5), typically  $23\Omega$  at  $+25^\circ\text{C}$  and 5V. Careful selection of  $C_1$  and  $C_2$  will reduce the remaining terms and minimize the output impedance. High value capacitors will reduce the  $1/(f_{PUMP} \times C_1)$  component, and low ESR capaci-

tors will lower the ESR term. Increasing the oscillator frequency will reduce the  $1/(f_{PUMP} \times C_1)$  term but may have the side effect of a net increase in output impedance when  $C_1 > 10 \mu\text{F}$ , and there is not enough time to fully charge the capacitors every cycle. In a typical application when  $f_{OSC} = 10 \text{ kHz}$  and  $C = C_1 = C_2 = 10 \mu\text{F}$ ,  $R_O$  in shown in Equation 5-3.

#### EQUATION 5-3:

$$R_O \cong 2 \times 23 + \frac{1}{5 \times 10^3 \times 10 \times 10^{-6}} + 4 \times ESR_{C1} + ESR_{C2}$$

$$R_O \cong (46 + 20 + 5 \times ESR_C) \Omega$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low  $1/(f_{PUMP} \times C_1)$  term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as  $10\Omega$ .

### 5.2 Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by two voltages, A and B, as shown in Figure 5-2. Segment A is the voltage drop across the ESR of  $C_2$  at the instant it goes from being

# TC7662B

charged by C1 (current flowing into C2) to being discharged through the load (current flowing out of C2). The magnitude of this current change is  $2 \times I_{OUT}$ , hence the total drop is  $2 \times I_{OUT} \times ESR_{C2}$  volts. Segment B is the voltage change across C2 during time  $t_2$ , the 1/2 of the cycle when C2 supplies current to the load. The drop at B is  $I_{OUT} \times t_2/C_2$  volts. The peak-to-peak ripple voltage is the sum of these voltage drops, as shown in Equation 5-4.

## EQUATION 5-4:

$$V_{RIPPLE} \cong \left( \frac{1}{2 \times f_{PUMP} \times C_1} + ESR_{C2} \times I_{OUT} \right)$$

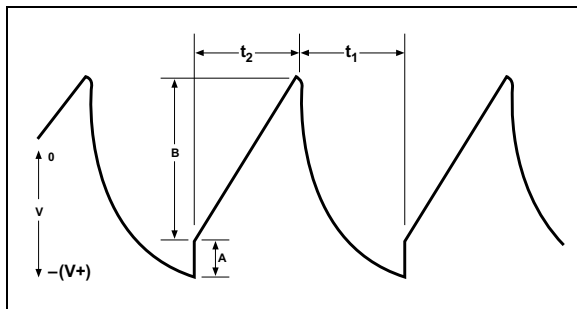


**FIGURE 5-2:** Output Ripple.

## 5.3 Paralleling Devices

Any number of TC7662B voltage converters may be paralleled to reduce output resistance (Figure 5-3). The reservoir capacitor, C2, serves all devices, while each device requires its own pump capacitor, C1. The resultant output resistance, as shown in Equation 5-5, would be approximately:

## EQUATION 5-5:

$$R_{OUT} = \frac{R_{OUT}(TC7662B)}{n}$$

$R_{OUT}(TC7662B)$  = the output resistance of the TC7662B, and  $n$  = the number of devices.

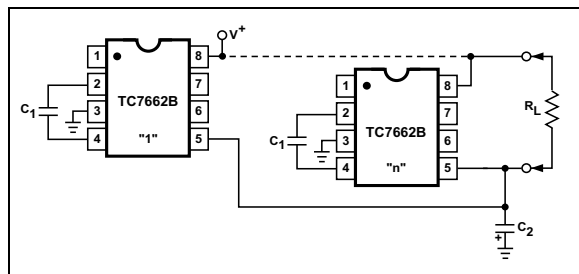


**FIGURE 5-3:** Paralleling Devices.

## 5.4 Cascading Devices

The TC7662B may be cascaded as shown in Figure 5-4 to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined in Equation 5-6.

## EQUATION 5-6:

$$V_{OUT} = -n(V_{IN})$$

$n$  is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TC7662B  $R_{OUT}$  values.

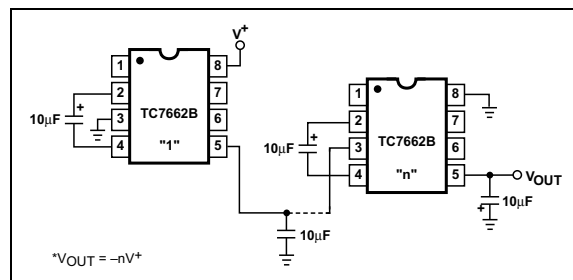


**FIGURE 5-4:** Cascading Devices for Increased Output Voltage.

## 5.5 Changing the TC7662B Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. This is achieved by one of several methods described in this section.

By connecting the BOOST pin (Pin 1) to  $V+$ , the oscillator charge and discharge current are increased and, hence, the oscillator frequency is increased by approximately 3.5 times. The result is a decrease in the output impedance and ripple. This is of major importance for surface mount applications where capacitor size and cost are critical. Smaller capacitors, e.g., 0.1  $\mu F$ , can be used in conjunction with the Boost pin in order to achieve similar output currents compared to the device free running with  $C_1 = C_2 = 1 \mu F$  or 10  $\mu F$ .

Increasing the oscillator frequency can also be achieved by overdriving the oscillator from an external clock as shown in Figure 5-5. In order to prevent device latch-up, a 1 k $\Omega$  resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 k $\Omega$  pull-up resistor to  $V+$  supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

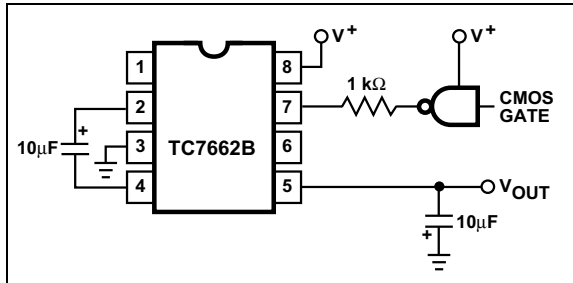


**FIGURE 5-5:** External Clocking.

It is also possible to increase the conversion efficiency of the TC7662B at low load levels by lowering the oscillator frequency. This reduces the switching losses (See Figure 5-6). However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C1) and reservoir (C2) capacitors; this is overcome by increasing the values of C1 and C2 by the same factor that the frequency has been reduced. For example, the addition of a 100 pF capacitor between pin 7 (Osc.) and V+ will lower the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (multiple of 10), and, thereby, necessitate a corresponding increase in the value of C1 and C2 (from 10 µF to 100 µF).

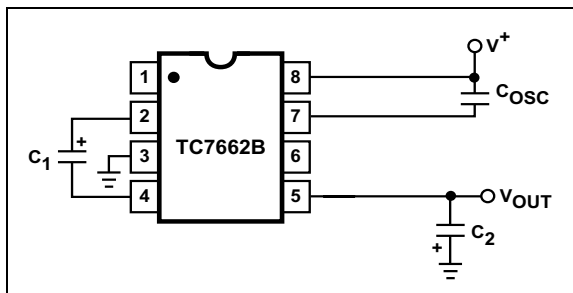


**FIGURE 5-6:** Lowering Oscillator Frequency.

## 5.6 Positive Voltage Doubling

The TC7662B may be employed to achieve positive voltage doubling using the circuit shown in Figure 5-7. In this application, the TC7662B's pump inverter switches are used to charge C1 to a voltage level of  $V^+ - V_F$  (where  $V^+$  is the supply voltage and  $V_F$  is the forward voltage on C1 plus the supply voltage ( $V^+$ ) applied through diode D2 to capacitor C2). The voltage thus created on C2 becomes  $(2 V^+) - (2 V_F)$ , or twice the supply voltage minus the combined forward voltage drops of diodes D1 and D2.

The source impedance of the output ( $V_{OUT}$ ) will depend on the output current, but for  $V^+ = 5V$  and an output current of 10 mA, it will be approximately 60Ω.

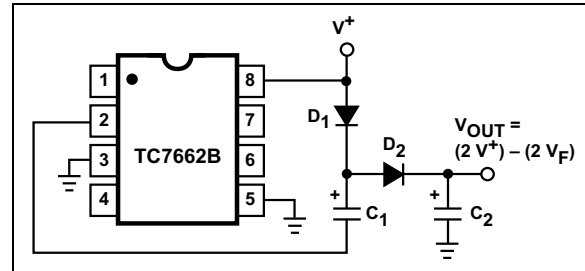


**FIGURE 5-7:** Positive Voltage Multiplier.

## 5.7 Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 5-8 combines the functions shown in Figure 5-1 and Figure 5-7 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9V and -5V from an existing +5V supply. In this instance, capacitors C1 and C3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C2 and C4 are pump and reservoir, respectively, for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

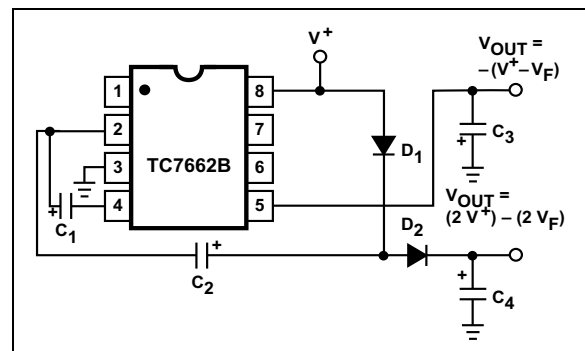


**FIGURE 5-8:** Combined Negative Converter and Positive Doubler.

## 5.8 Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in 1/2, as shown in Figure 5-9. The combined load will be evenly shared between the two sides, and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 5-4, +15V can be converted (via +7.5V and -7.5V) to a nominal -15V, with a rather high series resistance (~250Ω).

# TC7662B

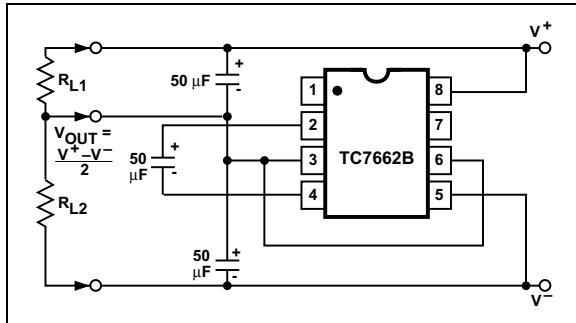


**FIGURE 5-9:** Splitting a Supply in Half.

## 5.9 Regulated Negative Voltage Supply

In some cases, the output impedance of the TC7662B can be a problem, particularly if the load current varies substantially. The circuit in Figure 5-10 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is advisable, since the TC7662B's output does not respond instantaneously to change in input but only after the switching delay. The circuit shown in Figure 5-10 supplies enough delay to accommodate the TC7662B while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown in Figure 5-10 provide an output impedance of less than 5Ω to a load of 10 mA.

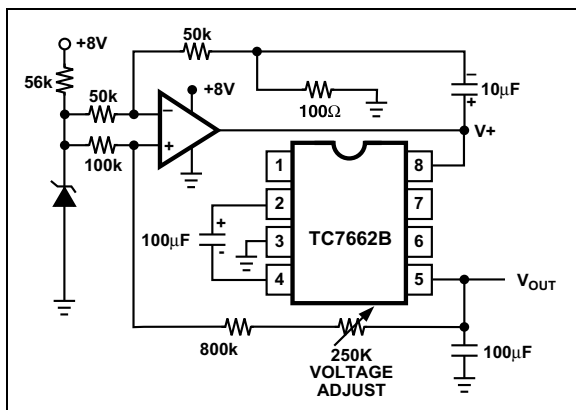


**FIGURE 5-10:** Regulating the Output Voltage.

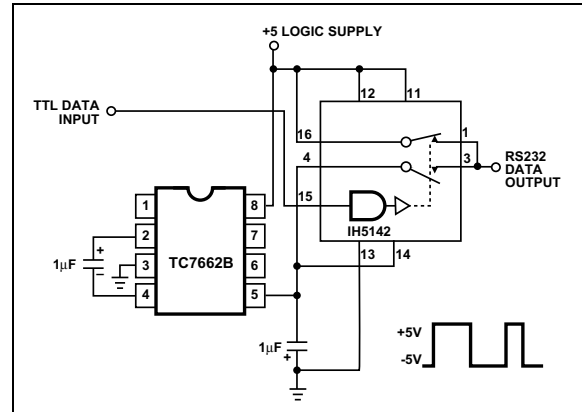
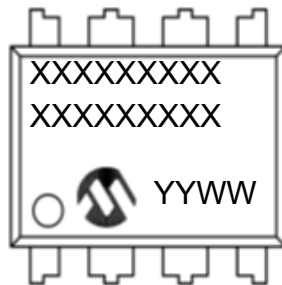


**FIGURE 5-11:** RS232 Levels from a Single 5V Supply.

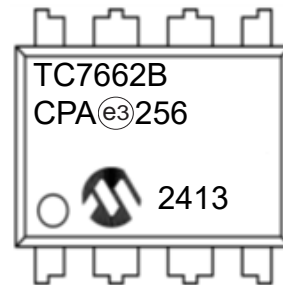
## 6.0 PACKAGE INFORMATION

### 6.1 Package Marking Information

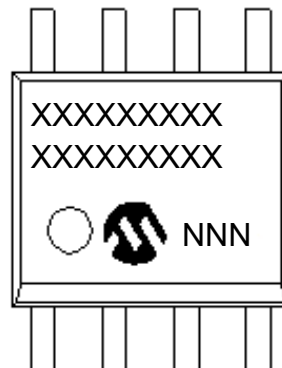
8-Lead PDIP



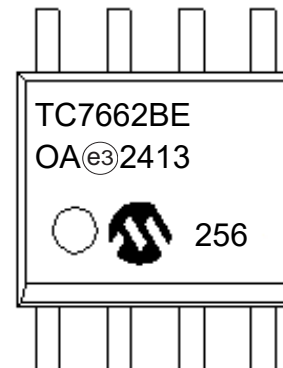
Example:



8-Lead SOIC



Example:



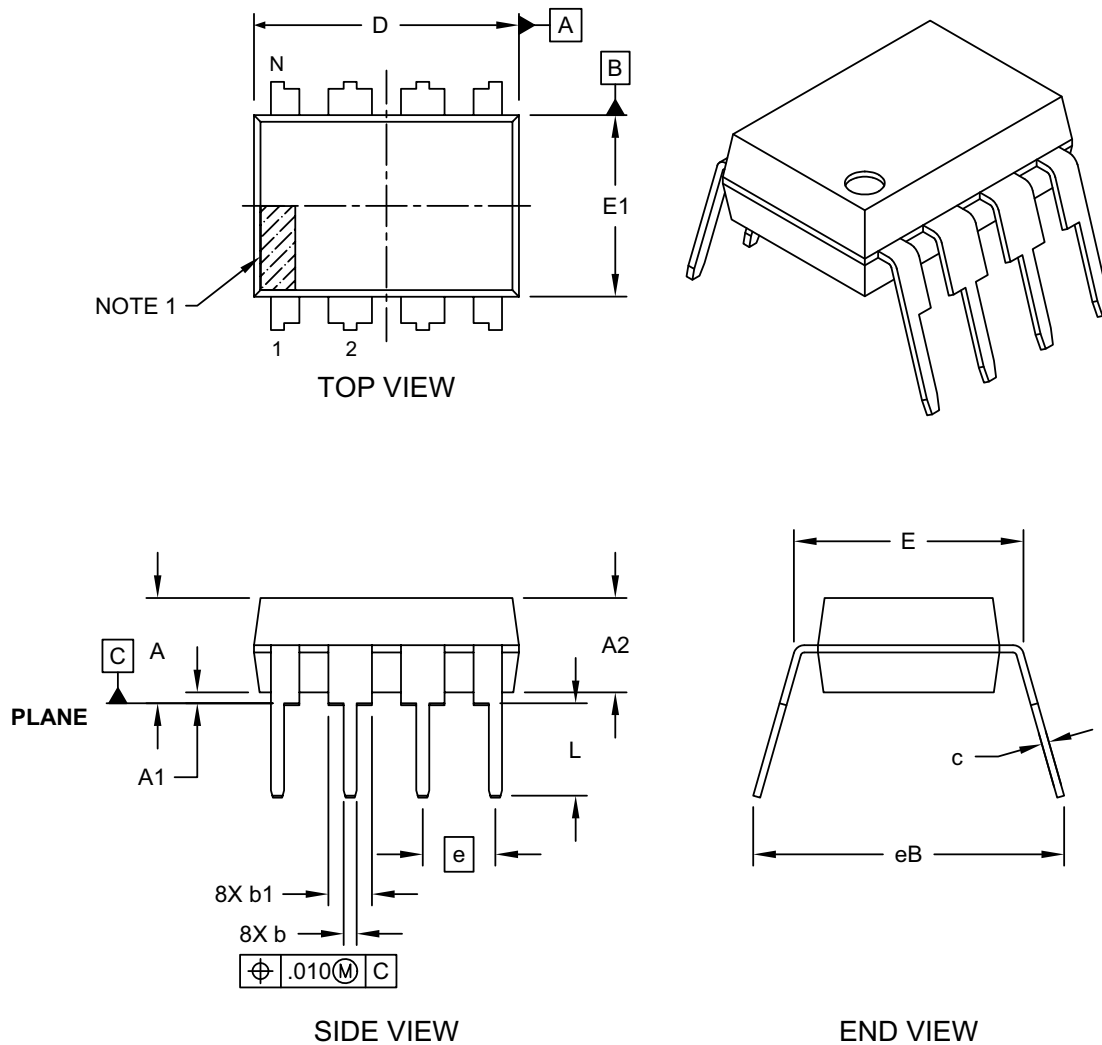
|                |        |                                                                                                                  |
|----------------|--------|------------------------------------------------------------------------------------------------------------------|
| <b>Legend:</b> | XX...X | Product Code or Customer-specific information                                                                    |
|                | Y      | Year code (last digit of calendar year)                                                                          |
|                | YY     | Year code (last 2 digits of calendar year)                                                                       |
|                | WW     | Week code (week of January 1 is week '01')                                                                       |
|                | NNN    | Alphanumeric traceability code                                                                                   |
|                | Ⓔ3     | Pb-free JEDEC designator for Matte Tin (Sn)                                                                      |
|                | *      | This package is Pb-free. The Pb-free JEDEC designator (Ⓔ3) can be found on the outer packaging for this package. |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

# TC7662B

## 8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

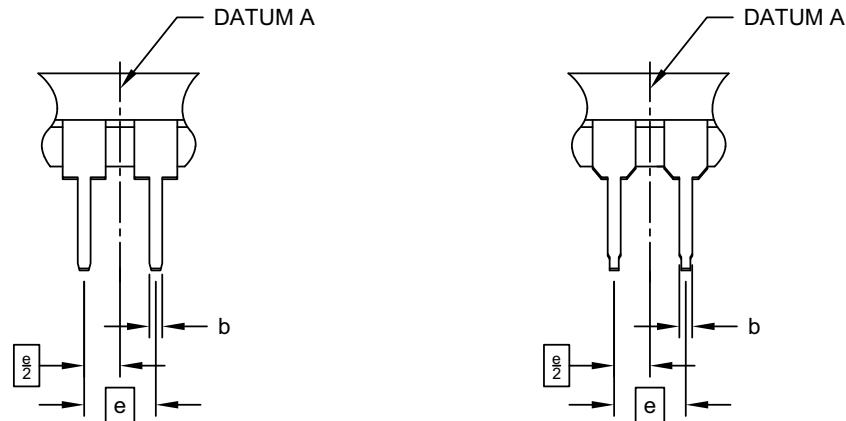


Microchip Technology Drawing No. C04-018-PA Rev G Sheet 1 of 2

## 8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

ALTERNATE LEAD DESIGN  
(NOTE 5)



| Units                      |    | INCHES   |      |      |
|----------------------------|----|----------|------|------|
| Dimension Limits           |    | MIN      | NOM  | MAX  |
| Number of Pins             | N  | 8        |      |      |
| Pitch                      | e  | .100 BSC |      |      |
| Top to Seating Plane       | A  | -        | -    | .210 |
| Molded Package Thickness   | A2 | .115     | .130 | .195 |
| Base to Seating Plane      | A1 | .015     | -    | -    |
| Shoulder to Shoulder Width | E  | .290     | .310 | .325 |
| Molded Package Width       | E1 | .240     | .250 | .280 |
| Overall Length             | D  | .348     | .365 | .400 |
| Tip to Seating Plane       | L  | .115     | .130 | .150 |
| Lead Thickness             | c  | .008     | .010 | .015 |
| Upper Lead Width           | b1 | .040     | .060 | .070 |
| Lower Lead Width           | b  | .014     | .018 | .022 |
| Overall Row Spacing        | §  | eB       | -    | .430 |

**Notes:**

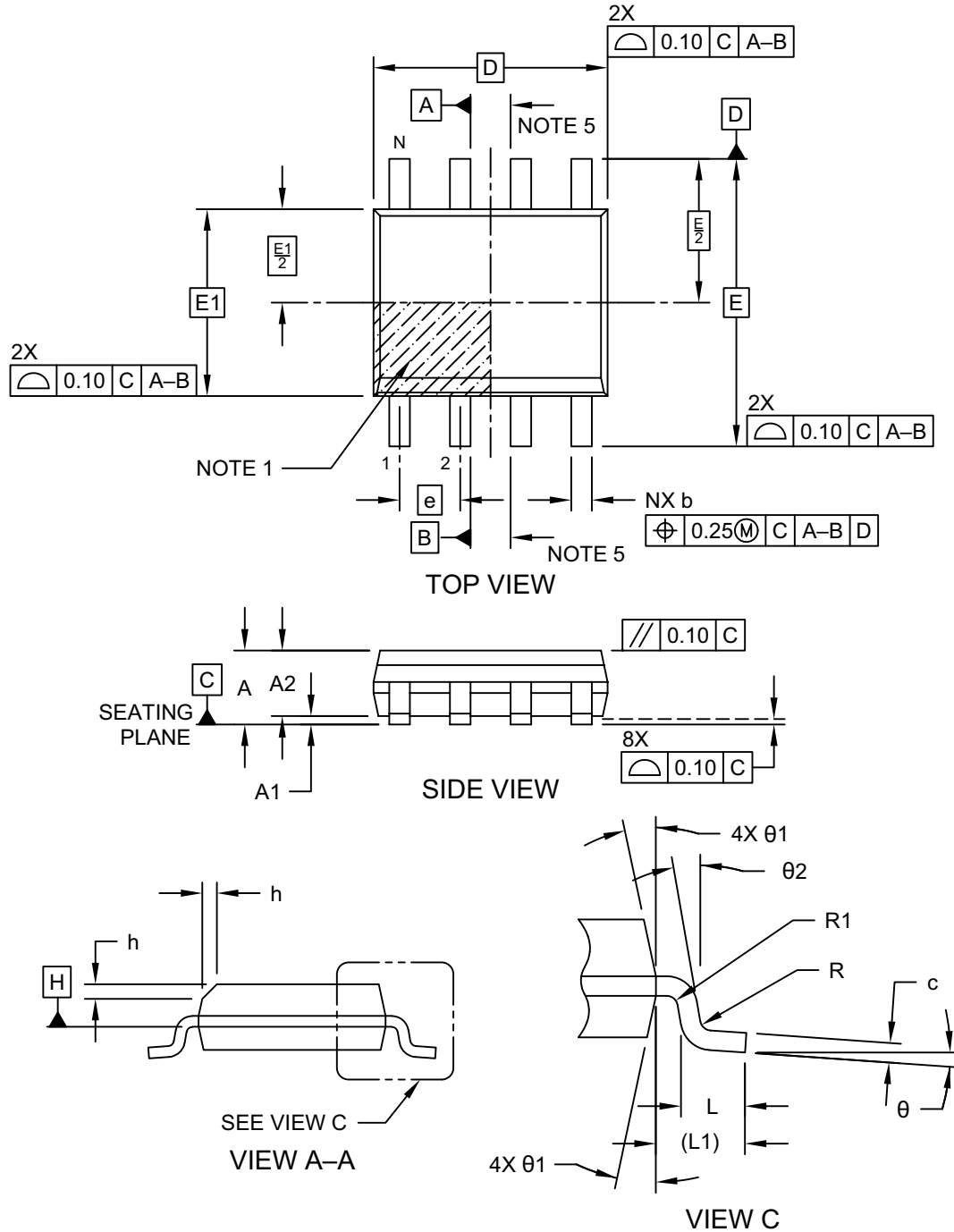
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-PA Rev G Sheet 2 of 2

# TC7662B

## 8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

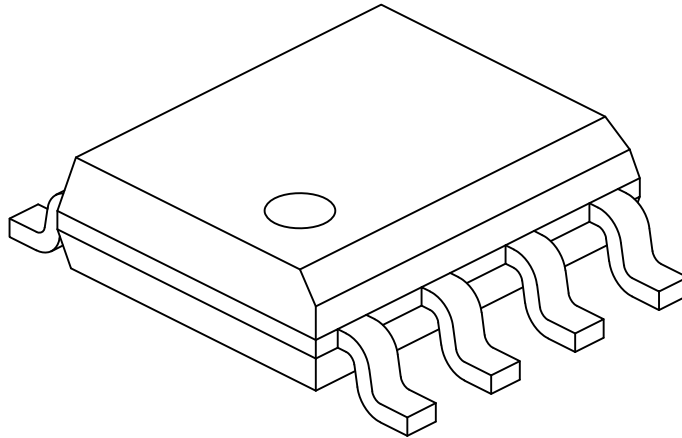
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-057-OA Rev K Sheet 1 of 2

## 8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                    |    | MILLIMETERS |     |      |
|--------------------------|----|-------------|-----|------|
| Dimension Limits         |    | MIN         | NOM | MAX  |
| Number of Pins           | N  | 8           |     |      |
| Pitch                    | e  | 1.27 BSC    |     |      |
| Overall Height           | A  | –           | –   | 1.75 |
| Molded Package Thickness | A2 | 1.25        | –   | –    |
| Standoff §               | A1 | 0.10        | –   | 0.25 |
| Overall Width            | E  | 6.00 BSC    |     |      |
| Molded Package Width     | E1 | 3.90 BSC    |     |      |
| Overall Length           | D  | 4.90 BSC    |     |      |
| Chamfer (Optional)       | h  | 0.25        | –   | 0.50 |
| Foot Length              | L  | 0.40        | –   | 1.27 |
| Footprint                | L1 | 1.04 REF    |     |      |
| Lead Thickness           | c  | 0.17        | –   | 0.25 |
| Lead Width               | b  | 0.31        | –   | 0.51 |
| Lead Bend Radius         | R  | 0.07        | –   | –    |
| Lead Bend Radius         | R1 | 0.07        | –   | –    |
| Foot Angle               | θ  | 0°          | –   | 8°   |
| Mold Draft Angle         | θ1 | 5°          | –   | 15°  |
| Lead Angle               | θ2 | 0°          | –   | –    |

**Notes:**

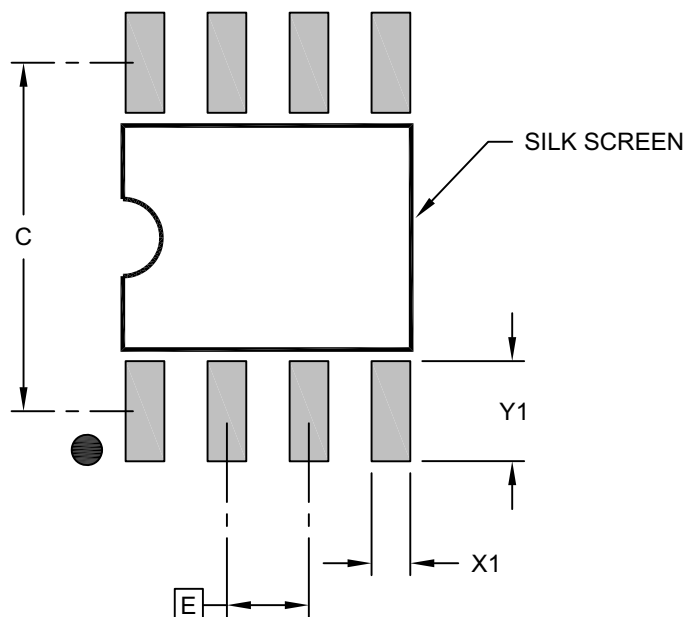
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
  - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-OA Rev K Sheet 2 of 2

# TC7662B

## 8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

| Dimension Limits        | Units | MILLIMETERS |      |      |
|-------------------------|-------|-------------|------|------|
|                         |       | MIN         | NOM  | MAX  |
| Contact Pitch           | E     | 1.27 BSC    |      |      |
| Contact Pad Spacing     | C     |             | 5.40 |      |
| Contact Pad Width (X8)  | X1    |             |      | 0.60 |
| Contact Pad Length (X8) | Y1    |             |      | 1.55 |

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-OA Rev K

## APPENDIX A: REVISION HISTORY

### Revision B (May 2025)

- Updated document layout.
- Added “Switching Frequency” and [Note 5](#) to the [Electrical Characteristics](#) table.
- Added [Section 3.0 “Pin Descriptions”](#).

### .Revision A (March 2001)

- Original release of this document.

# TC7662B

---

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO.                              |  | X                                               | XX                                                  | XXX           |
|---------------------------------------|--|-------------------------------------------------|-----------------------------------------------------|---------------|
| Device                                |  | Temperature Range                               | Package                                             | Tape and Reel |
| Device:                               |  | TC7662B: Charge Pump DC-to-DC Voltage Converter |                                                     |               |
| Temperature Range:                    |  | C                                               | = 0°C to +70°C (Commercial)                         |               |
|                                       |  | E                                               | = -40°C to +125°C (Extended)                        |               |
| Packages:                             |  | PA                                              | = 8-Lead PDIP                                       |               |
|                                       |  | OA                                              | = 8-Lead SOIC                                       |               |
| Tape and Reel Option <sup>(1)</sup> : |  | (blank)                                         | = Standard Packaging, 100/Tube SOIC<br>60/Tube PDIP |               |
|                                       |  | 713                                             | = Tape and Reel, 3300/Reel (SOIC package only)      |               |

**Examples:**

a) TC7662BCPA: Charge Pump DC-to-DC Voltage Converter, Commercial Temperature Range, PDIP Package, Tube

b) TC7662BEP A: Charge Pump DC-to-DC Voltage Converter, Extended Temperature Range, PDIP Package, Tube

c) TC7662BCOA: Charge Pump DC-to-DC Voltage Converter, Commercial Temperature Range, SOIC Package, Tube

d) TC7662BEOA: Charge Pump DC-to-DC Voltage Converter, Extended Temperature Range, SOIC Package, Tube

e) TC7662BCOA713: Charge Pump DC-to-DC Voltage Converter, Commercial Temperature Range, SOIC Package, Tape and Reel

f) TC7662BEOA713: Charge Pump DC-to-DC Voltage Converter, Extended Temperature Range, SOIC Package, Tape and Reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

# TC7662B

---

NOTES:

---

---

## Microchip Information

### Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at <https://www.microchip.com/en-us/about/legalinformation/microchip-trademarks>.

ISBN: 979-8-3371-1157-5

### Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at [www.microchip.com/en-us/support/design-help/client-support-services](http://www.microchip.com/en-us/support/design-help/client-support-services).

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

### Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.