

Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO**FUNCTIONAL DESCRIPTION**

The ASPL8801 series is a CMOS-based positive low-dropout linear regulator (LDO) featuring 500 mA/ 1.0A that provides high PSRR, high output voltage accuracy, low-noise and low supply current

It consists of a voltage reference, an error amplifier, a resistor-ladder for output voltage setting. It also has under-voltage lockout (UVLO), over current/short circuit protection circuit and over temperature shutdown circuit.

The ASPL8801 typically has 90mV dropout voltage (TDFN2020-6, I_{out}=500mA, V_{out}=1.8V) and 180mV dropout voltage (TDFN2020-6, I_{out}=1A, V_{out}=1.8V) and chip enable function (EN) for long battery life.

Excellent ripple rejection, load transient and line transient response make it ideal for the power sources of mobile communication devices or camera modules in low light condition. It can also turn on under full load condition, making it suitable for harsh system environment.

The ASPL8801 series LDOs have option for output current limit between 1.0A or 500mA by alternating the LCON pin between "H" or "L" for TDFN2020-6 package version.

MAIN FEATURES

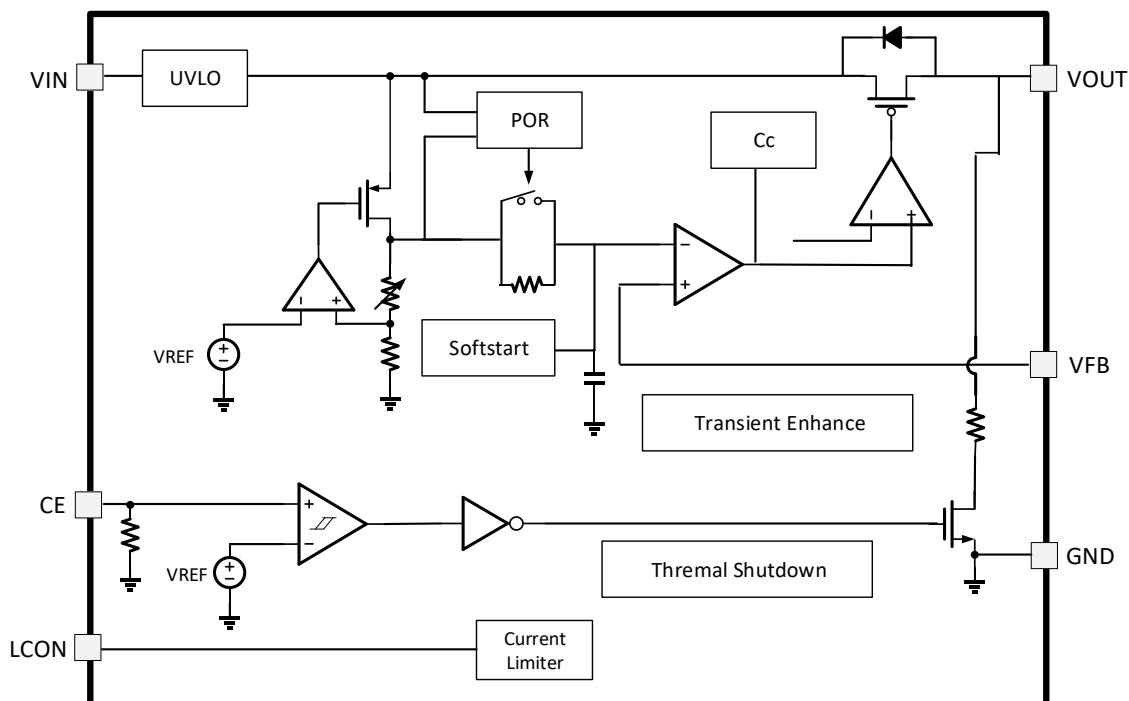
- Supply Current (no load) : 85μA (typ.)
- Supply Current (Standby) : 0.1μA (typ.)
- Dropout Voltage: 156mV(TDFN2020-6, I_{out}=1A, V_{out}=1.8V, typ.)
- High-PSRR
95dB (f=5kHz, I_{out}=10mA, lower V_{out})
85dB (f=5kHz, I_{out}=150mA, lower V_{out})
- Output Noise: 10μVrms (10-100KHz, 0.85V output voltage settings, typ.)
- Line Regulation: 0.01%/V
- Fixed Mode Voltage Range: 0.85V to 4.3V with 0.05V step.
- Adjustable Mode Voltage Range: 0.85V to 4.3V.
- Built-in Short Current Protection Limit: 120mA (LCON='H', 1.0A, typ.)
- Built-in Peak Current Protection Limit: 1.7A (LCON='H', 1.0A, typ.)
- Over Temperature Protection and Auto Recover
- Built-in Soft-Start and Inrush Current Limit
- Fast Auto Discharge Function for Power Down

APPLICATIONS

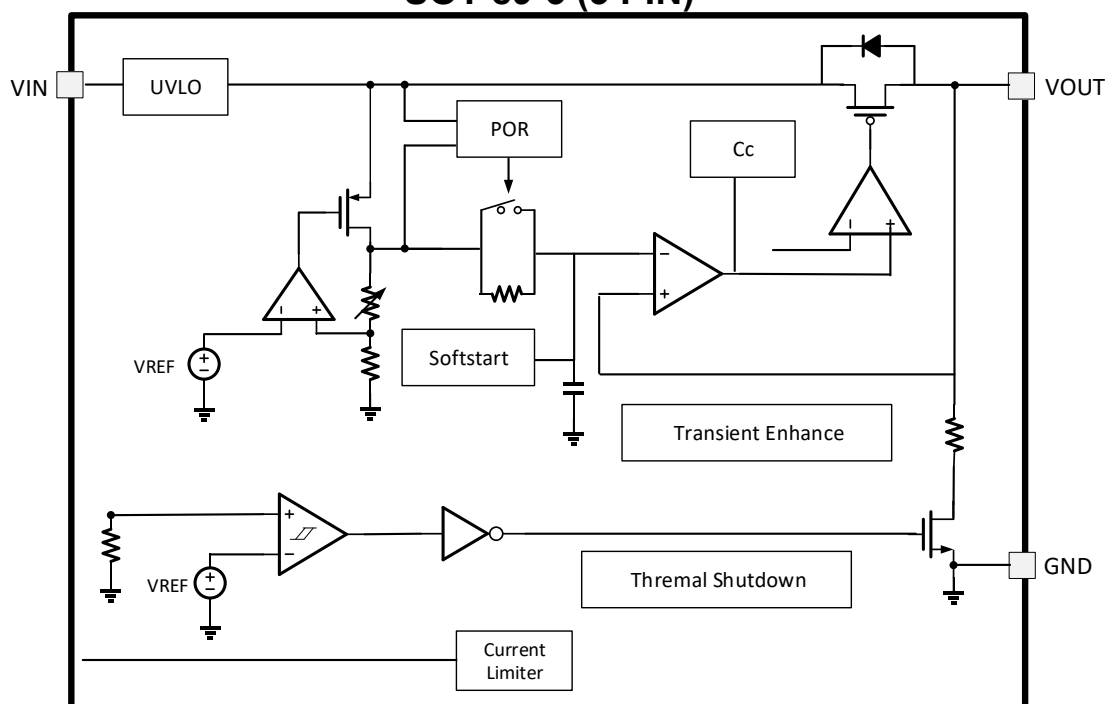
- Portable Device , Tablets and Smartphone
- Cameras, VCRs and Car Dash Cameras
- Low Light & Low Noise Cam Application
- Communications and Infrastructure
- AR or VR Application

BLOCK DIAGRAMS

TDFN2020-6 (6 PIN)

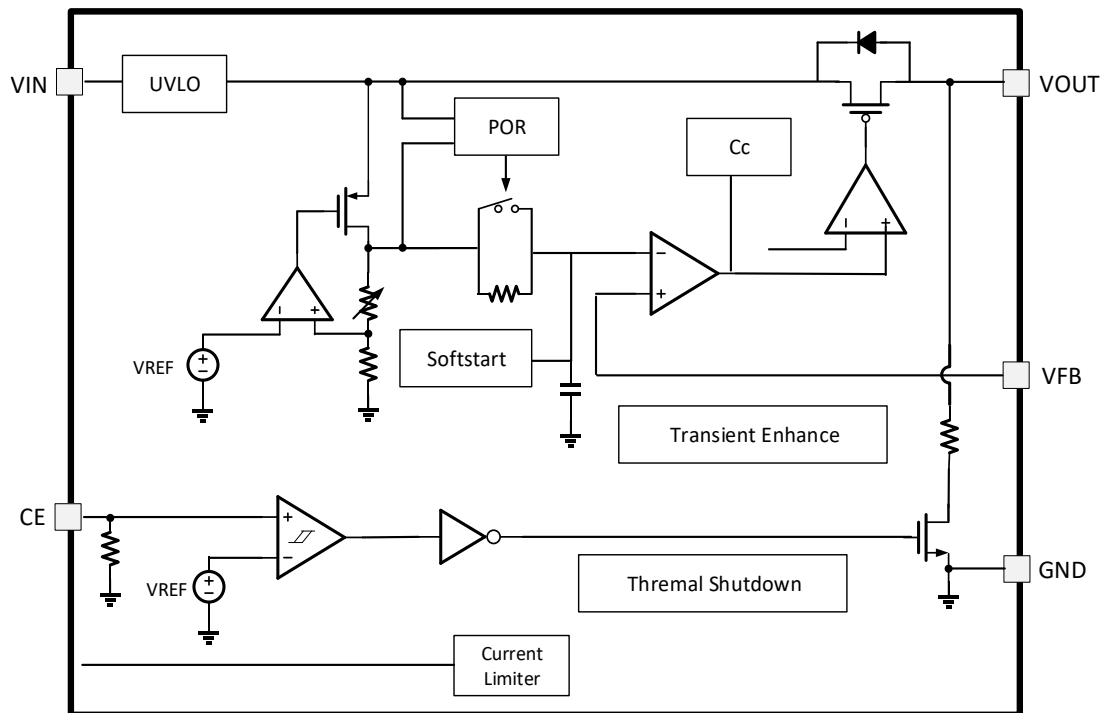


SOT-89-3 (3 PIN)

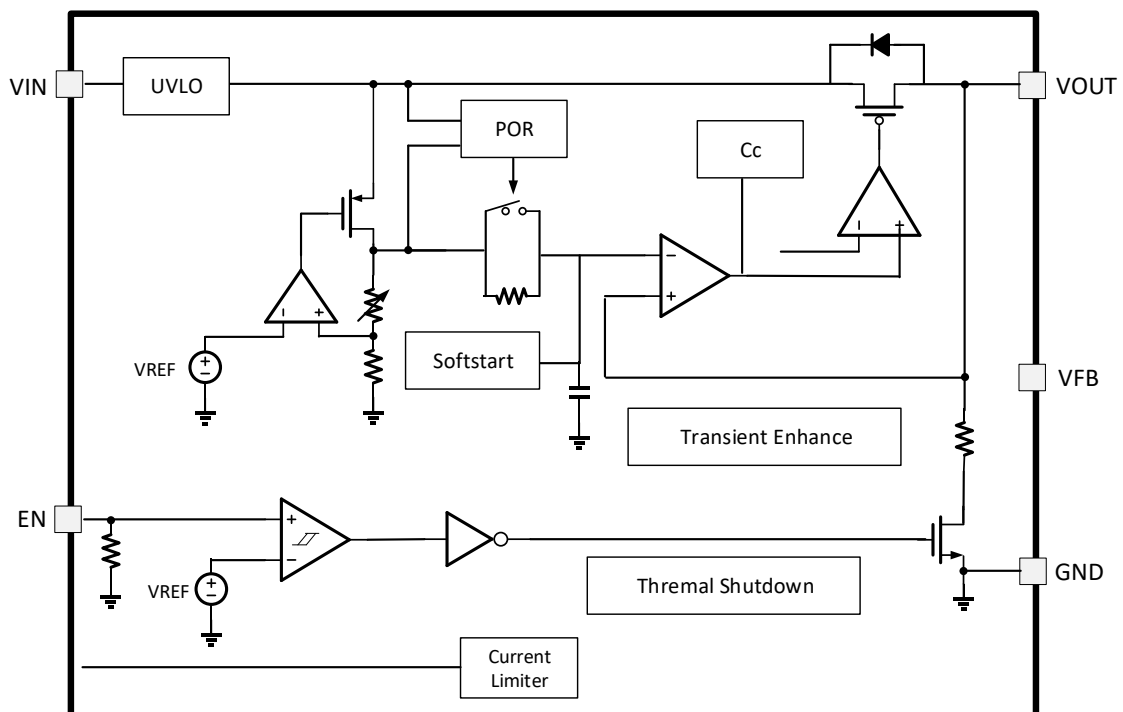


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SOT-89-5 (5 PIN)

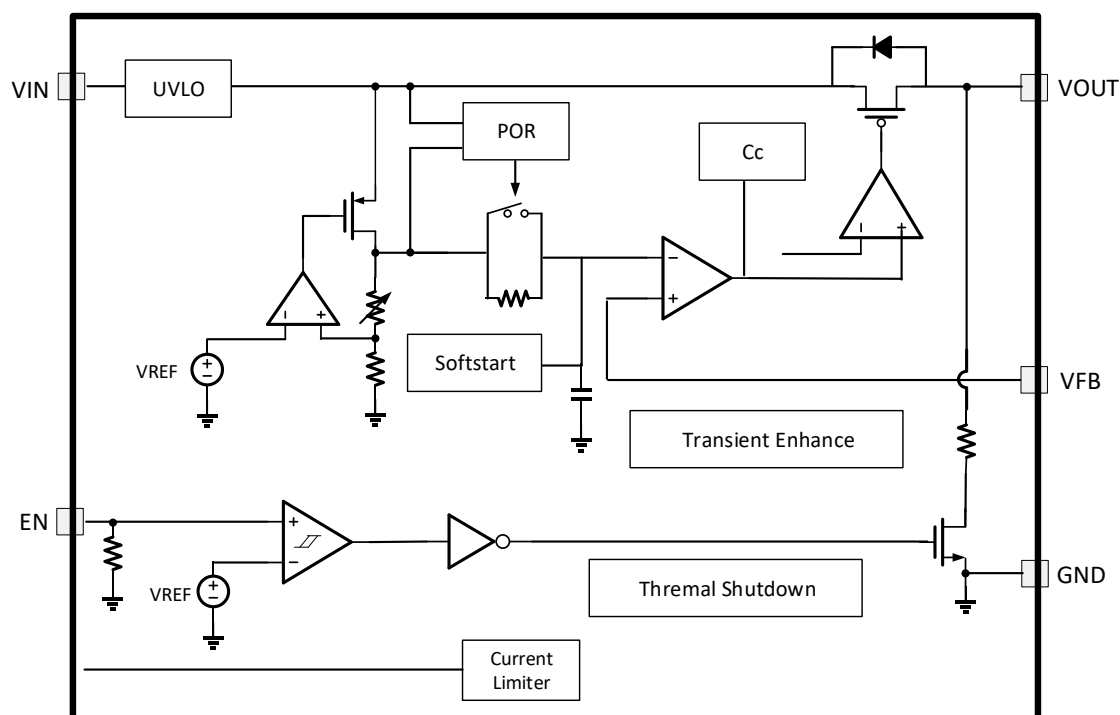


SOT-23-5 Fixed Mode (5 PIN)



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SOT-23-5 ADJ Mode (5 PIN)



***NOTICE : In SOT89-3, SOT89-5 and SOT23-5 package, ASPL8801 only support 1A current capability.**

SELECTION GUIDE

Product Name :ASPL8801-xxx-P

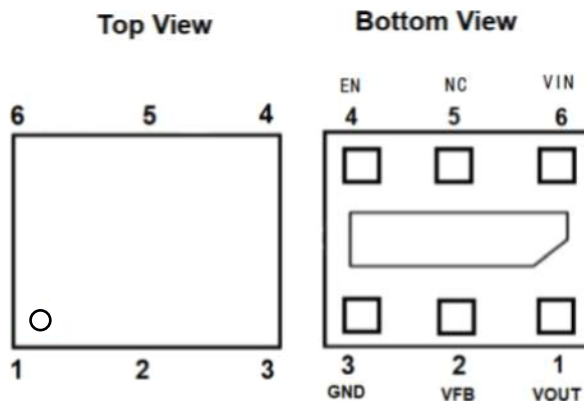
- xxx = Output Voltage → 120=1.2V , 330=3.3V , 085=0.85V
- P: Package → TH=TDFN2020-6 ; DI=SOT89-3 ; ZD=SOT23-5 fixed mode, ZD=SOT23-5 adj mode

(ASPL8801 series LDOs offer VOUT voltage available in 0.85V~4.30V with 0.05V step)

e.g. ASPL8801-120-TH → Original Version. Output voltage=1.2V, TDFN2020-6 package.

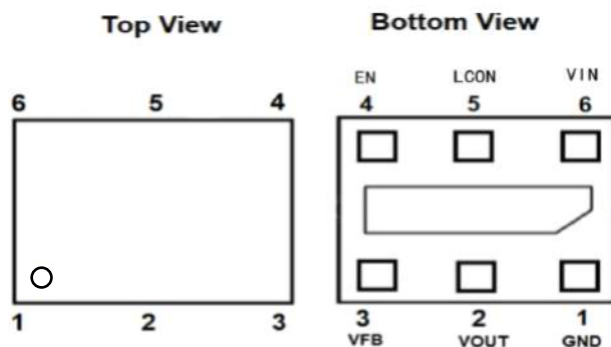
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

PACKAGE INFORMATION & PIN DESCRIPTION



TDFN2020-6 Pin Configuration

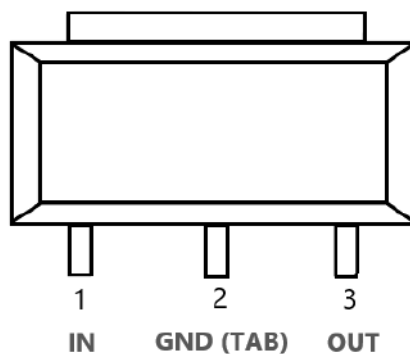
PIN No	Symbol	Pin Description
1	VOUT	Output Pin
2	VFB	Feedback Pin. In Adj mode, this is used to set VOUT
3	GND	Ground Pin
4	EN	Chip Enable Pin
5	NC	Normally Close
6	VIN	Input Pin
Exposed Pad	left open or connected to common ground	Connect to PCB metal area for heatsink purposes



TDFN2020-6 Pin Configuration

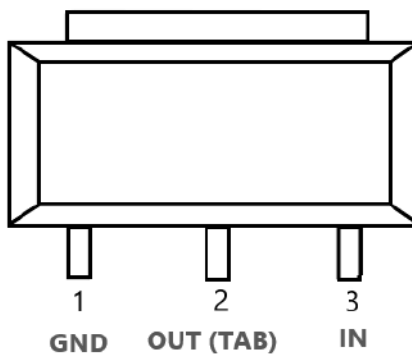
PIN No	Symbol	Pin Description
1	GND	Ground Pin
2	VOUT	Output Pin
3	VFB	Feedback Pin. In Adj mode, this is used to set VOUT
4	EN	Chip Enable Pin
5	LCON	Output Current Limit Alternate Pin
6	VIN	Input Pin
Exposed Pad	left open or connected to common ground	Connect to PCB metal area for heatsink purposes

Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO



SOT-89-3-AFT

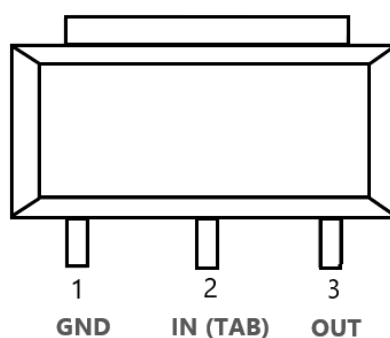
PIN No	Symbol	Pin Description
1	VIN	Input Pin
2	GND (TAB)	Ground Pin
3	OUT	Output Pin



SOT-89-3-BFT

PIN No	Symbol	Pin Description
1	GND	Ground Pin
2	OUT (TAB)	Output Pin
3	VIN	Input Pin

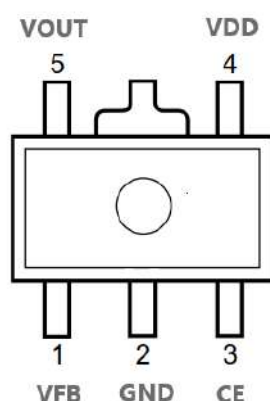
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO



SOT-89-3-CFT

Pin Configuration

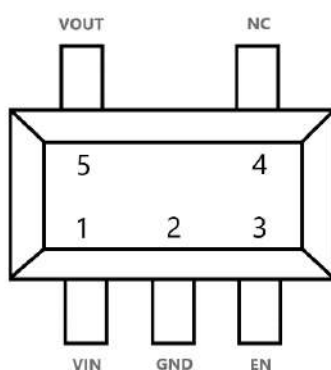
PIN No	Symbol	Pin Description
1	GND	Ground Pin
2	VIN (TAB)	Input Pin
3	OUT	Output Pin



SOT-89-5 Pin Configuration

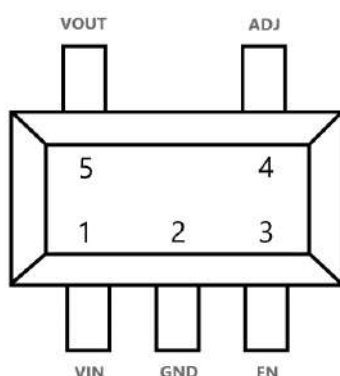
PIN No	Symbol	Pin Description
1	VFB	Feedback Pin. In Adj mode, this is used to set VOUT
2	GND	Ground Pin
3	CE	Chip Enable Pin
4	VDD	Input Pin
5	VOUT	Output Pin

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SOT-23-5 Pin Configuration (Fixed Mode)

PIN No	Symbol	Pin Description
1	VIN	Input Pin
2	GND	Ground Pin
3	EN	Chip Enable Pin
4	NC	No Connection
5	VOUT	Output Pin

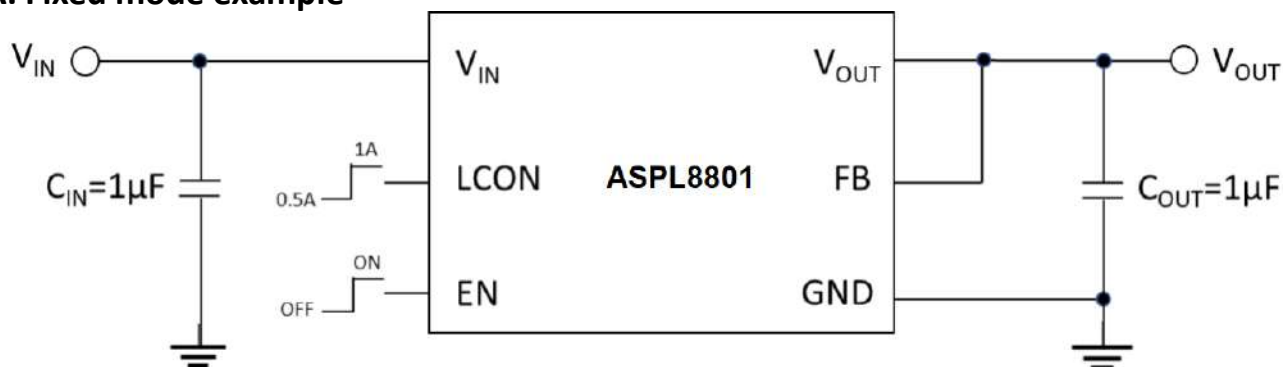


SOT-23-5 Pin Configuration (ADJ Mode)

PIN No	Symbol	Pin Description
1	VIN	Input Pin
2	GND	Ground Pin
3	EN	Chip Enable Pin
4	ADJ	ADJ Pin. In Adjustable mode, this is used to set VOUT
5	VOUT	Output Pin

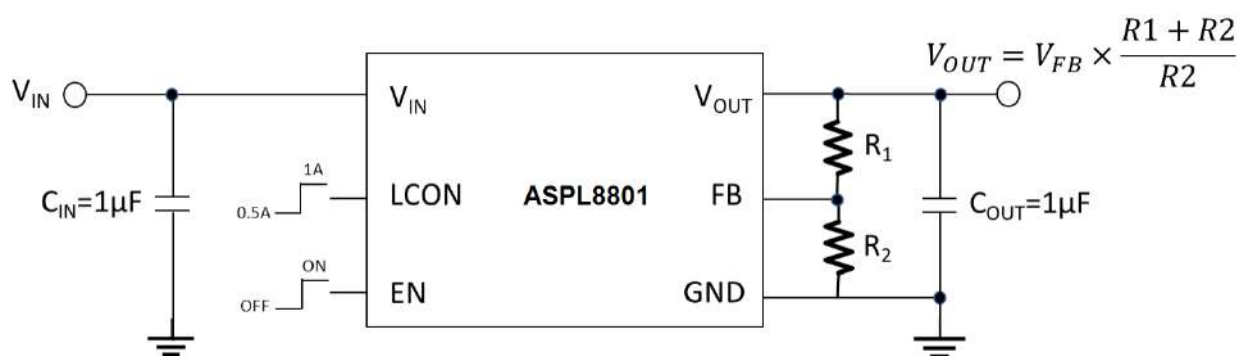
TYPICAL APPLICATION CIRCUIT

A. Fixed mode example



* Recommended Ceramic Capacitors for Vin and Vout: 1uF

B. Adjustable (ADJ) mode example



The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2 , according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2)$$

For this device, $V_{FB} = 0.85$ V.

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100)$$

For this device, $I_{FB} = 10$ nA.

Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating		Unit
V_{IN}	Input Voltage	6.0		V
V_{CE}	Input Voltage (CE Pin)	-0.3 to 6.0		V
V_{LCON}	Input Voltage (LCON Pin)	-0.3 to 6.0		V
V_{OUT}	Output Voltage	-0.3 to 6.0		V
P_D	Power Dissipation (Standard Land Pattern)	TDFN2020-6L	1400	mW
T_{OP}	Junction Temperature Range	-40 to 125		°C
T_{STG}	Storage Temperature Range	-55 to 125		°C

*The effective storage period is 24 months (I storage condition) .

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	1.32 to 5.5	V
V_{OUT}	Output Voltage	0.85 to 4.3	V
T_a	Operating Temperature Range	-40 to 85	°C
C_{IN}/C_{OUT}	Input/Output Capacitance	1/1	uF

ELECTROSTATIC DISCHARGE

Symbol	Parameter	Value	Unit
ESD	Human Body Mode	± 4	kV
	Machine Mode	± 250	V
	Charge Device Mode	± 1000	V

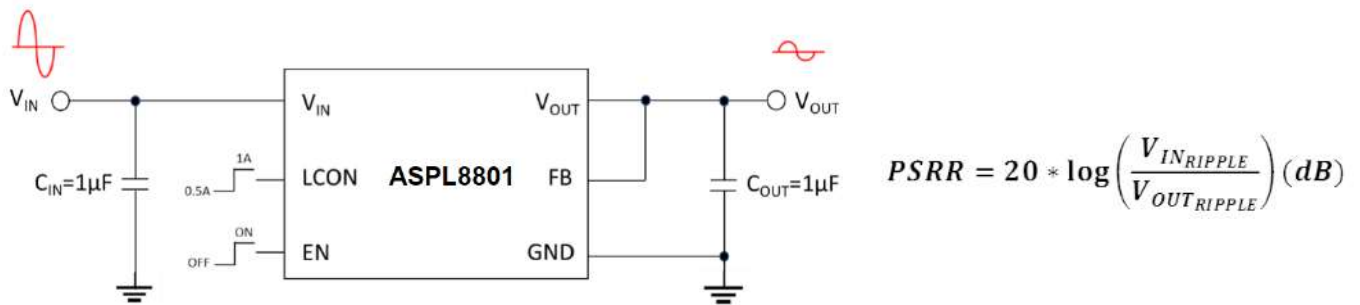
THERMAL DATA

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal resistance junction-ambient	80	°C/W

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ELECTRICAL CHARACTERISTICS

$V_{IN} = V_{SET}^{(1)} + 1.0\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = C_{OUT} = 1.0\text{ }\mu\text{F}$, typical values are at $T_J = 25\text{ }^\circ\text{C}$;
min./max. values are at $-40\text{ }^\circ\text{C} \leq T_J \leq 125\text{ }^\circ\text{C}$, unless otherwise noted.

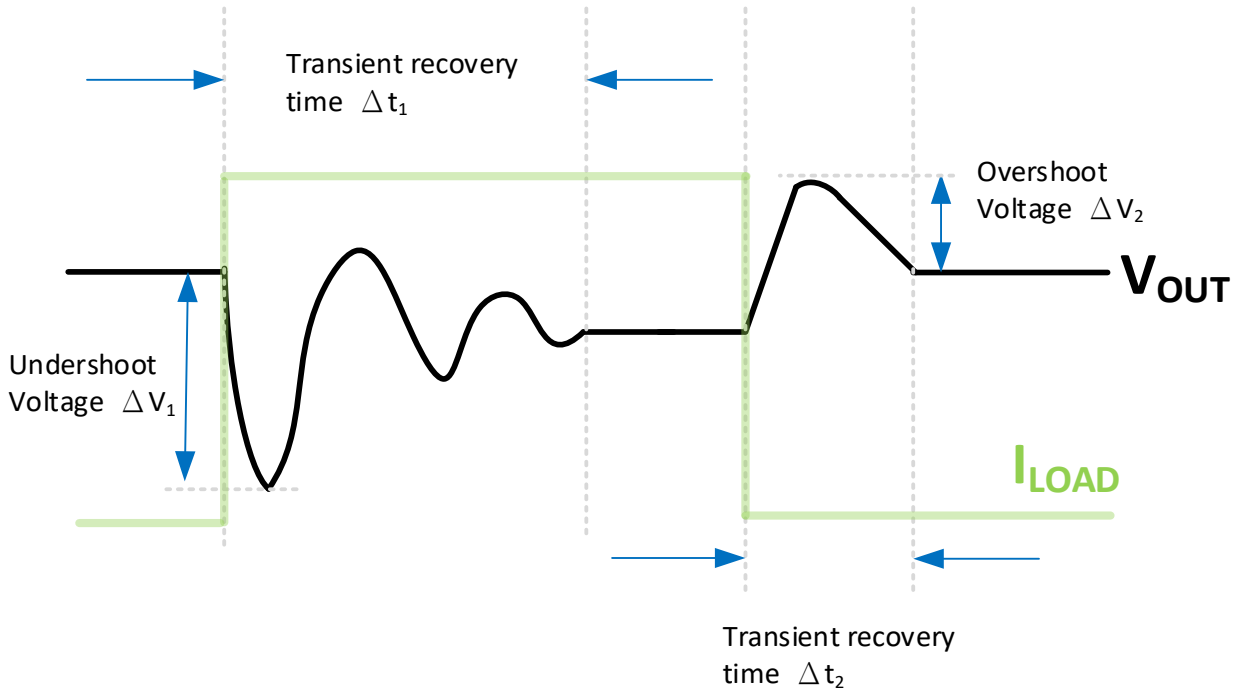
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.32		5.50	V
V_{OUT}	V_{OUT} accuracy	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$; $I_{OUT} = 0\text{ to }1\text{ A}$; $-40\text{ }^\circ\text{C} \leq T_J \leq 125\text{ }^\circ\text{C}$	-1.0		+1.0	%
ΔV_{OUT}	Static line regulation			0.01		%/V
ΔV_{OUT}	Static load regulation	$I_{OUT} = 10\text{ mA to }1000\text{ mA}$		1	2	mV
V_{DROP}	Dropout voltage	$I_{OUT} = 1\text{ A}$	$V_{OUT}=0.85\text{V}$	<420		mV
			$V_{OUT}=1.2\text{V}$	260		
			$V_{OUT}=1.8\text{V}$	156		
			$V_{OUT}=2.5\text{V}$	110		
			$V_{OUT}=3.3\text{V}$	95		
			$V_{OUT}=4.3\text{V}$	60		
I_Q	Quiescent current	$I_{OUT} = 0\text{ mA}$		85		μA
$I_{Standby}$	Standby current	V_{IN} input current in OFF MODE: $V_{EN} = \text{GND}$		0.1		μA
I_{LIM}	Output current limit			1.55	2.3	A
I_{SC}	Short-circuit current	$V_{OUT} = 0\text{ V}$	134		186	mA
e_N	Output noise voltage			10		μVrms
T_{TSD}	Thermal shutdown			165		$^\circ\text{C}$
CE	Enable input logic low	$V_{IN} = 1.32\text{ V to }5.5\text{ V}$			0.4	V
	Enable input logic high	$V_{IN} = 1.32\text{ V to }5.5\text{ V}$	1			
LCON	LCON input logic low	$V_{IN} = 1.32\text{ V to }5.5\text{ V}$			0.4	V
	LCON input logic low	$V_{IN} = 1.32\text{ V to }5.5\text{ V}$	1			

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ELECTRICAL CHARACTERISTICS (continued)


Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PSRR	Power Supply Rejection Ratio	$V_{IN} = V_{OUT} + 1V \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2V @ I_{OUT} = 1mA$	$V_{RIPPLE} \text{ Freq} = 1KHz$	84.1	96.4	dB
			$V_{RIPPLE} \text{ Freq} = 5KHz$	80.3	85.8	
			$V_{RIPPLE} \text{ Freq} = 10KHz$	78.4	84.2	
			$V_{RIPPLE} \text{ Freq} = 100KHz$	38.6	40.3	
			$V_{RIPPLE} \text{ Freq} = 1MHz$	35.1	35.4	
			$V_{RIPPLE} \text{ Freq} = 10MHz$	24.5	25.9	
		$V_{IN} = V_{OUT} + 1V \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2V @ I_{OUT} = 10mA$	$V_{RIPPLE} \text{ Freq} = 1KHz$	84.1	98.5	dB
			$V_{RIPPLE} \text{ Freq} = 5KHz$	83.5	94.5	
			$V_{RIPPLE} \text{ Freq} = 10KHz$	90.1	91.9	
			$V_{RIPPLE} \text{ Freq} = 100KHz$	44.0	45.8	
			$V_{RIPPLE} \text{ Freq} = 1MHz$	32.6	32.7	
			$V_{RIPPLE} \text{ Freq} = 10MHz$	28.7	30.3	
		$V_{IN} = V_{OUT} + 1V \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2V @ I_{OUT} = 30mA$	$V_{RIPPLE} \text{ Freq} = 1KHz$	83.7	96.6	dB
			$V_{RIPPLE} \text{ Freq} = 5KHz$	83.8	91.8	
			$V_{RIPPLE} \text{ Freq} = 10KHz$	91.3	104	
			$V_{RIPPLE} \text{ Freq} = 100KHz$	44.5	46.5	
			$V_{RIPPLE} \text{ Freq} = 1MHz$	26.3	26.8	
			$V_{RIPPLE} \text{ Freq} = 10MHz$	26.0	28.5	
		$V_{IN} = V_{OUT} + 1V \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2V @ I_{OUT} = 150mA$	$V_{RIPPLE} \text{ Freq} = 1KHz$	84.5	94.4	dB
			$V_{RIPPLE} \text{ Freq} = 5KHz$	80.6	84.4	
			$V_{RIPPLE} \text{ Freq} = 10KHz$	78.7	81.4	
			$V_{RIPPLE} \text{ Freq} = 100KHz$	43.7	45.2	
			$V_{RIPPLE} \text{ Freq} = 1MHz$	21.2	22.8	
			$V_{RIPPLE} \text{ Freq} = 10MHz$	27.8	28.9	

*This is ASPL8801-330-TH measurement data. Other PSRR information please contact Gutschsemi.

Load Regulation (Dynamic)



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ΔV_1	Undershoot Voltage	$I_{LOAD}=1mA\sim 250mA$		30		mV
		$I_{LOAD}=1mA\sim 500mA$		40		
		$I_{LOAD}=1mA\sim 1A$		62		
		$I_{LOAD}=0mA\sim 300mA$		50		
		$I_{LOAD}=0mA\sim 1A$		90		
ΔV_2	Overshoot Voltage	$I_{LOAD}=1mA\sim 250mA$		28		mV
		$I_{LOAD}=1mA\sim 500mA$		40		
		$I_{LOAD}=1mA\sim 1A$		60		
		$I_{LOAD}=0mA\sim 300mA$		35		
		$I_{LOAD}=0mA\sim 1A$		65		

Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Δt_1	Transient recovery time	$I_{LOAD}=1mA\sim 250mA$		10		μS
		$I_{LOAD}=1mA\sim 500mA$		16		
		$I_{LOAD}=1mA\sim 1A$		18		
		$I_{LOAD}=0mA\sim 300mA$		60		
		$I_{LOAD}=0mA\sim 1A$		80		
Δt_2	Transient recovery time	$I_{LOAD}=1mA\sim 250mA$		12		μS
		$I_{LOAD}=1mA\sim 500mA$		12		
		$I_{LOAD}=1mA\sim 1A$		16		
		$I_{LOAD}=0mA\sim 300mA$		90		
		$I_{LOAD}=0mA\sim 1A$		300		

*This table is ASPL8801-330-TH measurement data. For detail load regulation information about other ASPL8801 series LDOs, please contact Gutschsemi R&D team.

FUNCTION DESCRIPTION

A. Short-Circuit Protect and Current Limitation

ASPL8801 series LDOs can protect internal circuit under short-circuit condition on the output. When the load current increases above 1.55 A, the current limit and current foldback mechanism starts to restrict the I_{LIM} value. If the load resistance decreases even more then the foldback, circuit starts limiting the current to 0.2 A when $V_{OUT} = 0$.

B. Over Temperature Protection and Auto Recover

In order to prevent over thermal condition from damaging the device, ASPL8801 series LDOs have internal thermal limiting functions designed to protect the device. It will rapidly shut off PMOS pass element during over temperature condition.

C. Current Foldback

The current limiting/ current foldback circuit plays an important role by controlling any excessive output current. Our ASPL8801 series LDOs provide a current foldback circuit that can detect accurately when an over-current condition occurs.

D. Very Fast Transient Response

In addition to the main feedback loop, ASPL8801 series LDOs contain a fast-transient loop that allows the LDO to respond faster to large-output transients. ASPL8801 series LDOs that contain this loop are better able to minimize the effects of a load transient even the output capacitance is small. The recommended output capacitance value is 1 μ F. It's small size greatly reduce the cost and save PCB area.

E. Ultra High PSRR and Extreme Low Noise

Gutshsemi's ASPL8801 series high-performance LDO regulators feature remarkable power supply rejection ratio characteristics (up to 104 dB at 10 kHz) and extreme-low noise operation (as low as 6.3 μ VRMS with A-wt) resulting in cleaner and stable output voltages. Our LDO is very suitable for ultra-sensitive loads like camera module and security monitor, especially in low light condition.

F. Start-Up at Full Load

ASPL8801 series LDOs can start-up at full load, make it very suitable for heavy load start up condition and severe system timing constraint.

G. Auto Discharge Function

ASPL8801 series LDOs have an auto discharge function to quickly force the output voltage to zero. When the LDO is disabled, the auto discharge function quickly discharge the output capacitor, thereby reducing the output voltage to nearly zero. This function is very useful for quickly ON/OFF application.

H. Low Quiescent Current

ASPL8801 series LDOs consume only 85 μ A (typical) while operating with no load condition. By reducing the quiescent current, your application can stay in standby/sleep mode much longer than leading low quiescent current LDOs in the market.

I. Under Voltage Lock OUT (UVLO)

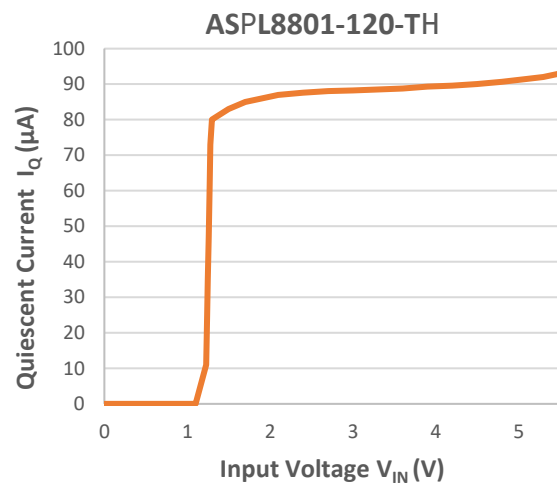
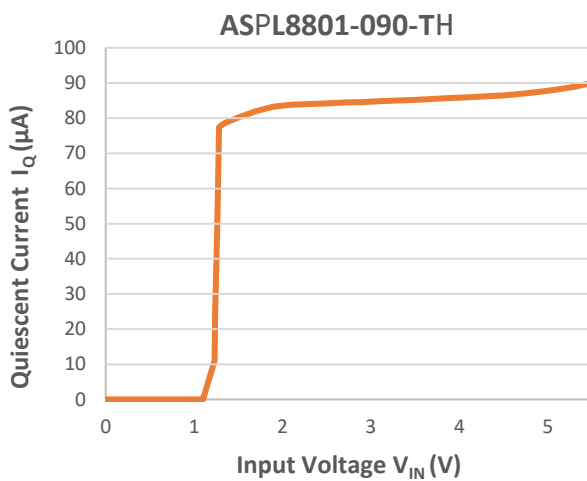
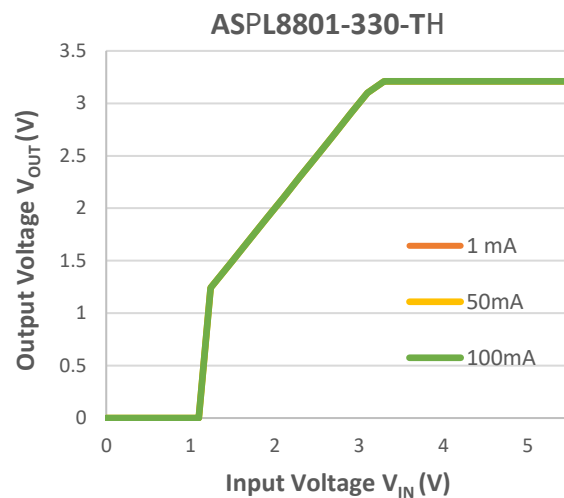
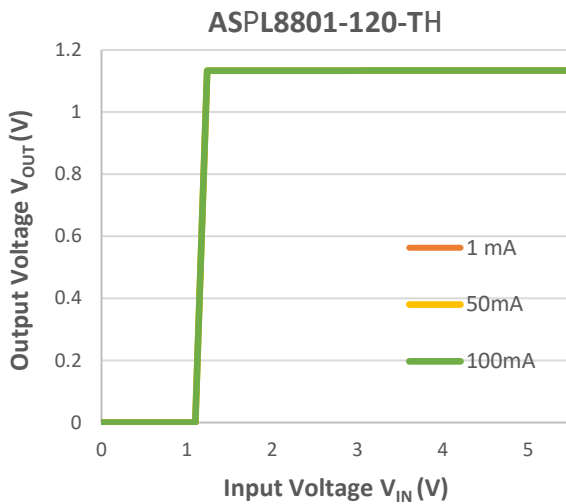
ASPL8801 has an undervoltage lockout (UVLO) function to make sure that whole circuit does nothing until the power supply voltage is high enough. When power supply voltage is high enough, reference circuit can generate right voltage ; logic function can generate correct control signals. This UVLO function can guarantee robust system performance.

Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

TYPICAL CHARACTERISTICS

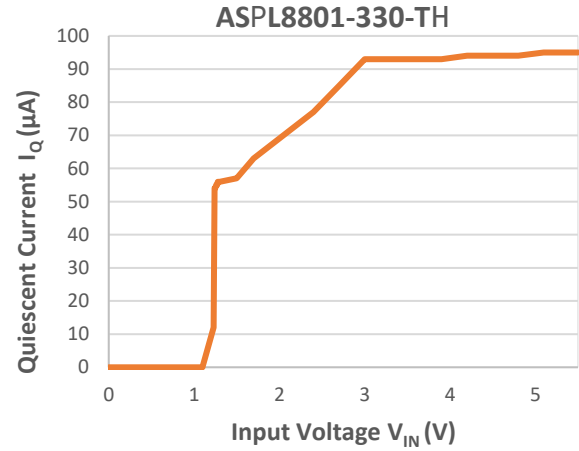
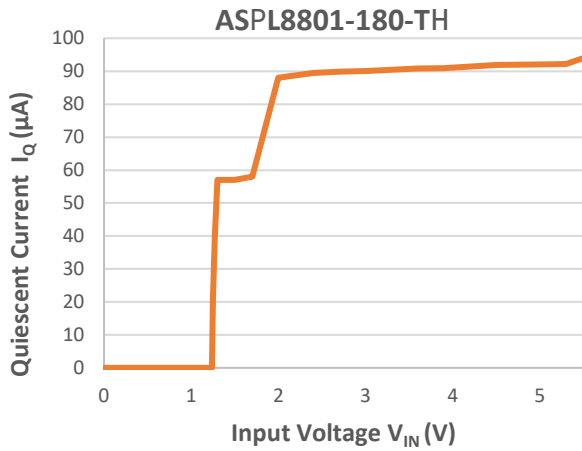
$V_{IN} = V_{SET}^{(1)} + 1.0\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = C_{OUT} = 1.0\text{ }\mu\text{F}$, LCON='H', typical values are at $T_J = 25\text{ }^\circ\text{C}$; min./max. values are at $-40\text{ }^\circ\text{C} \leq T_J \leq 125\text{ }^\circ\text{C}$, unless otherwise noted.

Output Voltage vs. Input Voltage ($C_{IN} = C_{OUT} = 1.0\text{ }\mu\text{F}$, $T_a = 25\text{ }^\circ\text{C}$)

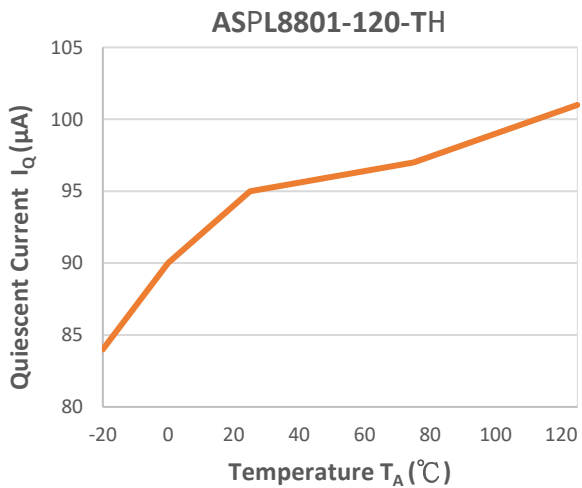




Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO



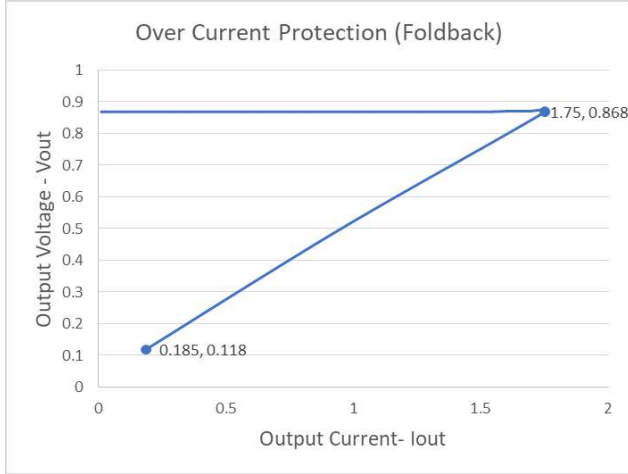
Supply Current vs. Temperature ($C_{IN} = C_{OUT} = 1.0\mu F$, $I_{OUT} = 0\text{ mA}$)



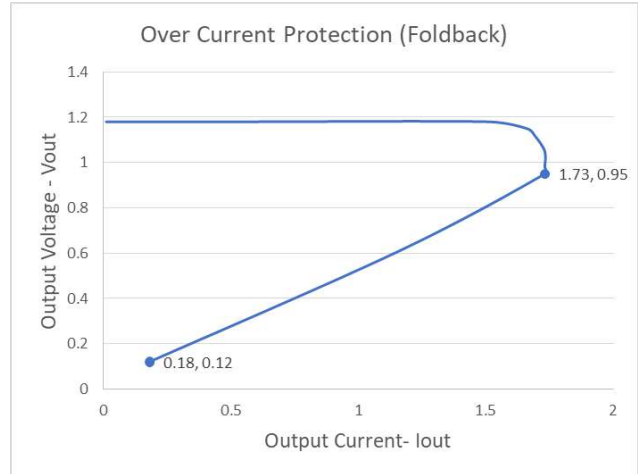
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

Over Current Protect Foldback Characteristic (LCON = V_{IN}, C_{IN} = C_{OUT} = 1.0 μ F, Ta = 25°C)

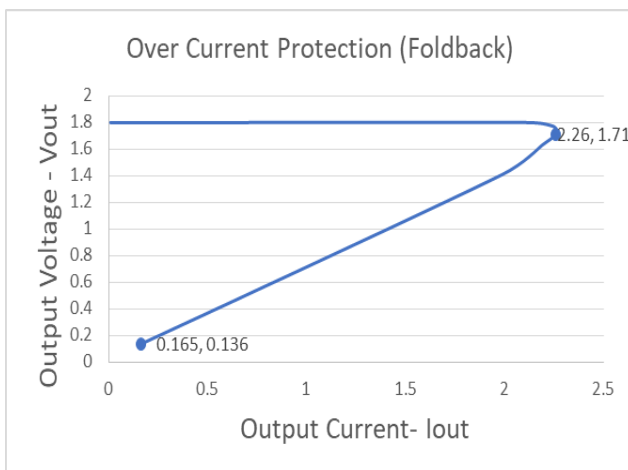
ASPL8801-090-TH



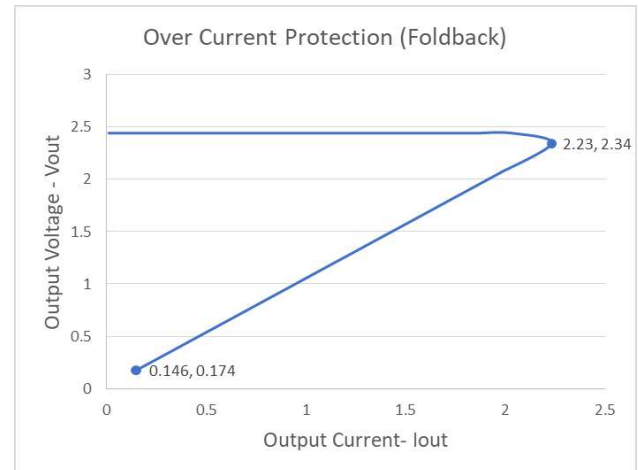
ASPL8801-120-TH



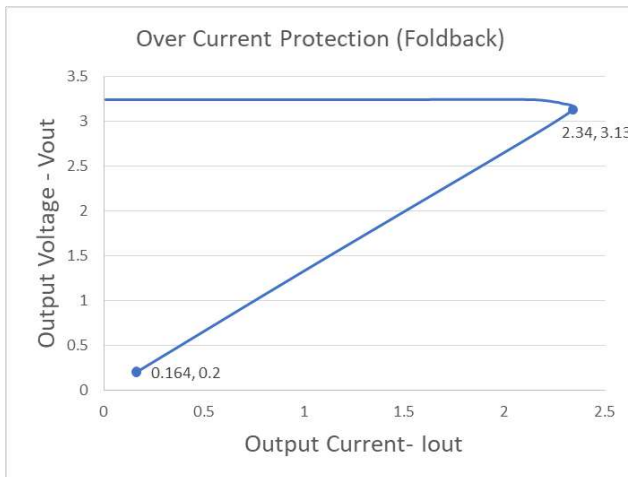
ASPL8801-180-TH



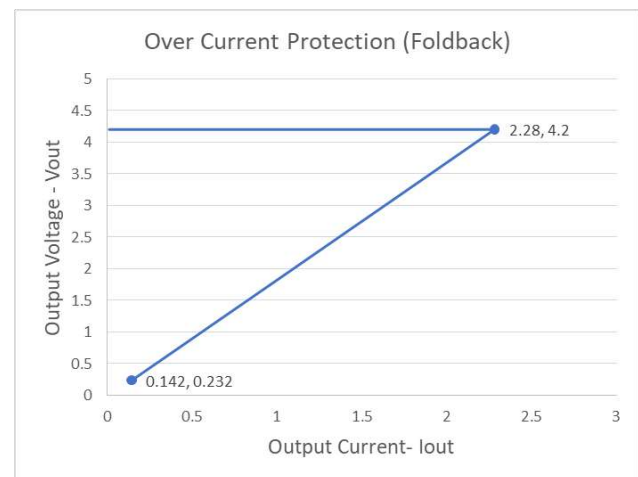
ASPL8801-250-TH



ASPL8801-330-TH



ASPL8801-430-TH

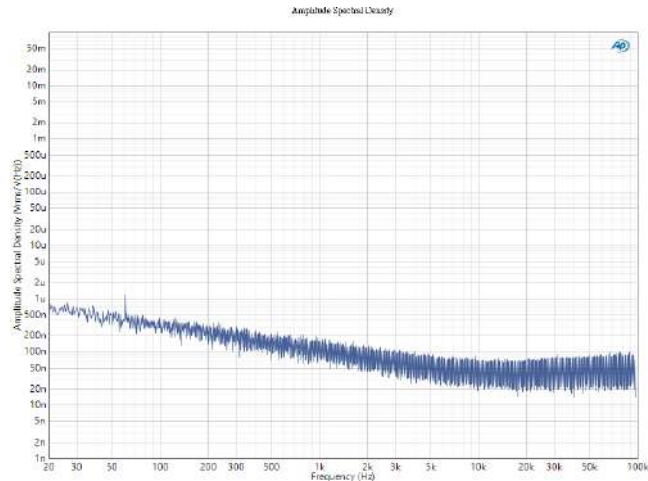


Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

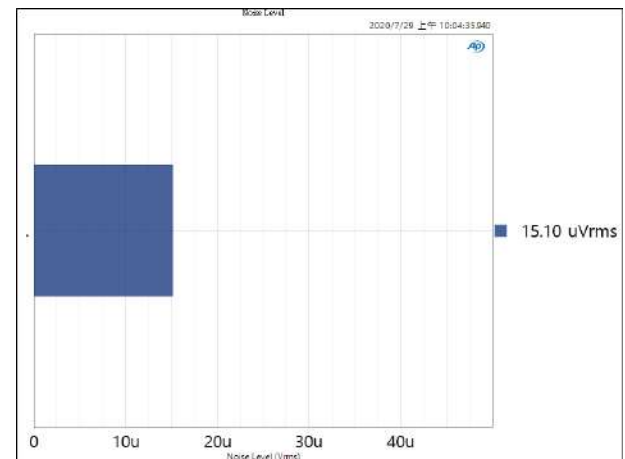
Output Noise Voltage (10 Hz to 100 kHz, $C_{IN} = C_{OUT} = 1.0 \mu F$, $T_a = 25^\circ C$)

ASPL8801-090-TH, $I_{OUT} = 100 \text{ mA}$

Amplitude Spectral Density

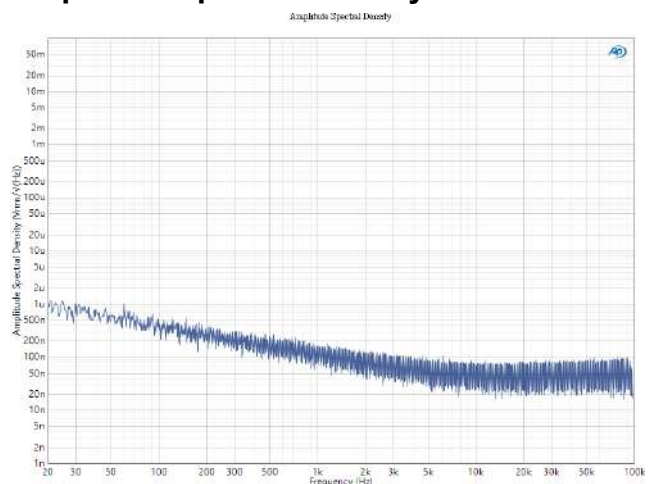


V_{RMS} from 10 Hz to 100 kHz

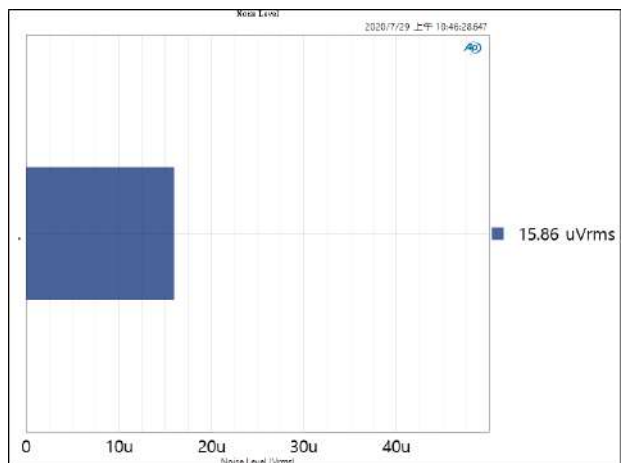


ASPL8801-120-TH, $I_{OUT} = 100 \text{ mA}$

Amplitude Spectral Density



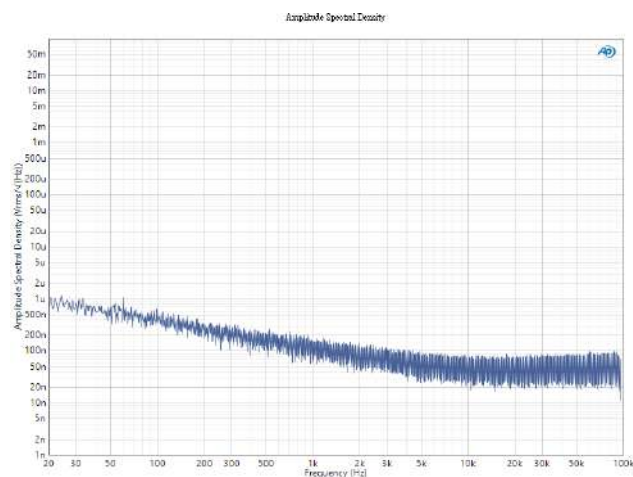
V_{RMS} from 10 Hz to 100 kHz



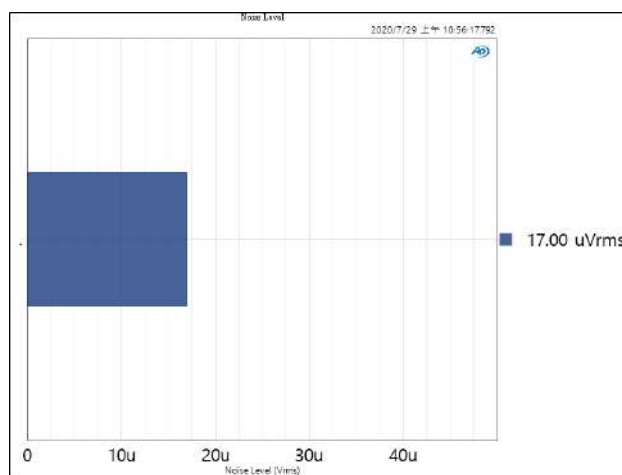
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

ASPL8801-330-TH, $I_{OUT} = 100\text{ mA}$

Amplitude Spectral Density



V_{RMS} from 10 Hz to 100 kHz



Power Supply Ripple Rejection vs. Frequency ($V_{IN}=V_{OUT}+1V$, $C_{IN} = C_{OUT} = 1.0 \mu F$, Ripple = 0.2 Vp-p, $T_a = 25^\circ C$)

ASPL8801-090-TH

[illegible]

1 Active Ch/Trace 2 Response 3 Stimulus 4 Me/Analysis 5 Instr State

1/2 1/8 Log Mag 20.00 dB/ ref 40.00 dB [RT]

1	2	3	4	5	6
1	3.0000000	kHz	80.372	dB	
2	5.0000000	kHz	92.135	dB	
3	10.000000	kHz	92.413	dB	
4	100.00000	kHz	41.642	dB	
5	1.0000000	MHz	29.277	dB	
6	10.000000	MHz	22.327	dB	

140.0

120.0

100.0

80.00

60.00

40.00

20.00

0.000

-20.00

-40.00

-60.00

1 Start 10 Hz

F [Hz]

Step 16 MHz

Keysight Network Analyzer

1 Active Ch/Trace 2 Response 3 Stimulus 4 Mkr/Analysis 5 Instr State

1 2 3 4 5 6

1	2	3	4	5	6
1	1.0000000	kHz	79.940	dB	
2	3.0000000	kHz	81.519	dB	
3	10.000000	kHz	91.025	dB	
4	100.00000	kHz	42.432	dB	
5	1.0000000	MHz	25.127	dB	
6	10.000000	MHz	23.901	dB	

Log Mag 20.00 dB/ Ref 40.00 dB [RT]

140.00

120.00

100.00

80.00

60.00

40.00

20.00

0.000

-20.00

-40.00

-60.00

Span 10 Hz

1000.0 Hz

Span 16 MHz

E5051B Network Analyser

1 Active Ch/Trace 2 Response 3 Stimulus 4 Mts/Analysis 5 Into State

7/8 Log Mag 20.00 dB/ ref 40.00 dB [RT]

1	1.000000	MHz	80.796	dB
2	5.000000	MHz	78.308	dB
3	10.000000	MHz	78.064	dB
4	100.00000	MHz	41.912	dB
5	1.000000	MHz	17.865	dB
>6	10.000000	MHz	22.079	dB

140.0

120.0

100.0

80.00

60.00

40.00

20.00

0.000

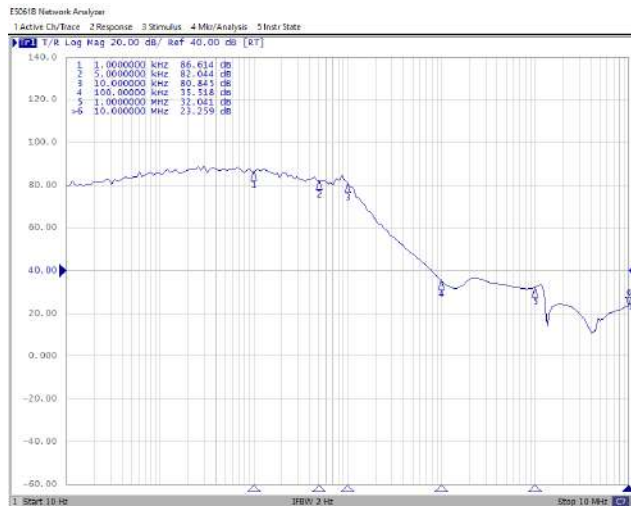
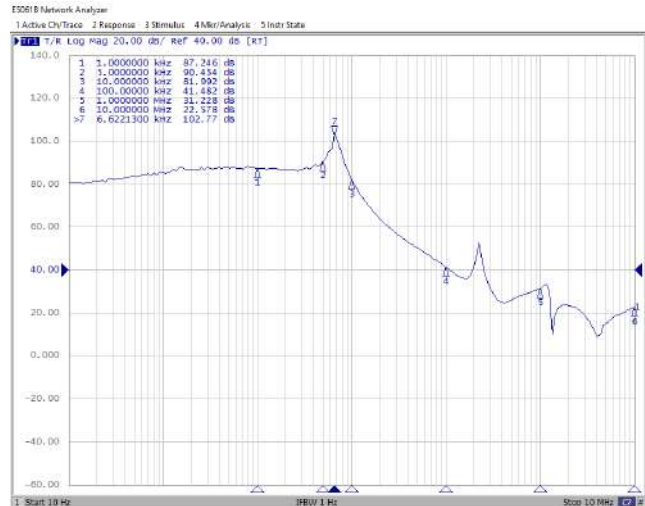
-20.00

-40.00

-60.00

1.000000 MHz 10.000000 MHz

Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

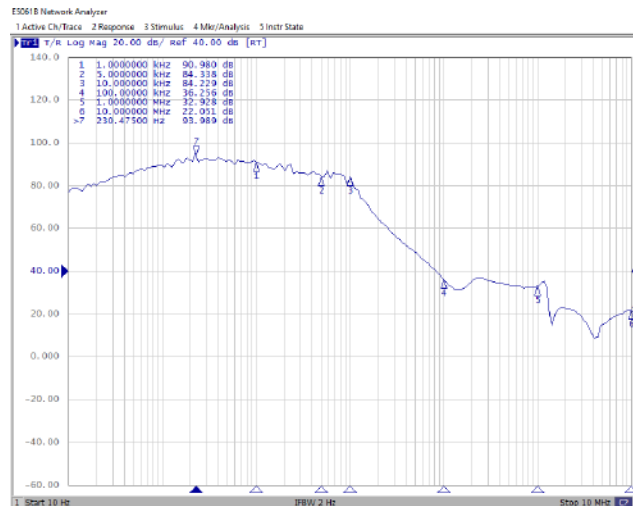
ASPL8801-120-TH
 $I_{Load}=1mA$

 $I_{Load}=10mA$

 $I_{Load}=30mA$

 $I_{Load}=150mA$

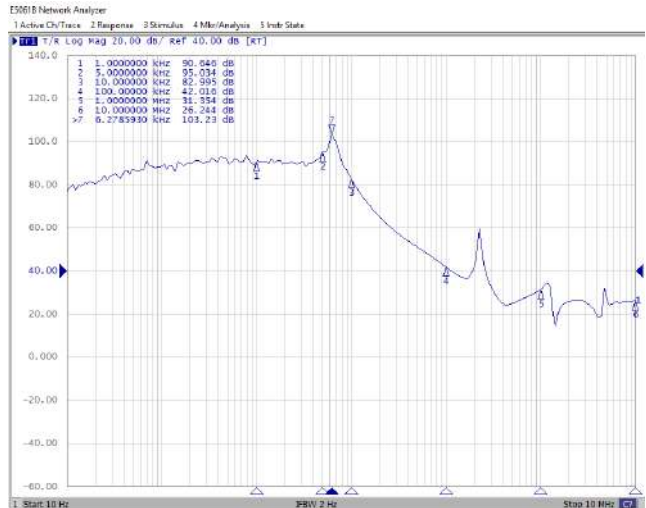

Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

ASPL8801-180-TH

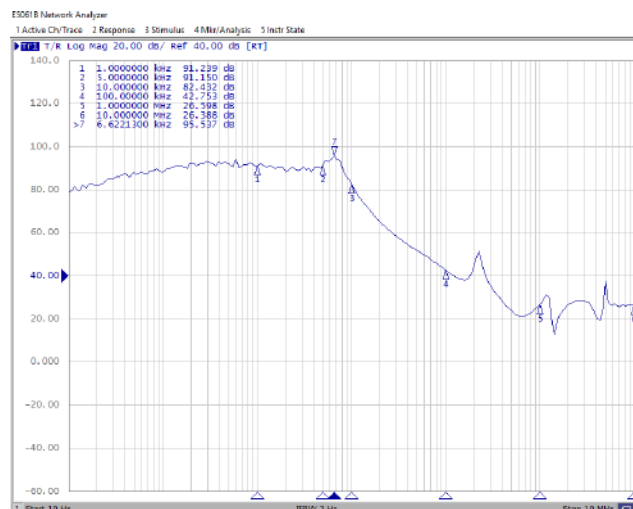
$I_{Load}=1mA$



$I_{Load}=10mA$



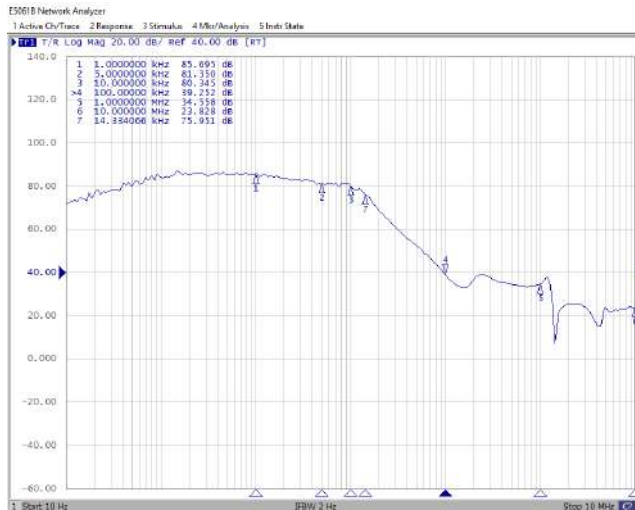
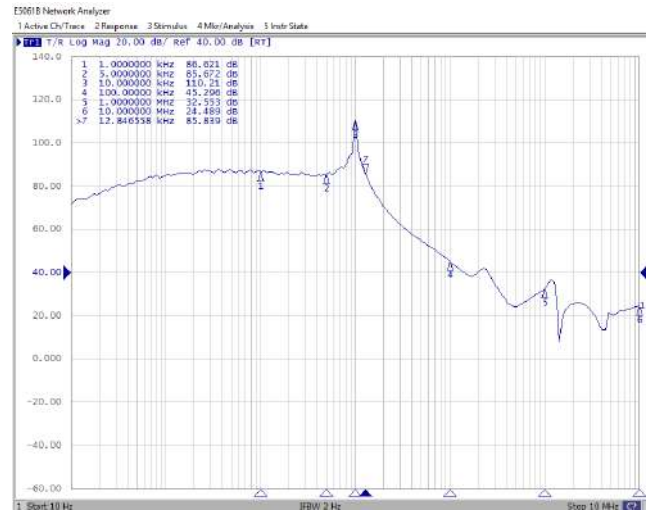
$I_{Load}=30mA$



$I_{Load}=150mA$



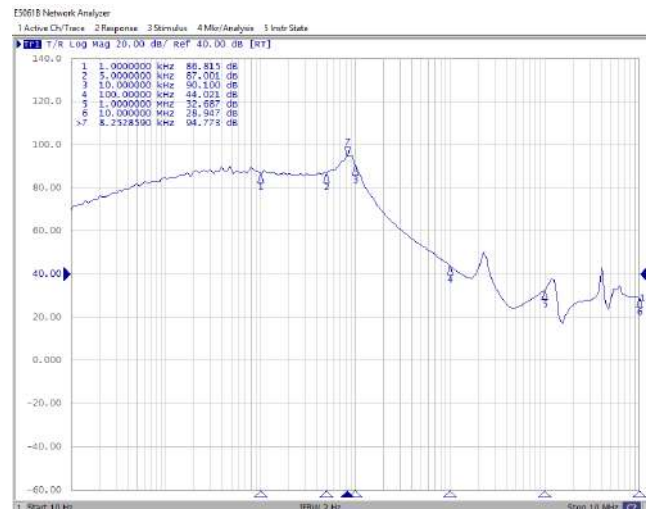
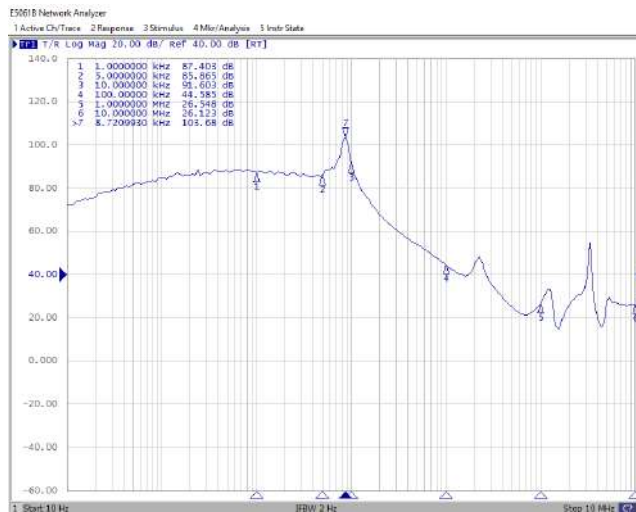
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

ASPL8801-250-TH
Load=1mA

I_{Load}=10mA

Load=30mA

I_{Load}=150mA


Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

ASPL8801-330-TH
 $I_{Load}=1mA$

 $I_{Load}=10mA$

 $I_{Load}=30mA$

 $I_{Load}=150mA$

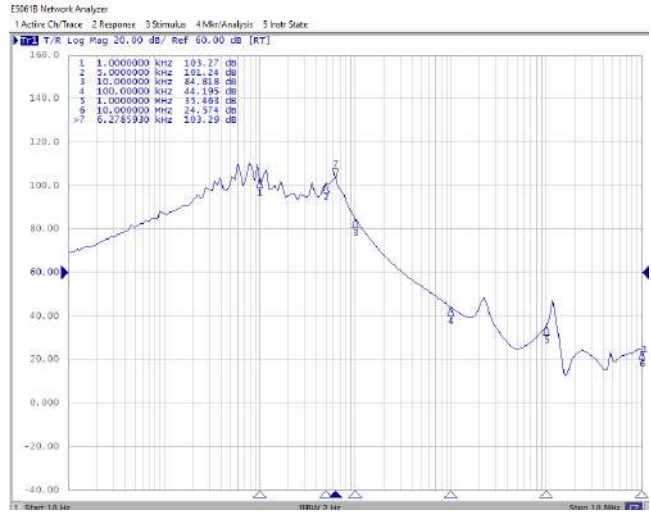

Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

ASPL8801-430-TH

Load=1mA



I_{Load}=10mA



Load=30mA



I_{Load}=150mA

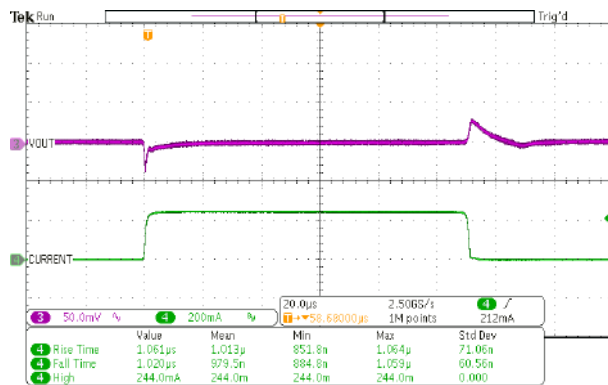


Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

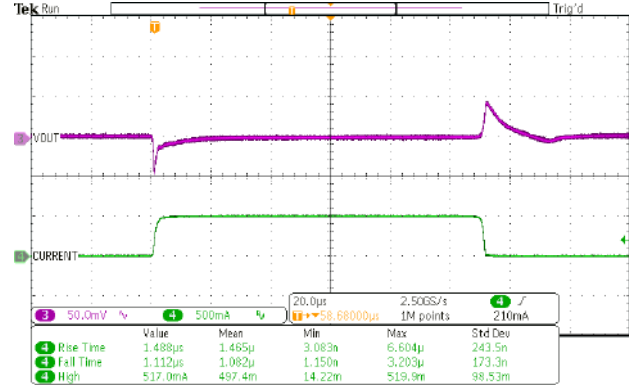
Load Transient Response ($V_{IN}=V_{OUT}+1V$, $C_{IN} = C_{OUT} = 1.0 \mu F$, $t_r = t_f = 1 \mu s$, $T_a = 25^\circ C$)

ASPL8801-090-TH

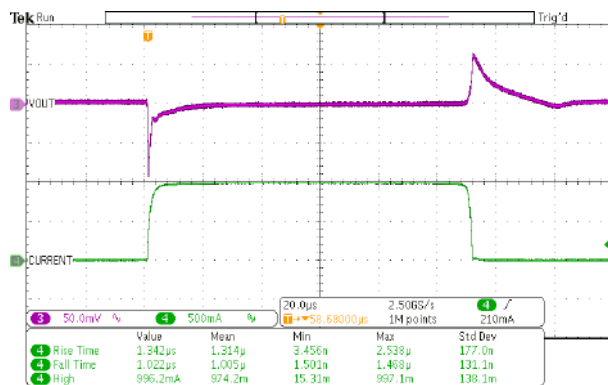
1mA -> 250mA



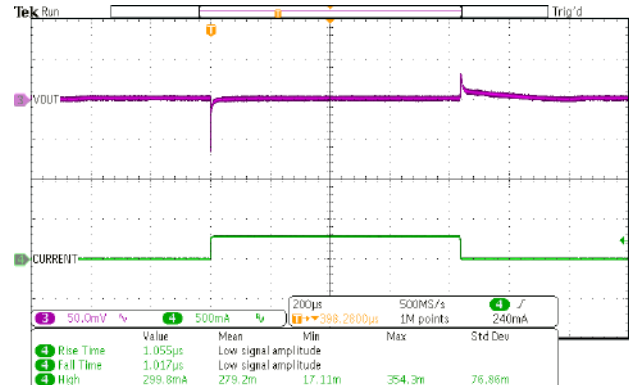
1mA -> 500mA



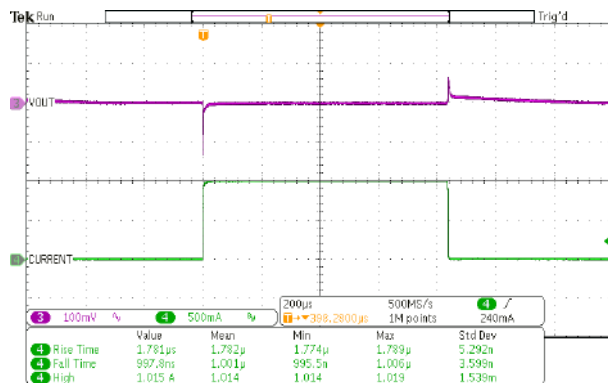
1mA -> 1000mA

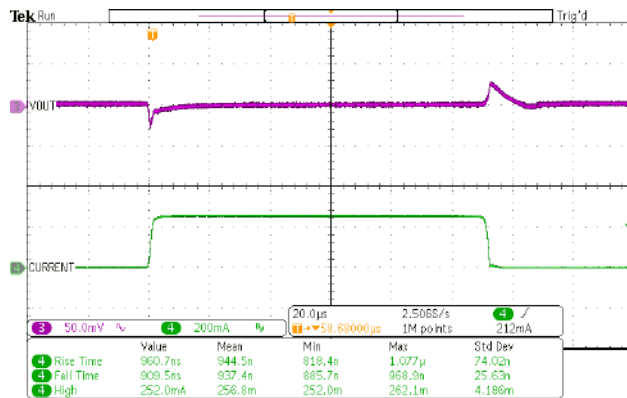
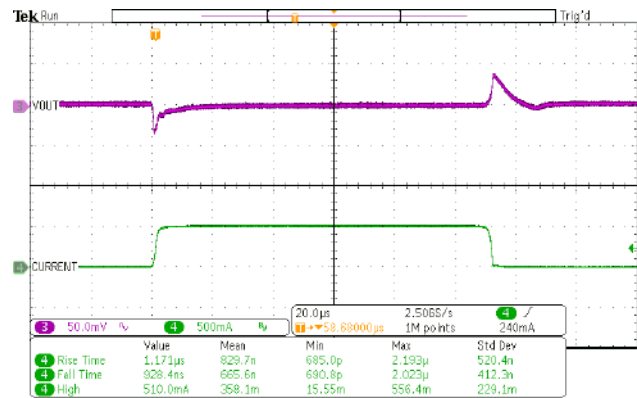
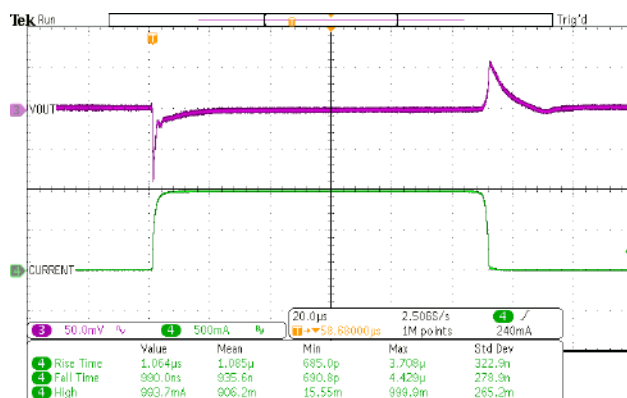
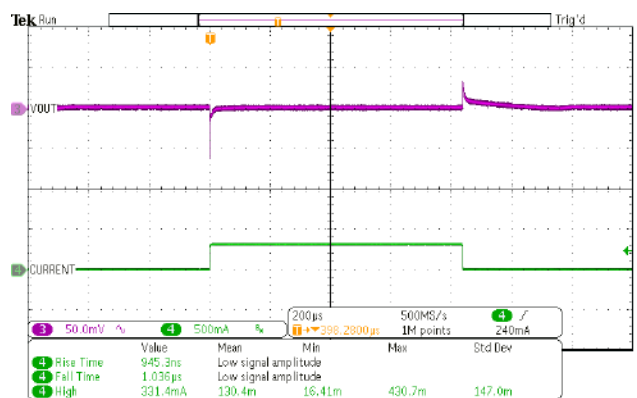
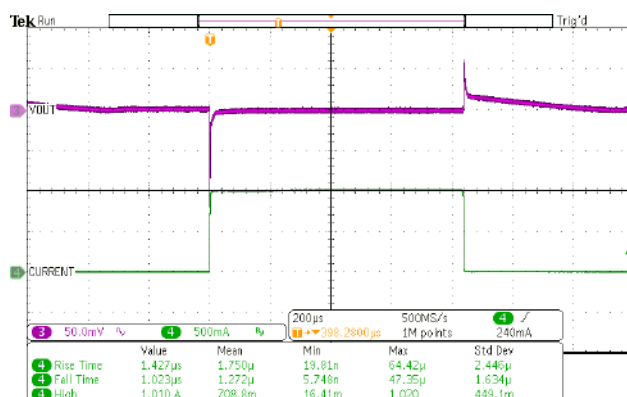


0mA -> 300mA



0mA -> 1000mA

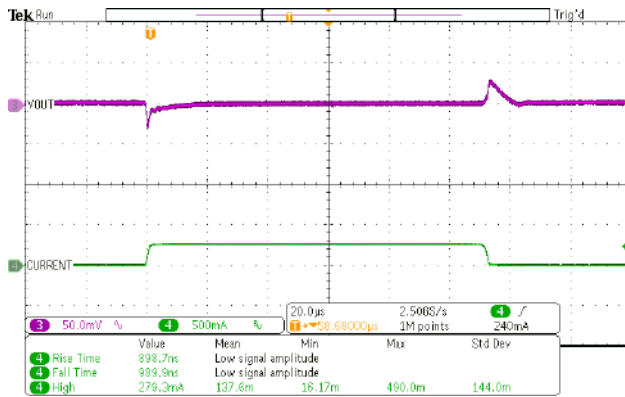


Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ASPL8801-120-TH
1mA -> 250mA

1mA -> 500mA

1mA -> 1000mA

0mA -> 300mA

0mA -> 1000mA


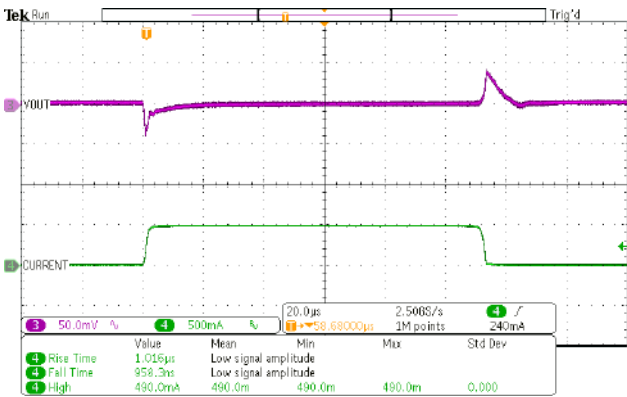
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

ASPL8801-180-TH

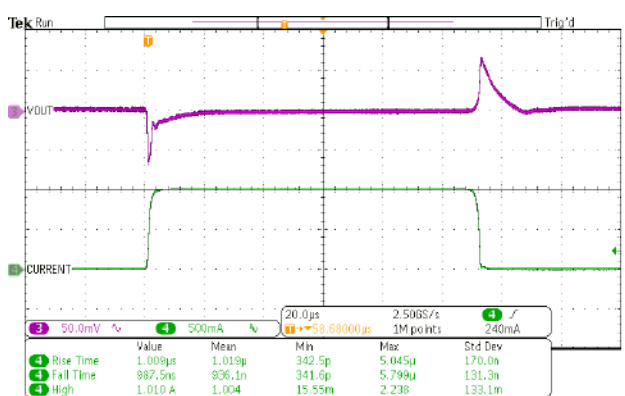
1mA -> 250mA



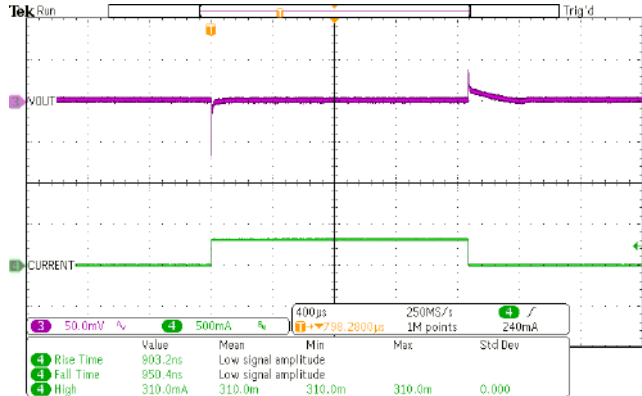
1mA -> 500mA



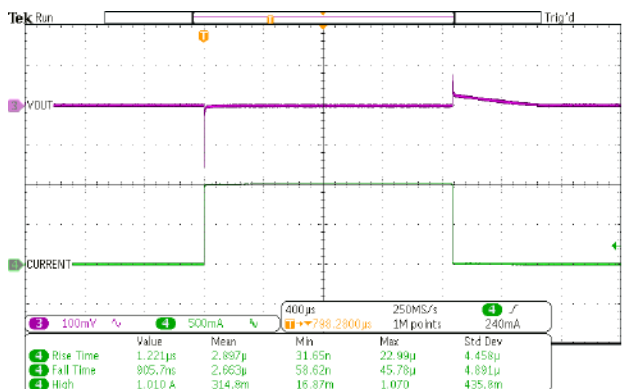
1mA -> 1000mA

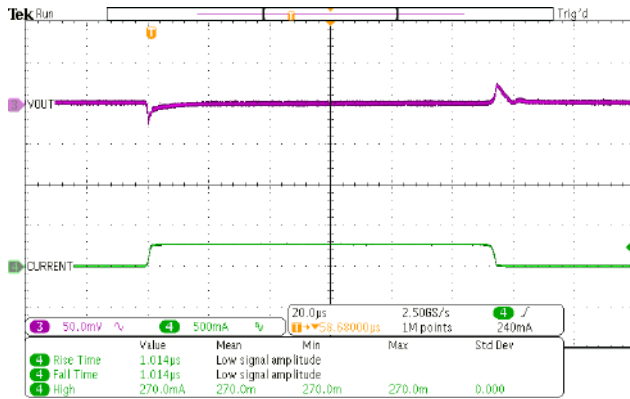
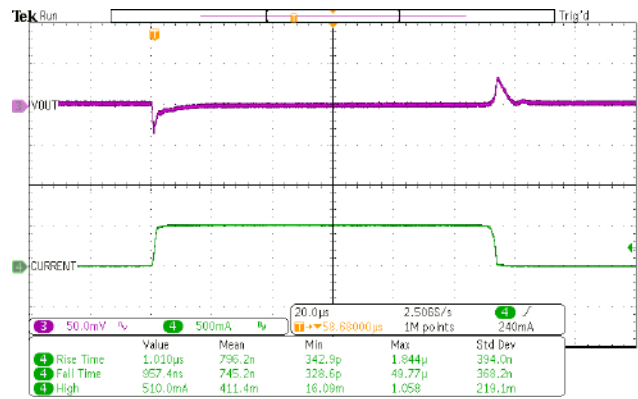
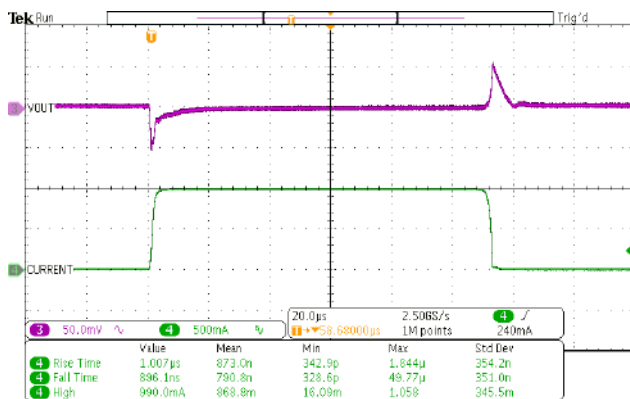
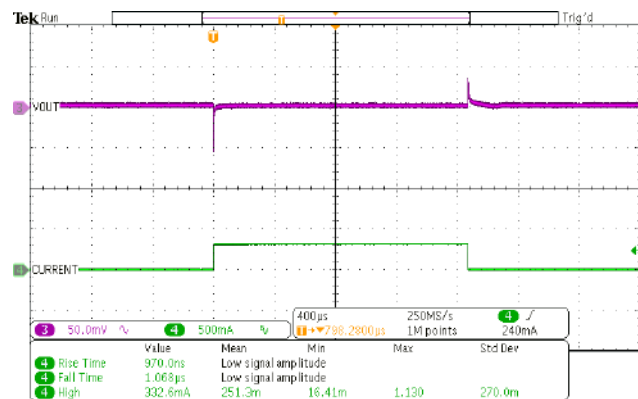
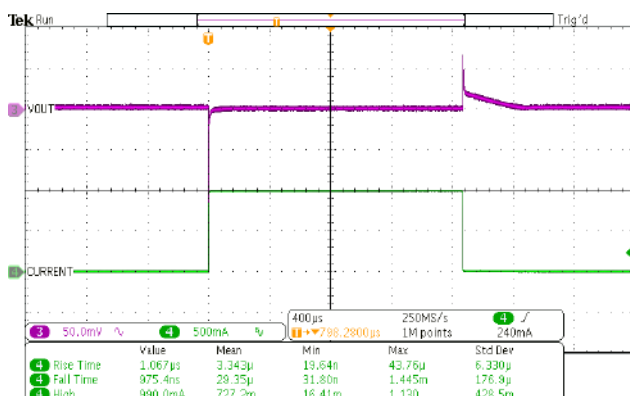


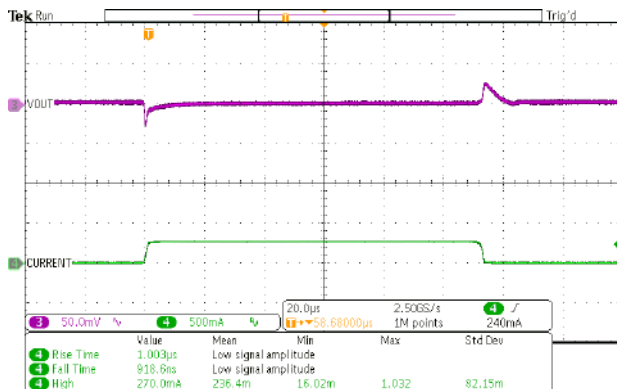
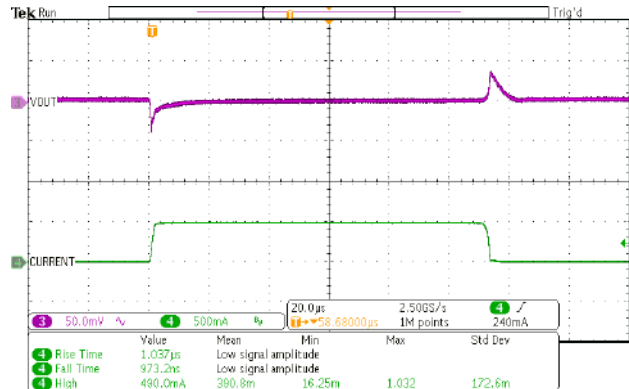
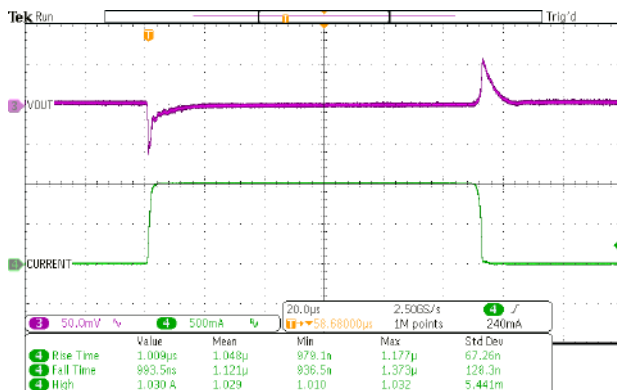
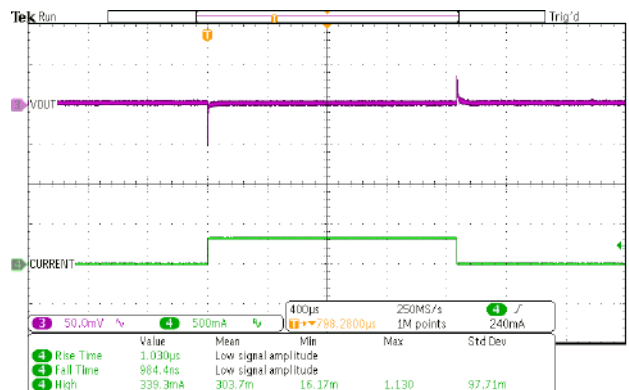
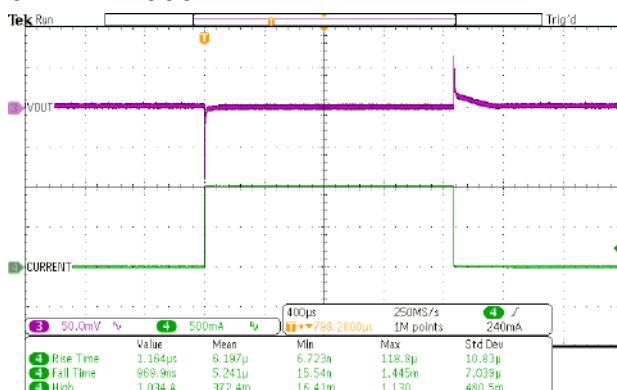
0mA -> 300mA



0mA -> 1000mA



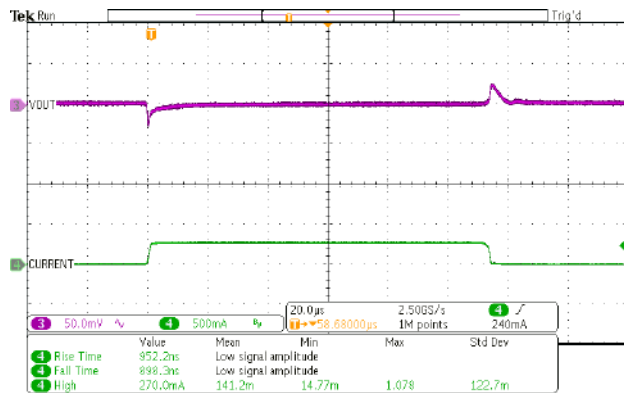
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ASPL8801-250-TH
1mA -> 250mA

1mA -> 500mA

1mA -> 1000mA

0mA -> 300mA

0mA -> 1000mA


Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ASPL8801-330-TH
1mA -> 250mA

1mA -> 500mA

1mA -> 1000mA

0mA -> 300mA

0mA -> 1000mA


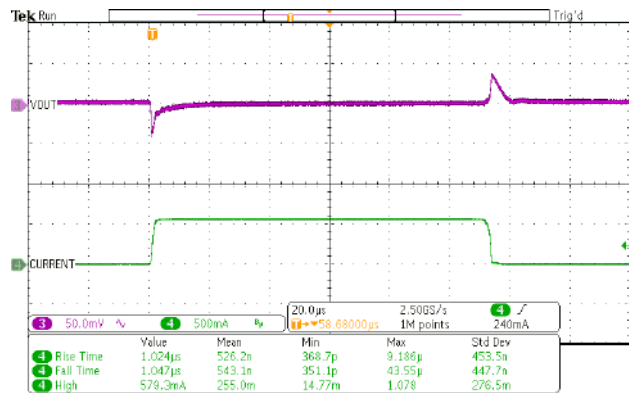
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

ASPL8801-430-TH

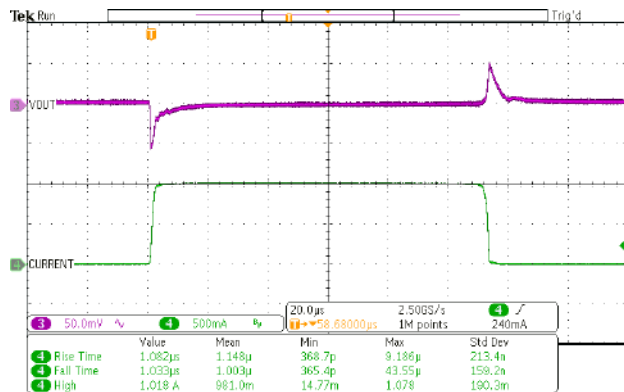
1mA -> 250mA



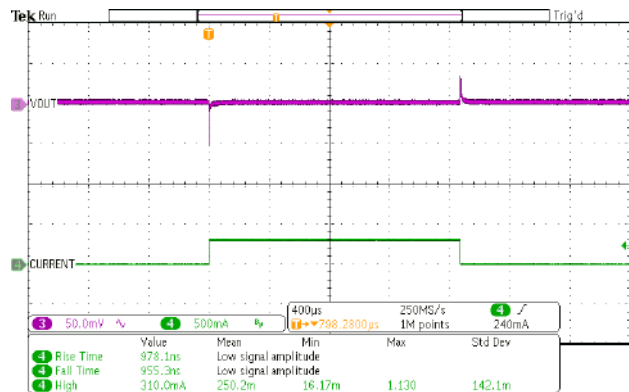
1mA -> 500mA



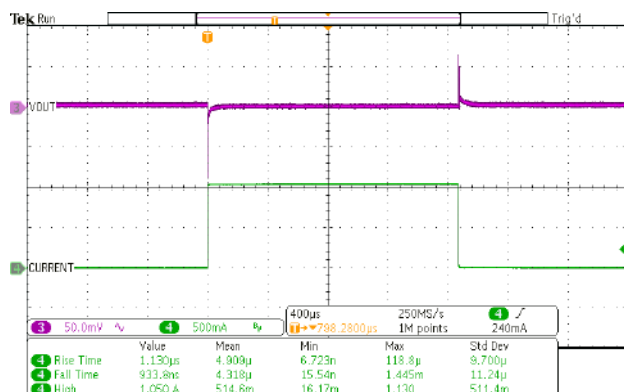
1mA -> 1000mA



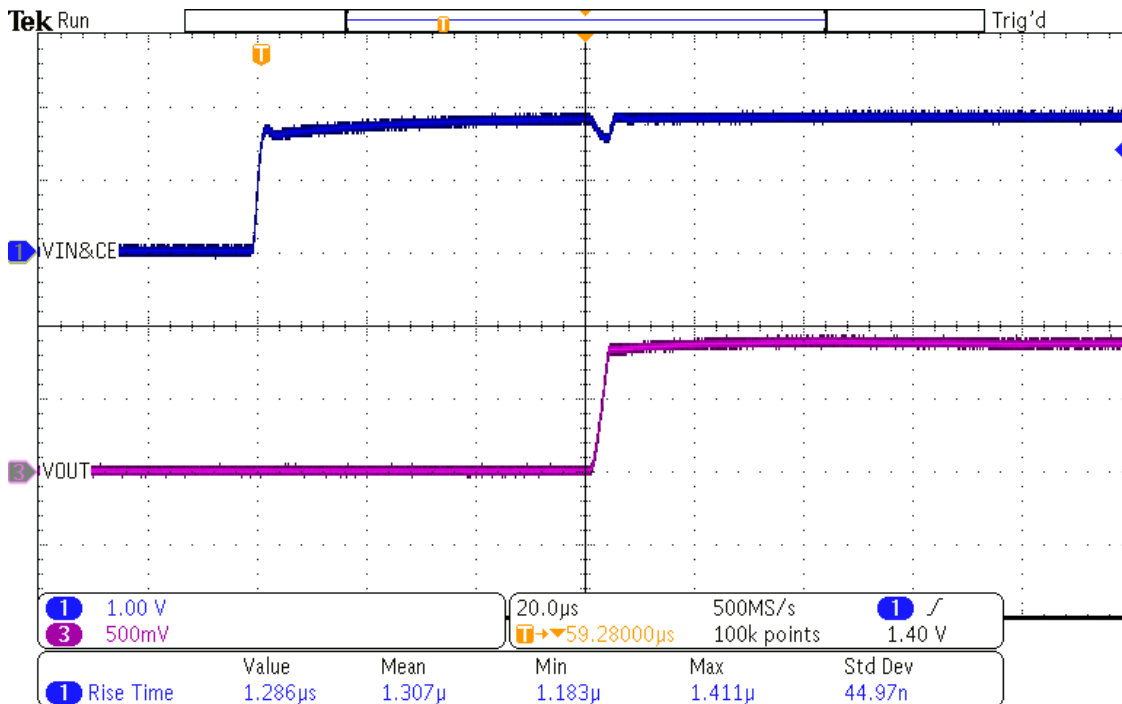
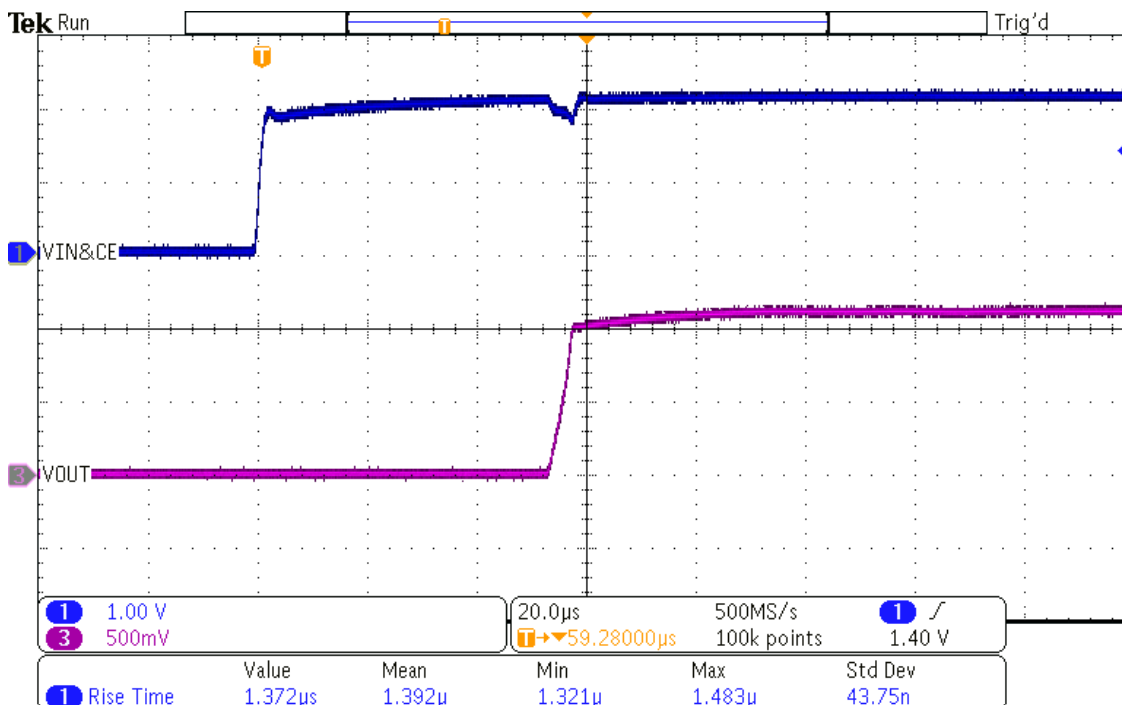
0mA -> 300mA

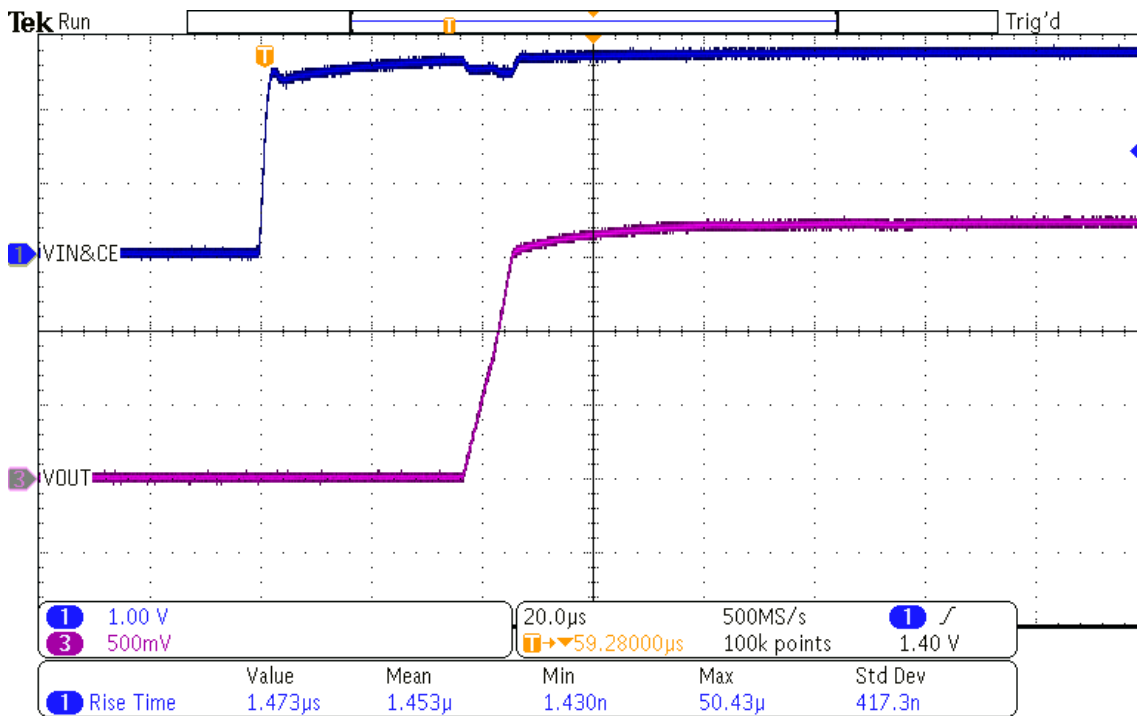
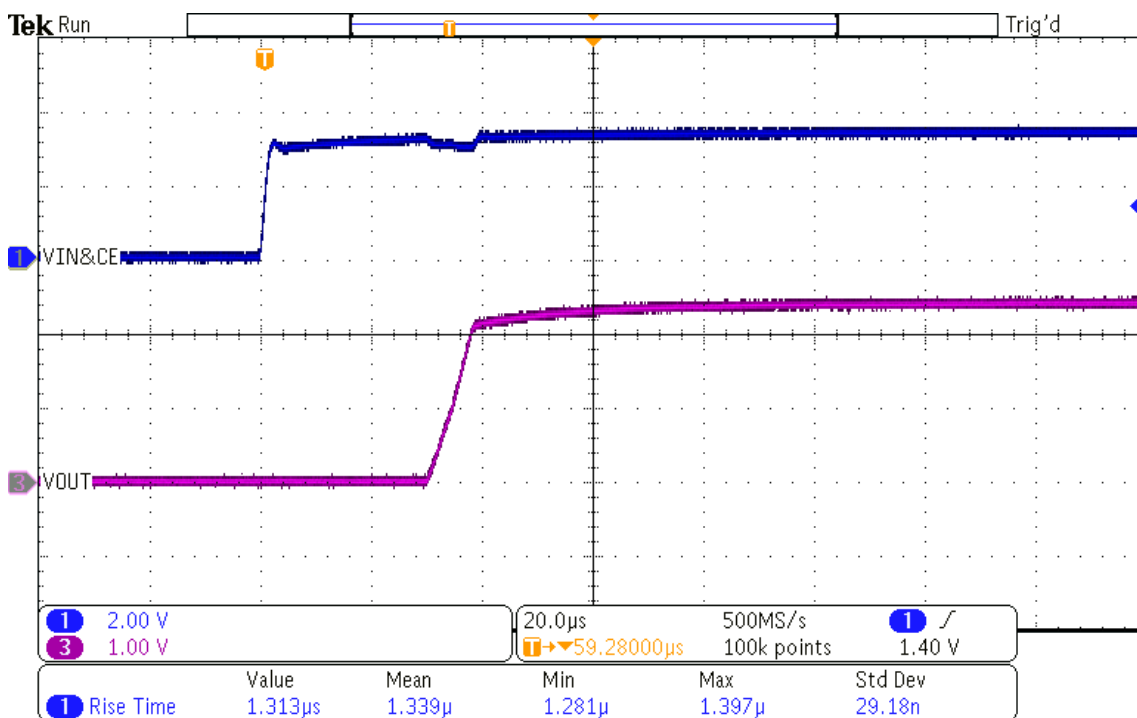


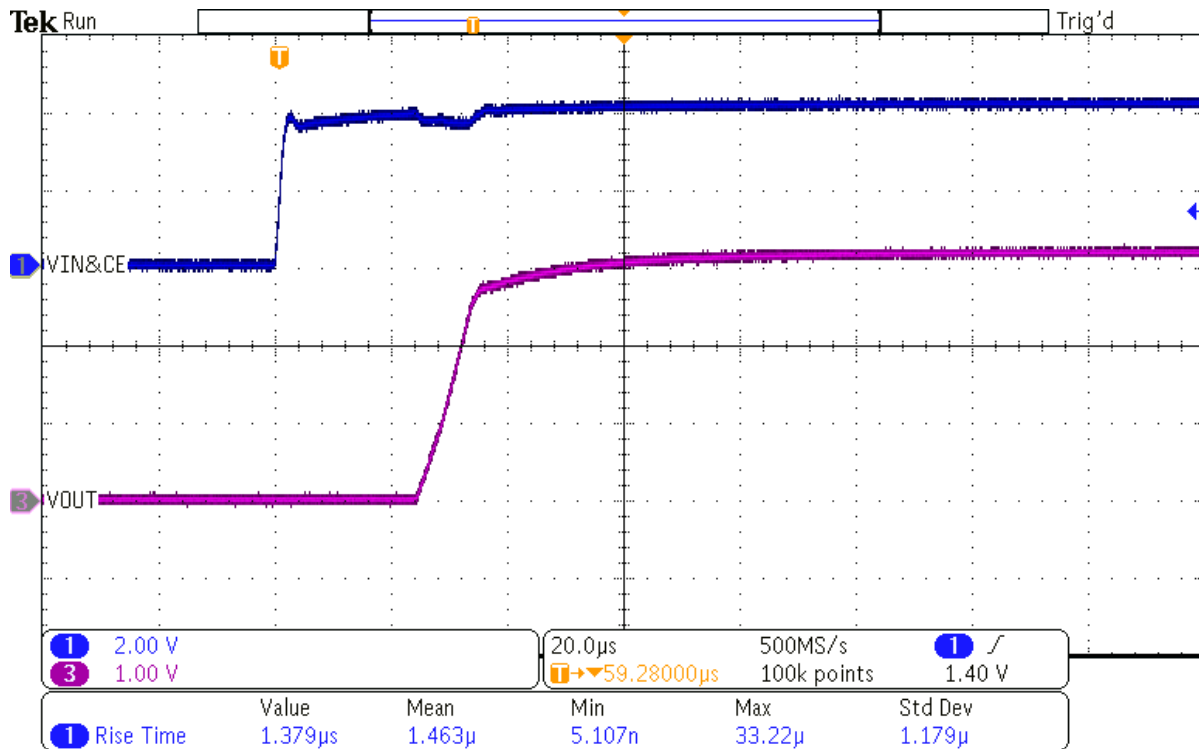
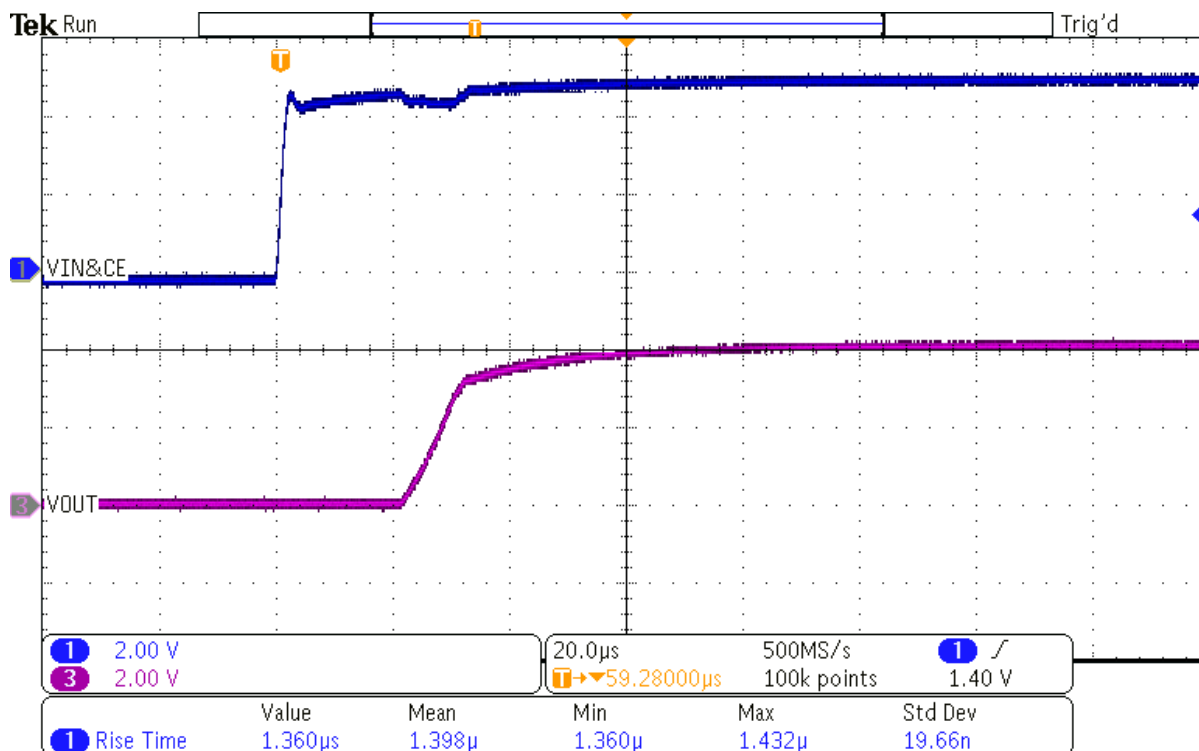
0mA -> 1000mA



Turn-on waveform by V_{IN} & CE @ light load ($V_{IN} = CE = 0$ V to $V_{OUT}+1$ V, $C_{IN} = C_{OUT} = 1.0$ μ F, $T_a = 25^\circ$ C, $I_{OUT} = 1$ mA)

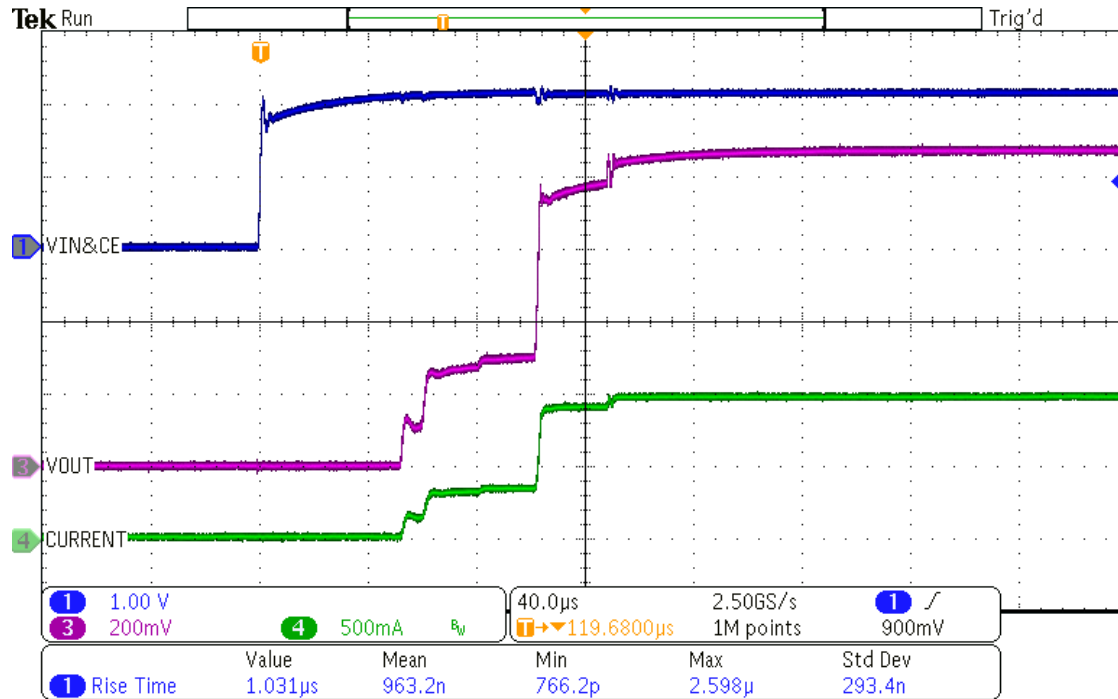
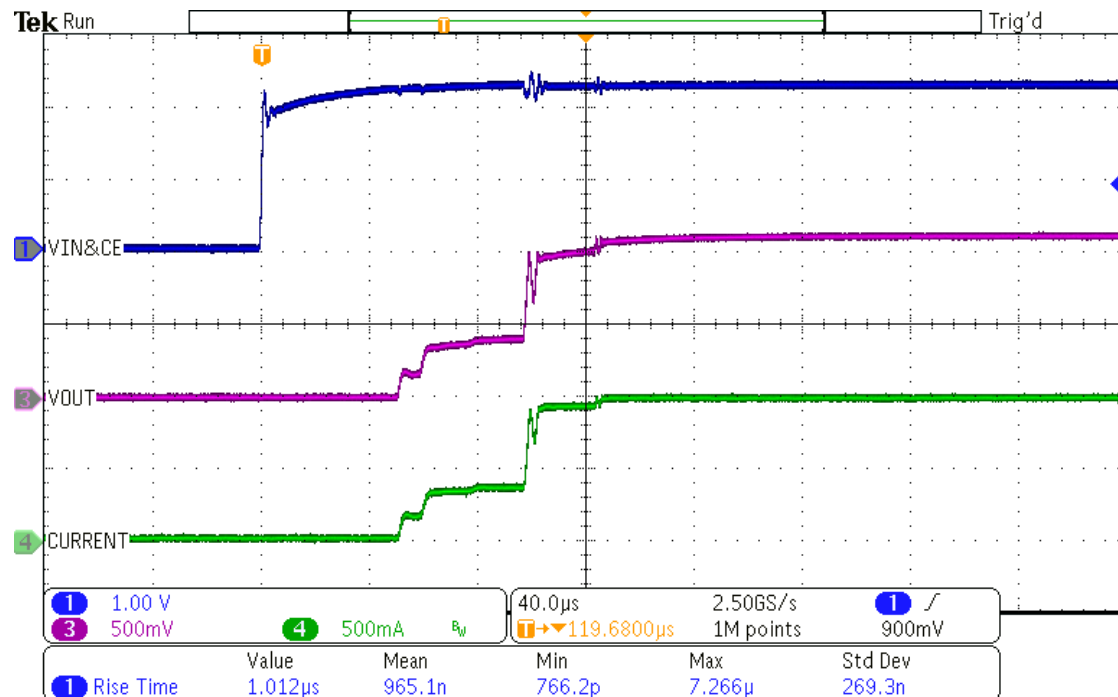
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ASPL8801-090-TH

ASPL8801-120-TH


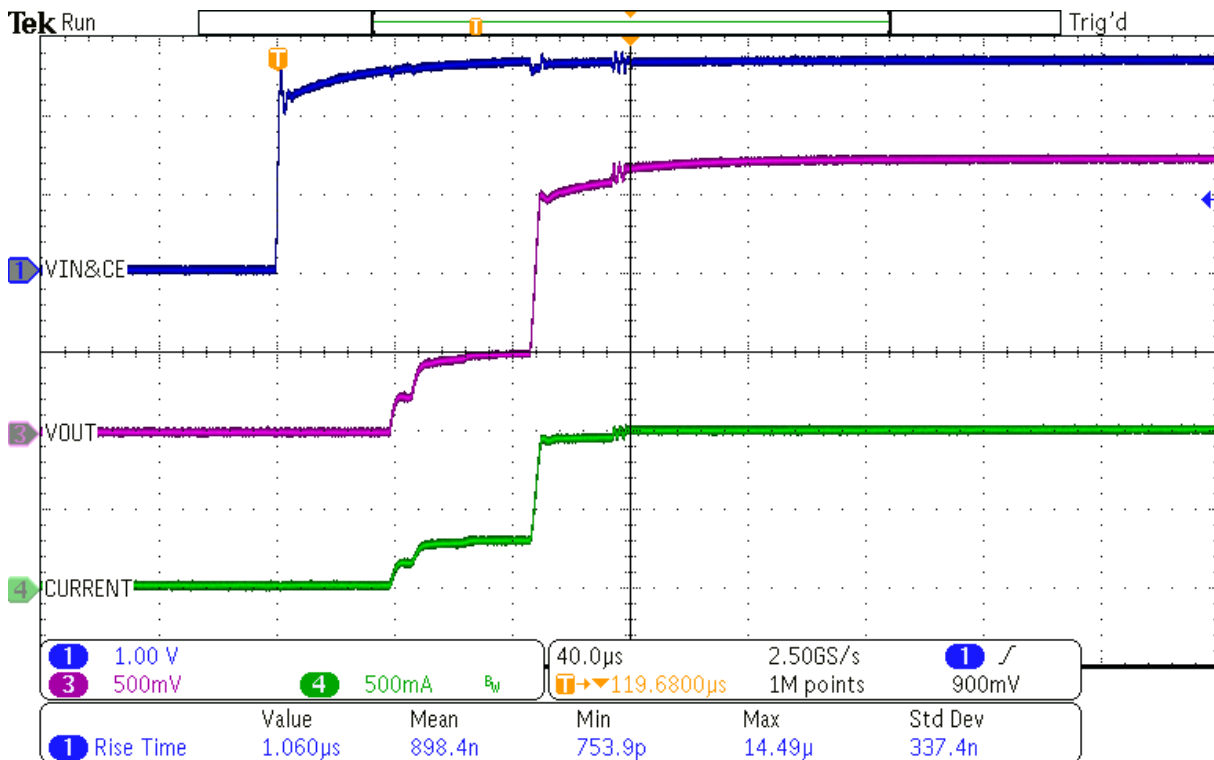
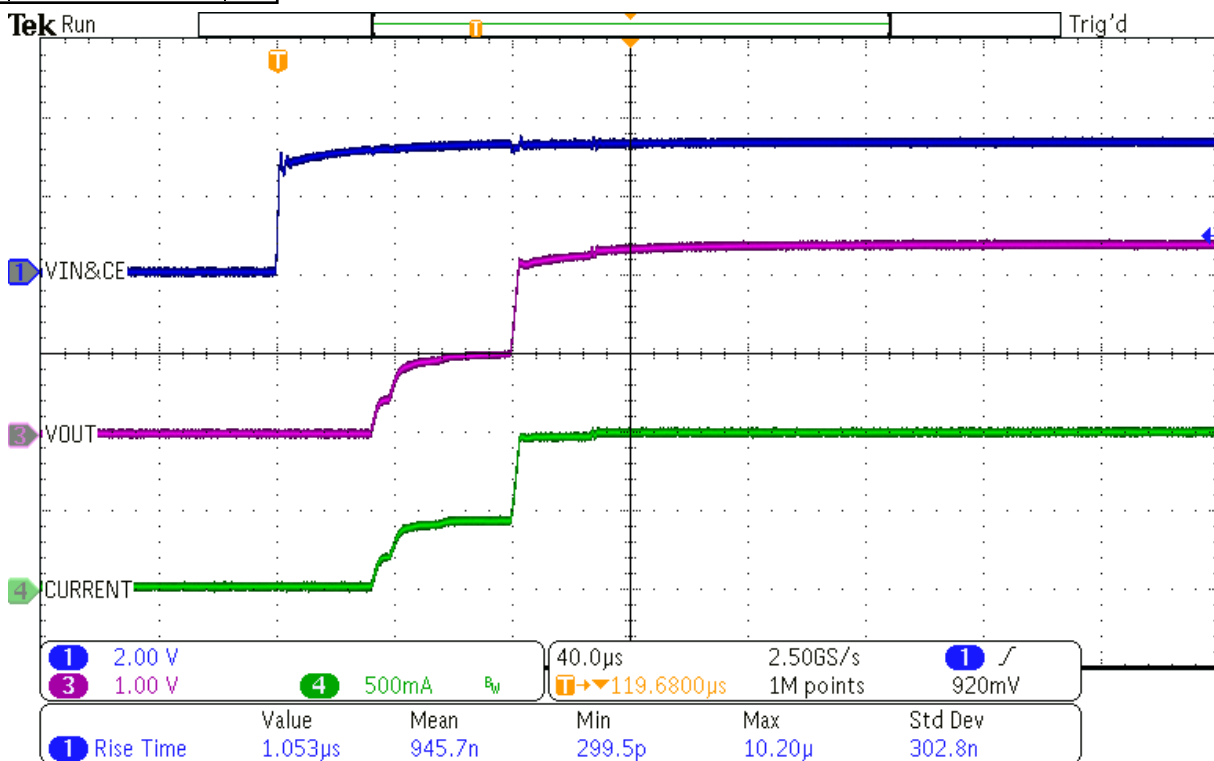
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ASPL8801-180-TH

ASPL8801-250-TH


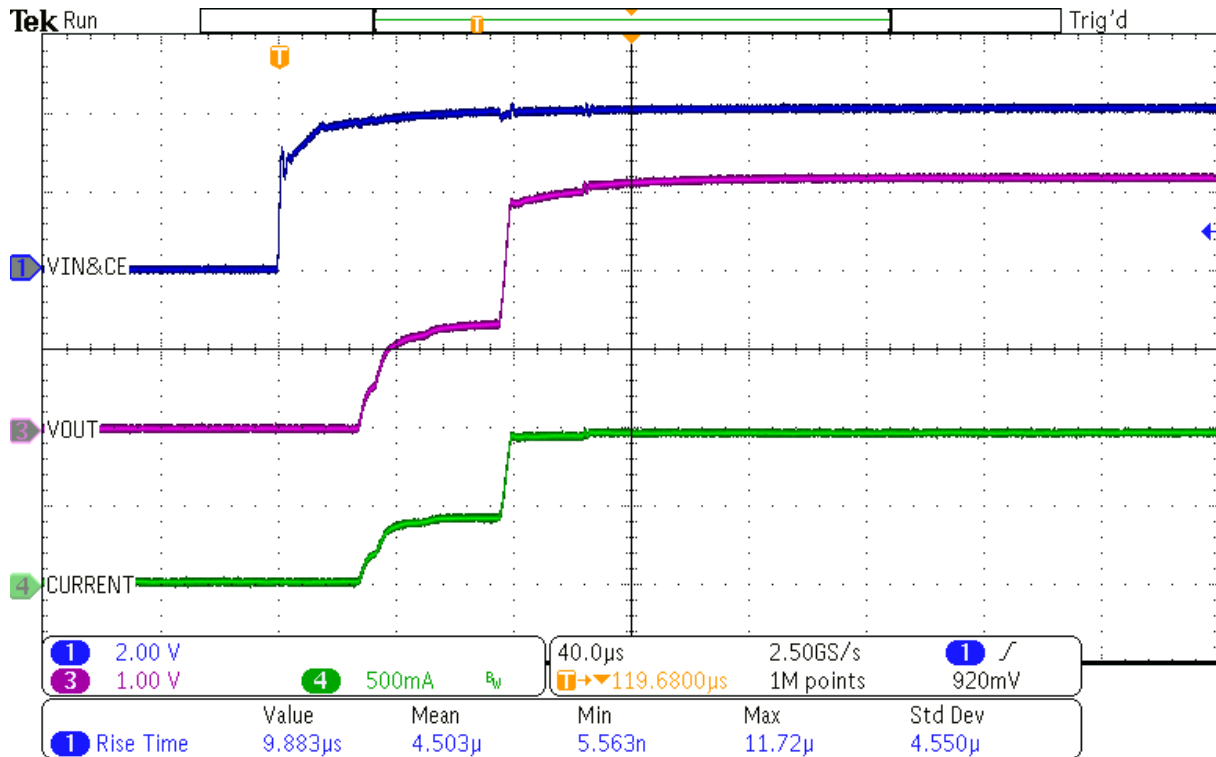
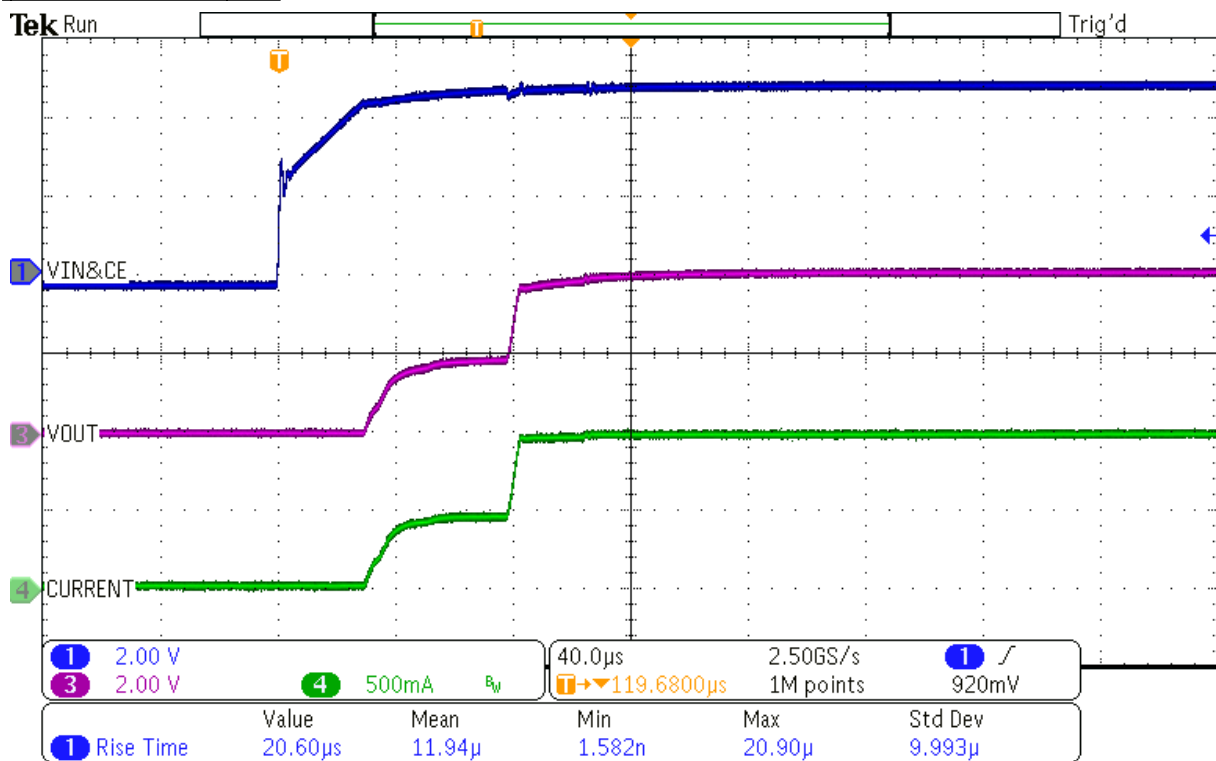
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ASPL8801-330-TH

ASPL8801-430-TH


Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

Turn-on waveform by V_{IN} & CE @ full load ($V_{IN} = CE = 0\text{ V}$ to $V_{OUT}+1\text{V}$, $C_{IN} = C_{OUT} = 1.0\text{ }\mu\text{F}$, $T_a = 25^\circ\text{C}$, $I_{OUT}=1\text{A}$)

ASPL8801-090-TH

ASPL8801-120-TH


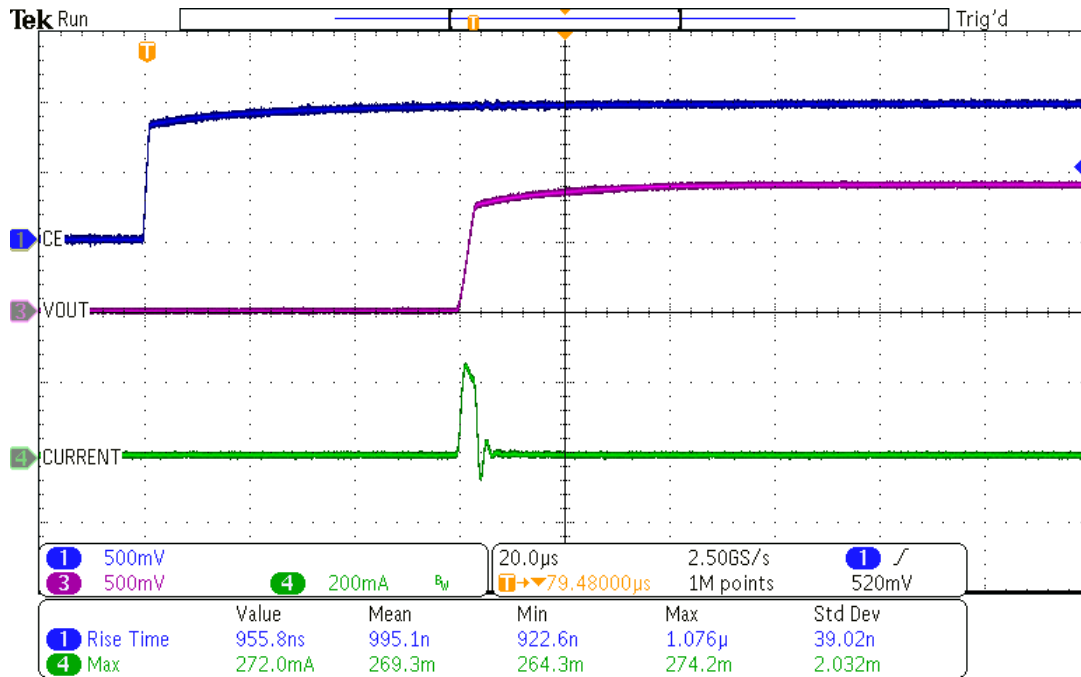
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ASPL8801-180-TH

ASPL8801-250-TH


Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ASPL8801-330-TH

ASPL8801-430-TH


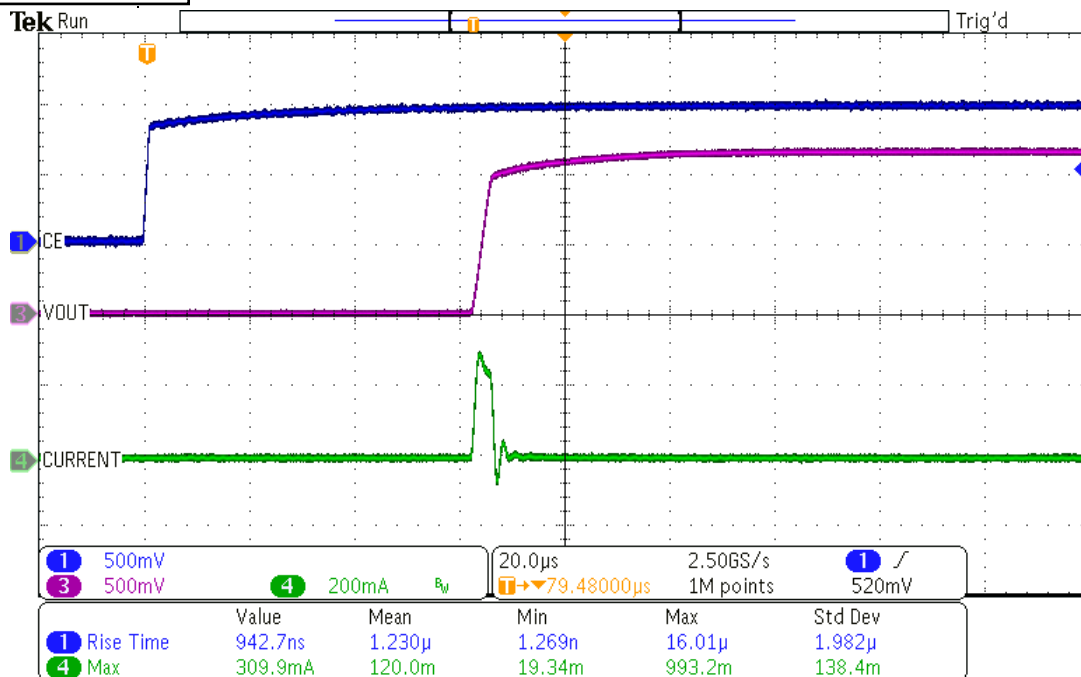
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

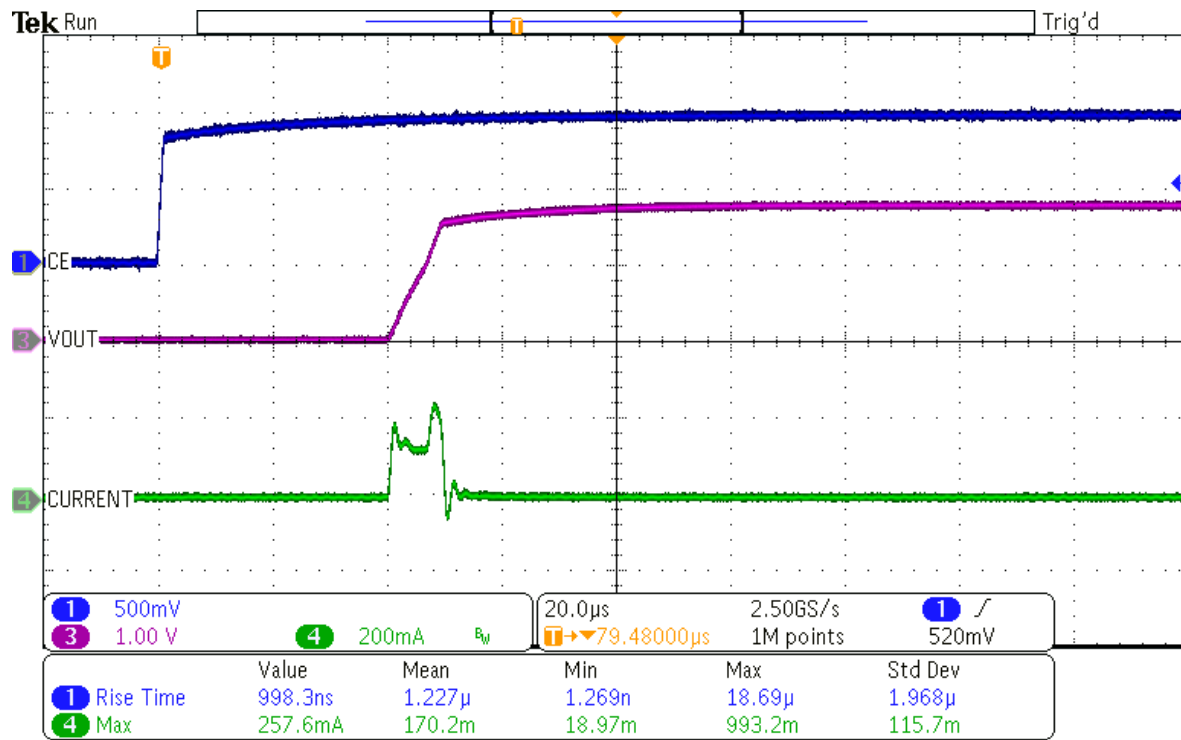
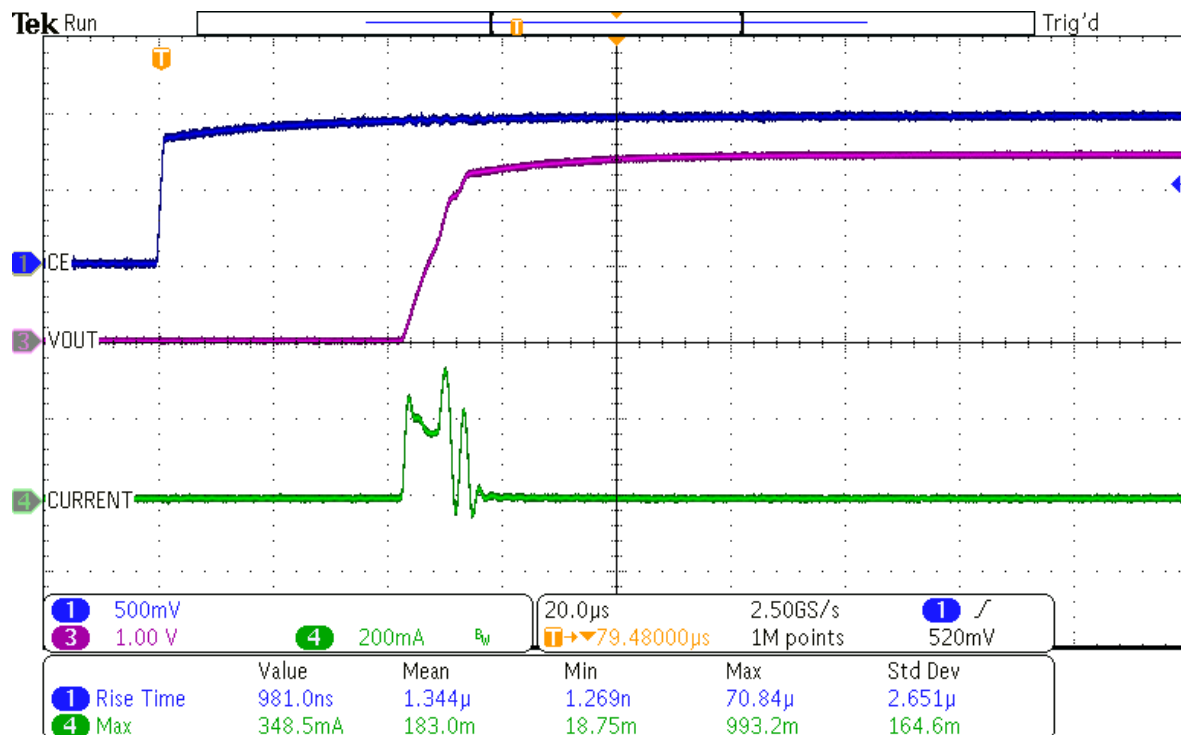
Turn-on by CE pin & Inrush current @ no load ($V_{IN} = V_{OUT} + 1V$, $CE = 0V$ to $1V$, $C_{IN} = C_{OUT} = 1.0 \mu F$, $T_a = 25^\circ C$, $I_{OUT} = 0 mA$)

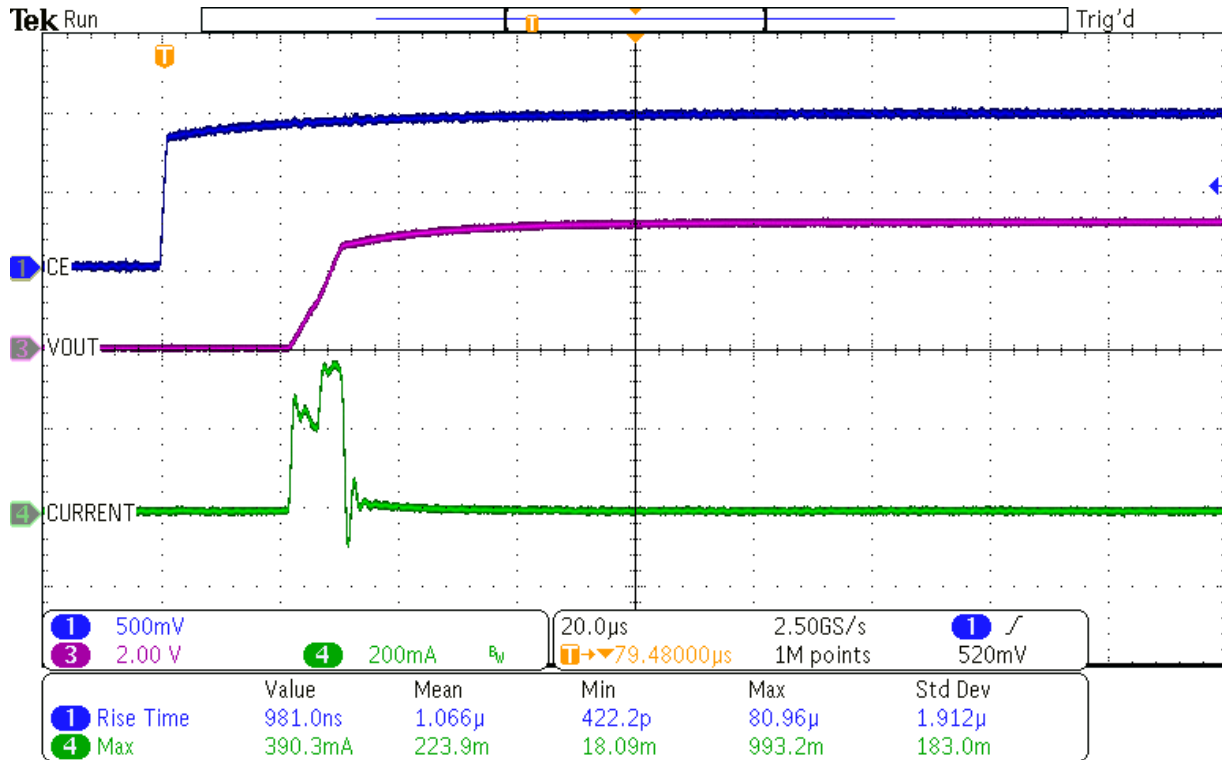
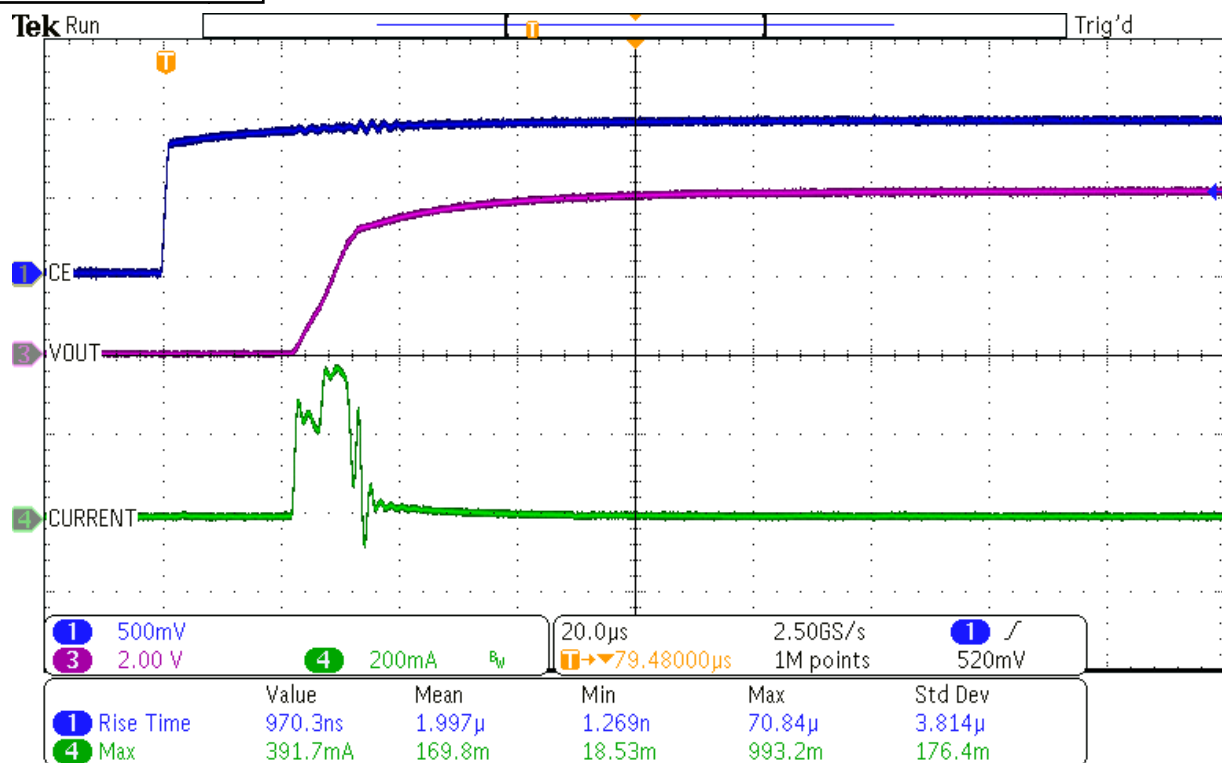
ASPL8801-090-TH



ASPL8801-120-TH

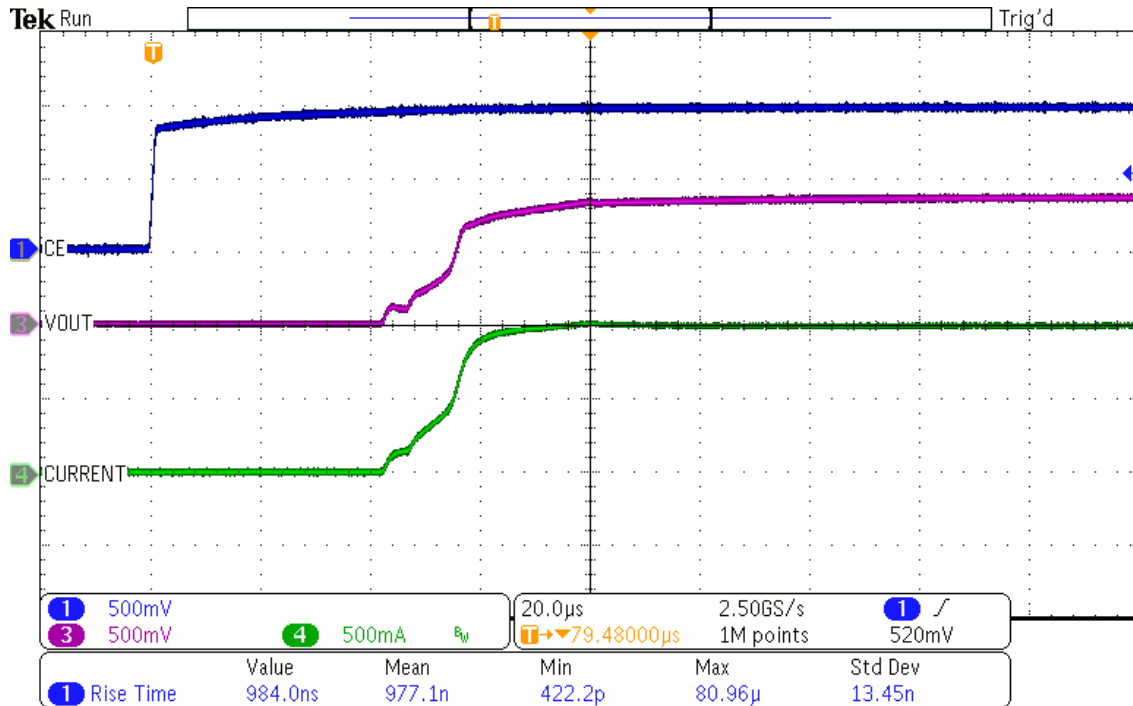
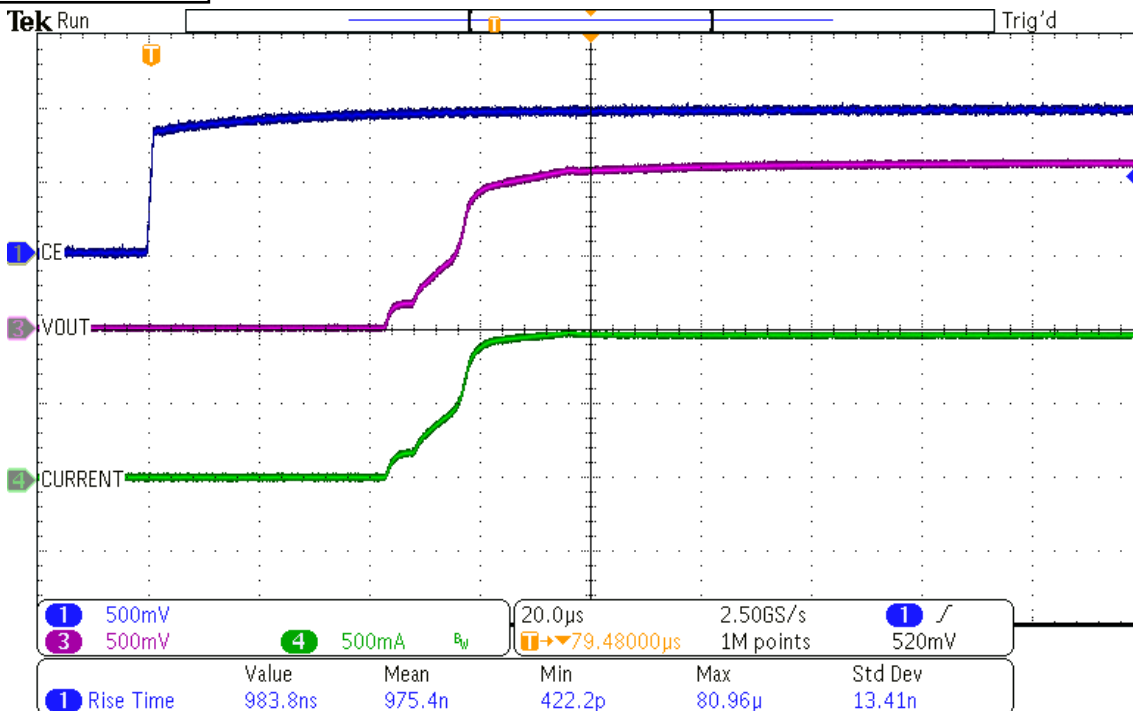


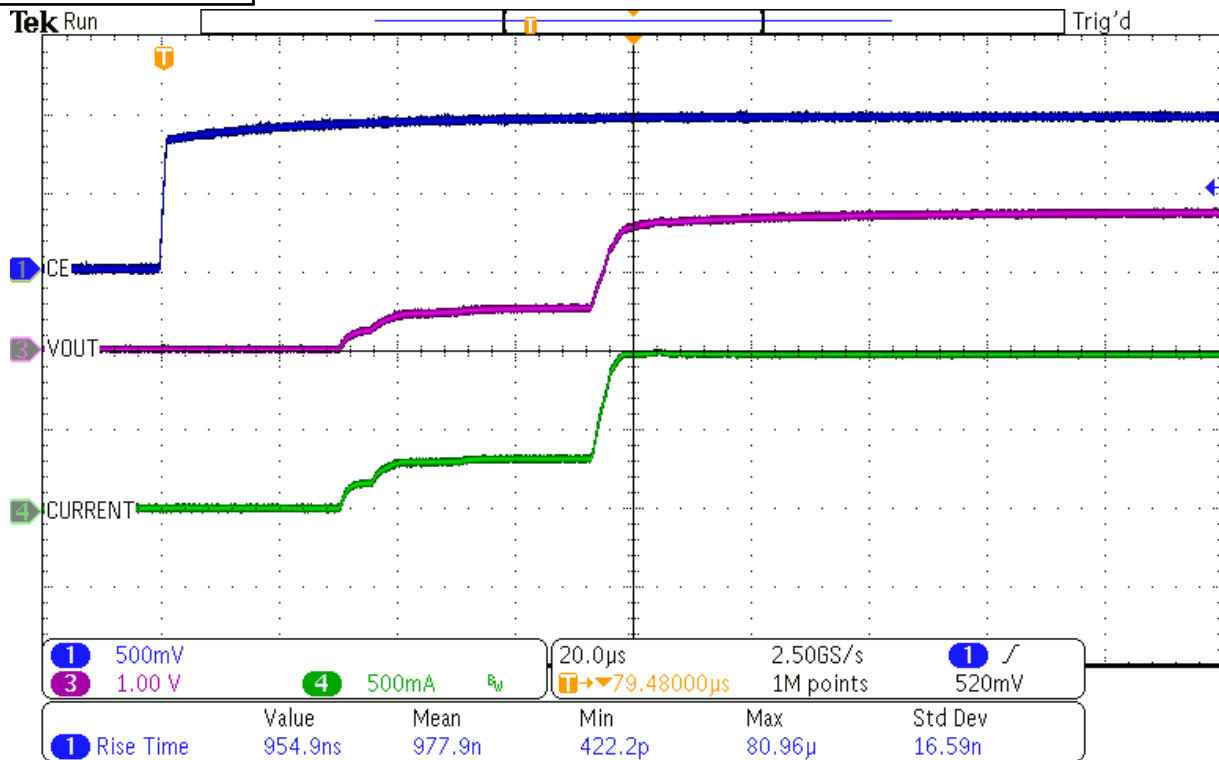
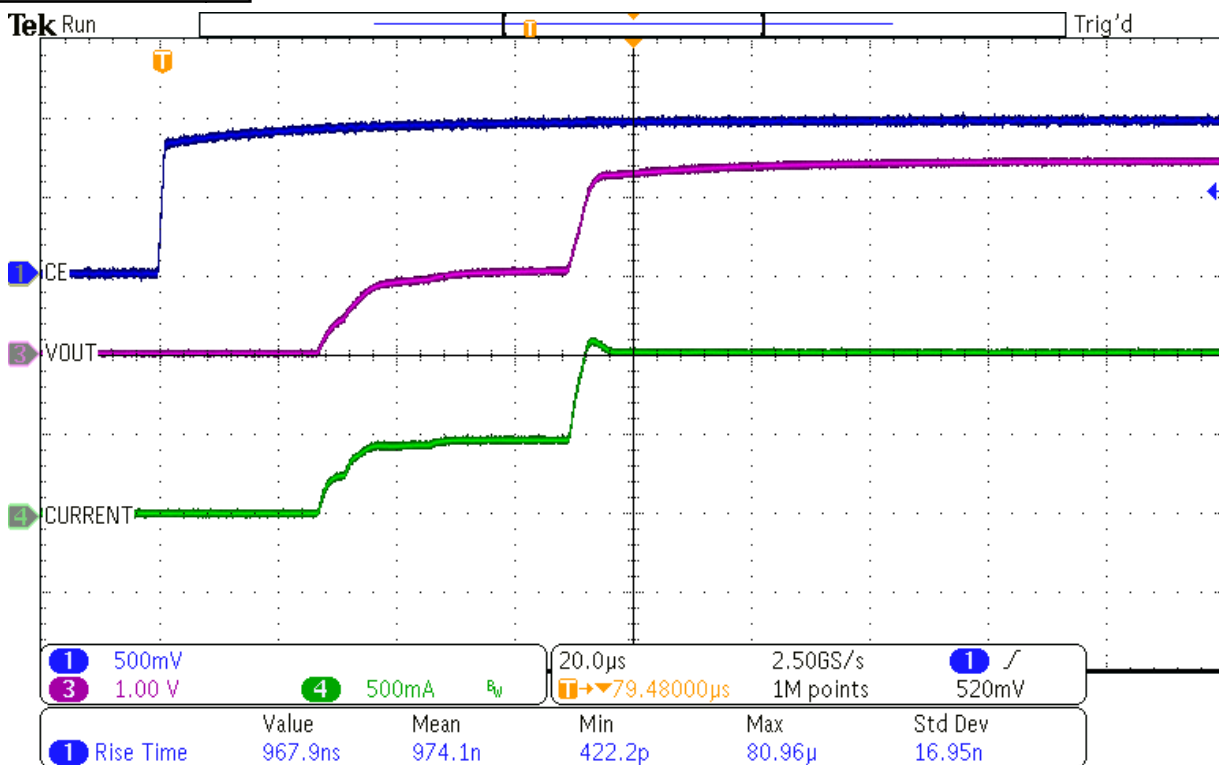
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ASPL8801-180-TH

ASPL8801-250-TH


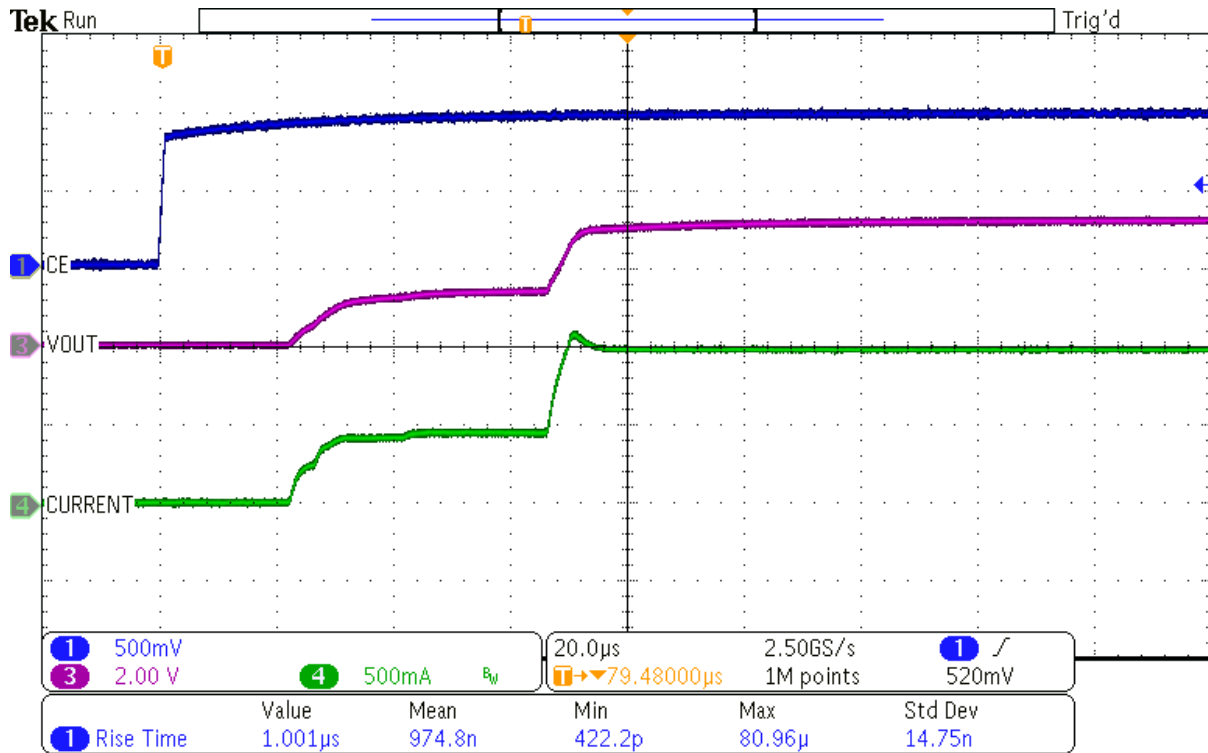
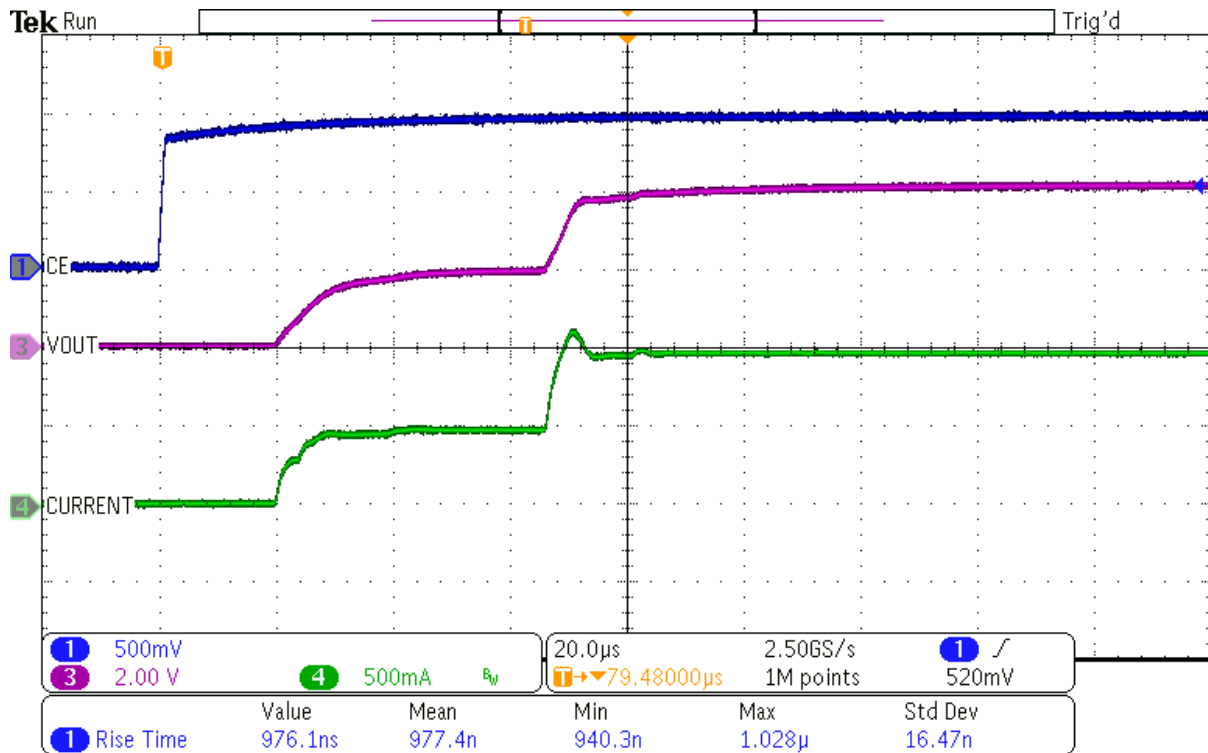
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ASPL8801-330-TH

ASPL8801-430-TH


Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

Turn-on by CE pin @ full load ($V_{IN} = V_{OUT} + 1V$, $CE = 0V$ to $1V$, $C_{IN} = C_{OUT} = 1.0 \mu F$, $T_a = 25^\circ C$, $I_{OUT} = 1A$)

ASPL8801-090-TH

ASPL8801-120-TH


Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ASPL8801-180-TH

ASPL8801-250-TH


Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
ASPL8801-330-TH

ASPL8801-430-TH




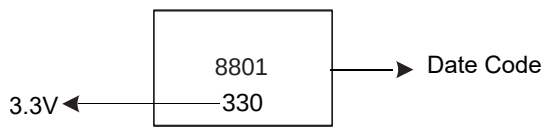
The current version is beta testing. It is recommended that for all test items, the voltage value of v_{in} is fixed at $v_{out}+1V$ to avoid unexpected situations! The future mass production version will not have this restriction.

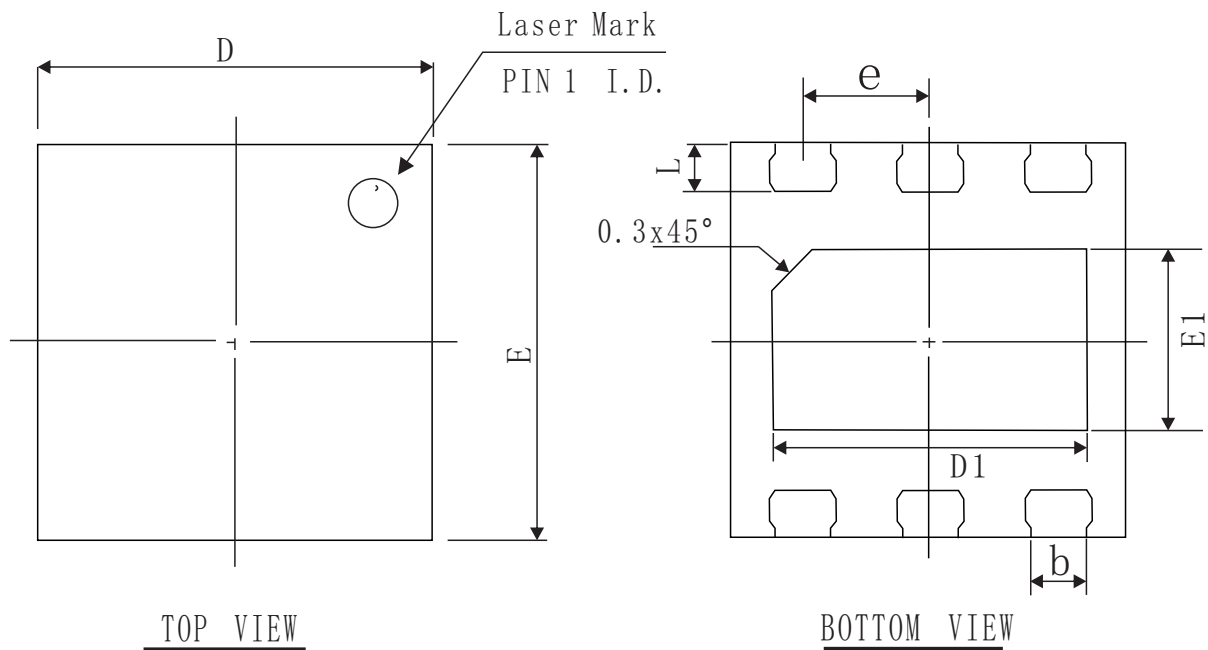
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

Ordering Information

Ordering Number	Package	Packing	Quantity	Pin definition
ASPL8801-xxx-TH-R(V1)	TDFN2020-6	Tape& Reel	3000/Reel	PIN1:GND,PIN2:VOUT,PIN3:VFB PIN4:EN PIN5:LCON PIN6:VIN
ASPL8801-xxx-TH-R(V2)	TDFN2020-6	Tape& Reel	3000/Reel	PIN1:VOUT,PIN2:VFB,PIN3:GND PIN4:EN PIN5:NC PIN6:VIN
ASPL8801-xxx-DI-R	SOT89-3	Tape& Reel	1000/Reel	NA
ASPL8801-xxx-ZD-R	SOT23-5	Tape& Reel	3000/Reel	PIN1:VIN,PIN2:GND,PIN3:EN PIN4:NC PIN5:VOUT

Notes: 1. xxx: Output Voltage, Refer to Marking Information.

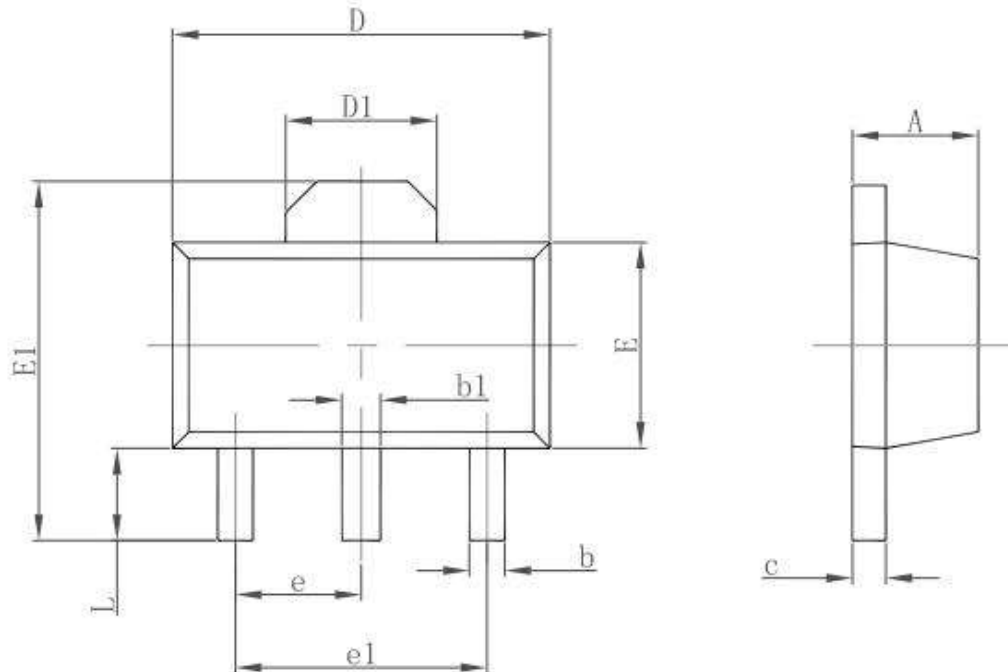
PACKAGE	MARKING
TDFN2020-6 SOT89-3 SOT23-5	

Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO
TDFN2020-6LPackage Information


SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	---	0.05
b	0.28	0.33	0.38
D	1.95	2.00	2.07
E	1.95	2.00	2.07
D1	1.50	1.60	1.70
E1	0.82	0.92	1.02
L	0.15	0.25	0.35
c	0.152 REF		
e	0.65 BSC		

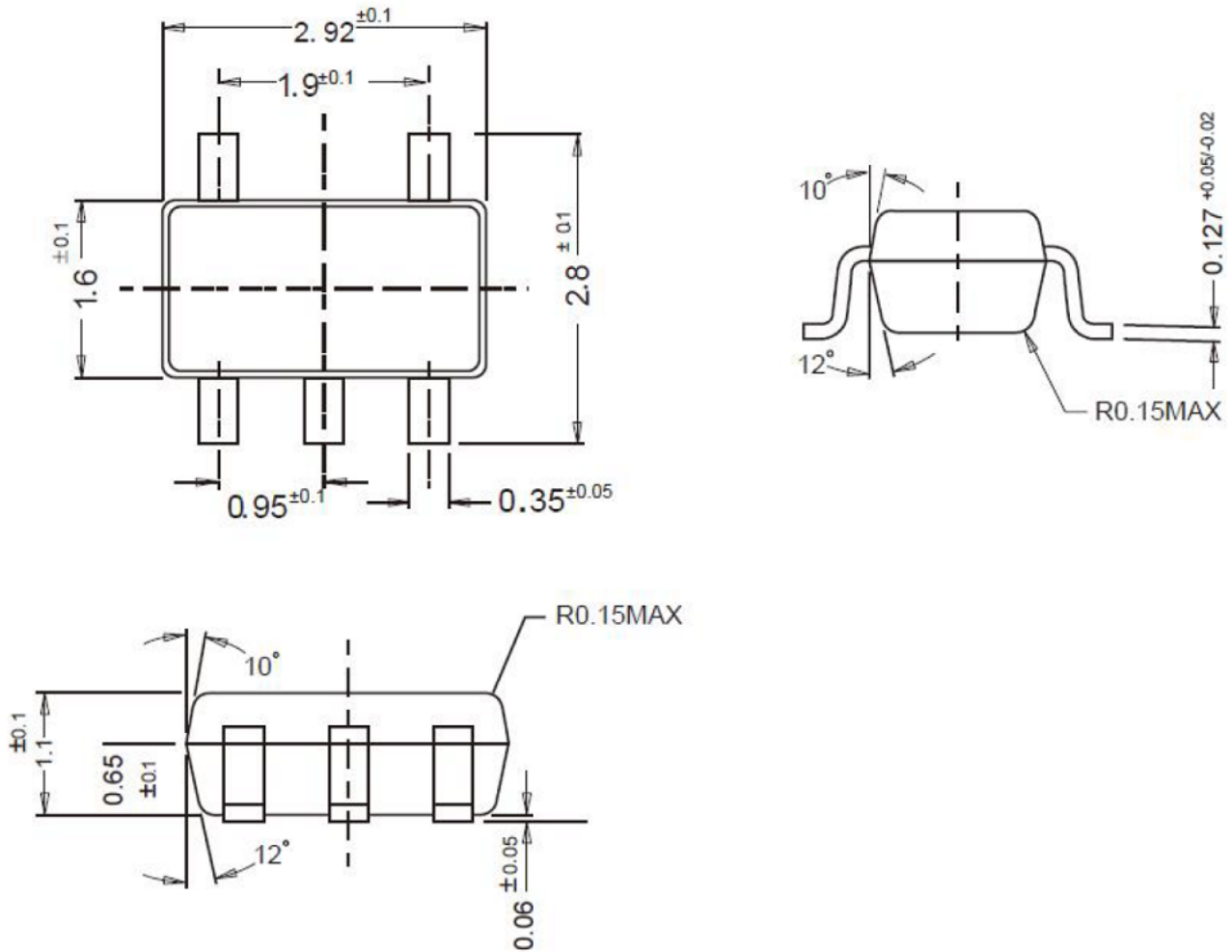
Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO

SOT89-3 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047

SOT23-5 Package Information



Low Noise High PSRR 1 Ch 500mA/1A Alternative LDO**IMPORTANT NOTICE**

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