

Octal Analog Switch Array

FEATURES

- Low On-Resistance: 55 Ω
- Rail-to-Rail Analog Input Range
- Serial Interface
- Low-Power— P_D : 35 nW
- TTL and CMOS Compatible
- Any Combination of 8 SPST to the Output
- High Speed— t_{ON} : 170 ns

BENEFITS

- Low Signal Distortion
- Devices Can Be Chained for System Expansion
- Reduced Board Space
- Reduced Switch Errors
- Reduced Power Supply Requirements
- Simple Interfacing

APPLICATIONS

- Audio Switching and Routing
- Audio Teleconferencing
- Data Acquisition and Industrial Process Control
- Battery Powered Remote Systems
- Automotive, Avionics and ATE Systems
- Summing Amplifiers

DESCRIPTION

The DG485 is an analog switch array consisting of eight SPST switches connected to a common output. This device may be used as an 8-channel multiplexer in serial control applications. Any, all or none of the eight switches may be closed at any given time. Combining low on-resistance ($r_{DS(on)}$ 55 Ω , typ.) and fast switching (t_{ON} : 170 ns, typ.), the DG485 is ideally suited for data acquisition, process control, communication, and avionic applications.

Control data is input serially into the shift register with each clock pulse. The shift register contents can be latched-in (via LD) at any point into an octal latch which in turn controls all switches. $\overline{RS}$ resets the shift register, forcing all latch inputs to a low condition (all switches off). The serial input (D_{IN}) and

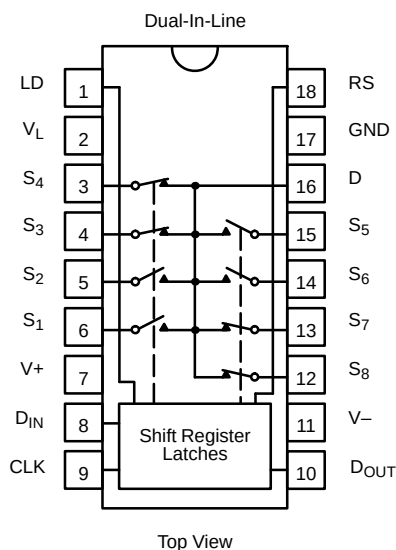
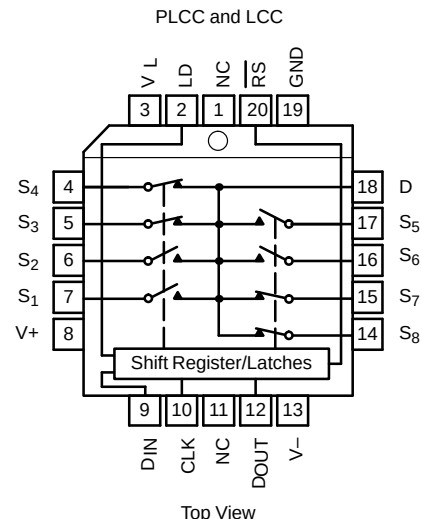
serial output (D_{OUT}) allow daisy chaining of multiple arrays for large systems.

Built on the Vishay Siliconix high voltage silicon gate process the DG485 has a wide 44-V power supply voltage rating. An epitaxial layer prevents latchup.

Each channel conducts equally well in either direction when on and blocks up to rail-to-rail voltages when off.

For additional information please refer to application note AN204.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLES AND ORDERING INFORMATION
TRUTH TABLE—DUAL-IN-LINE PACKAGE

$\overline{RS}$	CLK*	D_{IN}	D_1	D_n
1		0	0	D_{n-1}
1		1	1	D_{n-1}
1		X	D_1	D_n (No Change)
0	X	X	0	0

*CLK Input Edge Triggered

TRUTH TABLE—PLCC & LCC PACKAGES

LD*	D_n	L_n	SW_n
	0	0	OFF
	1	1	ON
	D_n	L_n	(No Change)

*LD Input Level Triggered

ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	18-Pin Plastic DIP	DG485DJ
	20-Pin PLCC	DG485DN
-55 to 125°C	LCC-20	DG485AZ/883

ABSOLUTE MAXIMUM RATINGS
Voltages Referenced to V_- V_+ 44 V

GND 25 V

Digital Inputs^a V_S , V_D (V_-) -2 V to (V_+) + 2 V
or 30 mA, whichever occurs first

Continuous Current (Any Terminal) 30 mA

Current, S or D (Pulsed 1 ms, 10% duty cycle) 100 mA

Storage Temperature (AZ Suffix) -65 to 150°C

(DJ, DN Suffix) -65 to 125°C

Power Dissipation (Package)^b18-Pin Plastic DIP^c 470 mW20-Pin PLCC, LCC^d 800 mW

Notes:

- Signals on S_X , D_X or IN_X exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered or welded to PC board.
- Derate 6 mW/°C above 75°C.
- Derate 10 mW/°C above 75°C.



SPECIFICATIONS ^a										
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ⁺ = 15 V, V [–] = –15 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f	Temp ^b	Typ ^c	A Suffix –55 to 125°C		D Suffix –40 to 85°C		Unit	
					Min ^d	Max ^d	Min ^d	Max ^d		
Analog Switch										
Analog Signal Range ^e	V _{ANALOG}		Full		–15	15	–15	15	V	
Drain-Source On-Resistance	r _{DS(on)}	V ⁺ = 13.5 V, V [–] = –13.5 V I _S = –5 mA, V _D = ±10 V	Room Full	55		85 125		85 125	Ω	
Delta Drain-Source On-Resistance ^g	Δr _{DS(on)}		Room	6					%	
Switch Off Leakage Current	I _{S(off)}	V ⁺ = 16.5 V, V [–] = –16.5 V V _D = ∓15.5 V, V _S = ±15.5 V	Room Full	0.01	–1 –20	1 20	–1 –10	1 10	nA	
	I _{D(off)}		Room Full	0.1	–10 –200	10 200	–10 –50	10 50		
Channel On Leakage Current	I _{D(on)}	V _± = ±16.5 V V _S = V _D = ±15.5 V One Switch At A Time	Room Full	0.11	–20 –500	20 500	–20 –50	20 50		
		V _± = ±16.5 V, V _S = V _D = ±15.5 V All Switches On	Room	0.2						
Input										
Input Current with V _{IN} Low	I _{IL}	V _{IN} Under Test = 0.8 V All Other = 2.4 V	Room Full	–0.0001	–1 –5	1 5	–1 –5	1 5	μA	
Input Current with V _{IN} High	I _{IH}	V _{IN} Under Test = 2.4 V All Other = 0.8 V	Room Full	0.0001	–1 –5	1 5	–1 –5	1 5		
Serial Data Output										
Output Voltage with V _{IN} Low – D _{OUT}	V _{OL}	I _O = 1.6 mA, V ⁺ = 4.5 V	Full	0.25		0.4		0.4	V	
Output Voltage with V _{IN} High – D _{OUT}	V _{OH}	I _O = –80 μA, V ⁺ = 16.5 V V _L = 4.75 V	Full	4.4	2.7		2.7			
Dynamic Characteristics										
Turn-On Time	t _{ON}	V _S = ±10 V See Figures 1, 8	Room Full	170		200 275		200 275	ns	
Turn-Off Time	t _{OFF}	V _S = ±10 V See Figures 2, 3, 8	Room Full	150		200 275		200 276		
Data Setup Time	t _{DS}	See Figures 4, 8	Room Full		40 60		40 60			
Data Hold Time	t _{DH}		Room Full		40 60		40 60			
LOAD Hold Time	t _{LH}	See Figures 5, 8	Room Full		100 150		100 150			
RESET Hold Time	t _{RH}		Room Full		100 150		100 150			
RESET ↑ to CLOCK ↑ Delay	t _{DRC}		Room Full		40 60		40 60			
Charge Injection	Q	V _S = 0 V, C _L = 1,000 pF Any One Channel	Room	17					pC	
Off Isolation ^e	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz See Figure 9	Room	–75					dB	
Maximum Clock Frequency	f _{CLK}		Room	10					MHz	

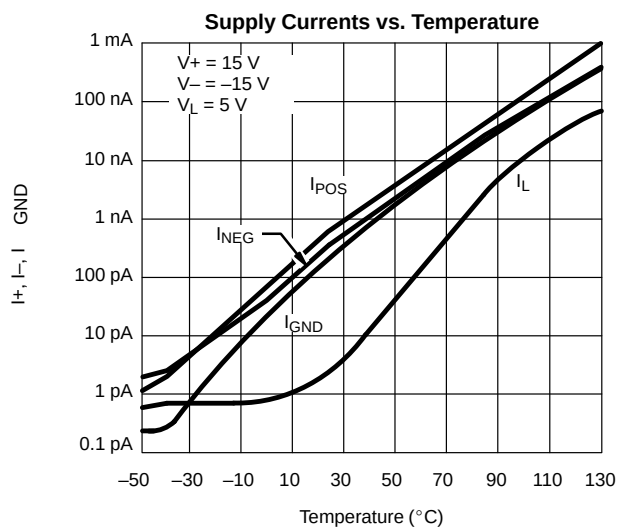
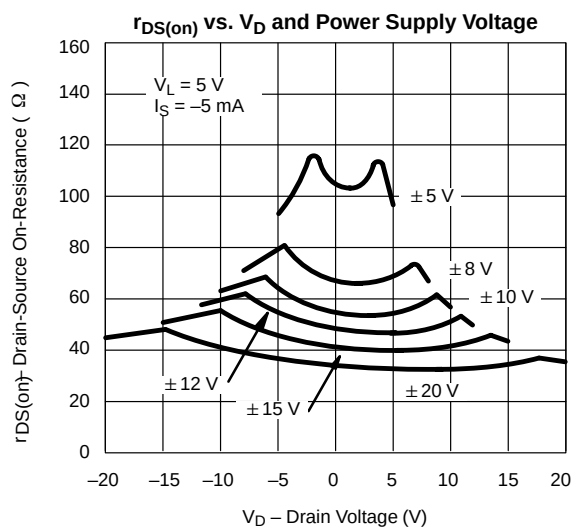
SPECIFICATIONS^a

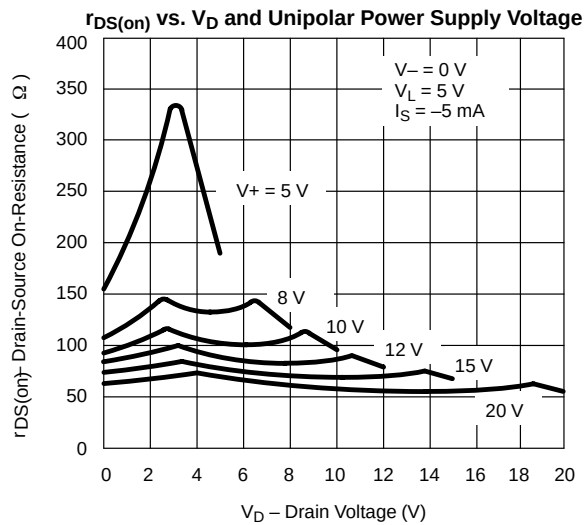
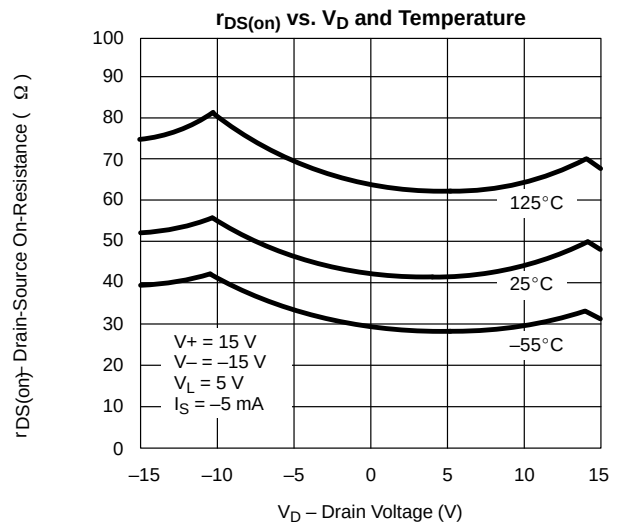
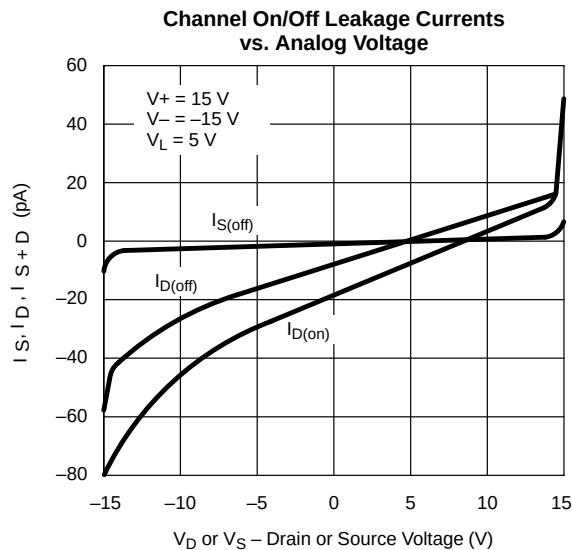
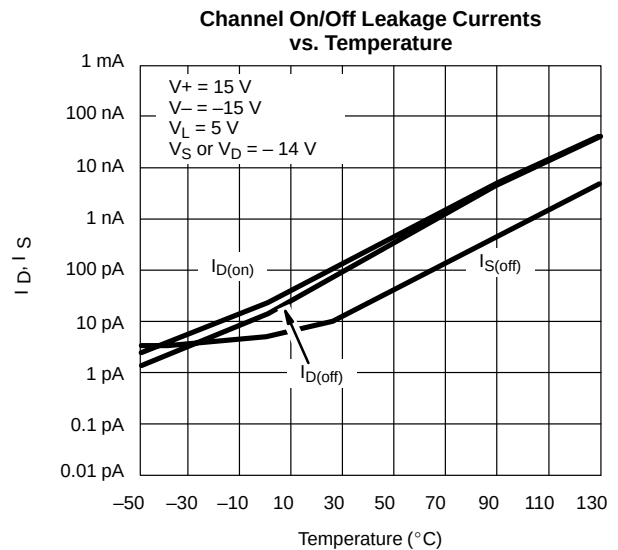
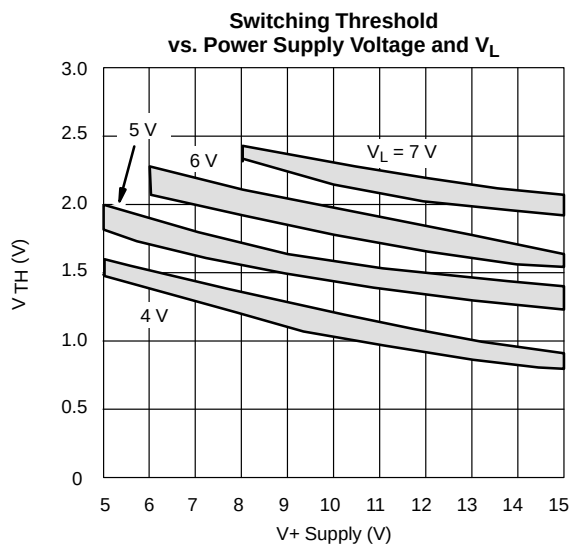
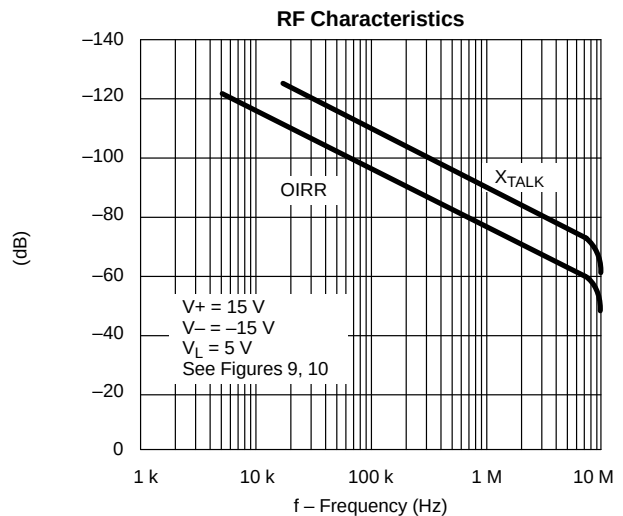
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V VL = 5 V, VIN = 2.4 V, 0.8 V ^f	Temp ^b	Typ ^c	A Suffix −55 to 125°C		D Suffix −40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Dynamic Characteristics (Cont'd)									
Source Off Capacitance ^e	CS(off)	Vgen = 0 V, Rgen = 0 Ω, f = 1 MHz	Room	7					pF
Drain Off Capacitance ^e	CD(off)		Room	43					
On-State Capacitance ^e	CD(on)	Vgen = 0 V, Rgen = 0 Ω, f = 1 MHz One Channel On	Room	53					
		Vgen = 0 V, Rgen = 0 Ω, f = 1 MHz All Channels On	Room	122					
Power Supplies									
Positive Supply Current	I+	V+ = 16.5 V, V− = −16.5 V VIN = 0 or 5 V, VL = 5.25 V DO _{OUT} Open	Room Full	0.001		3 10		3 10	μA
Negative Supply Current	I−		Room Full	−0.001	−3 −10		−3 −10		
Logic Supply Current	IL		Room Full	0.001		3 10		3 10	
Ground Current	IGND		Room Full	−0.001	−3 −10		−3 −10		

Notes:

- a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

g. For each V_D : $\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}^{MAX} - r_{DS(on)}^{MIN}}{r_{DS(on)}^{AVE}} \right)$

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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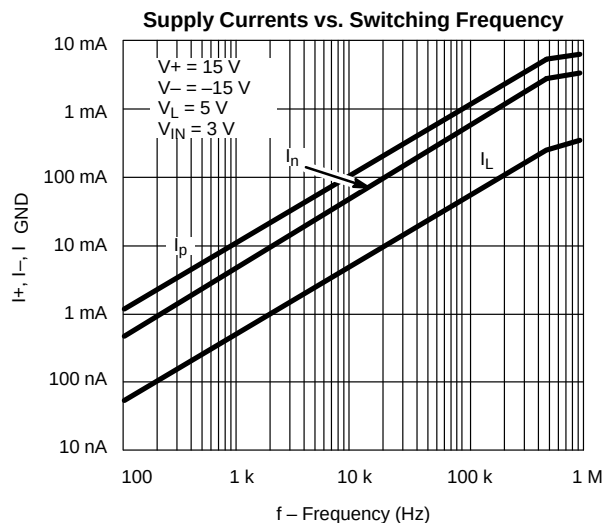
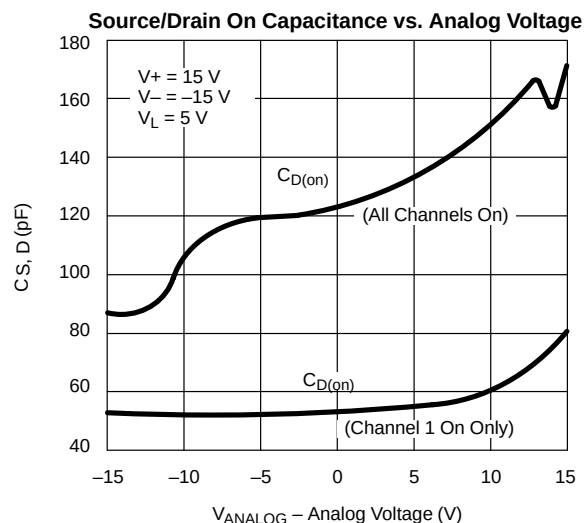
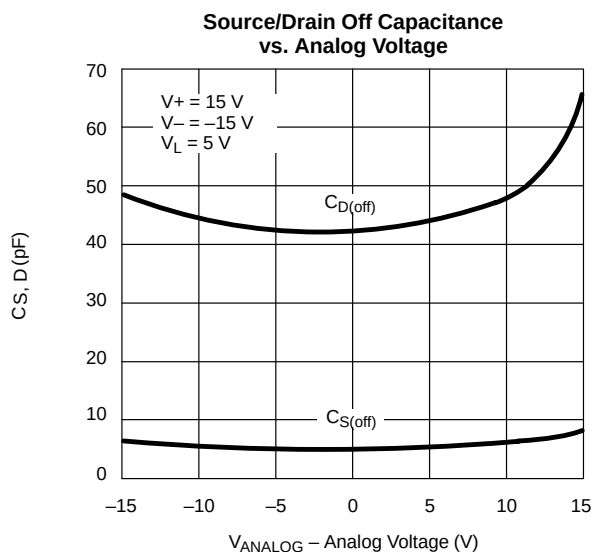
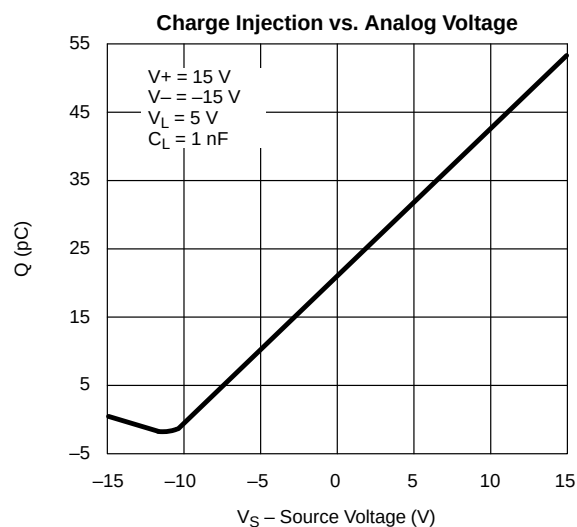
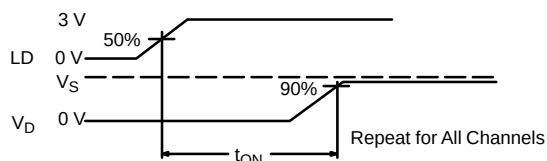
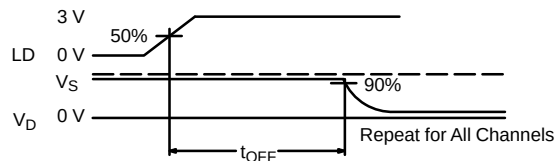
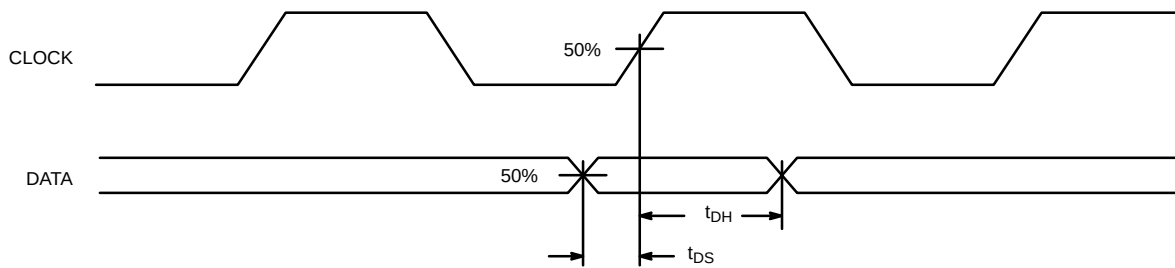
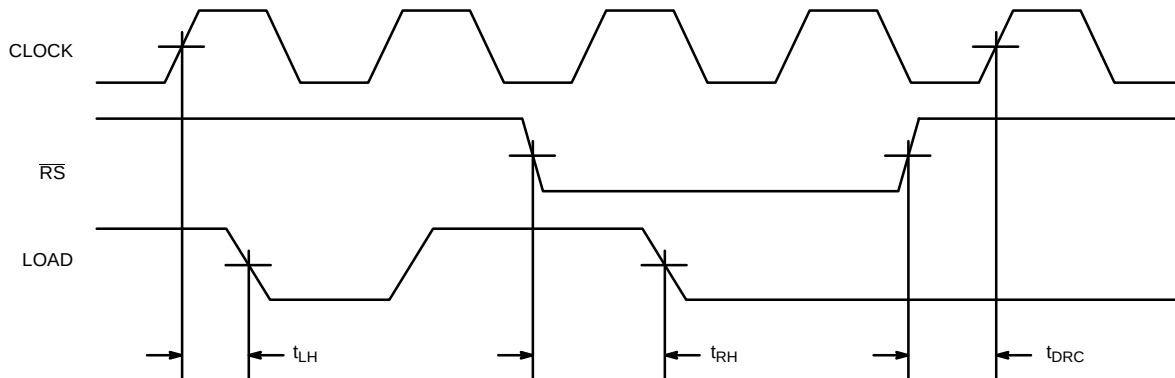
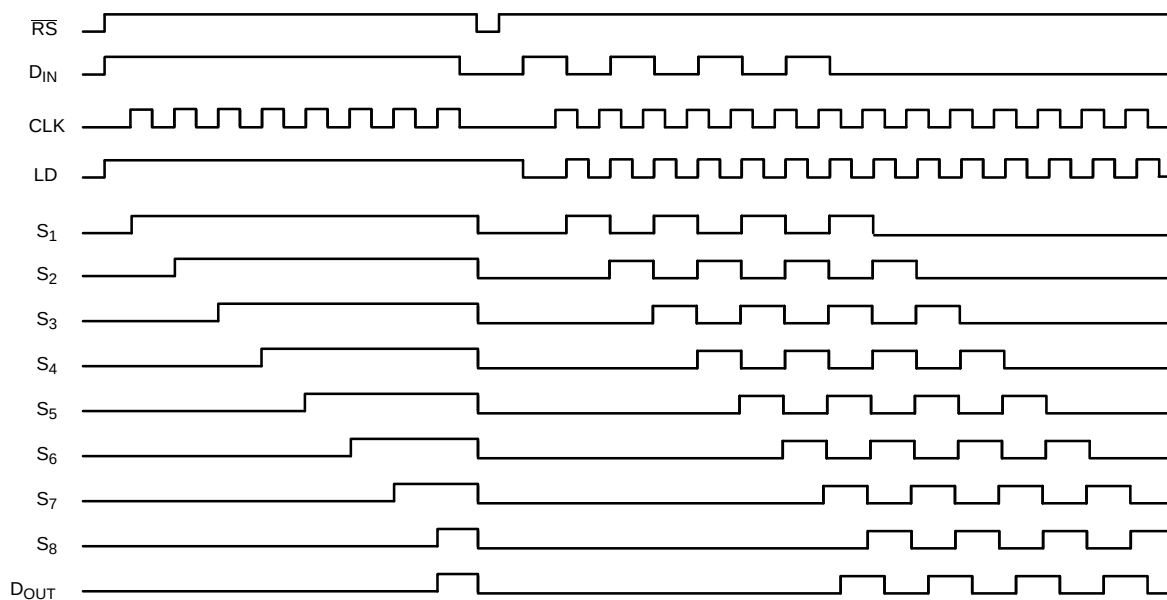
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

TIMING DIAGRAMS

FIGURE 1. t_{ON} from LD

FIGURE 2. t_{OFF} from LD

FIGURE 3. t_{OFF} from $\overline{RS}$

TIMING DIAGRAMS

FIGURE 4. Data Setup and Hold Time

FIGURE 5. Timing Relationships


$S_1 - S_8$ and D_{OUT} are expected output with the drain connected high. The sources require pull-down of 1 k Ω .

FIGURE 6.

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

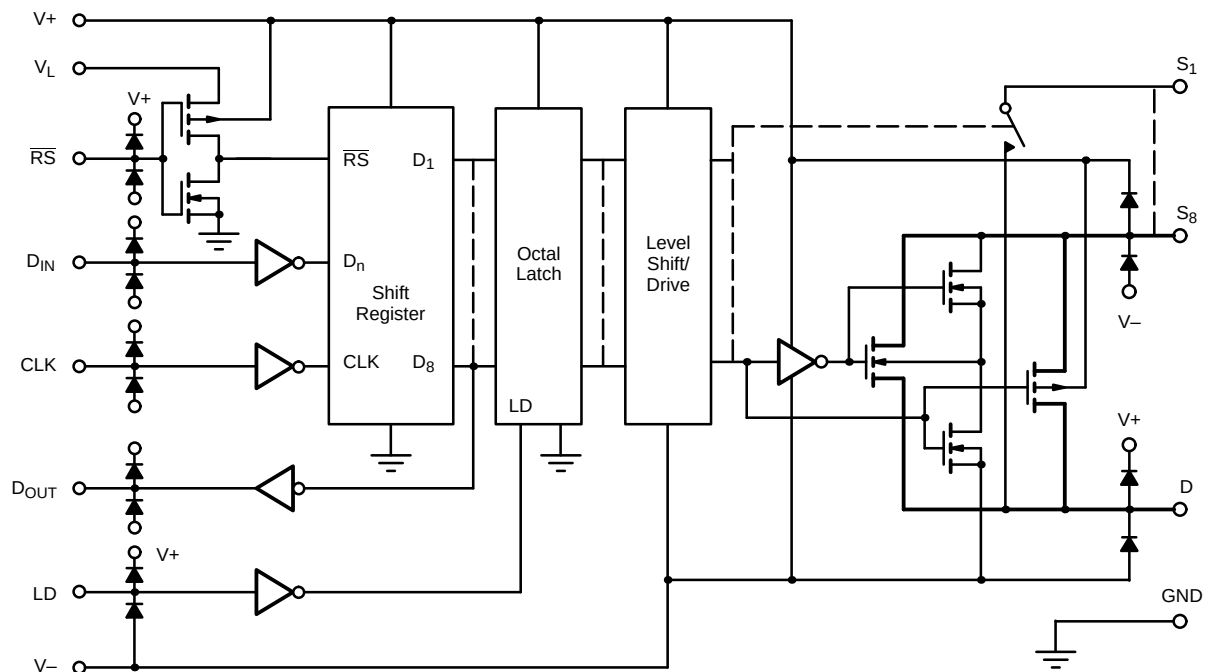
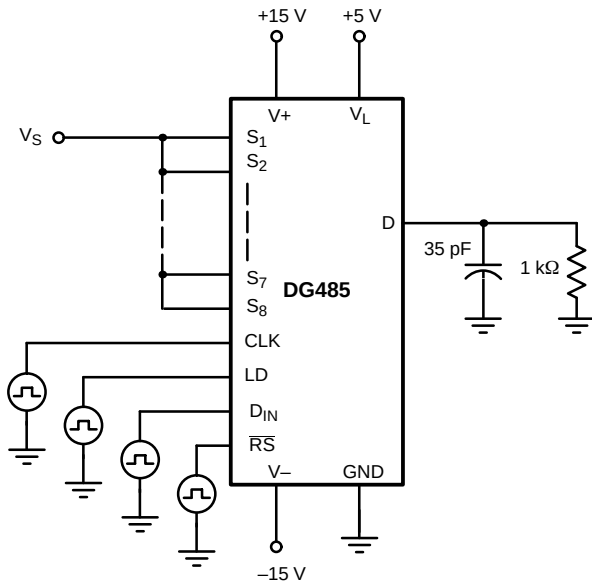
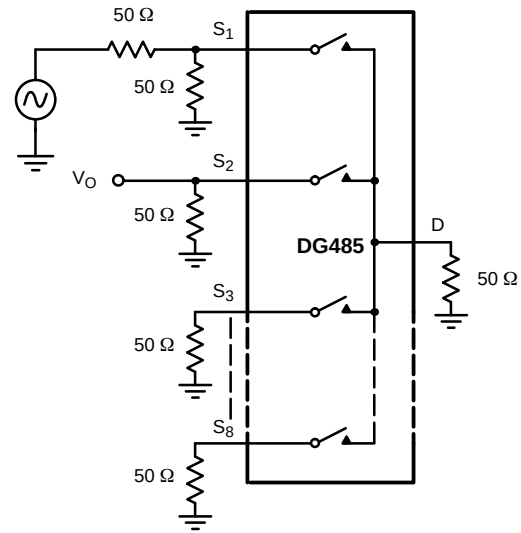
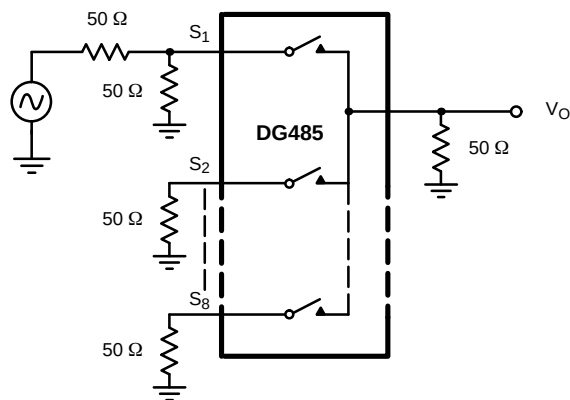
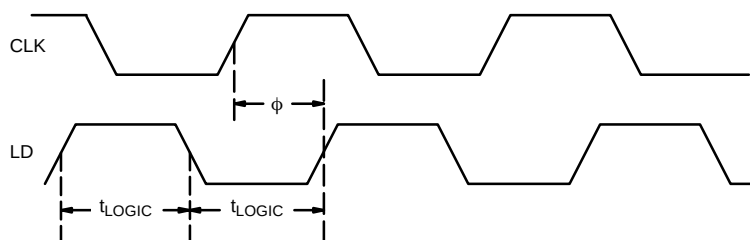


FIGURE 7.

TEST CIRCUITS

FIGURE 8. Switching Time Test Circuit

FIGURE 9. Adjacent Input Crosstalk

TEST CIRCUITS

FIGURE 10. Off Isolation

APPLICATIONS



ϕ = for CLK and LD inputs of the same frequency.
The recommended phase delay of LD from CLK is $\frac{1}{2} t_{\text{LOGIC}}$ to t_{LOGIC} :

$t_{\text{LOGIC(MIN)}}$: 80 ns at 25°C $V_+ = 15 \text{ V}$
150 ns at 125°C $V_- = -15 \text{ V}$
GND = 0 V

FIGURE 11.

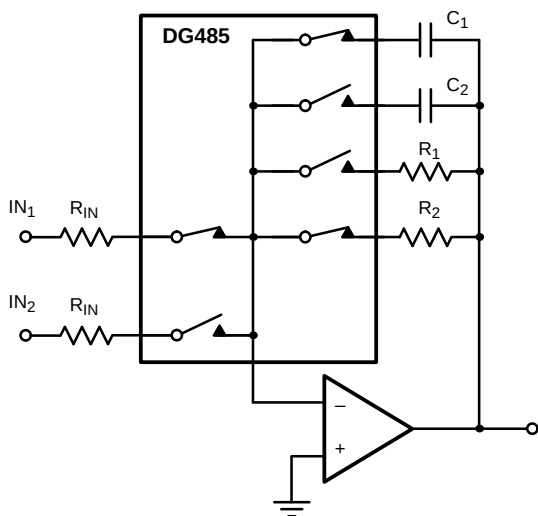


FIGURE 12. Multi-Function Circuit Provides Input Selection, Gain Ranging and Filtering with One DG485

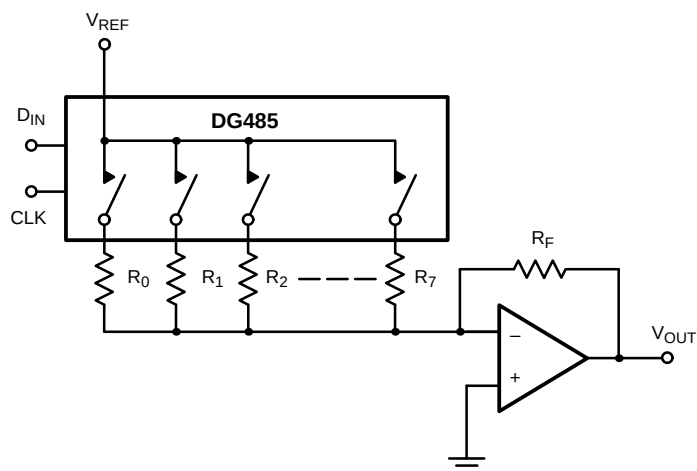


FIGURE 13. Serial DAC Circuit

APPLICATIONS

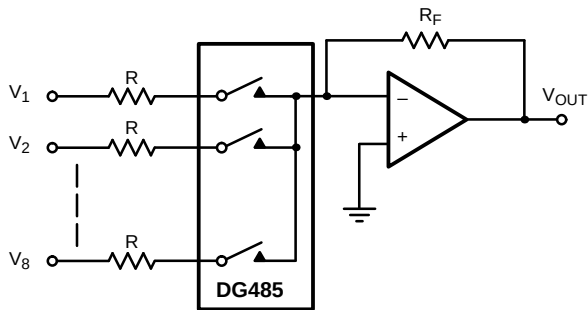


FIGURE 14. Summing Node Mixer

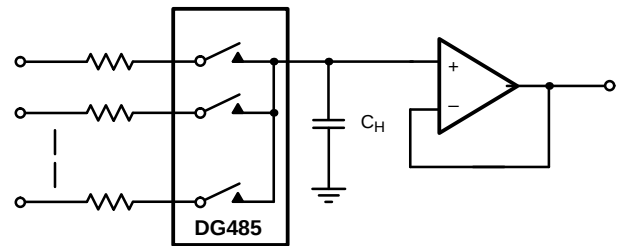


FIGURE 15. Multiplexing, Sampling Application

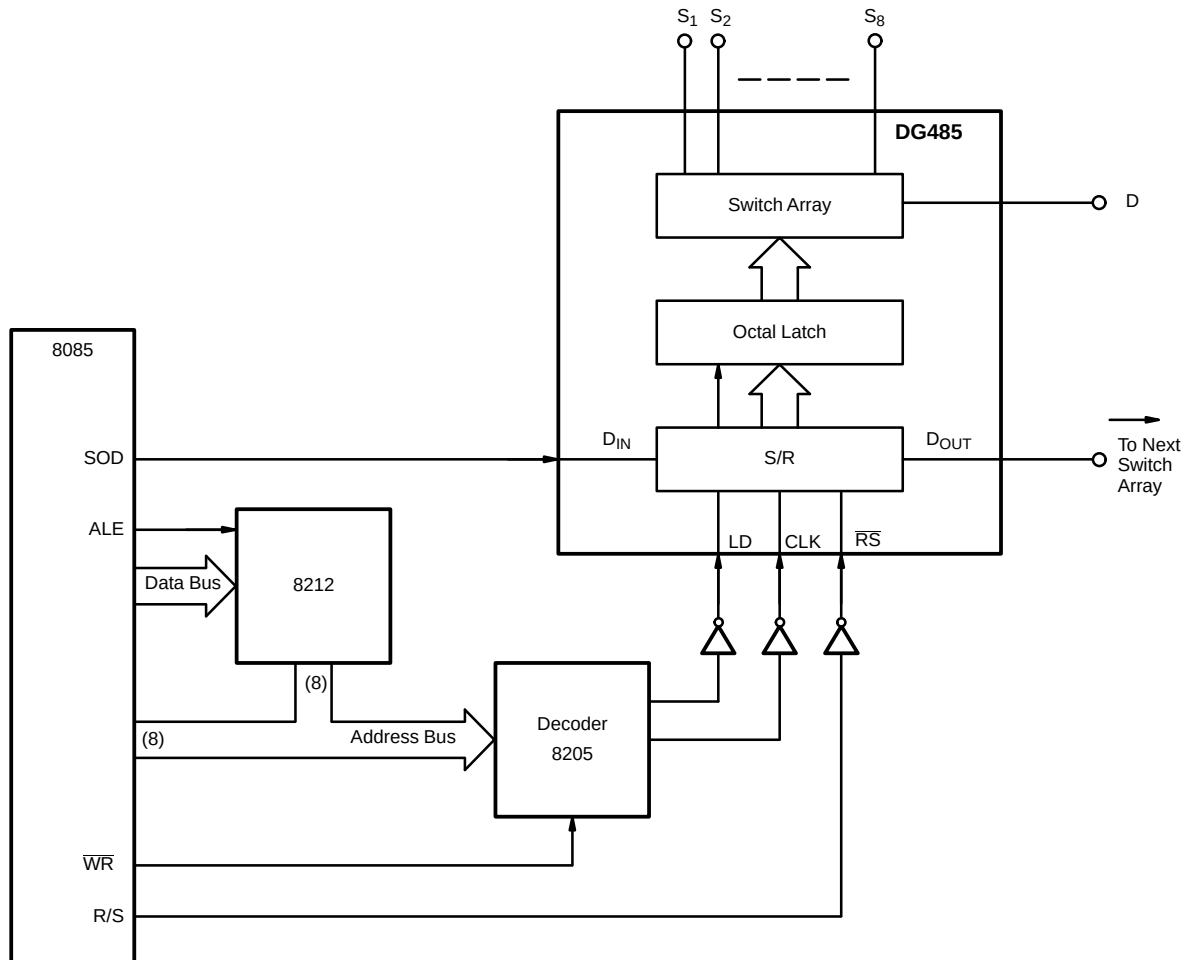


FIGURE 16. Direct Serial Interface (8085)