

DESCRIPTION

The NB687 provides a complete one-chip power solution for DDR4 memory with the highest power density and is also compatible with DDR3/3L. The NB687 integrates a high-frequency, synchronous, rectified, step-down, switch-mode converter (VDDQ) with a 1A source LDO (VPP), 1A sink/source LDO (VTT), and buffered low-noise reference (VTTREF).

The NB687 operates at high efficiency over a wide output current load range based on MPS's proprietary switching loss reduction technique and internal low $R_{DS(ON)}$ power MOSFETs.

Adaptive constant-on-time (COT) control mode provides fast transient response and easy loop stabilization. The DC auto-tune loop combined with the remote differential sense provides good load and line regulation.

The VPP LDO provides 1A of source current capability and requires only 47 μ F of ceramic capacitance. The VTT LDO provides 1A of sink/source current capability and requires only 22 μ F of ceramic capacitance. VTTREF tracks VDDQ/2 with excellent 1% accuracy.

The NB687 also provides a S3/S5 mode operation combined with EN1/EN2 control.

Full protection features include under-voltage lockout (UVLO), over-current limit (OCL), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The converter requires a minimal number of external components and is available in a QFN-16 (3mmx3mm) package.

FEATURES

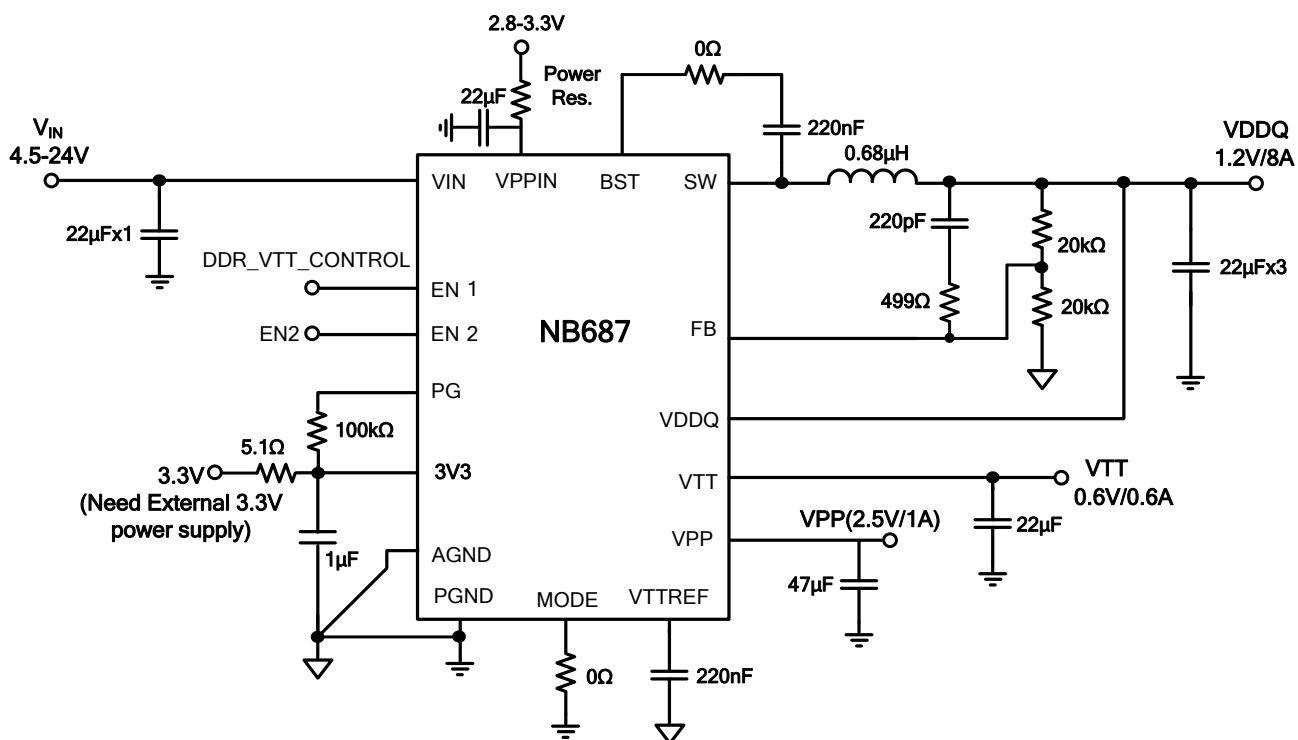
- Wide 4.5V to 28V Operating Input Range
- One-Chip DDR4 Design Compatible with DDR3/DDR3L
- Output Adjustable from 0.6V to 5V
- 100 μ A Low Quiescent Current
- 8A Continuous Output Current
- 10A Peak Output Current
- Selectable Ultrasonic Mode (USM)
- Selectable 500kHz/700kHz Switching Frequency
- Built-In 1A VPP LDO
- Built-In $\pm$ 1A VTT LDO
- 1% Buffered VTTREF Output
- Adaptive COT for Fast transient
- DC Auto-Tune Loop
- Low $R_{DS(ON)}$ Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Stable with POSCAP and Ceramic Capacitors
- Internal Soft Start (SS)
- Output Discharge
- OCL, OVP, UVP, and Thermal Shutdown
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS

- Laptop Computers
- Motherboards
- Networking Systems
- Servers
- Distributed Power Systems

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
NB687GQ	QFN-16 (3mmx3mm)	See Below

* For Tape & Reel, add suffix -Z (e.g.: NB687GQ-Z)

TOP MARKING

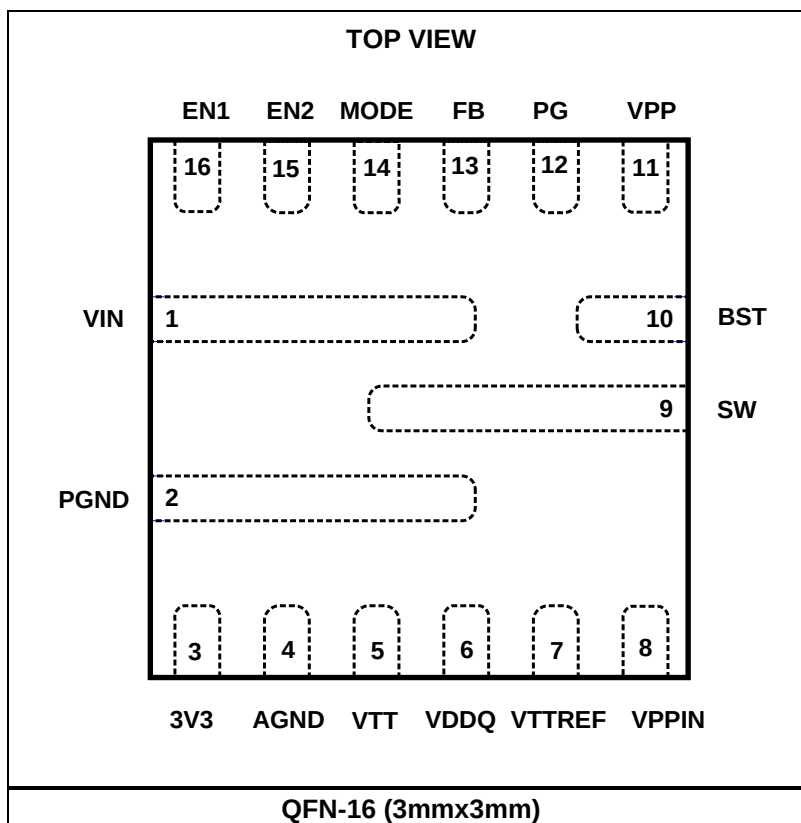
AVTY
 LLL

AVT: Product code of NB687GQ

Y: Year code

LLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply voltage (V_{IN})	28V
V_{SW}	-1V to 25V
V_{SW} (25ns)	-3.6V to 28V
V_{BST}	$V_{SW} + 4.5V$
I_{EN1}, I_{EN2}	100 μ A
All other pins	-0.3V to + 4.5V
Continuous power dissipation ($T_A = +25^\circ C$) ⁽²⁾	
QFN-16 (3mmx3mm)	2.3W
Junction temperature	150 $^\circ C$
Lead temperature	260 $^\circ C$
Storage temperature	-65 $^\circ C$ to +150 $^\circ C$

Recommended Operating Conditions ⁽³⁾

Supply voltage (V_{IN})	4.5V to 24V
Supply voltage (V_{CC})	3.15 V to 3.5V
Supply voltage (V_{PP_IN})	2.8 V to 3.5V
Output voltage (V_{OUT})	0.6V to 3.3V
I_{EN1}, I_{EN2}	50 μ A
Operating junction temp. (T_J)	-40 $^\circ C$ to +125 $^\circ C$

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
QFN-16 (3mmx3mm)	55	13 ... $^\circ C/W$

NOTES:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J(MAX)$, the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX) = (T_J(MAX) - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$, $3V3 = 3.3V$, $V_{PP_IN} = 3.3V$, $T_J = 25^{\circ}C$, $R_{MODE} = 0\Omega$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
3V3 supply current in normal mode	I_{3V3}	$V_{EN1} = V_{EN2} = 2V$, no load		160		μA
3V3 supply current in S3 mode	I_{3V3_S3}	$V_{EN1} = 0V$, $V_{EN2} = 2V$, no load		110		μA
3V3 shutdown current	I_{3V3_SDN}	$V_{EN1} = V_{EN2} = 0V$, no load			3	μA
MOSFET						
High-side switch on resistance	$HS_{RDS(ON)}$	$T_J = 25^{\circ}C$		22		$m\Omega$
Low-side switch on resistance	$LS_{RDS(ON)}$	$T_J = 25^{\circ}C$		7.5		$m\Omega$
Switch leakage	SW_{LKG}	$V_{EN} = 0V$, $V_{SW} = 0V$		0	1	μA
Current Limit						
Low-side valley current limit	I_{LIMIT}		10	11	13	A
Switching Frequency and Minimum Off Time						
Switching frequency ⁽⁵⁾	F_S	$R_{MODE} = 0\Omega$		700		kHz
		$R_{MODE} = 150k\Omega$		500		kHz
Constant on timer	T_{ON}	$V_{IN} = 6V$, $V_{OUT} = 3V$, $R_{MODE} = 150k\Omega$	1100	1200	1300	ns
Minimum on time ⁽⁶⁾	T_{ON_MIN}			60		ns
Minimum off time ⁽⁶⁾	T_{OFF_MIN}			390		ns
Ultrasonic Mode (USM)						
Ultrasonic mode operation period	T_{USM}	$V_{FB} = 0.62V$		30		μs
VDDQ Protection						
OVP threshold	V_{OVP}		125%	130%	135%	V_{REF}
UVP-1 threshold	V_{UVP-1}		70%	75%	80%	V_{REF}
UVP-2 threshold	V_{UVP-2}		45%	50%	55%	V_{REF}
Reference and Soft Start, Soft Stop						
Reference voltage	V_{REF}		594	600	606	mV
Feedback current	I_{FB}	$V_{FB} = 0.62V$		10	50	nA
V_{DDQ} soft-start time	T_{SStart_Vddq}	EN2 to PG up with VPP on		2.8	3.5	ms
V_{DDQ} soft-stop time ⁽⁶⁾	T_{SStop_Vddq}			1.6		ms
V_{PP} soft-start time	T_{SStart_Vpp}	EN2 to VPP OK	0.6	0.8	1	ms
V_{PP} shutdown delay time ⁽⁶⁾	T_{dstop_VPP}	EN2 to VPP off		30		ms

ELECTRICAL CHARACTERISTICS (continued)
 $V_{IN} = 12V$, $3V3 = 3.3V$, $V_{PP_IN} = 3.3V$, $T_J = 25^{\circ}C$, $R_{MODE} = 0\Omega$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable and UVLO						
EN1 rising threshold	V_{EN1_TH}		0.54	0.59	0.64	V
EN1 hysteresis	V_{EN1_HYS}			125		mV
EN2 rising threshold	V_{EN2_TH}		1.12	1.22	1.32	V
EN2 hysteresis	V_{EN2_HYS}			125		mV
Enable input current	$I_{EN1/2}$	$V_{EN1/2} = 2V$			5	μA
		$V_{EN1/2} = 0V$			1	
VCC under-voltage lockout threshold rising	$V_{CCV_{th}}$		2.9	3.05	3.13	V
VCC under-voltage lockout threshold hysteresis	V_{CCHYS}			280		mV
VIN under-voltage lockout threshold rising	$V_{INV_{TH}}$			4.2	4.4	V
VIN under-voltage lockout threshold hysteresis	V_{INHYS}			450		mV
Power Good (PG is VPP and VDDQ)						
PG when FB_VDDQ rising (good)	PG_{FB_Rising} (Good)	V_{FB} rising, percentage of V_{FB}		95		%
PG when FB_VDDQ falling (fault)	$PG_{FB_Falling}$ (Fault)	V_{FB} falling, percentage of V_{FB}		90		
PG when FB_VDDQ rising (fault)	PG_{FB_Rising} (Fault)	V_{FB} rising, percentage of V_{FB}		115		
PG when FB_VDDQ falling (good)	$PG_{FB_Falling}$ (Good)	V_{FB} falling, percentage of V_{FB}		105		
PG when VPP rising (good)	PG_{VPP_Rising} (Good)	V_{FB} rising, percentage of V_{FB}		95		%
PG when VPP falling (fault)	$PG_{VPP_Falling}$ (Fault)	V_{FB} falling, percentage of V_{FB}		90		
PG when VPP rising (fault)	PG_{VPP_Rising} (Fault)	V_{FB} rising, percentage of V_{FB}		115		
PG when VPP falling (good)	$PG_{VPP_Falling}$ (Good)	V_{FB} falling, percentage of V_{FB}		105		
Power good low-to-high delay	PG_{Td_L2H}				20	μs
Power good high-to-low delay	PG_{Td_H2L}				50	μs
EN low to PG low delay	$PG_{Td_EN\ low}$				3	μs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V

ELECTRICAL CHARACTERISTICS (continued)
 $V_{IN} = 12V$, $3V3 = 3.3V$, $V_{PP_IN} = 3.3V$, $T_J = 25^{\circ}C$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VPP LDO						
VPP output voltage	V_{PP}		2.45	2.5	2.55	V
VPP load regulation	REG_{VPP}	$I_{PP} = 1A$	2.4			V
UVP threshold	UVP_{VPP}			1.5		V
OVP threshold	OVP_{VPP}			3.2		V
Current limit	I_{LIMIT_VPP}		1.2	1.5	1.8	A
VTTREF Output						
VTTREF output voltage	V_{TTREF}			$V_{DDQ}/2$		
Output voltage tolerance to V_{DDQ}	V_{TTREF}/V_{DDQ}	$I_{VTTREF} < 0.1mA$, $1V < V_{DDQ} < 1.5V$	48.5%	50%	51.5%	
		$I_{VTTREF} < 10mA$, $1V < V_{DDQ} < 1.5V$	48%	50%	52%	
Current limit	I_{LIMIT_VTTREF}			16		mA
VTT LDO						
VTT output voltage	V_{TT}			$V_{DDQ}/2$		
VTT tolerance to VTTREF	$V_{TT}-V_{TTREF}$	$-10mA < I_{VTT} < 10mA$, $V_{DDQ} = 1.2V$	-15		15	mV
		$-0.6A < I_{VTT} < 0.6A$, $V_{DDQ} = 1.2V$	-20		20	mV
Source current limit	I_{LIMIT_SOURCE}		1.1	1.5		A
Sink current limit	I_{LIMIT_SINK}		1.1	1.5		A
Thermal Protection						
Thermal shutdown ⁽⁶⁾	T_{SD}			150		$^{\circ}C$
Thermal shutdown hysteresis	T_{SD_HYS}			25		$^{\circ}C$

NOTES:

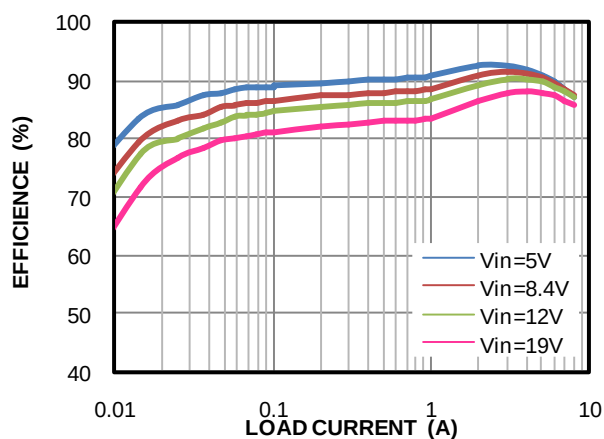
5) Based on MPS EVB test data, not tested in production.

6) Guaranteed by design.

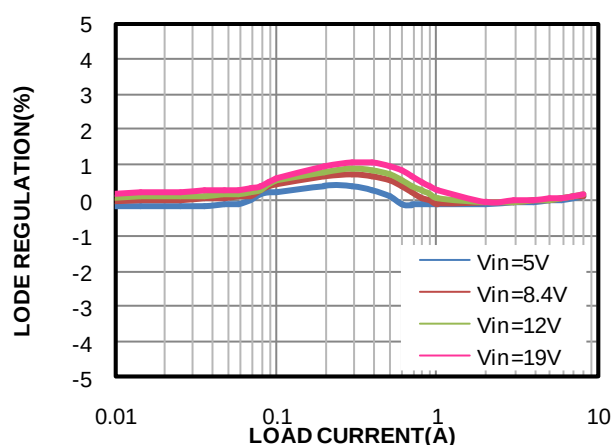
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$, $V_{DDQ} = 1.2V$, $L = 0.68\mu H/3.1m\Omega$, $F_{SW} = 700kHz$, $R_{MODE} = 0\Omega$, unless otherwise noted.

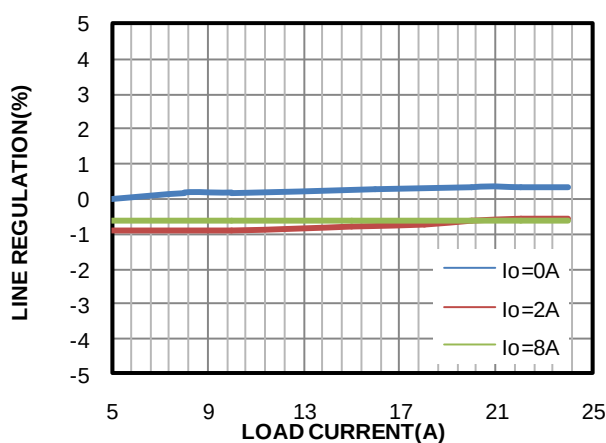
Efficiency vs. Load Current



Load Regulation vs. Load Current

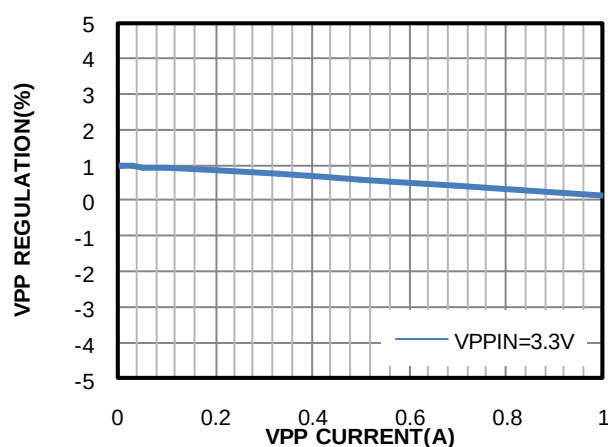


Line Regulation vs. Load Current



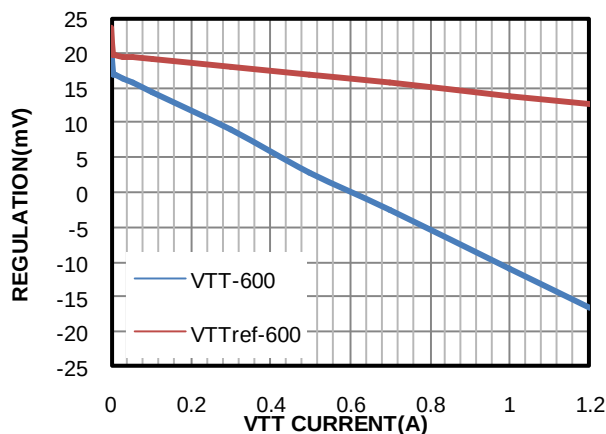
VPP Regulation

$V_{PP} = 2.5V$, $I_{OUT} = 0A$



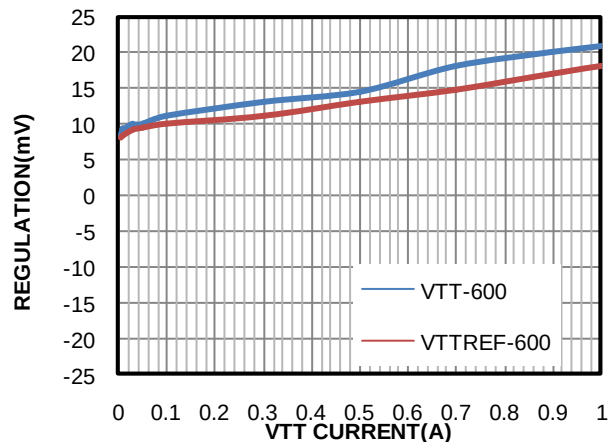
VTT Source Current

$V_{TT} = 0.6V$, $V_{TTREF} = 0.6V$, $I_{OUT} = 0A$,
 $I_{VTTREF} = 0A$

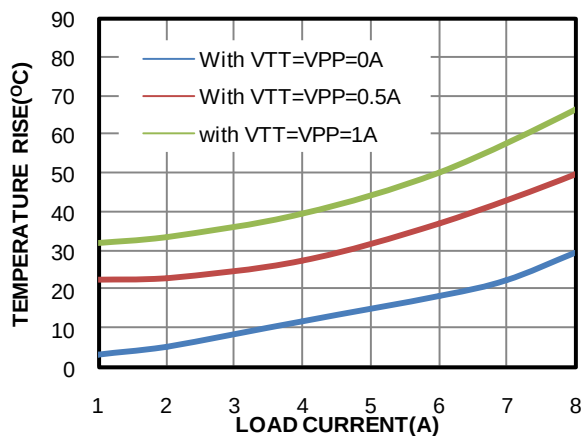
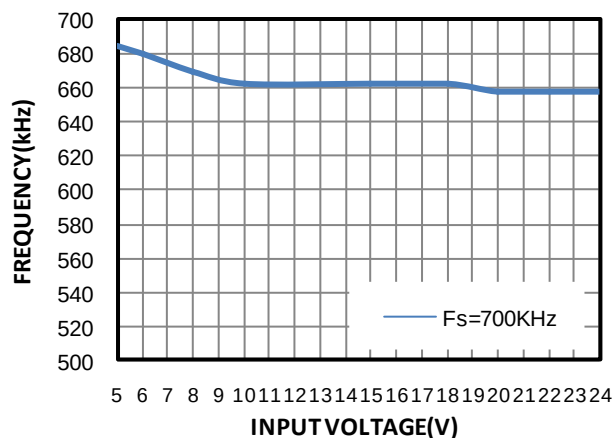
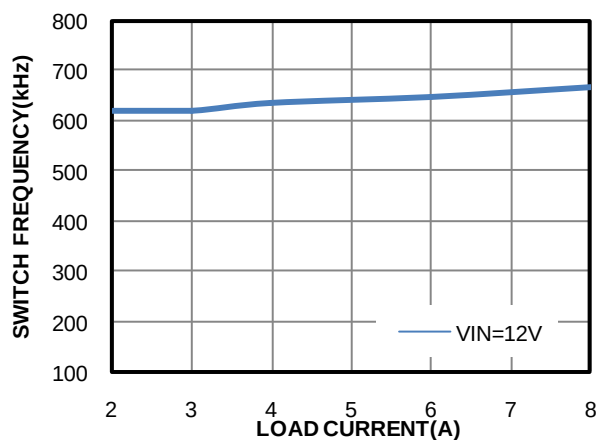


VTT Sink Current

$V_{TT} = 0.6V$, $V_{TTREF} = 0.6V$, $I_{OUT} = 0A$,
 $I_{VTTREF} = 0A$



TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = 12V$, $V_{DDQ} = 1.2V$, $L = 0.68\mu H/3.1m\Omega$, $F_{SW} = 700kHz$, $R_{MODE} = 0\Omega$, unless otherwise noted.

Temperature Rise vs. Load Current

Frequency vs. Input Voltage
 $I_{OUT} = 8A$

Switching Frequency vs. Load Current


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $L = 0.68\mu H/3.1m\Omega$, $F_{SW} = 700kHz$, $R_{MODE} = 0\Omega$, $T_J = +25^\circ C$, unless otherwise noted.

Input/Output Voltage Ripple

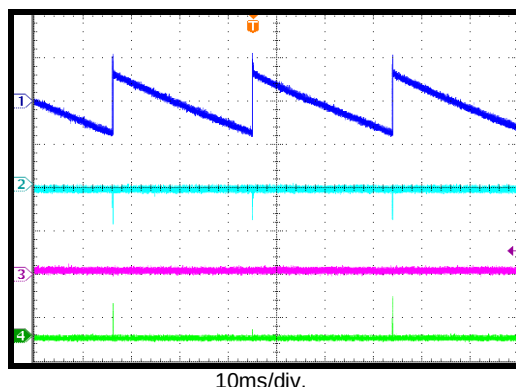
$I_{OUT} = 0A$

CH1:
 V_{OUT}/AC
20mV/div.

CH2: V_{IN}/AC
20mV/div.

CH3: V_{SW}
10V/div.

CH4: I_L
2A/div.



Input/Output Voltage Ripple

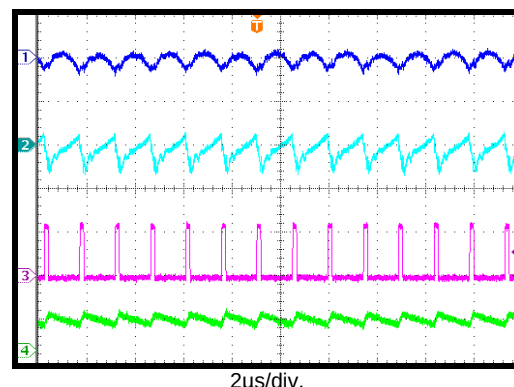
$I_{OUT} = 8A$

CH1:
 V_{OUT}/AC
20mV/div.

CH2: V_{IN}/AC
100mV/div.

CH3: V_{SW}
10V/div.

CH4: I_L
10A/div.



Power Good through VIN Start-Up

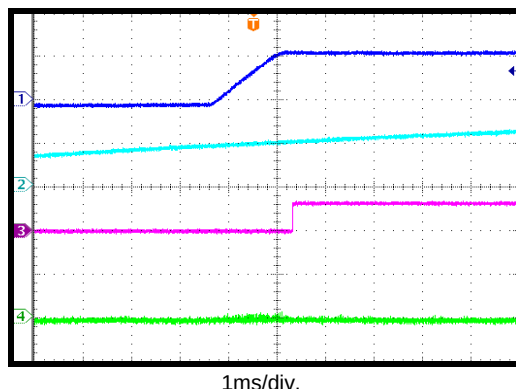
$I_{OUT} = 0A$

CH1: V_{OUT}
1V/div.

CH2: V_{IN}
5V/div.

CH3: V_{PG}
5V/div.

CH4: I_L
10A/div.



Power Good through VIN Shutdown

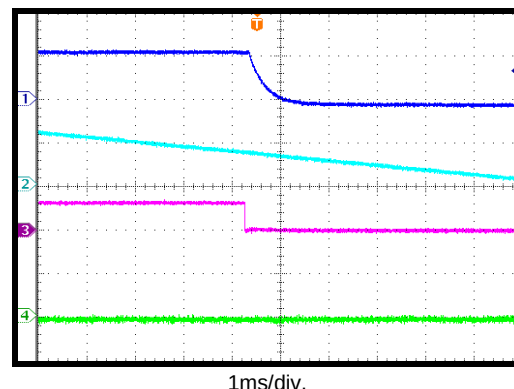
$I_{OUT} = 0A$

CH1: V_{OUT}
1V/div.

CH2: V_{IN}
5V/div.

CH3: V_{PG}
5V/div.

CH4: I_L
10A/div.



Power Good through EN2 Start-Up

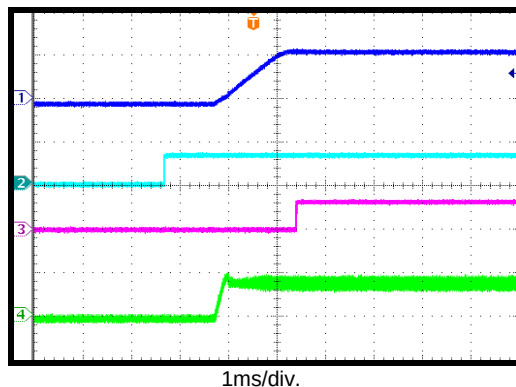
$I_{OUT} = 8A$

CH1: V_{OUT}
1V/div.

CH2: V_{EN2}
5V/div.

CH3: V_{PG}
5V/div.

CH4: I_L
10V/div.



Power Good through EN2 Shutdown

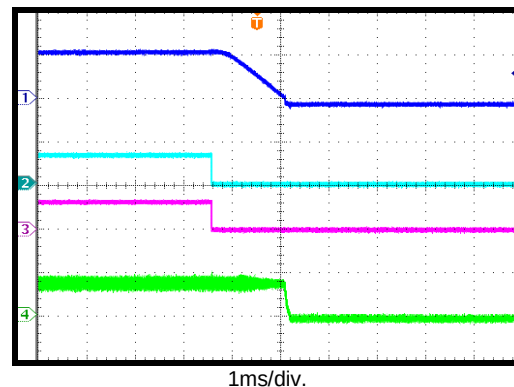
$I_{OUT} = 8A$

CH1: V_{OUT}
1V/div.

CH2: V_{EN2}
5V/div.

CH3: V_{PG}
5V/div.

CH4: I_L
10V/div.

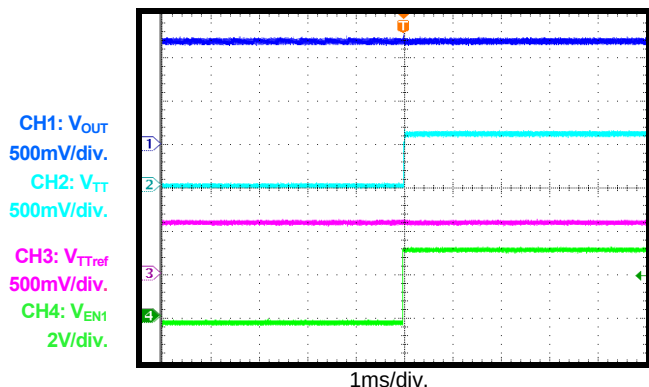


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $L = 0.68\mu H/3.1m\Omega$, $F_{SW} = 700kHz$, $R_{MODE} = 0\Omega$, $T_J = +25^\circ C$, unless otherwise noted.

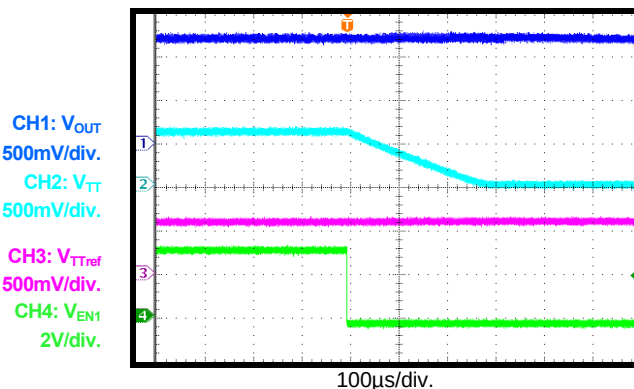
VTT Start-Up through EN1

$V_{IN} = 12V$, $I_{OUT} = 8A$, $I_{VTT} = 50mA$



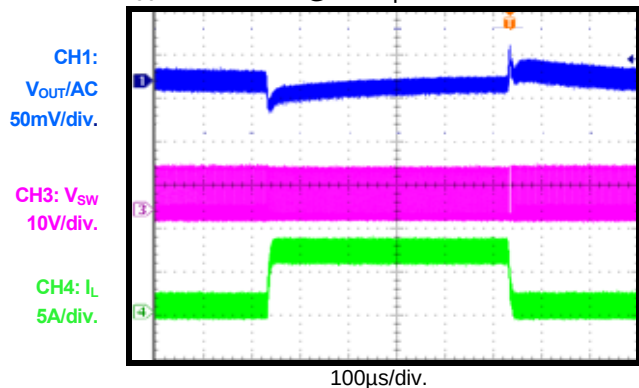
VTT Shutdown through EN1

$V_{IN} = 12V$, $I_{OUT} = 8A$, $I_{VTT} = 50mA$



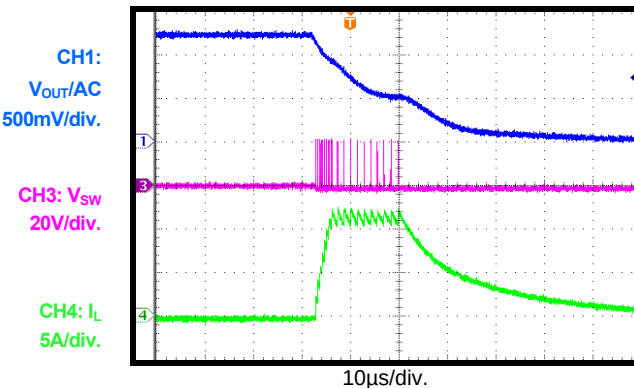
Transient

$V_{IN} = 12V$, $L = 0.68\mu H$, $C_{OUT} = 66\mu F$,
 $I_{OUT} = 0.8 - 7.2A @ 1.6A/\mu s$



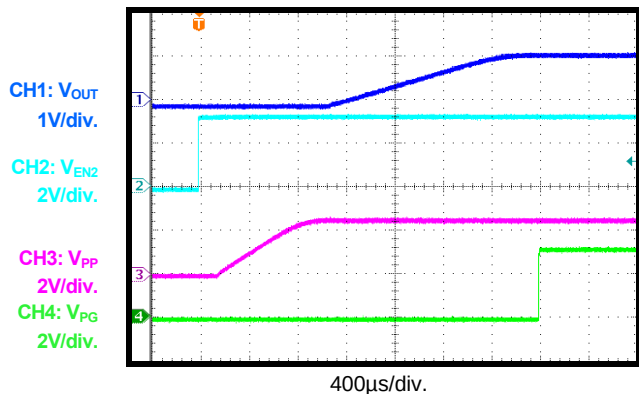
Short-Circuit Protection

$V_{IN} = 22V$



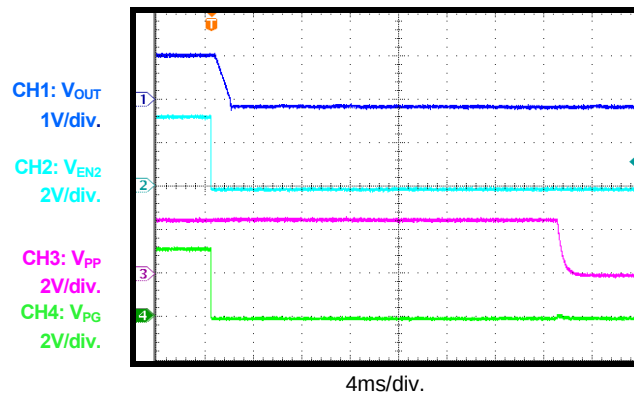
Soft Start by EN2 Start-Up

$I_{OUT} = 8A$



Soft End by EN2 Shutdown

$I_{OUT} = 8A$



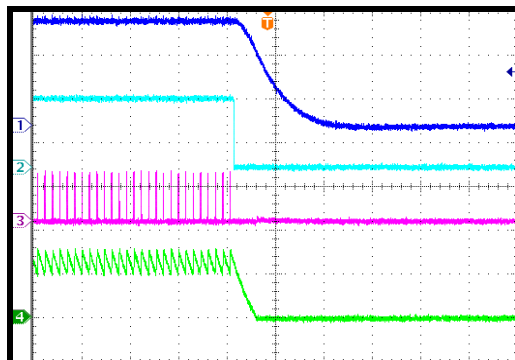
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $L = 0.68\mu H/3.1m\Omega$, $F_{SW} = 700kHz$, $R_{MODE} = 0\Omega$, $T_J = +25^\circ C$, unless otherwise noted.

Thermal Shutdown

$V_{IN} = 19V$, $I_{OUT} = 8A$

CH1: V_{OUT}
500mV/div.
CH2: V_{PG}
2V/div.
CH3: V_{SW}
20V/div.
CH4: I_L
5A/div.

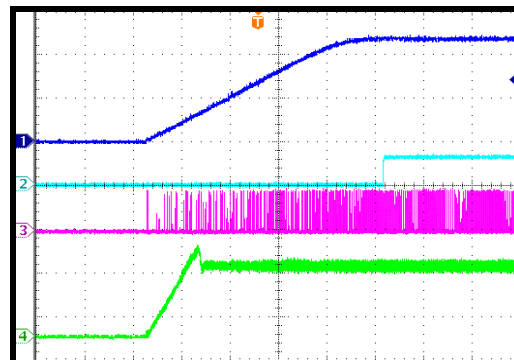


10µs/div.

Thermal Recovery

$V_{IN} = 19V$, $I_{OUT} = 8A$

CH1: V_{OUT}
500mV/div.
CH2: V_{PG}
5V/div.
CH3: V_{SW}
20V/div.
CH4: I_L
5A/div.



400µs/div.

PIN FUNCTIONS

PIN #	Name	Description
1	VIN	Supply voltage. VIN supplies power for the internal MOSFET and regulator. The NB687 operates from a +4.5V to +24V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
2	PGND	Power ground. Use wide PCB traces and multiple vias to make the connection.
3	3V3	External 3V3 VCC input for the controller and driver. Place a 1μF decoupling capacitor close to 3V3 and AGND.
4	AGND	Analog ground. The internal reference is referred to AGND. Connect GND of the FB resistor divider to AGND for better load regulation.
5	VTT	VTT LDO output. Decouple VTT with a minimum 10μF ceramic capacitor placed as close to VTT as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
6	VDDQ	Input of VTTLDO. Connect VDDQ to the output capacitor of the regulator directly with a thick trace (>100mil).
7	VTTREF	Buffered VTT reference output. Decouple VTTREF with a minimum 0.22μF ceramic capacitor placed as close to VTTREF as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
8	VPPIN	Supply voltage for VPP LDO. A 3.3V power supply is recommended. Decouple VPPIN with a minimum 22μF ceramic capacitor placed as close to VPPIN as possible. If the VPP function is not used, leave VPPIN floating.
9	SW	Switch output. Connect SW to the inductor and bootstrap capacitor. SW is connected to VIN when the HS-FET is on. SW is connected to PGND when the LS-FET is on. Use wide and short PCB traces to make the connection. Keep sensitive traces away from SW during layout.
10	BST	Bootstrap. Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
11	VPP	2.5V VPP LDO output. Decouple VPP with a minimum 47μF ceramic capacitor placed as close to VPP as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
12	PG	Power good output. PG is an open-drain signal and is high if the output voltage is within a proper range.
13	FB	Feedback. An external resistor divider from the output to GND tapped to FB sets the output voltage. Place the resistor divider as close to FB as possible. Avoid vias on the FB traces.
14	MODE	Mode pin to select the switching frequency. MODE can also set ultrasonic mode with a pull-down resistor.
15	EN2	Enable. EN1 and EN2 are digital inputs used to enable or disable the internal regulators. Once EN1 = EN2 = 1, the VDDQ regulator, VTT LDO, and VTTREF output are turned on. When EN1 = 0 and EN2 = 1, all regulators turn on except the VTT LDO. All regulators turn off when EN2 = 0 or EN1 = EN2 = 0. Do not float EN1 at any time. If the VTT LDO function is not used, tie EN1 to GND.
16	EN1	

BLOCK DIAGRAM

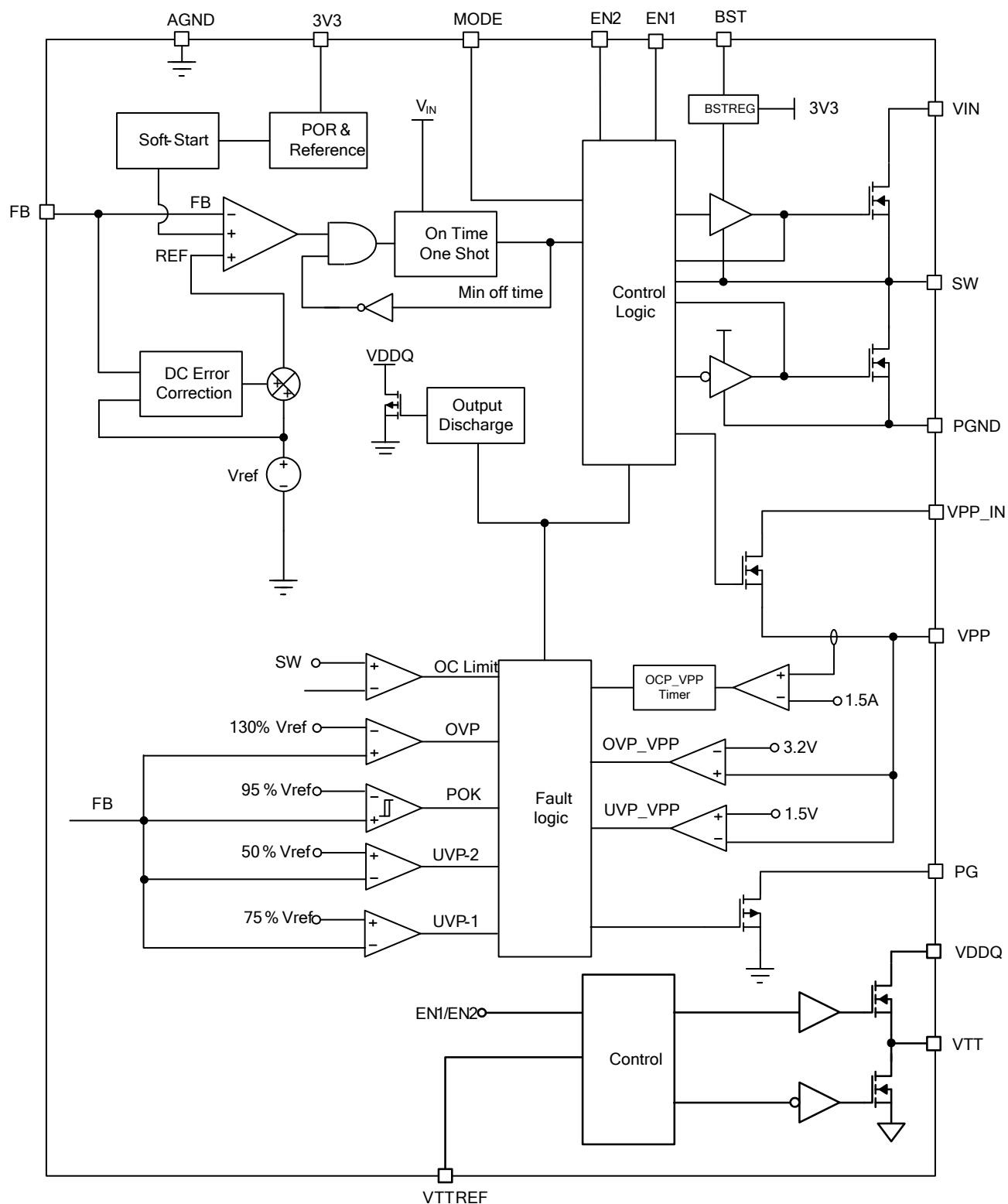


Figure 1: Functional Block Diagram

OPERATION

Pulse-Width Modulation (PWM) Operation

The NB687 is a fully integrated, synchronous, rectified, step-down, switch-mode converter with 2.5V/1A VPP and ± 1 A LDO current. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF} . By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps (see Figure 2). When V_{FB} is below V_{REF} , the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the next period begins.

In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

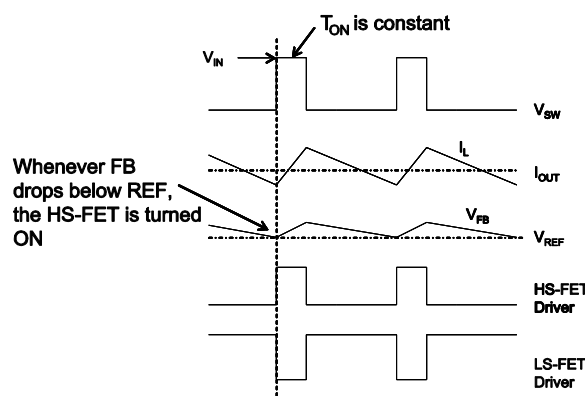


Figure 2: Heavy-Load Operation

Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load operation is shown in Figure 3. When V_{FB} is below V_{REF} , the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, V_{FB} cannot reach V_{REF} while the inductor current is approaching zero. The LS-FET driver enters tri-state (Hi-Z) whenever the inductor current reaches zero. A current modulator takes over control of the LS-FET and limits the inductor current to less than -1mA. The output capacitors discharge to GND through the LS-FET slowly. As a result, the efficiency in light-load condition is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode.

At light-load or no-load condition, the output drops very slowly, and the NB687 reduces the switching frequency naturally. High efficiency is achieved at light load.

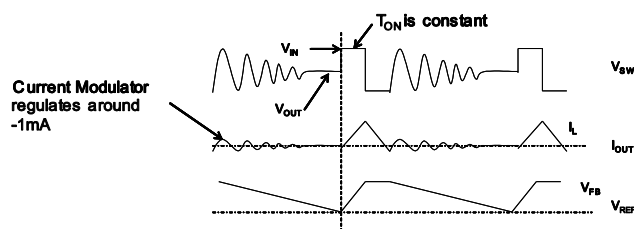


Figure 3: Light-Load Operation

As the output current increases from the light-load condition, the current modulator regulation time period becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$I_{OUT_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_S \times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Jitter and FB Ramp

Jitter occurs in both PWM and skip mode when noise in the V_{FB} ripple propagates a delay to the HS-FET driver (see Figure 4 and Figure 5). Jitter can affect system stability, with noise immunity proportional to the steepness of V_{FB} 's downward slope, so the jitter in DCM is usually larger than that in CCM. However, the V_{FB} ripple does not affect noise immunity directly.

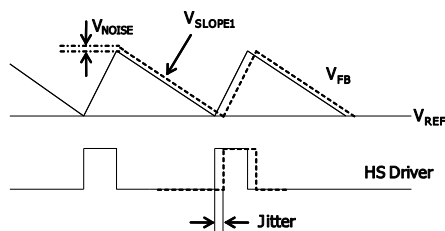


Figure 4: Jitter in PWM Mode

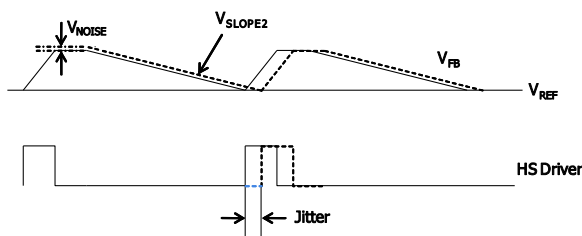


Figure 5: Jitter in Skip Mode

Operating without an External Ramp

The traditional COT control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to be an effective current-sense resistor. Ceramic capacitors cannot be used as output capacitors directly.

The NB687 has built-in internal ramp compensation to ensure that the system is stable even without the help of the output capacitor's ESR. Pure ceramic capacitor solutions can be used to reduce output ripple, total BOM cost, and board area significantly.

Figure 6 shows a typical output circuit in PWM mode without an external ramp circuit. See the Application Information section on page 21 for design steps without external compensation.

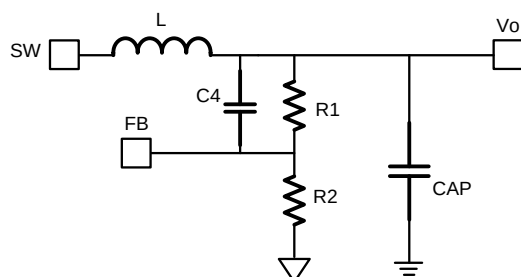


Figure 6: Simplified Output Circuit

When using a large capacitor (i.e.: OSCON) on the output, add a $>10\mu\text{F}$ ceramic capacitor in parallel to minimize the effect of the ESL.

Operating with an External Ramp

The NB687 is usually able to support ceramic output capacitors without an external ramp. However, in some cases, the internal ramp may not be enough to stabilize the system or the jitter is too big, so external ramp compensation is needed. See the Application Information section on page 21 for design steps with external ramp compensation.

VTT and VTTREF

The NB687 integrates high-performance, low-dropout linear regulators (VTT and VTTREF) to provide complete DDR3/DDR3L power solutions. VTTREF has a 10mA sink/source current capability and always tracks 1/2 of VDDQ with $\pm 1\%$ accuracy using an on-chip divider. A minimum $0.22\mu\text{F}$ ceramic capacitor must be connected close to the VTTREF terminal for stable operation.

VTT can respond quickly to track VTTREF with $\pm 30\text{mV}$ in all conditions. The current capability of the VTT regulator is up to 1A for both sink and source modes. Connect a minimum $22\mu\text{F}$ ceramic capacitor close to the VTT terminal.

VTTs should be connected to the positive node of the remote VTT output capacitor as a separated trace from the high-current line to VTT.

VPP

The NB687 integrates a high-performance, low-dropout, 2.5V linear regulator (VPP) to provide complete DDR4 power solutions. VPP has a 1A source current capability. Connect a minimum 47μF ceramic capacitor close to the VPP terminal.

Configuring the EN Control

The NB687 has two enable pins (EN1, EN2) to control the on/off function of the internal regulators. VDDQ, VTTREF, and VTT are turned on at S0 (EN1 = EN2 = high). In S3 mode (EN1 = low, EN2 = high), the VDDQ and VTTREF voltages remain on while VTT is turned off and left at a high impedance state (Hi-Z). The VTT output floats and does not sink or source a current in this state. In S4/S5 mode (EN1 = EN2 = low), all regulators are kept off and discharged to GND by a soft shutdown (see Table 1).

Table 1: EN1/EN2 Control

State	EN1	EN2	VDDQ	VPP	VTT REF	VTT
S0	High	High	On	On	On	On
S3	Low	High	On	On	On	Off (Hi-Z)
S4/S5	Low	Low	Off	Off	Off	Off
Others	High	Low	Off	Off	Off	Off

Ultrasonic Mode (USM)

Ultrasonic mode (USM) is designed to keep the switching frequency above the audible frequency area during light-load or no-load conditions. Once the part detects that both the HS-FET and LS-FET are off for about 30μs, it forces the PWM to the initial T_{ON}, so the switching frequency is out of the audible range. To keep V_{OUT} from rising too high, the NB687 shrinks T_{ON} to control V_{OUT}. If FB is still too high after shrinking T_{ON} to the minimum value, the output discharge function is activated and keeps V_{OUT} in a reasonable range. USM can be selected with MODE.

MODE Selection

The NB687 implements a mode pin (MODE) for multiple applications for USM and switching frequency selection. USM and the switching frequency can be selected by different resistors on the 3V3 logic MODE pin. There are four modes that can be selected for normal applications with external resistors (see Table 2). It is recommend to use a 1% accuracy resistor.

Table 2: Mode Selection

State	USM	Fs	Resistor to GND
M1	No	700kHz	0Hz
M2	Yes	700kHz	90kHz
M3	No	500kHz	150kHz
M4	Yes	500kHz	>230kHz or float

Power Good (PG)

The NB687 uses a power-good (PG) output to indicate whether the output voltage of the VDDQ regulator is ready or not. PG is the open drain of a MOSFET and should be connected to V_{CC} or another voltage source through a resistor (e.g.: 100kΩ). After the input voltage is applied, the MOSFET is turned on, so PG is pulled to GND before SS is ready. After both the FB and VPP voltages reach 95% of V_{REF}, PG is pulled high after a delay time (within 10μs). When the FB or VPP voltage drops to 90% of V_{REF}, PG is pulled low.

During start-up, PG is OK only when both VPP and VDDQ rise to the target. If VPP or VDDQ fault at any time, PG must be pulled low.

Soft Start (SS)

The NB687 employs a soft-start (SS) mechanism to ensure a smooth output during power-up. When EN rises high, the internal reference voltage ramps up gradually, and the output voltage ramps up smoothly as well. Once the reference voltage reaches the target value, the soft start finishes, and the device enters steady-state operation (see Figure 7).

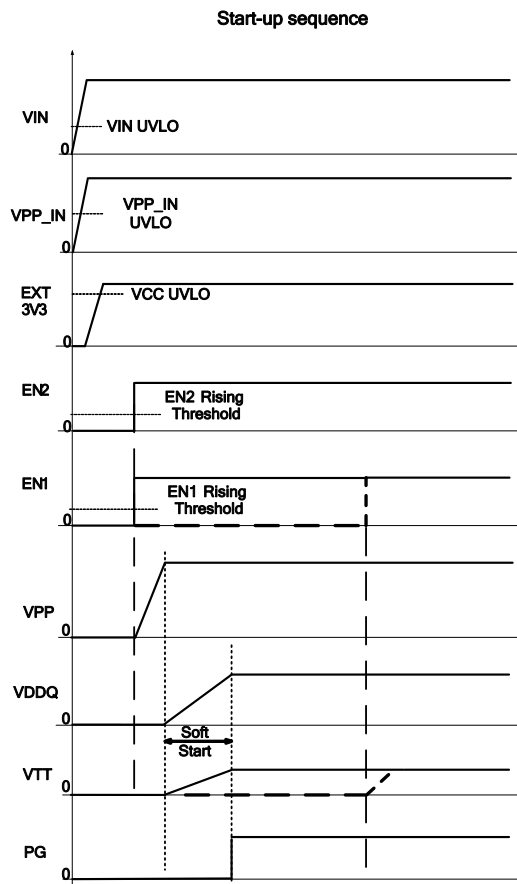


Figure 7: Start-Up Power Sequence

If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

Soft Shutdown

The NB687 employs a soft shutdown mechanism for DDR to ensure that VTTREF and VTT follow exactly half of VDDQ. When EN2 is low, the internal reference ramps down gradually, so the output voltage falls linearly. VDDQ starts to drop within 200µs of EN2 dropping down. VPP turns off after a 30ms delay (see Figure 8).

VPP

The NB687 integrates a high-performance, low-dropout, 2.5V, linear regulator (VPP) to provide complete DDR4 power solutions. VPP has a 1A source current capability. Connect a minimum 47µF ceramic capacitor close to the VPP terminal.

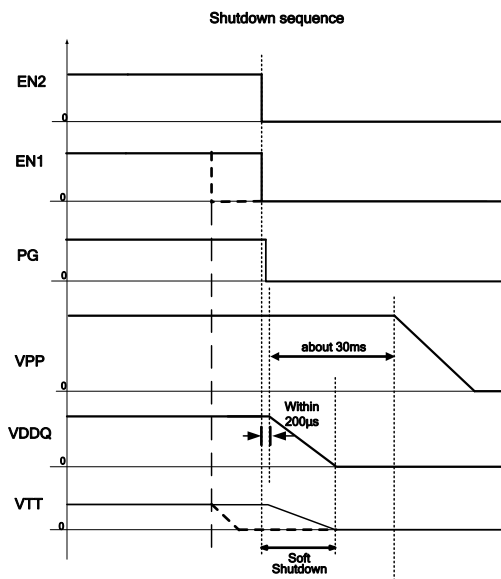


Figure 8: Soft-Shutdown Sequence

VDDQ Over-Current Limit (OCL)

The NB687 has a cycle-by-cycle over-current limiting control (OCL). The current-limit circuit employs a valley current-sensing algorithm. The part uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, PWM is not allowed to initiate a new cycle, even if FB is lower than REF (see Figure 9).

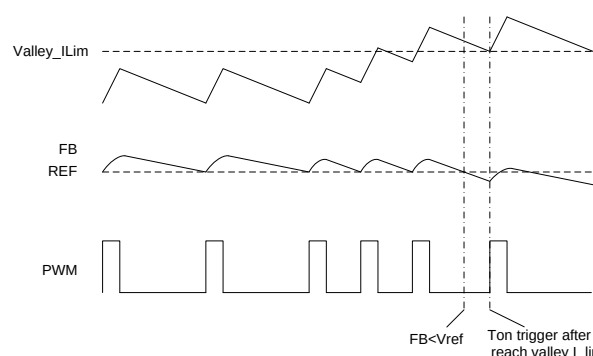


Figure 9: Valley Current-Limit Control

Since the comparison is done during the LS-FET on state, the OC trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (I_{OC}) can be calculated with Equation (2):

$$I_{OC} = I_{limit} + \frac{\Delta I_{inductor}}{2} \quad (2)$$

The OCL itself limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor, causing the output voltage to fall off. Eventually, the current crosses the under-voltage protection (UVP) threshold and latches off. Fault latching can be reset by EN going low or cycling the power of VIN.

VPP Over-Current Protection (OCP) and Over-/Under-Voltage Protection (OVP, UVP)

The VPP LDO has an internally fixed current limit for source operation. The part latches off if the current limit comparator has been on for 200 μ s.

When the VPP voltage goes higher than 3.2V, the over-voltage protection (OVP) comparator output goes high, and the part latches off directly after the comparator and logic delay.

When the VPP voltage drops below 1.5V, the under-voltage protection (UVP) comparator output goes high, and the part latches off directly after the comparator and logic delay.

VTT/VTTREF Over-Current Protection (OCP)

The VTT LDO has an internal, non-latched, fixed current limit of 1.5A for both sink and source operation. Once the current limit is reached, it adjusts the gate of the sink/source MOSFET to limit the current. VTTREF also has an internal, non-latched, 16mA current limit.

VDDQ OVP/UVP

The NB687 monitors a resistor-divided feedback voltage to detect over- and under-voltage (OV, UV). When the feedback voltage rises higher than 130% of the target voltage and the OVP comparator output goes high, and the circuit latches. The HS-FET driver turns off, and the LS-FET turns on, acting as a -2A current source.

To protect the part from damage, there is an absolute 3.6V OVP on VOUT. VOUT latches off once it reaches this value. The LS-FET acts the same as 130% OVP.

When V_{FB} is lower than 75% of V_{REF} but higher than 50%, the UVP-1 comparator output goes high. The part latches if V_{FB} remains in this range for about 32 μ s (latches the HS-FET off

and LS-FET on). The LS-FET remains on until the inductor current drops to zero. During this period, the valley current limit helps control the inductor current.

When the feedback voltage is lower than 50% of V_{REF} , the UVP-2 comparator output goes high, and the part latches off directly after the comparator and logic delay (latches the HS-FET off and LS-FET on). The LS-FET remains on until the inductor current drops to zero. Fault latching can be reset by EN going low or cycling the power of VIN.

Under-Voltage Lockout (UVLO) Protection

The NB687 has two under-voltage lockout (UVLO) protections: 3.05V VCC UVLO and 4.2V VIN UVLO. The part starts up only when both VCC and VIN exceed their own UVLO thresholds. The part shuts down when either the VCC voltage is lower than the UVLO falling threshold voltage (typically 2.8V) or VIN is lower than the 3.75V falling threshold. Both UVLO protections are non-latch off.

If an application requires a higher UVLO, use EN2 to adjust the input voltage UVLO by using two external resistors (see Figure 10).

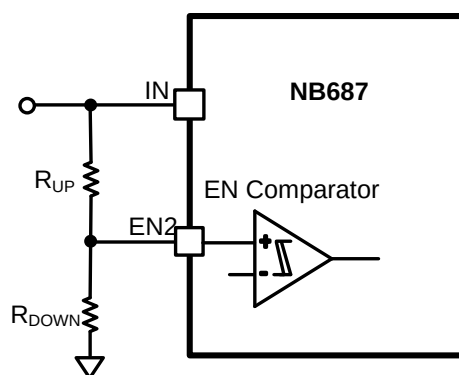


Figure 10: Adjustable UVLO

Thermal Shutdown

Thermal shutdown is employed in the NB687. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is a non-latched protection. There is a hysteresis of about 25°C. Once the junction temperature drops to about 125°C, a soft start is initiated.

Output Discharge

The NB687 discharges all outputs, including VDDQ, VTTREF, VTT, and VPP when the controller is turned off by a protection function (UVP, OCP, OVP, UVLO, or thermal shutdown). The discharge resistor on VDDQ is typically 3Ω. Note that the output discharge is not active during soft shutdown.

APPLICATION INFORMATION

Setting the Output Voltage with No External Ramp

The NB687 does not need ramp compensation for applications where POSCAP or ceramic capacitors are set as output capacitors. The output voltage is set by feedback resistors (R1 and R2) (see Figure 11).

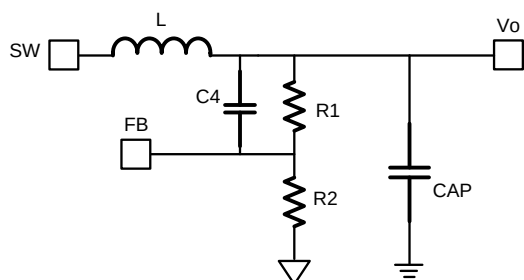


Figure 11: Simplified Circuit without External Ramp

First, choose a value for R2. R2 should be chosen reasonably, since a small R2 leads to considerable quiescent current loss, while a large R2 makes FB noise-sensitive. R2 is recommended to be between 5 - 50kΩ, using a comparatively larger R2 when V_{OUT} is low and a smaller R2 when V_{OUT} is high. Considering the output ripple, determine R1 with Equation (3):

$$R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \cdot R_2 \quad (3)$$

C4 acting as a feed-forward capacitor improves the transient and can be set in the range of 100pF - 1nF. A larger C4 leads to better transient but more noise sensitivity.

Setting the Output Voltage with an External Ramp

If the system is not stable enough or the jitter is too large when a ceramic capacitor is used in the output, an external voltage ramp should be added to FB through a resistor (R4) and capacitor (C4). Since there is already an internal ramp added in the system, a 1MΩ (R4), 220pF (C4) ramp is enough for the ramp, typically.

The output voltage is influenced by R4 in addition to the R1 and R2 divider (see Figure 12).

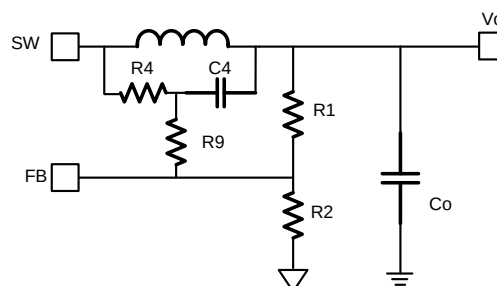


Figure 12: Simplified Circuit with External Ramp

R2 should be chosen reasonably, since a small R2 leads to considerable quiescent current loss, while a large R2 makes FB noise-sensitive. R2 is recommended to be between 5 - 50kΩ, using a comparatively larger R2 when V_{OUT} is low and a smaller R2 when V_{OUT} is high. Determine the value of R1 with Equation (4):

$$R_1 = \frac{1}{\frac{V_{REF}}{V_{OUT} - V_{REF}} - \frac{R_2}{R_4}} \cdot R_2 \quad (4)$$

Usually, R9 is set to 0Ω. To set a pole for better noise immunity, R9 can also be set using Equation (5):

$$R_9 = \frac{1}{2\pi \times C_4 \times 2F_{SW}} \quad (5)$$

It is recommended to set R9 to be in the range of 100Ω to 1kΩ to reduce its influence on the ramp.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For the best performance, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (6):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (9):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (9)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \quad (10)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

The output voltage ripple caused by the ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through a resistor (R4) and capacitor (C4).

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR dominates the output ripple. The output ripple can be approximated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

The maximum output capacitor limitation should also be considered in the design application. The NB687 has a soft-start time period around 1.6ms. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time and fails to regulate. The maximum output capacitor value (C_{O_max}) can be limited approximately with Equation (13):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{SS} / V_{OUT} \quad (13)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and T_{SS} is the soft-start time.

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and lower output ripple voltage but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30 - 50% of the maximum output current and keep the peak inductor current below the maximum switch current limit. The inductance value can be calculated with Equation (14):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (14)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, including short current, so I_{SAT} should be greater than 13A.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A four-layer layout is strongly recommended for better thermal performance. For best results, refer to Figure 13 and follow the guidelines below.

1. Keep the VDDQ trace width >100mil to prevent a voltage drop on the input of VTTLDO.
2. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
3. Place the input capacitors as close to VIN and GND as possible.
4. Place the decoupling capacitor as close to VCC and GND as possible.
5. Keep the switching node (SW) short and away from the feedback network.
6. Place the external feedback resistors next to FB.
7. Ensure that there is no via on the FB trace.
8. Keep the BST voltage path (BST, C3, and SW) as short as possible.
9. Keep the VDDQ trace >100mil and as short as possible since it also acts as the power-in of the LDO input.
10. Keep the VIN and GND pads connected with large coppers to achieve better thermal performance.
11. Add several vias with 10mil_drill/18mil_copper_width close to the VIN and GND pads to help with thermal dissipation.

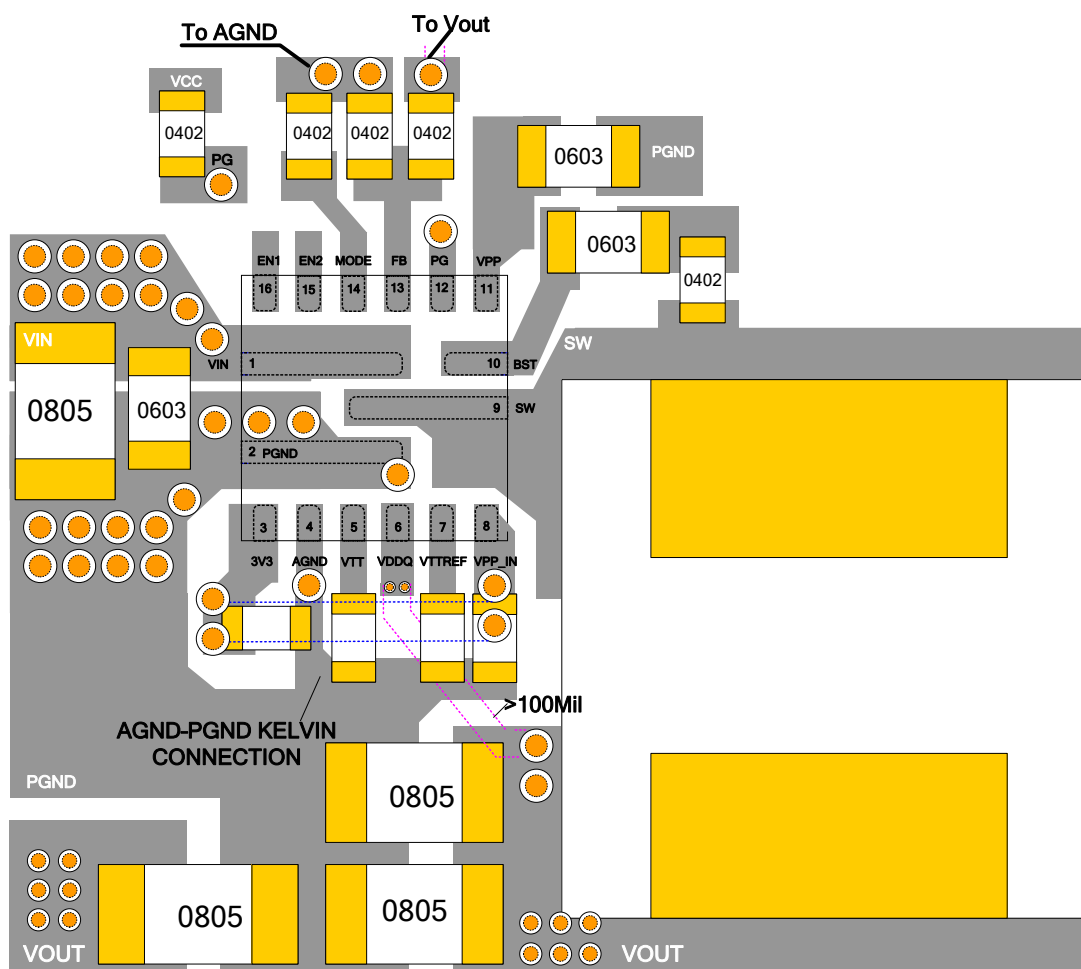


Figure 13: Recommended Layout

Design Example

For applications that require a current over 10A, it is recommend to add a 500kHz f_{sw} for better thermal and efficiency.

The NB687 also supports non-DDR applications with very compact external components.

Table 3 and Table 4 show design examples when ceramic capacitors are applied.

Table 4: Design Example for 700kHz F_{sw}

V_{OUT} (V)	C_{OUT} (F)	L (μ H)	R_{MODE} (Ω)	C4 (pF)	R1 (k Ω)	R2 (k Ω)
1.0	22 μ x3	0.68	0	220	13.3	20
1.2	22 μ x3	0.68	0	220	20	20
1.35	22 μ x3	0.68	0	220	28	22.1
1.5	22 μ x4	1.0	0	220	30.1	20
1.8	22 μ x4	1.0	0	220	40.2	20

Table 3: Design Example for 500kHz F_{sw}

V_{OUT} (V)	C_{OUT} (F)	L (μ H)	R_{MODE} (Ω)	C4 (pF)	R1 (k Ω)	R2 (k Ω)
1.0	22 μ x4	0.68	150k	220	13.3	20
1.2	22 μ x4	1.0	150k	220	20	20
1.35	22 μ x4	1.0	150k	220	28	22.1
1.5	22 μ x5	1.0	150k	220	30.1	20
1.8	22 μ x5	1.5	150k	220	40.2	20

TYPICAL APPLICATION

DDR4 Application

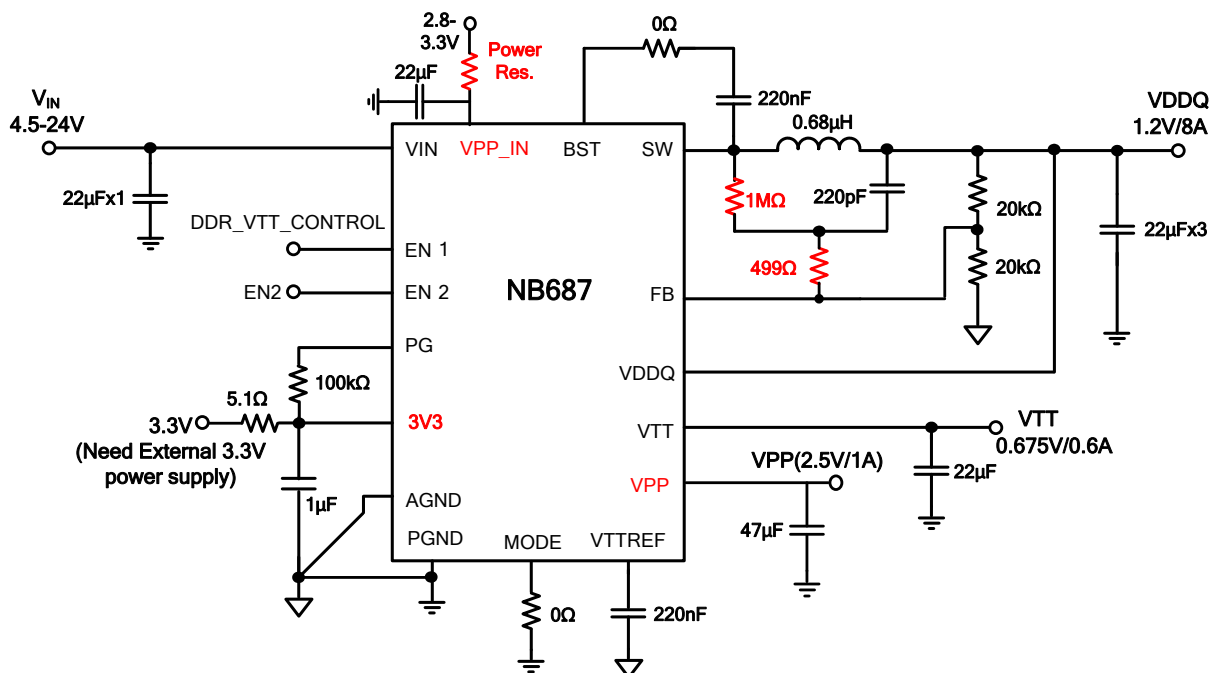


Figure 14: Typical DDR4 Application Circuit, $V_{IN} = 4.5 - 24V$, $V_{OUT} = 1.2V$, $I_{OUT} = 8A$, with VTT, $F_{SW} = 700kHz$

DDR3 Application

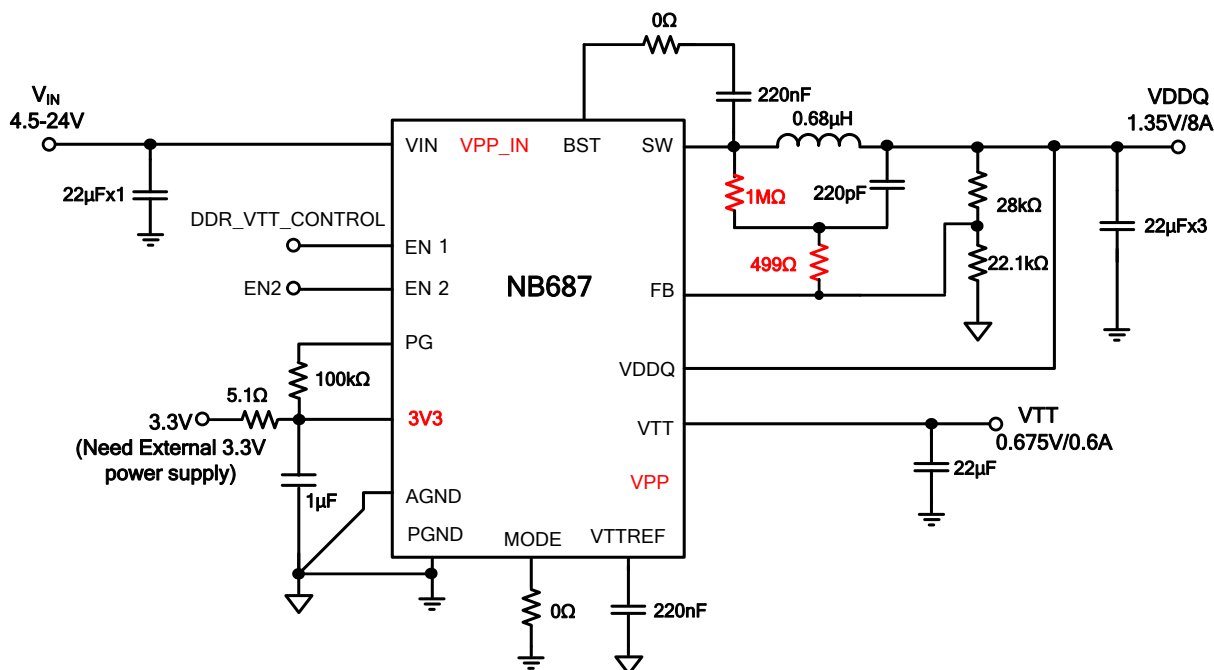
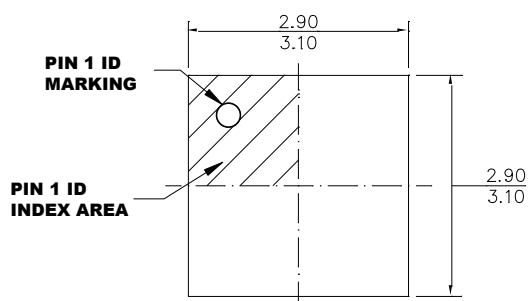


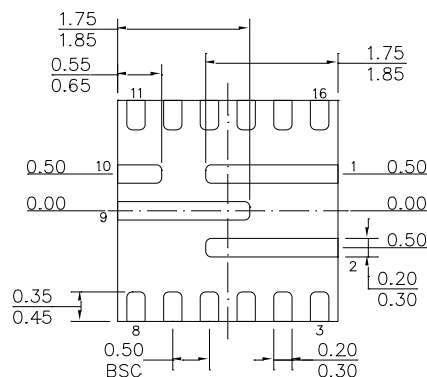
Figure 15: Typical DDR3L Application Circuit, $V_{IN} = 4.5 - 24V$, $V_{OUT} = 1.35V$, $I_{OUT} = 8A$, without VPP, $F_{SW} = 700kHz$

PACKAGE INFORMATION

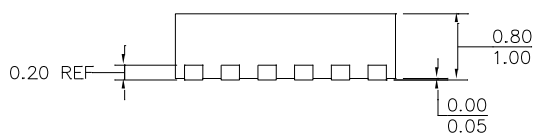
QFN-16 (3mmx3mm)



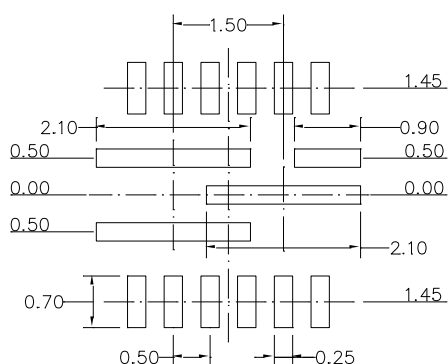
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

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